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A Compact Current–Voltage Model for 2-D-Semiconductor-Based Lateral Homo-/Hetero-Junction Tunnel-FETs

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***Abstract*— A fully analytical surface potential and current–voltage model is presented for the first time for both lateral homojunction (HMJ) and heterojunction (HTJ) tunneling-field-effect transistors (TFETs) based on 2-D semiconducting channel materials. The dynamic gate-modulated electrostatic potential at the source/channel tunneling junction is suitably captured by solving a quasi-2-D Poisson's equation in both source and channel. Subsequently, the band-to-band tunneling current is accurately derived starting from the Landauer's equation by integrating over all possible carrier energies (or wavevectors) over which tunneling is possible. The model employs Fermi–Dirac statistics in both the degenerate source and drain to compute the surface potential and net current, which yields more physical results than the commonly employed Boltzmann statistics. Its use in Landauer's approach for evaluating the net ON-current leads to an analytical model of the TFET, which physically guarantees zero drain current at zero drain–source bias. Input and output characteristics for both HMJ and HTJ TFETs are computed and compared against rigorous nonequilibrium Green's function (NEGF) simulations for different device parameters to prove the veracity of the model, and the match has been found to be excellent up to ultrashort channel length of 5 nm.**

***Index Terms*— 2-D materials, 2-D semiconductors, band-to-band tunneling, compact modeling, heterojunction (HTJ), low-power, nonequilibrium Green's function (NEGF), quantum device, steep-slope transistor, tunneling field-effect transistor (TFET), van der Waals heterostructures.**

I. Introduction

STEEP-SLOPE (or sub-*kT/q*) transistors are desirable for simultaneous supply-voltage or power scaling along with dimensional scaling, which is not feasible in nanoscale MOSFETs because of their Boltzmann-limited minimum subthreshold swing (SS) of 60 mV/decade at room temperature, and constitutes a major concern for their scalability into the sub-10 nm regime [1], [2]. Among the several sub-*kT/q* switches proposed to overcome this fundamental barrier, tunneling field-effect transistors (TFETs) have emerged as the most promising devices [3], [4]. However, TFETs fabricated from conventional 3-D materials like Si, Ge, and III–V compounds, exhibit either low ON-current, or a steep SS (i.e., SS $<$ 60 mV/decade) only at very low current values, because of their nonoptimal electrostatics and presence of interface traps [5]–[7]. These nonidealities that are detrimental to TFET performance can be significantly alleviated by using 2-D-materials, which, owing to their ultrathin body, relatively large bandgap, and pristine interfaces [8]–[10], provide excellent electrostatics and lead to low OFF-current and steep SS, as theoretically suggested in [11]–[13]. Moreover, the strong suppression of the density of states (DOS) into the bandgap of any 2-D material, commonly known as the *band-tail*, results in very steep SS for various 2-D–2-D and 3-D–2-D source/channel heterostructures [14], as was experimentally demonstrated in [15] using a degenerately doped 3-D (Ge) source and 2-D (MoS_2) channel vertical heterojunction (HTJ) TFET, where a minimum SS of 3.9 mV/decade and an average SS of $\sim$31 mV/decade over four orders of the drain current was observed for the first time albeit with very low ON-current, which limits its applicability in practical circuits. Among the several novel solutions proposed to overcome the typical low ON-currents in TFETs [16]–[18], 2-D semiconductor-based lateral HTJ TFETs introduced in [16] are the most attractive because their tunneling barrier heights can be made small by appropriately selecting the band overlap of source/channel materials and due to their atomic-scale tunneling barrier widths, which ultimately determines the ON-current. First principle transport studies in [16] have shown that the ON-current of 2-D lateral HTJ TFETs can be substantially higher than that for the 2-D lateral homojunction (HMJ) TFET or the 2-D-channel based vertical HTJ TFETs. Moreover, 2-D lateral-HTJ TFETs can achieve the smallest SS_{min} values compared to any other 2-D-channel based TFETs [14]. Hence, the wide gamut of 2-D materials available provides

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additional motivation to pursue 2-D source-channel lateral-HTJ TFETs for future low-power/energy-efficient electronics. Also, recent experimental breakthroughs on the fabrication of lateral HTJs of 2-D semiconductors [19] and doping of 2-D materials [20] has made fabrication of 2-D lateral-HTJ TFETs feasible.

In general, 2-D TFETs, owing to their ultralow leakage and superior performance, could be ideal for building next-generation ultralow-power electronics such as brain-inspired neuromorphic circuits [21]. 2-D-TFETs can also be employed for building a revolutionary new class of bio/gas sensors [8] due to their combined advantages of high sensitivity arising from their steep SS [22] and the atomically thin and pristine channel of the 2-D semiconductors with sizable bandgaps [8]. Hence, it is opportune to examine the prospects of 2-D lateral-HTJ TFETs for exploring various circuits, including low-power sensors, neuromorphic computing circuits, and other low-power integrated circuits. However, to study the behavior of these devices in circuits, we need to develop their compact models for accurate and fast simulations and carry out various design optimizations. There have been studies on the modeling of both HMJ and HTJ TFETs fabricated on bulk semiconductors [23]–[33], but only a few based on 2-D materials [34]–[36]. Moreover, most of these models [24], [28], [29], [32], [34], [35] are numerical, or do not model the source and drain Fermi degeneracy [23]–[27], [31]–[33], [36], or the drain bias dependence [24], [29], [32], [36] and cannot physically model zero drain current at zero drain–source bias [18], [23]–[27], [29], [31], [32]. Essentially, the incorporation of Kane's band-to-band tunneling model in [18], [24]–[27], [29], [31], [32], which predicts a nonzero tunneling carrier generation rate even at zero drain–source bias (due to presence of a nonzero electric field at source-channel junction), and an implicit assumption of fully occupied valence and fully empty conduction band [37] is what makes physically modeling zero drain current at zero drain bias unfeasible. Nevertheless, the inclusion of all the above-mentioned effects is critical in designing an accurate compact model, which will be useful for designing various circuits and predicting the performance of the 2-D TFETs in circuit operation. At present, a physically consistent, fully analytical model, which accounts for both the drain and gate bias dependence of drain current for both lateral- HMJ and HTJ TFETs, fabricated on 2-D materials is lacking, and that is what this article intends to address.

This article, therefore, starts by describing the device structure and the basic operation in detail (Section II), developing its analytical surface potential model by solving the pseudo-2-D Poisson's equation in both source and channel (Section III) to extract the energy band diagram, which is then applied to the analytically developed band-to-band tunneling current model (Section IV) to yield the drain–source current. Finally, conclusions are drawn in Section V.

II. Device Structure

A generic 2-D-semiconductor-channel double-gate (DG) n-type TFET device under consideration is shown in Fig. 1(a), and the device cross section under a certain bias is shown in Fig. 1(b) where the source depletion region, the fringing electric-field lines, and the device dimensions are shown.

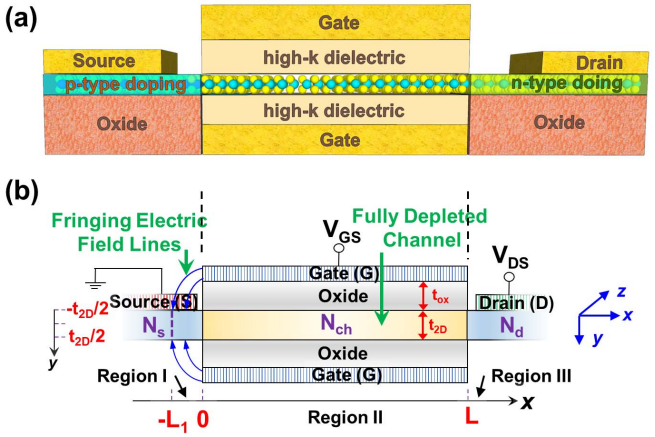

Fig. 1. (a) Cross-sectional view of the DG 2-D n-TFET. The source is strongly p-doped, the channel intrinsic or slightly n-doped, and the drain strongly n-type doped. (b) Cross section of the device under operation at a certain bias showing the fringing electric field lines from the gate terminating in the source, the fully depleted channel, and the profile of the source depletion region. The channel length of the device is L, L_1 refers to the source depletion length, t_{2D} is the thickness of the 2-D channel, while t_{ox} is the gate oxide thickness. The source, channel, and drain dopings are denoted by N_s, N_{ch}, and N_d, respectively. The source is grounded, and a voltage of V_{GS} and V_{DS} are applied to the gate and drain terminal, respectively. The direction of transport is along the x-axis, y-axis represents the confined direction along the two gates, and z-axis is along the direction of the transistor width.

As shown in Fig. 1(a), the source, channel and drain are made of 2-D semiconductor material. The lateral source-channel junction is either an HMJ or an HTJ, while the channel-drain junction is an HMJ. In this work, we discuss the behavior of an n-TFET, and therefore, the source is heavily doped p-type and the drain is heavily doped n-type [4]; while the channel is assumed to be intrinsic, or slightly n-doped. The requirement on the degenerate source and drain doping necessitate the consideration of Fermi–Dirac (FD) statistics to correctly account for the carrier distribution, over the more widely used Boltzmann distribution [see Fig. 2(a)]. Application of a positive gate-bias lowers the energy bands in the channel, which under sufficient applied bias causes the channel conduction band to overlap with that of the source valence band, allowing an appreciable number of carriers to tunnel, thereby constituting an ON-current [see Fig. 2(b)]. The use of an HTJ reduces the gate bias required to achieve this overlap of bands, thereby delivering more current at a particular gate bias. For designing an effective source-channel HTJ, both the conduction and valence bands in the source should be higher than the corresponding ones in the channel, as indicated in Fig. 2(b). However, too big an offset (broken gap – top sketch in [see Fig. 2(c)] will cause tunneling to take place even at negative gate-biases, and not form a good TFET. Therefore, in this work, we only consider staggered HTJs [bottom sketch in Fig. 2(c)].

III. Surface Potential Model

In this section we derive the surface potential model for the device. For a moderate gate–source voltage applied, it is

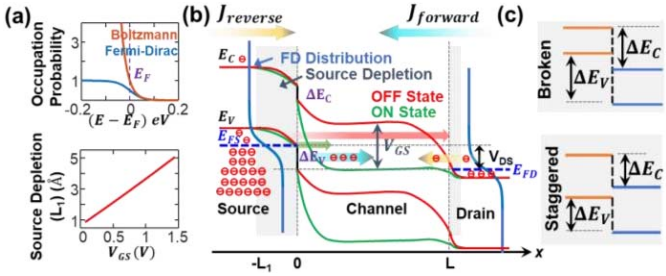

Fig. 2. (a) Comparison of FD and Boltzmann distribution as a function of energy, showing the inaccuracy of the latter in estimating carrier distribution (top) at energies $E < E_F$, the simulated source depletion length of a lateral 2-D-TFET as a function of the applied V_{GS} (bottom). (b) Sketch of the energy bands [conduction band (E_C), valence band (E_V)], source (E_{FS}) and drain (E_{FD}) Fermi levels showing an enhanced source depletion length (L_1) and the OFF- and ON-state of the device under the application of a certain V_{GS}. The electron distribution is shown in the p^+-doped source showing how the FD tail filtering gives rise to sub-60 SS. Also shown are the forward (flowing from drain to source) and reverse (flowing from source–drain) tunneling currents, the magnitude of which are determined by the position of the source and drain Fermi levels, respectively. (c) Schematic of the broken and staggered band-alignments at a HTJ showing band-offsets of ΔE_C and ΔE_V.

reasonable to assume that the entire ultrathin channel and only a small part of the source (Fig. 2(a), because of its high doping) is fully depleted. Under such a condition, the cross-sectional view of the device is illustrated in Fig. 1(b), where we show the source depletion region (Region I), the fully depleted channel (Region II), and the drain (Region III). The extreme thinness of the 2-D body causes a negligible voltage to drop across it, and therefore, the source depletion profile can be assumed to be uniform, up to a length of L_1. Also, note that although under the application of a strong positive gate bias, the part of the channel closer to the drain can be accumulated with electrons [23], we do not consider this in our model because 2-D TFETs are meant for low power operation, and therefore, the channel can be assumed to be depleted for all practical gate biases.

A. Solution for the Surface Potential

The surface potential solution is obtained by solving the pseudo-2-D Poisson's equation in both the source and the channel and using suitable boundary conditions in Fig. 1(b). The Poisson's equation modeling the potential in the depleted source can be written as

$$\frac{d^2\varphi_S(x,y)}{dx^2} + \frac{d^2\varphi_S(x,y)}{dy^2} = -\frac{qN_s}{\varepsilon_s} \tag{1}$$

where $\varphi_S(x,y)$ is the source potential, q is the electronic charge, ε_s is the permittivity of the source material, and N_s is the source doping. The solution of (1) is achieved using the parabolic approximation method [32] with the intrinsic Fermi level of the source as the reference. Gauss's law is applied to the top and bottom surfaces, while equating the vertical electric field to zero at $y = 0$ (because of symmetry). In addition, a gate-insulator effective thickness of $\pi t_{ox}/2$ is assumed (because of fringing electric field) [18], which leads to the following solution of the surface potential in the source (φ_s), evaluated at $y = \pm t_{2D}/2$:

$$\varphi_s = d_1 \sinh(\beta_1 x) + d_2 \sinh[\beta_1(x + L_1)] + V_{GS} - V_{FBS} - q\pi N_s t_{2D}/(4C_{ox}) \tag{2}$$

where d_1 and d_2 are constants of integration, L_1 is the source depletion length (to be evaluated), $V_{FBS} = [\varphi_m - (\chi_s + E_{GS}/2)]/q$ is the flat-band voltage of the source with respect to gate (χ_s and E_{GS} are the electron affinity and bandgap of the source, respectively, and φ_m is the metal work-function), $C_{ox} = \varepsilon_{ox}/t_{ox}$ (ε_{ox} is the permittivity of the gate insulator) is the insulator capacitance per unit area, and $\beta_1 = \sqrt{(4C_{ox})/(\pi\varepsilon_s t_{2D})}$.

Similarly, with the source intrinsic Fermi level as the reference, assuming full depletion of the channel, the 2-D Poisson's equation in the channel can be written as

$$\frac{d^2\varphi_{CH}(x,y)}{dx^2} + \frac{d^2\varphi_{CH}(x,y)}{dy^2} = \frac{qN_{ch}}{\varepsilon_{ch}} \tag{3}$$

where $\varphi_{CH}(x,y)$ is the potential in the channel, ε_{ch} is the permittivity of channel semiconductor material, and N_{ch} is the small n-type channel doping. In case the channel is p-doped, we must use a doping of $-N_{ch}$.

The solution of (3) under the same boundary conditions as assumed in (1), but with a gate oxide thickness of t_{ox}, yields the following expression for the channel surface potential (φ_{ch}) evaluated at $y = \pm t_{2D}/2$:

$$\varphi_{ch} = c_1 \sinh(\beta x) + c_2 \sinh[\beta(L - x)] + V_{GS} - V_{FBCH} + qN_{ch}t_{2D}/(2C_{ox}) \tag{4}$$

where c_1 and c_2 are constants of integration, $V_{FBCH} = [\varphi_m - (\chi_{ch} + E_{GCH}/2) + \Delta E_C + \Delta E_G/2]/q$ is the flat-band voltage of the channel with respect to gate (χ_{ch} is the electron affinity of the channel material, E_{GCH} is the bandgap and ΔE_C is the conduction band offset of the channel with respect to source), $\Delta E_G = E_{GCH} - E_{GS}$ is the difference of the channel and source bandgaps, and $\beta = \sqrt{(2C_{ox})/(\varepsilon_{ch}t_{2D})}$. Note that for simplicity in our model, we have considered the conduction band offset to be equal to the difference of the electron affinities of the channel and source (χ_s), i.e., $\Delta E_C = \chi_{ch} - \chi_s$. The valence band offset (ΔE_V) of the channel with respect to the source is therefore, given by: $\Delta E_V = \Delta E_G + \Delta E_C$.

The complete solution of the surface potential in the device requires the applications of suitable boundary conditions, which, when applied to (2) and (4) yield the values for the constants of integration and the source depletion length. With the intrinsic Fermi level of the source as the reference, we can write the following boundary condition (BC_{source}) at the end of the source depletion region ($x = -L_1$):

$$\varphi_{s|x=-L_1} = -[E_{GS}/(2q) + (E_V - E_{FS})/q]. \tag{5}$$

Similarly, at the channel-drain junction ($x = L$), neglecting drain depletion (because ON-current is independent of drain depletion length), we can write the following BC (BC_{drain}):

$$\varphi_{ch|x=L} = \frac{E_{GS}}{2q} + \frac{(E_{FD} - E_C)}{q} + V_{DS} - \frac{\Delta E_C}{q}. \tag{6}$$

The other two boundary conditions are obtained by equating the surface potential and the lateral displacement field between φ_s and φ_{ch} at the source-channel junction ($x = 0$).

Since the source and drain doping in TFET are generally degenerate to allow for greater ON-current and low contact resistance, it necessitates the use of FD statistics [Fig. 2(a)] to

evaluate the correct boundary conditions. For example, with a p-type source doping of N_s, we can write

$$N_s = \int_{-\infty}^{E_V} \mathrm{DOS}_{2D}[1 - f(E)]dE \tag{7}$$

where $\mathrm{DOS}_{2D} = g_1 m^*/(\pi\hbar^2)$ is the 2-D DOS, g_1 is the valley degeneracy [38], $m^* = \sqrt{m_{xv_s} m_{zv_s}}$ is the DOS effective mass of holes (m_{xv_s} and m_{zv_s} are effective masses of holes in source valence band along x- and z-direction, respectively), $\hbar$ is the reduced Planck's constant, $f(E)$ is the Fermi occupation probability for electrons, and E_V is the maxima of the valence band.

Using (7) we can find out $(E_V - E_{FS})$ to compute (5). Similarly, by applying Fermi statistics to the n^+ drain, we can obtain $(E_{FD} - E_C)$ to compute (6). Finally, applying all the BCs and after suitable mathematical substitutions, we arrive at the following expression from which L_1 can be computed analytically:

$$\tanh(\beta L)\left\{\begin{array}{l} c_1 - \dfrac{\varepsilon_s d_1 \beta_1}{\varepsilon_{ch}\beta}\left(1 - \cosh^2(\beta_1 L_1)\right) \\ +(V_{FBS} - V_{FBCH}) + \dfrac{q t_{2D}(N_{ch} + N_s\pi/2)}{2C_{ox}} \end{array}\right\}$$
$$= \left\{\varphi_{s|x=-L_1} + \frac{q N_s t_{2D}\pi}{4C_{ox}} - V_{GS} + V_{FBS}\right\}\cosh(\beta_1 L_1). \tag{8}$$

Note that c_1 is obtained by evaluating (4) at $x = L$ and equating it to (6), and d_1 is obtained by evaluating (2) at $x = -L_1$ and equating it to (5). Once L_1 is obtained from (8), all other constants of integration in (2) and (4) are obtained to yield the complete solution of the surface potential in the entire device.

To compare the validity of our surface potential model we compare our model results against those obtained from first principle 2-D numerical NEGF simulations [16]. We plot the obtained energy bands for both HMJ and HTJ TFETs as a function of lateral distance for different values of the V_{GS}, and list all device specifications, along with the model comparisons in Fig. 3. The parameters for the energy bands and the associated effective masses for both WTe_2 (source) and MoS_2 (channel) used for the simulations are: $\chi_s = 3.77$ eV, $\chi_{ch} = 4.5$ eV, $E_{GS} = 1.33$ eV, $E_{GCH} = 1.6$ eV, for $\Delta E_C = 0.73$ eV and $\Delta E_V = 1.0$ eV. The effective mass of electrons and holes in WTe_2 along x- (transport) and z-directions are $0.32m_0$ and $0.42m_0$ in both the conduction ($m_{xc_s} = m_{zc_s} = m_{c_s}$) and valence bands ($m_{xv_s} = m_{zv_s} = m_{v_s}$), respectively, where m_0 is the mass of an electron. For MoS_2, the effective mass of electrons in the conduction band along x- ($m_{xc_{ch}}$) and z- ($m_{zc_{ch}}$) are $0.5788m_0$ and $0.5664m_0$, respectively, while for the holes in the valence band they are equal at ($m_{xv_{ch}} = m_{zv_{ch}} = m_{v_{ch}}$) $0.66m_0$.

From Fig. 3 it can be observed that the match of our results against NEGF simulations is very good for both HMJ and HTJ TFETs for the simulated values of V_{GS} and V_{DS}, channel length, and source doping. Note that the doping concentrations have been normalized to a monolayer (~0.5-nm thick) 2-D-body. Because of the thin body and gate-dielectric, the electrostatic control over the channel potential is excellent for long channel transistors leading to almost flat energy bands

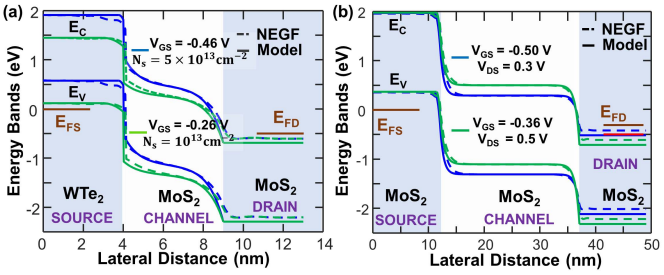

Fig. 3. Comparison of our surface potential model against NEGF simulations. (a) Lateral HTJ DG-2-D-TFET has been simulated with $N_{ch} = 5 \times 10^3$ cm^{-2}, $N_d = 2.5 \times 10^{13}$ cm^{-2}, $V_{DS} = 0.3$ V, $L = 5$ nm, $t_{2D} = 1$ nm, t_{ox} (SiO_2 dielectric) $= 1$ nm, $\varphi_m = 4.5$ eV and variable N_s, and V_{GS}. WTe_2 is the source material, and MoS_2 forms the channel and drain materials. (b) Lateral HMJ 2-D-TFET simulation with MoS_2 as the source, channel, and drain material. All other structural parameters are same as above, except $L = 25$ nm and $N_s = N_d = 5 \times 10^{13}$cm^{-2}, $\varphi_m = 4.96$ eV, and two different V_{DS}.

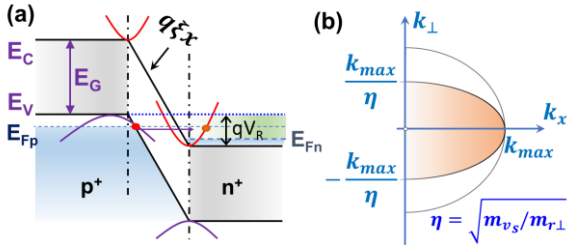

Fig. 4. (a) Simplified tunneling barrier where the energy bands, Fermi level in the p-(E_{Fp}) and n-(E_{Fn}) regions, average tunneling electric field (ξ) across the depletion region, and the net energy overlap of the bands (qV_R) are shown. ξ is calculated by the ratio of the electrostatic band-bending to the total tunneling distance of the carriers. (b) Diagram illustrating the reduced k-space (shaded) of electron wavevectors in the source that contribute to the tunneling current. The limits of the k wave-vector are obtained as noted in (9) and (10). The maximum value of k_x is k_{max} (9), which denotes the maximum electron wave-vector corresponding to an energy of qV_R, while the maximum value of $k_\perp$, the electron wave-vector along z-direction, is k_{max}/η. Also, since only positive electron wave-vectors along the tunneling direction contribute to tunneling, k_x has only positive values. $m_{r\perp}$ is the reduced perpendicular effective mass and has been defined in (10).

(surface potential dictated by gate electrode) except at the source and drain junctions, however, for shorter channel length transistors (~5-nm channel length) the short channel effects degrade the gate control over the channel potential as seen from Fig. 3(a). Although the effect of the drain depletion region becomes more apparent near the drain in these short channel transistors, however, as shown later in Fig. 7, its effect on the ON-current is still negligible because the source-channel tunneling electric field is still well accounted for. Also, the negative gate voltages in the simulations are because of the choice of the gate metal work-function. The position of the Fermi level in the source and drain regions relative to E_V and E_C, respectively, highlights the importance of incorporating FD statistics in our model. The small mismatch between the model and simulated energy bands near the drain is because of the presence of the intrinsic contact resistance present in any NEGF simulation.

After establishing our model and confirming its validity against NEGF simulations, we move on to Section IV where we model the drain current.

IV. Drain Current Model

In this section we derive the analytical tunneling current model for 2-D lateral-TFETs starting from Landauer's equation [39]. Both the forward current flowing from the drain to the source and the reverse current flowing from the source to the drain are computed to evaluate the net ON-current, which is given by the difference of these two. Moreover, as already stated, the doping concentration in both source and drain are high in TFETs, thereby making it imperative that we take the FD distribution of the carriers into account. This introduces a dependence of doping into the model and helps in achieving zero drain current at zero drain–source bias when used in Landauer's model for evaluating the current. This is because the source and the drain Fermi levels align at zero drain–source bias leading to symmetric source and drain carrier distribution, and hence, equal forward and reverse current.

A. Ranges of Electron Wave-Vector for Tunneling and Tunneling Probability

Fig. 4 shows a simplistic diagram of an electron tunneling from the valence band of a p^+-material to the conduction band of an n^+-material, across a generic bandgap of E_G. Also shown is the difference in the curvatures of the respective energy bands arising because of the difference in the effective mass of the carriers. Note that although this represents a generic p-n-junction tunneling diode, it must be realized that the physics of tunneling across the energy bands in this device is similar to that of an n-TFET which has a p^+ source and an n-channel, where the carrier concentration of the channel is varied by the application of V_{GS}. The applied V_{GS}, therefore, modulates the energy overlap (qV_R) and the tunneling electric field (ξ) in the device, hence, affecting the ON-current.

Since the energy of an electron (E) is related to its momentum wave-vector (k) and its effective mass (m^*) as $E = \hbar^2k^2/2m^*$, hence, any change of m^* during tunneling (isoenergetic process) from one band to another changes its k vector. This is manifested during tunneling from the source valence band to the channel conduction band of the TFET, whose difference in curvatures, along with the conservation of the perpendicular electron wave-vector (along the z-axis) while tunneling, causes a change in the lateral wave-vector (along x-axis) of the electron. Assuming the perpendicular electron wave-vector to be $k_\perp$, the lateral wave-vector in the source valence band to be k_{1x} and that in the channel conduction band to be k_{2x}, we obtain the following limits of the wave-vectors [23], [40] over which tunneling occurs.

For k_{1x}

$$-\sqrt{k_{\max}^2 - \frac{m_{v_s}k_\perp^2}{m_{r\perp}}} \le k_{1x} \le \sqrt{k_{\max}^2 - \frac{m_{v_s}k_\perp^2}{m_{r\perp}}}. \tag{9}$$

For $k_\perp$

$$-k_{\max}\sqrt{m_{r\perp}/m_{v_s}} \le k_\perp \le k_{\max}\sqrt{m_{r\perp}/m_{v_s}} \tag{10}$$

where, $k_{\max}^2 = 2m_{v_s}qV_R/\hbar^2$ denotes the maximum tunneling electron wave-vector, and $1/m_{r\perp} = (1/m_{zv_s} + 1/m_{zc_{ch}})$ is the reduced perpendicular effective mass. Therefore, the limits of k_{1x} is $k_{\max}$, and that of $k_\perp$ is $k_{\max}/\eta$ (defined in Fig. 4), which corresponds to an ellipsoidal region of the momentum space where the tunneling takes place [40]. However, as we will show later, since we are only considering electron tunneling from source to channel, k_{1x} has only positive values, and therefore, the lower limit of k_{1x} in (9) is 0. Also, since we are not considering any direct source to drain tunneling, the ranges of electron wave-vectors derived in (9, 10) are for electrons tunneling from source to channel only.

Applying Wentzel–Kramer–Brillouin (WKB) approximation [41], we can calculate the effect of $E_\perp$ on the tunneling probability of carriers $T(E_\perp)$, as

$$T(E_\perp) = \exp\left[-4\sqrt{2m_r^*}E_{GS}^{3/2}/(3q\xi\hbar)\right]\exp\left(-E_\perp/\bar{E}\right) \tag{11}$$

where $\bar{E} = q\hbar\xi/\sqrt{8m_r^*E_{GS}}$ and $m_r^* = (1/m_{xv_s} + 1/m_{xc_{ch}})^{-1}$ is the reduced effective mass, which effectively accounts for the electron-hole duality during band-to-band tunneling. Note that E_{GS} in (11) is the net energy barrier that the tunneling electrons have to surmount, and corresponds to the bandgap of the material where the tunneling commences from, and is therefore, of the source.

B. Extraction of the Tunneling Electric Field and the Band Overlap

To evaluate the tunneling probability (11) and the maximum allowable electron wave-vectors (9), (10), we need to extract the tunneling electric field (ξ) and the band energy overlap (qV_R). These two parameters are obtained from the solution of the surface potential obtained in Section III.

Since the reference of the surface potential solution is taken to be that of the intrinsic Fermi level of the source and is at a potential of $\varphi_s(x = -L_1)$, therefore, the tunneling electrons will reach the channel conduction band where the potential would be E_{GS}/q more than $\varphi_s(x = -L_1)$. This ensures that the total energy separation between the bands becomes equal to the source band gap energy E_{GS}. This net energy difference is due to both the electrostatic energy difference and the energy difference due to the band offset. In an HTJ therefore, the electrostatic energy difference must be $E_{GS} - \Delta E_C$. Denoting the x-coordinate in the channel where the tunneling terminates by L_2, L_2 is obtained by equating (4) to $(E_{GS} - \Delta E_C)/q + \varphi_s(x = -L_1)$. For an HMJ, however, $\Delta E_C = 0$, and results in larger L_2 than that in an HTJ.

Once L_2 is obtained, an average electrostatic tunneling electric field is extracted, which is assumed to remain constant across the entire tunneling distance for simplicity. For HTJs, this tunneling electric field is given by

$$\xi = \frac{E_{GS} - \Delta E_C}{q(L_1 + L_2)}. \tag{12}$$

For HMJs $\Delta E_C = 0$ in (12). This electric field is then used for all subsequent drain current calculations.

The screening length (λ), which is a measure of the decay of the surface potential [42], in the center of the channel of

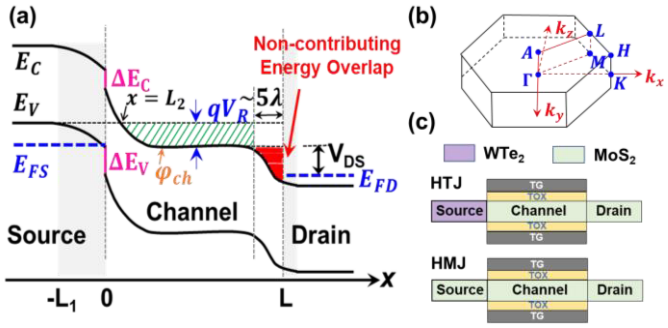

Fig. 5. (a) Band diagram of a TFET during ON-condition showing an energy overlap of qV_R (green shaded region) between the channel conduction and source valence bands, and the point where the channel conduction bands cross the source valence bands ($x = L_2$). The overlap of the energy bands indicated by a red shaded region (around 5λ from the drain) does not contribute to the tunneling current because of its large tunneling distance from the source energy bands, thereby resulting in low tunneling probability. The center surface potential (φ_{ch}) therefore, is obtained by averaging out the channel surface potential from $x = (L-5\lambda)$ to $x = L_2$. (b) BZ of a general hexagonal lattice showing symmetry points ***K***, ***M***, and ***Γ*** (on *xz*-plane), and vertically on top of them (along k_y-direction) are the ***H***, ***L***, and ***A*** points (in a coordinate system corresponding to Fig. 1(b)). (c) Material choices (top); WTe_2 (purple) and MoS_2 (green); schematic of WTe_2-MoS_2 HTJ and (bottom); MoS_2-MoS_2 HMJ.

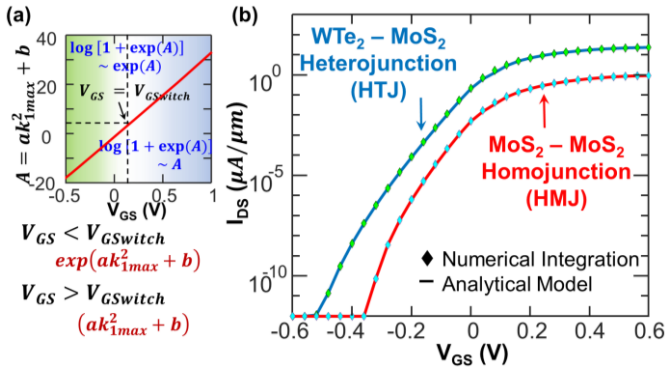

Fig. 6. (a) Diagram illustrating the approximation of (16) into two separate equations under different biases of operation. When $V_{GS} < V_{GSwitch}$ the factor A is lower than log(4), and can be approximated as an exponential function, while for higher gate biases it can be approximated as a linear function. The gate voltage around which this switch happens is denoted in (17). (b) Comparison of our analytical drain current model (solid line) against numerical simulations (symbol) for both WTe_2-MoS_2 DG-HTJ and MoS_2-MoS_2 DG-HMJ with $N_s = 5 \times 10^{13}$ cm^{-2}, $N_d = 2.5 \times 10^{13}$ cm^{-2}, $N_{ch} = 0$, $V_{DS} = 0.3$ V, $L = 25$ nm, $t_{2D} = 1$ nm, t_{ox} (SiO_2 dielectric) = 1 nm, and variable V_{GS}. Metal with a work-function of 4.5 eV is the gate electrode.

any DG field-effect transistor (FET) can be reduced to that of at its surface, given by $\sqrt{t_{ox}t_{2D}(\varepsilon_{ch}/2\varepsilon_{ox})}$, when the body thickness is very small. Since the net potential range over which the tunneling takes place (V_R) is defined by the useful overlap of energy bands [see Fig. 5(a)], it was found from extensive simulations that it is best approximated (for greater drain current saturation) by subtracting the potential at $x = L_2$ from the channel potential averaged out between $x = L_2$ to $x = L - 5\lambda$. Therefore, V_R is

$$V_R = \frac{1}{L - 5\lambda - L_2}\int_{L_2}^{L-5\lambda} \varphi_{ch} dx - [\varphi_{ch}]_{x=L_2} \tag{13}$$

where φ_{ch} is the channel surface potential and is obtained from (4).

Note that when $L_2 > (L - 5\lambda)$, we average the channel potential over the entire channel length. Once V_R and ξ are obtained, the tunneling probability and the ranges of electron wave-vector over which tunneling takes place (9), (10) are evaluated to yield the total drain current.

C. Analytical Model of Drain Current

The 1-D current density (A/m) can be written as [39]

$$J = 2q\int \frac{d^2k}{(2\pi)^2} v(E)T(E_\perp)(f_{sv} - f_{dc}) \tag{14}$$

where $v(E) = (1/\hbar)(dE/dk)$ is the velocity of electrons, $f_{sv} = 1/[1+\exp\{-(E_{1x}+E_\perp-(E_V-E_{FS}))/kT\}]$ is the Fermi occupation of electrons in the source valence band (E_{1x} and $E_\perp$ are energies corresponding to wave-vectors k_{1x} and $k_\perp$, respectively), f_{dc} is the Fermi occupation of electrons in the drain conduction band. For brevity, we show the derivation of the forward drain–source tunneling current (limited by f_{sv}) in this section. The derivation of the reverse source–drain current is similar, except for a small modification of the source Fermi voltage (E_{FS}/q) to the drain Fermi voltage (E_{FD}/q) by: $(E_{FD}/q) = (E_{FS}/q) + V_{DS}$ to account for applied V_{DS}. Please note that (14) implicitly assumes physics of 2-D materials because of the integration over 2-D DOS, and therefore, is not applicable for conventional bulk semiconductors. Moreover, monolayer 2-D materials have similar lattice constants and are generally direct bandgap semiconductors with the valence band maxima/conduction band minima occurring around the ***K***-point [see Fig. 5(b)]. This implies that the tunneling current model for both lateral-2-D based homo- and hetero-junction TFETs [see Fig. 5(c)] do not need consideration of phonon-assisted tunneling physics. For vertical 2-D-TFETs, however, the ***K***-point in the Brillouin zone (BZ) of one layer can overlap with either the ***K*** or ***K***′ point of the second layer, based on *AA* or *AB* stacking, respectively, and hence, tunneling can either be direct or through the assistance of phonons.

Substituting $T(E_\perp)$ from (11) into (14) and segregating terms, we can write the following:

$$J = \frac{q\hbar}{2\pi^2 m_{v_s}} \exp\left[-\frac{4\sqrt{2m_r^*}E_{GS}^{3/2}}{3q\xi\hbar}\right]\int_{k_{\perp\min}}^{k_{\perp\max}} \exp\left(-\frac{\hbar^2k_\perp^2}{2m_{v_s}\overline{E}}\right)dk_\perp \times \int_0^{k_{1\max}} \frac{k_{1x}}{1+\exp\left(\frac{E_V-E_{FS}}{kT} - \frac{\hbar^2k_\perp^2}{2m_{v_s}kT} - \frac{\hbar^2k_{1x}^2}{2m_{v_s}kT}\right)}dk_{1x} \tag{15}$$

where $k_{\perp\min}$ and $k_{\perp\max}$ are the minimum and maximum ranges of (10), and $k_{1\max}$ is the maximum value of (9) for a certain $k_\perp$. Since k_{1x} is the electron wave-vector along tunneling direction in the source, hence, the integration in (15) is only carried out for positive values of k_{1x}.

The finite integration over k_{1x} in (15) is evaluated as

$$\frac{1}{2a}\log\left[\frac{1+\exp(ak_{1\max}^2+b)}{1+\exp(b)}\right] \tag{16}$$

where $a = \hbar^2/(2m_{v_s}kT)$ and $b = \hbar^2k_\perp^2/(2m_{v_s}kT) - (E_V - E_{FS})/kT$.

To obtain an analytical model of tunneling current, (16) must be simplified, as both $k_{1\max}$ (9) and b (16) are functions of $k_\perp$, which will subsequently be integrated over in (15). As will be shown later, the drain current for the term $\log[1+\exp(b)]$ in (16) is negligibly small compared to the other terms primarily due to the absence of the maximum tunneling wave-vector ($k_{1\max}$) and can be safely ignored for all practical purposes. Also, plotted in Fig. 6(a) is the maximum value of the function $(ak_{1\max}^2 + b) = A$ as a function of V_{GS} for a certain device configuration, and under certain bias. As can be observed from Fig. 6(a), as V_{GS} is swept from a negative to a positive bias, A changes from a negative value to a positive value around a certain V_{GS}. When $\exp(A) <\sim 4$, the logarithmic function in (16) can be approximated as an exponential function [see Fig. 6(a)], while for higher values, it is best approximated as a linear function [see Fig. 6(a)]. The gate bias where this demarcation lies is denoted by $V_{GSwitch}$ and is obtained by equating $\exp(ak_{1\max}^2 + b)$ to 4 in (16) to obtain

$$\begin{aligned} V_{GSwitch} = &\left(\varphi_{s|x=-L_1} + \frac{E_{GS} - \Delta E_C}{q}\right) \\ &+ [1.6kT + E_{FD}]\frac{m_{v_s}}{q m_{xc_{ch}}} - \frac{qN_{ch}t_{2D}}{2C_{ox}} \\ &+ \frac{1}{\beta(L-L_2)}[c_2\cosh\{\beta(L-x)\} \\ &- c_1\cosh\{\beta x\}]_{L_2}^{L} + V_{FBCH}. \end{aligned} \tag{17}$$

When $V_{GS} < V_{GSwitch}$, the logarithmic function in (16) can be approximated solely by an exponential function of $(ak_{1\max}^2 + b)$ to yield the following expression for current:

$$\begin{aligned} J_1 = &\frac{qkT}{4\hbar^2\pi^2}\sqrt{\frac{2\pi m_{v_s}}{\left(\frac{\eta^2-1}{kT} + \frac{1}{\overline{E}}\right)}}\exp\left[-\frac{4\sqrt{2m_r^*}E_{GS}^{3/2}}{3q\xi\hbar}\right] \\ &\times \exp\left[\frac{m_{xc_{ch}}qV_R}{m_{v_s}kT} - \frac{(E_V - E_{FS})}{kT}\right] \\ &\times \left[\operatorname{erf}\left\{k_\perp\sqrt{\hbar^2\left(\frac{\eta^2-1}{kT} + \frac{1}{\overline{E}}\right)/(2m_{v_s})}\right\}\right]_{k_{\perp\min}}^{k_{\perp\max}}. \end{aligned} \tag{18}$$

When $V_{GS} > V_{GSwitch}$, the logarithmic function in (16) is best approximated as a linear function, and after suitable mathematical manipulations, we obtain the following expression for the current density:

$$\begin{aligned} J_2 = &\frac{qkT}{2\hbar\pi^2}\exp\left[-\frac{4\sqrt{2m_r^*}E_{GS}^{3/2}}{3q\xi\hbar}\right] \\ &\times\left[\begin{array}{l} \left(\frac{m_{xc_{ch}}qV_R}{m_{v_s}kT} - \frac{(E_V-E_{FS})}{kT}\right)\left[\frac{\sqrt{2m_{v_s}\overline{E}}\pi}{2\hbar}\operatorname{erf}\left(\frac{\hbar k_\perp}{\sqrt{2m_{v_s}\overline{E}}}\right)\right]_{k_{\perp\min}}^{k_{\perp\max}} \\ -\frac{\hbar^2(\eta^2-1)}{2m_{v_s}kT}\left[\begin{array}{l}\frac{\sqrt{\pi}}{4(\hbar^2/2m_{v_s}\overline{E})^{3/2}}\operatorname{erf}\left(\frac{\hbar k_\perp}{\sqrt{2m_{v_s}\overline{E}}}\right) \\ -\frac{k_\perp m_{v_s}\overline{E}}{\hbar^2}\exp\left(-\frac{\hbar^2k_\perp^2}{2m_{v_s}\overline{E}}\right)\end{array}\right]_{k_{\perp\min}}^{k_{\perp\max}} \end{array}\right]. \end{aligned} \tag{19}$$

Therefore, we have a piecewise model for the drain current, where J_1 (18) is valid until $V_{GS} < V_{GSwitch}$, and J_2 (19) is valid when $V_{GS} > V_{GSwitch}$. To make a smooth model for the drain current valid over the entire range of gate biases, we need to link these two piecewise models seamlessly. This is enabled by using a tan-hyperbolic smoothing function (S)

$$S = 0.5 + 0.5\tanh[28(V_{GS} - V_{GSwitch})] \tag{20}$$

which switches from a minimum value of 0 to a maximum value of 1 around $V_{GS} = V_{GSwitch}$. The factor of 28 determines the steepness of this switch and has been found to give the best match with numerical simulation results. The final expression of the forward tunneling (J_f) current flowing from the drain to the source can therefore, be expressed, using (18)–(20) to yield

$$J_f = J_1[1 - S] + J_2 S. \tag{21}$$

Similarly, the reverse current (J_r) flowing from the source to the drain can be calculated by the simple substitution of the source Fermi level with the drain Fermi level in (15)–(17) to compute (18)–(20) and subsequently, (21). Therefore, the net tunneling current density (J) flowing from the drain to the source of the TFET is given as

$$J = J_f - J_r. \tag{22}$$

To ascertain the validity of our approximations and simplifications made in the derivation of the analytical model, we compare and show the excellent match of our analytical model results against those obtained by numerically integrating (15) in Fig. 6(b), where the schematic of the TFETs is shown in Fig. 5(c). As observed from Fig. 6(b), our model results compare exceedingly well against the numerical simulations, thereby confirming the validity of all the simplifications, the neglect of the $\log[1+\exp(b)]$ term in (16), and the smoothness of the piecewise drain current model. Also observed in the figure is the higher ON-current of the HTJ TFET over HMJ TFET for the entire range of the gate bias, bringing out the importance of using a suitable source-channel junction for improving the electrical characteristics.

A constant leakage current of 10^{-20} A/μm is assumed to be flowing in the device from the drain to source, except at zero V_{DS} where the net current in the device should be zero. This is accomplished by modeling the net OFF-current per unit width (W) of the device as a function of V_{DS} as

$$I_{OFF} = 10^{-14}\tanh[30V_{DS}] \tag{23}$$

where the tan hyperbolic function ensures continuity of the $I_{DS} - V_{DS}$ characteristics.

The results obtained from our model have been compared against those obtained from NEGF simulations [16] in Fig. 7, where the transfer characteristics ($I_{DS} - V_{GS}$) of both HMJ (MoS_2-MoS_2) and HTJ (WTe_2-MoS_2) DG-2-D-TFETs (note that DIBL, important for short channel technology nodes, has already been accounted for in the surface potential model) have been plotted and compared against. The reasonably good match of the results against NEGF simulations for a variety of device parameters, such as channel length, gate dielectric constant, and gate and drain biases, proves the veracity and robustness of the model, which has been derived from scratch without employing any fitting parameters.

Fig. 8 shows the output characteristics ($I_{DS} - V_{DS}$) for various V_{GS} and device parameters. At zero V_{DS} the net drain

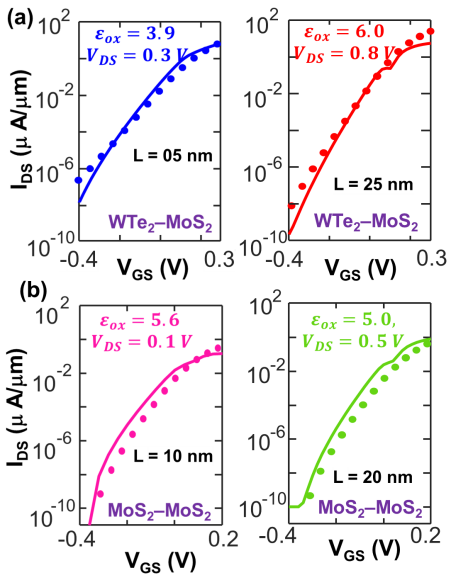

Fig. 7. I_{DS}–V_{GS} comparison of our analytical model (solid lines) against NEGF simulations (symbols) for both (a) WSe_2-MoS_2 DG-HTJ and (b) MoS_2-MoS_2 DG-HMJ device at varying gate oxide permittivity, channel length, and V_{DS}. The devices have a source and drain doping concentrations of 5×10^{13} cm^{-2} and 2.5×10^{13} cm^{-2}, respectively with intrinsic channel. The body (t_{2D}) and gate oxide thicknesses (t_{ox}) are 1 nm each. Metals with work-function of 4.56 eV and 4.5 eV are used for HTJ and HMJ simulations, respectively.

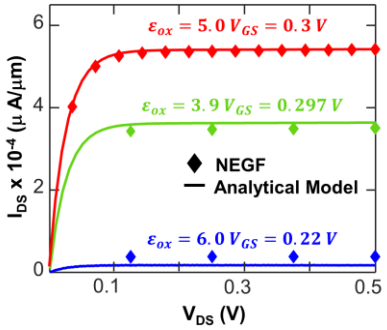

Fig. 8. I_{DS}–V_{DS} comparison against NEGF simulations for WTe_2-MoS_2 DG-HTJ device with various gate dielectrics and V_{GS}. Device parameters for simulation are same as in Fig. 6(b) with a channel length of $L = 20$ nm and $\varphi_m = 4.96$ eV.

current is zero because of the equal contribution of the forward and the reverse current. However, as V_{DS} continues to increase, the contribution of the reverse current diminishes because of the decrease in the carrier occupation at the drain, thereby increasing the net drain current, until it eventually saturates at higher V_{DS}. TFETs, therefore, show more pronounced drain current saturation with V_{DS} compared to MOSFETs, and the same is observed clearly from our figure. Most importantly, Figs. 7 and 8 show the excellent match of our model results compared to the NEGF simulations for a variety of device parameters.

The development of any compact model is incomplete without the inclusion of the capacitance in the device, which allows the modeling of transient characteristics. The low efficiency of charge transport at the source-channel junction in a TFET compared to a MOSFET because of the presence of a tunnel barrier in the former limits its gate–source capacitance (C_{GS}); however, the larger channel charge at the drain side of the TFET (n-n$^+$ junction) compared to the MOSFET leads to increased gate–drain capacitance (C_{GD}). Although the accurate modeling of these capacitances relies on modeling the channel charge from the surface potential model, a simplistic modeling allows a 30–70 partition of the gate capacitance to C_{GS} and C_{GD}, respectively, [16], irrespective of the applied voltage, and the same has been incorporated into our compact model.

V. Conclusion

A rigorous compact modeling framework for 2-D channel TFETs has been developed that is valid for both lateral homo- and hetero-source-channel junctions down to ultrashort channel length of 5 nm. The framework incorporates fully analytical modeling of the surface potential in the source and channel by accurately considering the junction electrostatics, the fringing gate electric field lines, and the carrier distribution profile dictated by FD statistics. Subsequently, the average tunneling electric field and the net potential range for the tunneling carriers are derived from the developed surface potential model to evaluate the transmission probability of the tunneling carriers by employing the WKB approximation. Finally, the drain current model was derived by analytically solving the 2-D Landauer's equation by considering both the forward and reverse currents and by appropriately integrating over the allowed electron wave-vectors. The good agreement of our model with NEGF simulations, without the use of any fitting parameters, for both 2-D lateral HMJ and HTJ TFETs, at various channel lengths and structural parameters, provides necessary validation. Our developed compact model can be utilized to study the performance of these various lateral 2-D TFETs and circuits derived from them, including novel neuromorphic circuits.

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References

[1] T. Sakurai, "Perspectives of low-power VLSI's," *IEICE Trans. Electron.*, vol. E87-C, no. 4, pp. 429–436, 2004.

[2] W. Cao, J. Kang, D. Sarkar, W. Liu, and K. Banerjee, "2D semiconductor FETs—Projections and design for sub-10 nm VLSI," *IEEE Trans. Electron Devices*, vol. 62, no. 11, pp. 3459–3469, Nov. 2015, doi: 10.1109/TED.2015.2443039.

[3] T. Baba, "Proposal for surface tunnel transistors," *Jpn. J. Appl. Phys.*, vol. 31, no. 4B, pp. L455–L457, Apr. 1992, doi: 10.1143/JJAP.31.L455.

[4] Y. Khatami and K. Banerjee, "Steep subthreshold slope n- and p-type tunnel-FET devices for low-power and energy-efficient digital circuits," *IEEE Trans. Electron Devices*, vol. 56, no. 11, pp. 2752–2761, Nov. 2009, doi: 10.1109/TED.2009.2030831.

[5] R. Gandhi, Z. Chen, N. Singh, K. Banerjee, and S. Lee, "Vertical Si-nanowire n-type tunneling FETs with low subthreshold swing (≤ 50 mV/decade) at room temperature," *IEEE Electron Device Lett.*, vol. 32, no. 4, pp. 437–439, Apr. 2011, doi: 10.1109/LED.2011.2106757.

[6] K. Tomioka, M. Yoshimura, and T. Fukui, "Steep-slope tunnel field-effect transistors using III–V nanowire/Si heterojunction," in *Proc. IEEE Symp. VLSI Technol.*, Jun. 2012, pp. 47–48, doi: 10.1109/VLSIT.2012.6242454.

[7] C. Convertino, C. B. Zota, H. Schmid, A. M. Ionescu, and K. E. Moselund, "III–V heterostructure tunnel field-effect transistor," *J. Phys., Condens. Matter*, vol. 30, no. 26, Jul. 2018, Art. no. 264005, doi: 10.1088/1361-648X/aac5b4.

[8] P. Ajayan, P. Kim, and K. Banerjee, "Two-dimensional van der Waals materials," *Phys. Today*, vol. 69, no. 9, pp. 38–44, Sep. 2016, doi: 10.1063/PT.3.3297.

[9] B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti, and A. Kis, "Single-layer MoS_2 transistors," *Nature Nanotechnol.*, vol. 6, no. 3, pp. 147–150, Mar. 2011, doi: 10.1038/nnano.2010.279.

[10] W. Cao *et al.*, "2-D layered materials for next-generation electronics: Opportunities and challenges," *IEEE Trans. Electron Devices*, vol. 65, no. 10, pp. 4109–4121, Oct. 2018, doi: 10.1109/TED.2018.2867441.

[11] Y. Khatami, J. Kang, and K. Banerjee, "Graphene nanoribbon based negative resistance device for ultra-low voltage digital logic applications," *Appl. Phys. Lett.*, vol. 102, no. 4, Jan. 2013, Art. no. 043114, doi: 10.1063/1.4788684.

[12] W. Cao, D. Sarkar, Y. Khatami, J. Kang, and K. Banerjee, "Subthreshold-swing physics of tunnel field-effect transistors," *AIP Adv.*, vol. 4, no. 6, Jun. 2014, Art. no. 067141, doi: 10.1063/1.4881979.

[13] Y. Taur, J. Wu, and J. Min, "Dimensionality dependence of TFET performance down to 0.1 V supply voltage," *IEEE Trans. Electron Devices*, vol. 63, no. 2, pp. 877–880, Feb. 2016, doi: 10.1109/TED.2015.2508282.

[14] H. Zhang, W. Cao, J. Kang, and K. Banerjee, "Effect of band-tails on the subthreshold performance of 2D tunnel-FETs," in *IEDM Tech. Dig.*, Dec. 2016, pp. 30.3.1–30.3.4, doi: 10.1109/IEDM.2016.7838512.

[15] D. Sarkar *et al.*, "A subthermionic tunnel field-effect transistor with an atomically thin channel," *Nature*, vol. 526, no. 7571, pp. 91–95, Oct. 2015, doi: 10.1038/nature15387.

[16] W. Cao, J. Jiang, J. Kang, D. Sarkar, W. Liu, and K. Banerjee, "Designing band-to-band tunneling field-effect transistors with 2D semiconductors for next-generation low-power VLSI," in *IEDM Tech. Dig.*, Dec. 2015, pp. 12.3.1–12.3.4, doi: 10.1109/IEDM.2015.7409682.

[17] A. Szabo, C. Klinkert, D. Campi, C. Stieger, N. Marzari, and M. Luisier, "*Ab initio* simulation of band-to-band tunneling FETs with single- and few-layer 2-D materials as channels," *IEEE Trans. Electron Devices*, vol. 65, no. 10, pp. 4180–4187, Oct. 2018, doi: 10.1109/ted.2018.2840436.

[18] Y. Dong, L. Zhang, X. Li, X. Lin, and M. Chan, "A compact model for double-gate heterojunction tunnel FETs," *IEEE Trans. Electron Devices*, vol. 63, no. 11, pp. 4506–4513, Nov. 2016, doi: 10.1109/TED.2016.2604001.

[19] P. K. Sahoo, S. Memaran, Y. Xin, L. Balicas, and H. R. Gutiérrez, "One-pot growth of two-dimensional lateral heterostructures via sequential edge-epitaxy," *Nature*, vol. 553, no. 7686, pp. 63–67, Jan. 2018, doi: 10.1038/nature25155.

[20] P. Luo *et al.*, "Doping engineering and functionalization of two-dimensional metal chalcogenides," *Nanosc. Horizons*, vol. 4, no. 1, pp. 26–51, 2019, doi: 10.1039/c8nh00150b.

[21] K. Banerjee, "2D materials for smart life," in *Proc. IEEE 2nd Electron Devices Technol. Manuf. Conf. (EDTM)*, Kobe, Japan, Mar. 2018, pp. 4–6, doi: 10.1109/EDTM.2018.8421451.

[22] D. Sarkar and K. Banerjee, "Proposal for tunnel-field-effect-transistor as ultra-sensitive and label-free biosensors," *Appl. Phys. Lett.*, vol. 100, no. 14, Apr. 2012, Art. no. 143108, doi: 10.1063/1.3698093.

[23] A. Pal and A. K. Dutta, "Analytical drain current modeling of double-gate tunnel field-effect transistors," *IEEE Trans. Electron Devices*, vol. 63, no. 8, pp. 3213–3221, Aug. 2016, doi: 10.1109/TED.2016.2581842.

[24] L. Liu, D. Mohata, and S. Datta, "Scaling length theory of double-gate interband tunnel field-effect transistors," *IEEE Trans. Electron Devices*, vol. 59, no. 4, pp. 902–908, Apr. 2012, doi: 10.1109/TED.2012.2183875.

[25] M. Gholizadeh and S. E. Hosseini, "A 2-D analytical model for double-gate tunnel FETs," *IEEE Trans. Electron Devices*, vol. 61, no. 5, pp. 1494–1500, May 2014, doi: 10.1109/TED.2014.2313037.

[26] S. Kumar *et al.*, "2-D analytical drain current model of double-gate heterojunction TFETs with a SiO_2/HfO_2 stacked gate-oxide structure," *IEEE Trans. Electron Devices*, vol. 65, no. 1, pp. 331–338, Jan. 2018, doi: 10.1109/TED.2017.2773560.

[27] Y. Guan, Z. Li, W. Zhang, and Y. Zhang, "An accurate analytical current model of double-gate heterojunction tunneling FET," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 938–944, Mar. 2017, doi: 10.1109/ted.2017.2654248.

[28] Y.-K. Lin, S. Khandelwal, J. P. Duarte, H.-L. Chang, S. Salahuddin, and C. Hu, "A predictive tunnel FET compact model with atomistic simulation validation," *IEEE Trans. Electron Devices*, vol. 64, no. 2, pp. 599–605, Feb. 2017, doi: 10.1109/TED.2016.2639547.

[29] R. B. Salazar, H. Ilatikhameneh, R. Rahman, G. Klimeck, and J. Appenzeller, "A predictive analytic model for high-performance tunneling field-effect transistors approaching non-equilibrium Green's function simulations," *J. Appl. Phys.*, vol. 118, no. 16, pp. 164305–164311, 2015, doi: 10.1063/1.4934682.

[30] Y. Taur, J. Wu, and J. Min, "An analytic model for heterojunction tunnel FETs with exponential barrier," *IEEE Trans. Electron Devices*, vol. 62, no. 5, pp. 1399–1404, May 2015, doi: 10.1109/TED.2015.2407695.

[31] J. U. Mehta, W. A. Borders, H. Liu, R. Pandey, S. Datta, and L. Lunardi, "III–V tunnel FET model with closed-form analytical solution," *IEEE Trans. Electron Devices*, vol. 63, no. 5, pp. 2163–2168, May 2016, doi: 10.1109/TED.2015.2471808.

[32] M. G. Bardon, H. P. Neves, R. Puers, and C. Van Hoof, "Pseudo-two-dimensional model for double-gate tunnel FETs considering the junctions depletion regions," *IEEE Trans. Electron Devices*, vol. 57, no. 4, pp. 827–834, Apr. 2010, doi: 10.1109/TED.2010.2040661.

[33] Y. Guan *et al.*, "An accurate analytical model for tunnel FET output characteristics," *IEEE Electron Device Lett.*, vol. 40, no. 6, pp. 1001–1004, Jun. 2019, doi: 10.1109/LED.2019.2914014.

[34] M. O. Li, D. Esseni, J. J. Nahas, D. Jena, and H. G. Xing, "Two-dimensional heterojunction interlayer tunneling field effect transistors (thin-TFETs)," *IEEE J. Electron Devices Soc.*, vol. 3, no. 3, pp. 200–207, May 2015, doi: 10.1109/JEDS.2015.2390643.

[35] J. Min and P. M. Asbeck, "Compact modeling of distributed effects in 2-D vertical tunnel FETs and their impact on DC and RF performances," *IEEE J. Explor. Solid-State Comput. Devices Circuits*, vol. 3, pp. 18–26, Dec. 2017, doi: 10.1109/JXCDC.2017.2670606.

[36] Y. Zhang, Z. Li, and Y. Guan, "Analytical drain current model of double-gate monolayer transition metal dichalcogenide TFET," *IEEE Trans. Electron Devices*, vol. 66, no. 8, pp. 3652–3658, Aug. 2019, doi: 10.1109/TED.2019.2922421.

[37] D. Esseni, M. Pala, P. Palestri, C. Alper, and T. Rollo, "A review of selected topics in physics based modeling for tunnel field-effect transistors," *Semicond. Sci. Technol.*, vol. 32, no. 8, pp. 083005-1–083005-27, 2017, doi: 10.1088/1361-6641/aa6fca.

[38] W. Cao, J. Kang, W. Liu, and K. Banerjee, "A compact current–voltage model for 2D semiconductor based field-effect transistors considering interface traps, mobility degradation, and inefficient doping effect," *IEEE Trans. Electron Devices*, vol. 61, no. 12, pp. 4282–4290, Dec. 2014, doi: 10.1109/TED.2014.2365028.

[39] R. Landauer, "Spatial variation of currents and fields due to localized scatterers in metallic conduction," *IBM J. Res. Develop.*, vol. 1, no. 3, pp. 223–231, Jul. 1957, doi: 10.1147/rd.13.0223.

[40] N. Ma and D. Jena, "Interband tunneling in two-dimensional crystal semiconductors," *Appl. Phys. Lett.*, vol. 102, no. 13, pp. 132102–132105, 2013, doi: 10.1063/1.4799498.

[41] L. D. Landau and E. M. Lifshitz, *Quantum Mechanics*. Reading, MA, USA: Addison-Wesley, 1958, p. 174.

[42] R.-H. Yan, A. Ourmazd, and K. F. Lee, "Scaling the Si MOSFET: From bulk to SOI to bulk," *IEEE Trans. Electron Devices*, vol. 39, no. 7, pp. 1704–1710, Jul. 1992, doi: 10.1109/16.141237.