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Authors

Pecenak, Zachary K
Haghi, Hamed Valizadeh
Li, Changfu
[et al.](#)

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Aggregation of Voltage-Controlled Devices During Distribution Network Reduction

Zachary K. Pecenek, Hamed Valizadeh Haghi, *Senior Member, IEEE*, Changfu Li, *Student Member, IEEE*, Matthew J. Reno, *Member, IEEE*, Vahid R. Disfani, *Member, IEEE*, and Jan Kleissl *Member, IEEE*

Abstract—Quasi-steady state time-series (QSTS) simulation of distribution feeders can become computationally burdensome due to many buses and devices, long simulation horizons, and/or high temporal resolution. To reduce this burden, network reduction removes buses and shifts loads/generation to the remaining buses of the circuit to produce a smaller equivalent. However, voltage-controlled devices have traditionally limited network reduction, since their operation depends on the measurement of voltage at their local bus. This work includes the reduction of buses with voltage-controlled devices by replacing the local voltage measurement with an estimate from a fast voltage sensitivity approach, which is integrated directly into a modified QSTS simulation. Comprehensive tests on an unbalanced feeder with real operating data and volt-var controlled inverters show agreement in cumulative reactive power output between the reduced and the original feeder circuits. The maximum voltage error is 0.005 Vp.u., which is nearly identical to the error in a benchmark reduction without smart inverter voltage control. The algorithm converges for every time step, even when reducing the frequency of which the voltage estimation was updated. While the reduction methodology is demonstrated for inverter volt-var control, since it represents a frequent use case, it can be extended to other voltage-controlled devices.

Index Terms—Distribution system, network reduction, quasi-steady state time-series simulations, volt-var control, smart inverter, voltage estimation, voltage sensitivity.

I. INTRODUCTION

POWER system studies are becoming increasingly complex and computationally expensive due to a growing number of variable renewable energy devices. Reduction of power system models can counteract this problem [1–3]. For a radial feeder power flow solution, computation time decreases monotonically with a decreasing number of buses in the reduced feeder circuit [4].

Simplifications in power flow of real distribution feeders has been a recent focus in the literature. The segmentation method introduced in reference [5] proposes a data-driven approach in which power flow results, or measured data, can be used to represent a portion of the circuit. While this method shows high accuracy on realistic feeders, devices whose operation depends on voltage (i.e. switched capacitors, transformers, voltage regulators,

photovoltaic (PV) systems inverters, etc.) must be preserved in the reduced feeder circuit, restricting the achievable reduction in size.

The method developed in [4, 6] uses the nodal voltage equation to reduce the circuit to a subset of buses with aggregated load and generators. The methodology is shown to be applicable to several diverse feeders and reproduces voltages accurately. While the method reduces power delivery components (i.e. load and generators) and simple distribution lines, devices such as static capacitors and transformers cannot be aggregated and require the preservation of additional buses associated with those elements.

Reference [7] introduced the inversion reduction technique, which improves on the methods of [4, 6] in speed and accuracy and allows for the reduction of static capacitors and transformers, in addition to loads, PV systems, and distribution lines. Thus, only a minimal number of buses needs to be retained. Like the previous methods, however, buses with voltage-controlled equipment cannot be removed during circuit reduction.

Many other valid approaches to the reduction of power systems networks have been proposed in literature. Four of the more popular network reduction techniques are discussed and their performance in static power flow simulations is compared in reference [8] commonly for transmission networks: i) Ward reduction [9], ii) Kron reduction [10], iii) Dimo’s method [11], and iv) Zhukov’s reduction [12]. For the two feeders investigated (IEEE 14 bus and IEEE 118 bus), all methods produced significant voltage errors due to reduction ($> 0.01pu$), while the Ward reduction method produced the lowest error overall. In addition, several studies [13–15] cover network equivalence for multiphase transmission systems from the electromagnetic transient perspective. For dynamic analysis, methods such as Krylov subspace methods [16, 17], balanced truncation [18, 19], and balanced residualization [20] have been applied for power system model reduction. However, dynamic and electromagnetic transient model reduction techniques are not generally applicable to distribution feeders in static power flow analysis.

The inability of the existing methods to remove voltage-dependent buses presents a significant obstacle to computational speed-up for quasi-static power flow analysis on distribution feeders as solar PV and their inverters are becoming increasingly common on distribution feeders. Many distribution system operators are starting to require these inverters to act as voltage-controlled devices, for example as per the requirements of CA Rule 21 and IEEE 1547 [21]. Inverters then modify their reactive (and sometime even active) power autonomously using the local voltage as the control input. This poses a significant problem for existing reduction methods, since each PV bus must be

Z. K. Pecenek is with Bankable Energy | XENDEE, San Diego, CA, 92121 {emails: zpecenek@xendee.com}

H. Valizadeh Haghi, C. Li, and J. Kleissl are with the Department of Mechanical and Aerospace Engineering and Center for Energy Research at University of California San Diego, La Jolla, CA 92093 USA {emails: valizadeh@ieee.org, chl447@ucsd.edu, jkleissl@ucsd.edu}

V. R. Disfani is with the Department of Electrical Engineering at University of Tennessee, Chattanooga, TN 37403 USA {email: vahid-disfani@utc.edu}

M. J. Reno is with Sandia National Laboratories, Albuquerque, NM 87185 USA {email: mjreno@sandia.gov}

retained and the number of PV buses is significant, e.g. 893,000 distributed PV projects in California [22].

Recently published reference [23] proposed a novel approach to the reduction of distribution feeder models with voltage controlled smart inverters. The authors propose an optimization-based approach, which defines a single aggregate control curve for all aggregated inverters, which attempts to minimize the voltage between the aggregated node at a time-step and its nominal voltage. However, the effectiveness of the approach cannot be generalized as the test system consists of only 10 buses, which each have the same magnitude and time-series shape for demand and PV, and the impedance of the network is not specified. Further, solving an optimization problem during each step of a time series simulation is unlikely to provide run-time savings.

In this work, we propose a methodology to improve general distribution feeder reduction techniques, allowing for the reduction of voltage-controlled devices for large unbalanced systems. Examples with hundreds of PV and loads with varying magnitudes and time-series shapes are demonstrated. PV smart inverters are studied as an example of a voltage-controlled device. Individual PV/Inverter systems are retained when being moved to the remaining buses, allowing for inverter control actions based on a unique control curve for each inverter, which match the original power flow by estimating the voltage shift from the original inverter bus.

Specifically, the main contributions of this work to the existing literature on circuit reduction is:

- A methodology to aggregate voltage-controlled devices on the distribution system for time series applications. This novelty is significant as it dramatically increases the network reduction opportunities for typical solar power integration studies at high PV penetration which typically contain hundreds of voltage-controlled solar power inverters per feeder.
- The methodology retains individual PV systems and control curves, removing the need for a single piece-wise control curve.
- As the available headroom is critical for volt-var control, when reducing inverters we retain the inverters AC rating and the PV DC generator size (i.e. over- or under-sized inverters). All previous paper assumed equal AC and DC ratings. This novelty extends the generality of the reduction method.

The paper is organized as follows. Section II summarizes the basic reduction methodology applied in this paper, which was derived in a previous work. Section III introduces the underlying principle used to aggregate inverters. Section IV introduces an algorithm to extend the methodology of inverter aggregation to time series simulations. Two case studies are used to validate the approach in Section V. Section VI concludes the paper and discusses future work.

II. CIRCUIT REDUCTION METHODOLOGY

A. Overview of method derived in reference [7]

Circuit reduction creates an equivalent smaller feeder of critical buses (CBs) by removing other (non-critical) buses. Critical buses

are generally selected by the user, typically as a set of buses which are the focus of the analysis. For example, if a hosting capacity analysis is being performed, a subset of buses near a proposed PV system might be kept as critical buses, while all other buses on the system are designated as non-critical and removed from the analysis. As such, voltages from the non-critical buses are not computed and output by the model. The success of circuit reduction is typically measured by the accuracy of voltages at the CBs and the savings in computation time. Reduction consists of replacing buses, distribution lines, and transformers of the circuit with equivalent fewer buses, longer lines, and transformers. The loads, static capacitors, and generators on the removed buses are represented through aggregate loads, static capacitors, and generators at the CBs.

The inversion reduction technique described in this section was proposed and validated in [7] for real multi-phase distribution feeders. In Section III, we will improve and extend the generality of this method to consider voltage-controlled devices. However, the methodology introduced in sections III and IV is independent of the inversion reduction technique, and can be applied generally to any network reduction technique which aggregates power injection devices. Rather, the method in [7] is chosen as it represents an ongoing effort by the authors.

Consider the nodal voltage equations for the original feeder circuit as well as a reduced equivalent circuit composed of only the critical buses (CB) in the original feeder circuit as

$$V_o = \mathbf{Z}_o I_o, \quad (1)$$

$$V_r = \mathbf{Z}_r I_r, \quad (2)$$

where the subscripts o and r represent the original and reduced feeder circuits, respectively. Bold font indicates a matrix. The variables $V_o \in \mathbb{C}^{M \times 1}$ and $V_r \in \mathbb{C}^{m \times 1}$ are the nodal voltage for each circuit, where M and m indicate the nodes in the original and reduced circuits, respectively. The network impedance matrices for each circuit are given by $\mathbf{Z}_o \in \mathbb{C}^{M \times M}$ and $\mathbf{Z}_r \in \mathbb{C}^{m \times m}$. Finally, $I_o \in \mathbb{C}^{M \times 1}$ and $I_r \in \mathbb{C}^{m \times 1}$ represent the nodal current injection. Since the reduction objective is equivalence of the voltage of the CBs in the original feeder circuit with the buses of the reduced feeder circuit (i.e. $V_o(\text{CB}) = V_r$), we can write

$$\mathbf{Z}_{o,\text{CB}} I_o = \mathbf{Z}_r I_r, \quad (3)$$

where $\mathbf{Z}_{o,\text{CB}} \in \mathbb{C}^{m \times M}$ is the impedance matrix with all rows removed except those that correspond to the critical buses.

To remove the dependence on current, a constant power assumption is introduced (see [7] for a detailed analysis on the impact of the constant power assumption):

$$S = \text{diag}(\tilde{V}) I^*, \quad (4)$$

where the superscript $*$ represents the conjugate, \tilde{V} is the nominal nodal voltage, and I is the nodal current injection. Substituting (4) into (3) and simplifying yields a vector of equivalent power injections in the reduced feeder circuit (S_r).

$$S_r = \mathbf{W} \times S_o, \quad (5)$$

where $\mathbf{W} = \text{diag}(\tilde{V}_r) \times (\mathbf{Z}_r^{-1} \times \mathbf{Z}_{o,\text{CB}})^* \times \text{diag}(\tilde{V}_o)^{-1}$ is the power aggregation weight matrix ($\mathbf{W} \in \mathbb{C}^{M \times M}$).

Separate power injection matrices for the full $S_o \in \mathbb{C}^{M \times 1}$ and reduced circuits $S_r \in \mathbb{C}^{m \times 1}$ are created for loads and generators (including PVs). The reduced impedance network (\mathbf{Z}_r) is formed by simply removing the rows and columns of \mathbf{Z}_o that do not correspond to CB:

$$\mathbf{Z}_r = \mathbf{Z}_o(\text{CB}, \text{CB}). \quad (6)$$

Static capacitors, which have a constant impedance, are retained as part of the network (as a reactance) in the reduced feeder circuit. During conversion of the network from impedance matrix to line and bus elements, the capacitors are either aggregated into the line impedance, or as a shunt impedance on a bus. Note that the calculation of \mathbf{W} depends on both the \mathbf{Z}_{bus} and \mathbf{Y}_{bus} , meaning the inverse of the nodal admittance matrix must be calculated. The reader is directed to reference [24] to ensure that their system is invertible, and thus suitable for this approach.

B. Limitations of [7]

The limitations of circuit reduction techniques for aggregating voltage-controlled devices is demonstrated on the IEEE 13 buses circuit [25] (Fig. 1a), retrofitted with a three-phase PV system PV_{692} on bus 692. To remove bus 692, PV_{692} must be split between the two neighboring buses, creating two new systems ($\text{PV}_{671}, \text{PV}_{675}$) (Fig. 1b). If the inverter of the original PV system was executing volt-var control, the reactive power injection from the inverter should be carried over to the reduced feeder circuit.

However, the power flow results between the original and reduced feeder circuit would then mismatch in voltage (not shown) due to the equivalent PVs experiencing different voltages from the original bus, thus creating different output from the smart inverters. Further, since the aggregation method produces a single PV system on any reduced node (which is the amalgamation of several neighboring PV systems), it is not clear what the volt-var curve should look like for the aggregate system, if the original PV inverters all have different volt-var setpoints.

The methodology introduced in Section (III) addresses this problem with the proposed aggregation formulation for voltage-controlled devices.

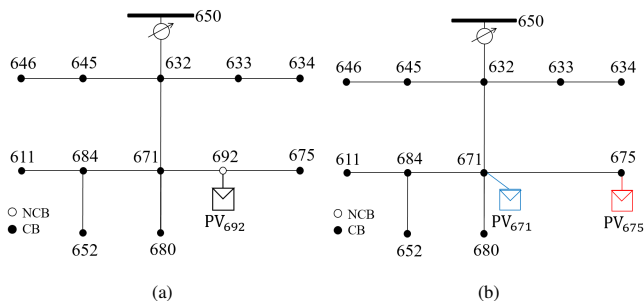


Fig. 1: IEEE 13 bus system. (a) The original feeder circuit was retrofitted with a PV system at bus 692. (b) The reduced feeder circuit with bus 692 removed results in two PV systems on the neighboring buses 671 and 675.

III. AGGREGATION OF VOLTAGE-CONTROLLED DEVICES

A. Primary control schemes

Control of voltage on distribution feeders through primary voltage-control devices such as on-load tap-changing transformers (OLTC) and capacitor banks has been the most common

approach historically [26]. OLTC primary control attempts to maintain a fixed voltage at the transformer's secondary side, by altering tap position, which changes the ratio of secondary to primary side voltage. In contrast, capacitor banks provide voltage regulation through reactive power support.

More recently, regulatory changes from California Rule 21 and IEEE 1547 [21] grid codes allow DER inverters to assist in voltage regulation through modification of their power output. A common scheme is volt-var control, where the inverters typically operate autonomously [27], where var support is determined following a fixed control curve that is programmed into the inverter. An example of such a control curve is given in Fig. 2a, where voltage setpoints (V_a, V_b, V_c, V_d) determine reactive power (var) output.

A common link between all primary control schemes is that each relies on voltage measurements at a distinct point on the circuit, which are typically taken from a single node, or line on the circuit.

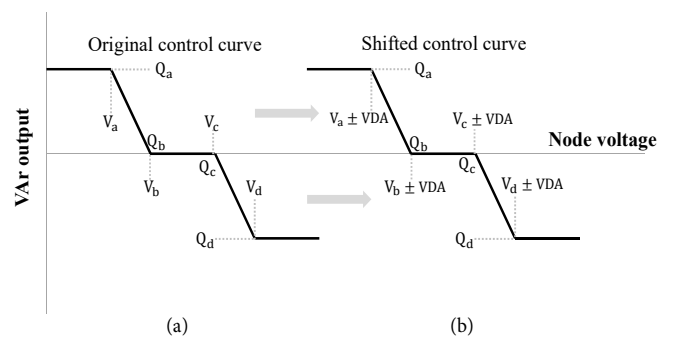


Fig. 2: Depiction of the category B type volt-var curve as defined by the IEEE 1547 standard [21]. Applying the voltage difference addend (VDA) to the volt-var curve results in a shift of the voltage setpoints but maintains the same curve shape and the same reactive power.

This work proposes a method in which primary control actions of a voltage regulator are maintained in the circuit reduction despite the removal of the voltage measurement bus. This is accomplished by preserving the reference voltage measurements even with that bus being removed (see Section III-C). While the examples in this paper consider volt-var control by inverters, the reduction can also be applied to (i) any inverter control scheme depending on voltage measurements, and (ii) capacitor and OLTC control schemes by applying a shift to the measured voltage upon which it is making its action.

B. Preservation of individual PV inverter systems during aggregation

To improve on the methodology summarized in Section II and introduced in reference [7], changes to the reduction formulation must be made. First, we modify the formulation by introducing separate vectors representing power injection (S) for loads and different types of generators, for example PV systems (S_{PV}).

In Eq. (5) as posed in reference [7], PV systems in the reduced feeder circuit ($S_{r_{\text{PV}}}$) were aggregated equivalents of the original PV systems ($S_{o_{\text{PV}}}$) from the full circuit. This approach would require piece-wise volt-var curves to represent the amalgamated system, which are inherently hard to design and inaccurate.

Thus, a novelty of this work is that the movement of individual PV systems (and the corresponding voltages) is traced and separate PV systems at each node are retained during aggregation. To do that, $\mathbf{S}_r \in \mathbb{C}^{m \times M}$ takes the form of a matrix, which maps a PV system on node M in the original circuit to its position on aggregated node m .

$$\mathbf{S}_r = \mathbf{W} \times \text{diag}(S_o), \quad (7)$$

Note that Eq. 7 differs from Eq. 5 in the diagonal on the power injection vector. Each row of the matrix \mathbf{S}_r represents a bus on the reduced feeder circuit, and each column represents a bus in the original feeder circuit. Each entry represents a single PV system that is transferred from the original bus to a reduced bus. Therefore, this approach allows co-locating several PV systems – each with a different solar irradiance input and power factor – at a single bus in the reduced system. Summing the rows of \mathbf{S}_r results in the vector form of Equation (5) (i.e. $\sum \mathbf{S}_r = S_r$).

PV systems are composed of PV panels with an aggregate DC capacity rating and an inverter with an AC capacity rating, which generally differs from the PV DC ratings. Since voltage control is proportional to the headroom in the inverter, both the inverter AC rating and the PV DC capacity rating need to be tracked. PV inverter AC ratings are aggregated separately as

$$\bar{\mathbf{S}}_r = \mathbf{W} \times \text{diag}(\bar{S}_o), \quad (8)$$

where the bar indicates the inverter AC ratings. This means that a separate vector (\bar{S}) which is composed of the AC ratings of the PV inverters must also be mapped during reduction.

Equivalent to preserving PV systems, this novel approach also allows preserving individual loads and generators (as opposed to using a combined equivalent at each bus). Therefore details unique to each load can be retained. For example, two state models or ZIP loads that operate according to characteristic parameters could be preserved after movements of the loads in the reduced model. Since this paper focuses on voltage control, the accuracy improvement through these more advanced load models will be demonstrated in future work.

The above modifications to the reduction methodology that track the movement of PV systems (7) and inverters (8) yield the final reduction methodology applied in this paper. However, as demonstrated in Section II-B without modifying the voltage based control scheme the power flow of the two circuits will still diverge. The remedy to this is derived in Section III-C.

C. Inverter volt-var curve shift

The var output of an inverter depends on the voltage of its original bus. However, when the inverter is moved to a new bus as part of the reduction, the voltage it measures changes, modifying the var output of the inverter.

To remedy this, the inverter voltage control curve (volt-var, Fig. 2b) is "shifted" by the modeled difference in voltage between the original bus and the new bus. Thus, the inverter output will depend on the voltage on the original bus, as opposed to the voltage on the new bus, preserving the power flow to be the same. Hereafter, the voltage shift is referred to as the voltage difference addend (VDA).

The VDA is estimated from voltage drop equations (see references [4, 6] for alternative uses of these equations). For any three bus system with neighboring buses i, j, k , where j is between buses i and k , we can write the p -phase voltage vector for buses j and k as:

$$V_j = V_i + \mathbf{Z}_{ij}(I_j + I_k), \quad (9)$$

$$V_k = V_j + \mathbf{Z}_{jk}I_k, \quad (10)$$

where $V \in \mathbb{C}^{p \times 1}$ and $I \in \mathbb{C}^{p \times 1}$ are the vectors of voltages and current injections of the p -phase bus, respectively. $\mathbf{Z} \in \mathbb{C}^{p \times p}$ is the full impedance matrix of the line connecting the buses, where the diagonal elements denote self impedances and off-diagonal elements denote mutual impedances between different phases of the line. Fig. 3 shows a schematic of the system.

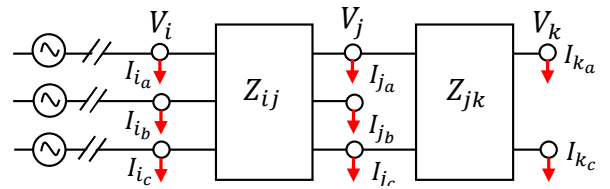


Fig. 3: Depiction of 3 bus subsection of the feeder in which the middle bus, B_j , is connected upstream to a 3-phase bus B_i and connected downstream to a 2-phase bus B_k . The red arrows represent current flow out of the nodes.

We can define the voltage change between neighboring buses i, j , and k as:

$$\Delta V_{ji} = V_j - V_i = \mathbf{Z}_{ij}(I_j + I_k), \quad (11)$$

$$\Delta V_{kj} = V_k - V_j = \mathbf{Z}_{jk}I_k, \quad (12)$$

$$\Delta V_{ki} = V_k - V_i = \mathbf{Z}_{jk}I_k + \mathbf{Z}_{ij}(I_j + I_k). \quad (13)$$

For an inverter moved between these neighboring buses, Equations (11)-(13) yield the appropriate VDA. However, determining these equations becomes algorithmically complex for larger systems with differing topologies and large inverter movement distance.

A more general approach is using the nodal voltage equations as

$$V_o = \mathbf{Z}_o \times I_o. \quad (14)$$

The voltage difference between any two buses can quickly be determined by subtracting the rows of Equation (14) (e.g. $\Delta V_{6,1}$ denotes row 6 minus row 1). Thus, for each PV system moved from bus i in the original circuit to bus k in the reduced circuit, the appropriate VDA for the loading (current injections) can be calculated by subtracting row i from row k .

IV. EXTENDING SECTION III TO TIME SERIES SIMULATION OF THE AGGREGATED NETWORK

A. Framework overview

Quasi-static time series (QSTS) analysis solves steady state power flow sequentially under changing demand and generation. However, the VDA methodology as introduced above is only applicable for the loading considered during the reduction (here the rated loading). However, for feeders with variable loading – and at high PV penetration the loading may even be negative and vary significantly between day and night – the assumption

of a feeder at constant loading may introduce larger reduction errors in the voltage at the reduced buses. Thus, the ability of a reduction technique to handle changes in load is essential.

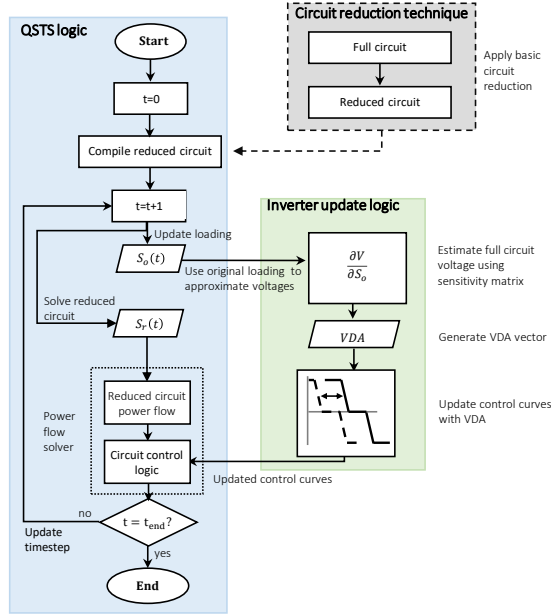


Fig. 4: Flowchart describing the QSTS logic introduced in this work (left, blue box), which employs a parallel updater for the VDA (right, green box). The circuit reduction, which is executed just once, is shown in the top right, gray box. The dashed black lines indicate that the reduction is independent of the QSTS framework. Note, at each time step, the loading of the original circuit (S_o) is used to inform the VDA estimation, while the reduced circuit is solved in the powerflow solver.

To accomplish this, we introduce an integrated framework, which computes the VDA in real time during the QSTS. This framework is visualized through the flowchart in Fig. 4. On the left hand side, a typical QSTS logic solves the power flow for the reduced feeder circuit. After the initial compilation of the circuit, the solver iteratively solves the power flow for a predefined number of time-steps for known loading conditions. Within the solution loop at each time step, the loading is given as input and the power flow solution is obtained. The power flow solution is then input to the controller, which iteratively solves the control problem. The loop ends after all time steps have been solved.

In parallel with the power flow solver, the VDA for each inverter is updated. The updater uses a fast voltage estimation technique, which considers the loading for the original feeder circuit at the present time step to estimate the change in the nodal voltage of each bus in the original feeder circuit. The VDA for each inverter volt-var curve and each time step is determined by the (estimated) voltage difference between the original PV bus and the bus it is aggregated to in the reduced feeder circuit.

B. Voltage estimation through sensitivities

An estimate of nodal voltages of the full circuit considering the actual loading is needed to estimate the VDA. Fast voltage estimation is needed in a number of power systems applications and is often achieved with low error using voltage sensitivities or distribution factors that relate changes in voltages to changes in loading [28–32].

Non-linear sensitivity equations model the effect of varying load consumption (and equivalently for generator output) on the voltage of each bus on the network. All loads are set to operate at rated capacity. Next, the apparent power for each load is varied independently from zero to 100% of its rated power output in increments of 2%, and the voltage of each bus on the circuit is recorded. This process is repeated for every load and generator element in the feeder model. Mathematically, for any bus $m \in M$, we model the nodal voltage change due to change in apparent power (S) for a given load $\ell \in L$ (a similar form represents changes in voltage to changes in generation), using a polynomial of degree C as

$$V^{(\ell,m)} = a_o^{(\ell,m)} + a_1^{(\ell,m)} S_\ell + a_2^{(\ell,m)} S_\ell^2 + \dots + a_C^{(\ell,m)} (S_\ell)^C, \quad (15)$$

where a represents the coefficients of the polynomial. The term $a_o^{(\ell,m)}$ represents the voltage of the bus m at full load consumption. Thus, the remaining portion of the right hand side gives the voltage deviation caused by a drop in the loading (S_ℓ). Therefore, we can write

$$\Delta V^{(\ell,m)} = a_1^{(\ell,m)} S_\ell + a_2^{(\ell,m)} S_\ell^2 + \dots + a_C^{(\ell,m)} S_\ell^C. \quad (16)$$

Note that a first order polynomial recovers the linear sensitivity factors commonly found in the literature. The extra terms account for nonlinearity in load models. We fit Eq. (16) with a second order polynomial. As outlined in Appendix A, the second order fit provides the most accurate fit for this circuit.

The polynomial fitting is completed off-line and represents a fixed feeder configuration. The overall number of the power flow calculations to calculate the sensitivity $\Delta V^{(\ell,m)}$ for the real feeder in the following case study with 364 PVs and 471 loads is $50 \times (364 + 471)$, which is only 4% of the power flow calculations needed for an annual analysis at 30 s timesteps ($120 \times 24 \times 365$), which is a typical use case for network reduction.

$$\frac{\partial V}{\partial S} = \begin{matrix} & a_C^{(\ell_1,m_1)} S_{\ell_1}^C & \dots & a_C^{(\ell_1,M)} S_{\ell_1}^C \\ & a_2^{(\ell_1,m_1)} S_{\ell_1}^2 & \dots & a_2^{(\ell_1,M)} S_{\ell_1}^2 \\ a_1^{(\ell_1,m_1)} S_{\ell_1} & \dots & a_1^{(\ell_1,M)} S_{\ell_1} & \\ \vdots & \vdots & \vdots & \\ a_1^{(L,m_1)} S_L & \dots & a_1^{(L,M)} S_L & \\ a_1^{(g_1,m_1)} S_{g_1} & \dots & a_1^{(g_1,M)} S_{g_1} & \\ \vdots & \vdots & \vdots & \\ a_1^{(G,m_1)} S_G & \dots & a_1^{(G,M)} S_G & \end{matrix} \begin{matrix} S_L^C \\ S_L^2 \\ S_L \\ S_{g_1}^2 \\ S_G^2 \\ S_{g_1}^C \\ S_G^C \end{matrix}$$

Fig. 5: The three dimensional equation used to estimate the change in nodal voltage as a function of the change in loading and generation. The current state of loading for each load (S_ℓ) and generator (S_g) is input to the polynomial and the voltage change is determined. The total change in voltage from full loading is determined by summing the individual contributions of each load.

To estimate voltage systematically, a three dimensional function is created, as depicted in Fig. 5. The marginal change in voltage at each bus from each load is represented by the matrix

$\partial\mathbf{V}/\partial\mathbf{S} \in \mathbb{C}^{M \times (L+G)}$, where L and G are the number of loads and generators in the system, respectively. The total predicted change in nodal voltage ($\partial V \in \mathbb{C}^{M \times 1}$) is found by summing along the L and G dimensions. The final predicted voltage vector ($\tilde{V} \in \mathbb{C}^{M \times 1}$) is the cumulative change of the voltage of each bus at full loading versus actual loading as $\tilde{V} = a_o + \partial V$.

The VDA for a PV system that was moved from a bus m_o in the original feeder circuit to a bus m_r in the reduced feeder circuit can then be calculated as

$$\text{VDA} = \tilde{V}_{m_o} - \tilde{V}_{m_r}. \quad (17)$$

In the model, all loads and generators (except for PV inverters) operate at constant power factor, such that changes in real power correlate to reactive power. For applications with loads at variable power factor, a separate entry for both the active and reactive component of the load should be considered in $\partial\mathbf{V}/\partial\mathbf{S}$.

C. Benchmark Feeder

To test the accuracy of the method, we compare the voltage prediction to real power flow results for 53 days (11/25/2014 to 1/16/2015) on a real unbalanced California medium voltage distribution feeder (Fig. 9). The feeder was introduced in [4]. The feeder has 621 multi-phase buses, two distribution transformers, one large capacitor bank (1350 kvar), 364 distributed rooftop PV systems, and 471 loads. As such, this feeder has very few null injection points. All loads are modeled as a constant power load model. A PV penetration of 150% (i.e. the total AC nameplate capacity of the PV systems divided by the total rated load in the circuit) was used to create significant over-voltage conditions representative of future high PV penetration scenarios. The feeder lines are modeled with shunt capacitance, mutual coupling components, and all neutral connections are assumed to be grounded perfectly. The volt-var curve is a category B type curve that includes a deadband (Fig. 7a), according to the IEEE 1547 2018 standard [21]. The voltage setpoints are $v_a = 0.95$, $v_b = 0.98$, $v_c = 1.02$, and $V_d = 1.05$. A reactive power availability of 100% was used, which exceeds the 44% specified in the IEEE standard. Maximum reactive power will result in a worst-case scenario for feeder reduction, since voltage errors are amplified for larger reactive power injection / absorption. All inverters are sized according to a 1.05 AC/DC ratio. Real power is not curtailed to prioritize vars.

Each load on the feeder operates under the same time-series shape scaled by its peak load, while each PV time-series is uniquely determined using a sky imager according to the method introduced in [4]. The irradiance and load time-series are of 30 s resolution, which mark the resolution of the power flow simulation over the period. The rationale behind using 30 s time resolution is discussed in reference [4].

The mean and confidence intervals for the voltage estimation error (i.e. difference in nodal voltage and actual power flow solution ($V_{\text{predict}} - V_{\text{pf}}$) are given in Fig. 6. For the 53 days, the maximum voltage estimation error is on the order of 10^{-4} p.u.. The estimation error is correlated to the shape of load consumption (00:00-07:00; 17:00-24:00) and PV generation (08:00-16:00).

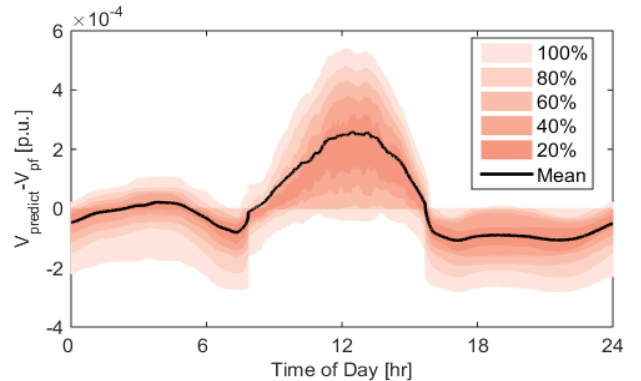


Fig. 6: Confidence interval (0-100%) of the bus-by-bus voltage estimation error over a 53 day test period. The voltage estimation is the difference between the voltage estimated per Section IV-C and the voltage from power flow.

V. CASE STUDIES

A. Snapshot case study

The example introduced in Section II-B is extended here to demonstrate application of the VDA, without the time series framework. The PV system PV_{692} in Fig. 1a is rated at 600 kW_{DC} and 600 kW_{AC} and outputs half of its rated AC power or 300 kW (100 kW per phase). The load on bus 692 is 171 kW. All loads are operating at their rated power (i.e. highest loading). OpenDSS [33] is used to solve the power flow and apply volt-var control. The volt-var curves of Section IV-C are used.

The VDA modified control curves for each phase of the resulting PV systems are given in Fig. 7. In all phases, we observe that VDA is positive for the downstream bus (675) and negative for the upstream bus (671). A larger shift is noted for the control curves on phase A of the inverters, relative to the other two phases, indicating a larger voltage difference resulting from more loading on that phase.

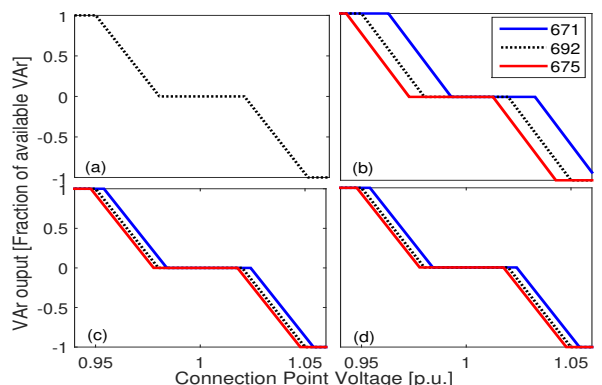


Fig. 7: Volt-var curves for the PV systems on the IEEE 13 bus system. (a) The three phase curve for the original system PV_{692} for reference. The VDA modified curve for PV_{671} and PV_{675} for (b) Phase A, (c) Phase B, and (d) Phase C.

For system equivalence, the two smaller PV inverters on each phase in the reduced feeder circuit should cause equivalent nodal voltages and equivalent reactive power support. A comparison between the reduced and original feeder voltage is shown for the uncontrolled (Fig. 8a) and controlled power flows (Fig. 8b). Without volt-var control, bus 692 experiences an ANSI voltage violation (< 0.95 p.u.) for both Phases A and C. Volt-var control

raises the feeder voltages. Consistent with our prior works [4, 7], the reduction produces insignificant errors (6.5×10^{-5} p.u.) for a circuit without volt-var control. The novelty in this paper is the small error in the nodal voltage after volt-var control is applied. For this particular snapshot, the reduction voltage error actually decreases with volt-var control, which is expected since volt-var reduces the range of feeder voltages.

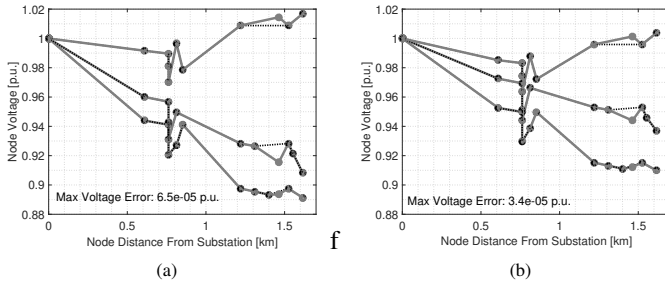


Fig. 8: Three-phase voltage as a function of distance from the substation for all buses of the original IEEE 13-bus circuit (gray) and the reduced feeder circuit (dashed black). (a) Power flow without inverter voltage control. (b) Power flow with volt-var control from PV inverters. The removed bus 692 is at a distance of 1.48 km and its gray dot therefore does not have a corresponding black dot.

The total reactive power produced from the inverters of PV_{671} and PV_{675} (reduced feeder circuit) at each phase is 0.99, 1.05, 1.01 times the reactive power output from the inverter on PV_{692} (original feeder circuit). The largest (5%) relative error for Phase B is due to the normalization of a small absolute number (i.e. negligible reactive power output). The reactive power provided from the substation and the reactive power losses for the reduced feeder circuit are nearly identical to the full feeder (ratios of 1.0001 and 1.0004, respectively). The small reactive power error is attributed to errors in calculating VDA at the reduced bus assuming a static current equal to the rated current of the load, which is corrected using the approach in Section IV.

B. QSTS case study

1) *Study overview:* The VDA time series framework is tested on the real unbalanced medium voltage California distribution feeder, introduced in Section IV-C for the 24 hour period on 11/21/2014. The study day represents worst-case conditions, since it contains a large range of net loads from a mid-day low to the evening peak, and the irradiance profile varies due to partial cloud cover causing rapid swings in voltage and inverter var output. The VDA was updated at every time step given the actual load and generator power from the polynomial in Equation (16).

The feeder is reduced to 20 randomly selected buses from the original 621 (97% reduction) as shown in Fig. 9. Due to inverter splitting, the original 364 inverters were mapped to 1200 equivalent inverters on the reduced feeder circuit (see Equation (7) and Section V-A).

Fig. 10 shows timeseries of maximum and minimum feeder voltages. During the middle of the day the maximum voltage reaches 1.1 p.u., which exceeds the upper voltage limit of the deadband (1.02 p.u.; Fig. 7a). When volt-var control is applied, the voltage is lowered to 1.045 p.u. During the evening peak loading ($\approx 17:00-23:00$), the voltage reaches a low of 0.92 p.u.

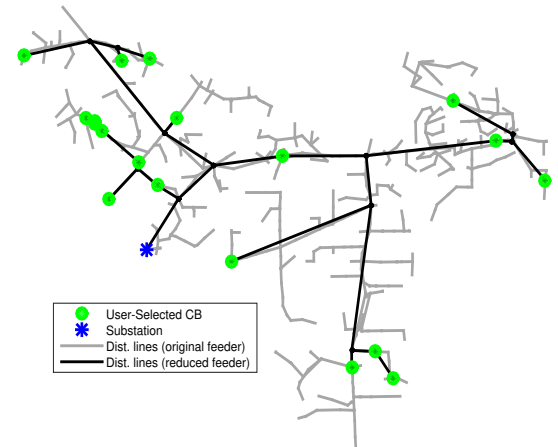


Fig. 9: The original and reduced feeder circuit topology. Given the high concentration of PV systems in the original feeder circuit, each remaining CB contains a number of inverters.

When volt-var control is applied, the minimum voltage is raised to 0.98 p.u.

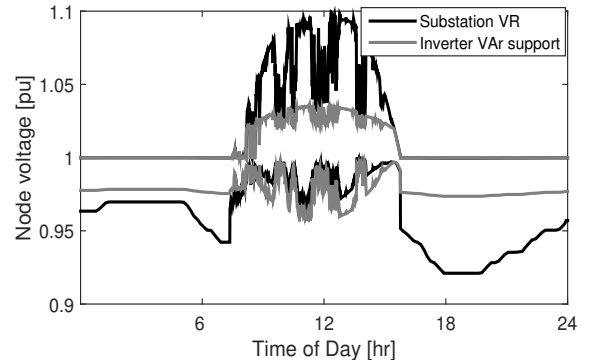


Fig. 10: Maximum and minimum feeder voltage time-series for the full feeder on 11/21/2014: (black) voltage control only by the substation OLTC (no inverter control); (gray) volt-var controlled inverters.

2) *Error in var output and voltage:* The error in total reactive power output in the reduced feeder circuit (not shown) correlates with the amount of total reactive power output. Var absorption, which coincides with large solar PV active power injection, causes greater errors. This is consistent with Fig. 6, where the largest deviation in estimated voltage was observed midday with high solar irradiance and the fact that the var output errors are correlated to voltage estimation errors.

The nodal voltage error (Fig. 12) incurred from reduction alone (i.e. the circuit without volt-var control) is generally small, with a maximum error magnitude of 4×10^{-3} p.u. With volt-var control, the greatest voltage deviations are again observed during periods of high irradiance, since voltage errors are proportional to errors in reactive power output. Generally, the error incurred through including the VDA is on the same order as the error due to reduction. In some cases, the error post-voltage control is reduced, indicating that the VDA methodology does not introduce additional error to the reduction methodology, on average.

The impetus for applying the VDA becomes clear when comparing the methodology against a scenario where no VDA is applied, as shown in Fig. 11. Instead, we reduce the circuit model, leaving the original setpoints of the volt-var curve. Here,

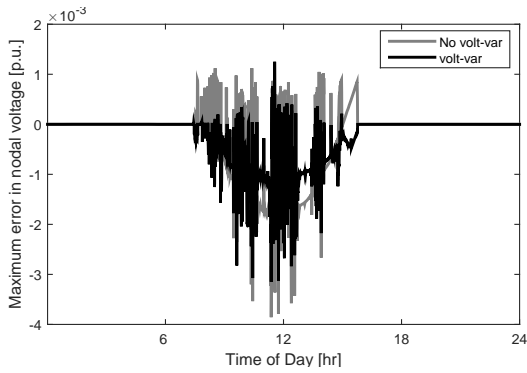


Fig. 11: Maximum nodal voltage error between the reduced and original feeder circuit (black) with and (gray) without volt-var control

we can see leaving the original setpoints produces nodal voltages errors as high as -0.06 p.u., which is more than half the ANSI C84.1 tolerance of acceptable voltage limits (i.e. 0.95 p.u. and 1.05 p.u.). The mean error is bounded between ± 0.03 p.u. In contrast, the proposed method produces a maximum error of 0.003 p.u., with a mean error bounded to 0.0008 p.u.

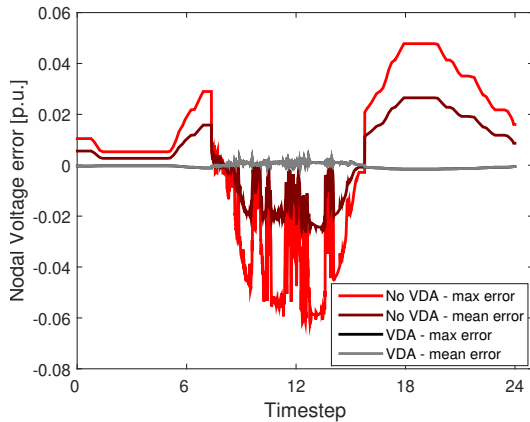


Fig. 12: Voltage error (maximum and mean) for the reduced model when considering the VDA adjustment to inverter setpoints, and when using the original inverter setpoints without any adjustment (No VDA). Note the mean error when considering the VDA is hidden behind the maximum error in the plot.

3) *Run-time considerations and update logic:* Applying the VDA at every time step increases simulation time to 2.5 times compared to the annual simulation of the full circuit (Fig. 13, abscissa of 100), defeating the purpose of feeder reduction. To achieve computational savings, we tested a modification that allowed the VDA to be updated at a lower (equally spaced) frequency. Updating the VDA less than 33% of the time (every 3 steps, or 960 total) produces simulation time savings compared to full feeder simulations. In the extreme, updating the VDA only once at the first time step yielded time savings of 63% compared to annual simulations of the full circuit, consistent with time savings in [4] without the VDA method.

However, when the VDA is not updated and the system loading changes (as is a signature of QSTS simulations), power flow convergence issues arise, since the inverter curves no longer match the system conditions. Specifically, OpenDSS is not able to find a solution when applying the control scheme based on the VDA curves of the last update due to control adjustments

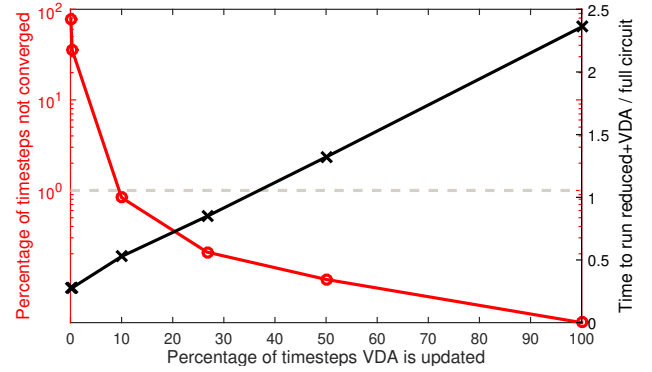


Fig. 13: Double y -axis plot comparing time savings and power flow convergence with the frequency of VDA updates. Left, red (log scale): Percentage of time steps, when the power flow solution does not converge due to an insufficient update frequency of the VDA curves. Updating the VDA every time step (i.e. 100%) results in no convergence issues. Right, black: Time to run the reduced feeder circuit and update the VDA normalized by the time required to run the full circuit. The grey dashed line indicates the time required to run the full circuit.

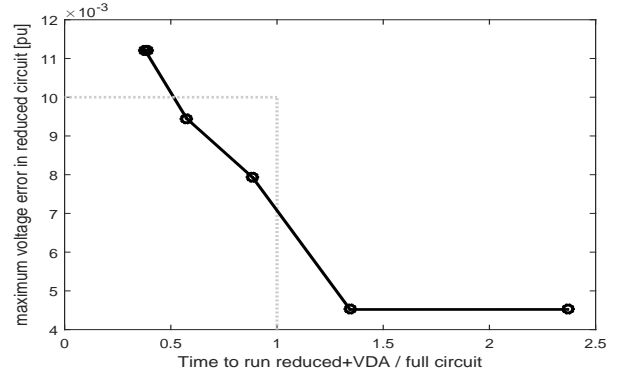


Fig. 14: Maximum voltage error versus the time to run the circuit for a number of VDA update frequencies (Fig 13) after implementing the logic preventing convergence issues. The gray dashed box indicates the region with time savings and errors less than 10% (i.e. 0.01 p.u.).

creating an infeasible operating point (see reference [34] for a discussion on power flow non-convergence). Considering Fig. 13, there is no update frequency less than 100%, that guarantees power flow convergence and produces time savings. To overcome this issue, in the presence of non-convergence, the VDA should be updated and the simulation for the non-convergent time step should be repeated. This adds a few extra VDA updates to the overall solution, but guarantees convergence for all time steps.

Fig. 14 confirms that time savings are a trade-off with voltage error and that run times reductions up to 50% compared to the full circuit are achievable while producing less than 10% errors (i.e. 0.01 p.u.). Future work will focus on an adaptive solver for optimally choosing the number of time steps to update the VDA to realize maximum time savings and minimize voltage error. For instance, one strategy could be to update VDA less often when net load changes are small such as at night or in overcast conditions.

VI. CONCLUSIONS

In this work, voltage-controlled inverters are included in circuit reduction. Traditionally, voltage-controlled devices required preserving additional buses in the reduced feeder circuit, as their voltage information is needed as input to the controlled devices. This limits the circuit reduction time savings, considering the

large penetration of voltage-controlled DER devices in modern distribution networks. The circuit reduction method with voltage estimation is demonstrated for PV inverters with volt-var control. However, the methodology can be extended to other control schemes that depend on local voltage measurements and also other voltage-controlled equipment, such as OLTCs and capacitors.

The methodology improves the circuit reduction technique first proposed in reference [7] to retain individual inverters on each aggregated bus, as opposed to the traditional composite. The control curve of each inverter is shifted by a voltage difference added (VDA) to link the expected voltage on the original inverter bus to the measured voltage on the reduced bus. A general voltage sensitivity estimation technique generates the shift for time series application with changing feeder loading.

The method is shown to be highly accurate for a 24 hour simulation on a real unbalanced California distribution feeder with 97% of the circuit removed. The maximum nodal voltage error for the period is always less than 2.5×10^{-3} p.u., which is nearly identical to the error due to reduction itself. Trade-offs between time savings, voltage error, and the voltage estimation update frequency were discussed.

Though the method derivation is general enough to consider advanced models such as zip and two-stage loads, as well as variable power factor generators, these were not tested directly in the work, and will be included in future work.

APPENDIX A VOLTAGE SENSITIVITY MODELING

A. Modeling bus voltage versus load consumption

This appendix discusses the effect of load model and polynomial fit on the sensitivity estimation. Voltage sensitivity and distribution factors for voltage prediction have been analyzed analytically in references [28, 30]. Here, a numerical approach for the feeder and the methodology considered is given. In Fig. 15, the bus with the largest voltage change in the circuit (bus 1008) is analyzed. For three load models, all loads are varied from no consumption to two times the rated loading for purpose of demonstration, and the change in bus voltage is recorded.

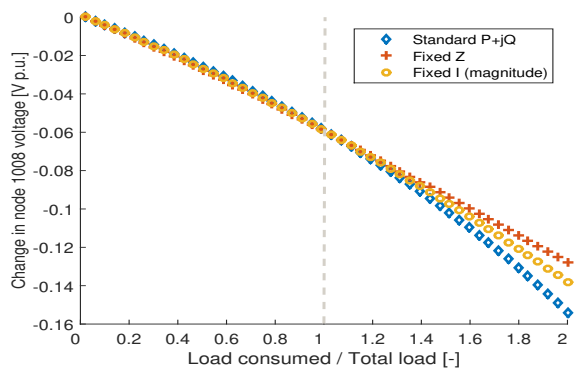


Fig. 15: Voltage change for bus 1008 due to the change from no loading to increased total feeder loading. Three different load models are examined for each load: i) Constant power loads; ii) constant impedance loads; iii) Constant current magnitude loads.

Polynomials of order 1-3 are fit to the lines. The goodness of fit of these lines are represented using common statistical

TABLE I: Goodness of fit measures for increasing order of polynomial model fits (15) to the change in voltage of bus 1008 with respect to change in feeder loading (Fig. 15).

	Fit order	P+JQ	Fixed Z	Fixed I
Linear	SSE	1.4×10^{-3}	1.5×10^{-5}	4.7×10^{-7}
	RMSE	5.5×10^{-3}	5.6×10^{-4}	1.0×10^{-4}
	r^2	0.984	0.999	0.999
Quadratic	SSE	7×10^{-5}	3.6×10^{-6}	1.3×10^{-8}
	RMSE	2.8×10^{-4}	2.75×10^{-4}	1.2×10^{-5}
	r^2	0.998	0.999	0.999
Cubic	SSE	4.1×10^{-4}	2.4×10^{-7}	8.4×10^{-10}
	RMSE	2.9×10^{-3}	7.2×10^{-5}	4.3×10^{-6}
	r^2	0.995	0.999	0.999

measures such as i) sum of squares due to error (SSE); ii) Coefficient of determination (r^2); iii) Root mean square error (RMSE). Both Table I and Fig. 15 show that the load model affects the linearity of the change in voltage with loading, where the constant impedance load model is the most linear and the constant power ($P + jQ$) is the most non-linear. Regardless, for all load models, the quadratic polynomial provides an accurate fit and is chosen in this work.

REFERENCES

- [1] H. Oh, "Aggregation of buses for a network reduction," *IEEE Trans. Power Syst.*, vol. 27, no. 2, pp. 705–712, 2012.
- [2] —, "A new network reduction methodology for power system planning studies," *IEEE Trans. Power Syst.*, vol. 25, no. 2, pp. 677–684, 2010.
- [3] D. Santos-Martin and S. Lemon, "Simplified modeling of low voltage distribution networks for pv voltage impact studies," *IEEE Trans. Smart Grid*, vol. 7, no. 4, pp. 1924–1931, 2015.
- [4] Z. K. Pecanak, V. R. Disfani, M. J. Reno, and J. Kleissl, "Multiphase distribution feeder reduction," *IEEE Trans. on Power Sys.*, vol. 33, no. 2, pp. 1320–1328, 2017.
- [5] A. P. Reiman, T. E. McDermott, M. Akcakaya, and G. F. Reed, "Electric power distribution system model simplification using segment substitution," *IEEE Trans. Power Sys.*, vol. 33, no. 3, pp. 2874–2881, 2017.
- [6] M. J. Reno, K. Coogan, R. Broderick, and S. Grijalva, "Reduction of distribution feeders for simplified pv impact studies," in *Photovoltaic Specialists Conference (PVSC), 2013 IEEE 39th*.
- [7] Z. K. Pecanak, V. R. Disfani, M. J. Reno, and J. Kleissl, "Inversion reduction method for real and complex distribution feeder models," *IEEE Trans. on Power Sys.*, vol. 34, no. 2, pp. 1161–1170, 2018.
- [8] S. M. Ashraf, B. Rathore, and S. Chakrabarti, "Performance analysis of static network reduction methods commonly used in power systems." IEEE, 2014.
- [9] J. B. Ward, "Equivalent circuits for power-flow studies," *Electrical Engineering*, vol. 68, no. 9, pp. 794–794, 1949.
- [10] G. Kron, *Tensor analysis of networks*. J. Wiley & Sons, 1939.
- [11] P. Dimeo, "Nodal analysis of power systems," 1975.
- [12] J. Machowski, J. Bialek, and J. R. Bumby, *Power system dynamics and stability*. John Wiley & Sons, 1997.

- [13] A. Morched and V. Brandwajn, "Transmission network equivalents for electromagnetic transients studies," *IEEE Trans. Power App. Syst.*, no. 9, pp. 2984–2994, 1983.
- [14] A. Morched, L. Marti, and J. Ottevangers, "A high frequency transformer model for the emtp," *IEEE Trans. Power Del.*, vol. 8, no. 3, pp. 1615–1626, 1993.
- [15] A. Morched, J. Ottevangers, and L. Marti, "Multi-port frequency dependent network equivalents for the emtp," *IEEE Trans. on Power Del.*, vol. 8, no. 3, pp. 1402–1412, 1993.
- [16] D. Chaniotis and M. Pai, "Model reduction in power systems using krylov subspace methods," *IEEE Trans. on Power Sys.*, vol. 20, no. 2, pp. 888–894, 2005.
- [17] Z. Zhu, G. Geng, and Q. Jiang, "Power system dynamic model reduction based on extended krylov subspace method," *IEEE Trans. on Power Sys.*, vol. 31, no. 6, pp. 4483–4494, 2016.
- [18] C. Huang, K. Zhang, X. Dai, and W. Tang, "A modified balanced truncation method and its application to model reduction of power system," in *2013 IEEE Power & Energy Society General Meeting*. IEEE, 2013, pp. 1–5.
- [19] S. Ghosh and N. Senroy, "Balanced truncation approach to power system model order reduction," *Electric Power Components and Systems*, vol. 41, no. 8, pp. 747–764, 2013.
- [20] C. Huang, K. Zhang, X. Dai, and W. Wang, "Model reduction of power systems based on the balanced residualization method," in *2012 IEEE PESGM*. IEEE, 2012, pp. 1–7.
- [21] "Ieee standard for interconnection and interoperability of distributed energy resources with associated electric power systems interfaces," *IEEE Std*, pp. 1547–2018, 2018.
- [22] E. Solutions, "California distributed generation statistics and charts." [Online]. Available: <https://www.californiadgstats.ca.gov/charts/>
- [23] H. Kikusato, T. S. Ustun, J. Hashimoto, and K. Otani, "Aggregate modeling of distribution system with multiple smart inverters," in *2019 International Conference on Smart Energy Systems and Technologies (SEST)*. IEEE, 2019, pp. 1–6.
- [24] M. Bazrafshan and N. Gatsis, "Comprehensive modeling of three-phase distribution systems via the bus admittance matrix," *IEEE Trans. on Power Sys.*, vol. 33, no. 2, pp. 2015–2029, 2017.
- [25] "Ieee test circuits description." [Online]. Available: <https://ewh.ieee.org/soc/pes/dsacom/testfeeders>
- [26] T. Gönen, *Electric power distribution system engineering*. McGraw-Hill New York, 1986.
- [27] Z. K. Pecanak, J. Kleissl, and V. R. Disfani, "Smart inverter impacts on california distribution feeders with increasing pv penetration: A case study," in *2017 IEEE PESGM*.
- [28] R. Baldick, "Variation of distribution factors with loading," *IEEE Trans. Power Syst.*, vol. 18, pp. 1316–1323, 2003.
- [29] S. Singh and S. Srivastava, "Improved voltage and reactive power distribution factors for outage studies," *IEEE Trans. Power Syst.*, vol. 12, no. 3, pp. 1085–1093, 1997.
- [30] K. Christakou, J.-Y. LeBoudec, M. Paolone, and D.-C. Tomozei, "Efficient computation of sensitivity coefficients of node voltages and line currents in unbalanced radial electrical distribution networks," *IEEE Trans Smart Grid*, vol. 4, no. 2, pp. 741–750, 2013.
- [31] A. J. Wood and B. F. Wollenberg, *Power generation, operation, and control*. John Wiley & Sons, 2012.
- [32] M. U. Qureshi, S. Grijalva, M. J. Reno, J. Deboever, X. Zhang, and R. Broderick, "A fast scalable quasi-static time series analysis method for pv impact studies using linear sensitivity model," *IEEE Trans on Sust. Energy*, 2018.
- [33] R. C. Dugan and T. E. McDermott, "An open source platform for collaborating on smart grid research," in *PESGM, 2011 IEEE*. IEEE, 2011, pp. 1–7.
- [34] F. Dong, T. Kostyniak, and B. Lam, "Dealing with power flow solution difficulties," *Siemens, PTI eNewsletters, USA*, 2012.