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DISCLAIMER

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for Protein Crystallography

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Two-dimensional pixel array image sensor for protein crystallography

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ABSTRACT

A 2D pixel array image sensor module has been designed for time resolved Protein Crystallography. This smart pixels detector significantly enhances time resolved Laue Protein crystallography by two or three orders of magnitude compared to existing sensors like films or phosphor screens coupled to CCDs. The resolution in time and dynamic range of this type of detector will allow to study the evolution of structural changes that occur within the protein as a function of time. This detector will also considerably accelerate data collection in static Laue or monochromatic crystallography and make better use of the intense beam delivered by synchrotron light sources.

The event driven pixel array detectors, based on the Column Architecture, can provide multiparameter information (energy discrimination, time), with sparse and frameless readout without significant dead time.

The prototype module consists of a 16x16 pixel diode array bump-bonded to the integrated circuit. Different detector materials (Silicon, CdZnTe) are evaluated. The detection area is 150x150 μm^2 connected to the readout electronics. The individual pixel processor consists of a low-noise amplifier shaper followed by a differential threshold comparator which provides the counting of individual photons with an energy above a programmable threshold. To accommodate the very high rates, above $5 \times 10^8/cm^2/s$, each pixel processor has a 3 bit pre-scaler which divides the event rate by 8. Overflow from the divider which defines a pseudo fourth bit will generate a readout sequence providing the pixel address. Addresses, generated locally as analog signals, are converted off-chip and used to increment a location in an histogramming memory to generate the computerized image of the Laue diagram.

KEYWORDS: Crystallography, Pixel detector, X-ray imaging, Sensor, CdZnTe

1. INTRODUCTION

Synchrotron radiation offers several advantages for the study of the structure of biological molecules, including higher flux, higher brightness, and a broad bandpass. This allows for more rapid data collection rates, more accurate data, the ability to look at microcrystals, and the use of multiple-wavelength and polychromatic methods. To optimally utilize the rapid data collection capabilities of synchrotron radiation sources, detectors which can rapidly detect and output the diffraction information are necessary. Furthermore time-resolved x-ray crystallography using polychromatic radiation (Laue diffraction) from a synchrotron source offers an approach to studying time-dependent biological processes in protein crystals. Monochromatic and polychromatic biological crystallography, as well as solid state diffraction experiments, place great demands on the detector system, as well as on the source and the sample.

This work targets the optimization and initiation of construction over the next three years of a 15x15 cm detector containing one million 150x150 micron pixels. This detector will offer the sensitivity, dynamic range, and spatial resolution that are optimal for the use at high-brightness synchrotron sources for diffraction experiments in biological crystallography and materials science applications. Furthermore the rapid rate of data collection and transfer optimizes the efficient utilization of these synchrotron radiation sources. This detector will also possess the temporal resolution required to perform x-ray crystallographic experiments on biologically relevant time scales down to milliseconds. This detector will offer several advantages over present detector types such as charge coupled devices and imaging plates, including the ability to accurately record extremely weak and extremely strong reflections simultaneously, a markedly decreased point spread function, single photon counting capabilities, and rapid throughput of data. This detector will not only be applicable to problems in biological structure, but to solid state diffraction as well. It represents the next logical step in detector development after the progression from film to imaging plates to present day charge coupled devices.

2. PIXEL ARCHITECTURE

The Protein Crystallography Pixel (PCP) consists of monolithic arrays of reverse biased semiconductor diodes hybridized with an Application Specific Integrated Circuit (ASIC) instrumenting each diode in the array. The Silicon diode array (or CdZnTe at higher photon energies) is bump-bonded to the integrated circuit forming a module (figure 1). The column based architecture allows the IC's output pads to be located on one side of the module which makes easier the assembly of the detection area.

A 16x16 prototype array has been tested and preliminary results are presented here. The readout, based on the column architecture principle[1], will accept high counting rates. This detector will allow time resolved Laue Crystallography to be performed in a frameless operation mode, with zero dead time.

The readout electronics architecture is shown in figure 2. The individual pixel processor consists of a low-noise amplifier-shaper followed by a comparator which provides the counting of individual photons with an energy above a programmable energy threshold. To accommodate the very high rates, above $5.10^8/cm^2/s$, each pixel processor has a 3 bit pre-scaler which divides the event rate by 8. Overflow from the divider which defines a pseudo fourth bit will generate a readout sequence where the pixel's address is readout. The pixel address, generated locally, will be used to increment a location in an histogramming memory. A Laue diagram will be generated from this data.
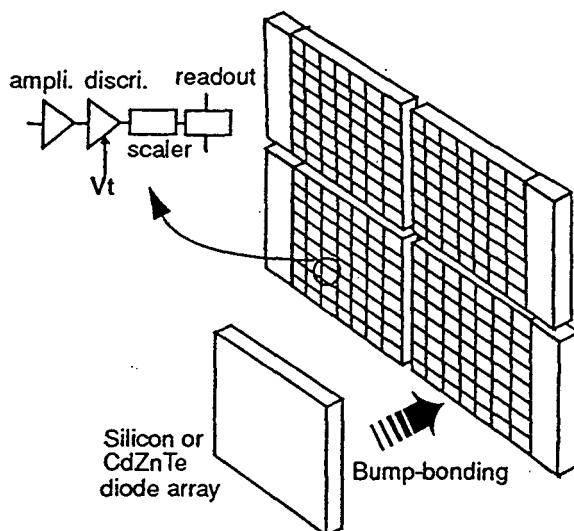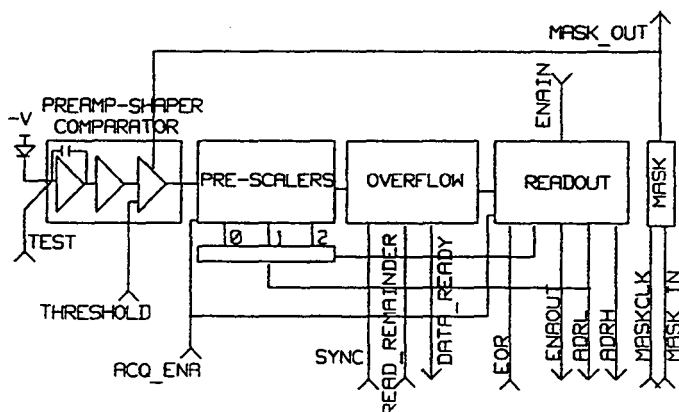

Figure 1: PCP module

Figure 2: Electronics architecture

3. RESULTS ON THE 8x8 FRONT-END PROTOTYPE

An 8x8 analog pixel prototype has been already integrated and tested[2]. This first prototype contains only the analog front-end (integrator and shaper) and is used to characterize different hybridization processes as well as the different detector material to be used (Si and CdZnTe).

The preamplifier is a cascoded low noise integrator with a DC reset. The shaper amplifier performs an RC-CR shaping. The feedback resistor is implemented with a MOS transistor biased in its linear region allowing the shaping time constant to be adjusted from 50ns to 150ns. Both the integrator and the shaper are described in reference 2. To accommodate the large counting rate (1MHz peak on one pixel) and to keep an infinite dynamic range(i.e. without saturating the front-end), the preamplifier is continuously reset with a time constant of less than 1μs to avoid any pile-up.

The 8x8 analog pixel array has been bump bonded to the diode array using a gold bump technique by AMKOR (Chandler, Az)[3]. Hybridization techniques will be discussed in paragraph 7. Table 1 summarizes the performances measured on the analog prototype. The noise contribution due to the fast reset of the integrator (parallel noise generated by the MOS feedback resistor) is small compared to the thermal noise.

An x-ray source (Fe[55]) has been used to characterize and calibrate the noise of the front-end and the hybridization. Figure 3 gives the measured energy spectrum. The energy resolution is 480 eV (FWHM). The Kβ peak at 6.5keV appears as hump to the right of the main peak. The plateau at the lower energies must be due to a 'dead layer' at the interface on the illuminated back side of the detector where part of the charge is not collected. Crosstalk between pixels was measured to be less than 0.5%.
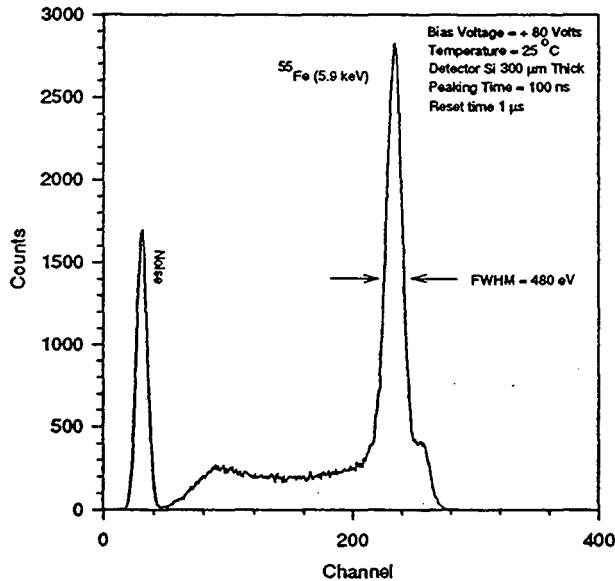

Fig.3: Energy spectrum of the Fe[55]

Gain	690 mV/fC (110mV/1000e-)
Shaping time constant (adjustable from 50ns to 150ns)	100ns
Energy resolution (FWHM) ENC (preamp reset < 1μs)	480 eV 60 e- rms
Noise count over threshold of 500e- for 1h30	20 counts
Crosstalk	< 0.5%
Power consumption (V_{supply}=3V)	50μW
Sustainable peak rate per pixel	>1 MHz

Table 1: Front-end performances (Si detector connected)

The noise count measured over a threshold of 400e- is about 20 counts (average) over a period of acquisition 1h30. This is an improvement of few order of magnitude compared to actual performance with CCD, figure 4. It will be possible to accurately record extremely weak and extremely strong reflection simultaneously of static crystallography and dynamic range of 10^7 and above appear feasible even with a slight loss of efficiency.
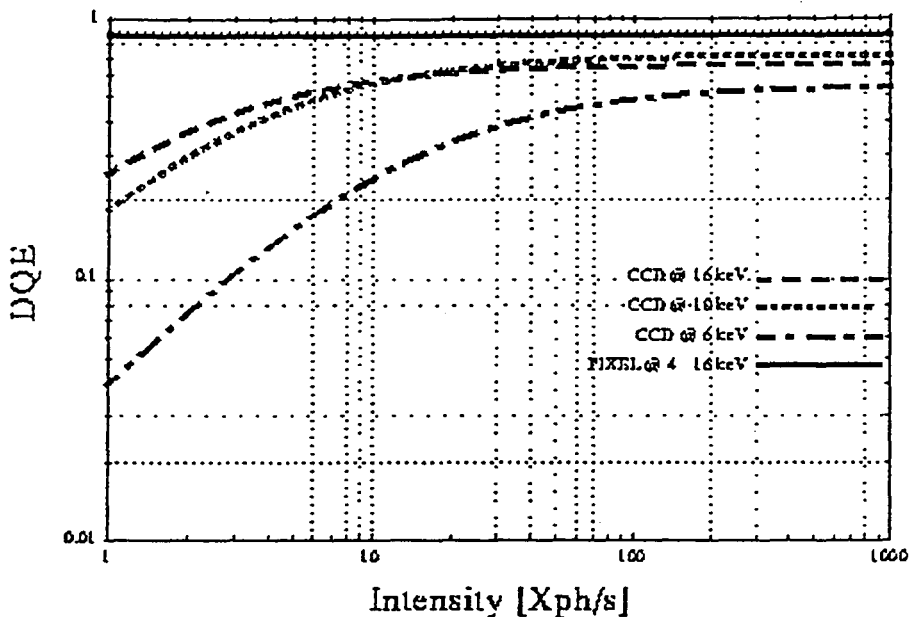

Figure 4: Detector Quatum Efficiency (DQE) as a function of intensity (10 second exposure)

4. DIFFERENTIAL COMPARATOR

The comparator is DC coupled to the preamp-shaper to achieve the energy discrimination. Previous measurements of the DC output voltage of the shaper on the 8x8 array have shown a process flow dependency (figure 5).

The measurements of the 8x8 arrays over 17 chips give a standard deviation of the shaper's output voltage between 3.5mV and 9mV with an average σ=7mV (from pixel to pixel on one chip). The expected value, as interpolated (to the corresponding gate oxide thickness) from reference 4, was around 5mV.
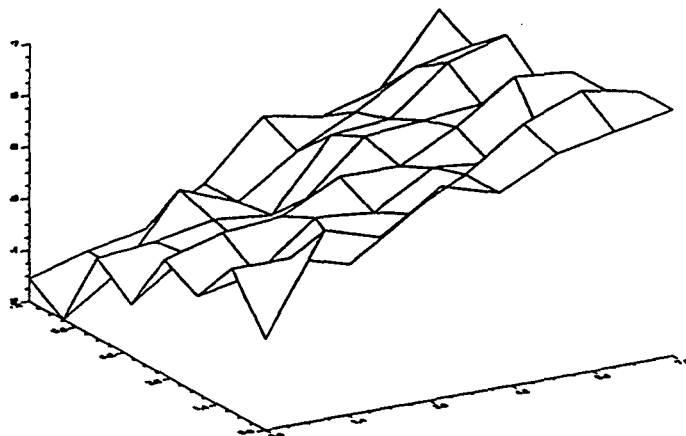

Fig.5: DC output voltage of the shaper (8x8 array)

A differential comparator has been implemented for its common mode rejection. The DC output level of the shaper is duplicated for each pixel by a 'dummy' shaper, figure 5, providing the DC voltage with a better matching due to reduced distance effects[4]. The threshold voltage is applied to the comparator as a differential voltage.
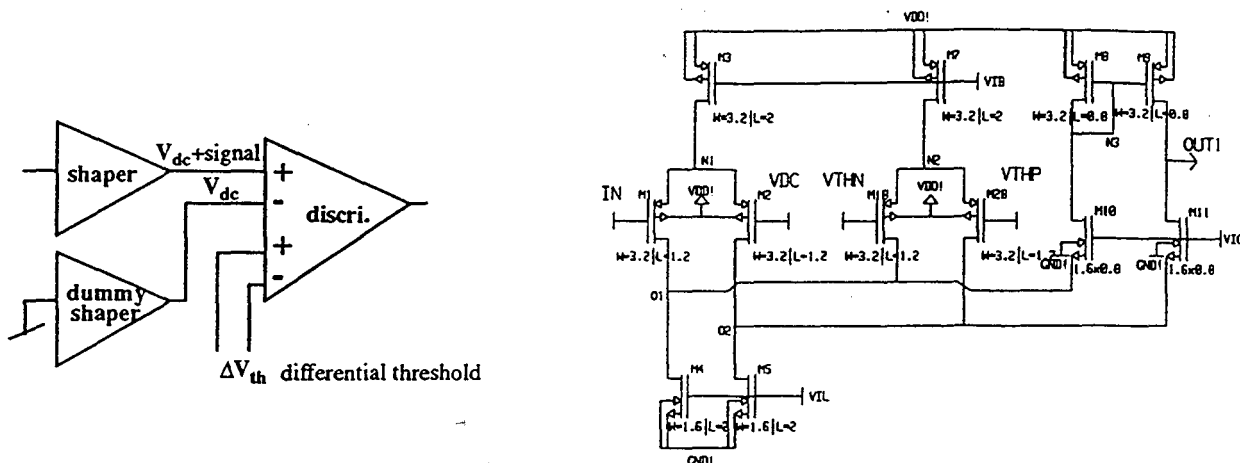
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Fig.6: Differential comparator

Figure 6 shows the schematic of the differential comparator. The offset is dominated by the threshold mismatch between transistors M1, M2, M1B and M2B and is temperature independent (the differential pairs being of the same conductivity type and having the same geometry). The effective threshold is defined by combining the differential threshold applied with the transient response of the comparator. Simulations have shown that the effective threshold equivalent charge is $Qth_{eff.} \approx Qth + 300e-$ (considering a amplifier-shaper with 50ns peaking time and a gain of about 100mV/1000e-).

5. LAYOUT

The technology used is the *HP 0.8μm CMOS* process available through *MOSIS*. This technology has three layers of metal available. The third layer has been only used in the layout as a ground plane to shield the electronics from the detector and to prevent any coupling from the digital circuitry to the inputs. Figure 7 shows the layout of 2 pixel cells sharing the same address generator. The input pad is 50x50 μm^2 and a input calibration logic has been added to select any desired pixel for calibration. There are no active circuitry under the pad to avoid damage due to the assembly. Power supplies for the analog front-end and the digital readout are independent.

An 8x8 front-end prototype has been also integrated in the HP 0.5μm technology for evaluation (mainly noise performances). This higher density technology could allow to scale down the pixel size from 150x150μm^2 to 100x100μm^2.
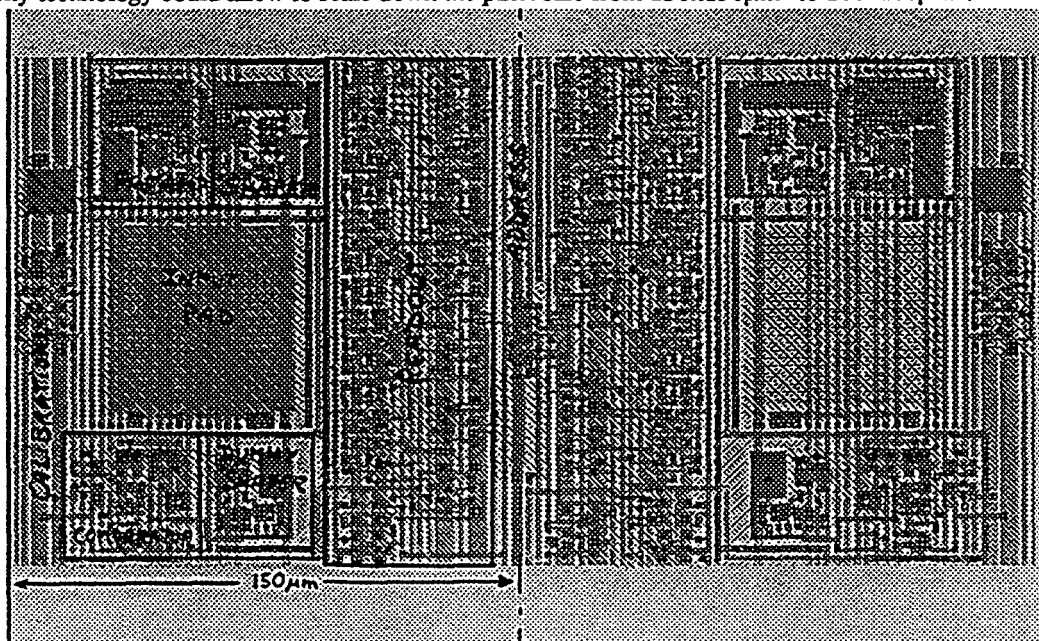

Fig.7: Layout of a dual pixel cell

6. PRELIMINARY RESULTS ON THE 16x16 ARRAY PROTOTYPE

The 16x16 pixel array prototype has been integrated and is presently under test. The pixel architecture as shown in figure 2 includes the preamplifier-shaper, the differential comparator followed by the pre-scaler (3 bits) and the readout logic. When a pixel has accumulated 8 counts, the overflow bit (the pseudo fourth bit) sends a signal to the end of the column via the DATA_READY line. Two adjacent pixels are readout in figure 8 (note that the DATA_READY signal is proportional to the number of pixel to be readout).

A synchronization signal SYNC is generated to prevent any overwriting of the overflows while the pre-scalers are counting and the readout sequence starts. The *ripple logic* sends the overflowing pixel's address, (ADRL, ADRH) to the end of the column where they will be formatted and forwarded to the data acquisition logic. These addresses are analog currents generated at the pixel level to reduce the switching across the column compared to digital addresses. The *end of read signal* (EOR) resets the pixel and the next pixel is read out.
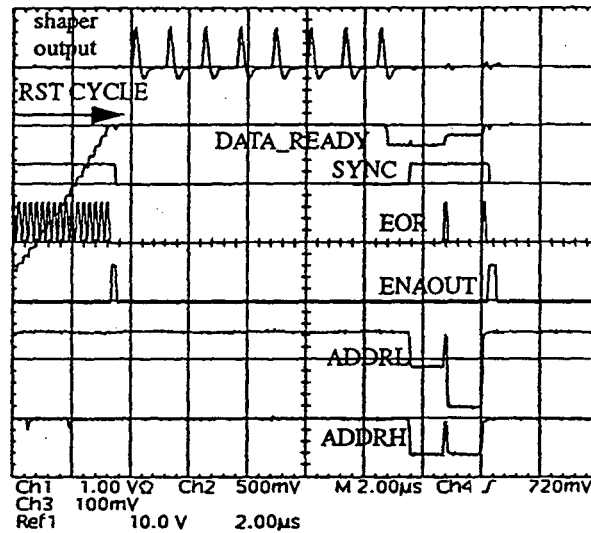

Fig.8: Column readout (acquisition mode)

When a pixel address readout has been completed, the *end-of-column logic* sends an *end-of-read* signal (EOR) and processes another overflowing pixel, if any. The delay induced by the ripple logic is about 600ps/gate The maximum delay for the ripple logic to scan the 100 pixel, which will be contained in a dual column, will be about 60ns.

The readout sequence ends when the *end-of-column* receives the ENAOUT of the *ripple logic*. When the acquisition has stopped a *read remainder* cycle allows to get the contents of the 3 bit pre-scalers. Figure 9 shows the different content of the pre-scaler generated as analog currents corresponding to the 3 bits value.

The minimum threshold above noise which can be set seems to be around 1000e- (assuming a good linearity of the comparator within a gain of about 100mV/1000e-). The minimum threshold above noise is still higher than expected (>300e- corresponding to 3 noise sigma). The minimum signal which can be detected without false count is about 2000e- due to coupling between the comparators and the front-end seen during the readout cycle on the shaper's output in figure 8. The next prototype will have some improvements, in particular coupling and clock-feedthrough issues will be addressed. Minimum threshold should be reduced down to 500e-.

During *synchronization* of the overflows (SYNC) and the *end of read* (EOR) where only pixels with informations will see any logic switching (gate or inverter switched) in order to reduce digital peak currents. The end of column logic will be also implemented, generating the SYNC and EOR signals. The analog addresses and the remainder bits will be digitally encoded to be readout serially. The digital address will be sent to a histogramming memory to generate the computerized Laue diagram. The histogramming memory DSP (HSP48410 histogrammer/accumulating buffer) is configured to operate in the asynchronous mode where each address points to a 24 bit register (counter) yielding to a 10 bit x 24 bit memory unit. The 10 bit pixel address from the column encoder is sampled and the associated pixel's 24 bit register is incremented.
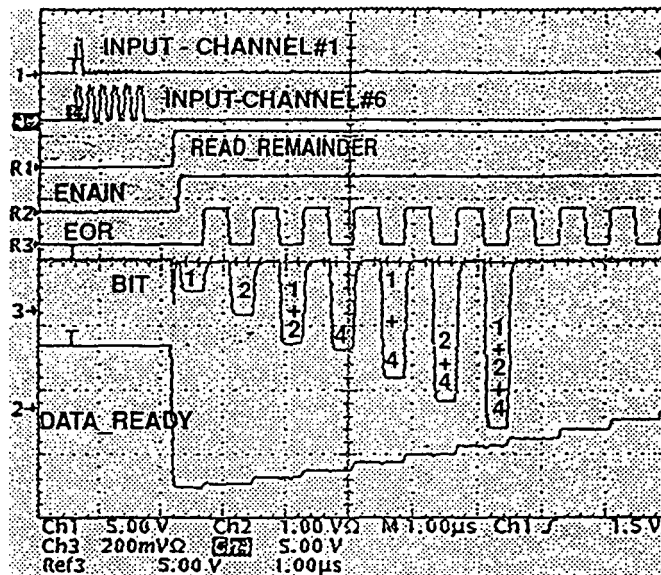
fig.9: Column readout (read-remainder mode)

7. HYBRIDIZATION TECHNOLOGY

Chip hybridization technology as well as wafer level technologies have been investigated for prototypes and production,[5]. At the chip level gold bumps and conductive thermoplastic are affordable and proven for bumps no less than 50μm in diameter. They are also effective at the wafer/module level hence offer an effective transition from a prototype to a module. Assemblies have been made by *AMKOR* using gold bump, [3]. This process is limited in term of number of bump per chip due to the large pressure required (30 gr/bump).

An other hybridization technique is under investigation at *ETEC* (Peabody, MA) using conductive thermoplastic. This process has the advantage of being low temperature, low pressure and thus less likely to damage the ASIC or the detector particularly in the case of CdZnTe where surface damage can lead to a substantial increase of surface current.

Combining the 2 processes, gold bump on the ASIC and thermoplastic on the detector side would reduce considerably the pressure needed for large number of bump and would also reduce the complexity of the thermoplastic process.

Wafer level processes (solder bumps, indium bumps) cannot be easily or cheaply adapted to the chip level bumping but are very effective for mass production quantities. However solder cannot be used with CdZnTe due to the high temperature required.

8. DATA ACQUISITION SYSTEM

The basic specifications of the architecture and the technology have been defined in collaboration with the U.C.-San Diego group. The information generated by the detector assemblies consists of the pixel address within the detector system. Columns of 100 pixels operate independantly and in parallel in order to accomodate the very high incident hit rate. Time occupancy for a pixel address at the level of the column is of the order of 80ns.The storage of information will be implemented through the usage of histogramming memory modules. These modules will be built around standard, fast, off-the-shelf, commercial memory chips[6]. The chip's controllers will be optimized for speed.

9. CONCLUSIONS

A 16x16 pixel array prototype has been designed for protein crystallography. Time resolved Laue crystallography will be performed in a frameless operation mode without dead time (concurrent readout and acquisitions) for counting rate above 5×10^8/cm^2/s (100kHz average/pixel). The functionality of the column architecture has been demonstrated and preliminary results are very encouraging. The minimum threshold can be set around 1000e- to detect minimum signal above 2000e- (improvement in the next prototype should reduce the minimun threshold around 500e-. Systematic tests have now to be performed, especially threshold uniformity and effects of readout cycles on the threshold.

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This detector will also considerably accelerate data collection in static Laue or monochromatic crystallography and make better use of the intense beam delivered by synchrotron light source.

Pixel arrays detectors can be used for a broad range of further applications, most notably for medical imaging and non-destructive testing. This approach to pixels is particularly suited to applications where either dynamic processes, or very high event counting rates must be accomodated. Also the sorting of individual photons according to their energy provides information not available by energy-integrating devices (i.e. dual energy mammography for clutter removal). Material science is a potential for extensive use of these detectors for x-ray diffraction applications. Satellite mapping of the sky for X-ray sources is another typical scientific application.

ACKNOWLEDGMENTS

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