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Electrical Characterization of Individual Colloidal Semiconductor Nanocrystals

By

Matthew Thomas Sheldon

A dissertation submitted in partial satisfaction of the
requirements for the degree of

Doctor of Philosophy

in

Chemistry

in the

Graduate Division

of the

University of California, Berkeley

Committee in charge:

Professor A. Paul Alivisatos, Chair

Professor Stephen R. Leone

Professor Alex K. Zettl

Spring 2010

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Semiconductor Nanocrystals**

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By Matthew Thomas Sheldon

Abstract

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Professor A. Paul Alivisatos, Chair

Strategies for the device integration and electrical characterization of individual colloidal semiconductor nanocrystals are presented. Results emphasize the insight gained by studying the electronic structure of individual nanocrystals as opposed to measurements of ensembles of particles. An analysis of a variety of device geometries, material systems, and nanocrystal morphology and functionality shows that the method of electrical contact has a dominating role in the electrical behavior of the samples. Further, interactions with the electrode contact reflect the unique electronic and surface structure of the individual nanocrystals.

In studies utilizing nanoscale lithography to directly deposit metal electrodes onto nanocrystals under vacuum, samples behave as single electron transistors (SET). Devices made from CdTe nanorods contacted by Pd display strong electron-electron correlations, which limit the flow of current to one electron at a time across the nanocrystal. Measurements also indicate that chemical reactions induced by the electrode metal cause diffusion of interface species and compositional modification of the nanoparticle. Interface chemical reactions may completely transform the nanocrystal under study, also altering the nanocrystal electronic structure.

To avoid these complications, alternative strategies for device fabrication take advantage of the self-assembly of heterostructure nanoparticles. Synthetic methods for the direct solution-phase growth of Au electrodes on CdSe nanorod tips provide a 100,000-fold increase in the conductivity of single particles. Device response indicates ensemble electron physics and a Schottky barrier at the electrode contact, allowing quantitative determination of interface electronic structure.

The methods of self-assembly are extended to a variety of heterostructure nanoparticles optimized for electronic and optoelectronic functionality. This work demonstrates the increasing sophistication of high-quality electrical devices achievable via self-assembly and verifies the process as an excellent route to the next generation of electronic and optoelectronic devices utilizing colloidal semiconductor nanocrystals.

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Chapter 1.

INTRODUCTION

The past decades have seen continual growth in a field of inquiry commonly referred to as nanoscience, defined by the convergence of several disciplines studying structures ranging in size from a few to several hundred nanometers. The ongoing miniaturization of integrated circuits fabricated by the semiconductor industry has finally approached “the bottom”,¹ where small clusters and few monolayers of atoms define transistors, and further gains in computation speed and power are anticipated to require precise control of single electrons, spins, and photons.² Fundamental and applied research in biology and medicine, embodied by proteomics, genomics, and genetic engineering, seek to relate basic molecular units of organic molecules to the complex functional structures of organisms. Similarly, researchers in materials science, chemistry and physics attempt to better bridge understanding of the domains of quantum mechanics, single atoms, and molecules with macroscopic systems optimized to help solve some of the largest challenges that face society, such as energy production on a global scale. Across disciplines, such research requires understanding of the unique behavior that characterizes the nanoscale, since the forces and dynamics in this size regime define the organization of matter and thereby the flow of energy and information through it.

Semiconductor nanocrystals are an important class of nanoscale material for probing this intermediate size regime, between molecules and macroscopic matter. Often called “quantum dots” or “artificial atoms”, these materials are nanometer sized crystalline semiconductor particles comprised of ~100 to ~100,000 atoms. Owing to refinement in methods of self-assembly, semiconductor nanocrystals are produced in mole quantities per batch and exhibit well-defined size, morphology and composition, which are controlled by synthetic strategies during and after their growth. Furthermore, nanocrystal electronic structure is defined uniquely by the interplay of these controllable parameters, providing an excellent platform to systematically vary nanoscale properties.^{3,4} These attributes have led to a range of applications for semiconductor nanoparticles including medical diagnostics, catalysis, information processing, and energy storage and conversion.⁵⁻¹¹

This work details the electrical characterization of semiconductor nanocrystals, and the rich insight gained by studying the electrical response of individual nanocrystals integrated into devices, one at a time. Consistent with trends in nanoscience, this research employs a multidisciplinary approach. Nanoparticles are synthesized using colloidal, air-free methods from inorganic chemistry. Nanoparticle structure and morphology is characterized with a variety of spectroscopy and microscopy techniques common to chemistry and materials science. Individual particles are integrated into test chips via nanofabrication strategies recently pioneered by the semiconductor device industry and by new methods of self-assembly. Accurate descriptions of electron transport through nanocrystals require both old and new concepts from solid state physics and single-

electronics. Finally, analysis necessitates special attention to the unique properties of nanocrystal surfaces and interfaces, as electrical studies of nanoscale objects can be dominated by the influence of the measurement technique. That is, the transport behavior depends crucially on the contact method. Single nanoparticle electrical measurements are thus an excellent system for optimizing the next generation of electronic and optoelectronic devices, and for understanding the fundamental consequences of nanoscale solid-state chemistry and physics.

1.1 Electronic Structure of Semiconductor Nanocrystals

Several factors give rise to the unique electronic structure of semiconductor nanocrystals. Because their physical dimensions place nanocrystals between molecules and macroscopic, bulk semiconductors, it is useful to discuss these contributions to electronic structure with concepts from molecular orbital theory and solid-state physics. We begin this treatment with an overview of bulk semiconductor electronic structure, and extend these models to describe nanocrystal behavior.

According to the tight binding approximation, the electronic structure of bulk matter arises from the superposition of wave functions describing isolated atoms located at each lattice site in the underlying crystal structure of the material.^{3, 12} The tight binding approximation is closely related to the linear combination of atomic orbitals method (LCAO) used to describe the electronic structure of molecules, with the semiconductor imagined as an infinitely large molecule. Analogous to the bonding and anti-bonding molecular orbitals generated from the linear combination of two individual atomic orbitals, in the limit of infinite lattice atoms, discrete atomic orbitals combine to form energy bands of infinitesimally spaced molecular orbitals delocalized across the entire lattice. These bands exhibit the electronic character of the respective bonding and anti-bonding states. The tight binding approximation accurately predicts the lack of states between the bands of HOMO and LUMO character, which by the convention of solid state physics, is usually called the band gap, located in energy between the valence and conduction bands respectively. Selection rules for optical excitations across this gap and a range of semiconductor material properties, such as the band width, carrier density, effective mass, and phonon coupling therefore reflect the structure and symmetry of the semiconductor's underlying unit cell.¹²

At a temperature of 0 K, a perfect semiconductor crystal lattice will display intrinsic carrier distributions, meaning that the valence band is completely filled with electrons while the conduction band is completely empty. In this situation, the chemical potential of the material, also commonly called the Fermi level, resides at the center of the band gap. Intrinsic defects due to local variations in geometry and stoichiometry or extrinsic defects due to impurity atoms with a distinct electronic valence, as well as thermal activation, can alter the electron distribution around the band gap. Consequently, in most semiconductors the majority of available charge carriers, and hence the Fermi level, resides near the conduction band edge if the material is n-type or near the valence band edge if it is p-type. The operation of most semiconductor devices relies on the specific energy location of the Fermi level and the magnitude of the band gap.

Optical excitation of sufficient energy also promotes electrons across the band gap, placing a negative charge carrier, an electron, into the conduction band and effectively creating a positive charge carrier, a hole, in the valence band from which the electron was removed. Coulombic attraction between these photo-generated carriers of opposite charge can create a bound state, called an exciton, conceptually similar to the ground state of the hydrogen atom. Materials parameters, such as the dielectric constant of the semiconductor and effective masses of the carriers in the conduction and valence band, define the binding energy and Bohr radius of this excited electron-hole pair. The Bohr radius serves as a rough estimate of the 'size' or spatial extent of carrier excitations in the semiconductor. After excitation, the carriers can recombine non-radiatively via phonon coupling, or emit radiation characteristic of the excitonic state. In photodetection or photovoltage (PV) applications of semiconductors, the goal is to separate excited charge carriers into an external circuit before recombination.

When considering nanocrystal electronic structure, the assumption of infinite lattice sites applied by the tight binding approximation no longer holds. Rather, the continuous bands of electronic states observed in extended solids become more discrete in nanocrystals, as fewer atomic orbitals contribute to the overall wavefunction. The effect is most pronounced at band edges, such that relatively few, atomic-like states define the electronic structure and dynamics near the band gap.³ Since most semiconductor devices depend on the behavior of electrons near the band gap, this has profound consequences for applications of nanocrystals. For example, the concentration of oscillator strength to these few transitions near the band edge entails that nanocrystals often have high quantum yield and strong fluorescence,^{13, 14} useful in biological labeling experiments and display technologies that would otherwise require organic dyes.⁵

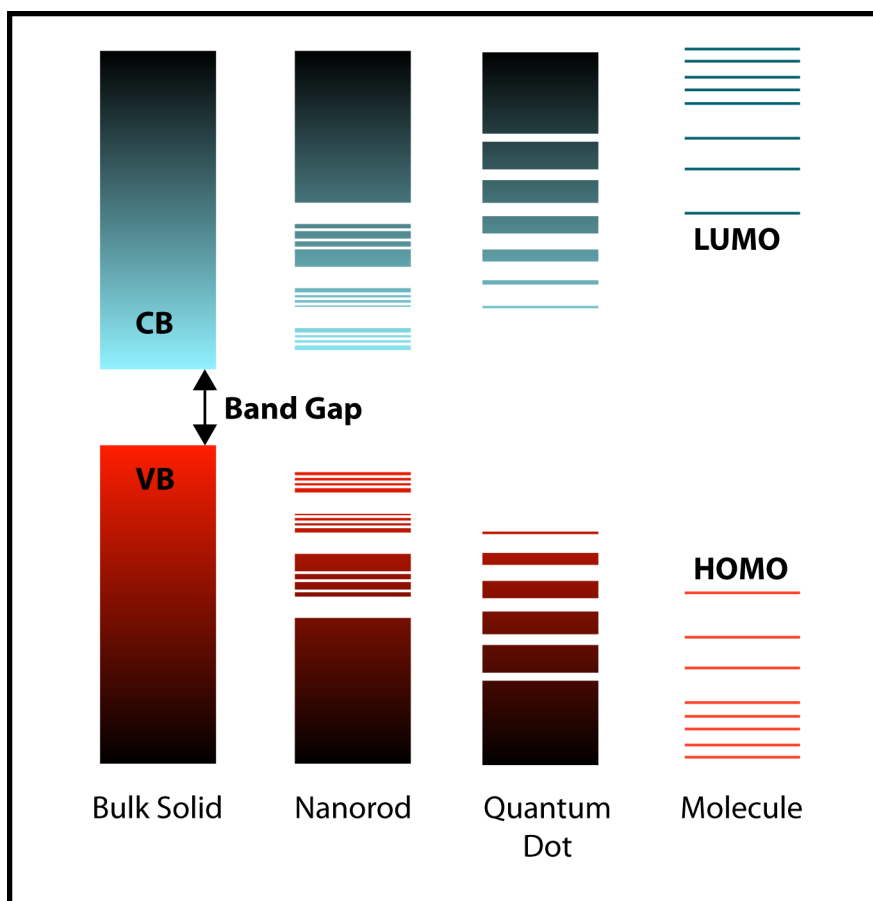


Figure 1.1 Schematic energy diagrams of nanorods and spherical “quantum dot” nanocrystals compared with bulk solids and molecules. The valence band (VB) and conduction band (CB) in the bulk semiconductor correspond with the HOMO and LUMO states of a molecular species. The splitting of band edge states in the nanorod reflects the contribution from distinct radial and longitudinal carrier confinement.

The separation between all states, and thus the band gap, also increases in magnitude as the physical dimension of the nanoparticle encroaches on the exciton Bohr radius. An analogy to the particle-in-a-box model (also called the infinite square well) from quantum mechanics helps rationalize this behavior. When the spatial dimension of the confining potential decreases, the Schrödinger Equation predicts the energy of the quantized states, defining the probability distribution of the confined particle in 1-D, to scale as $1/r^2$, where r is the box length. Essentially, the quadratic dispersion relation of a free particle is quantized in the box to discrete energy states that correspond to a wave function which is resonant with the length of the potential well. If we imagine the nanoparticle as the potential well which confines charge carriers, we anticipate the same dependence of the discrete electronic states on nanoparticle diameter. However, the position-momentum uncertainty relation predicts this effect is only pronounced for sufficiently small geometries, which entail a superposition of many momentum states to describe a well-defined position for the charge carrier. In a semiconductor nanocrystal this is the case, precisely because the charge carrier position is well defined by the nanoparticle size and the exciton Bohr radius. More sophisticated treatments corroborate

this basic picture, adjusting for the specific dispersion relation of electrons in the solid predicted by the tight binding approximation. This adjustment is especially necessary for correct modeling of crystallites much smaller than the exciton Bohr radius.³ Taken together, the above phenomena are described as “quantum size effects”, the consequence of “quantum confinement” in semiconductor nanoparticles.

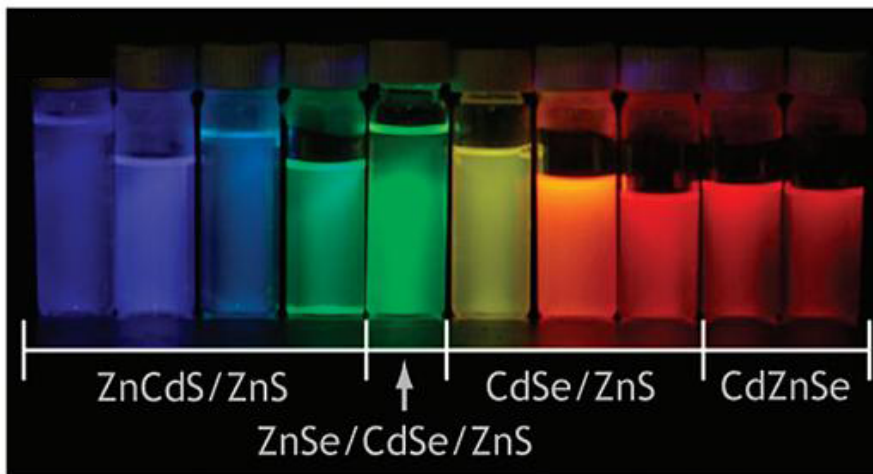


Figure 1.2 Color series of nanoparticle solutions spanning the entire visible spectrum. These particles are used for quantum dot based LED displays. *This image is licensed under the Creative Commons Attribution-ShareAlike 3.0 License.*

The ability to tune the energy of these discrete, atomic-like states near the band edge, ultimately via synthetic strategies as described below, is one reason why the particles have earned the nickname, “artificial atoms”. A demonstration is depicted in Figure 1.2, which shows fluorescence from recombination across the nanocrystal band gap spanning the entire visible spectrum, due to synthetic control of the size and composition of the nanoparticle. Anisotropic nanocrystals, such as nanorods, will exhibit distinct confinement effects for each limiting dimension, the rod diameter versus the rod length for example (see Figure 1.1), allowing even more control of the nanocrystal electronic fine structure.¹⁵ During single nanoparticle electrical studies, we often hope to probe the electronic structure resulting from this quantum confinement directly, via electron injection.

1.2 Semiconductor Nanocrystal Surface Structure

Another contribution to nanoparticle electronic behavior, distinct from quantum size effects, results from nanoparticle surface structure. This consideration is especially important for nanoparticle based electronic devices, because the nanoparticle surface defines the interface to charge injection. Moreover, the equilibration of electrons in an electrically contacted nanocrystal with those in the electrode metal depends crucially on the metal-semiconductor interface density of states. The equilibration process determines if a contact is ohmic, rectifying, or a tunneling barrier.¹⁶ Therefore the surface electronic structure has a profound effect on overall device performance.

The disruption of lattice periodicity at a semiconductor surface introduces localized electronic states, distinguished from the bulk band structure by the particular surface stoichiometry, symmetry, and dangling bonds introduced along a cleaved facet. The energy location of these surface states may be in the band gap, called “mid-gap states”, and lower in energy than the bulk Fermi level in the case of “surface traps”. This alters not only the equilibrium electron configuration at the surface, but may also induce structural rearrangement of surface species or surface amorphization, both examples of surface reconstructions.¹⁷ Further, the cleaved surface may exhibit heightened reactivity, if exposed to oxygen, for example.

Semiconductor nanocrystals also commonly exhibit well-defined crystalline facets. Because surface atoms comprise a significant fraction of the total atoms per nanocrystal, the increase in surface-to-volume ratio with decreasing size leads to an increased role of surface states in the overall electronic distribution. This imparts a strong size dependence on electronic equilibration and thermodynamic phase stability.^{18, 19} The effect is manifest in well-characterized melting temperature depression for smaller nanoparticles, observed for example in CdSe nanocrystals, due to the increased number of unsaturated surface bonds.²⁰ However, pressure-induced phase transitions of CdSe nanoparticles show the opposite trend, requiring higher pressures for phase transitions than bulk CdSe because of the larger energy barrier to structural reorganization at the surface.^{19, 21, 22} This highlights that while the surface of the nanocrystal plays an important role in the overall behavior of the nanostructure, many factors must be considered to understand the specific consequences.

Nanocrystals may also exhibit unique surface reconstructions compared to bulk semiconductors, because of the organic or inorganic species used to control the growth of the nanoparticle, stabilize the particles as colloids in solution, and passivate unsaturated surface atoms.^{23, 24} The ideal passivation treatment will bond surface atoms of the semiconductor epitaxially to a material with a much larger band gap and minimize lattice strain or changes in bond order, so to eliminate any states in the band gap of the nanocrystal. In practice, this is a challenging goal that must be optimized for the surface chemistry of a particular semiconductor material. Furthermore, it may be undesirable to introduce such a passivating species, often an insulator, in the metal-semiconductor interface at the nanocrystal electrode contact.

The optimal nanocrystal surface passivation is the subject of very active research in semiconductor nanocrystal based electronics. Recent strides understanding the fundamental chemistry that governs exchange of surface species^{4, 25} has led to ensemble nanocrystal devices with all inorganic interfaces displaying greatly enhanced conductivity and carrier mobility.²⁶ Increasing evidence suggests that the surface structure may also control the Fermi level and carrier concentration of the nanocrystal. For example, lead chalcogenide nanocrystals switch from p-type to n-type carrier distributions when an electronegative or electropositive organic ligand, respectively, binds to the nanocrystal surface.^{27, 28}

In chapter 3 of this study, we show how the nanocrystal surface reactivity at an evaporated metal contact leads to interface chemical species that dominate electron transport across the single nanocrystal device. In chapter 4 and 5 we demonstrate an alternative method to contact individual nanorods directly via solution phase growth of metal tips, which displace surface ligands at the contact electrode. This strategy produces

superior electronic performance, allowing quantitative analysis of the electronic structure at the metal-semiconductor nanoparticle interface and provides a basis for further study of the electrical characteristics of a variety of nanostructures.

1.3 Synthesis of Colloidal Semiconductor Nanocrystals

Extensive studies over the last 30 years have resulted in refinements of wet chemical techniques for synthesis of semiconductor nanoparticles with well-defined size, morphology, and composition.²⁸⁻³⁶ The standard method employed in this study induces thermal decomposition of organometallic precursors into monomers in a bath of surfactant species that reversibly coordinate to the nanoparticle surface during crystallization, usually under air-free conditions. These coordinating species are generally organic surfactants with long hydrophobic chains and a polar head group that interact strongly with the ionic lattice of the semiconductor. Common surfactant classes, also called surface ligands, include alkylphosphonic acids, alkylamines, alkylcarboxylic acids, alkylthiols, etc.

Surfactants serve three important roles in nanocrystal synthesis. First, they have strong influence over growth kinetics and particle morphology, by selectively binding to specific crystal facets and adjusting the rate of monomer addition along that dimension.²⁹⁻³¹ Second, the surfactants stabilize the nanoparticles as colloids in solution, allowing for solution-phase processing of large quantities of the nanocrystals without aggregation. Finally, these surfactants serve as the native passivating agents on the nanocrystal. Section 1.2 considers how these passivating surface species also adjust the nanocrystal electronic behavior.

By careful control of the reaction conditions and chemical species, many syntheses produce monodisperse samples of nanocrystals with spherical, rod, disk, cube, sheet, plate, or tetrapod shapes.²⁹ Often these shapes reflect the crystallinity of the thermodynamic phase stabilized during growth. For example, CdSe will nucleate in a tetrahedral zinc-blende phase to adopt tetrahedron nanoparticle morphology. If the hexagonal wurzite phase of CdSe is stabilized instead during growth, the nanoparticles will adopt elongated hexagonal nanorod morphology.^{32, 33} This shape is most easily incorporated into single nanocrystal electrical devices, and the length and diameter can be tuned separately. By sequentially promoting each crystal phase during the nanoparticle synthesis, CdSe tetrapods form, exhibiting four wurzite arms extending from each face of a zinc-blende core.^{29, 34}

In chapters 4 and 6 we discuss further modifications to nanoparticle structure and morphology that can be achieved after synthesis is complete. Selective cation exchange will produce local regions or fully converted particles of a distinct chemical species, while maintaining the overall as-synthesized nanoparticle morphology.^{35, 36} It is also possible to selectively deposit metal only on the tips of nanorod particles.³⁷ Both strategies are important for optimizing nanocrystals as functional materials in electronic and optoelectronic devices.

1.4 Advantages of Single Nanoparticle Studies

Historically, characterization of semiconductor nanocrystal electronic behavior necessitated studies on large ensembles of nanocrystals, in the form of nanocrystal thin film solids, integrated into two-terminal and three-terminal field effect transistor (FET) device geometries.³⁸⁻⁴¹ In part, this was due to the ease with which nanocrystals are drop-cast or spin-cast from solution into well packed thin films between macroscopic electrodes. Robust nanoscale contacts to individual nanocrystals require state-of-the-art nanofabrication, for ~ 20 nm lithography resolution, and refinements in nanoparticle synthesis. Samples of anisotropic nanorods are needed that maintain quantum confinement along the particle diameter while still being addressable by e-beam lithography, unlike previously available spherical particles. In chapter 2 we discuss device fabrication strategies.

Initially, proposed applications of ensemble nanoparticle solids focused on the advantage that stemmed from the easier synthesis and solution processability of the materials, compared to large-scale vacuum deposition of thin film crystalline semiconductors. For example, nanocrystal solids could cheaply replace the active layer in thin film photovoltaics,¹¹ while the electronic behavior of the material could also be optimized via quantum confinement, to best match absorption with the solar spectrum. In practice, nanoparticle solids are highly defective electronic materials, exhibiting conductivity and carrier mobility that has yet to compete with conventional thin film devices.^{41, 42} Many factors contribute to the poor electronic response, usually characterized by large hysteresis and low conductivity.⁴⁰ Local variations in particle size may introduce nonuniform carrier potentials. Interfaces between nanoparticles, ligand shells and surface structure,^{27, 43, 44} and packing order all affect transport of electrons across the device.^{42, 43} Much ongoing research addresses the transport challenges in these highly disordered systems.⁴

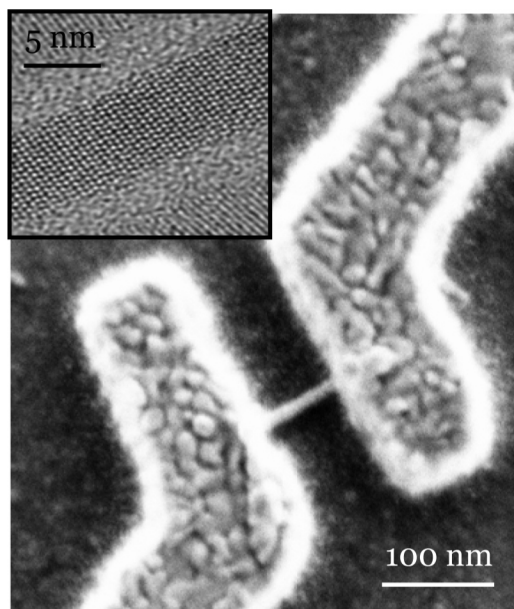


Figure 1.3 SEM of a single CdTe nanorod device contacted by Pd electrodes, with TEM of single nanorod (inset). After electrical measurement, devices can be characterized with high-resolution microscopy and spectroscopy.

A distinct advantage of single particle studies is the conceptual simplicity of the experiment, which allows decoupling of single particle versus ensemble and inter-particle electronic effects. Further, Figure 1.3 demonstrates that high-resolution microscopy and spectroscopy can characterize the morphology, and crystal structure, including defects or impurities, of a single nanocrystal in a working device. Indeed, these characterization techniques are essential aspects of the work presented in later chapters and difficult to apply to ensembles of nanocrystals.

A recent shift in strategies for utilizing nanoparticles in functional devices attempts to circumvent the complexities associated with nanoparticle thin film solids. Increasingly, researchers endeavor to build complex functionality into single nanoparticle heterostructures and then integrate these nanoparticles in an organized way into larger geometries. The hierarchical structure of proteins and membranes required for photosynthesis may be an appropriate guiding principle if artificial photosynthesis is the goal. To this end, recent work demonstrated success in the design of single nanoparticle p-n junctions³⁶ for carrier separation, and single nanoparticle photocatalysts.⁴⁵ For these new classes of advanced materials, single particle measurements are essential to optimize nanoparticle performance and answer fundamental questions about the interaction of light and matter at the nanoscale. Single particle electrical characterization of more complex nanoparticle heterostructures is the subject of the second half of this dissertation.

1.5 Dissertation Outline

Following the introduction in Chapter 1 to the basic concepts relevant to nanocrystal electrical characterization, a central organizing premise of this dissertation is

the difference between “top-down” and “bottom-up” strategies for single nanocrystal device integration and the consequent effect on nanocrystal electronic behavior.

Generally, “top-down” refers to fabrication methods like those employed by the semiconductor device industry in cleanrooms, to lithographically define nanoscale electrodes that are deposited under vacuum directly onto individual nanocrystals. Chapter 2 details the specific “top-down” approach developed for these studies. Chapter 2 also introduces the physics of single electron transistors (SET), as strong electron-electron correlations limit charge injections to a single electron at a time into nanocrystals contacted by this method.

Chapter 3 expands on work previously published in a peer-reviewed journal demonstrating the limitations of the “top-down” approach. Characteristic coupling behavior of single electrons in the single CdTe nanorod devices suggested chemical reactions induced by the Pd electrode metal. High-resolution spectroscopy and microscopy confirmed the presence of an alloyed, chemically distinct region that diffused approximately 25 nm from the nanocrystal-electrode interface. This chemical reactivity is common at all metal-semiconductor interfaces formed by the vacuum deposition of evaporated metals, and the spatial extent of the reaction front reflects the heat of formation of chemical species available at the interface.⁴⁶ The same behavior in the confined geometry of a nanocrystal device may chemically transform the entire nanoparticle under study, which is generally undesirable. This behavior severely restricts the choice of electrode metals to those that may not react with the sample, if the electronic structure of the as-prepared nanoparticle is required. This limitation is not amenable to every application. Further, the interface reactivity is likely complicated by the unique surface chemistry of nanocrystals.

To better optimize nanocrystal-based electronic devices and avoid these constraints, Chapter 4 and 5 present alternative strategies for device fabrication using “bottom-up” methods that take advantage of the ability to self-assemble nanoscale materials. Just as the nanorods are prepared in batches via chemical synthesis, it is also possible deposit metal spheres directly on the nanorod tips in solution and preserve a high quality, abrupt nanocrystal-metal interface. These tips serve as the contact electrode to the nanoparticle. Individual nanoparticle heterostructures will then spontaneously adsorb across predefined nanoscale junctions from solution if drying conditions are appropriate, for integration into macroscopic devices.

Chapter 4 reports work previously published in a peer-reviewed journal describing many advantages of the “bottom-up” approach. CdSe nanorods with solution-deposited Au tips show 100,000-fold increase in conductivity, and electrical current is no longer limited by electron-electron correlations like in the earlier SET devices. Instead ensemble electron dynamics across Schottky barriers are observed, more analogous to conventional macroscopic semiconductor devices. Chapter 4 also emphasizes modeling of interface structure and transport properties from temperatures ranging from 4K- 475K to quantitatively describe interface electronic band structure. The large conductivity enhancement results from a 75% lower interface contact barrier compared with non-tipped samples.

Chapter 5 describes work extending the method and analysis, in Chapter 4, to a variety of complex nanocrystal heterostructures, outlining trends in single nanocrystal electronic behavior. Syntheses and electrical characterization of single nanocrystal p-n

junctions are explored as well as other nanocrystal heterostructures optimized for PV, followed finally by a comment on promising future directions in single particle electrical characterization.

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Chapter 2. “Top-Down” Devices

Experimental and Theoretical Approach

2.1 Synthesis of Cadmium Telluride Nanorods

The high-temperature synthesis of colloidal cadmium telluride (CdTe) nanorods characterized in these studies was performed under air-free conditions with standard Schlenk-line techniques following the procedure in reference 1.¹ Cadmium oxide (CdO) (99.99+%), tellurium (Te) (99.8%, 200 mesh), and tri-n-octylphosphine oxide (C₂₄H₅₁OP or TOPO, 99%), methyl-phosphonic acid (MPA, 99%) and propyl-phosphonic acid (PPA, 99%) were purchased from Aldrich. n-Octadecylphosphonic acid (C₁₈H₃₉O₃P or ODP, 99 %) was purchased from Polycarbon Industries. Trioctylphosphine (TOP) (90%) was purchased from Fluka. All solvents used were anhydrous, purchased from Aldrich, and used without further purification. The Te precursor solution was prepared by dissolving tellurium powder in TOP (concentration of Te 10 wt%). The mixture was stirred overnight at 100 °C, until all Te was dissolved.

A typical synthesis of CdTe rods is described below. This reaction also produces a large fraction of particles with tetrapod morphology that can be separated during later purification steps. First, a mixture of ODP, TOPO, MPA, PPA and CdO is combined in a 50 mL three-necked flask connected to a Liebig condenser and degassed under vacuum at 120 °C for approximately one hour after bubbling stops. Milligram quantities of MPA and PPA help promote high aspect ratio in the nanorods. The surfactant and cadmium precursor mixture was heated slowly under argon until the CdO decomposed and the solution turned clear and colorless around 300 °C. Next, 1.5 g of TOP was added and the temperature was further raised to 320 °C for 1 hour. The mixture was then cooled to 120 °C and degassed for another hour, before being heated again to 320 °C. Next, the Te:TOP precursor solution was injected quickly. The temperature drop, usually to 315 °C, was maintained at this value throughout the synthesis. Synthesis is stopped after 5-10 minutes by removing the heating mantle and by rapidly cooling the flask.

After cooling the solution below 70 °C, 3–4 ml anhydrous toluene was added to the flask, and the product was transferred to an argon glovebox. The minimum amount of anhydrous methanol, which was required to cause the precipitation of the nanocrystals after centrifugation, was added to the reaction product. Careful control of methanol concentration and centrifugation speed can also separate tetrapods from nanorods during this step. After centrifugation and removal of the supernatant, the precipitate was re-dissolved twice in toluene, re-precipitated with methanol and stored in the glovebox. The resulting nanoparticles are soluble in common organic solvents, such as toluene and chloroform. The particles are generally stable for years in solution in the glovebox. The aspect ratio of the nanorods is controlled by the Cd/Te and Cd/ODP molar ratio as well as the concentration of MPA and PPA according to the strategy outlined.¹ The synthesis in this study was optimized to provide CdTe nanorods with approximately 7 nm diameters and 80 nm lengths.

This general procedure will also produce nanorods of cadmium selenide (CdSe) or cadmium sulfide (CdS). The precursors and molar ratios necessary for CdSe nanorods can be found in the reports by Peng, et al.²⁻⁴ The details of CdS nanorod synthesis are described.⁵ Chapter 4 and Chapter 5 outline chemical modifications to nanocrystals and methods for forming nanocrystal heterostructures after they are synthesized and purified according to the above procedure.

2.2 “Top-Down” Device Fabrication

As discussed in Chapter 1, robust nanoscale electrical contacts to individual semiconductor nanocrystals require nanoscale lithography. The fabrication of devices in this study utilized the electron-beam lithography and optical lithography facilities at the University of California, Berkeley Microlab. Identification of nanoparticles on test chips and post-measurement analysis required high-resolution transmission electron microscopy (HR-TEM) and scanning electron microscopy (SEM) at the Molecular Foundry at Lawrence Berkeley National Laboratory. Test chips were fabricated on 6” Si wafer substrates with 300nm thermal oxide, purchased from Nova Electronic Materials, Ltd.

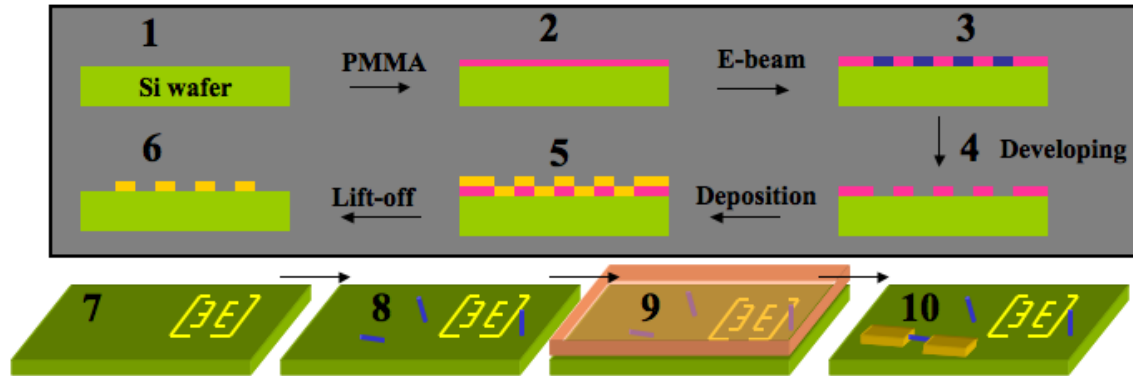


Figure 2.1 Cartooned fabrication process for single nanocrystal based devices. Nanocrystals are imaged by SEM with respect to the pre-defined alignment markers during step 8.

Silicon test wafers were first patterned with photolithography to create 100 μm by 100 μm with 5 / 45 nm thick Cr / Au squares, respectively, as back gate electrodes, and then coated with a 10 ± 5 nm Si_3N_4 dielectric layer deposited by plasma enhanced chemical vapor deposition. The thin Si_3N_4 dielectrics layer was characterized to have only $\sim \text{pA}$ leakage current per applied Volt bias and a breakdown voltage greater than 9 V at 5 K in most cases. The substrate was then patterned with alignment markers fabricated by e-beam lithography (JEOL 6400 SEM equipped with Nability lithography systems) on top of the Au square back gate area.

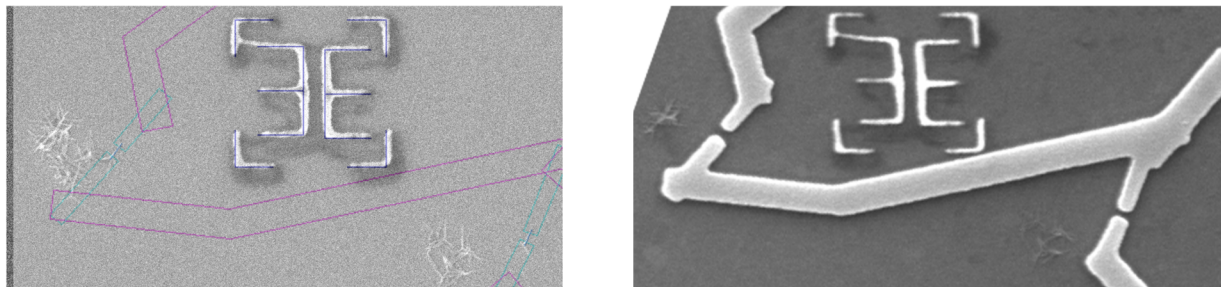


Figure 2.2 SEM showing single nanocrystals before (left) and after (right) electrode contact. The bracketed alignment marker “3E” is 1 μm x 1 μm . Alignment accuracy better than 30 nm is routine. See Figure 1.3 for a higher magnification zoom at the device.

Purified CdTe nanorods prepared according to the synthesis above were diluted in anhydrous toluene to concentrations of ~ 1 μM of cadmium in toluene. The procedure for making quantitative stock solutions of nanocrystals is described Robinson et al., and correlates UV-Vis absorption data with inductively coupled plasma mass spectrometry (ICP-MS) measurements of standard nanocrystal solutions.⁵ Approximately 20 drops of the nanocrystal solution were spin-deposited sequentially onto the substrate with pre-patterned alignment markers at 2000 rpm. The individual nanorods were well separated with an area density of $\sim 1\text{-}10$ / μm^2 . The positions of nanorods were located with respect to the alignment markers using SEM (Zeiss Gemini Ultra-55) at low accelerating voltage (< 1 kV) and low beam current in order to avoid damage to the sample before electrical characterization.

The substrate was then spin-cast at 4000 rpm for 60 seconds for each layer of a bi-layer electron beam resist treatment. First, methyl methacrylate-methacrylic acid copolymer (MMA-MAA) was deposited and cured for 5 minutes at 150 $^{\circ}\text{C}$. Next 950 KD polymethyl methacrylate (PMMA) was deposited, followed by a minimum 30 minute cure at 150 $^{\circ}\text{C}$. Both resists were purchased from Microchem Inc. Electron-beam lithography and electron-beam metal evaporation were used to define 60 nm thick palladium contacts onto individual nanorods. For some experiments, devices were prepared on Si_3N_4 TEM windows instead, with an otherwise identical procedure in order to allow HR-TEM characterization of the electrode-nanocrystal interface. Better than 30 nm alignment accuracy is routinely achieved on either substrate, ensuring high yield of contacted nanorods.

2.3 Device Physics of Single Electron Transistors

Initial studies characterizing the electrical behavior of single nanocrystals observed strong electron-electron correlations during transport, such that the nanocrystals behaved as single electron transistors (SET).⁶⁻⁹ Chapter 3 reports an extension of this earlier work, in which the characteristic coupling of single electron states in individual semiconductor nanorods indicated the problematic chemical reactivity at electrode contacts described in section 1.6. An introduction to the theoretical framework that

defines device operation of SET's will aid interpretation of the results presented in Chapter 3.

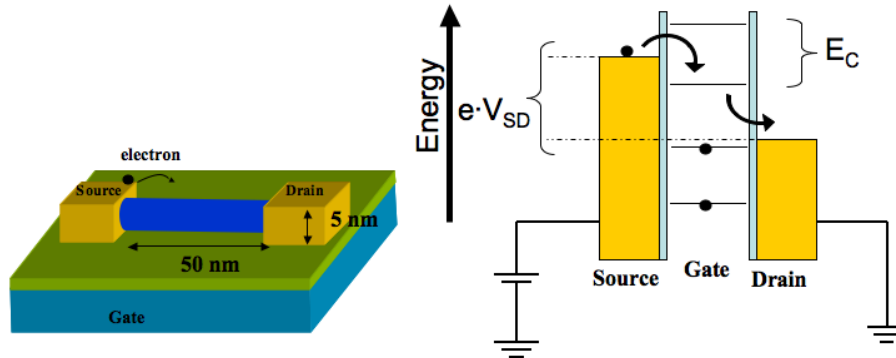


Figure 2.3 Device schematic (left) and simplified energy diagram (right) of a single nanorod SET. A current will only flow when the source-drain bias (V_{SD}) accesses a single electron state in the nanocrystal. These states separate at regular intervals by the charging energy, E_C .

The simplest SET consists of two tunnel junctions in series, sequestering a central region, called an island, which is also capacitively coupled to a gate electrode. As cartooned in Figure 2.3, the potential of electrons on either side of the island is controlled by the applied voltage of the source and drain electrodes. For current to flow, an electron must tunnel from the source electrode onto the island and then off of the island into the drain electrode. However, the self-capacitance of the island confers an energy cost associated with the addition or removal of charge. From classical electromagnetic theory, the energy required to charge or discharge a capacitor is $q^2/2C$, where q is the amount charge transported and C is the capacitance, defined by the local geometry and dielectric environment. If the island is approximated as a sphere, $C = 4\pi\epsilon r$ where ϵ is the permittivity of the surrounding medium and r is the radius of the sphere.

This simple description predicts that nanoscale geometries with very low capacitance can require significant energy to remove or add the elementary quantum of charge corresponding to a single electron, e . For example, an electrically neutral 10 nm sphere surrounded by air will exhibit a charging energy, $E_C = e^2/2C = 14$ meV, required for an additional electron to occupy the sphere. After one electron is added to the sphere, a second electron will require an additional 14 meV to reside there. Essentially, the first electron hinders the addition of the second through the strong coulombic repulsion of such a confined local geometry. Each single electron state on the sphere is therefore separated

in energy by E_C , where the magnitude of E_C scales inversely with size.

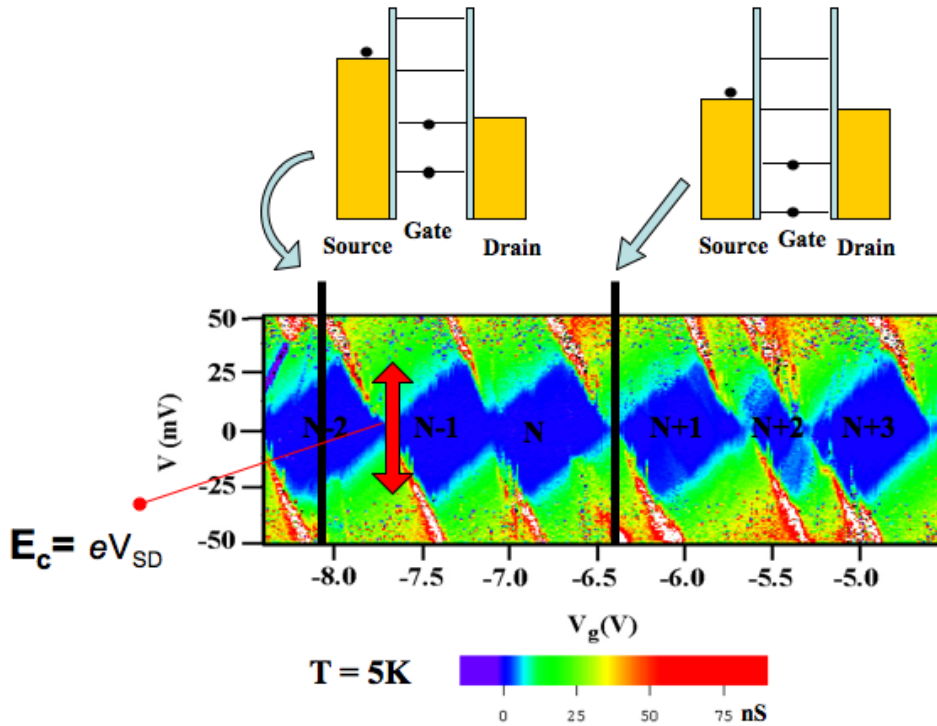


Figure 2.4 “Stability plot” of differential conductance (dI_{SD}/dV_{SD}) as a function of source-drain bias (V_{SD}) and gate bias (V_G) in a single nanorod. Each vertical slice of the plot corresponds to the $I_{SD}-V_{SD}$ response at a unique gate voltage, with the schematic energy diagram at the onset of conduction pictured above. The charging energy, E_C , is extracted from the maximum source-drain voltage span of the coulomb diamond. Each diamond defines a stable electron configuration on the nanorod, which has one more electron than the left-adjacent diamond.

Experimentally, E_C is probed by measuring the minimum bias required for current to flow across the SET, to overcome the so-called “coulomb blockade” induced by the electron-electron repulsion. Alternatively, an applied gate voltage to the island will shift all of the single electron states up or down in energy compared to the Fermi level of the source and drain electrodes. At an infinitesimal source-drain bias, current will only flow when resonant tunneling through a single electron state is possible (see Figure 2.4). This is the mechanism by which the transistor gate controls the flow of single electrons. It is useful to plot the differential conductance through an SET as a function of source-drain bias (V_{SD}) and gate bias (V_G), as in Figure 2.4, to emphasize regions of stable, non-changing electron occupation on the island. These diagrams are called stability plots. The regions where no current flows correspond to the blue “coulomb diamonds” in Figure 2.4. Moving from left to right where adjacent diamonds touch corresponds to adding an additional charge, increasing the stable electron occupation on the island by one. This ability to control the electron configuration on the island explicitly via an external circuit is another reason why such nanoscale materials are sometimes called “artificial atoms”.

Numerous studies have verified the device physics of SET’s since the advent of high quality nanoscale junctions in the late 1980’s. See Devoret¹⁰ for a review of the

history and theoretical framework in the field, including interactions arising from electron spin, and Wasshuber¹¹ for a modern treatment of computational methods for modeling SET device operation. Careful analysis of differential conductance plots obtained from SET's provides some of the most detailed information available elucidating quantum confinement and dimensional control in matter. Many experimental parameters can be extracted from the plots, including relative magnitude of tunnel barriers on and off the island, the excited state electronic structure, and single spin and single photon coupling.¹⁰ A few important considerations for utilizing this powerful research technique follow. First, the island and contact electrodes must be small in order to minimize capacitance with the leads and ensure strong electron repulsion, for large E_C . To avoid thermal excitations of carriers through the single electron states and a loss of resolution in the stability plot, it is often necessary to work at cryogenic temperatures so that $E_C \gg k_B T$. Also, the uncertainty principle requires that the resistance across the tunnel barriers defining the device is larger than h/e^2 and is relatively symmetric at the source and drain electrode contact to ensure a potential well on the island. All of these conditions must be true for a nanoscale object to behave as an SET.¹⁰

Until this point in the discussion, the description of SET device operation has been generally applicable to any nanoscale system. Prototypically, metallic nanostructures exhibit SET behavior,^{12,13} because the single electron states ultimately result from the quantization of the electric charge in the form of electrons, rather than any attenuation of the density of states (DOS) in the band diagram of the metal nanostructure. However, one of the most compelling reasons for studying semiconductor nanostructure SET's is the intriguing possibility that single electron states may couple with the discrete atomic-like states near the band edge in these materials. This coupling can allow electrically mediated "single electron spectroscopy" of the band edge DOS, and a schematic of the process is cartooned in Figure 2.5. Experimentally, this coupling is manifest as a steady increase in size of coulomb diamonds in the stability plot, maximizing at the band gap value as the gate voltage sweeps through the band edge. This behavior has been observed in semiconductor SET's fabricated entirely via nanolithography with atomic layer deposition (ALD) of the semiconductor material and in semiconductor carbon nanotubes, for example.^{14, 15}

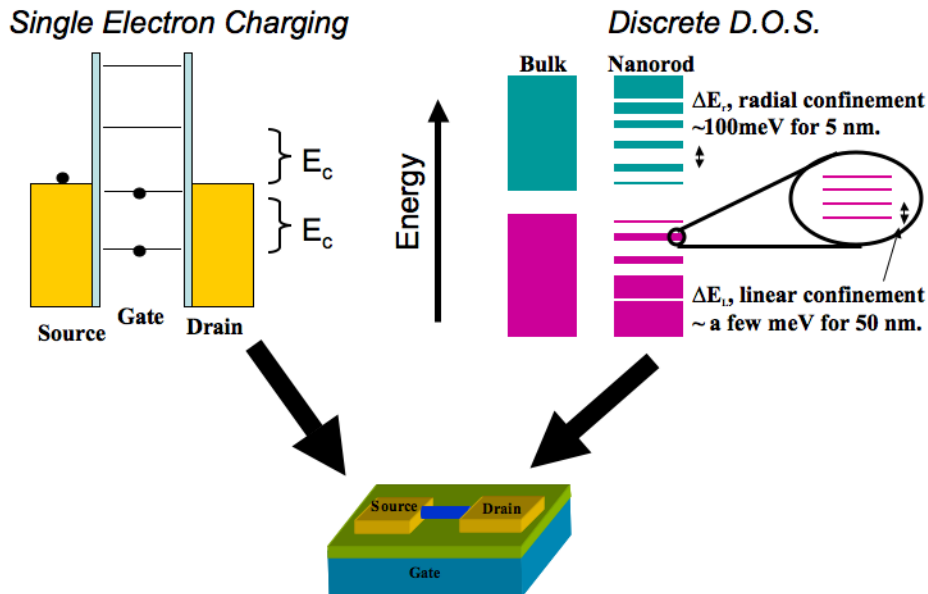


Figure 2.5 Schematic energy diagrams of two different nanoscale electronic phenomena, which may couple in a semiconductor nanocrystal SET.

Unfortunately, direct coupling of the of the electronic structure resulting from quantum confinement and the single electrons states due to coulomb blockade has not been observed systematically in colloidal semiconductor nanorod-based SET's.^{6, 8} In many cases individual CdTe or CdSe nanorods display the regular, periodic diamonds pictured in Figure 2.4, but there is no indication of a band gap for gate voltages that can be probed experimentally. Further, there is no clear dependence on the metal comprising the contact electrode, which sets the Fermi level of tunneling electrons. More commonly, stability plots of single nanorods exhibit a stochastic, or saw-tooth structure in the non-conducting regions indicative of multiple SET's in series. Figure 2.6 provides a schematic energy diagram that produces a saw-tooth stability plot. In this arrangement, there is no gate bias that will allow tunneling of electrons at an infinitesimal source-drain bias, and a larger source-drain bias must always be applied for current to flow. In the worst cases, common for SET's fabricated from CdS nanorods, the devices show no electrical response at all despite indication of successful fabrication by SEM. Chapter 3 describes experiments that rationalize this behavior in terms of compositional segmentation along the nanorods induced by chemical reactions at the deposited metal electrode contacts. Later chapters explore successful strategies for avoiding this complication altogether.

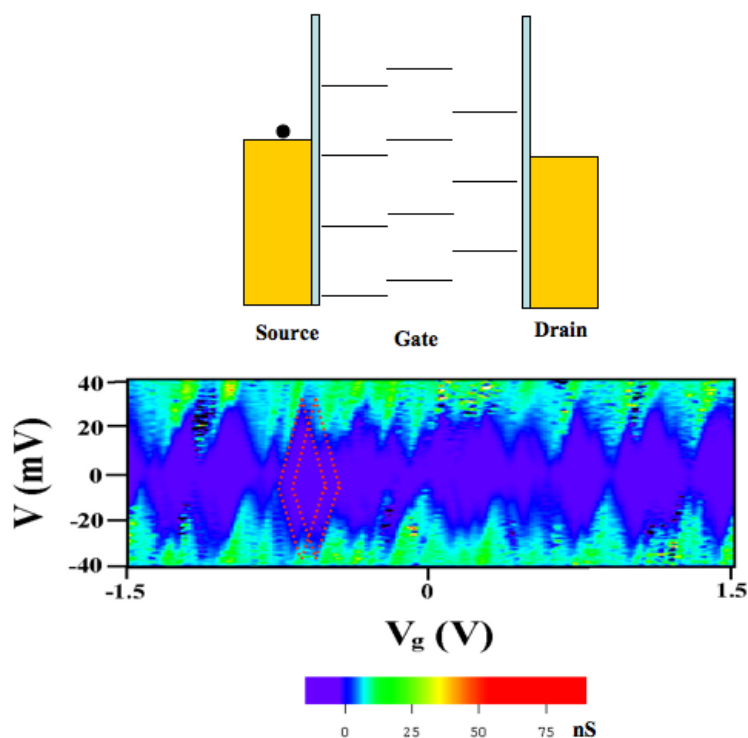


Figure 2.6 Schematic energy diagram (top) of multiple single electron states in-series. The stability plot (below) shows the electrical response from a single CdTe nanorod that exhibited electrical behavior consistent with such an energy diagram.

2.4 Chapter 2 Bibliography

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Chapter 3. “Top-Down” Devices

Reactivity at Electrical Contacts to Individual Semiconductor Nanorods

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3.1 Single Electron Transport in Semiconductor Nanorods

We report the results of charge transport studies on single CdTe nanocrystals contacted via evaporated Pd electrodes. Device charging energy, E_C , monitored as a function of electrode separation drops suddenly at separations below ~ 55 nm. This drop can be explained by chemical changes induced by the metal electrodes. This explanation is corroborated by ensemble X-Ray photoelectron spectroscopy (XPS) studies of CdTe films as well as single particle measurements by transmission electron microscopy (TEM) and energy dispersive X-Rays (EDX). Similar to robust optical behavior obtained when nanocrystals are coated with a protective shell, we find that a protective SiO_2 layer deposited between the nanocrystal and the electrode prevents interface reactions and an associated drop in $E_{C,\text{MAX}}$. This observation of interface reactivity and its effect on electrical properties has important implications for the integration of nanocrystals into conventional fabrication techniques and may require novel structures for functional nanocrystal-based devices.

Three-terminal electrical measurements can carefully probe the electronic structure of a wide range of mesoscopic systems and nanostructures.^{1,2} This stems from the ability to systematically adjust the energy required to add or remove a charge from a nanoscale object. At low temperatures and in a magnetic field one can also control the quantum or spin level that is being probed.¹ Information obtained in this way provides perhaps the most detailed look into the effects of quantum confinement and dimensional control of semiconductor systems. When we investigate nanostructures in three terminal geometries, however, questions arise regarding the nature of the electrical contacts. Indeed as we study smaller and smaller nanostructures it becomes increasingly likely that the electrical contacts substantially modify the quantum object under study.

Our interest is in the electrical study of colloidal semiconductor nanocrystals. Due to their size-dependent optical properties and the ability to introduce them into diverse chemical and biological environments, colloidal dots and rods are one of the most important examples of controlled quantum structure available.^{3,4} This control comes at a price; the solution-based preparation as well as complicated surface ligand chemistry

makes reliable electrical contacts and reproducible measurements of these structures difficult.

Prior studies of CdSe nanocrystals and nanorods illustrate these difficulties. The nanostructures resist a unified description of quantum confinement effects by both optical and electrical characterization except by the most gentle experimental techniques. For example, scanning tunneling microscopy⁵ as well as break junction experiments⁶ show a well defined band gap and are even capable of resolving level structure in sufficiently small nanocrystals. These results can be consistent with energy gaps and level structure observed with optical spectroscopies.^{5,7} However, individual nanocrystal electrical behavior is sensitive to local charge environment,^{8,9} and two terminal measurements must be interpreted with care if comparison to an absolute energy scale is desired. It is more challenging to reconcile the complex charging energy patterns obtained when nanocrystals are instead addressed by lithographically deposited electrodes with the band gaps and level structures obtained by these other methods.¹⁰

To explore the mechanism behind these differences, we present a systematic study of the electrical properties of single semiconductor nanocrystals addressed by lithographically defined electrodes in a three-terminal geometry. Specifically we track variations in nanorod charging energy as a function of electrode spacing for both bare and insulated nanocrystals.

3.2 Device Fabrication and Characterization

We prepared CdTe nanocrystals as reported previously¹¹ and deposited them from toluene solutions onto test chips. Nanocrystals were located with respect to predefined alignment markers and we used electron beam lithography to create source and drain contacts (5 nm Cr / 45 nm Pd). A Au film separated from the device by 10 nm of SiN served as a back gate. A schematic of a single nanocrystal device is shown in Figure 3.1a. Electrode separation varied from 30 nm to 100 nm as measured by scanning electron microscopy (SEM) (Figure 3.1b). All results reported here were measured at 5 K in a Janis (STVP-100) He4 flow cryostat.

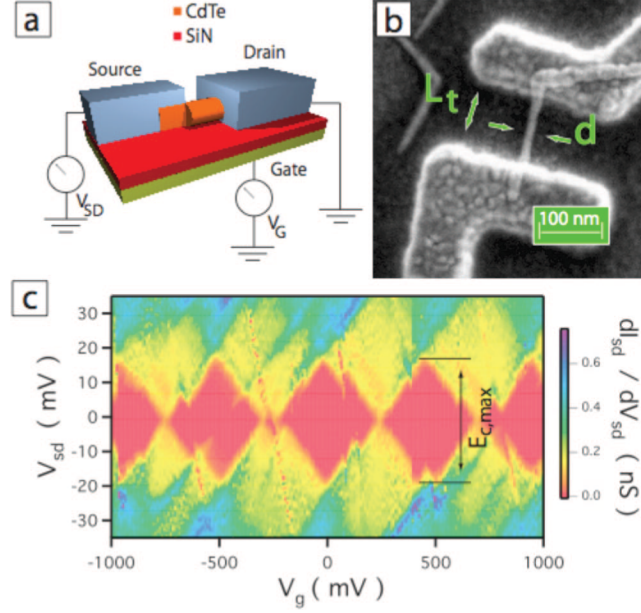


Figure 3.1 (a) Schematic of a three terminal single nanocrystal (NC) device. The Au gate is separated from the NC by 10 nm of Si_3N_4 . Pd source and drain electrodes are defined by e-beam lithography. (b) SEM image of single nanocrystal device of diameter, d , and total length, L_t . (c) Stability plot of single nanocrystal device. We extract the charging energy ($E_{c,max}$) from the source-drain span of nonconducting (red) regions.

We measured source-drain current (I_{sd}) as a function of source-drain voltage (V_{sd}), as well as gate voltage (V_g). To visualize the results, we plotted the differential conductance (dI_{sd}/dV_{sd}) as a function of both V_{sd} and V_g (Fig 3.1c). This highlights regions of zero conductance, which represent stable single electron charge states on the nanocrystal.² The energy to charge an object goes as $e^2/2C$, where C is capacitance and proportional to the size of the object. This confers an inverse relationship between the charging energy and the size of the region to be charged. Simply put, it is the energy required to offset the repulsive forces generated by adding an extra electron to the object. We determine this parameter experimentally. For each device, we measure $E_{c,MAX} = eV_{sd,MAX}$, where $V_{sd,MAX}$ is the voltage difference between the upper and lower limits of the largest region of zero conductance, outlined by the black line in Figure 3.1c.

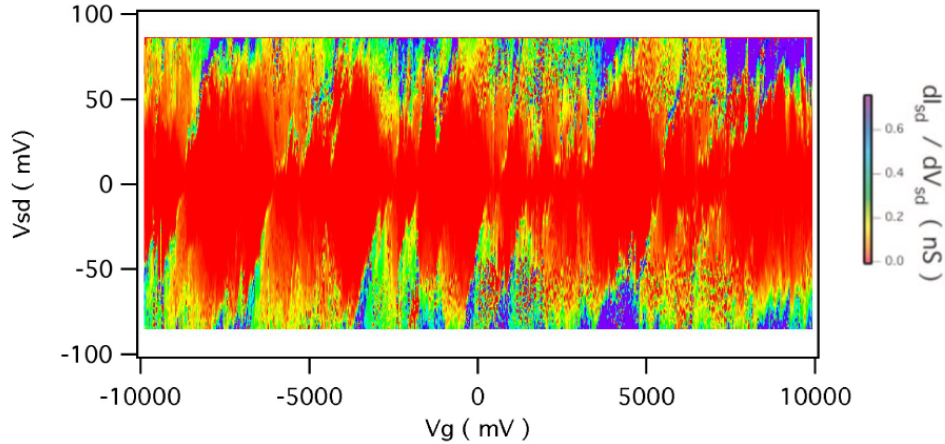


Figure 3.2 Stability plot of a single nanocrystal device exhibiting “in-series” behavior ($L_t > 55$ nm). Here also, we extract the charging energy ($E_{c,max}$) from the source-drain span of non-conducting (red) regions.

The electrical behavior of the devices falls into two categories. In the first (Figure 3.1c) we observe evenly spaced, uniform charging energies. These regular coulomb diamonds suggest a single charged object with nearly continuous energy levels. In the second (fig 3.2), devices exhibit electrical behavior more consistent with multiple tunnel junctions in series *viz.* higher maximum charging energies, and a jagged profile along the diamond edges.^{2,12} For either case, we expect $E_{C,MAX}$ to track well with the device dimensions.

We recorded $E_{C,MAX}$ as a function of electrode separation, L_t , on the nanocrystal. In principle it is more accurate to track the volume of nanocrystal material between the electrodes, however the SEM resolution limits the determination of significant differences in the nanocrystal diameter, which was ~ 12 nm for all devices.

3.3 Reactivity at Electrode Contacts

Figure 3.3 reveals that for electrode separations greater than 60 nm, $E_{C,MAX}$ increases as expected with decreasing electrode separation; however, below ~ 55 nm the charging energy drops with decreasing electrode separation. This unexpected result can be accounted for when we consider the possibility that there is a chemical transformation of the nanorod when the metal electrode is deposited on it and that this zone of chemical transformation extends 20-30 nm into the nanorod, as cartooned in Figures 3.3c-e. Several lines of evidence that support this picture are described below.

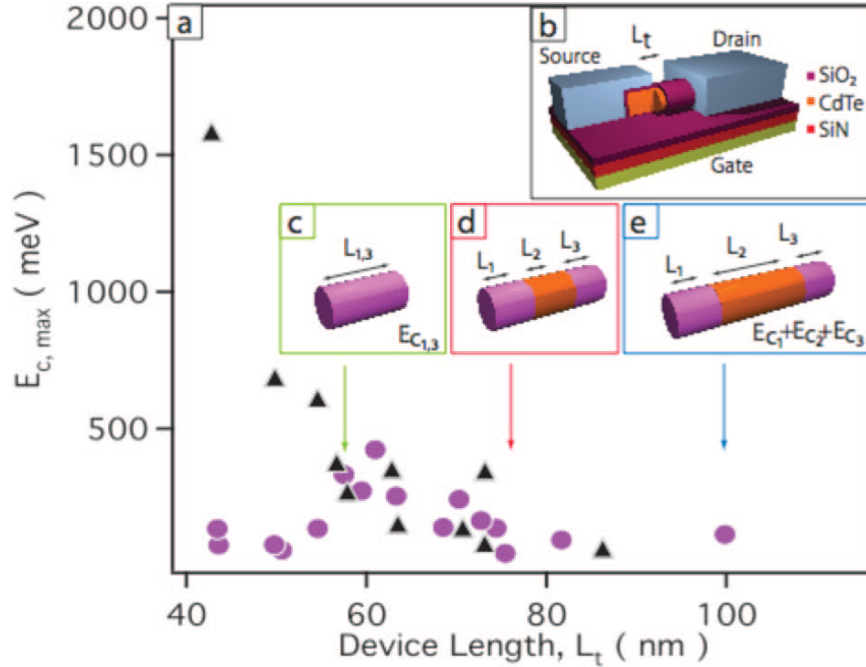


Figure 3.3 (a) Largest addition energy ($E_{c,max}$) of nanorod devices vs. electrode separation. Purple circles show devices not treated with SiO_2 . Black triangles show devices protected by SiO_2 film as drawn in (b). (c-e) Without SiO_2 treatment, transport is determined by the interplay between zones of reacted NC near the electrodes (purple) and unreacted NC in the middle (orange). For sufficiently small $L_t \sim 55$ nm (c) the reaction spans the NC and $E_{c,max}$ drops. At larger L_t (d, e) charges pass from reacted to unreacted zones. This leads to “in-series” contributions to the total addition energy ($E_{c,max}$).

First, consider the electrical measurements themselves, in the context of the nanorod consisting of three zones. There are two “interaction zones” near each electrode where the nanorods are chemically modified, separated by a central zone that consists of pristine nanorod. The size of the outer interaction zones (red) remains roughly constant, limited presumably by a solid-state diffusion process. When electrode spacing (L_t) decreases, these interaction zones encroach on the center zone (orange). The energy to charge the center zone dominates $E_{C,MAX}$ when its length is reduced below that of the outer zones. At small enough L_t , the chemically modified zones merge to span the entire NC; the charging energy falls as the volume is now twice the size of a single interaction zone (Figure 3.3c). For $L_t < 55$ nm we observe mostly simple electrical behaviors. This corroborates our interpretation as it suggests multiple tunnel junctions in series ($L_t > 55$ nm) give way to simple energy spectra of a singly charged zone for shorter electrode spacing, as in Figure 3.1c, ($L_t < 55$ nm). The drop in $E_{C,MAX}$ around ~ 55 nm indicates that the interaction zones extend approximately 20-30 nm into the nanocrystal. We note that this interface is likely not abrupt, as cartooned in Figure 3.3, but a gradient whose sharpness and extent is defined by the chemistry of the electrode and the semiconductor.

The total energy to charge the device is approximately the sum of the individual charging energies of each region. For devices in series, stochastic level alignments lead to fluctuations in $E_{C,MAX}$. Fractionally, these can be as high as $N^{-1/2}$, where N is the number of zones.¹³ This contributes to the observed scatter in our $E_{C,MAX}$ data.

A second line of evidence that supports the above picture arises when we consider nanorods protected from reaction with the evaporated metal via a thin oxide barrier layer. We coated test chips of CdTe nanocrystals with a thin 5 nm layer of SiO₂ before depositing the electrodes. This helped distinguish whether the discontinuity in E_{cmax} was due to a specific chemical interaction of Pd with CdTe at the interface, or rather an electrostatic effect of the device geometry.¹⁴ Figure 3.3a shows that for the protected nanorods, the charging energy simply increases with decreasing electrode separation, as expected. The trend in $E_{\text{C,MAX}}$ vs. L_t is maintained for these SiO₂-treated devices to the smallest L_t achievable in our experiment, with no observed discontinuity. This shows that electrostatic effects and geometry are not responsible for the discontinuity in $E_{\text{C,MAX}}$. The non-reactive SiO₂ film arrests the compositional segmentation of the nanocrystal. The use of thermal deposition techniques to add the SiO₂ layer admits the possibility of pinhole shorts. These allow relatively easy flow of charge carriers despite the thickness of the insulating layer, while still providing some barrier to atomic diffusion. Experiments are currently underway on more robustly protected nanocrystals.

The results and interpretation we present are consistent with prior studies describing the modification of the composition and electronic structure of bulk semiconductors in contact with metal electrodes. Differential scanning calorimetry has tracked the reactivity of CdTe surfaces with many metals.¹⁵ Consistent with thermodynamic arguments, these reactions occur at temperatures far lower than those required to thermally deposit metal electrodes during conventional lithography. Brillson¹⁶ and others^{17,18} showed that bulk metal-CdTe interfaces react to form metal-Cd alloys or metal-Te complexes. These reactions alter the local electronic structure and overall semiconductor device performance. Importantly, un-favored reactions can occur, but are limited to a ~20 nm distance from the interface,¹⁶ a length scale similar to our findings. In fact, surface structure plays a key role in semiconductor reactivity. For example surface stoichiometry, controlled by etching¹⁹ tunes the reactivity of semiconductor surfaces.¹⁵ We note that we expect our nanocrystal surfaces to be quite reactive due to defects, dangling bonds and incomplete ligand coverage. We also note that the diameter of our nanorods is on the same order as the size of a bulk semiconductor surface.

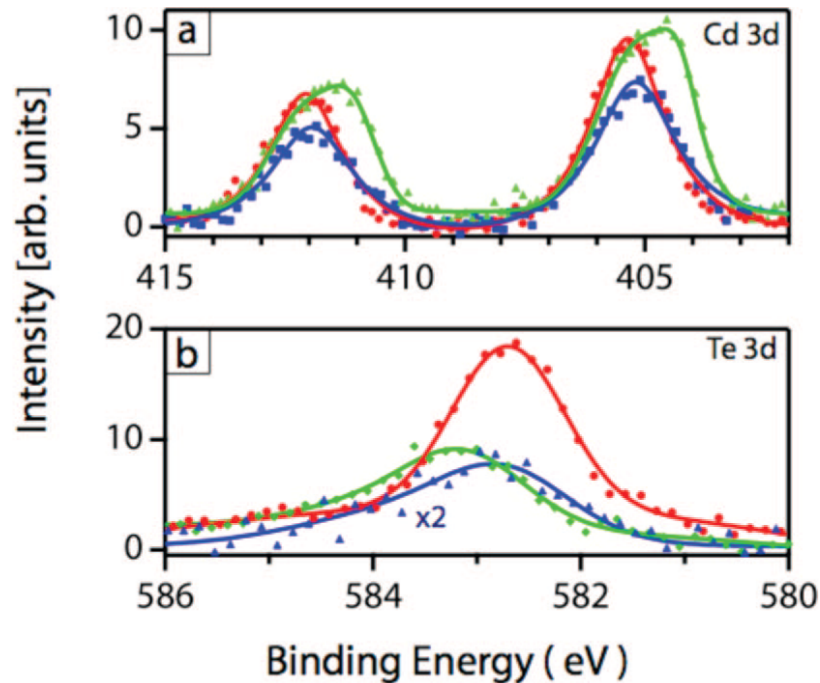


Figure 3.4 XPS data: red curves are CdTe films, blue curves are SiO₂-coated CdTe films with 8 Å Pd over-layer, green curves are CdTe films with 8 Å Pd over-layer; (a) Cd 3d emission reveals a shift to lower binding energies and (b) Te 3d emission shifts to higher energies only for unprotected (green) films.

To further confirm that the electrode reacts with the nanocrystal, we tracked changes in core electron binding energies of dense monolayer films of CdTe nanocrystals when Pd is evaporated on top, using X-Ray photoelectron spectroscopy (XPS). We considered films of nanocrystals with, and without a thin layer of Pd (0.8 nm). We compared these to films of nanocrystals protected by a 5 nm SiO₂ barrier both with, and without Pd. Figure 3.4 summarizes the results. When Pd is deposited directly on the nanocrystal film, we observe shifts to lower binding energy for Cd 3d electrons as well as shifts to higher binding energy for Te 3d electrons. This indicates a chemical change occurs in the nanocrystals only when they are in intimate contact with Pd. This further implies that Cd alloys with Pd, in excellent agreement with previous results.^{15,18} In the case of SiO₂ protected nanocrystal films, we observe little to no shifts in Cd or Te binding energies. This highlights that shifts in binding energies originate from the interaction of the NC in direct contact with Pd.

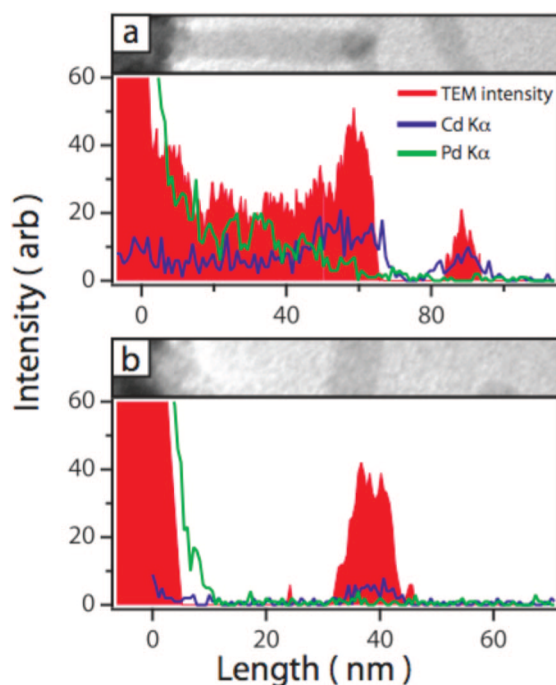


Figure 3.5 TEM data of CdTe NCs in contact with Pd. The intensity profile (taken from the center of the images) is shown in red. $K\alpha$ radiation from Cd (blue) and Pd (green) is superimposed. (a) Pd is present throughout much of the nanocrystal in contact with the electrode though not present at all in a NC not in contact with the electrode found at ~ 80 nm. (b) Control image shows excellent agreement between electrode edge as determined by both intensity and Pd $K\alpha$ signal.

Finally, we simultaneously spatially and chemically profiled the reaction zone between the metal electrode and individual nanorods. We cast films of CdTe nanocrystals onto Si_3N_4 (30 nm) TEM windows. Next, we deposited 50 nm of Pd in 100 nm wide strips. We investigated these samples using a JEOL 2100-F transmission electron microscope (TEM) (STEM mode, 200 kV, probe size 2 nm) equipped to analyze energy dispersive x-rays (EDX). We measured line scans of elemental composition for single nanocrystals at the electrode-nanocrystal interface and along the length of the nanocrystal by tracking $K\alpha$ emission from Pd, Cd and Te. The K lines were used instead of L to insure good separation between these elemental signals, and control samples indicate that we have good discrimination. Figure 3.5 highlights two representative cases. Figure 3.5a shows a TEM image (grey scale), line scan (red) and corresponding Pd $K\alpha$ (green) and Cd $K\alpha$ (blue) emissions. Pd is present throughout the nanocrystal. Consistent with our hypothesis, this indicates diffusion of Pd into the CdTe nanocrystal and concomitant alteration of the nanocrystal composition near the metal-semiconductor interface. Figure 3.5b shows a representative control and highlights the good elemental discrimination, signal to noise, as well as excellent alignment between the intensity and elemental line scans.

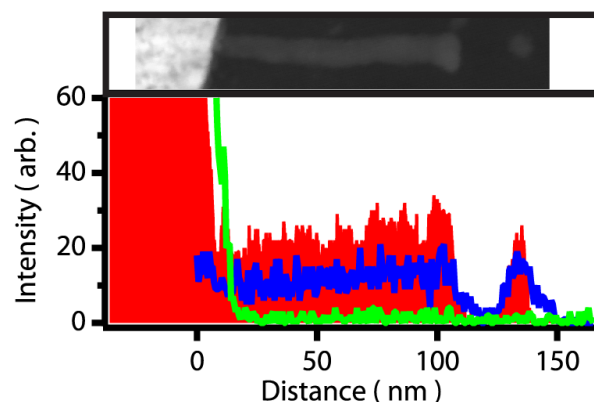


Figure 3.6 TEM data for CdTe NCs protected from Pd by SiO₂. The intensity profile (taken from the center of the images) is shown in red. $K\alpha$ radiation from Cd (blue) and Pd (green) is superimposed. There is no Pd present in the protected nanocrystal.

Taken together the TEM, XPS and the differences between electrical data with and without SiO₂ all point to a reaction between the electrode and the nanocrystal. Though this reactivity is general to all semiconductor surfaces – i.e. the first ~10 nm – it has a dominant effect on the properties of nanocrystals. The following chapters discuss strategies for avoiding this interface reactivity in single nanocrystal devices.

3.4 Chapter 3 Bibliography

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Chapter 4. “Bottom-Up” Devices

Enhanced Semiconductor Nanocrystal Conductance via Solution Grown Contacts

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4.1 Introduction

Characterization of interface reactivity discussed in Chapter 3 proved that it is essential to apply alternative contact methods for device integration of single colloidal nanocrystals for most applications. Chapter 4 and 5 describe a variety of nanocrystal heterostructure motifs that avoid the complications due to nanocrystal reactivity described previously, by taking advantage of bottom-up device fabrication. Here, we report a 100,000-fold increase in the conductance of individual CdSe nanorods when they are electrically contacted via direct solution phase growth of Au tips on the nanorod ends. Ensemble UV-Vis and X-Ray photoelectron spectroscopy indicate this enhancement does not result from alloying of the nanorod. Rather, low temperature tunneling and high temperature (250-400 K) thermionic emission across the junction at the Au contact reveal a 75% lower interface barrier to conduction compared to a control sample. We correlate this barrier lowering with the electronic structure at the Au-CdSe interface. Our results emphasize the importance of nanocrystal surface structure for robust device performance and the advantage of this contact method.

4.2 Single Nanocrystal Electronic Behavior

Single nanostructure electrical measurements directly probe the fundamental limits of semiconductor device miniaturization, providing some of the most precise characterization available of electronic structure resulting from quantum confinement and dimensional control.¹ When the strategy is employed for colloidal semiconductor nanocrystals we also learn the ultimate transport efficiencies of these materials, crucial for determining their utility in photovoltaic applications, as one important example, without the convolution of particle-particle carrier hopping mechanisms or particle size dispersity that are difficult to account for in studies of nanocrystal thin film solids.²

Besides fabrication challenges, single particle experiments are complicated by the specific electronic structure of the semiconductor-metal interface between the nanoparticle and the device electrode, which critically determines the barrier physics to charge injection and thereby overall device performance. The nanocrystal surfactant

coverage, heightened surface energy, and decreased density of states may contribute to the complex interface of a contacted device.^{3,4} Indeed, the variety of II-VI semiconductor colloid single particle electrical behaviors reported in the literature suggests the contact method may be as important as the sample itself for determining the device properties at such small scales. For example, previous work from this group tracked severe compositional modification of single nanocrystals into separate regions with coupled electrical response when contacted by traditional lithographic techniques.⁵ This contrasts trapping⁶ or STM experiments⁷ that display tunneling behaviors that depend significantly on the strength of the coupling to the electrode and therefore also the nanocrystal interface electronic structure.

The goal of this study is to offer a systematic comparison of CdSe nanorods with and without Au tips to test the influence of the contacts. Using a synthetic method reported previously, CdSe nanorods are tipped with Au in solution, giving an intimate, abrupt nanocrystal-metal contact free of surfactant. We compare electrical response to a control sample of standard CdSe rods, with nanocrystals of both type individually adsorbed to pre-defined Au junctions. We report a large increase in the conductance of the Au-tipped CdSe heterostructures and explain this in terms of the differing electronic structure of the Au-CdSe interface for both samples.

4.3 Device Fabrication and Measurement

CdSe nanorods were synthesized and purified using a previously published method⁸ and dissolved in toluene. (red TEM, fig. 4.1). A fraction of the sample was tipped with Au according to a method described previously by Mokari.⁸ (green TEM, fig. 4.1). Briefly, a toluene solution containing gold trichloride (AuCl_3 , 12 mg, 0.04 mmol), didodecyldimethylammonium bromide (DDAB, 40 mg, 0.08 mmol) and dodecylamine (DDA, 70 mg, 0.37 mmol) was sonicated for 5 minutes and then added dropwise to a suspension of nanorods stirring under N_2 . The product was precipitated with methanol and separated by centrifugation.

Source and drain electrodes with junctions spanning 20-40 nm were fabricated on silicon wafer test chips using e-beam lithography, followed by deposition of 55 nm Au on 10 nm Ti. A film of 10 nm of silicon nitride or aluminum oxide was deposited via atomic layer deposition [ALD] before the electrodes to prevent shorting through the silicon substrate.

The nanorod samples were adsorbed to these pre-defined Au junctions by submerging the chip in the appropriate μM nanorod-toluene solution, and drying with N_2 . Once fabricated, the current through individual nanorod devices was characterized in a two-terminal geometry as a function of source-drain voltage and temperature. All data reported here were measured in a 10^{-6} torr atmosphere with a Janis Research ST-500-2 micromanipulated probe station, chilled with liquid He or N_2 cryogen.

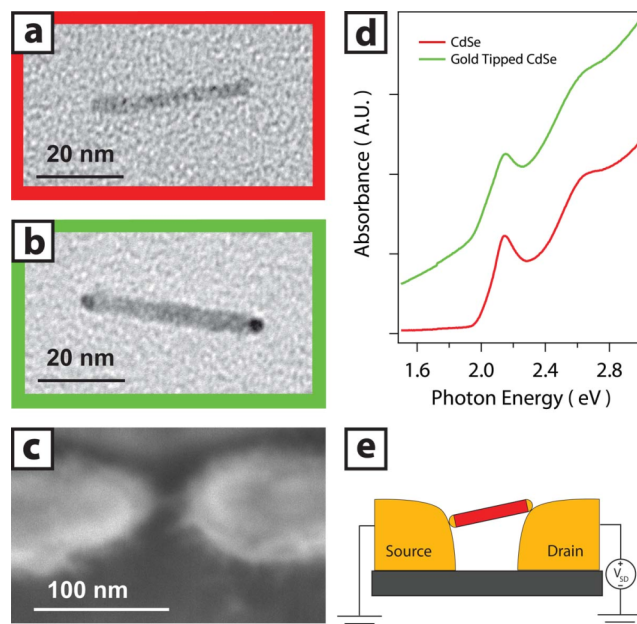


Figure 4.1 TEM image of CdSe nanocrystal before (a) and after (b) Au tip growth. SEM image (c) and schematic (e) of single nanocrystal 2-terminal device. After submersing a silicon wafer test chip in a toluene-nanocrystal solution, the evaporating solvent orients individual nanocrystals across predefined Au electrodes fabricated via e-beam lithography. (d) Solution phase optical spectra indicate onset of first exciton absorption at 2 eV for both CdSe (red) and Au-tipped CdSe heterostructure (green) samples.

4.4 Observation of Enhanced Conductivity

Characteristic room temperature electrical data of individual particles from this study are summarized for CdSe [red trace] and Au-tipped CdSe [green trace] nanocrystals in figure 4.2b. Devices made with Au-CdSe heterostructure nanocrystals display an average 6-decade increase in conductivity near zero applied bias (fig. 4.2a) compared to the control CdSe devices. This drastic improvement represents a lower limit for the enhancement the Au tip provides, as our experimental sensitivity was limited to resistance less than $10^{13} \Omega$.

Numerous studies report the conductivity of individual semiconductor nanostructures or estimate that value from the electrical response of thin film nanocrystal solids. The wide range of values in the literature confirms that conductance is highly sensitive to the semiconductor material, surface treatment and contact method. For II-VI semiconductors in particular, spin-cast CdSe nanocrystal thin films without chemical surface treatments or annealing display almost no measurable conductance, greater than $10^{14} \Omega \text{ cm}$ resistivity or $10^{20} \Omega$ resistance per nanocrystal.⁹ When individual nanocrystals are contacted via evaporated metals, alloying and diffusion at the contact alters the semiconductor composition, complicating interpretation, though conductance is generally improved to give $10^9 \Omega$ resistance per a CdTe nanorod.⁵ In this study, because both measured device types consisted of a single CdSe nanocrystal contacted by Au, we propose that the factor that accounts for the stark difference in conductance is the alkylphosphonic acid surfactant layer bound to the pure nanocrystal surface.¹⁰ This

surfactant is not present at the Au-CdSe metal-semiconductor interface of the heterostructure nanocrystals. It is thus critical to understand how surface ligands influence interface electronic structure, and consequently overall device performance, which this report explores in detail.

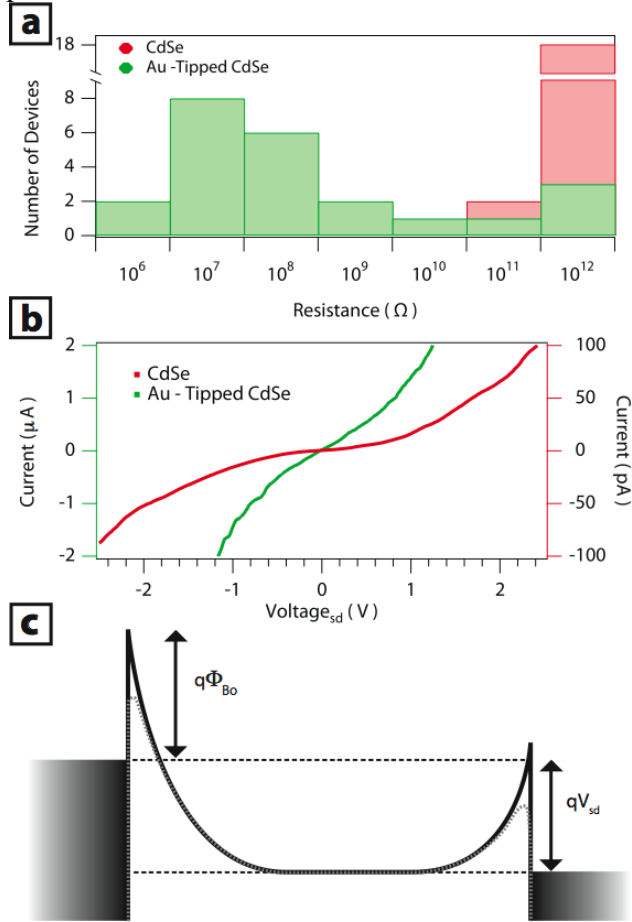


Figure 4.2 (a) Histogram of room temperature device resistance near 0 V applied bias. (b) Representative two-probe I-V trace of a CdSe device (red) and an Au-tipped CdSe device (green) at room temperature. Note the color-coded axes correspond to pA (red) and μA (green) scales. (c) Simplified energy-band diagram of proposed barrier structure across a device under bias. The dashed grey line shows the barrier lowering due to the image potential, not drawn to scale.

Ensemble TEM analysis (fig 4.3) indicates good monodispersity of the starting CdSe rods, with dimensions 4.8 (± 0.8) by 32 (± 5) nm. During synthesis of the heterostructures, the amount of precursor added was optimized for the desired degree of Au overgrowth to give spherical 3.4 (± 0.8) nm diameter Au tips [fig 4.1b]. This treatment otherwise preserves the nanocrystal surface structure, so that surfactant coverage is identical along the walls of the nanorods both with and without Au tips.

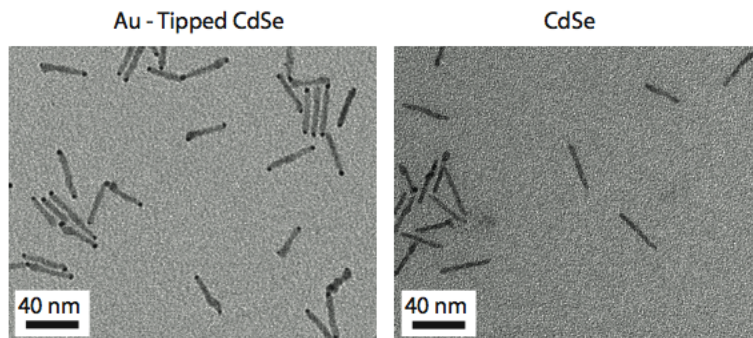


Figure 4.3 Ensemble transmission electron microscopy [TEM]. Statistical analysis of micrographs like those above displaying Au-tipped CdSe nanorods (left) and control CdSe nanorods (right) indicate good sample monodispersity. The nanorods have dimensions $4.8 (\pm 0.8)$ by $32 (\pm 5)$ nm with $3.4 (\pm 0.8)$ nm diameter Au spheres after tip growth.

The critical step of contacting individual nanocrystals to the lithographed electrodes also occurred via self-assembly. Individual nanorods spontaneously bridged the predefined junctions [fig. 4.1c] after submersion in a nanocrystal solution, placed there via the evaporating solvent front and likely oriented by the shrinking strand of solvent that minimized surface tension across the junction.¹¹ The technique is robust, with >75% junctions yielding working electrical devices confirmed by SEM. Control experiments with junctions submerged in pure toluene displayed no electrical response [fig. 4.4]. Though we cannot confirm a single nanocrystal per junction in every device, due to the difficulty of imaging individual CdSe nanorods by SEM, the micrographs indicate we did not measure aggregates or ensembles of particles and that both samples were present in similar surface concentrations near the junctions. Further, multiple particles in parallel across a junction would change the conductance by a multiplicative factor of the number of nanorods in parallel, which could not account for the several orders of magnitude increase observed here for the two different device types.

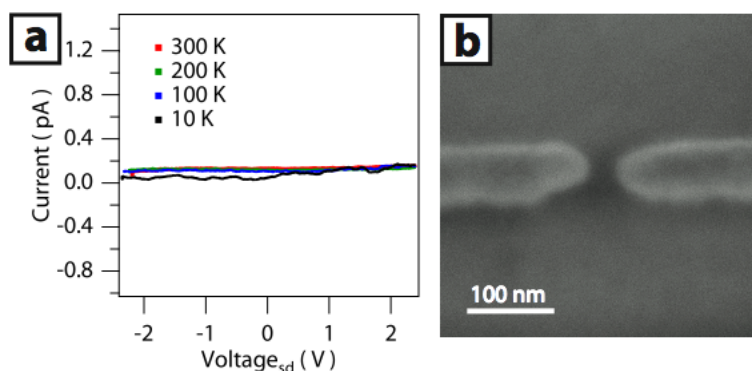


Figure 4.4 Background current of an empty Au junction (a) There is no current response from an Au junction without a nanorod present, across the temperature range of our study. (b) Scanning electron micrograph [SEM] of a device with no nanorods.

An alternative explanation for the enhancement in conductance of the Au-CdSe heterostructures could be that the Au tip growth method fundamentally alters the

semiconducting region of the heterostructure, forming a conductive Au-Cd-Se alloy. However, this explanation is inconsistent with several lines of evidence. Previous studies⁸ by High Resolution Transmission Electron Microscopy [HRTEM] of similarly prepared heterostructure nanocrystals indicate well defined lattice planes corresponding to CdSe and Au in the center and at the tips of the nanocrystal, respectively, in intimate atomic contact. Cryogenic scanning tunneling microscopy [STM] measurements on individual heterostructures¹² corroborated these findings, reporting metallic conduction at the tips and an interior band structure corresponding to CdSe. In addition to these findings, in this study, X-ray photoelectron spectroscopy [XPS] measurements of spin-cast films identified insignificant chemical shifts in the Cd or Se signals of the heterostructures [fig. 4.5]. In addition, UV-Vis absorbance spectra of the two samples show an identical onset for the first exciton absorption at 2.0 eV (fig. 1d), indicating no clear difference in the composition of the semiconductor material in both nanostructures. Based on our measurements and the previous studies, clearly the CdSe region is not alloyed in the heterostructures. The sample purity is further confirmed by examination of the temperature dependence of the nanocrystal conductance.

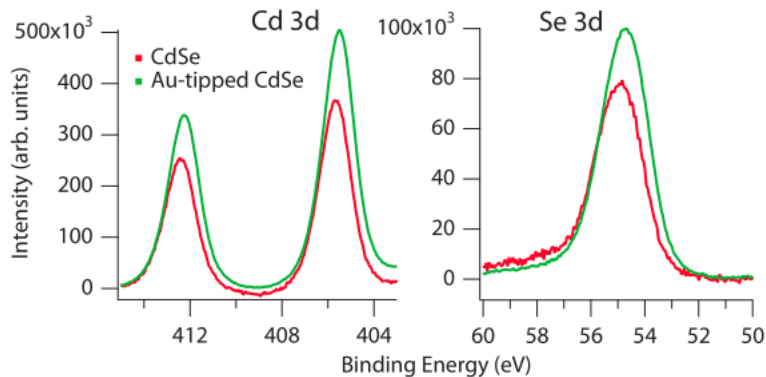


Figure 4.5 X-ray photoelectron spectroscopy. The Cd 3d signal (left) and Se 3d signal (right) for an ensemble of CdSe nanorods (red) and Au-tipped CdSe nanorods (green) show no significant difference in binding energy. A peak shift or broadening of ~ 2 eV would indicate a change in the oxidation state or chemical environment of the Cd or Se atoms present in the Au-tipped CdSe sample.

Both samples in this study exhibit conductivity that is not monotonic with temperature, displaying a minimum conductance near 200 K and a steady increase in conductance to the lowest and highest temperatures probed, from 4.2 K to 400 K. Across this temperature range the Au-tipped samples maintain conductances larger than the control CdSe samples, while both devices exhibit a similar trend in temperature dependence (fig. 3 and 4). However, the magnitude of the conductance enhancement has a strong temperature and voltage dependence, discussed fully below. In general, semiconductor conductivity is the product of carrier concentration and carrier mobility, with each parameter dependent on the thermal activation of free carriers or phonons respectively.¹³ It is necessary to consider both contributions across different temperature regimes to accurately describe the device behavior we observe. In this study, the low temperature device response (< 200 K) suggests tunneling electrons traverse the nanocrystal via a pathway with resistance proportional to the temperature dependent

phonon occupation. The high temperature behavior (> 250 K) indicates a transport mechanism dominated by thermally activated carriers. In both temperature regimes we see evidence of a lowered conduction barrier at the Au-CdSe interface of the heterostructures, which we correlate with the observed conductivity enhancement.

4.5 Low Temperature Response

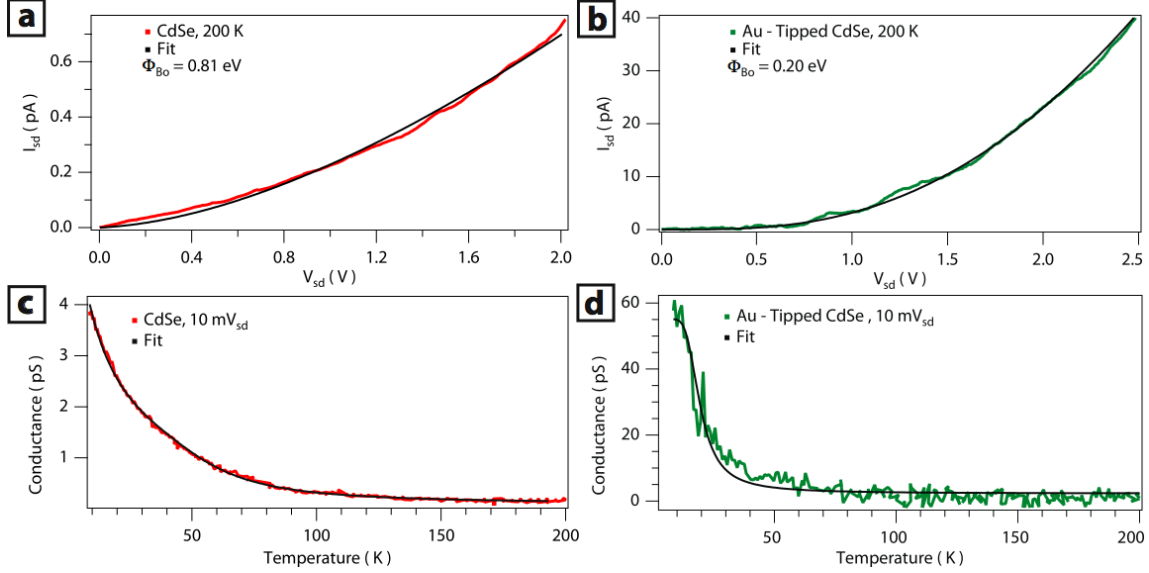


Figure 4.6 Positive I-V trace of a CdSe device (a) and Au-CdSe heterostructure device (b) at 200K with fit (black) to eq. (1). The low bias conductances of a CdSe device (c) and an Au-CdSe heterostructure device (d) with fits to eq. (4) and eq. (3), respectively, reflect the contribution from the Einstein model for heat capacity.

At low temperatures when the thermal activation of carriers is negligible, the current-voltage dependence of both samples suggests carriers tunnel onto the nanocrystal through a voltage-dependent contact barrier. Similar electrical response from individual colloidal CdSe nanocrystals was also observed by Gudinsken¹⁴ and Steinberg¹⁵. Figure 2c diagrams a simplified proposed barrier structure across a biased nanocrystal device. The left barrier at the higher potential side has the limiting conductance that dominates the observed device response. The tunnel barrier width at the left electrode Fermi level decreases upon increasing bias and the device response is symmetric under reverse polarity. The following expression derived in Section 4.8 gives the voltage-dependent tunneling current, I , through such a barrier:

$$I = CV \cdot \exp\left(-2\sqrt{\frac{m\epsilon_s}{\hbar^2 N_D}} \cdot \left[\sqrt{(V + \Phi_{Bo}) \cdot \Phi_{Bo}} - V \cdot b\right]\right) \quad (1)$$

with

$$b = \text{ArcCosh}\left(\sqrt{\frac{V + \Phi_{B_0}}{V}}\right) \quad (2)$$

where Φ_{B_0} is the barrier height, ϵ_s , N_D , and m are the semiconductor permittivity, doping concentration, and effective mass of CdSe, and C is a wave function coupling constant of the electrode to the nanorod.

Figures 4.6a and 4.6b show the high quality of the least squares fit of the device response to equation (1) under positive bias at 200 K. Similar behavior is observed for samples under reverse bias and at lower temperature. The fit determines barrier heights of 0.81 eV for the CdSe device and 0.20 eV for the Au-tipped CdSe device. The lower barrier results in the improved conductance of the heterostructure devices. Further, the control CdSe device shows a two order of magnitude smaller coupling constant, C . Independent of applied bias, this lower coupling constant likely corresponds to an additional barrier between the electrode and the CdSe surface due to alkylphosphonic acid surfactant molecules. This barrier is not diagrammed in figure 4.2c. The fit also determines doping concentrations, N_D , by assuming the bulk CdSe values for ϵ_s , and m .¹³ For the Au-CdSe device in Figure 4.6, $N_D = 4.4 \times 10^{18} \text{ cm}^{-3}$ and for the CdSe control device $N_D = 1.7 \times 10^{21} \text{ cm}^{-3}$. We note that the model of Eq.(1) uses approximations of bulk geometry to solve Poisson's equation, with simplifications at high voltages, and it ignores the effect of an image potential at the electrode interface. Further, the fit parameter containing these materials constants fluctuates over a large range of values during the fitting routine, complicating quantitative analysis. More sophisticated models that better account for the unique structure of the nanocrystal-electrode interface and contributions to current at large voltages will likely yield a more accurate fit. However, the barrier heights and doping concentration determined by this method are in good agreement with a high temperature thermal activation analysis. The high temperature analysis does not have the same limitations described here, and it will be discussed more fully below.

We also plot the low temperature dependence of the low bias conductance for the same CdSe device (fig. 4.6c) and Au-CdSe heterostructure device (fig. 4.6d). The strong increase in conductance with lower temperature is clearly visible for both samples. This low temperature dependence is directly reflected in the temperature dependence of the coupling constant C in Eq.(1). This means that the wave function coupling between the electrode and both nanorod samples is reduced by inelastic scattering caused by phonon fluctuations. We propose that this reduction is directly proportional to the temperature-dependent occupation of phonons, as defined by the Einstein model¹⁶ for heat capacity, C_V . The likelihood of inelastic phonon scattering depends on the number of available phonons. We model the low temperature, low bias resistance of the device, Ω , also accounting for other in-series contributions, Ω_o , to give

$$\Omega = \Omega_o + \alpha C_V = G^{-1} \quad (3)$$

$$\text{with } C_V = 3Nk_B \left(\frac{\theta_E}{T}\right)^2 \frac{e^{\theta_E/T}}{(e^{\theta_E/T} - 1)^2} \quad (4)$$

where α is the proportionality constant, N is the number of oscillators in the solid, θ_E is the Einstein temperature, a material-dependent fitting parameter related to the characteristic phonon frequency, and G is the low bias device conductance.

The least squares fit of equation (3) to the low temperature, low bias conductance of the Au-CdSe heterostructure device displayed in figure 4.6d shows that this proposed mechanism very accurately describes the trend. The fit also determines that $\theta_E = 140\text{K} \pm 3\text{K}$. We note that corrections to the Einstein heat capacity model are generally only significant below $0.1 * \theta_E$ or ~ 14 K in this study, with the Debye T^3 Law only applicable up to a few degrees K, for example.¹⁶ Figure 4.6c shows the low temperature, low bias conductance of the CdSe heterostructure device. The best fit to this data includes a linear temperature dependent term, b , to give:

$$\Omega = \Omega_0 + \alpha C_v + bT = G^{-1} \quad (5)$$

The high accuracy of the fit with this phenomenological correction suggests that a complete description requires consideration of other temperature dependent mechanisms for the CdSe device resistance ($b = 0.01$ T Ω /K). Our analysis cannot distinguish if scattering from the surfactant shell or the semiconducting region contributes to the observed behavior. Future work will examine the role of surface treatments on the magnitude and specific temperature dependence of the trend.

4.6 High Temperature Response

At temperatures above 250 K, we see strong evidence of a transport mechanism dominated by thermally activated charge carriers. Numerous scientific studies have determined that Au contacts to bulk CdSe form Schottky barriers.¹⁷ In the absence of interface states, the ideal barrier height determined by these experiments is 800 meV, the difference of the work function of Au ($\Phi_{m,Au} = 5.38$ eV) and the electron affinity of CdSe ($\chi_{CdSe} = 4.58$ eV).^{13,17} Considering the typical behavior at bulk Au-CdSe interfaces and the contact barriers observed during the low temperature analysis above, our devices likely consist of a rectifying junction at each Au contact. For a particular bias polarity, the higher potential side limits the total current across the device. Indeed, a high temperature conduction mechanism of thermionic emission over a reverse-biased Schottky diode well describes our observed data. This mechanism results from same interface barrier diagramed in Figure 4.2c, with electrons thermally activated over the barrier rather than tunneling through it, but with the inclusion of an image potential at the electrode that raises or lowers the barrier under forward or reverse bias, respectively. The super-linear current-voltage response (fig. 4.2b) results from barrier height lowering with increased bias because of the image force according to

$$I = AA^{**} T^2 \exp\left(\frac{-q\Phi_{BE}}{k_B T}\right) \quad (6)$$

where

$$\Phi_{BE} = \Phi_{Bo} - \sqrt{\frac{qE}{4\pi\epsilon_s}} \quad (7)$$

and

$$E = \sqrt{\frac{2qN_D}{\epsilon_s} \left(V + \Phi_{bi} - \frac{k_B T}{q} \right)} \quad (8)$$

where A is the contact area, A^{**} is the effective Richardson constant, Φ_{BE} is the effective barrier height, Φ_{Bo} is the ideal barrier height in the absence of an image force, E is the maximum electric field at the junction, ϵ_s and N_D are the semiconductor permittivity and doping concentration of CdSe, and Φ_{bi} is the built-in potential.¹³ Importantly, these relations show that $\ln(I)$ is linear with $V^{1/4}$ in the limit of voltage greater than the built-in potential. Also, the slope of an activation energy plot of $\ln(I/T^2)$ versus $1/T$ gives the bias-dependent effective barrier height, Φ_{BE} . This thermionic emission model is only valid at relatively high temperatures where A^{**} and Φ_{BE} are temperature-independent, and other contributions to carrier mobility and concentration are negligible.

The linearity of the $\ln(I)$ versus $V^{1/4}$ plots in figure 4.7a demonstrates the validity of the thermionic emission model description. We emphasize that an extensive examination of many of the other proposed mechanisms for transport in nanoscale semiconductors, including variable range hopping², space-charge-limited¹⁸, Fowler-Nordheim tunneling¹⁵, or single electron tunneling⁶ do not describe the data as accurately as the standard thermionic emission model we propose. However, the devices necessarily deviated from the linear response displayed in Figure 4.7a at decreased temperatures, where the low temperature analysis discussed above is appropriate. It is likely in the high temperature range that the thermally activated carriers, especially at low bias, mask any background tunneling current.¹⁹ The slope of the activation energy plot of $\ln(I/T^2)$ versus $1/T$ for a CdSe device at varying bias (fig. 4.7b) was used to determine the voltage dependence of the effective barrier height, Φ_{BE} . These data are summarized for both device types in figure 4.7c. Here we see clear evidence of the bias-dependent barrier height lowering predicted by the thermionic emission model. Solving equations (7) and (8) for Φ_{BE} gives

$$\Phi_{BE} = \Phi_{Bo} - \sqrt{\frac{q}{4\pi\epsilon_s} \sqrt{\frac{2qN_D}{\epsilon_s} \left(V + \Phi_{bi} - \frac{k_B T}{q} \right)}} \quad (9)$$

The thermal energy, $k_B T$, is small compared to V and Φ_{bi} allowing the simplification²⁰ $\Phi_{bi} = \Phi_{Bo} - k_B T \ln(N_C/N_D) \approx \Phi_{Bo}$ where N_C is the effective conduction band density of states, to give

$$\Phi_{BE} \approx \Phi_{Bo} - \sqrt{\frac{q}{4\pi\epsilon_s} \sqrt{\frac{2qN_D}{\epsilon_s} (V + \Phi_{Bo})}} \quad (10)$$

The least squares fit to equation (10) with Φ_{B_0} as a free parameter is excellent (fig. 4c) obtaining $\Phi_{B_0} = 0.85$ eV and for the CdSe device and $\Phi_{B_0} = 0.21$ eV for the Au-CdSe heterostructure device. These values are in excellent agreement with the low temperature tunneling fitting, where $\Phi_{B_0} = 0.81$ eV and 0.20 eV are obtained for CdSe and Au-CdSe devices respectively.

Recall that Φ_{B_0} is the ideal barrier height, with a predicted value of 800 meV for a bulk Au contact to CdSe free of surface or interface states. The control CdSe devices display a barrier very close to this value, giving good correspondence with the reported behavior at ideal bulk contacts despite that surfactant shell that likely remains on the nanocrystal. However the Au-CdSe heterostructure devices deviate from this value significantly, suggesting that interface structure drastically modifies the electronic environment at the contact. Specifically, our analysis shows a 75% decrease in the Schottky barrier of the Au-CdSe heterostructure device compared to the CdSe control device. Schottky barrier lowering resulting from induced mid gap states is well characterized at bulk Au-CdSe interfaces²¹, giving barrier heights highly dependent on contact structure. Similarly, we attribute the barrier decrease to electronic hybridization or induced mid-gap states at the electrode interface, which accommodate the charge redistribution due to Fermi level equilibration, for lower overall interface polarization. The decreased barrier at the Au-CdSe interface of the heterostructure nanocrystals gives rise to the large conductance enhancement observed for those devices.

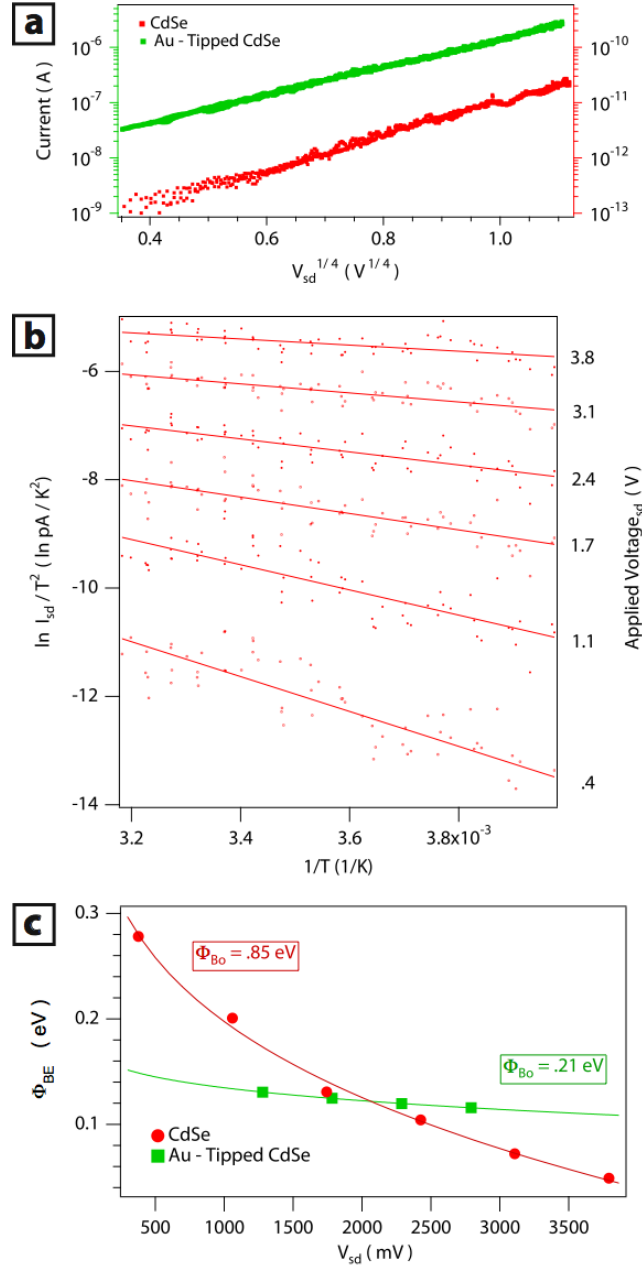


Figure 4.7 (a) Room temperature $\ln(I)$ vs $V^{1/4}$ plot for a CdSe (red) and an Au-CdSe heterostructure (green) device. The linear behavior is consistent with a thermionic emission model and was observed across devices above 250K. (b) Activation energy $\ln(I/I^2)$ vs $1/T$ plot at several bias values for a CdSe device. The fitted slopes (solid traces) give the bias-dependent effective barrier height Φ_{BE} , summarized in (c) for the same CdSe device (red circles) and an Au-CdSe heterostructure device (green squares). The fit in (c) to equation 5 (solid traces) shows the reduced barrier height Φ_{Bo} at the Au-CdSe contact of the heterostructure device.

4.7 Interpreting the Interface Electronic Structure

The fit to the data displayed in figures 4.7b and 4.7c must be considered with care. Our analysis follows from the solution to the Poisson equation conventionally employed to describe bulk semiconductor-metal interfaces.¹³ Although much recent experimental work^{20,22,23} applied this model directly to nanoscale electrical devices, as we have here, theoretical treatments^{3,4} suggest corrections to this picture may be required. In particular, there is little theoretical discussion of the impact of large surface-volume ratios and ligand shells on interfacial charge redistribution, especially for colloidal nanostructures as small as in this study. Indeed, if we assume bulk values for the CdSe semiconductor permittivity, the fit to equation (10) gives the seemingly unphysical prediction of less than one dopant per hybrid Au-CdSe nanocrystal, $N_D = 3.5 \times 10^{17} \text{ cm}^{-3}$. For the CdSe control device in fig. 4, $N_D = 1.3 \times 10^{21} \text{ cm}^{-3}$, a more reasonable carrier concentration. Also note that a factor of 10 larger doping concentration is obtained for the Au-CdSe nanocrystal compared to the low temperature tunneling current fit, while the CdSe nanocrystal dopant concentration is very similar to the low temperature fit. Besides the approximations mentioned above, one possible reason for this discrepancy between fits is that the tunneling formula of Eq.(1) does not consider the image potential. If the image effect were also included in the low temperature model, the fit would determine a lower barrier height, giving a smaller value of N_D . The barrier reduction is more significant in the low barrier case of an Au-CdSe device, thus it has a smaller effect on the fitted dopant concentration at a larger barrier, as in a CdSe control device.

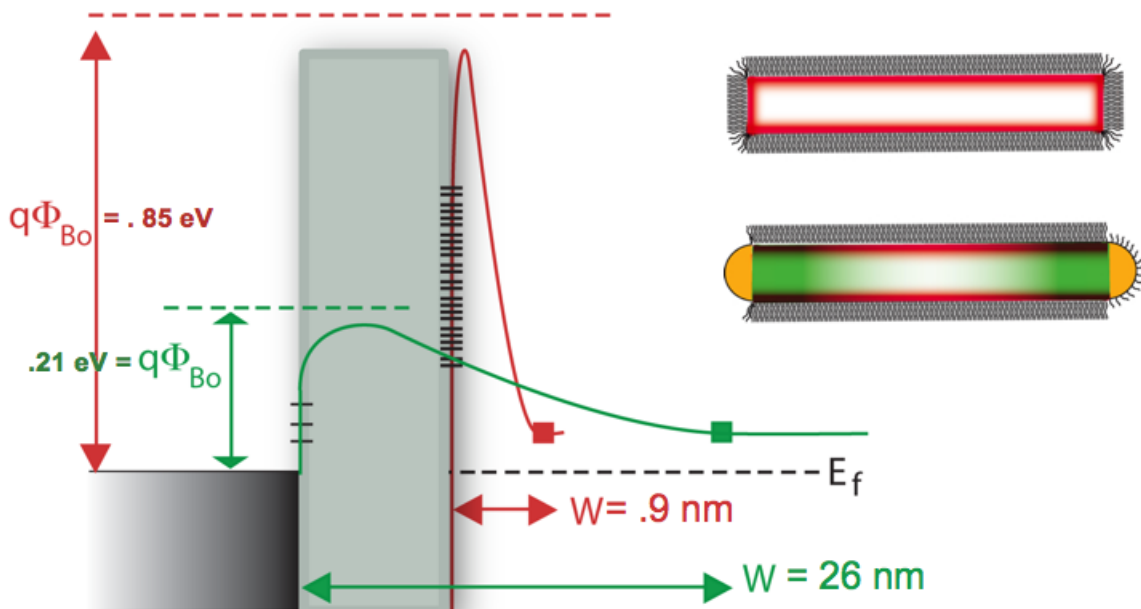


Figure 4.8 Schematic band diagrams comparing electronic structure of CdSe (red) and Au-CdSe (green) samples at the Au electrode contact. Barrier heights are determined directly by the thermionic emission fit. Fits for the depletion width assumes bulk dielectric constants for CdSe. The high and low temperature electronic response of the

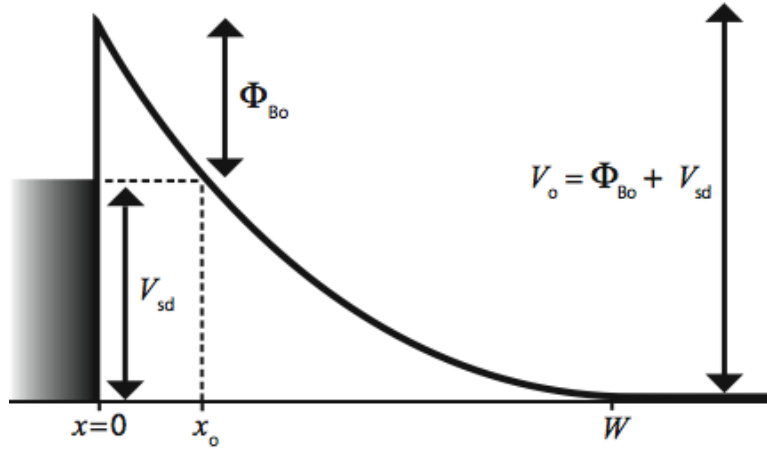
samples suggests a large in-series resistance for the CdSe sample (grey block) and the presence of interface states.

A possible explanation for the apparently low dopant concentration in the Au-CdSe device is that the actual dopants are localized at the surface, not inside the rod as the bulk formula assumes. The de-charging of these dopant sites causes the depletion layer and contributes to the potential barrier lowering. If the dopant sites are located at the surface, and the depletion layer length is similar to the rod diameter, then the ability of de-charging to lower the potential at the center of the rod, where the majority of current flows, is less efficient. Accounting for this would be similar to including a large effective screening constant in the fitting formula, leading to a much larger and more reasonable N_D , or the equivalent surface doping concentration. The fitted depletion length, W , by eq. (S2) gives $W = 7\text{nm}$ for the Au-CdSe device, consistent with this interpretation. The fitted doping concentration for the CdSe device is much larger than for the Au-CdSe device. Here again, it is possible that the device exhibits behavior due to de-charging of the surfactant related surface states at the tip of the rod. These states are directly in the current path, and thus they are very effective for lowering the potential, giving an apparently large N_D . Despite these complications, a key feature of the thermionic emission model fit to determine the barrier height, as in figure 4.7, is that it requires no assumptions about material constants, doping concentration, or other parameters at the complex electrode interface.

In summary, we provide direct measurement of the effect of surfactant on a semiconductor nanocrystal surface and at a metal-semiconductor hybrid interface. We show that the superior performance of Au-tipped heterostructures results from a lower Schottky barrier, and that the synthetic method for tip growth does not alter the chemical composition of the semiconductor. Further, our work demonstrates the increasing sophistication of high quality electrical devices achievable via self-assembly, and verifies this process as an excellent route to the next generation electronic and optoelectronic devices utilizing colloidal nanocrystals.

4.8 Derivation of Low Temperature Model

The procedure follows from the general strategy outlined by Sze, with the barrier structure diagrammed below. Electrons tunnel from left to right under bias.



N_D = doping density
 ϵ_s = semiconductor permittivity
 q = elementary charge
 W = depletion width
 m = effective mass

Poisson's equation defines the potential as a function of distance from the electrode, x , in terms of the voltage across the contact $V_o (=V_{sd}+\Phi_0)$

$$V(x) = \frac{q}{2\epsilon_s} N_D (W - x)^2 \quad (S1)$$

$$\text{where } W = \sqrt{\frac{2\epsilon_s V_o}{qN_D}} \quad (S2)$$

$$\text{and } x_0 = W - \sqrt{\frac{2\epsilon_s}{4\pi q N_D}} V_{sd} \quad (S3)$$

The overall current due to tunneling will be equal to:

$$I_{sd} \propto V_{sd} \cdot e^{-2\Gamma} \quad (S4)$$

where Γ is the tunneling phase factor:

$$\Gamma = \int_0^{x_0} k(x) dx = \int_0^{x_0} \sqrt{\frac{2mq}{\hbar^2} \left[\frac{4\pi q N_D}{2\epsilon_s} (W-x)^2 - V_{sd} \right]} dx \quad (S5)$$

with the definition for the electron wave vector:

$$k(x) = \sqrt{\frac{2mq}{\hbar^2} (V(x) - V_{sd})} \quad (S6)$$

The integral in equation (S5) can be solved by substitution, note that:

$$\int_1^a \sqrt{y^2 - 1} dy = \frac{1}{2} (a\sqrt{a^2 - 1} - b) \text{ where } b = \text{ArcCosh}(a) \quad (S7)$$

$$\text{then } \Gamma = \sqrt{\frac{4m\epsilon_s V_{sd}^2}{4\pi\hbar^2 N_D}} \int_1^{\sqrt{V_0/V_{sd}}} \sqrt{y^2 - 1} dy \quad (S8)$$

$$\text{giving } \Gamma = \sqrt{\frac{m\epsilon_s}{\hbar^2 N_D}} \cdot \left[\sqrt{(V_{sd} + \Phi_0) \cdot \Phi_0} - V_{sd} \cdot \text{ArcCosh} \left(\sqrt{\frac{V_0}{V_{sd}}} \right) \right] \quad (S9)$$

Substitution of equation (S9) for Γ into equation (S4) reproduces the expression for the tunneling current, equation (1), in Section 4.5 above.

4.9 Chapter 4 Bibliography

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Chapter 5. “Bottom-Up” Devices

Trends in Single Nanocrystal Device Transport

Results in Chapter 4 demonstrated the advantage of self-assembled heterostructure nanoparticles for use in electrical devices. Here we provide more insight into the general applicability of metal-semiconductor nanoparticle heterostructures. We also consider other post-synthesis modifications to nanocrystals, via solution phase cation exchange, to access new semiconductor materials and construct single particle semiconductor-semiconductor interfaces. Preliminary experiments suggest these modifications may provide synergistic electronic and optoelectronic functionality in single nanoparticles.

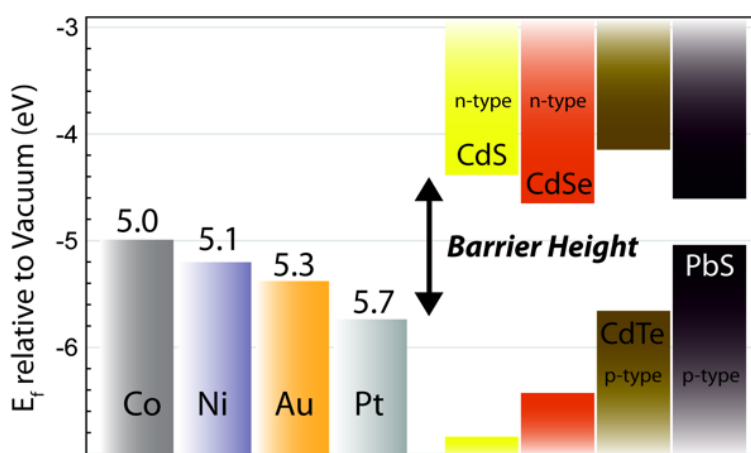


Figure 5.1 Bulk Fermi level (E_f) diagram of metal and semiconductor materials currently amenable to the tipping procedure. The offset between the metal Fermi level and majority carrier band determines the ideal barrier height expected across the nanocrystal-electrode interface.

5.1 Metal-Semiconductor Nanocrystal Heterostructures

The first reported metal-semiconductor nanorod heterostructure synthesis optimized the growth of Au on CdSe nanorods and demonstrated many variations of the basic morphology.¹ The original procedure dissolves metal salt (AuCl_3) and gentle reducers and surfactants (dodecylamine and dodecylammonium bromide), into a room-temperature μM solution of CdSe nanorods dissolved in toluene. Within minutes, metal will form on both nanocrystal ends. Nanorods in solution for longer, on the order of hours, will exhibit a single-sided metallic tip. It is believed that Ostwald ripening

mediates the transition from double-sided to single-sided Au tips.² Increase in precursor concentration will cause non-local deposition of Au along the entire nanorod surface, rather than increased size of the metal tip. However, more recent experiments show that the size of the Au tip can be increased to arbitrarily large size if Au is reduced via a photo-mediated process with nanorods present.^{3,4}

Currently, the mechanism of Au deposition is not fully understood. Evidence for nanoparticle etching during metal growth and inductively coupled plasma atomic emission spectroscopy (ICP-AES) elemental analysis of the residual growth solution suggest that Au(III) reduces to Au(0) through the oxidation of Se²⁻.^{1,5} However, the mechanism may depend crucially on the size-dependent redox power of nanoscale materials.⁵ The Au likely deposits preferentially on the nanorod tips because these are the nanocrystal facets with highest surface energy, based on studies of anisotropic nanorod formation.^{6,7}

Despite many unanswered questions regarding the specific mechanism of Au-tipping, the basic procedure has been extended to a variety of semiconductor nanorod substrates and metals. To date, metal tips of Au, Pt, Co, Ni and alloys of these metals have been deposited from solution onto nanocrystals, with active research exploring more metal precursors and alternative procedures like galvanic exchange, for example, to increase the variety of metals that may be utilized.^{3-5, 8-12} Demonstrated semiconductor substrates include CdS, CdSe, and CdTe with a variety of anisotropic and isotropic nanocrystal morphologies. For all materials, metal deposition is initially facet selective. Combined with methods for chemical transformation of the semiconductor material (see section 5.2), many semiconductor-metal heterostructures may be possible.

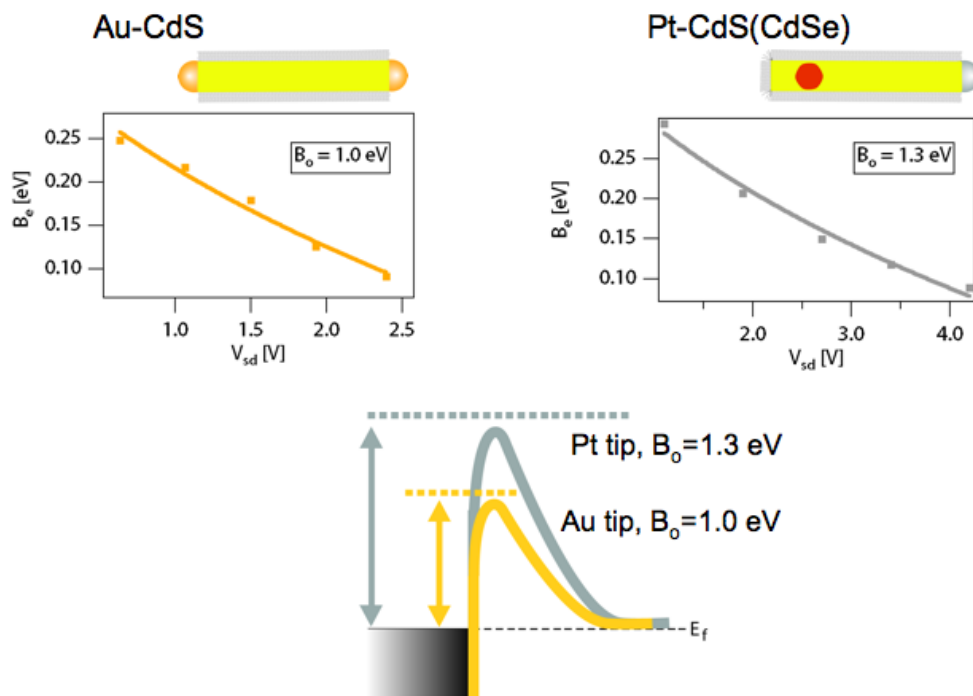


Figure 5.2 Electrical responses of CdS heterostructures. The schematic barrier diagram (bottom) summarizes the barrier fits according to the thermionic emission model (top), as described in Chapter 4. CdS heterostructures maintain barrier heights very close to the ideal Fermi level offset.

We consider metal-semiconductor heterostructures that may be optimal for photovoltaic and photocatalytic applications. Bulk CdS exhibits a peak absorption very close to the peak intensity in the solar spectrum, at 2.42 eV. Recent work in our lab⁸ demonstrated that heterostructures of CdS nanorods with an embedded CdSe dot core and a Pt tip (see Figure 5.2) in water solution show high efficiency for H₂ evolution, with an apparent quantum yield near 20% under solar flux. In these structures, holes are confined to the CdSe core while electrons are delocalized, reducing H⁺ when transferred to the Pt tip. Because the core size, rod length, and tip metal can all be tuned via synthetic strategies, there is strong interest to optimize the transfer of electrons to the metal tip, while minimizing recombination of photo-generated electron-hole pairs. Current work explores further modifications to the heterostructures that may allow O₂ evolution as well.

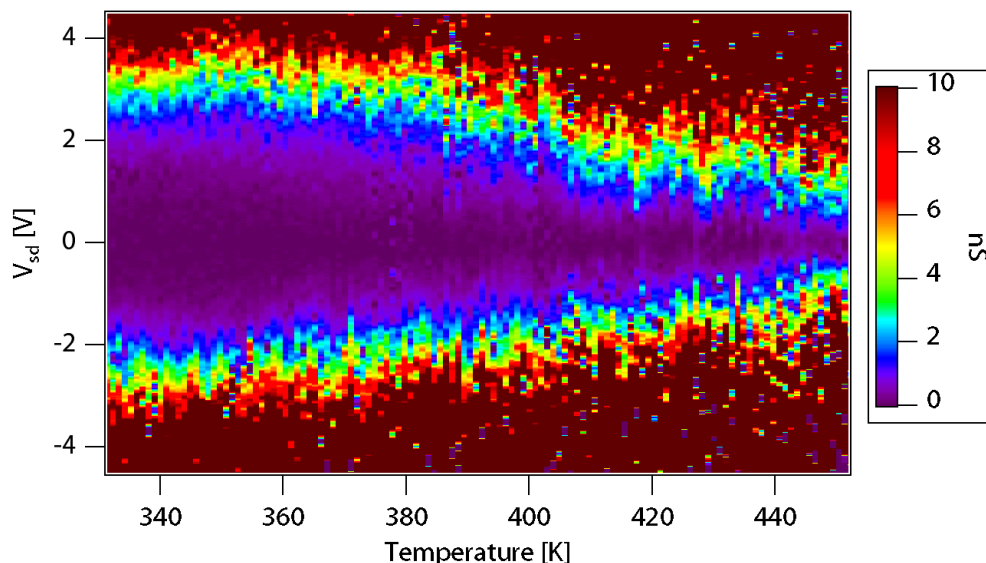


Figure 5.3 Temperature dependence of differential conductance across a CdS-Pt heterostructure nanoparticle. The increase in conductance with increasing temperature is consistent with thermionic emission across a Schottky barrier, allowing determination of the barrier height as described in Chapter 4. The fit is displayed in Figure 5.2.

We employ the same methodology outlined in Chapter 4 to directly measure the barrier height between the CdS rod and the Pt tip, to better understand the electronic structure of these nanocrystal heterostructure photocatalysts. Figure 5.3 shows the temperature-dependent current response of a single Pt-tip heterostructure nanoparticle. The increasing current with increasing temperature fits well with a model of thermionic emission over a Schottky barrier at the metal-semiconductor interface. The fitted barrier height of 1.3 eV is very close to the predicted value, based on the Fermi level offset of CdS and Pt (Figure 5.1).

However, in a device geometry the Pt tip is shorted to the source and drain electrodes, allowing the metal to maintain neutrality while the semiconductor Fermi level adjusts to equilibrate to the electrodes. This equilibration process is distinct from the situation of a nanocrystal heterostructure decoupled from electrode leads, such as when the nanocrystals are dissolved in a water solution. In this second scenario, the limited capacity of the nanoscale Pt tip to hold excess electrons will alter the equilibration of the Fermi level across the metal-semiconductor interface. Specifically, we can consider the Schottky barrier measured in a single Pt-tip heterostructure nanocrystal device, as above, and compare that with the single electron charging effects discussed in Chapter 2 and Chapter 3 to analyze how charge transfer events across the interface alter the overall heterostructure equilibration of a free particle. Figure 5.4 cartoons the interface equilibration process of a CdS-Pt heterostructure decoupled from electrode leads. Here, the increase of the Fermi-level of the Pt-tip with each single electron transferred from the CdS results in a net lower interface barrier. A lower barrier may help explain the high efficiency for H₂ evolution from these materials. Ongoing studies employ optical techniques to measure the Pt-CdS barrier in single heterostructure particles decoupled from electrode leads.

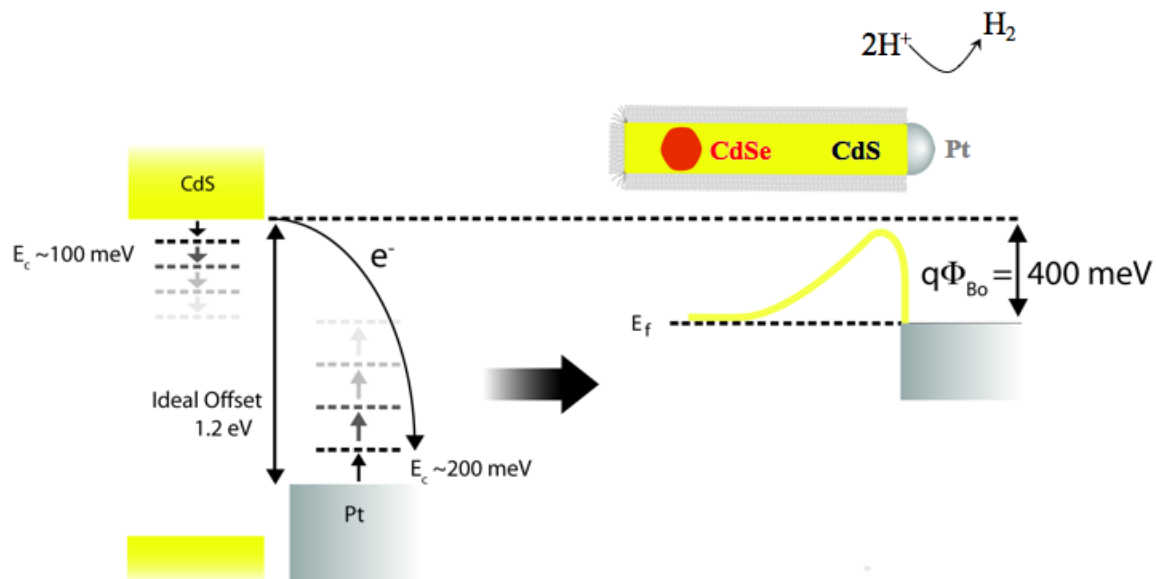


Figure 5.4 Cartooned equilibration process of a CdS-Pt heterostructure particle decoupled from electrode leads. The increase of the Fermi Level of the Pt-tip with each transferred electron predicts a lower Schottky barrier at the metal-semiconductor interface of free heterostructure particles compared to those in device geometries, as in Figure 5.2 and 5.3.

As summarized in Figure 5.2, electrical characterization utilizing the methodology described in Chapter 4 shows that CdS nanorods with Au tips or Pt tips maintain the ideal interface barrier height predicted by the difference in the respective metal-semiconductor Fermi levels (see Figure 5.1). This trend is contrary to the observed behavior of Au-CdSe heterostructures, which showed significant barrier lowering for the solution deposited Au. This difference suggests a lack of any mid-gap states at the metal-CdS interface formed during growth, which would lower the interface Schottky barrier. Better understanding of the tipping procedure may elucidate the relevant difference in interface structure for the Au-CdSe versus the Au-CdS particles, and it ultimately may allow controlled synthetic tuning of the interface barrier, based on growth conditions.

5.2 Cation Exchange for Nanocrystal Heterostructures

Cation exchange is a facile method for replacing the cations in a semiconductor nanoparticle while maintaining the anionic lattice and the overall nanoparticle morphology. The process had been described in detail elsewhere,¹³⁻¹⁵ and the general procedure is similar to the process for metal tipping described above. Comparable working conditions and metal salt concentrations are employed, though no additional reducing agent is added with the metal salt that may cause its reduction to elemental metal. Rather, the metal salt cation displaces the native cation in the lattice of the starting nanocrystal at a stoichiometric ratio. Thus, by carefully controlling the concentration of nanoparticles in solution and the concentration of added metal salt, it is even possible to partially exchange a single nanocrystal. This strategy provides a semiconductor

heterojunction within a single nanocrystal, allowing for a single nanocrystal p-n junction, for example, which may efficiently split photogenerated excitons at the single nanocrystal level.^{13,14}

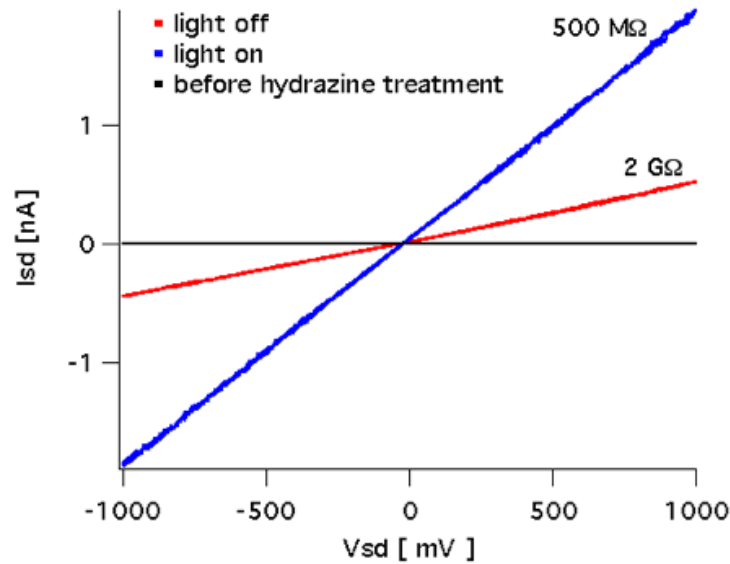


Figure 5.5 Photoresponse of a single PbS nanocrystal device.

We have used the technique to produce nanorods of the Pb chalcogenide family from nanorods of CdS, CdSe, or CdTe for electrical characterization using the methodology in Chapter 4. In particular, Pb chalcogenide nanocrystals are interesting materials for PV applications, because numerous studies report increased efficiency for multiple exciton generation from absorption of single photons with energy larger than the nanocrystal band gap.^{16,17} If such multiple carriers could be exploited in an electrical circuit, Pb chalcogenide nanocrystals would be excellent candidates for the active components in next generation solar cells. Much research on nanocrystal thin film solids hopes to optimize Pb chalcogenide nanocrystal specifically for this goal.^{17,18}

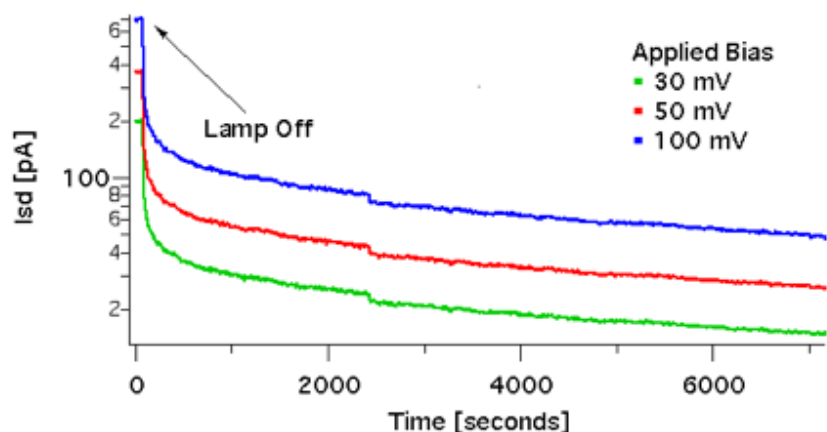


Figure 5.6 Relaxation of photogenerated carriers in a single PbS nanocrystal device. The long decay suggests traps states in the nanocrystal.

Single particle electrical studies are ongoing, but initial data show a strong photoresponse in the electrical signal from single PbS nanorod (Figure 5.5). Borrowing surface treatment strategies from ensemble studies, the best signal results from nanorods that have been rinsed with a 1 μM solution of hydrazine in acetonitrile.¹⁸ The time evolution of the photoresponse also shows a decay characteristic of the lifetime of trap states in the nanocrystal (Figure 5.6). Future work will examine the time dependence of the photo signal and the full spectral response, seeking enhancements that may be due to multiple carrier generation.







	Material	Treatment	Resistance	Comment
	CdS	none	> 10 T Ω	current below detection limit
	CdS	Hydrazine, surfactant free	100's G Ω	on Au electrodes, similar to Au tips
	Pt-CdS(CdSe)	oleylamine, Pt-acetylacetonate	0.1-10 T Ω $B_0 = 1.3$ eV	robust to tipping procedure
	Au-CdS	MeOH, DDA, AuCl	0.1-100 T Ω $B_0 = 1.0$ eV	robust to tipping procedure
	Au-CdSe	MeOH, DDA, AuCl	10 M Ω -100 G Ω $B_0 = 1.0$ eV	strongly etched by tipping procedure
	PbS, PbSe, PbTe	Hydrazine, surfactant free	M Ω 's, ohmic-like transport	dissolved during tipping, large photoresponse

Figure 5.7 Trends in single nanocrystal device transport. The stability of particles during the tipping procedure is correlated with ideal barrier heights in the finished device.

5.3 Chapter 5 Bibliography

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