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Charge Noise and Dephasing in Silicon-Based Lateral Quantum Dots

A dissertation submitted in partial satisfaction
of the requirements for the degree
Doctor of Philosophy in Physics

by

Blake Michael Freeman

2017

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2017

ABSTRACT OF THE DISSERTATION

Charge Noise and Dephasing in Silicon-Based Lateral Quantum Dots

by

Blake Michael Freeman
Doctor of Philosophy in Physics
University of California, Los Angeles, 2017
Professor Hong-Wen Jiang, Chair

Quantum computing has become a thriving field over the past several decades. Although many candidate systems exist, this dissertation will focus on quantum dots as a quantum computing implementation, specifically lateral quantum dots in silicon based heterostructures. Lateral quantum dots use trapped electrons in semiconducting heterostructures to form qubits, the basic building block of a quantum computer. There are several potential qubit implementations using quantum dots and new qubit schemes, such as the valley qubit presented in Chapter 4, are still being investigated. Many of these implementations have already been successfully demonstrated. In this sense, research into quantum dots is a maturing field, having successfully demonstrated proof of concept for multiple qubit implementations. If quantum dots are to succeed as a quantum computing platform research needs to focus on improving the qubits themselves. Decoherence and dephasing need to be improved, but also yield and reproducibility. In this work I describe experiments intended to help understand and improve the performance of lateral quantum dots. I fabricated multiple lithographically identical devices on Si/SiO_2 and Si/SiGe heterostructures to com-

pare charge noise on the two Silicon based substrates. I describe the first conclusive observation and characterization of a valley based qubit. The noise characteristics of the valley qubit are particularly attractive as it's operation is resistant to charge noise, the primary source of noise in Silicon based qubits. Finally I present the on-going development of a novel gate architecture for lateral quantum dots. Called a hybrid architecture, this design possesses good tunability along with simple fabrication and a reduced number of total gates relative to other leading architectures; this has the potential to dramatically improve yield and scalability.

The dissertation of Blake Michael Freeman is approved.

Ya-Hong Xie

Stuart Brown

Hong-Wen Jiang, Committee Chair

University of California, Los Angeles

2017

For my parents, Mark and Joan.

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VITA

2012–2017	Graduate Researcher University of California Los Angeles Advisor: HongWen Jiang
2016–2017	Dissertation Year Fellowship
2011–2012	Teaching Assistant University of California Los Angeles
2011–2012	Robert Finkelstein Graduate Fellowship
2011	B.S. in Physics, B.A. in Mathematics University of Washington
2009–2011	Undergraduate Researcher University of Washington Advisor: Christopher Wrede

PUBLICATIONS

J.S. Schoenfield, B.M. Freeman, H.W. Jiang. (2017) *Coherent Manipulation of Valley States at Multiple Charge Configurations of a Silicon Quantum Dot Device.* Nature Communications **8**, 64.

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CHAPTER 1

Introduction

1.1 Background

Understanding quantum mechanics has driven an extraordinary amount of technological progress throughout the 20th century. From the theory of the photo-electric effect in 1905[Ein05] to Bloch's development of a quantum theory of solids in the late 1920s[Blo29] and perhaps most importantly the development of the solid-state transistor at Bell labs in 1947[Bra47], it was a time of enormous breakthroughs in physics that shifted our understanding of the natural world. Even more than the atomic bomb, it was the theory and development of semiconductors that shaped society in the 20th century.

During the 1940s and 50s, basic digital computers using vacuum tube logic circuitry had been developed and digital computing was already a growing field[TBJ13]. With development of the, far less bulky semiconductor based, transistor in 1947 its application in the development of digital computers was immediately clear. A chain reaction began; the development of digital computers opened up new possibilities, allowing for physical calculations and simulations that had previously been impractical or impossible. This in turn spurred development in our understanding of semiconductor physics and in our ability to design better computers, a cycle that sent us

hurtling towards microprocessors with over 10 million transistors by the end of the century. Progress shows little sign of stopping, as of the writing of this dissertation microprocessors with transistor counts nearing 10 billion are available for home use. In fact, there is a good chance that in your pocket right now is a microprocessor with billions of times more computing power than the supercomputers of the 1950s and 1960s.

Progress is slowing somewhat however, and as transistors begin to reach nanometer scales, new physics and engineering hurtles are expected to come in to play, dramatically slowing the advancement of conventional computing power by the mid 2020s [Wal16]. Nevertheless, we may only be scratching the surface of the computing power quantum mechanics has to offer us. Beginning in the 1980s, the concept of a quantum computer was first proposed and research followed suit[Ben80, Fey82]. Conventional computers are quantum in the sense that they rely on our understanding of semiconducting band gaps, an emergent and robust quantum phenomenon. A quantum computer on the other hand relies on more fundamental quantum properties like quantization, entanglement and superposition. These properties are delicate and easily disturbed by their environment. Hence most qubit systems are best observed at low temperatures in well isolated systems. This presents many technical challenges, but success would allow for quantum computers that perform many algorithms impractical for a conventional computer. If the 20th century was the century of the digital computer, then perhaps the 21st century will prove to be the century of the quantum computer.

1.2 Quantum Computing

The theoretical side of quantum computation is already a well-developed field, most of which is beyond the scope of this dissertation. Several useful algorithms have been developed which could run faster on a quantum computer than conventional computers. The most famous, Shor's algorithm, would allow for fast prime factorization of large numbers [Sho97]. The effective implementation of Shor's algorithm would break most modern encryption schemes, as they rely on the inability of conventional computers to quickly factor large numbers. Perhaps more enticing to the reader, who is likely a student of quantum mechanics, is quantum computations promise of effectively modeling complicated quantum systems[Sim94].

Quantum computing's theoretical underpinnings rely on the concept of the quantum bit or qubit, as it is often called. In the development of quantum algorithms a qubit is treated abstractly as an idealized quantum two level system (TLS). Unlike a conventional bit with two states 0 and 1, a qubit spans a super position of the quantum states $|0\rangle$ and $|1\rangle$ in a sense providing for an infinite number of states. The qubits state, $|\Psi\rangle$, can be written

$$|\Psi\rangle = \alpha |0\rangle + \beta |1\rangle , \tag{1.1}$$

where α and β are complex numbers with the restriction that $\alpha^2 + \beta^2 = 1$. In addition to superposition, multiple qubits can be entangle to produce states of the form $|\Psi\rangle = \alpha |0\rangle_1 |1\rangle_2 + \beta |1\rangle_1 |0\rangle_2 + \gamma |0\rangle_1 |0\rangle_2 + \beta |1\rangle_1 |1\rangle_2$. Here $|N\rangle_M$ represents state qubit M in a state N. Entangled qubits have no definite state of their own, and quantum mechanics is fundamentally required to describe them as no classical analogue exists.

While all of this may seem tantalizing, it is important to acknowledge that quantum computing, particularly in terms of practical implementation is a nascent field. There are still many technological hurtles to overcome before quantum computers begin performing useful calculations. One challenge that I will discuss in detail is coherence. Qubits must remain in a coherent state for the duration of any calculation performed. At first glance, the fact that even the longest lived implementations of quantum computing are currently producing coherence times on the order of us or ms may make it seem impossible[ZDM13]. Fortunately, there is a solution: quantum error correction codes. The use of gate implemented quantum error correction codes could in principle allow for a quantum state to be maintained forever[BDS96, KLV00]. This does however depend on the nature of the errors occurring. More importantly, before these codes can be implemented effectively a threshold of about 10^4 qubit operations per error must be reached. So far this has not been demonstrated in any physical system, and reaching this limit is a major goal of experimental research on the many candidate systems currently being investigated.

Following coherence, scalability is another problem. Some of the earliest research on quantum computing was in liquid state NMR systems, as well as on trapped ions[VSB01]. Much like early vacuum tube computers these systems suffer from poor scalability. While there have been several recent proposals regarding ways to scale up trapped ion systems effectively, these solutions are not simple. With respect to scalability, solid-state implementations of quantum computing have good potential, especially quantum dot systems discussed in this thesis. Fabrication of lateral quantum dots relies on the same lithographic tools and methods developed and perfected over the last several decades in the semiconductor industry. These tools are capable of routinely patterning nm scale designs. This means success in

developing smaller systems could lead to a relatively fast and practical scale up on this platform. Despite this advantage, solid-state systems do come with their own problems, particularly in terms of coherence. After all, solid state quantum computers need to control a single element of an enormously complicated system; isolating this part while simultaneously allowing for precision control is no small task.

Finally, transmission of quantum information is another developing field that will be critical for the long term success of quantum computing. The ability to transmit quantum state information coherently within a system or across large distances between systems poses a problem. Entanglement with photons presents a possible solution. Following entanglement with a qubit system photons can subsequently be transmitted coherently over kilometers or more in waveguides[Mat12]. Entangling quantum systems such as quantum dots or super conducting qubits is a growing field, which has already seem some success by placing qubit systems in electromagnetic resonators[ZDM13].

1.3 Qubits

A good physical qubit should behave as much as possible like an ideal quantum two level system (TLS), and allow for full control of the qubit state. Unfortunately these two properties are at odds as any system that allows for good control of a qubit's state by its nature will introduce noise into the qubit system via its control systems. The best solution is to strike a good balance, and several candidate systems are currently being investigated towards this end.

Currently researched solid state qubit systems generally rely on isolating and controlling a nuclear spin, an electron spin or a superconducting circuit containing

a Josephson junction. This dissertation will focus on the control of electrons within semiconductor based quantum dots. Single qubits have been implemented in a variety of ways using electrons in quantum dots. For the following discussion a quantum dot can be simply defined as a potential well capable of confining an electron on the order of its deBroglie wavelength. Before discussing the most common types of quantum dot based qubits, I will first discuss the Bloch sphere as it will be used repeatedly as a means to visualize single qubit systems throughout this dissertation.

1.3.1 Bloch Sphere

We saw previously that a qubit state can be written, $|\Psi\rangle = \alpha|0\rangle + \beta|1\rangle$, with $\alpha^2 + \beta^2 = 1$. It is useful to represent the qubit state as a point on a sphere of radius 1, a representation referred to as a *Bloch sphere*. Using standard spherical coordinates θ and ϕ we can rewrite our qubit state as follows,

$$|\Psi\rangle = \cos(\theta/2)|0\rangle + e^{i\phi}\sin(\theta/2)|1\rangle . \tag{1.2}$$

Using this representation, the computational basis states $|0\rangle$ and $|1\rangle$ lie along the $+\hat{z}$ and $-\hat{z}$ axes respectively. By plugging in $\theta = \pi/2$ we can work out the states lying along the x and y axes, which correspond to the eigenstates of the Pauli operators σ_x and σ_y. All together, the Pauli matrices can be thought of as x, y and z operators,

$$\sigma_x = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix}, \sigma_y = \begin{bmatrix} 0 & -i \\ i & 0 \end{bmatrix}, \sigma_z = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix}. \tag{1.3}$$

Using the Bloch sphere representation we can visualize the state of a qubit

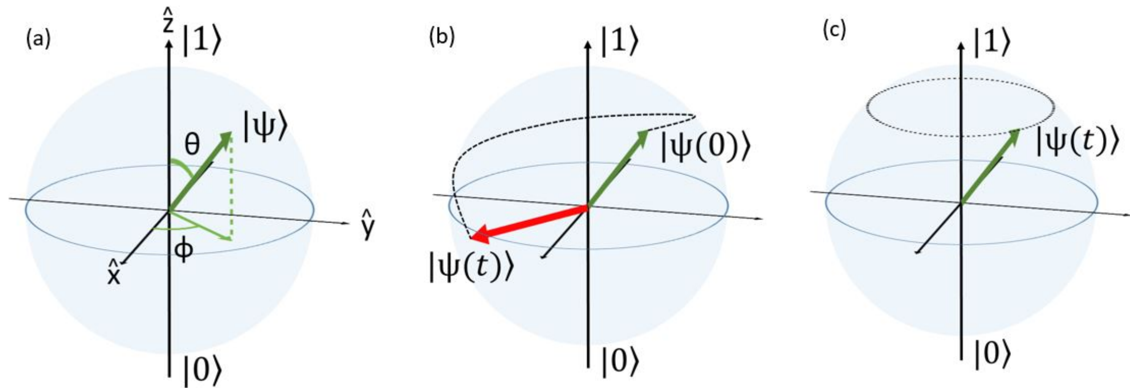

Figure 1.1: (a) A wave function rewritten in the form of Eq. 1.2 can be simply visualized on the unit sphere using the spherical coordinates θ and ϕ. This representation is called the Bloch sphere. Note that the basis states $|0\rangle$ and $|1\rangle$ are generally taken to lie along the $\hat{z}$ axis. (b) Given an initial state $|\psi(0)\rangle$, time evolution of $|\psi(t)\rangle$ is governed by the states Hamiltonian $H(t)$. As time passes, the state will trace out a path along the surface of the Bloch sphere. (c) In the case that the Hamiltonian is time independent and $|0\rangle$ and $|1\rangle$ represent eigenstates of the Hamiltonian, $|\psi(t)\rangle$ will precess around the $\hat{z}$ axis and trace out a continuous circle on the Bloch sphere.

throughout its evolution by tracing a continuous line on the surface of the Bloch sphere as seen in Figure 1.1. For a given initial state, the time evolution of our qubit is governed by the time dependent Schrodinger equation, $i\hbar\frac{d|\Psi\rangle}{dt} = H(t)|\Psi\rangle$, where $H(t)$ is the system's Hamiltonian. It is the time dependence of the Hamiltonian that holds the key to qubit manipulation. By switching terms of a qubit's Hamiltonian on and off, the qubit can be rotated from one state to another as desired. To a degree all physical qubit schemes can be defined by the type of Hamiltonian terms one can manipulate along with a measurement scheme. To gain some intuition regarding the time evolution of qubits we first consider the simplest case of a time independent Hamiltonian. In this case the qubit state as a function of time is $|\Psi(t)\rangle = e^{-i\hat{H}t/\hbar}|\Psi(0)\rangle$, which can be rewritten,

$$|\Psi(t)\rangle = (\cos(|\vec{n}|t/\hbar)\hat{I} - i\sin(|\vec{n}|t/\hbar)(n_x\sigma_x + n_y\sigma_y + n_z\sigma_z)/|\vec{n}|)\,|\Psi(0)\rangle\,. \qquad (1.4)$$

Here the vector $\vec{n}$ is given by the projection of the Hamiltonian onto the Pauli matrices given by $n_i = Tr[\hat{H}\sigma_i]/2$. Examination of Eq. 1.4 shows that the state of the system rotates about the axis given by $\vec{n}$ at a rate proportional to its magnitude. By writing qubit Hamiltonians using Pauli matrices we can often quickly intuit how particular rotations are meant to happen. Any physical system serving as a qubit will need two axis control, meaning the Hamiltonian as a function of time will need components comprising at a minimum two Pauli matrices.

Following the qubit's manipulation, the state of the qubit will need to be read out. Given the nature of quantum mechanics readout is at best a predictive measurement. This measurement is generally accomplished by a projective measurement onto one of two orthogonal basis states, $|0'\rangle$ and $|1'\rangle$ that may or may not coincide with the

operation basis $|0\rangle$ and $|1\rangle$. Each individual measurement will then return $|0'\rangle$ or $|1'\rangle$ with probability $P_{0'} = |\langle 0'|\Psi\rangle|^2$ and $P_{1'} = |\langle 1'|\Psi\rangle|^2$ respectively. To learn the final state of the qubit repeated measurements will reveal these probabilities and thus the magnitudes of α' and β' the state's coefficients in the measurement basis. Interestingly though, it will reveal nothing of their relative phase which may be extracted through more detailed measurements involving either additional rotations or measurement bases.

Performing any calculation using a quantum computer will rely on many repeated measurements of an identically prepared qubit. This produces an ensemble that lends itself well to a density matrix representation. Using a density matrix approach will allow us to visualize decoherence and dephasing. In this picture the ensemble is described by a density matrix ρ, which, when written in the form,

$$\rho = \frac{1}{2}(\hat{I} + \vec{b} \cdot \vec{\sigma}). \tag{1.5}$$

Here $\vec{b}$ is the Bloch vector, which for a pure state is simply the vector coordinates of the system's state on the Bloch sphere. If the ensemble represents a mixed state, however, $\vec{b}$ no longer lies on the Bloch sphere but within it, i.e. $|\vec{b}| < 1$. Using the Bloch sphere to visualize mixed states will come in useful when we are discussing dephasing; the length of the vector $\vec{b}$ will decay as the system loses coherence.

1.3.2 Spin Qubits

Perhaps the simplest and most studied qubit scheme using a trapped electron is the spin qubit [ZDM13, HPT07]. The spin qubit uses the intrinsic spin-1/2 of the electron, which has two eigenstates, as the qubit TLS. Generally in this implementation

an electron is trapped in a quantum dot to use as a qubit. The qubit is placed in a large constant $\vec{B}$ field which we can take to be in the $\hat{z}$ direction. Two axis control of the qubit is implemented via an oscillating magnetic field in the $\hat{x}$ direction from a nearby RF resonator. The Hamiltonian then takes the form,

$$\hat{H}(t) = \hbar\gamma/2(B_0\sigma_z + B_1\cos(\omega t + \phi)\sigma_x), \tag{1.6}$$

where γ is the gyromagnetic ratio of the qubit. This system shares many properties with traditional NMR spin systems, which are often examined in the rotating frame. When the precession rate of the state around the $\hat{z}$ axis due to the fixed $\hat{z}$ field is equal to the frequency ω the system is said to be on resonance. When examined in a frame rotating at frequency ω the system has a fixed field B_1 in the x-y plane allowing for two axis control.

While the simple physics associated with spin qubits is appealing they are not generally considered a leading qubit candidate. As spin qubits require fabrication of a resonantor and an experimental setup with a large fixed magnetic field they present additional technical challenges. Multi qubit systems consisting of single spins may also struggle to address qubits individually. Still, measurements of single electron spins in quantum dot systems provide a valuable tool for understanding and characterizing potential semiconductor based quantum dot systems.

1.3.3 Charge Qubits

The charge qubit uses a single electron in a double quantum dot system, which can simply be thought of as a double well potential containing a single particle. Instead of using the electrons spin to form an operational basis a charge qubit uses the location

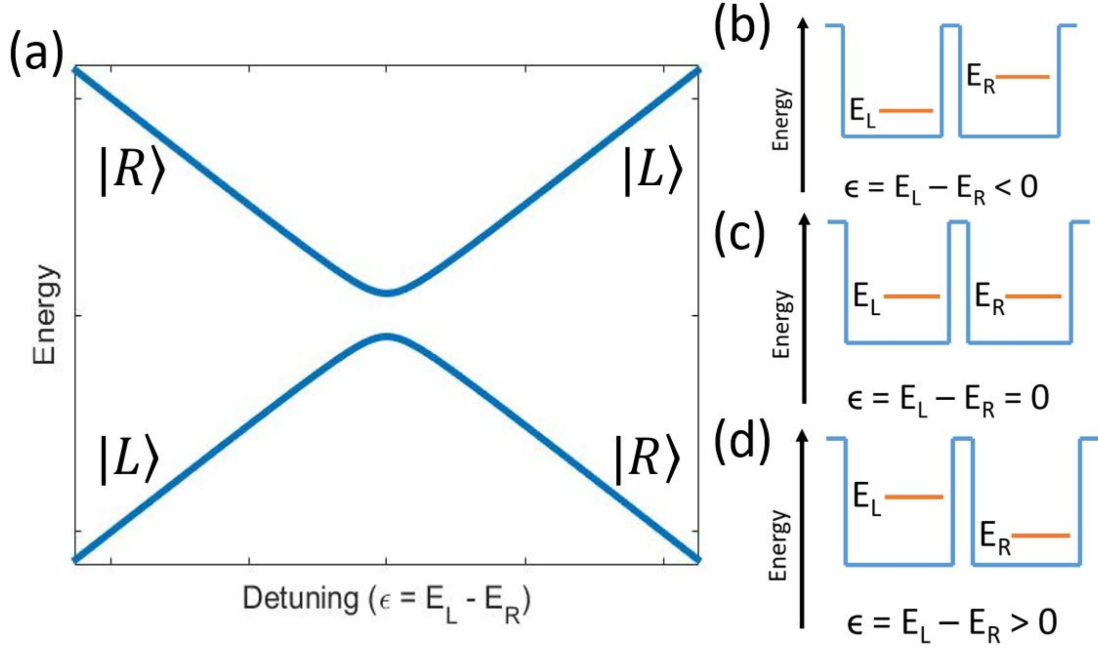

Figure 1.2: (a) Energy dispersion as a function of detuning (ϵ) for a simple 2-state charge qubit system given by Eq. 1.7, the anticrossing gap at $\epsilon = 0$ is equal to 2Δ. Also shown are qualitative representations of the energy of levels in the system given that (b) $\epsilon < 0$, (c) $\epsilon = 0$ and (d) $\epsilon > 0$.

of the electron $|L\rangle$ or $|R\rangle$ for the left and right dot respectively. Many quantum dot qubit schemes are described using a detuning parameter ϵ, which represents the difference in energy between the states $|L\rangle$ and $|R\rangle$. The following chapter will discuss the physical properties of quantum dots in more detail, but in general ϵ is a parameter that is simple to control. The charge qubit Hamiltonian takes the form,

$$\hat{H}(t) = \epsilon(t)\sigma_z + \Delta\sigma_x. \tag{1.7}$$

Here Δ is the coupling between the two dots. This coupling is tunable in most quantum dot systems, but will be considered fixed for the purposes of charge qubit operation. Figure 1.2 shows the dispersion relation for a charge qubit as a function of detuning, ϵ. Charge qubit control is best intuitively understood in terms of the adiabatic theorem, which tells us that if we change the Hamiltonian fast enough (diabatically), the systems state will remain unchanged while a slow (adiabatic) transition will keep the system in the ground state regardless of that state's superposition in terms of $|L\rangle$ and $|R\rangle$. Consider a charge qubit at a large negative epsilon, here the ground state in the energy basis, $|E_0\rangle \simeq |L\rangle$. If the system begins with $|\Psi\rangle = |L\rangle$ at negative epsilon then raising epsilon to a large positive value will result in a θ rotation on the Bloch sphere the size of which is determined by the rate of change in epsilon $\frac{\partial \epsilon}{\partial t}$. The extreme cases of this rotation are: $\theta = 0$, an immediate diabatic transition, and $\theta = \pi$, a slow adiabatic transition. The charge qubit then has two axis control, using passages through $\epsilon = 0$ for θ rotations and time spent at $\epsilon >> 0$ for rotations about the $\hat{z}$ axis. Figure 1.3 shows the system's energy dispersion along with a sample qubit manipulation.

Charge qubits have been successfully controlled and characterized in various substrates[ZDM13, PPL10, CLT13]. Charge qubits have value as an experimental tool, but much like single spin qubits are not expected to provide a useful qubit for quantum computing. As discussed later, fluctuations in electric fields in the environment surrounding the qubit are referred to as charge noise. Charge noise is the primary source of decoherence for most quantum dot based qubits[ZDM13]. As charge qubits are particularly susceptible to these fluctuations they tend to have short coherence times unsuitable for computing qubits.

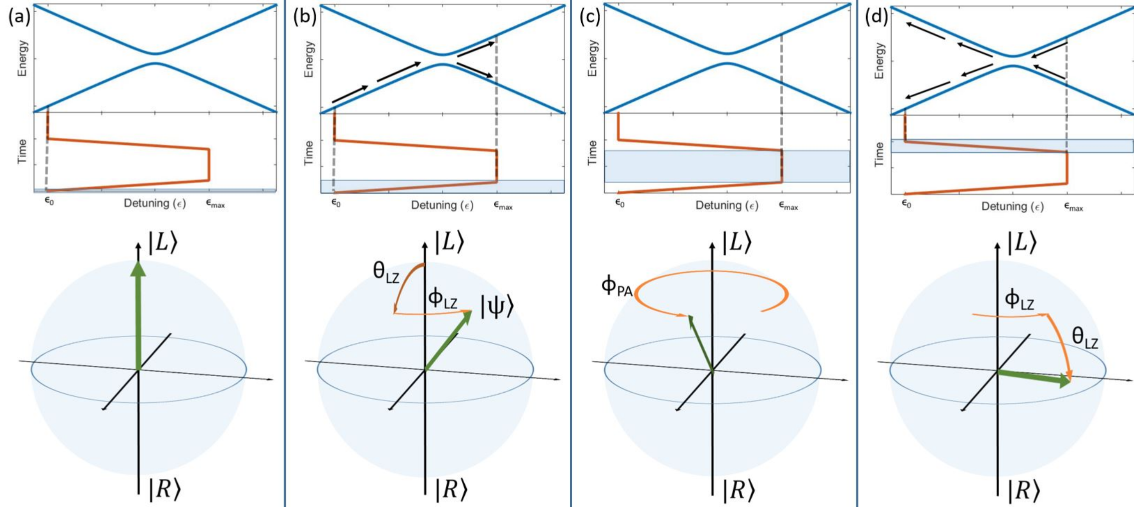

Figure 1.3: In this figure each frame depicts part of the process of basic charge qubit operation. The top plot shows the system's dispersion relation, and below it the system's detuning as a function of time under the influence of a trapezoidal detuning pulse. Each frame highlights a portion of the detuning pulse and a Bloch sphere illustrates the corresponding changes of the qubits state. (a) Step 1, initialization. The system begins at a large negative epsilon and is allowed to relax to the ground state $|L\rangle$ before qubit operations begin. (b) Step 2, pulse rise. The system's detuning is raised from its starting point at ϵ_0 to a value ϵ_{max}. During this step the system undergoes a Landau-Zener transition that includes both a θ_{LZ} and ϕ_{LZ} rotation the magnitude of which can by adjusting by changing the speed at which the system passes through the anti-crossing at $\epsilon = 0$. (c) Step 3, phase accumulation. Here the system is allowed to sit at a large positive detuning where the state will undergo a ϕ_{PA} rotation which can be adjusted by changing ϵ_{max} or the duration of this step. (d) Step 4, measurement. The system is returned to ϵ_0, once again undergoing a Landau-Zener transition. The system can subsequently be measured by projection on to the basis states $|L\rangle$ and $|R\rangle$.

1.3.4 Exchange Based Qubits

Many of the most promising qubit schemes are based not on the single spin-1/2 system, but on a two dimensional subspace of a larger system of 2 or even 3 electron spins[ZDM13, HPT07]. The simplest and most common exchange based qubit is the singlet-triplet qubit. Using a double quantum dot system, similar to the charge qubit, but now with 2 electrons, 1 in each dot. The qubits's operation relies on the singlet and the lowest energy triplet state, in the presence of a fixed magnetic field, to form a computational basis. The system can be manipulated by control of the detuning ϵ similar to the charge qubit. The detuning parameter affects the wavefunction overlap of the two electrons and hence the strength of the exchange interaction. Given that the singlet and triplet states have different total spins two axis control requires some additional system components, either an EM resonator or more commonly a nearby micromagnet to create an inhomogeneous magnetic field between the two quantum dots in the system. Using an alternative exchange interaction based qubit scheme avoids this complication. By using three electrons to form a single qubit, and using the two dimensional subspace $S = 1/2$, $S_z = 1/2$ of the three spin hamiltonian as a computation basis, two axis control can be implemented without the additional experimental challenges of fabricating a nearby micromagnet or resonator[DB00, MBT13, ELS15]. Exchange based qubits are generally best described in higher than 2 dimensions; this gives a clearer picture of their more complicated energy dispersion relations.

Another advantage of exchange based qubits is the simplicity of readout. Readout in quantum dots is generally performed by charge sensing. Charge sensing readouts allow for experimental measurement of the charge configuration on the dots. The

details will be covered later, but it is possible to measure the system to see whether, for example, it has two electrons in the left dot versus an electron in each of the two dots. This allows for a simple projective measurement based on the Pauli exclusion principle. While the qubit is generally manipulated with a single electron in each quantum dot, when a readout is performed, the detuning is rapidly pulsed to make two electrons in a single dot the most favorable state. This effectively pushes the two electrons to occupy the same spatial quantum state; however, given that the total quantum state of an electron must be anti-symmetric, this is only possible if the system is in the singlet state. Then the charge sensor will observe a change in charge configuration only for the singlet state providing an effective readout. In practice this 'spin blockade' is often difficult to observe, particularly in Silicon-based quantum dots, due in part to the existence of low lying excited states that provide for the formation of an anti-symmetric spatial wavefunction with both electrons in a single dot. Silicon based systems often suffer from nearly degenerate *valley states* that arise due to its crystalline symmetry. Understanding valley states and how devices can be engineered to form qubits with consistently large energy splittings between valley states is currently an active area of research. Interestingly, qubits based on this valley degree of freedom have been proposed and very recently observed for the first time. Although exchange based qubits are a very active area of research, they will not be covered in detail in this thesis. For a more detailed discussion see [ZDM13].

1.3.5 Valley Qubits

Although qubits based on the valley degree of freedom have been proposed for quite sometime, their observation is a relatively recent development[CSK12]. Chapter 4

will present the first conclusive observation of such a valley qubit. Similar to a charge qubit, a valley qubit consists of a single electron in a double quantum dot system. It is critical that one of the two quantum dots have a large valley splitting while the other dot has a relatively small splitting. The excited valley state in the dot with the large splitting can then be ignored and the system described in terms of the three charge eigenstates $|L\rangle, |R_g\rangle$ and $|R_e\rangle$. Here $|R_g\rangle$ and $|R_e\rangle$ represent the ground and excited valley states of the right dot. The states in the right dot provide the computational basis and the left dot allows for initialization and readout. The details of valley qubit operation will be discussed in detail in chapter 4. Valley qubits offer an advantage over other qubit implementations in that they possess a relatively flat dispersion relation in the region of detuning where qubit manipulation happens. This flat dispersion gives the valley qubit an intrinsic resistance to charge noise allowing for long dephasing times. There are still several practical challenges with regard to valley qubit fabrication. In particular, the energy splitting of the valley degeneracy depends on the microscopic details of the heterostructure interface near the quantum dot[ZLS13]. This makes fabricating devices with consistent valley splittings difficult. Many theoretical questions remain regarding how the local details of the heterostructure give rise to different valley splittings. Studying and characterizing valley qubits may prove to be valuable for developing this theory.

CHAPTER 2

Silicon-Based Lateral Quantum Dots

2.1 Gate Defined Quantum Dot Basics

2.1.1 Introduction to Field Effect Transistors

Field effect transistors (FETs) form the basis of nearly all modern computer chips and, as we will see, they have the potential to form the basis of a future generation of quantum computing chips. FETs are formed on various semiconducting heterostructures, but all share some common traits. FET heterostructures consist of a metallic top gate, an insulating layer, and finally a semiconducting layer. For the purpose of demonstrating operation, I will describe the fundamentals of the ubiquitous Si/SiO_2 based FET (MOSFET).

A basic FET has 4 gates, a source (V_S), a drain (V_D), a top gate (V_{TG}) and a bottom gate, which we will assume is always grounded. To start we will examine the heterostructure and how it behaves under the influence of the topgate, for the moment ignoring the source and drain gates. The heterostructure consists of a metallic top gate, a Si/SiO_2 insulating layer, a Si bulk layer, and finally a metallic bottom gate. Figure 2.1 plots the Silicon band diagram in 1 dimension along the z-axis of the hetero structure with V_{TG} = 0, where z=0 represents the interface between the Si

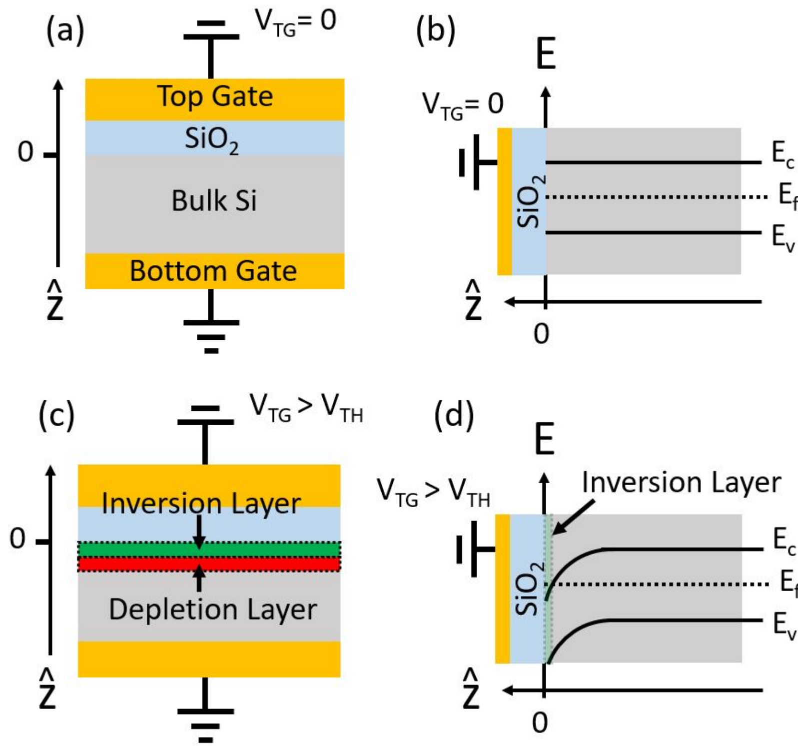

Figure 2.1: Basic principles of FET operation. (a) A cross sectional view of a MOSFET device showing the components of the heterostructure. When the topgate is grounded no current can flow through the bulk Silicon. (b) Cross sectional view rotated 90 degrees relative to (a). Here we plot the Fermi level E_f along side the energy of the conduction, E_c, and valence, E_v, bands within the bulk Silicon. When the topgate is grounded the Fermi level lies between the valence and conduction bands as expected for a semi-conductor. (c) A conducting layer can be turned on near the Si/SiO_2 interface by raising the topgate above some threshold voltage V_{TH}. This can be thought of as the topgate attracting charge carriers to the interface and forming an *inversion layer.* In terms of the device band structure, the topgate bends the band structure of the bulk near the interface until the conduction band drops below the Fermi level and the inversion layer turns on as shown in (d).

and Si/SiO_2 layer. By definition, in an undoped semiconductor the valence band is completely filled, and the Fermi energy lies between the conduction and valence bands.

Now consider the same structure but with a positive V_{TG}. This will tend to draw electrons from the bulk of the silicon leaving a positively charged *depletion layer* near the interface. Above some threshold voltage, V_{TH}, enough electrons will be drawn to the interface to form a conducting channel called an *inversion layer*. In terms of the semiconductor band diagram, a positive voltage applied to the top gate tends to bend the band diagram near the interface. A large enough voltage will shift the conduction band below the Fermi level of the bulk Si and a conducting channel will form[Dav98].

When connected to a source of electrons, the inversion layer can be thought of as a two dimensional electron gas (2DEG). The potential well at the interface is sharp enough relative to an electrons deBroglie wavelength that the cold electrons used in our experiments remain trapped in the $\hat{z}$ direction. Now that we have a conducting channel we can turn off and on with our top gate we need a way to make electrical contact with our inversion layer. This is where the source and drain contacts come in. These are highly n-doped regions that naturally conduct electrons. At one end they are connected to a source or drain voltage, while the other end overlaps with part of the inversion layer as in Figure 2.2b. Then current is free to flow between the source and drain contacts only when the topgate is used to turn on the inversion layer, creating an electronic switch and the basis of modern computing.

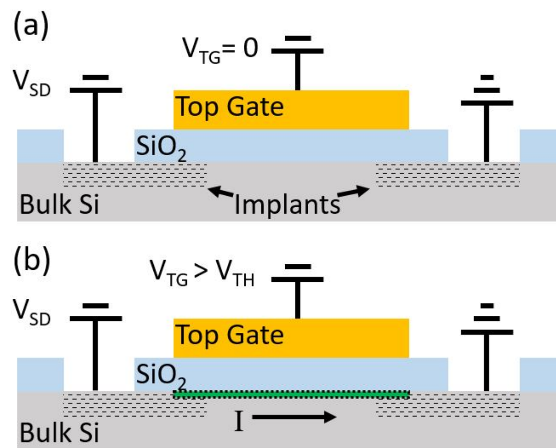

Figure 2.2: Cross section of a MOSFET device showing top gate, implant regions. In the case that $V_{TG} = 0$, (a), no current can flow from source to drain, but when V_{TG}¿V_{TH}, (b), the 2DEG is turned on and current is free to flow. Note that the insulating SiO_2 layer has been removed in order to make contact with the implanted bulk Silicon.

2.1.2 Depletion Gated Quantum dots

Broadly speaking, *quantum dot* refers to any potential well, generally in solid state systems, capable of confining one or many electrons on the order of its wavelength. This confinement gives rise to discrete energy levels that behave in many ways like artificial atoms with orbitals filled according to Hund's rule[Bir03]. In the previous section we saw how a FET can confine electrons in the $\hat{z}$ direction by forming an inversion layer at an interface. To form a quantum dot using an FET, then, all that remains is to further confine some of the electrons in our 2DEG in the x-y plane.

The simplest way to accomplish this is by fabricating additional gates, called depletion gates, between the topgate and the Si/SiO_2 layer. Depletion gates can be used to selectively turn off regions of the 2DEG by applying a negative voltage. The depletion gates work somewhat like a cookie cutter, preventing conduction in a region below the gate. The geometry of the depletion gates can be used to define a very small region disconnected from larger conduction regions connected to the source and drain of the FET. This is demonstrated qualitatively in Figure 2.3. Also shown is a scanning electron microscope (SEM) image of a set of depletion gates on Si/SiO_2 intended to form a single quantum dot. Following dot formation, small changes in depletion gate voltages can be used to adjust tunnel couplings to the source and drain as well as electron occupation number in the dot. Note the scale bar on the SEM image indicating the size of the dot is around 100nm and depletion gates as narrow as 20nm. Such is the scale required to see clear quantum effects, but, as we shall see, fabrication of devices on this scale presents many challenges.

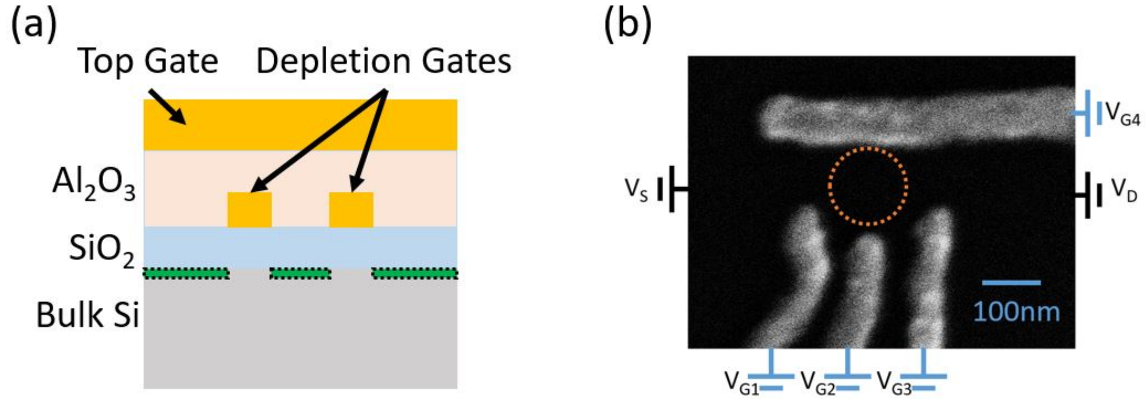

Figure 2.3: (a) Cross section of a depletion mode quantum dot. The large global topgate is used to turn on the 2DEG at the interface. Small local depletion gates, located between the topgate and 2DEG, allow for regions under the gate to be switched off. When designed properly, depletion gates allow for confinement of electrons in all 3 spatial directions. (b) Scanning electron micrograph of depletion gates intended to form a single quantum dot, taken before fabrication of a global topgate. The black regions of the image are bare Si/SiO_2. At the interface below these black regions the global topgate will turn on the 2DEG, allowing for conduction. The grey lines are gold depletion gates; tuning the voltages on these gates can turn off the 2DEG at the interface near the gate. When properly tuned the depletion gates form a potential well at the dot location indicated by the orange circle. The labeled voltages are under the users control. Black labels indicate electrical contact to the interface while blue labels indicate electrical contact with a depletion gate.

2.1.3 Accumulation Gated Quantum Dots

Recently, a modified Quantum Dot architecture has become popular, referred to as accumulation mode devices[ZHM15, ELS15]. Accumulation mode devices do away with the large global topgate and use a set of smaller local topgates. As opposed to depletion gate devices, which selectively turn off the 2DEG to confine electrons, accumulation mode devices selectively turn on the 2DEG to confine electrons. Figure 2.4 lays out the basics of an accumulation mode device. Note the overlapping gate architecture, which provides for an even smaller dot size and improved tunability as each quantum dot has its own topgate. Despite these benefits accumulation mode devices come with their own set of problems, most notably a dramatic increase in the difficulty of the fabrication process.

2.2 Device Fabrication

2.2.1 Lithography Basics

Lithography forms the basis for much of modern semiconductor fabrication. From its ancient Greek roots, lithography means stone writing, and historically refers to a printing process in which a flat plate (stamp) is worked with oil to help ink stick to certain areas. Ink can then be applied to the stamp and the stamp applied to paper. In semiconductor fabrication lithography refers to a process by which the surface of a substrate is covered with resist that is then selectively removed (a variety of methods are possible for this) exposing the surface of the substrate in certain areas only. The exposed areas can then be subjected to a variety of processes independently of the covered areas. Most commonly the areas exposed by lithography are either etched to

Figure 2.4: (a) Cross section view of an accumulation mode quantum dot device. Two larger topgates on the left and right turn on conduction to the implanted regions (not shown). The center topgate is used to adjust the potential on the dot. The layered depletion gates separating the dot's topgate from the source and drain topgates are used to adjust the shape of the potential and the tunneling rate between the source and drain to the dot. (b) Accumulation mode devices generally consist of 3 layered sets of aluminum gates insulated from each other by their native oxide. The shown design forms 3 quantum dots, 2 in series, and a single dot separated by a center wall. The bottom barrier or *wall* layer, turns off 2DEG regions to form two small channels. The second topgate layer deposits large source and drain topgates that extend from the edge of the channels formed by the walls to the implant regions. This layer also deposits the local topgates for each individual dot covering a region of the channel formed by the walls, but separated from other topgates by small gaps. The final layer fills in the small gaps left in the channel with tunneling gates. By turning off the 2DEG below the walls and tunneling gates and turning it on below the topgates quantum dots can be formed. (c) SEM image of device made using pattern in (b), predicted dot locations indicated by red circles.

remove material, or deposited upon to add material. Figure 2.5 shows the basics of deposition using lithography. By using multiple lithographic steps very complicated and small electronic structures can be fabricated.

The most common form of lithography in semiconductor processing is photolithography. In photolithography a light sensitive resist is applied to the substrate. A mask selectively exposes the resist to light. A photolithography mask generally consists of a glass plate which has been coated in reflective metal such that light may pass through in the shape of the desired pattern only. In many cases repeated steps of lithography must be aligned with each other. Placing both the mask and the coated sample in a mask aligner accomplishes this. The mask aligner allows for precise movement of the sample relative to the mask. Following alignment, the sample is gently pressed against the mask and exposed to ultraviolet light. The sample is then developed in a chemical developer that removes the exposed resist only. When pushed to the limit using high frequency light some industry processes have managed to write photolithography patterns on the nanometer scale. However, for most practical purposes and using only publicly available technology, photolithography is wavelength limited to around 500nm - 1um. To achieve the 50nm linewidth needed for lateral quantum dots an alternative method is required.

Electron beam lithography patterns the smallest leads. Qualitatively similar to photolithography processing, a specialized electron beam resist is applied to the substrate. The resist is selectively exposed to a high energy electron beam and then developed to remove the exposed resist. While purpose built e-beam lithography equipment does exist, our lab uses a modified scanning electron microscope (SEM). The SEM produces a high energy electron beam that is swept using a magnetic lens called a scanning coil. A computer controls the scanning coils to sweep the beam in

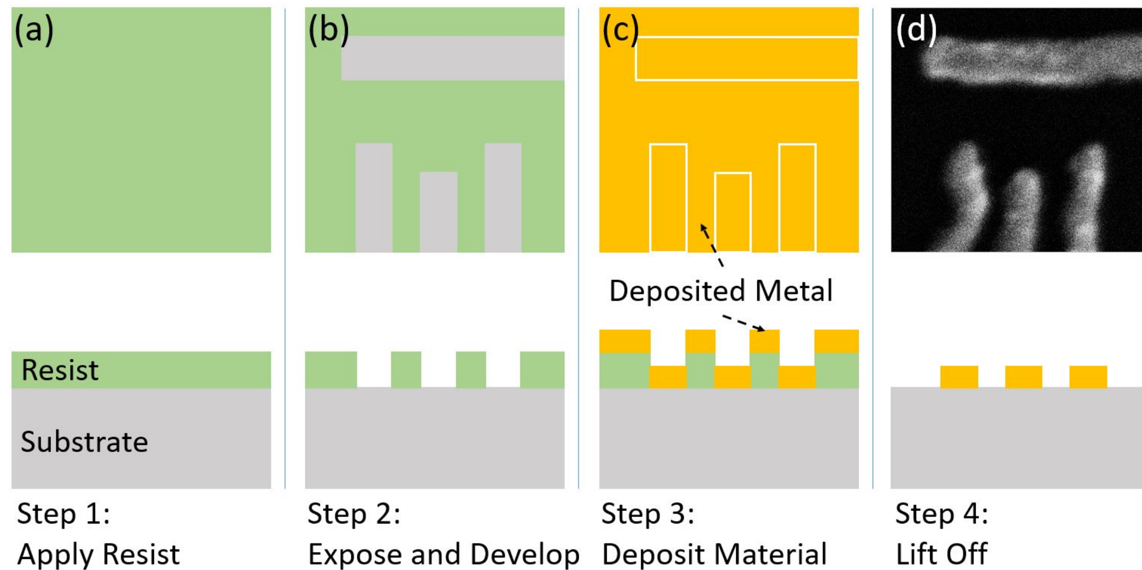

Figure 2.5: Basics of a lithography process consolidated into four steps. The top panels show the substrate as viewed from above at each step, while the bottom panels show a cross sectional cut away. (a) Apply resist: The substrate is cleaned and a thin layer of resist is applied via spin-coater over the entire substrate. (b) Expose and develop: The resist is selectively exposed in the shape of the desired pattern either via UV light (photolithography) or high energy electron beam (e-beam lithography). Following exposure, the substrate is submerged in a chemical developer which removes only exposed resist. (c) Deposit material: Material (generally metal) is deposited via evaporation covering the entire sample, but crucially only making contact with the substrate where the resist has been developed away. Alternatively material could be selectively removed at this step, for instance by submerging the substrate in an etchant. (c) Lift Off: The sample is submerged in a solvent which removes the remaining resist along with the metal deposited on top of it.

shape of the desired pattern. Using a 30 keV beam in our SEM we have successfully achieved linewidths in the 20-50nm range. Using electron beam lithography does come with its own set of drawbacks.

Since the device is patterned using a single swept beam, exposure can take a long time, particularly since increasing current tends to increase the beam's cross section and reduce exposure resolution. On top of this the writing area is limited to $\sim 200\mu\text{m}^2$, so each device must be aligned and exposed individually making the process time-consuming and labor-intensive relative to photolithography where entire arrays of devices can be exposed simultaneously. Finally there is evidence to suggest that the electron beam can damage the substrate and introduce defects, particularly in the case of Si/SiO_2 based devices. These defects can subsequently trap charge affecting qubit formation and possibly contributing to charge noise experienced by the device. To address these concerns there has been recent interest in pursuing device fabrication via nano imprint technology.

2.2.2 Substrates

Most of the early work on semiconductor quantum dots was performed on GaAs substrates, for several reasons largely related to simplicity of fabrication. First, GaAs heterostructures not requiring a global topgate were used, reducing the number of fabrication steps. Additionally, the electron's effective mass in GaAs is $0.067m_e$; this makes for 'larger' electrons and larger acceptable dot sizes and tolerances relative to Si based structures where $m_{eff} \approx m_e$. While e-beam lithography is still necessary for fabrication of the smallest leads on GaAs devices, yield is much better when operating away from the limits of its capabilities. Pushing the resolution limits of

common e-beam lithography is generally required to fabricate functional quantum dots on Silicon substrates. Ultimately, for reasons related to noise, which will be discussed in Chapter 3, much of the field has moved to Silicon based heterostructures despite the additional difficulty of fabrication.

The sections that follow give a qualitative walk-through of our fabrication procedures for Si/SiO_2. However, most of our discussion will also apply to Si/SiGe as the only difference in our procedures when fabricating on Si/SiGe versus Si/SiO_2 is that a hydrofluoric (HF) acid etch is not required to make contact to the implanted regions and the annealing temperatures are different. In this discussion I will ignore the various cleaning steps between each lithography, but a more quantitative step by step procedure that includes details of equipment used is laid out in Appendix ?.

2.2.3 Depletion Mode Fabrication

Fabrication begins using a commercially available Si/SiO_2 wafer. Most of our Si/SiO_2 based devices were fabricated on undoped float zone grown wafers ($\rho > 10,000\Omega/cm$) with 20nm of dry thermal oxide grown. Following receipt of the wafers, 30nm thick Cr alignment markers are evaporated to guide the alignment of subsequent lithography, Figure 2.6a. It is important to align arrayed devices with the crystal lattice at this step. Not doing so will lead to difficulties cleaving individual devices following fabrication as the wafer will tend to break along the lattice directions. The square lattice directions are generally marked by two flat edges in an otherwise circular commercial wafer.

The next step uses photolithography to define regions for ion implantation. The patterned resist is left on and the wafer is sent out to be commercially implanted

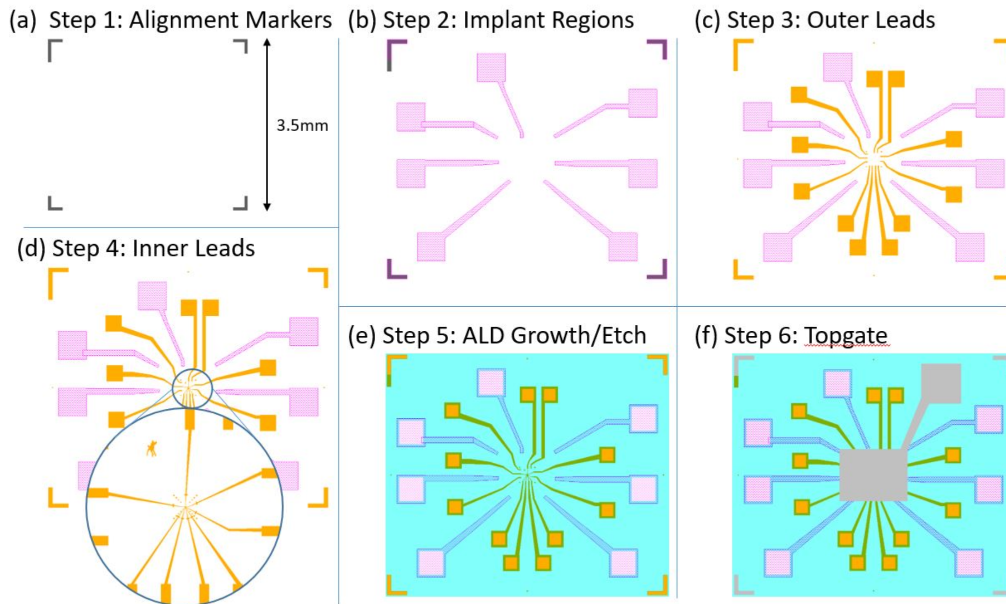

Figure 2.6: Top down cartoon of depletion mode device fabrication, showing how multiple lithography steps can be used to make a functioning quantum dot. (a) Using photolithography, alignment markers are laid down in chrome. (b) Using photolithography, the substrate is selectively exposed to a high energy ion beam creating implant regions. (c) Using photolithography, a set of large outer leads which will eventually make contact with the depletion gates are laid down in gold. (d) Using e-beam lithography the depletion gates are deposited in gold running from the device to the outer leads. The close up in (d) shows the inner e-beam leads making contact with the outer photo leads, note that even at this scale the device area itself is too small to see. (e) Using an atomic layer deposition system a conformal layer of insulating Al_2O_3 is grown over the entire sample. Following growth, photolithography is used to to selectively etch the insulating layer over the wirebonding pads of both the implant regions and the leads. (f) A global topgate is laid down in Al via photolithography and the device is ready to be tested.

with $2x10^{15}/cm^2$ 14KeV Phosphorous ions, Figure 5b. Following this, the wafer is ready to be annealed in a rapid thermal annealer at 750C for 30s.

Next, photolithography is used to make a set of 5nm Cr 45nm Au outer leads. Here, the 5nm Cr layer is used to help Au adhere to the SiO_2 surface. These leads will connect the innermost device leads, fabricated using e-beam lithography, to large contact pads used for wirebonding and provide alignment markers for e-beam lithography.

Now the sample is ready for electron beam lithography. Resist is applied, exposed, and developed; then the innermost leads are evaporated using 5nm Cr 45nm Au. After evaporation of the innermost leads lift off and any subsequent cleaning must be performed carefully as the nm scale leads are easily damaged.

Following application of the inner leads 100nm of Al_2O_3 is grown on the sample using atomic layer deposition. This insulating layer will prevent the global topgate from shorting to the inner or outer gold leads.

Photolithography is then used to pattern the global top gate and 300nm of Aluminum is evaporated. Another photolithography exposes only the wirebonding areas for the Ohmic contacts and outer Au leads which are then etched in Transetch-N to remove the Al_2O_3 layer above the pads. The final lithography step is a photolithography exposing only the Ohmic contact pads. These are then etched using buffered oxide etchant, exposing the implanted Silicon underneath.

At this point we have sometimes included a forming gas anneal step for Si/SiO_2 samples. The anneal happens in 380 torr of 15% H_2 85% N_2 at 400C for 30 minutes. Forming gas annealing is known to reduce the defects in SiO_2 and improve mobility in MOSFET devices. This step has been shown to help repair damage to the oxide

caused by electron beam lithography[KTL17]. We also observe that this annealing step seems to improve the quality of the Al_2O_3 oxide layer increasing its dielectric constant. Despite this we still have some concerns regarding this step. This step tends to alloy the Cr/Au device leads, increasing their resistance and potentially reducing the high frequency performance of the device. Annealing also has the potential to damage smaller or softer leads of the device, particularly if the innermost leads are evaporated in Al as opposed to Cr/Au. Given this and the fact that we have not observed a dramatic difference in real world device performance we sometimes skip this step. A detailed study of the charge noise experienced by annealed versus unannealed quantum dots would be a valuable contribution to the field.

To finish the ohmic contacts, a small amount of indium solder is applied by hand using a fine tipped soldering iron and great care. This step requires practice and steady hands to achieve the required precision $\sim$.2mm but indium makes good ohmic contacts with n-doped silicon. Designing a mask with this step in mind it useful to include some extra empty space around each ohmic contact pad to allow some room for error. The sample is now ready to be cleaved in to individual devices and mounted.

The sample is covered with a thick layer of photoresist to protect the underlying devices during cleaving, which is done by hand using a diamond scribe. Following a final cleaning for the individual devices, they are now ready to be mounted and wirebonded. We have used a variety of device carriers, from commercially available 16-pin DIP chip carriers to several custom made carriers, which will be discussed in more detail in the following section. The chips are secured to the carrier using A4 superglue. Finally the chip pads are connected to the carrier pads with Aluminum wire using a wirebonding machine and the device is ready for screening.

2.2.4 Accumulation Mode Fabrication

Very recently our lab has begun developing an accumulation mode device fabrication procedure. Many of the steps remain the same as the depletion mode fabrication steps, however the overlapping gate architecture requires several additional steps.

While characterizing and operating depletion mode devices, the depletion gate voltages are usually between -1V and .4V. Although variable most of our depletion gates, which are insulated from the 2DEG by 20nm of Silicon Oxide, will begin to leak to the 2DEG around .6V. We believe this leakage usually occurs as a result of oxide damage due to wirebonding. In depletion mode devices this is largely not an issue as the only large positive voltage is applied to the global topgate that has a bonding pad protected by an additional 100nm of Al_2O_3. In accumulation mode devices, the local dot topgates, as well as the source and drain gates, are patterned directly on the SiO_2 layer, resulting in unwanted leaks at small positive voltages. To mitigate this problem we break up the outer photolithography leads into an inner and outer part. The inner part lies directly on the SiO_2, and the outer part, including the wirebonding pad, lies on a 40nm layer of Al_2O_3 to provide protection during wirebonding.

The addition of a photolithography step doesn't add too much difficulty to fabrication; as a result, most of the challenges related to accumulation mode fabrication come from the 4 steps of electron beam lithography required. Three sets of inner leads are now evaporated as shown in Figure 2.4. Aluminum is used as it forms a native oxide, which serves to electrically isolate overlapping gates. For the overlapping gate architecture to work, each of the e-beam lithographies must be aligned with the last to a precision of order 10 nm. The alignment markers produced using

photolithography are not precise enough so new precision alignment markers near the device area are required; furthermore, as aluminum is difficult to image in a SEM it makes poor e-beam alignment markers. These reasons prohibit patterning the first set of leads in parallel with the alignment markers and means a 4th electron beam lithography is required to make gold markers. We have found that a pair of square markers 1um from the device works well. More details regarding accumulation mode device fabrication will be discussed in Chapter 6 and a step by step procedure is included in Appendix A.

2.3 Experimental setup

2.3.1 Installation of a Triton 200 Dry Dilution Refrigerator

Our lab is equipped with multiple cryogenic refrigerators; when I first arrived in the lab we had three set-ups: a top loading He3 refrigerator capable of 300mK temperatures and two wet dilution refrigerators both capable of sub 100mK temperatures. While all three of these refrigerators perform well once a working device is successfully cooled, they suffer from long turnaround times and small sample mounting volumes. The wet dilution refrigerators take around a week to remove existing samples and load new samples in; the top loading He3 is much better, taking between 4 -24hrs depending on how much of the He4 you are willing to lose. Given that each refrigerator accommodates a single sample (2 samples in the case of the Janis 500 dilution refrigerator), screening many quantum dots using these systems is an exercise in frustration. Fortunately, during my time in the lab I had the privilege of spearheading the installation of a Triton 200 dry dilution refrigerator. With a turnaround

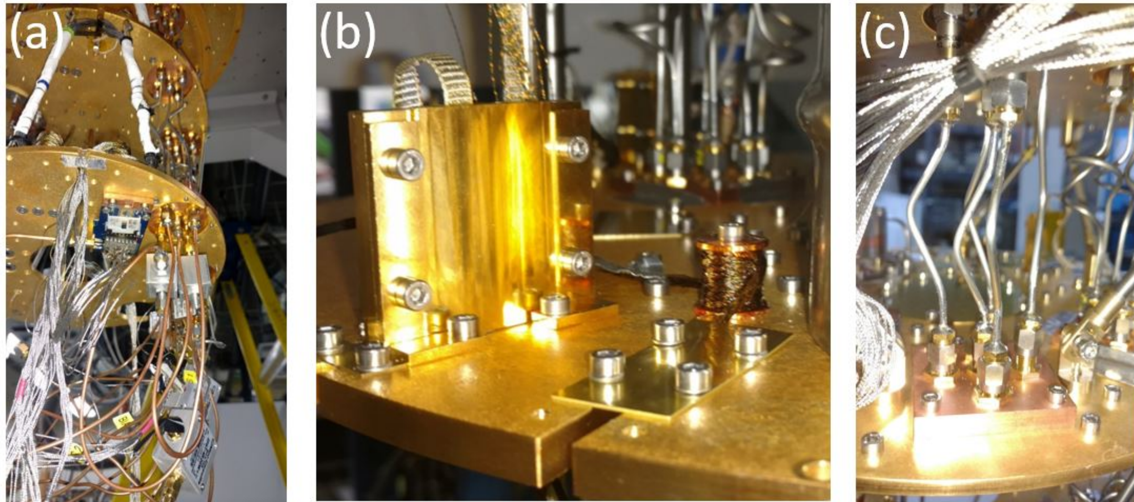

Figure 2.7: Triton 200 dilution refrigerator. (a) Mixing chamber plate with custom high frequency and DC wiring. A device can be seen mounted on the plate (blue PCB). (b) Heatsinking of DC lines can be seen for both factory DC lines (compression plate) and added lines (copper bobbin and varnish). (c) The high frequency lines are thermally anchored to each refrigerator plate; note the small bend to reduce thermal stress on the system during warm up and cool down.

time of 24 hrs and accommodation for 6-8 samples at sub 50mK temperatures this refrigerator has dramatically improved our screening capabilities.

The refrigerator was delivered with 24 DC lines installed and heat sunk, but with no wired breakouts or high frequency lines. The existing DC lines, consisting of a single cryogenic loom, were wired to three 8-pin single inline packages (SIP) on the mixing chamber plate to be plugged into sample carriers. On the room temperature end, the wiring was connected to a breakout box with 24 BNC inputs.

Given our desire to test many devices simultaneously, we initially added 36 additional DC lines, including 4 additional SIP plugs for device and 4 wires to single pins

used to bias cryogenic bias-tees on the mixing chamber plate. The new DC lines used shielded coaxial cooner wire; made from stainless steel, its poor thermal conduction works well for cryogenic wiring. At each plate of the refrigerator the wires were wrapped several times around a copper heatsink bobbin and subsequently glued to the bobbin using Lakeshore's VGE-7031 cryogenic varnish. This helped to heatsink the wires, bringing their temperature into equilibrium with each plate all the way down to the mixing chamber.

A set of 9 high frequency lines were designed and installed. Using semi-rigid SMA cables with stainless steel shielding, the high frequency lines were passed through custom copper plates at each refrigerator plate. While this process serves to cool the SMA shielding, cooling the signal wire is more difficult. To this end, a 20dB attenuator is placed in the high frequency line close to the 4K plate. Cooling the signal wire in this fashion grounds the line and requires the use of bias tees on the mixing chamber plate. We have had success with several commercially available bias-tees, but care must be taken to use only components with C0G (NP0) capacitor dielectrics and thin film resistors. Additionally, many broad band bias tees use strong magnetic materials in their inductors and must not be used for any experiment involving a large magnetic field.

Following a year of successful operation, we decided to add even more lines to expand the potential number of devices again, adding an additional 16 DC lines (2 SIPs) and 5 high frequency lines. Two out of the 5 new high frequency lines were set-up with high frequency amplifiers on the 4K plate to enable reflectometry measurements on devices. While cryogenic amplifiers are expensive, we have avoided the cost by using two minicircuits ZX85-12G-S+ amplifiers. These are not designed for cyrogenic use, but other groups have found success operating these amplifiers at

liquid helium temperatures [HHP15]. To use these amplifiers the capacitor protecting the +5V line-in must be unsoldered and removed, otherwise it will fail upon thermal cycling and prevent the amplifier from powering on.

2.3.2 Device Mounting

Before installation of the Triton 200 system device screening, was performed by mounting the device on to a 16 DIP chip carrier and submerging the device directly into liquid helium at 4K using a probe with a 16 pin socket. After a successful screening the device was removed and remounted on a custom carrier made for our Janis 500 dilution refrigerator accommodating 2 high frequency inputs. Remounting devices to suitable carriers after screening was regularly damaging devices so I set out to make a device carrier that was suitable for use in a regular liquid helium dewar, in our Janis 500 dilution refrigerator, and in our Triton 200 dry dilution refrigerator. This way devices can be screened and moved between refrigerators without remounting.

The carrier was designed to accommodate a large variety of devices, accepting up to 24 DC voltages and 4 SMA HF lines. In many cases this has allowed us to accommodate two devices on a single holder. The primary challenge was making a board that is narrow enough for the 4k dewar, low profile enough for the JDR 500, and mounted conveniently in the Triton system. This required careful hand routing of lines and a multi-layer PCB. Past experience led us to have the boards gold-plated as wire-bonding to copper (tinned or bare) is difficult. Figure 2.8 shows both CAD drawings and end result for the boards.

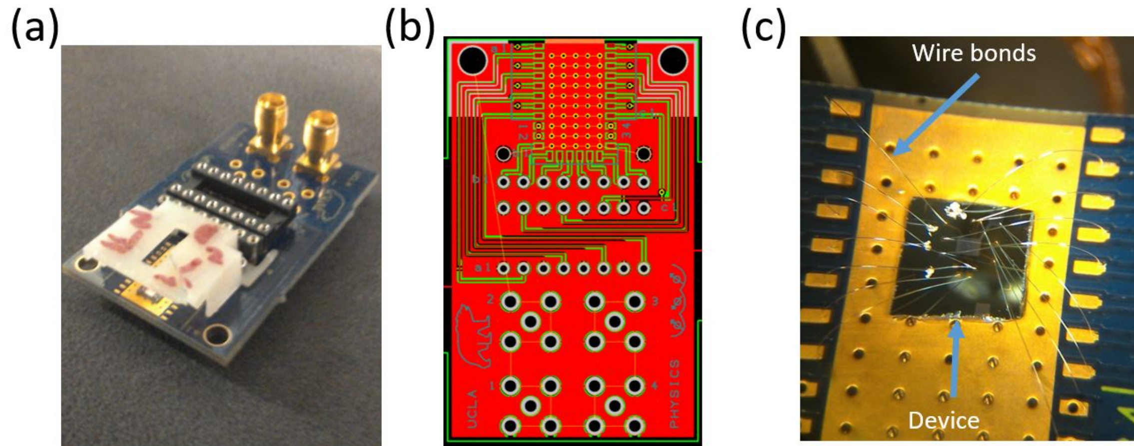

Figure 2.8: (a) Device fully mounted and ready for cooldown. Wirebonds and device can be seen below the white protective cap. (b) CAD image of carrier layout (top layer). (c) Close up image of mounted device, showing the sample glued to the ground plane and connected to the holder contacts via wirebond.

2.3.3 Device Filtering

When the device is in good thermal contact with the mixing chamber of a dilution refrigerator we can assume that the lattice temperature of the device heterostructure is in thermal equilibrium with the refrigerator's base temperature, generally below 50 mK. Despite this the electron temperature of the device's source and drain can be substantially higher. Measurements of electron temperature on unfiltered DC lines yield results between 200-400 mK across our setups; while these temperatures are acceptable for observing many qubit behaviors, if we wish to maximize coherence times by reducing the electron temperature filtering of the DC lines is required.

To begin including cryogenic filtering in our experiments I designed a stackable system of filters for our Triton 200 refrigerator. The filters can accommodate 8,

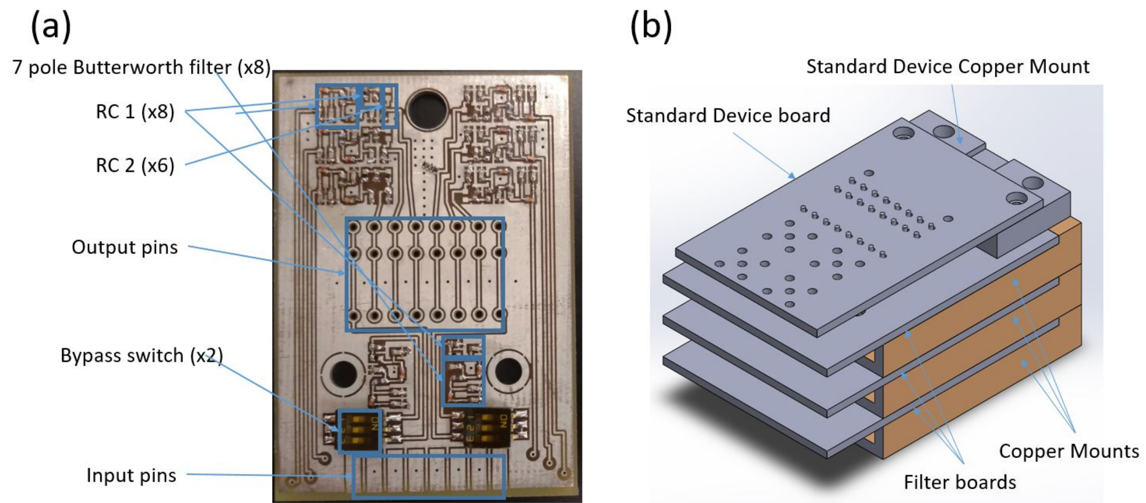

Figure 2.9: (a) Cryogenic filters for up to 8 DC lines with various components labeled. (b) The modular stacking structure was designed to be flexible, allowing for fast mounting and adjustment of the number of filtered lines 8, 16 or 24. Shown is a CAD illustration of a device board mounted to a 3x filter stack (24 lines). (c) Circuit diagram of the cryogenic filter showing the Butterworth filter and two RC filters along with their respective frequency cut offs.

16 or 24 DC lines by simply stacking them on top of each other. Finally the chip holder described in the previous section plugs directly into the filter stack as shown in figure 2.9. Each line is filtered using an 8 pole Butterworth filter with a cutoff frequency of ∼80MHz followed by two RC filters with cutoff frequencies of 145 KHz and 160 KHz. Due to time constraints a detailed analysis of the filter's performance on electron temperature has not been performed. Attenuation data were taken using several methods between 1 Hz and 5GHz, shown in Figure 2.10. Several unintended resonances exist in the 1 - 100 MHz range likely due to filter geometry. The filter is still expected to provide a noticeable improvement in electron temperature and initial measurements on filtered devices suggest an improved signal to noise ratio yielding particularly clean charge sensing data.

2.4 Characterizing a Double Quantum Dot

2.4.1 Introduction and Device Layout

To develop an understanding of basic measurement techniques commonly seen in quantum dot literature the initial characterization of a double quantum dot device will be discussed. The device to be characterized has a depletion gate pattern identical to the one shown in Figure 2.11. The bottom 5 depletion gates control the chemical potential and tunnel couplings of the double quantum dot system. The outer 2 gates, used to control tunneling to the source and drain, are referred to as barrier left (BL) and right (BR) respectively. The center gate, used to tune inter-dot coupling, is referred to as (T) and the remaining two gates are the left (PL) and right (PR) plungers, used to tune the chemical potential and hence the occupation

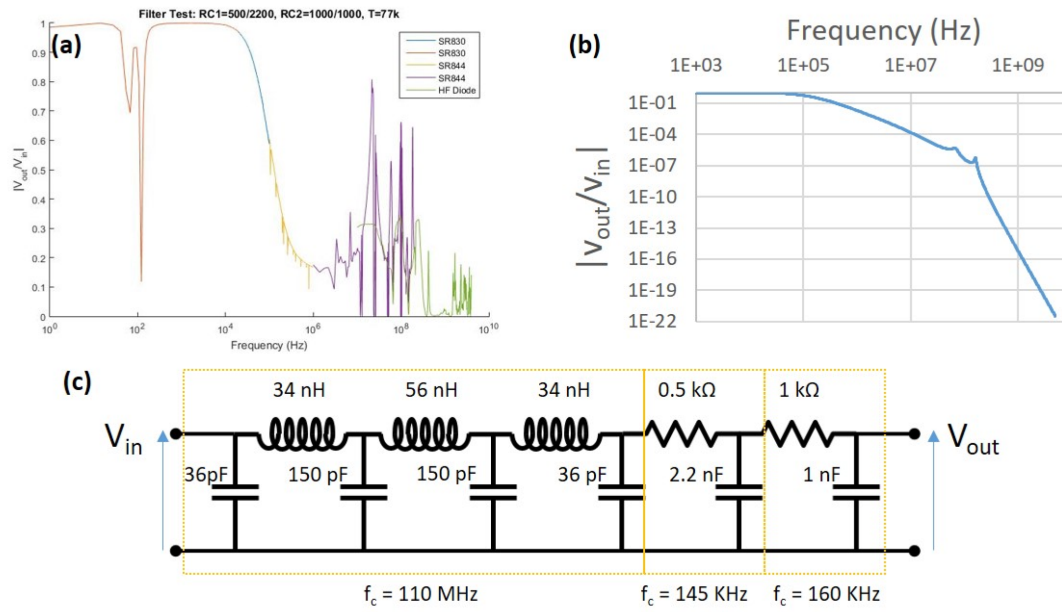

Figure 2.10: (a) Attenuation data through a filtered line submerged in liquid nitrogen at 77 K. Data was taken via either lockin amplifier or high frequency diode depending on the frequency range. Several unanticipated resonances between 1 MHz and 100MHz exist, probably due to filter geometry. (b) SPICE simulation of the filter showing attenuation data. Plotted in log-log so that effects of both the RC filters and the higher frequency Butterworth filter can be seen.

of the dots. Above the control gates is a thick "wall" gate, which is generally left grounded. Finally, above the wall, there is the Q gate. The Q gate is used to adjust the resistance of the quantum point contact (QPC) current channel. As we will see later the QPC channel can be used to measure changes in dot occupation.

For a basic understanding of how control gates are used to manipulate our double quantum dot system we can model the system as seen in Figure 2.11b. This is a simplification as it ignores various cross capacitance and the contribution of discrete quantum energy levels to chemical potential, but it helps provide an intuitive understanding of ubiquitous stability diagram. For brevity, the details of the result will be ignored, but can be found in various review articles and books[WDE02]. Some algebra results in the chemical potential $\mu_{1(2)}(N_1, N_2)$ of dot 1(2) where N_1 and N_2 are the number of electrons on dots 1 and 2. This chemical potential is a function of the depletion gate values. We will assume for the moment that both the source and drain are grounded and define their chemical potential $\mu_L = \mu_R = 0$. Then we can plot a stability diagram as a function of voltage on PL and PR. This stability diagram shows regions of stable dot occupation numbers, which can be found by calculating the largest value of N_1 and N_2 for which both $\mu_1(N_1, N_2)$ and $\mu_2(N_1, N_2)$ are less than 0.

Figures 2.12a and 2.12b show stability diagrams resulting from extremely low or high inter-dot couplings. In the case $C_M \to 0$, the result is two independent dots while a large coupling as in Figure 2.12b will effectively lead to a single large dot. In the intermediate regime shown in Figure 2.12c regions of the stability diagram are defined by lines of $\mu_{1(2)}(N_1, N_2) = 0$ called charging lines and lines of $\mu_1(N_1+1, N_2) = \mu_2(N_1, N_2 + 1)$ called inter-dot lines. The points where all three lines meet, on either end of interdot lines, are called triple-points. At these points the equality

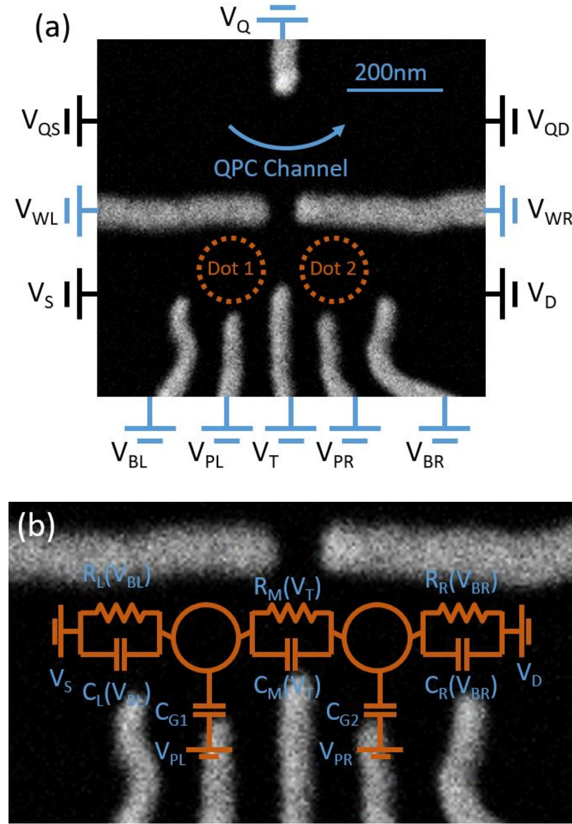

Figure 2.11: (a) SEM image of the depletion gates on a double quantum dot device with dot locations indicated by the orange circles. (b) SEM image superimposed with a basic capacitance model of the double dot system. Each quantum dot is modeled as an island with $N_{1(2)}$ electrons on it connected to the gates, the source, and the drain by a system of capacitors and resistors. The electron occupation on the dots is adjusted via the voltages V_{PL} and V_{PR} for the left and right dots respectively. Resistance and capacitance between the system and the source/drain can be tuned using the outside barrier gates, V_{BL} and V_{BR}. Similar tunneling between the two dots is controlled via the tunneling gate V_T.

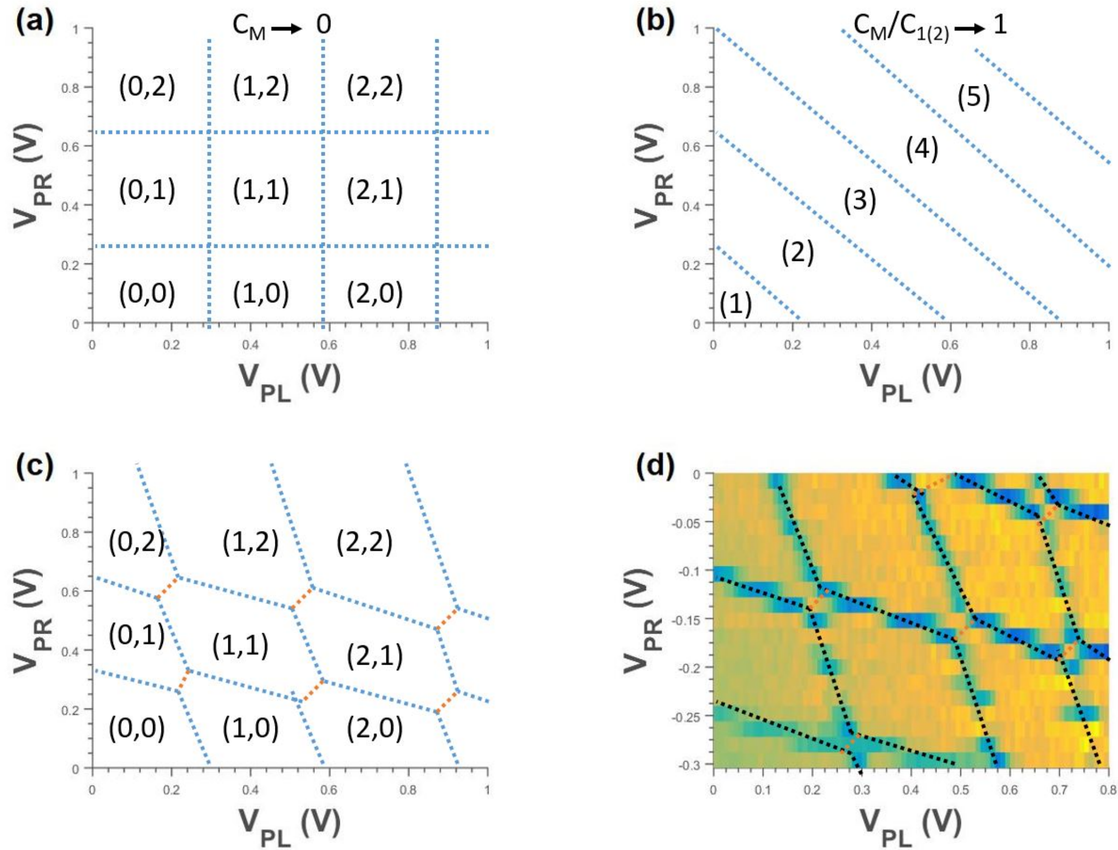

Figure 2.12: Stability diagrams indicating the stable charge configuration of the left and right dots. The tuple (N1,N2) indicates the number of electrons on the left and right dots respectively. (a) In the case of zero coupling the dots behave independently, only responding to the voltage of their respective plungers. (b) In the case of strong coupling, the system behaves like a single large dot; the occupation is an equal function of either plunger. (c) In the intermediate region the stability diagram forms a 'honeycomb' consisting of charging lines (blue) and interdot lines (orange). (d) Measured stability diagram of a double quantum dot device displaying a characteristic honeycomb pattern.

of chemical potentials, for instance, $\mu_2(N_1, N_2) = \mu_2(N_1, N_2) = \mu_1(N_1 + 1, N_2) = \mu_1(N_1, N_2 + 1) = 0$ allows for current to flow from source to drain via single electron (or hole) hopping. If a source-drain bias is applied these regions will expand into *bias triangles*, triangular regions where current can flow.

2.4.2 Transport Measurements

When characterizing a new device the first step is generally to take several transport measurements, beginning with transport through the QPC. A small bias of ~1mV is placed across the QPC channel and current through the channel is measured. The global top-gate voltage is slowly raised until a current is measured through the channel. At this point the functionality of all depletion gates is checked; cross capacitances are strong enough that applying a negative voltage of ~-1V on any gate should affect the current through the channel. To populate the quantum dots, the global top-gate will generally have to be raised further beyond the QPC turn on voltage.

A reasonable method to ensure that the double quantum dot system is populated before moving to charge sensing measurements is to place a small bias across the source and drain of the double quantum dots and raise the topgate voltage until bias triangles can be observed as a function of V_{PL} and V_{PR} such as in Figure 2.13c. Note how these bias triangles reveal parts of the underlying stability diagram. The bias triangles represent an enlargement of the triple points from a conducting point to a conducting region. This measurement has the added benefit of allowing for the calculation of the lever arms α, which relate the voltage on the depletion gates to the chemical potential of the dots.

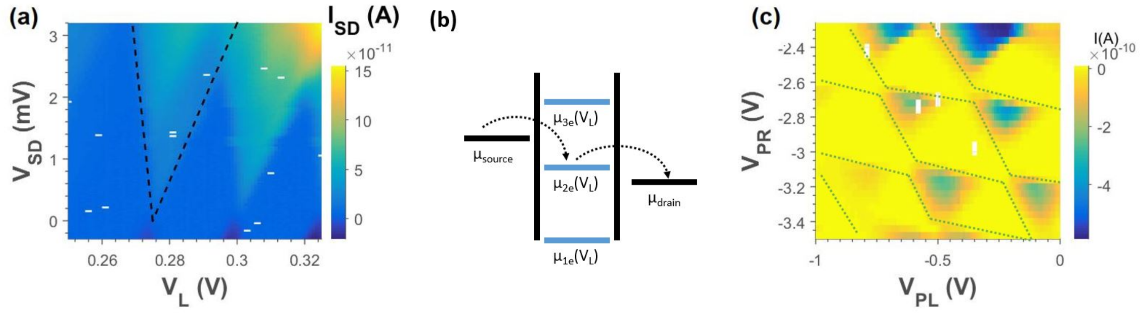

Figure 2.13: (a) Measurement of current through a single quantum dot as a function of plunger voltage versus bias voltage. As the discrete energy levels of the dot pass through the bias window between source and drain, current flows. This common measurement produces diamond-like patterns dubbed 'Coulomb diamonds.' (b) Illustration of current flowing from source to drain through a single dot. The chemical potentials of the source and drain are fixed by an applied voltage. The chemical potential of the dot is then adjusted via a depletion gate. This shifts the chemical potential of the dot's energy levels. As the levels pass through the bias window current flows from source to drain. (c) Sample current measurement through a double quantum dot system as function of left and right plunger gates. This measurement produces 'bias triangles' where current can flow.

While not a standard practice during characterization, transport through the system when it has been tuned into a single dot configuration will be discussed as this will be relevant in the following chapter. Raising the voltage on the T gate can often tune this double dot system into a large single dot. In this case, a common measurement is current through the dot as a function of bias voltage V_{SD} versus a depletion gate adjusting the chemical potential of the dot. This measurement produces a 'Coulomb Diamond' as seen in Figure 2.13a. The diamond is produced as the chemical potential of discrete energy levels pass through the bias window a process shown in Figure 2.13b. At large enough bias windows the current contributions of multiple energy levels can be observed. Coulomb diamond measurements allow for calculation of the gate's lever arm, the charging energy of the system, energy splittings of excited states, and, as we will see later, charge noise.

2.4.3 Charge Sensing Measurements

While transport measurements through the quantum dots are useful for characterization they are not used for qubit operation. Generally qubit experiments are performed using one of several charge sensing techniques. Our device set up uses the nearby QPC channel to sense changes of electron occupation on the double dot system in the following way.

The device is first tuned to a regime where we expect the dots to be occupied. Then the QPC channel is biased and the current adjusted using the Q gate. The Voltage V_Q is tuned such that the current through the QPC is away from any conductance plateaus and a strong function of V_Q. When this is the case the current through the QPC channel will also be a strong function of its surrounding electro-

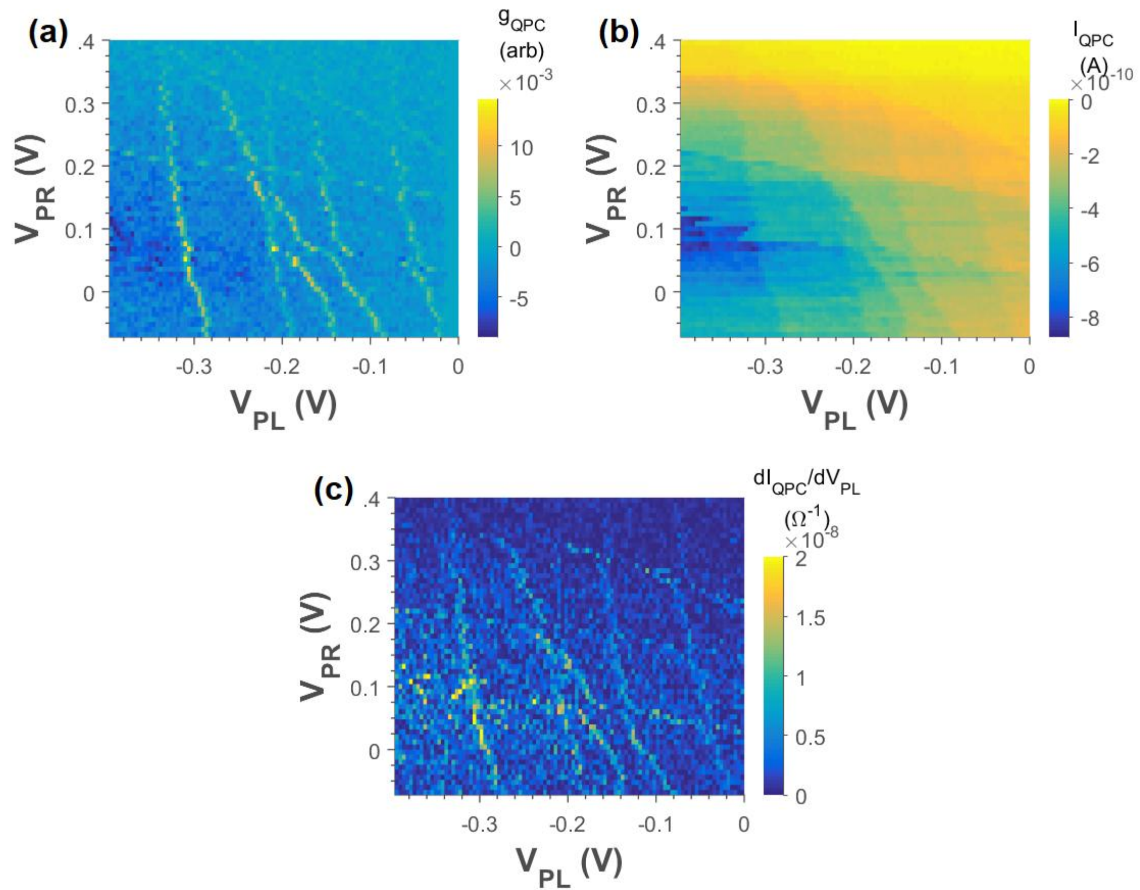

Figure 2.14: To demonstrate the different types of QPC charge sensing measurements, three simultaneously acquired stability diagrams are shown. (a) Data acquired via lockin amplifier responding to a small oscillating voltage (dither) of about 1mV at 100Hz added to depletion gate V_{PL}. The charging lines appear as spikes in signal due to an electron hopping on and off of a dot as a result of the dither. (b) Direct current data through the QPC; note the discontinuities representing charging events. These discontinuities can be used to map out the stability diagram, although it is usually easier to examine the derivative. (c) Derivative of the DC data from (b) with respect to V_{PL}.

static environment. If the QPC channel is sensitive enough we can now measure the QPC current as a function of V_{PL} and V_{PR}. When a depletion gate is tuned such that an electron is added to a dot (or moves between dots) the current through the QPC channel will shift suddenly. Then the stability diagram is revealed as in Figure 2.14 and 2.12.

In many cases a direct measurement is difficult to see so a homodyne measurement using a lockin amplifier is used. In this case a small oscillating voltage is placed on a depletion gate (PL for instance), generally around 1 mV and at a frequency less than 1kHz. When the system is at a charge transition, this oscillating voltage will repeatedly add and remove an electron to a dot. The lockin isolates and averages over this process yielding a dramatic increase in QPC sensitivity. Figure 2.14 shows stability diagrams taken using both DC and homodyne measurement.

2.4.4 Qubit Measurements

Once the device produces a clear charge sensing signal the depletion gate voltages are adjusted to bring the device into a nice double dot regime. In order to observe qubit behaviors pulse experiments are performed by attaching high frequency pulse or arbitrary waveform (AWG) generators to depletion gates PL and PR and the device is tuned to be near an interdot transition. Depending on the qubit implementation, a variety of pulse shapes and rates can be used. Figure 2.15 shows an example of an experimental set up for pulse based experiments on a single quantum dot.

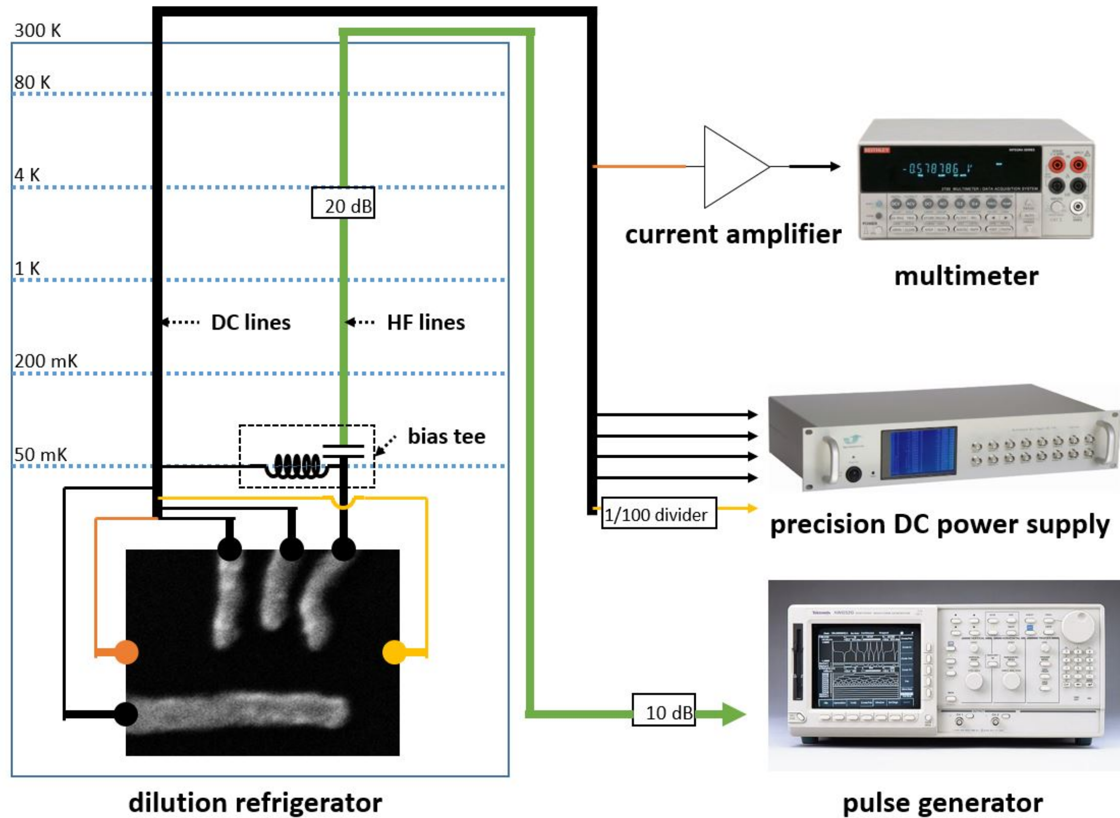

Figure 2.15: Showing wiring from the inner most device leads to experimental electronics at room temperature. The source and drain lines are shown in yellow and orange respectively. The dashed blue lines indicate *plates* within a dilution refrigerator fixed at the label temperature. The DC lines are heatsinked at each plate, while the HF line has a 20dB attenuator near the 4 K plate to help cool the line. This necessitates the use of a bias tee on the 50mK plate.

CHAPTER 3

Charge Noise in Silicon Quantum Dots

3.1 Relaxation and Coherence in Quantum Dots

3.1.1 Noise in Qubit Systems

Unlike in a conventional bit in a digital computer, noise is an important problem for the qubits in a quantum computer. For a traditional bit that has two states, say on is +5V and and off is 0V, the problem of noise is addressed by treating any value above 2.5V as on and any value below as off. This approach can mitigate the effects of noise as even fluctuations as large as 1V would be acceptable.

As we saw previously, a good qubit should function as a quantum mechanical two level system. Such a system has a state represented by $|\psi\rangle = \alpha\,|0\rangle + \beta\,|1\rangle$ and even a small fluctuation in an α or β represents a new computational state. Over the course of a calculation, such fluctuations may introduce large errors. In light of this, dealing with noise in quantum systems is a pressing issue in all implementations of quantum computing and is being addressed in two ways: first, by the development of quantum error correcting codes and architectures that reduce the systems susceptibility to noise and second, by working to reduce the noise in individual qubit systems. To model this noise in our systems, the simple Schrödinger equation based formalism

developed in the previous chapter will no longer be sufficient, and a density matrix approach is more suitable.

3.1.2 Understanding Relaxation and Dephasing Times

We can break down noise experience by a qubit into two distinct types, dephasing and decoherence. Decoherence represents a relaxation of the qubit in an arbitrary state, $\alpha |0\rangle + \beta |1\rangle$, to its ground state, $|0\rangle$, through an exchange of energy with its environment. The time scale of this interaction is denoted by T_1, the relaxation rate.

To understand dephasing it is useful to rewrite our state as $|\psi >= \cos\theta/2 |0\rangle + e^{i\phi} \sin\theta/2 |1\rangle$ and consider a Bloch sphere representation as discussed in the previous chapter. As previously discussed, in the case where θ does not equal 0 or π the state vector will process about the z axis are a frequency governed by the qubits energy splitting. Noise in the qubit's environment that causes fluctuations in the qubits energy splitting during its operation will thus tend to blur the phase ϕ with a timescale denoted by T_2.

The final timescale regularly reported for qubits in literature is T_2^*, sometimes referred to as the free induction decay time. To introduce the concept I will first explain it in the context of nuclear magnetic resonance (NMR) where much of this physics was first explored and which I believe provides a better intuitive understanding of T_2^*.

NMR explores the spin physics of samples by examining the behavior of a macroscopic number of spins simultaneously. The spins are placed in a fixed magnetic field in the $\hat{z}$ direction and manipulated by application of a rotating magnetic field in the $x - y$ plane. Following manipulation, measurement is sensitive to the procession,

not of a single spin, but of all of the spins in the sample, i.e. the net magnetization in the $x - y$ plane. Now consider the case where we rotate our magnetization into the $x - y$ plane and watch measure decay. Based on our previous discussion you might guess that it would decay on the timescale T_2, but what is observed is the much faster decay, referred to as free induction decay (FID) with timescale T_2^*. This decay is due to small spatial variations in the magnetic field experienced by each spin causing them to process at slightly different frequencies resulting in a situation where the individual spins are still in a coherent state, but not in phase with each other. Hence, as any measurement is of the net magnetization the signal will decay. Various techniques exist for periodically bringing these spins back in phase so that the dephasing time T_2 can still be measured. In the context of individual qubits we are no longer subject to these spatial variations in procession rates but are instead subject to temporal fluctuations in the procession rate of a single qubit over the course of repeated measurements. As any individual quantum measurement of qubits returns only a single value, $|0\rangle$ or $|1\rangle$, any measurement of phase as a function of time will necessarily rely on repeated measurements of a qubit over a period of time. In this way our qubit ensemble over time mirrors the NMR based ensemble over space with slow temporal fluctuations in qubit dephasing mirroring spatial fluctuations in NMR dephasing.

Although common, it is somewhat reductionist to assign a single value for T_1, and T_2 in a qubit system. These values are generally not fixed and depend on a multitude of factors including qubit energy splittings and couplings, values that are regularly modified throughout the course of qubit operations. Additionally there may be multiple distinct timescales for T_1 and T_2 as dephasing or decoherence may arise from multiple distinct microscopic sources. However, as we will see in Chapter

5, a single value is often enough to provide insight and reproduce observed data via simulation.

3.1.3 Microscopic Origins of Noise in Semiconductor Quantum dots

Decoherence (T_1) in spin based qubits requires an exchange of energy with the surrounding lattice; this interaction is mediated by emission of a phonon to the lattice. In most III-V semiconducting materials the dominate source of spin-phonon coupling is via the piezoelectric effect. However, another advantage of using silicon over other substrates is that it lacks a piezoelectric effect. The only remaining source of phonons in Si is due to local fluctuations in lattice spacing (deformation potential). While these phonons do not couple to pure single spin states, in practice the eigenstates will contain elements of orbital and valley states due to spin orbit interaction, resulting in coupling to the phonon bath[ZDM13]. In silicon single spin as well as singlet triplet T_1 times on the order of ms and higher have been observed[ELS15].

With regards to dephasing, there are two primary dephasing mechanisms in semiconductor quantum dots: fluctuations in the local magnetic field due to the nuclear Overhauser field and fluctuations in the electrical potential due to charge noise[ZDM13]. Nuclear spins will only affect qubit schemes that incorporate spin and this noise is the primary component of dephasing in many older GaAs based qubits where large nuclear spins are present. However, over the past decade focus has shifted towards Silicon based heterostructures as a means to solve this problem. Silicon is used because its primary natural isotope ^{28}Si has a nuclear spin of 0, dramatically reducing noise. While the spin 1/2 ^{29}Si still makes up 5% of natural Silicon, single spin dephasing times on the order of hundreds of μs have been observed in

Silicon based quantum dots a significant improvement over the $\sim \mu s$ times observed in GaAs dots[BFN11]. Even further improvements in single spin dephasing can be expected through the use of isotopically purified Silicon. This has been explored in donor based qubits more extensively than in laterally gated dots, but has yielded promising single spin dephasing times on the order of seconds[ELS15].

Silicon thus would seem to be a great platform for spin based quantum computing with excellent single spin dephasing and decoherence times. This may ultimately prove to be the case, but most practical proposed implementations of quantum computing rely on some sort of exchange coupled qubit like the double dot exchange qubits or the triple dot exchange only qubits discussed in Chapter 2. However, measurement of dephasing times in exchange based qubits, even in isotopically purified Si/SiGe samples, are on the order of μs much faster than predicted due to Overhauser effects. While the source of this dephasing is still not completely understood the remaining dominant source of noise in exchange based qubits is expected to be charge noise[ZDM13].

Unlike Overhauser noise, charge noise has the potential to affect the operation of most single qubit implementations, single spin qubits being the notable exception. Charge noise is simply noise in the chemical potential of the quantum dot's energy levels. This noise can arise from various sources, including voltage noise on control gates and source-drain contacts, as well as potential wells in the environment surrounding the qubit caused by defects that give rise to fluctuators. These fluctuators periodically trap and release one or more electrons giving rise to fluctuations in the electrostatic background. Noise from voltage sources can be mitigated by choosing low noise voltage sources in addition to room temperature and cryogenic filtering. For most practical purposes, fluctuators in the qubit's environment are the primary

source of charge noise. These fluctuators give rise to the fairly ubiquitous $1/f$ power spectral density (PSD)[PGF14].

3.1.4 Introduction to $1/f$ Charge Noise

Sometimes called pink or flicker noise, $1/f$ noise spectra appear in nearly all electronic devices. Despite its apparent ubiquity, research has failed to produce a universal theory regarding the source of $1/f$ noise. Instead, $1/f$ noise appears to arise via a variety of different physical mechanisms depending on the system examined. In many systems, including semiconductor quantum dots, there is still debate within the community regarding the source of $1/f$ noise spectra. What all theories of $1/f$ noise share in common, however, is that the spectrum arises from coupling to a distribution of fluctuators with broadly distributed switching times[PGF14]. As $1/f$ noise poses an obstacle for nearly every solid state implementation of quantum computing, whether superconductor or semiconductor based, understanding its physical origins and how it affects qubits is an important problem.

Consider a single fluctuating quantity with relaxation rate γ, then the correlation function $x(t)$ is proportional to $e^{-\gamma|t|}$. This yields a spectral density that is Lorentzian in frequency,

$$S_x(\omega) \propto \frac{\gamma}{\omega^2 + \gamma^2}. \tag{3.1}$$

Such a spectrum has been observed several times in current noise measurements from QPCs and single quantum dots[KCT97, LTH90]. This results from a fluctuator close to the device, whose state has a strong enough affect on the electric potential experienced by the dot or QPC to dominate the noise spectrum. When the device

is biased these fluctuations in turn cause measurable current fluctuations. Most measurements of current through QPCs or quantum dots, however, produce a $1/f$ noise spectrum. This is because the system is subject to noise from many fluctuators with different relaxation rates γ giving rise to a distribution of relaxation rates $P(\gamma)$. Then the noise spectral density is,

$$S_x(\omega) \propto \int_0^\infty d\gamma P(\gamma) \frac{\gamma}{\omega^2 + \gamma^2}. \tag{3.2}$$

If $P(\gamma) \propto 1/\gamma$ in some range $\gamma_{max} > \gamma_{min}$ then this spectral density is proportional to $1/\omega$ in the range $\gamma_{max} > \omega > \gamma_{min}$ [PGF14]. Now what remains is to specify the microscope processes that can give rise to such a distribution of relaxation rates, and this in turn depends on the system being examined. While the debate is not closed regarding the origin of fluctuators influencing quantum devices on Silicon heterostructures, it is widely believed that charge traps near the heterostructure's interface are largely responsible[CHD10]. The source of these charge traps in various systems is still a topic of discussion and there has been some debate as to whether charge noise in Si/SiO_2 based heterostrucutres would be larger than Si/SiGe based structures due to the properties of the interface and the fact that SiO_2 is an amorphous solid. As we shall see evidence is beginning to suggest this may not be the case.

3.1.5 Understanding the Importance of Low Frequency $1/f$ Noise in Qubit Systems

Now that we have overviewed the sources of noise experience by our quantum dot systems, lets explore the simplest model we can to understand how this noise affects

the practical operation of a qubit. The simple charge qubit system discussed in Chapter 2 is a good place to start. Recall its Hamiltonian given by,

$$H_{CQ} = \begin{bmatrix} \frac{\epsilon}{2} & \Delta \\ \Delta & -\frac{\epsilon}{2} \end{bmatrix}. \tag{3.3}$$

To examine how noise affects dephasing we rotate the system into the energy eigenbasis,

$$H'_{CQ} = \begin{bmatrix} \frac{\varepsilon}{2} & 0 \\ 0 & -\frac{\varepsilon}{2} \end{bmatrix} \tag{3.4}$$

Where we have defined $\varepsilon = \sqrt{\epsilon^2 + \Delta^2}$. Now to see the affects of noise we will work with the Bloch vector $\vec{M}$ using the density matrix ρ, to define $\rho = (1 + \vec{M} \cdot \vec{\sigma})$. We will limit our discussion to longitudinal noise, where $\varepsilon(t) = \varepsilon_0 + \varepsilon_{noise}(t)$ while noise in the off diagonal terms is 0. This case, called pure dephasing, is most relevant for our understanding and simpler to analyze than perpendicular noise. Using the Bloch vector formulation the Schrondinger equation can be rewritten,

$$\dot{\vec{M}} = -\varepsilon(t) M_y \hat{x} + \varepsilon(t) M_x \hat{y} + 0\hat{z}. \tag{3.5}$$

Note that M_z remains unaffected by longitudinal noise and is conserved, this makes intuitive sense as we expect pure dephasing to affect the Bloch vector in the x-y plane only. To see this decay we will have to examine the average over the stochastic process $\varepsilon_{noise}(t)$. It is convenient to rewrite the Schrodinger equation in terms of the x-y components of $\vec{M}$ only which can be neatly done, by defining $M_{xy} = M_x + iM_y$. Then we have evolution governed by $\dot{M}_{xy} = i\varepsilon(t) M_{xy}$ with the solution,

$$M_{xy}(t) = e^{i\phi_0(t)+i\phi_{noise}(t)}M_{xy}(0), \phi_0(t) = \int_0^t \varepsilon_0(t),$$
$$\phi_{noise}(t) = \int_0^t \varepsilon_{noise}(t). \tag{3.6}$$

Averaging over the stochastic process $\varepsilon_{noise}(t)$ yields,

$$< M_{xy}(t) >= e^{i\phi_0(t)} < e^{i\phi_{noise}(t)} > M_{xy}(0). \tag{3.7}$$

Now we make the assumption that the noise is Gaussian and that the integration time t is significantly longer than the correlation time of $\varepsilon_{noise}(t)$. In this case the integral for $\phi_{noise}(t)$ is a sum of random elements; then according to the central limit theorem such a sum has a gaussian distribution. This allows us to rewrite,

$$< e^{i\phi_{noise}(t)} >= \int \frac{1}{\sqrt{2\pi < \phi^2_{noise} >}} e^{\frac{-\phi^2}{2<\phi^2_{noise}>}+i\phi} d\phi = e^{-<\phi^2_{noise}>} \tag{3.8}$$

where,

$$< \phi^2_{noise} >= \int_0^{t_1} dt_1 \int_0^{t_2} dt_2 S_\varepsilon(|t_1 - t_2|). \tag{3.9}$$

Here S_ε is the correlation function of $\varepsilon_{noise}(t)$, which when rewritten as its fourier transform, $S_\varepsilon(\omega)$, represents the power spectral density of $\varepsilon_{noise}(t)$. Then we have,

$$< \phi^2_{noise} >= 2 \int_0^\infty d\omega (\frac{\sin^2(\omega t/2)}{\omega/2})^2 S_\varepsilon(\omega) \tag{3.10}$$

When t is large relative to the operation frequency ε_0 we can make the approximation

$$< \phi^2_{noise} >= 2\pi t S_\varepsilon(0) \tag{3.11}$$

Then $T_2^* = 1/(\pi S_\varepsilon(0))$. This is interesting for a few reasons, first, in the case of 1/f noise, $S_\varepsilon(0) \to \infty$ meaning the integral diverges and this analysis falls apart. However, it does highlight an important point, that pure dephasing is heavily dependent on low frequency noise and further that characterizing low frequency charge noise provides a useful metric for comparing charge noise between devices.

3.2 Comparison of Low Frequency Charge Noise in Identically Patterned Si/SiGe and Si/SiO2 Quantum Dots

3.2.1 Introduction

Research on laterally gate defined semiconductor quantum dot has largely been confined to GaAs[HPT07] and more recently Si/SiGe and Si/SiO2 heterostructures[ZDM13]. As previously discussed, silicon based quantum dots provide several potential advantages over other platforms including a long electron spin coherence lifetime due to a small Overhauser field[MBH12, HRX14, PSS12, PTD12, SPV11] and well developed fabrication techniques and facilities due to its ubiquity in modern semiconductor technology. However, coherence of electrically controlled qubits in silicon, particularly for exchange based qubits, is susceptible to charge noise, which can create fluctuations in both qubit energy levels and orbital motion of electrons[Sak81, CZ13, PGF14, RMA16, MMN16].

Charge noise in semiconductor quantum dots generally exhibits a $1/f$ noise spectrum, which originates from defects and impurities at both heterostructure interfaces and within the semiconductor's bulk that periodically trap electrons resulting in fluctuations in the potential landscape[LDH94, KCA01]. When deviations from $1/f$ oc-

cur they are generally the result of a fluctuator in close proximity to the quantum dot. Such a system produces a Lorentzian noise spectrum but was not observed in this experiment. We chose to study Low Frequency noise in particular for a few reasons. As demonstrated in section 3.1.5, low frequency noise is the primary contributor to pure dephasing (T_2^*). Low frequency noise is also simple to measure as its $1/f$ spectrum is large at low frequency making measurements simpler and more forgiving. This same $1/f$ spectra also implies that the majority of noise power related charge noise and contributing to decoherence occurs in the Hz to MHz range. This noise has been studied extensively in GaAs for quantum dot and quantum point contact (QPC) systems [LTH90, JFH04, KCT97, BKP08, HFC03, SNN95, LDH94, PPL10, DSL91] and more recently in Si/SiGe[TOF13]. However, such a study has not yet been done for Si/SiO_2 based quantum dots. It has been speculated that Si/SiO_2 may be particularly susceptible to background charge fluctuations relative to other systems, such as Si/SiGe, as the amorphous SiO_2 may give rise a rough interface containing higher defect/impurity density[Sak81, CZ13].

Measurements are further complicated by the fact that measured charge noise depends on a variety of factors, not just the substrate, which makes useful comparisons of charge noise measurements difficult. Aside from the temperature, which plays a large role, fabrication techniques, oxide or spacer thickness, and gate geometry and filtering all have the potential to play a role. To help mitigate these factors we performed charge noise measurements on multiple SiGe and Si/SiO_2 based devices that were fabricated in parallel using the same techniques whenever possible in order to present the best comparative measurement of the charge noise in these two different types of Si-based materials. Notable exceptions include the addition of an oxide etch step for Si/SiO_2 based Ohmic contacts and slightly different annealing

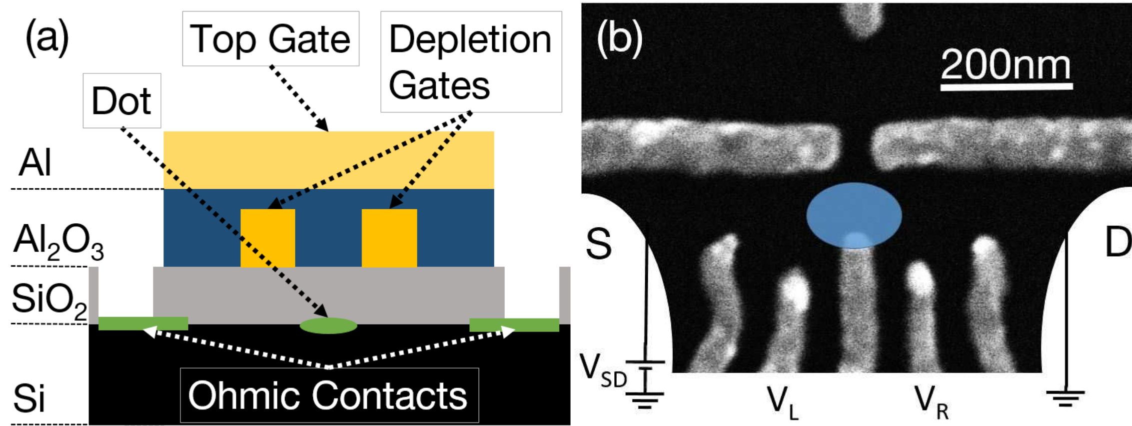

Figure 3.1: (a) Schematic cross section of a Si/SiO_2 device. (b) SEM image of a device with the same depletion gate pattern as the devices used. Note the predicted dot location marked with a blue oval. Depletion gate V_L was used to adjust chemical potential of the dot. The location of the source and drain are marked (S and D). For these measurements a bias, V_{SD}, was applied across the dot.

recipes. However, all depletion gates were fabricated using identical electron beam lithography patterns and processes. Based on our experience fabricating and imaging devices, depletion gate location is accurate to within 10nm of design. Finally, most of the measurements were performed using the same measurement set up in the same dry dilution refrigerator. In this chapter we present several measurements of low frequency charge noise in these Si/SiO_2 and Si/SiGe dot systems using transport measurements.

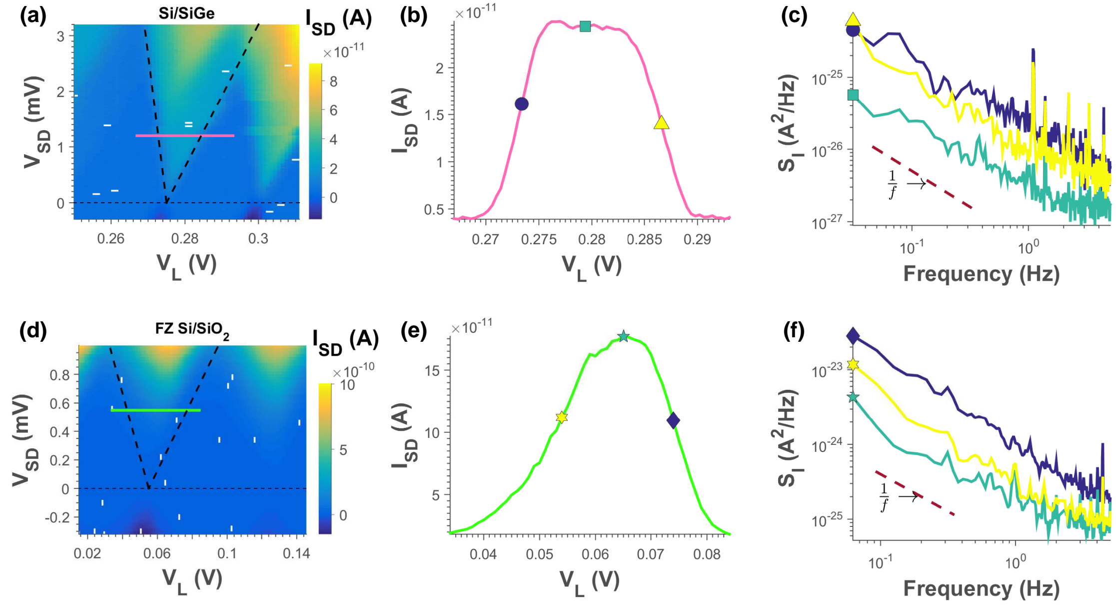

Figure 3.2: (a) ((d)), Coulomb diamond for the Si/SiGe (FZ Si/SiO_2) device, DC current through the dot, I_{SD} is plotted versus the bias voltage, V_{SD} and the tuning gate voltage, V_L. The pink (green) line marks the location of the current trace shown in (b) ((e)). (b) ((e)), I_{SD} current trace across the marked current peak in the Si/SiGe (FZ Si/SiO_2) dot. (c) ((f)) Current noise spectra taken along the current trace. The spectra are color coded to match the markers in (b) ((e)) at the value of V_L where they were taken. Note how the magnitude of the spectra is correlated with $\frac{\partial I_{SD}}{\partial V_L}$. The large peaks above 1 Hz are permanent features due to the pulse tube cooler operating in the refrigerator during measurement.

3.2.2 Device and Measurement Setup

Measurements from four devices are presented in this chapter. Two Si/SiO_2 and two Si/SiGe devices were fabricated and measured. One Si/SiO_2 was fabricated on a lightly boron doped silicon wafer grown using the Czochralski (CZ) process and a second on an un-doped float-zone (FZ) silicon wafer. The purpose of using both CZ and FZ MOS substrates was to examine the possibility of a relation between resistivity, defect density, and measured charge noise. As FZ silicon has a much higher resistivity (>10000 Ω-cm), than the CZ wafers used ($\sim$20 Ω-cm) any large differences in charge noise power should be observable. Both Si/SiO_2 devices have 20nm of thermally grown oxide. The Si/SiGe devices were fabricated on the same substrate consisting of a 16nm silicon well, a 40nm $Si_{.7}Ge_{.3}$ spacer and a 2nm Si cap. All devices were fabricated by first patterning Ti/Au depletion gates on the substrate. Following this 100nm of Al_2O_3 was grown using atomic layer deposition to provide an insulating layer. Finally, a 300nm global top gate was patterned over the device area. Figure 3.1 shows a schematic cross section view of the Si/SiO_2 devices, as well as a scanning electron microscope (SEM) image of the depletion gate layout used on all devices. The electrical confinement potential is defined by applying appropriate voltages on the depletion gates. Our devices were fabricated with the intention of forming two quantum dots. However, for the purpose of simplifying noise measurements for this experiment all systems were tuned to form one large single dot instead. The predicted single dot configuration is highlighted by a blue circle in Figure 3.1. This location was estimated based on the relative strength of depletion gates. The Appendix presents more details regarding the fabrication processes.

All devices were measured in dilution refrigerators cooled to a base temperature

of approximately 60mK. DC current data in the Coulomb blockade regime were obtained by applying a source drain bias on the order of millivolts. The resulting current was measured after passing through a SR570 low noise current amplifier. Noise spectra were obtained using a SR785 spectrum analyzer.

3.2.3 Transport Measurements

To acquire low frequency noise data from our systems, we first tuned to a region where the device behaves as a single dot in the Coulomb blockade regime. Subsequently all data were taken modifying only the bias voltage across the dot, V_{SD}, or the voltage on gate V_L, used to adjust the chemical potential of the dot's energy levels, ϵ. The lever arm α of the gate V_L, which relates $V_L \alpha = \epsilon$, and charging energies were extracted from Coulomb Diamond measurements where current, I_{SD}, is measured through the dot relative to V_{SD} and V_L, a sample trace can be seen in Figure 3.2[KMM97]. These values are reported in Table I.

Low frequency current noise spectra up to 5 Hz, constrained by the bandwidth of our high sensitivity current amplifier, were recorded with a fixed bias as a function of V_L across several peaks in I_{SD}. The spectra and corresponding DC current across a single peak are shown in Figure 3.2 for both substrates. Note the $1/f$ frequency dependence of the data. The predicted shot noise of our device at the maximum DC current measured, ˜200pA, is 6×10^{-29} A^2/Hz, well below the observed noise floor in both systems. Figures 3.2 and 3.3 demonstrate that the noise level is largest on the sides of the current peak and exhibits a local minimum near the maximum value of current. As previous experiments have observed we confirm that, the noise level is strongly correlated with trans-conductance $dI/d\epsilon$ and exhibits a local minimum

at the peak of the current profile[JFH04]. Given that the maximum current through the dot is set by tunneling rates to the source and drain, Γ_S, and Γ_D respectively, and is observed to be relatively constant over a single current peak, we approximate the noise due to fluctuations in Γ_S, Γ_D and ϵ as uncorrelated. Then, to first order, small current fluctuations in time about a fixed point $(\epsilon_0, \Gamma_{S0}, \Gamma_{D0})$ are given by,

$$\delta I(t) = \frac{\partial I}{\partial \epsilon}\delta\epsilon(t) + \frac{\partial I}{\partial \Gamma_S}\delta\Gamma_S(t) + \frac{\partial I}{\partial \Gamma_D}\delta\Gamma_D(t) + \frac{\partial I}{\partial V_{SD}}\delta V_{SD}(t). \tag{3.12}$$

As has been previously observed the strong correlation of noise with transconductance indicates that the majority of noise is due to fluctuations in ϵ as opposed to tunneling[JFH04, DSL91]. Also of note is the final term, the contribution of bias noise to the systems current noise. Unfortunately this term was overlooked during the initial analysis and publication[FSJ16]. Measurements of $\frac{\partial I}{\partial V_{SD}}$ were not performed during the collection of current data, however, based on Coulomb diamond plots taken separately on the devices as well as voltage noise spectra we are able to estimate this noise contribution and find this oversight has a minimal effect on the following analyses. In future measurements we perform a differential measurement of $\frac{\partial I}{\partial V_{SD}}$ providing for more accurate results.

In order to isolate the noise in ϵ for comparison with other systems we subtract the spectra measured at maximum I_{SD}, defining $V_L = V_0$ at this location. Since $dI_{SD}(\epsilon)/dV_L$ is 0 at this point, and hence $dI_{SD}/d\epsilon$ as well, the spectra $S_I(V_0, f)$ represents the noise contribution due to fluctuations in tunneling rates as well as any other uncorrelated background noise in our system. Then,

$$\Delta I_\epsilon(V_L, f) = \sqrt{S_I(V_L, f) - S_I(V_0, f)}, \tag{3.13}$$

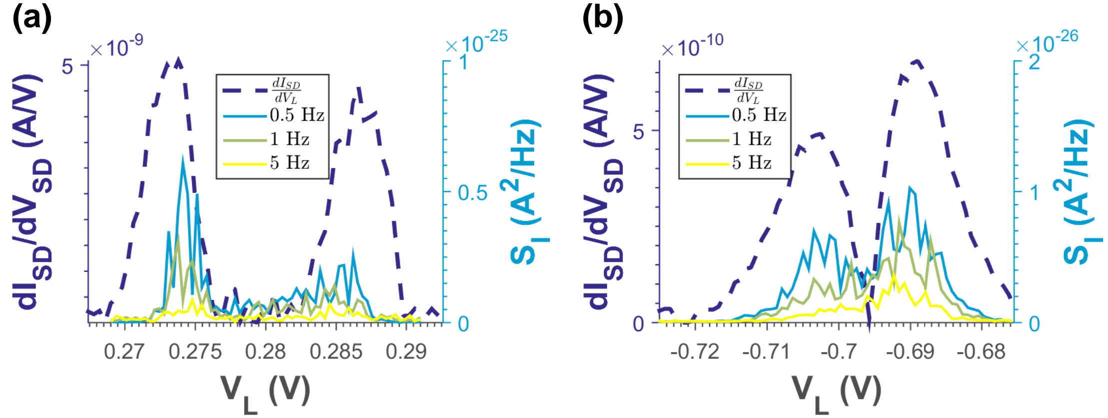

Figure 3.3: Current noise, S_I, as a function of V_L at .5 Hz, 1 Hz and 5Hz plotted versus transconductance dI/dV_L for SiGe (a) and CZ Si/SiO$_2$ (b).

where ΔI_ϵ is the spectral density of current noise due to fluctuations of ϵ only. Finally, since the magnitude of potential fluctuation is small we can use the relation $\Delta I_\epsilon \alpha = |dI_{SD}/dV_L|\Delta\epsilon$ to convert the current noise into potential noise[JFH04]. In order to produce a single spectrum for the charge noise in each device we averaged several points around the peak value of $|dI_{SD}/dV_L|$, where our sensitivity is best. The resulting spectra are consistent with a $1/f$ model; several example spectra are plotted in Figure 3.4. In order to examine the variability of noise, $\Delta\epsilon$ was measured at a minimum of two Coulomb peaks in each device and the extracted values were found to be consistent within error. Values for $\Delta\epsilon$ at 1Hz are reported in Table I; these final values were obtained by averaging all measurements on each device. The lowest observed noise was in the FZ Si/SiO$_2$, $.49 \pm .10\mu eV/\sqrt{Hz}$ at 1 Hz.

Temperature dependence of $\Delta\epsilon$ was measured over several different temperatures between 60mK and 500mK in one of the SiGe devices as well as the CZ Si/SiO$_2$ device. The standard $1/f$ noise model assumes an even spatial distribution of electron

traps and activation energies. This model gives rise not only to a $1/f$ frequency dependence, but also to a temperature dependence of the following form[JFH04, DSL91].

$$S \propto \frac{kT}{f} \tag{3.14}$$

Temperature dependence of measured potential fluctuations across a single Coulomb peak are plotted in Figure 3.5 for the CZ Si/SiO_2 and a SiGe device. Temperature dependence is observed in both the Si/SiGe and the Si/SiO_2 systems. The measured temperature dependence is consistent with a linear model, although more detailed measurements could reveal nonlinearities. There are several practical considerations that could explain a departure from the expected linear dependence. In particular, the effective electron temperature is likely higher than the measured base temperature of the device. This should create a region of nonlinearity in the measured $1/f$ noise versus temperature at low temperatures as the electron temperature does not depend linearly on the measured lattice (refrigerator) temperature. Alternatively, it has been suggested that for a regime in which several states contribute to the total current through the device relaxation of conduction electrons within the device may enhance $1/f$ noise by transferring energy to nearby impurities[JFH04, KCA01]. If such a processes contributed substantially to potential fluctuations, temperature dependence could depart from the expected form. However, we find this unlikely as measurements taken at several bias voltages between .5mV and 1.5mV did not show any clear signs of bias dependence.

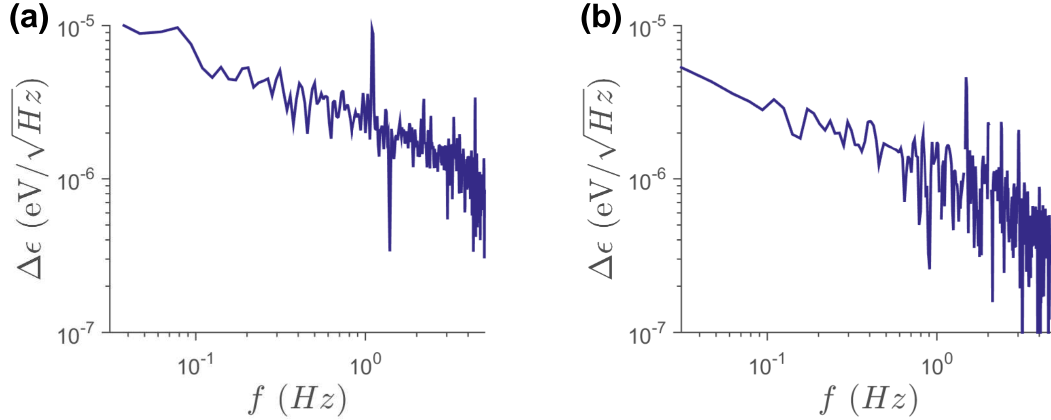

Figure 3.4: Potential energy fluctuations calculated by averaging several points near the maximum value of transconductance for SiGe (a) and CZ SiO_2 (b).

3.2.4 Findings

We fabricated several identically patterned Si/SiO_2 and Si/SiGe quantum dot systems and measured low frequency charge noise in order to make a direct comparison between substrates. Noise was measured using transport data through single quantum dots operating in the coulomb blockade regime. Noise measurements at separate current peaks on the same device were found to be similar. Temperature dependence of both systems was also examined and observed to be consistent with standard $1/f$ noise models. The measured charge noise in both Si-based materials was found to be roughly the same order of magnitude. Therefore, measured noise from our Si/SiO_2 devices compares favorably with our measurements of Si/SiGe as well as with previous measurements of low frequency noise in GaAs systems[BSJ14], demonstrating that low frequency charge noise in Si/SiO_2 quantum dot systems is low enough to support spin qubits for quantum information processing. This finding is somewhat

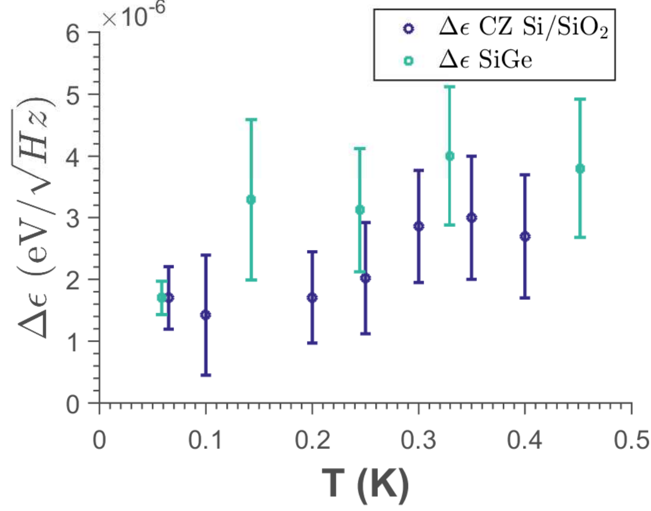

Figure 3.5: Temperature dependence of measure potential energy noise at $1Hz$ across a single Coulomb peak for the CZ Si/SiO$_2$ device and a Si/SiGe device.

surprising since it has been observed that charge impurities in Si/SiO$_2$ devices, tend to have a strong effect on dot locations and tunneling rates from device to device. It is possible that the majority of charge impurities are much deeper in energy and contribute little to charge noise. In fact, we have observed that, once cooled, dot formation on Si/SiO$_2$ devices remains stable but can be difficult to modify via control gate voltages. This suggests that the impurities affecting dot formation might have large activation energies and may be treated as fixed charges.

3.2.5 Outlook

Following the publication of these results several groups have had success with qubit systems in Si/SiO$_2$ [ZHC17] substantiating our results, but several challenges remain in the development of Si/SiO$_2$ based qubits. In particular the relatively large number

Sample	$\Delta\epsilon\ \mu eV/\sqrt{Hz}$	$\alpha\ eV/V$	$E_C\ meV$
CZ Si/SiO_2 BE5	$1.70 \pm .43$	0.03	1.3
FZ Si/SiO_2 AF5	$0.49 \pm .10$	0.01	0.7
Si/SiGe AB3	$2.0 \pm .23$	0.02	1.7
Si/SiGe AC2	$2.1 \pm .24$	0.09	2.5

Table 3.1: Summary of device measurements. The $\Delta\epsilon$ value is reported at $1Hz$ for every device as well as the lever arm α and the charging energy E_C.

of defects that affect dot formation and make tuning devices difficult. There is some evidence that these defects may in part be caused by exposure to high energy electrons used to pattern the depletion gates during electron beam lithography[KTL17]. To tackle this problem our lab is spearheading an effort to fabricate quantum dot devices use nano imprint lithography as an alternative to electron beam lithography. Repeating noise measurements on these devices should provide insight into the origin of these traps.

While Si/SiGe's crystalline structure is less susceptible to damage due to electron beam lithography we are still interested in continuing noise characterization of Si/SiGe devices. Accumulation mode gate architectures are currently gaining popularity in the field relative to the depletion mode devices measured here. These devices are significantly more complicated to fabricate than depletion mode devices, requiring alignment on the order of nanometers throughout multiple electron beam lithography steps, but provide improved tunability. Our lab is currently in the process of developing an accumulation mode recipe and planning to perform comparative noise measurements on those devices, similar to the measurements presented here.

Accumulation mode architecture is discussed in more detail in Chapter 6.

CHAPTER 4

Observation and Characterization of a Si/SiGe Based Valley Qubit

4.1 Introduction to Valley Qubits

4.1.1 Valley Degree of Freedom in Silicon

Bulk silicon possesses an indirect bandgap, such that the top of the valence band lies along a different crystal momentum direction than the bottom of the conduction band[Dav98]. This band structure is shown in Figure 4.1; note how the top of the valence band lies along the Γ direction while the bottom of the conduction band lies about 85% of the way to the X direction. These minima lie along (100) "like" directions of the bulk silicon crystal of which there are six and are often referred to as valleys[Dav98].

While the bulk valley states are six fold degenerate, when a silicon heterostructure is used to form a 2DEG the degeneracy is lifted. When an interface is formed along the (100), direction as in our quantum dot systems, the 6 fold valley is split into a low energy 2 fold degeneracy and a high energy 4 fold degeneracy[Dav98]. It is this lower two fold degeneracy that, as we shall see is important for Si based quantum dots.

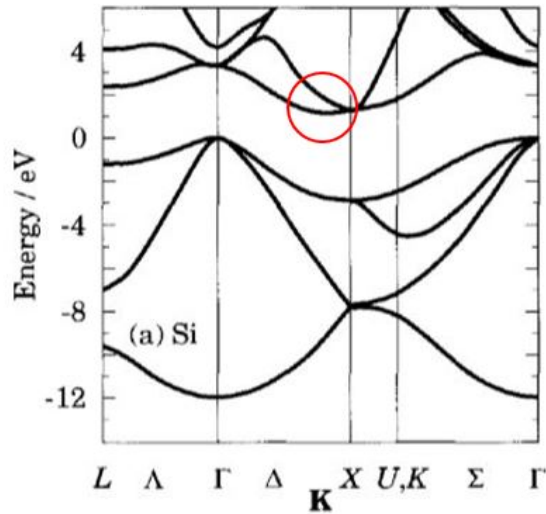

Figure 4.1: Band structure in 3 dimensions for Silicon. Note the indirect bandgap and the valley minima (circled in red).

In practice the low energy 2 fold degeneracy is split again; from here forward, when I refer to valley splitting, this is the energy splitting that I am referring to. The splitting of the 2 fold degeneracy arises from the atomic scale disorder at the interface[YRR13, CSK12, ZLS13, HRX14]. The valley splitting affects electrons confined in quantum dots by adding an additional quantum degree of freedom beyond spin and orbital. As we shall see, the existence of a valley state is a nuisance for many exchange interaction based qubit implementations[ZDM13], but also provides an opportunity to develop a new type of qubit based on the valley degree of freedom itself.

4.1.2 Valley Qubits in Silicon

Although there are multiple potential implementations of a valley-state based qubits, the version described here is based on experiments performed in our lab that resulted in the first definitive observation of a valley qubit.

Our valley qubit is realized in a double quantum dot system with an asymmetric valley splitting. Let us consider for example the case where the left dot has a small valley splitting and the right dot has a large splitting. Then for the purposes of this analysis we can ignore the valley splitting in the right dot. A single electron in this system has 3 states available to it, $|R\rangle$, $|L_{v1}\rangle$ and $|L_{v2}\rangle$. In this basis, the Hamiltonian can be written as follows:

$$H = \begin{bmatrix} \frac{\epsilon}{2} & \Delta & \Delta_e \\ \Delta & -\frac{\epsilon}{2} & 0 \\ \Delta_e & 0 & -\frac{\epsilon}{2} + \delta \end{bmatrix} \tag{4.1}$$

Here ϵ is the energy difference between the $|R\rangle$ and $|L_{v1}\rangle$ states, a parameter that is under our control via depletion gate voltages. Δ and Δ_e are couplings between $|R\rangle$ and $|L_{v1}\rangle$ or $|L_{v2}\rangle$ respectively.

The energy spectrum as a function of detuning is plotted in Figure 4.3b. For the purposes of operation, consider the right dot as the initialization and readout dot and the left dot as a the operation dot. First, the electron is allowed to relax at large negative detuning, ϵ_0 placing it into the state $|R\rangle$ The detuning is then pulsed from negative detuning to positive detuning. This pulse passes the system through two avoided level crossings. The first of which is with the $|L_{v1}\rangle$; this crossing should be passed adiabatically such that the system remains in the ground state, which is

now $|L_{v1}\rangle$. The second avoided crossing is with $|L_{v2}\rangle$; this transition is non-adiabatic and results in a both θ_{load} and ϕ_{load} rotation in the Hilbert space spanned by $|L_{v1}\rangle$ and $|L_{v2}\rangle$. The system then spends a period of time accumulating phase, $\Delta\phi$, and the process is reversed as the detuning returns to ϵ_0. Depending on the rotations performed and thus, the details of the pulse, the qubit will either return to $|L_{v1}\rangle$ or $|R\rangle$. Readout is then performed by a charge sensing measurement. This entire process is detailed in Figure 4.3.

The key take away is that, in the operational basis $|L_{v1}\rangle$, $|L_{v1}\rangle$ we have arbitrary θ control by adjusting the rise time of the pulse and ϕ control by adjusting pulse width, giving us the two axis control necessary to form a functional qubit. But, the valley qubit is more than just a novelty, it has several very appealing features.

First and likely most important is the valley qubits resistance to charge noise. Charge noise has been discussed at length in the previous chapters, but its primary deleterious effect is fluctuations in the detuning of a quantum dot system. As the rate of phase accumulation in the system is determined by the energy splitting systems in which the energy splitting is a strong function of epsilon will also be subject to strong dephasing due to charge noise. Here, the valley qubit really shines as in the phase accumulation stage of operation $E_{v2} - E_{v1} \sim \delta$ and $\frac{d(E_{v2}-E_{v1})}{d\epsilon} \sim 0$ minimizing the effect that charge noise. The valley qubit also benefits from a fairly simple fully electrical control, with no magnetic field required as while as a wide range of potential operation frequencies.

Previous work has demonstrated a similar system in the three state hybrid qubits based on the spin degree of freedom[KSS14, SSW14, CLY16]. These hybrid qubits share many properties with valley qubits, including a large detuning region of charge

noise resistance. In fact they are often modeled with an identical Hamiltonian making it potentially difficult to differentiate between the two systems. However, in the sections that follow I will present the first ever definitive observation of a valley qubit, which was performed in our lab.

4.2 Characterization of a Valley Based Qubit

4.2.1 Introduction and Motivation

As discussed in the previous sections, understanding the valley degree of freedom is essential not just for the development of valley qubits, but for the implementation of any silicon based quantum computing platform. It is particularly important, however, for exchange based qubits that rely on Pauli spin blockade for readout, as a small valley splitting will prevent the blockade by providing a nearly degenerate energy level. Small valley splittings are difficult to measure with traditional magnetospectroscopy techniques. This provides additional motivation for studying valley qubits, as it provides a means of measuring valley splittings in silicon devices without using magnetospectroscopy.

Here, we report the coherent manipulation of a qubit based on the two valley states of an electron confined in a silicon quantum dot. Coherent evolution between the states that have a relatively small energy splitting of 20 μeV is excited by a fast electrical pulse, and the results are projected as the occupations of two different charge states for read-out by a nearby charge-sensing channel. Additionally, we carry out the valley qubit operations at multiple charge configurations of the double quantum dot device.

The dependence of coherent oscillations on pulse excitation level and duration allows us to map out the energy dispersion as a function of detuning as well as the phase coherence time of the valley qubit. The energy structure of the valley qubit is similar to spincharge hybrid qubits and it shares a desirable resistance to charge noise[KSS14, SSW14, CLY16]. The experiment shows that the valley states being manipulated are good quantum numbers.

4.2.2 Device and Setup

Measurements were performed on a device similar to the device in Figure 4.2a. Although the device is distinct from any of those for which noise measurements were performed in Chapter 4, it is of the same design, with an identical gate pattern and fabrication procedures. Additionally, the device was fabricated on the same Si/SiGe substrate as the devices in Chapter 4, consisting of a 16nm Si well, a 40nm $Si_{.7}Ge_{.3}$ spacer and a 2nm Si cap.

Measurements were performed at 40mK in a Triton 200 dry dilution refrigerator. The electron occupation of the dots was measured by the use of a nearby charge sensing channel. This type of sensing channel is referred to as a quantum point contact (QPC). The conductance of the QPC depends strongly on the occupation of the nearby quantum dots. A small bias voltage is applied to the channel and the current through the QPC channel is measured. The signal is enhanced by applying a small ($\sim$1mV) oscillating voltage to one of the depletion gates, while a differential current measurement is performed at the same frequency using a lockin amplifier. When the voltage configuration is such that the oscillating voltage will tend to repeatedly add and remove an electron from one of the dots, a strong signal is measured at the

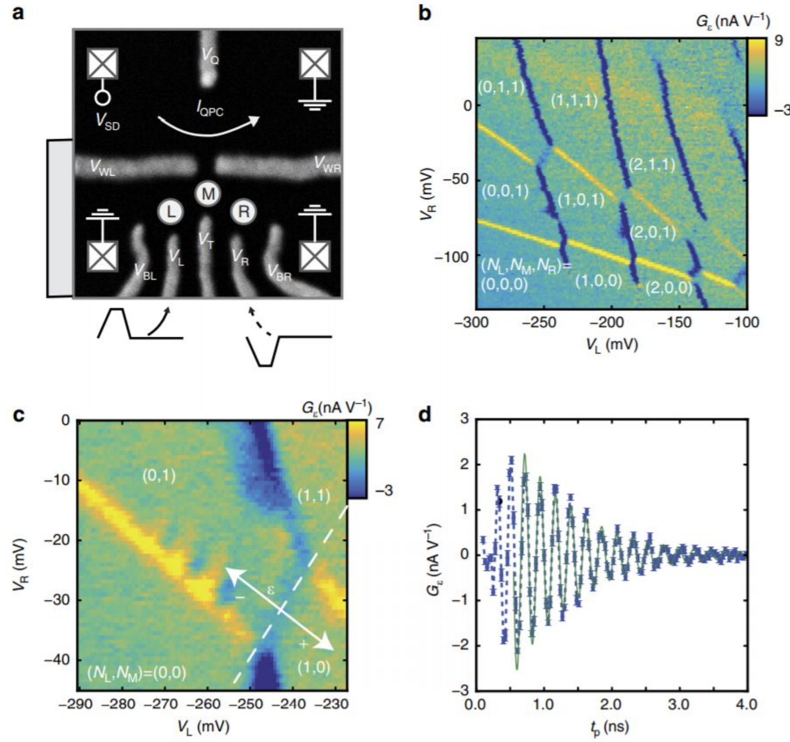

Figure 4.2: **(a)** A scanning electron micrograph of the quantum-dot-forming region in a lithographically identical device: The three circles represent the estimated location of three dots. The squares represent ohmic contacts. Note the presence of the QPC charge sensing channel above the dot system. The grey scale bar pictured at left represents 500 nm. **(b)** Example charge stability diagram for our system taken using QPC charge sensing. Note that the system is actually a triple dot although the valley qubit behavior is observed between the left and middle dots. **(c)** Stability diagram of the (1,0,1) ↔ (0,1,1) transition under the influence of a 500 ps square pulse with an amplitude of +30 mV on VL. The 0 detuning line is shown as a dotted line and the detuning axis is shown as a solid arrow. **(d)** Time domain oscillations: Fixing V_L and V_R at values within the interference region and fixing the pulse height at +24 mV, the width of the square pulse is varied, resulting in an oscillatory average charge occupation. Error bars are the one standard deviation range for that data point as taken over 10 averages. Also shown is a fitted decaying sinusoid used to extract a frequency (4.41 0.01 GHz here) and decay time (0.90 0.04 ns), the latter of which serves as a lower bound on T_2*. A moving average with a window of several periods of the oscillation has been subtracted prior to fitting to counteract pulse duty cycle effects

lockin. When scanning over depletion gate voltages this measurement produces a stability diagram like the one shown in figure 4.2b.

As seen in that figure, in the region where valley qubit oscillations were observed the device behaves as a triple dot. The valley qubit system however, consists of only the left and middle dots. A three tuple (N_L, N_M, N_R) will be used to indicate electron occupation number in each dot. As the right dot is largely irrelevant to the valley qubit's operation we will often abbreviate to a pair of numbers (N_L, N_M) and ignore the occupation of the right dot. The Hamiltonian is modeled as in equation 4.1, ϵ is referred to as the detuning and represents the energy difference between the ground states in the left and middle dots. The left dot has a small valley splitting, δ, and serves as the operation dot, while the middle dot has a large valley splitting that can be ignored and serves as the readout dot. Then the discussion in 5.1.2 holds, the only modification being $|R\rangle \rightarrow |M\rangle$ in our particular system. Figure 4.3 presents a detailed picture of operation and readout for our valley qubit.

4.2.3 Observation of Coherent Oscillations

While operating, the system is parked at some V_{L0} deep in the readout dot and a square pulse of pulse height p_h and pulse width t_p is applied to the gate V_L. As ϵ is linearly proportional to V_L up to some constant α, this amounts to fixing the system at ϵ_0 and pulsing in ϵ. While the pulse applied is square, in practice the high frequency lines to the device filter the signal resulting in a pulse with longer rise and fall times, this allows the necessary adiabatic transition through the $|R\rangle$ $|L_v1\rangle$ avoided crossing. Following the pulse, the system sits at ϵ_0 for an extended period of time while the QPC measures charge occupation allowing for qubit readout. When

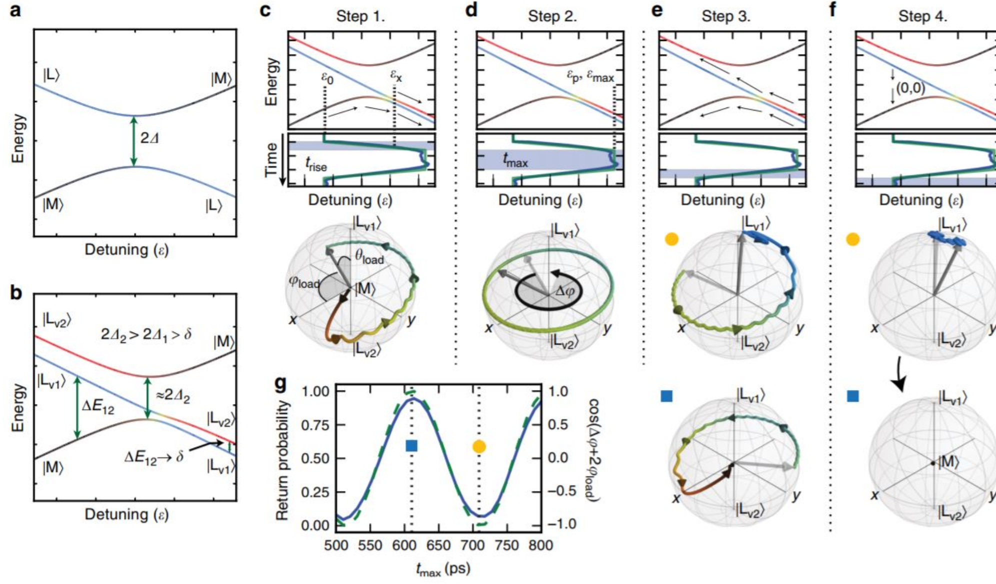

Figure 4.3: **(a)** Two state energy spectra for a traditional charge qubit with tunnel coupling Δ and no valley states. **(b)** Valley qubit energy spectra as a function of ϵ derived from H in Eq. 4.1. **(c)** The first step in pulse exciting a valley qubit, showing the systems position on the spectra, starting at the initialization and measurement point ϵ_0 and moving through the two avoided transitions. This induces both a θ and ϕ rotation θ_{load} and ϕ_{load} respectively. **(d)** The second stage is phase accumulation, the system is parked at a large positive ϵ for a time t_{max} where it performs a ϕ rotation $\Delta\phi$. **(e)** The return stage; similar to during the pulse rise, both θ and ϕ rotations are performed. **(f)** In the final measurement/initialization stage, depending on the paramaters of the pulse the system returns to either $|M\rangle$ or $|L_{v1}\rangle$. Subsequently the system relaxes to $|M\rangle$. **(g)** The simulated probability of the electron returning to state $|M\rangle$ at the end of read-out is plotted along with $\cos \Delta\phi + 2\phi_{load}$ as a function of tmax, showing that the total accumulated phase is encoded in the return probability.

p_h and t_p are scanned they produce stability diagrams with detuning dependent coherent oscillations as shown in Figure 4.4.

Using these results we are able to present estimates of all parameters in the Hamiltonian, Eq.4.1 as well as extract a lower bound on T_2*. While a more detailed discussion of parameter extraction follows in the next chapter regarding the development of my GPU simulation platform, the extraction of T_2* bounds is quite simple. The lines of fixed p_h as a function of t_p produce sinusoids that decay exponentially with a characteristic time that represents the bound on T_2*.

Note the ϵ dependence of T_2*; this is a confirmation of the existence of a charge noise resistant region at larger positive detunings. This dephasing is consistent with being proportional to d$\frac{d(E_{v2}-E_{v1})}{d\epsilon}$ as shown in Figure 4.5 at least for values of ϵ_p below 400μeV. Measured values of T_2* are also shown and generally lie in the range of .5-1.5ns depending on the value of ϵ. Note that beyond $\sim$400ueV T_2* begins to decay not increase as might be expected due to the dispersion. We believe this is due to the pulse not being purely in the ϵ direction. If ϵ_p is large enough the system will pulse into the (1,1) region during phase accumulation resulting in a strong dephasing component due to relaxation of the system to the (1,1) ground state.

4.2.4 Estimation of T_2* From Charge Noise Measurements

Using the results of noise measurements and our discussion of dephasing in Chapter 3, we can make a rough estimate of T_2*. Pure dephasing will result from noise in the energy splitting between the operation states, as we are only interested in dephasing during the phase accumulation stage where the operation states are approximately energy eigenstates. Here, $|Lv1\rangle \approx |E_1\rangle$ and $|Lv2\rangle \approx |E_2\rangle$. Now defining $E_{12}(\epsilon) =$

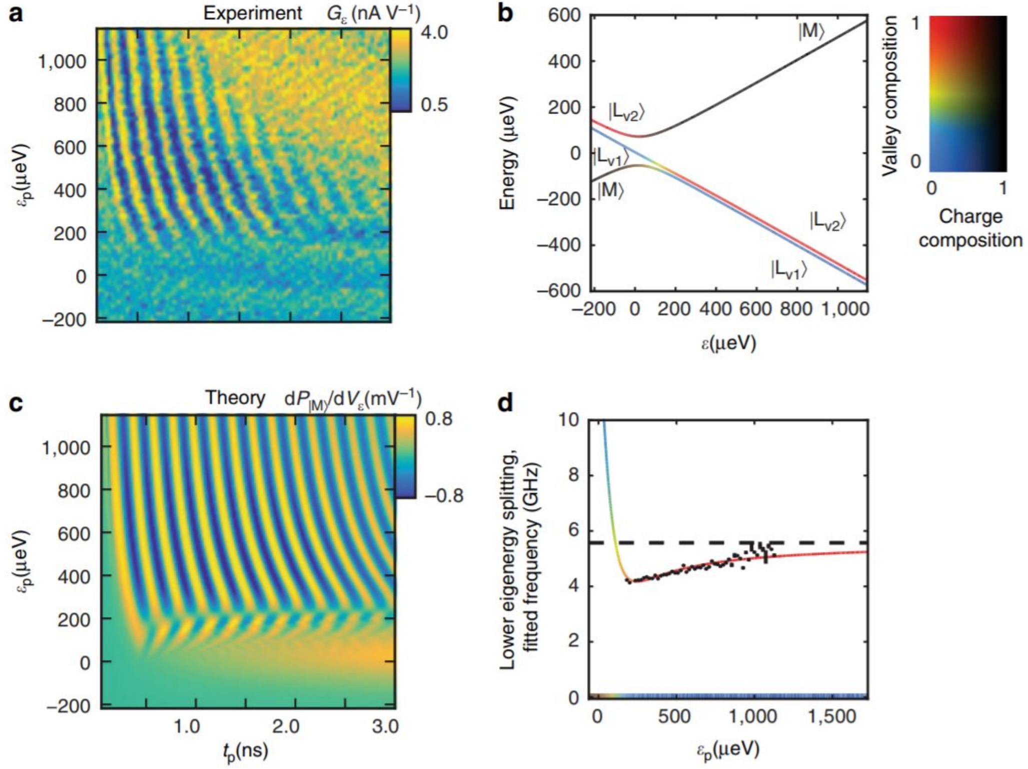

Figure 4.4: **(a)** Pulse detuning (ϵ_p) versus pulse width (t_p), note how the oscillations are only visible in the charge noise protected region. **(b)** Energy spectrum using the extracted couplings and valley splitting. The 2d color bar provides information about the energy eigenstates' makeup in the $|M\rangle, |L_{v1}\rangle, |L_{v2}\rangle$ basis. **(c)** Simulated qubit data using the GPU simulation platform discussed in Chapter 6; a trapazoidal pulse with a rise time of 200ps was used. **(d)** Experimentally extracted frequencies plotted along with the separation between the lower two eigenenergies as a function of detuning: The extracted value of the valley splitting, δ, is plotted as a dotted line. The color of the fitted curve is the color associated with the middle eigenstate at a detuning using the coloring from **b**. Along the bottom axis, the color represents the makeup of the ground state.

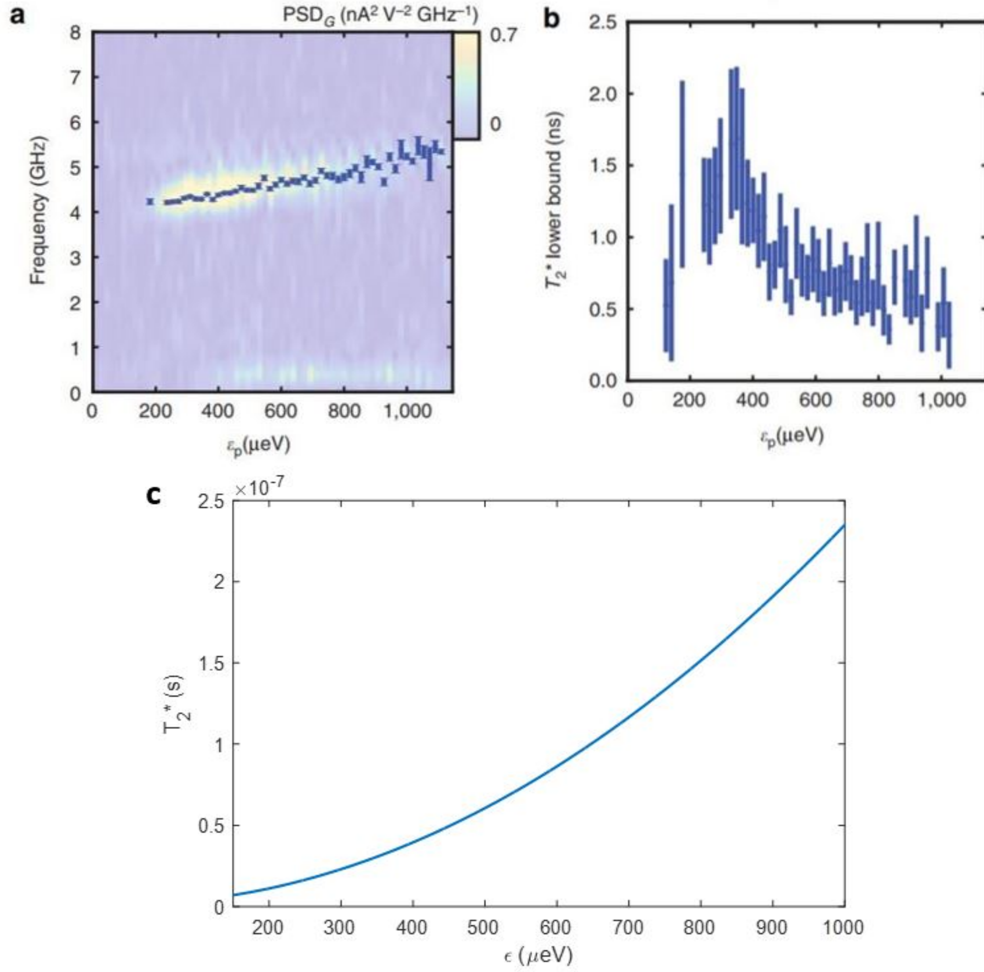

Figure 4.5: **(a)** The dispersion extracted from the transconductance data in Figure 4.4a: The points are the frequencies extracted by applying a decaying sinusoidal fit to each cut in ϵ_p. The background is the magnitude of the power spectral density of those same cuts. **(b)** The extracted values of the decay time from the sinusoidal fit: This value is a lower bound on phase decoherence time T_2*. The decay time increases rapidly at first and then begins to decrease. The longest value directly observed is 1.5 ns. **(c)** Predicted values of T_2* using noise measurements from Chapter 4.

$E_2(\epsilon) - E1(\epsilon)$ where the energy values are calculated by diagonalizing the full 3 state Hamiltonian. Treating these two states as a "2-d" system with the following Hamiltonian,

$$H \approx \begin{bmatrix} \frac{E_{12}(\epsilon)}{2} & 0 \\ 0 & -\frac{E_{12}(\epsilon)}{2} \end{bmatrix} \tag{4.2}$$

Recall the discussion of dephasing in Chapter 3 where we calculated $T_2{}^*$ for a spin qubit in a magnetic field with transverse noise. This system is identical and our discussion applies. Making the association $B + b(t) = E_{12} + \frac{\partial E_{12}}{\partial \epsilon}(\epsilon)\epsilon_{noise}(t)$ we are left with the following Hamiltonian,

$$H \approx \begin{bmatrix} \frac{E_{12}(\epsilon)}{2} + \frac{\partial E_{12}}{\partial \epsilon}(\epsilon)\frac{\epsilon_{noise}(t)}{2} & 0 \\ 0 & -\frac{E_{12}(\epsilon)}{2} - \frac{\partial E_{12}}{\partial \epsilon}(\epsilon)\frac{\epsilon_{noise}(t)}{2} \end{bmatrix}. \tag{4.3}$$

Then from our discussion of dephasing in Chapter 3 we have,

$$\langle \phi^2(t) \rangle = 2\int_0^\infty d\omega \Big(\frac{\sin\frac{\omega t}{2}}{\omega/2}\Big)^2 S_\epsilon(\omega) \tag{4.4}$$

Now using our results from Chapter 4 we know the power spectral density of ϵ,

$$S_\epsilon(\omega) = \frac{2\pi(\Delta\epsilon)^2}{\omega} \tag{4.5}$$

Now this gives rise to two problems; first recall that for long timescales we used the identity $\lim_{t\to\infty} \sin^2(t\omega/2)/\pi t(\omega/2)^2 = \delta(x)$ to get the result $T_2{}^{*-}1 = \pi S_\epsilon(0)$. Now as discussed previously things, start to fall apart for a $1/f$ noise spectrum as the result diverges, so let's consider which parts of the noise spectrum are essential to understand our results. Our lockin collects results averaging for a characteristic time

of $.3s$, thus it is unlikely that fluctuations below $3Hz$ will contribute to dephasing. Additionally fluctuations faster than the repetition rate, $33MHz$ will average out and produce minimal dephasing. Our second problem is that the identity used to simplify the integral is not valid on the timescales we are interested in. Consider that within the restricted frequencies using our longest observed T_2*$= t = 2ns$ and our largest frequency $\omega \approx 200e6$ rad/s we get $t\omega/2 = .2$. This is small enough that we will approximate $\sin(t\omega/2) \approx t\omega/2$ for the purpose of this back of the envelope calculation. This leaves us the following integral,

$$\langle \phi^2(t) \rangle = t^2(\Delta\epsilon)^2 \int_{2\pi*3Hz}^{2\pi*22MHz} d\omega \frac{4\pi}{\omega} \approx 200 * t^2(\Delta\epsilon)^2 \tag{4.6}$$

Interestingly, this produces a result suggesting that dephasing may decay like e^{-t^2} as opposed to e^{-t} at shorter timescales. In anycase, we can still extract a characteristic time, using the result $\Delta\epsilon = 2\mu\text{eV}/\sqrt{Hz}$ from Chapter 4 and multiplying it by the factor $\frac{\partial E_{12}}{\partial \epsilon}(\epsilon)$ as in Equation 4.3. This produces an estimate of T_2* at each value of ϵ within the phase accumulation region. The results are plotted in Figure 4.5 and range from around 10ns at $\epsilon = 200ueV$ to 240ns at $\epsilon = 100$ueV.

This estimate is about an order of magnitude too large in the range $200\mu eV < \epsilon_p < 400\mu eV$ which, as previously discussed, is the range that the system remains in the (1,0) state during phase accumulation. The discrepancy is plausible for a variety of reasons; most importantly there are several sources of noise in addition to 1/f not accounted for in our estimation, for example shot noise from the nearby QPC. Additionally, $\Delta\epsilon$, which varies from device to device, was not measured on this particular sample. Ultimately the result is close enough to suggest that, as predicted, charge noise is likely the primary source of dephasing in our system.

4.2.5 Discussion and Conclusions

As there are other qubit systems with similar energy dispersions (in particular the spin-charge hybrid qubit), it is essential to verify that what we are seeing is in fact a valley state based qubit, not one that relies on spin or orbital states. The strongest evidence that this qubit is indeed a valley qubit comes from the observation of qubit behavior at consecutive anticrossings. We are able to reproduce the results seen in a (1,0)-(0,1) configuration in a (2,0)-(1,1) configuration. Such behavior is unlikely to be spin state based. The reproduced qubit behavior also maintains a very similar dispersion and valley splitting δ, which is in line with the prediction that the valley orbit coupling is unaffected by the occupation of the dot[JYP13]. Finally we are able to rule out orbital states as the energy splitting δ is simply too small. An electron confined within a 40nm well would have a first excited state lying .4meV above the ground state, an order of magnitude too large.

Given this evidence we are confident that we have observed and characterized the first verified valley qubit. Understanding and characterizing valley splittings on Silicon based qubits is important as most favored implementations, especially those based on exchange interaction relay in spin to charge conversion via Pauli blockade for readout[ZDM13], as a small valley splitting prevents Pauli blockade. As valley splittings in Silicon are often below the threshold for characterization using magnetospectroscopy using valley qubit characterization provides a means of measuring valley splittings in Silicon devices that would otherwise be unmeasurable.

Finally, valley qubits themselves could provide an appealing means of qubit implementation. Their charge noise resistant nature and fast operation are appealing, but many obstacles remain. In particular valley qubit splittings seem to vary sub-

stantially over devices even those fabricated on the same substrate.

CHAPTER 5

Efficient Simulation of Qubits and Qubit Dephasing for Quantum Dot Systems

5.1 Building a versatile Louisville GPU simulation platform

The density matrix formulation of quantum mechanics lends itself naturally to simulating qubits. As is the case with the QPC charge sensing channel in the previous subsection, measurements often directly represent an average return probability over many runs. Unlike in most traditional systems where the density matrix formulation represents an ensemble of many individual particles, in our case we shall use it to represent a statistical ensemble of the same system over many identical control sequences. The impetus for developing a user friendly and versatile simulation suite was born out of a desire to understand several strange oscillations first observed in one of the earliest MOS quantum dot devices I fabricated. While I was never able to understand these particular oscillations, over time the project evolved into a fast and flexible simulation suite for the lab.

As we have seen previously, the scanned data we observe using a differential QPC measurement amounts to the (unnormalized) derivative of a probability distribution. This distribution represents the average probability of an electron being in the left

or right dot over an extended period of time subject to a set of variables. Generally two of these variables are modified and scanned to produce a 2d plot. So the requirements of our simulation platform are as follows: Allow simulation as a function of parameters commonly modified during qubit experiments. Allow simulation under the influence of an arbitrary pulse shape. Allow simulation of systems of arbitrary dimension. Finally, the simulation should be completed in a reasonable amount of time.

It quickly became clear that it would be impossible to meet the time requirement using standard personal computer CPU computing. Fortunately, as each data point in a 2d scan represents an independent calculation these simulations are easily parallelizable. Moving these simulations to a modern computer gaming graphics processing unit (GPU) has proven to be a convenient and economical solution that produces results within a reasonable timescale even for larger Hamiltonians (we have simulated up to 9x9). Although designed for the rapid manipulation of computer graphics and image processing, GPUs possess a highly parallelized architecture with hundreds or even thousands of independent processing cores which lends itself well to processing parallelizable simulations such as the qubit simulations we wish to perform.

Matlab's parallel computing package allows parallel processing on a CUDA based GPU via the Matlab function arrayfun(). Unfortunately arrayfun() has several restrictions regarding the functions it will parallelize and most existing Matlab functions are not supported. This required independent development of several functions designed to run on the GPU, including a fourth order Runge-Kutta ODE solver. In the first iteration of my simulation suite, an initial density matrix is evolved using the quantum Louisville equation,

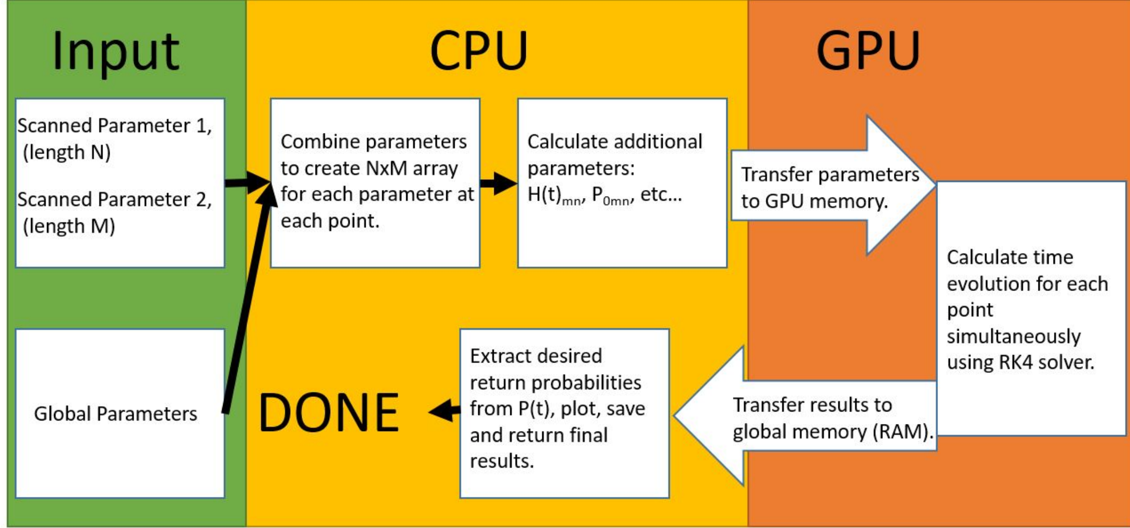

Figure 5.1: Graphical outline of the steps in a GPU simulation.

$$\frac{\partial\rho}{\partial t} = \frac{1}{i\hbar}[H, \rho] \tag{5.1}$$

The basics of the simulation are laid out in Figure 5.1.

While this simulation is useful for understanding our systems and even extracting parameters it fails to capture many of the dynamics of a real qubit. In particular, it cannot reproduce any dephasing or relaxation effects as the Louisville equation produces only unitary transformations on a density matrix. In order to include these effects we must turn to the Lindblad master equation.

5.2 Lindblad Master Equation and Dephasing

To introduce dephasing into our simulations we require something more than the Liouville equation, $\frac{\partial\rho}{\partial t} = \frac{1}{i\hbar}[H, \rho]$, which provides for only the unitary evolution of

our system. To include relaxation and dephasing we require a non unitary extension of the Liouville equation, the Lindblad master equation. The Lindblad master equation is the most general Markovian master equation providing for density matrix evolution. The Lindblad equation is trace-preserving and completely positive. In its most general form the Lindblad equation for an N-dimensional system takes the following form,

$$\frac{\partial\rho}{\partial t} = \frac{1}{i\hbar}[H,\rho] + \sum_{n,m=1}^{N^2-1} h_{nm}\Big(A_n\rho A_m^\dagger - \frac{1}{2}\left\{A_m^\dagger A_n,\rho\right\}\Big) \tag{5.2}$$

Here, A_n are an arbitrary orthonormal basis of the operators that act on the system's Hilbert space. The coefficients h must form a positive semi-definite matrix in order for the Lindblad equation to be trace-preserving. Now, it is the details of both H and h that will determine the evolution of the density matrix ρ. While it is possible to arrive at theoretical predictions for the matrix h by performing a partial trace over a bath of bosons for instance[PGF14, Qin16], we are more interested in fitting our results and extracting sensible values of T_1, T_2 and T_2*. To do so, let us first examine an arbitrary h in a simple spin 1/2 system. Using the intuition developed there, we can adapt our understanding to the three state hyperqubit system.

We begin with the following Lindblad equation,

$$\frac{\partial\rho}{\partial t} = \frac{1}{i\hbar}[H,\rho] + \sum_{n,m=1}^{3} h_{nm}\Big(\sigma_n\rho\sigma_m^\dagger - \frac{1}{2}\left\{\sigma_m^\dagger\sigma_n,\rho\right\}\Big) \tag{5.3}$$

where the σ_n are the traditional Pauli matrices. After expanding the sum, the results can be recast in the following form,

$$\frac{\partial\rho}{\partial t} = \frac{1}{i\hbar}[H,\rho] - \begin{bmatrix} -\Gamma_{12}\rho_{22} + \Gamma_{21}\rho 11 & \gamma_{12}\rho_{12} \\ \gamma_{12}\rho_{21} & \Gamma_{12}\rho_{22} - \Gamma_{21}\rho 11 \end{bmatrix} \tag{5.4}$$

where $\gamma_{12} = \frac{1}{2}(\Gamma_{12}+\Gamma_{21})+k_{12}$. The matrix in equation 3 will henceforth be called the relaxation matrix, R. Now from examination we can see that in the $\hat{z}$ eigenbasis, Γ_{12} and Γ_{21} represent tunneling to and from the spin +1/2 respectively. In most cases we will prohibit tunneling of a ground state to an excited state, setting $\Gamma_{21} = 0$, then we can make the connection $\Gamma_{12} = \frac{1}{T_1}$. Now let us examine γ_{12} which represents dephasing in the system. Because of the restrictions placed upon us by the Lindblad equation we will always end up with some dephasing due to the relaxation rates Γ. This makes good intuitive sense as a relaxation from one eigen state to another should certainly destroy any coherence. We also have an additional contribution, a pure decoherence term k_{12}. As an ansatz, then, we present the following relations, $\gamma_{12} = \frac{1}{T_2}$ and $k_{12} = \frac{1}{T_2^*}$. This leads us to the popular rule of thumb,

$$\frac{1}{T_2} = \frac{1}{2T_1} + \frac{1}{T_2^*} \tag{5.5}$$

Now that we have broken down the Lindblad master equation and the ensuing relaxation matrix for a spin 1/2 system, let's take a look at the relaxation matrix for our valley qubit system with the following 3x3 Hamiltonian,

$$H = \begin{bmatrix} \frac{\epsilon}{2} & \Delta & \Delta_e \\ \Delta & -\frac{\epsilon}{2} & 0 \\ \Delta_e & 0 & -\frac{\epsilon}{2}+\delta \end{bmatrix} \tag{5.6}$$

As in Chapter 4, this Hamiltonian is in the charge basis, of the left, right and right valley states. In any real system the values in the relaxation matrix are going to be a function of the detuning, ϵ. In particular these values will tend to be a strong function of epsilon near any avoided level crossing in the energy level diagram. To avoid this problem we will consider our relaxation matrix only during qubit phase accumulation which occurs at large positive values of ϵ, taking in to account the

energy levels in this regime and following the same steps as before in the spin 1/2 case we arrive at the following relaxation matrix,

$$R = \begin{bmatrix} \Gamma_{12}\rho_{11} & \gamma_{12}\rho_{12} & \gamma 13\rho_{13} \\ \gamma_{12}\rho_{21} & -\Gamma_{12}\rho_{11} - \Gamma_{23}\rho_{33} & \gamma_{23}\rho_{23} \\ \gamma_{13}\rho_{31} & \gamma_{23}\rho_{32} & \Gamma_{23}\rho_{33} \end{bmatrix} \tag{5.7}$$

As previously mentioned, we are primarily interested in the dephasing of our qubit as it accumulates phase in the large positive ϵ region. Here, our system should be primarily in the two operation states, setting the relaxation matrix outside of that subsystem to zero yields the following,

$$R = \begin{bmatrix} 0 & 0 & 0 \\ 0 & -\Gamma_{23}\rho_{33} & \gamma_{23}\rho_{23} \\ 0 & \gamma_{23}\rho_{32} & \Gamma_{23}\rho_{33} \end{bmatrix} \tag{5.8}$$

Again we have $\Gamma_{23} = 1/T_1$, $\gamma_{23} = 1/T_2$ and $k_{23} = 1/T_2^*$. Now as the experiment results we have for comparison do not perform any sort of echo or T_2 measurement our results are likely dominated by pure dephasing and T_2^* yielding the very simple result,

$$R = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & k_{23}\rho_{23} \\ 0 & k_{23}\rho_{32} & 0 \end{bmatrix} \tag{5.9}$$

All that remains then is to pick values for our relaxation matrix R and simulate the dephasing using the following differential equation,

$$\frac{\partial \rho}{\partial t} = \frac{1}{i\hbar}[H, \rho] - R \tag{5.10}$$

Adding Eq. 5.8 or Eq. 5.9 to my GPU simulation using Matlab is difficult for two reasons: as these equations only apply intuitively in the energy eigen-basis a

transformation matrix must be calculated by diagonalizing the Hamiltonian at every time step in the differential equation solver; additionally, we expect the values T_1, T_2 and T_2^* to vary as a function of ϵ. Although I plan to continue developing this platform and eventually include the possibility of an epsilon dependent relaxation matrix, for the moment I have ignored this and implemented only a static relaxation matrix. Dealing with the basis transformation has proven to be tricky. Matlab has no function for diagonalization on the GPU; even with such a function the performance hit would be large as each parallel calculation has the potential to be at a unique value of ϵ at each time step. Including the diagonalization within the RK4 solver would mean diagonalizing potentially thousands of matrices at each time step. Such a process is computationally intensive especially if we hope to maintain the versatility of the software by allowing simulations of arbitrary dimensions. To simplify and expedite the simulation, I first calculate the transformation matrices D and D^{-1} using the cpu at coarse intervals across the entire span of possible detuning values, ϵ, in the simulation. These are then loaded onto the GPU in advance of the simulation and accessed as needed throughout the simulation, allowing a minimal performance hit at the cost of GPU memory usage and some precision due to the coarse graining. To confirm functionality, a simple two-state charge qubit was simulated with and without dephasing. The results are in Figure 5.2.

5.3 Converting simulated return probabilities to simulated QPC signals

Recall that the measured data in Chapter 4 is taken using a lockin current amplifier. The signal from the lockin can be written,

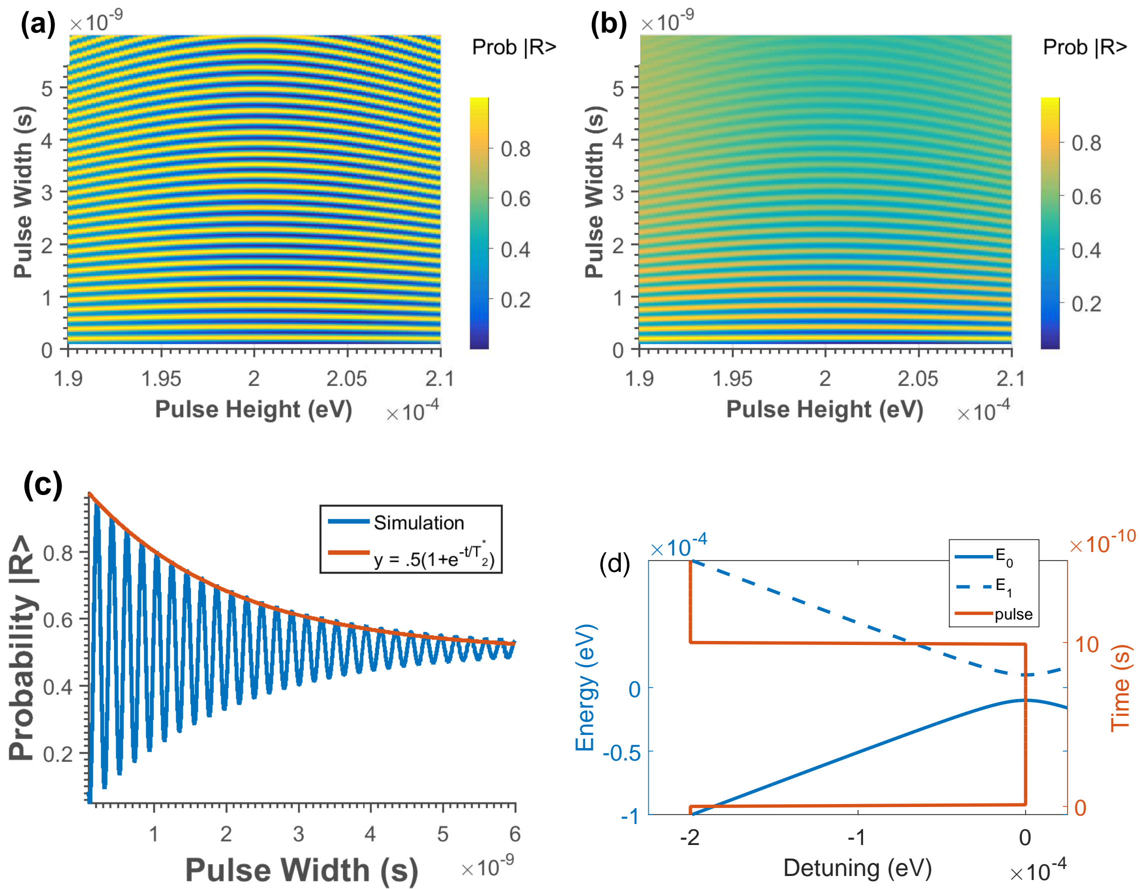

Figure 5.2: (a) Simulated charge sensing signal for a charge qubit under the influence of a square pulse, as a function of pulse height and pulse width. (b) Simulation of a charge qubit, identical to (a), but with the inclusion of a 2ns dephasing term. (c) Cross section from (b) with exponential overlaid showing good agreement. (d) Energy level diagram for the simulated charge qubit system, with the applied pulse overlaid.

$$\text{Re}[I_{lockin}] = \int I(\theta(V + A\sin(\phi)))\sin(\phi)d\phi \tag{5.11}$$

where the measured current, I, is a function of parameters θ, which in turn depend on the fixed side gate bias voltage, V. The quantity A is the lock-in voltage excitation amplitude. Since the lockin excitation is applied to V independently of the pulse generator we can rewrite the signal as follows,

$$\text{Re}[I_{lockin}] = \int I(V_0 + A\sin(\phi), V_p, t_p)d\phi, \tag{5.12}$$

where $V_0 = \epsilon_0/\alpha$, V_p is the applied pulse width and t_p is the pulse duration. For a small dither we can approximate $I = I(V_0) + A\frac{\partial I}{\partial V_0}\sin(\phi)$. Then we get the following result,

$$\text{Re}[I_{lockin}] = \int (I(V_0) + A\frac{\partial I}{\partial V}\sin(\phi))\sin(\phi)d\phi = A\pi\frac{\partial I}{\partial V_0}. \tag{5.13}$$

The lockin signal is proportional to the derivative with respect to V_0 and hence to ϵ_0 as well. To replicate the lockin signal, two separate simulations are calculated with a small change in ϵ_0 so that the derivative can be calculated.

5.4 Valley Qubit Parameter Extraction and Simulation

To fit for the coupling values Δ and Δ_e, the valley splitting δ is first measured from the calculated dispersion. At large ϵ δ can approximately be read off and we find δ = 5.57GHz. To fit for Δ and Δ_e we require a lever arm α to convert the voltage on V_L to the corresponding ϵ, $V_L\alpha = \epsilon$. Unfortunately we were unable to measure α on the device used for our valley qubit experiment before the device failed. Measurements of α on several other lithographically identical devices produced values

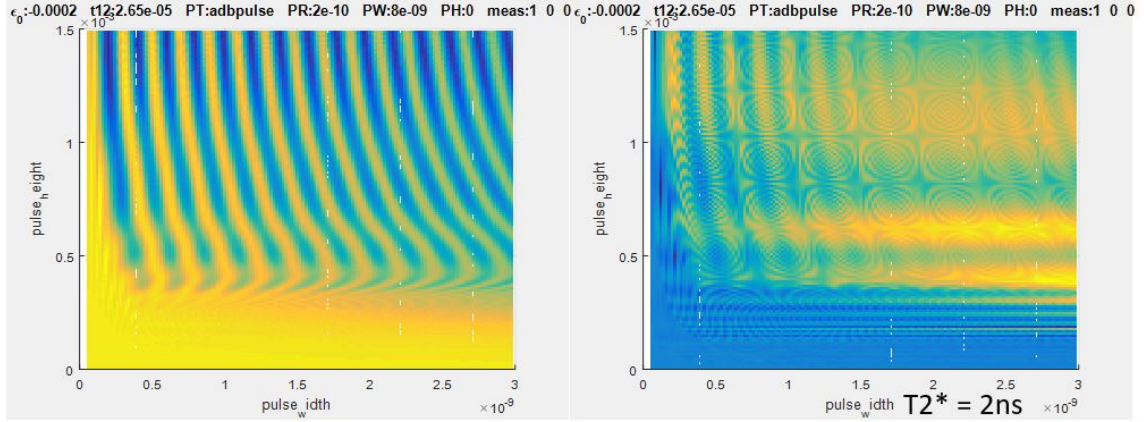

Figure 5.3: **(a)** Simulated valley qubit system using measured parameters without dephasing. **(b)** Identical simulation with the inclusion of a $T_2^* = 1ns$ dephasing.

between $\alpha = .01eV/V$ to $\alpha = .05eV/V$. To produce an estimate for Δ and Δ_e we assume that $\alpha = .03eV/V$. By fitting decaying sinusoids at each value of ϵ in our scans we are able to extract a dispersion relation as seen in 4.5. We can then numerically calculate $\Delta E(\epsilon, \Delta, \Delta_e)$ and fit the results to our measured dispersion, yielding a rough estimate of $\Delta = 6.4$GHz and $\Delta_e = 13.6$GHz.

Plugging these values into our simulation reproduces the observed data exceptionally well as seen in Figure 4.4, serving as evidence for the functionality of our simulation and the analysis of our valley qubit. We would also like to produce a simulation of our data that includes dephasing. In order to do this we use a fixed value of $T_2^* = 2ns$ in the middle of the measured range. The results can be seen in Figure 5.3

CHAPTER 6

Development of a Novel High Yield Gate Architecture for Si/SiGe Quantum Dots

6.1 Introduction

All of the measurements presented in previous chapters were taken on depletion mode devices. In fact, the majority of existing research on quantum dots to date was performed on depletion mode devices. However, limited by available fabrication technology, most depletion mode devices have gate patterns producing confinement on the order of 200nm or higher. In Silicon based devices where $m_e \sim m_{eff}$ these potential wells are much larger than wavefunctions of the trapped electrons, this limits control and tunability of the confinement potential. Recently there has been interest in alternative architectures such as accumulation mode devices[ZHM15]. These devices provide improved control and tunability at the cost of increased difficulty of fabrication. In this chapter, I will present several alternative *hybrid mode* device architectures developed in our lab. These *hybrid mode* designs are an attempt to design an architecture that benefits from the tunability of local top-gates, while simultaneously simplifying fabrication and reducing the total number of required control gates.

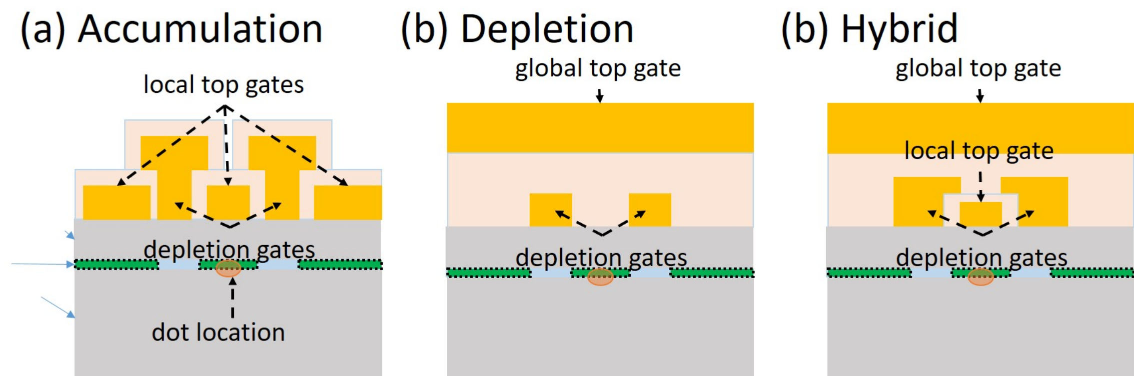

Figure 6.1: Schematic cross sections of three quantum dot architectures intended to produce a single dot (location marked with orange circle). (a) Accumulation architecture, 2DEG is controlled via local (directly on the substrate) topgates and depletion gates only. (b) Depletion architecture, 2DEG is controlled via a large global topgate and local depletion gates. (b) Hybrid architecture, 2DEG is controlled via a large global topgate, as well as local depletion gates and topgates.

The move to hybrid designs was motivated by our experience fabricating and testing accumulation mode devices. When performing electron beam lithography for accumulation mode devices, the second layer, including the local topgates for our quantum dots as well as the larger source and drain topgates as seen for our accumulation mode design in Figure 6.3e, is exceptionally sensitive to dosage. Writing larger features close to smaller features during electron beam lithography is difficult due to the presence of incidental dosage. Another challenge when making accumulation mode devices is alignment. While our alignment is consistently within $\sim$50nm this shift is still enough to produce devices with bare areas in the transport channel, making dot creation and control difficult or impossible. Additionally, we occasionally experience leakage problems from the source and drain top gates to the 2DEG on accumulation mode devices.

In order to address these issues we have moved towards fabricating *hybrid mode* devices attempting to simplify fabrication while maintaining the tunability benefits of accumulation mode devices. This has primarily been accomplished by removing the 4 independent source and drain topgates in favor of a larger global topgate protected by an additional layer of Al_2O_3. This fixes most device leakage issues, reduces the required leads, and increases the success rate of our e-beam lithography steps by reducing dosage sensitivity and simplifying alignment. Figure 6.1 shows a cross-sectional illustration of the differences between accumulation, hybrid and depletion mode devices. Screening of these devices is ongoing, and while alignment between tunneling barriers and local topgates of the dots has proven to still be an issue, we have had success with several DC transport measurements on these devices.

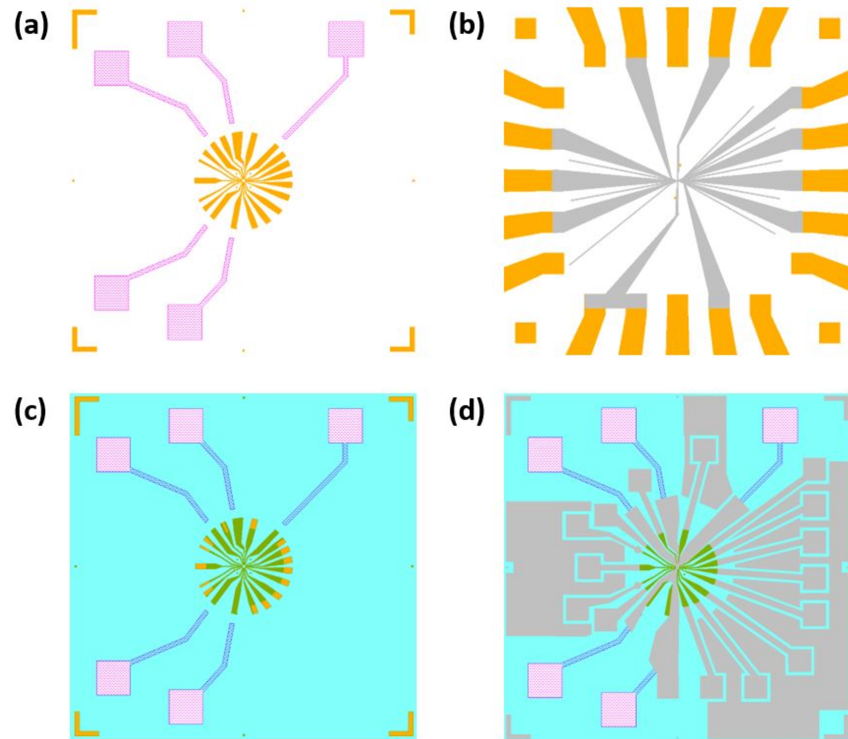

Figure 6.2: Schematics outlining the fabrication of a hybrid device. (a) Following annealling and deposition of a set of gold photolithography leads the sample is ready for electron beam lithography. (b) Four e-beam lithography patterns are fabricated in the $33\mu\text{m}^2$ device region. A set of small alignment markers near the device, and the three layers detailed in Figure 6.3. (c) An insulating layer of Al_2O_3 is grown using atomic layer deposition (ALD) then selectively etched using photolithography. (d) The outer set of photolithography gates is patterned and deposited, this layer also includes the global topgate in hybrid mode devices.

6.2 Device Fabrication

The fabrication steps are shown qualitatively for both hybrid and accumulation mode devices in Figure 6.3 and Figure 6.2. Note the difference in fabrication between the two types of devices, with the difficult to write pattern in Figure 6.3e simplified. The process begins with photolithography for 30nm Cr alignment markers, then another photolithography to define the ion implanted regions. After ion implantation the substrate is cleaned and annealed in a rapid thermal annealer. To reduce leakage issues and protect the substrate from damage via wirebonding the photolithographically defined portion of the gates is broken into two steps: an inner section that is patterned directly on the substrate, and an outer set of leads patterned on a 80nm layer of Al2O2. The inner leads are patterned in 5nm Cr 45nm Au following the annealing step, while the outer set of leads will be the final lithography performed on the devices.

With the inner set of photolithography leads patterned as in Figure 6.2a, the samples are ready for e-beam lithography. During depletion mode fabrication, a set of square alignment markers approximately 10 μm in size are patterned in Ti/Au along with the photolithography leads. Located approximately 100 μm from the center device area these markers provide sufficient precision for the e-beam lithography pattern to align with the photolithography pattern. However, this technique produces inner device leads with positions varying by as much as ~1um, too large a variation to align several subsequent e-beam layers. To produce good accumulation and hybrid type devices we require alignment precision of ~10nm. To accomplish this in the first e-beam lithography step, the devices are patterned with two 100nm^2 square alignment markers approximately 1 μm from the device area. These align-

ment markers are patterned separately from the first device layer so they can be made with Ti/Au. The alignment markers must be made independently of the first aluminum e-beam lithography layer (walls), as Al is difficult to image in an SEM and makes a poor alignment marker. These markers regularly produce well-aligned devices; however, misalignment is still an ongoing problem. Improving this alignment would improve our yield, but would likely require moving to alternative electron beam lithography equipment.

With the precision alignment markers placed the three layers of aluminum comprising the device itself are patterned using e-beam lithography; Figure 6.3 schematically outlines this process. First, a wall layer is made to deplete regions and define transport channels using 30nm Al. Second, a topgate layer is made consisting of the local topgates for each dot using 50nm Al. Unlike in a regular accumulation mode design, the second layer is written without topgates for each source and drain contact. Finally, a tunneling barrier layer is fabricated using 70nm Al. Each layer is electrically isolated from the others due to the native oxide formed on the Al layers.

Following fabrication of the device a 80nm layer of Al_2O_3 is grown over the entire substrate using ALD. This insulating layer is then selectively etched as in Figure 6.2 exposing ohmic contact wirebonding pads and the outer section of the existing gold photolithography leads. Finally, the outer photolithography leads are patterned and evaporated using a large 200nm Al layer. This layer contains all of the wirebonding pads for gates in addition to the global topgate itself. The device is now ready for cleaving, mounting, and wirebonding.

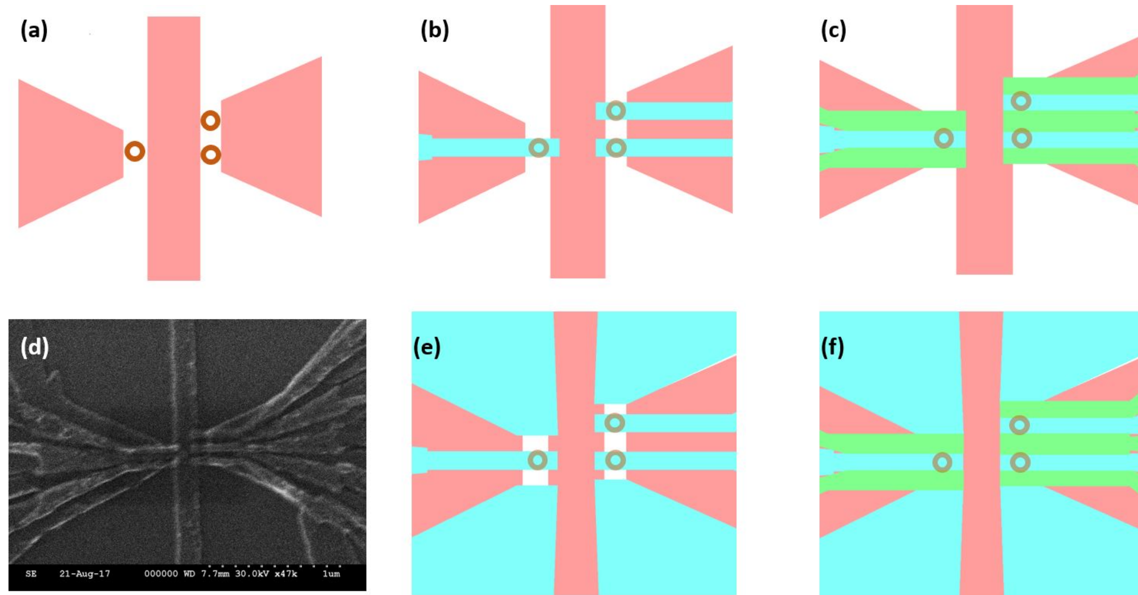

Figure 6.3: Outline of e-beam lithography steps for hybrid devices. In each panel two orange circles indicate the design location of a quantum well. (a) The bottom layer consists of *walls*, depletion gates used to define two transport channels that will contain dots. (b) Local topgates or *plungers*. Shown in blue these gates are used to adjust the depth of the quantum well at each dot. (c) Tunnel barriers, shown in green, used to adjust interdot and source/drain tunnel couplings. (d) SEM image of a completed hybrid mode device. (e) Alternative second layer used in a more standard accumulation mode architecture. The large source and drain topgates can make consistent dosing during e-beam lithography a challenge. (f) Third layer, showing a completed accumulation mode design.

6.3 Measurements and Results

Figure 6.3 shows an annotated device layout. The design is intended to form a large single within the left transport channel and a smaller set of double dots in the right channel. All measurements presented were taken using devices fabricated on a Si/SiGe substrate consisting of a 40nm SiGe spacer and a 10nm Si well. Many setbacks and challenges have accompanied developing a new device design, but we have recently had success with several hybrid mode devices making DC transport measurements through the single dot channel. Characterizing the double dot channel has proven more difficult, likely due to a more difficult alignment or tunneling rates that are too restrictive for transport measurements. Figure 6.4 shows transport through the single dot side as a function of the local topgate voltage V_P and a tunneling barrier V_{BR}. The device appears stable and can be tuned from QPC like behavior to dot like behavior by adjusting V_{BR} and V_{BL}.

We have had repeated success creating tunable single dots in the single dot channel, but have been unable to use this channel to obtain charge sensing data of the double dot system. Successful single dot current measurements, have allowed for low frequency charge noise measurements acquired using identical techniques to those developed in Chapter 3. Measurements on two separate devices produced values of $7e-6 \pm 1e-6\mu\text{eV}/\sqrt(Hz)$ and $1.75e-6 \pm .2e-6\mu\text{eV}/\sqrt(Hz)$ at 1Hz. These measurements are in line with but somewhat higher than previous measurements on depletion mode devices. The reason for this increase is not entirely clear, but given that gate architecture is expected to effect charge noise, the increase is perhaps not surprising. Figure 6.5 shows data used to calculate low frequency noise, as well as an extracted charge noise spectra.

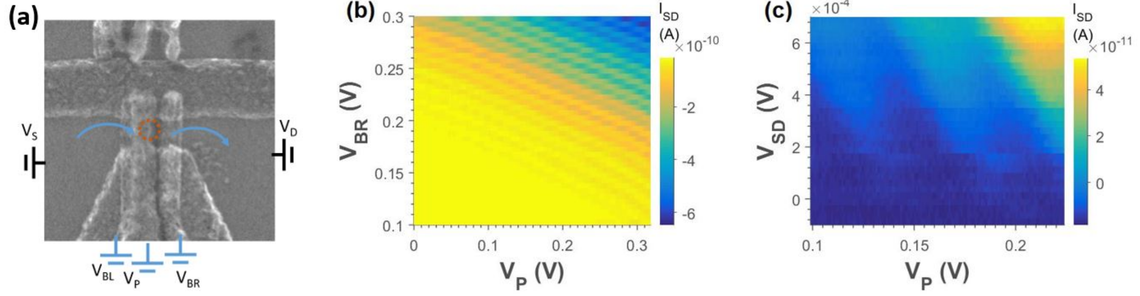

Figure 6.4: Transport measurements through single dot side of a hybrid mode device. (a) Single dot side of a hybrid system showing relevant gate voltages. (b) With other gate voltages fixed DC current is measured as a function of V_P and V_{BR} showing clear single dot current oscillations. (c) Coulomb diamond measurement showing current as a function of V_{SD} and V_P over several current peaks.

Sample	$\Delta\epsilon$ $\mu eV/\sqrt{Hz}$	α eV/V	E_C meV
U2BG3 peak 1	$1.75 \pm .25$	0.037	4.5
U2BG3 peak 2	2.1 ± 1.0	0.037	4.5
T2DE3	7.0 ± 1.0	0.028	2.1

Table 6.1: Summary of device measurements. The $\Delta\epsilon$ value is reported at $1Hz$ for every device as well as the lever arm α and the charging energy E_C.

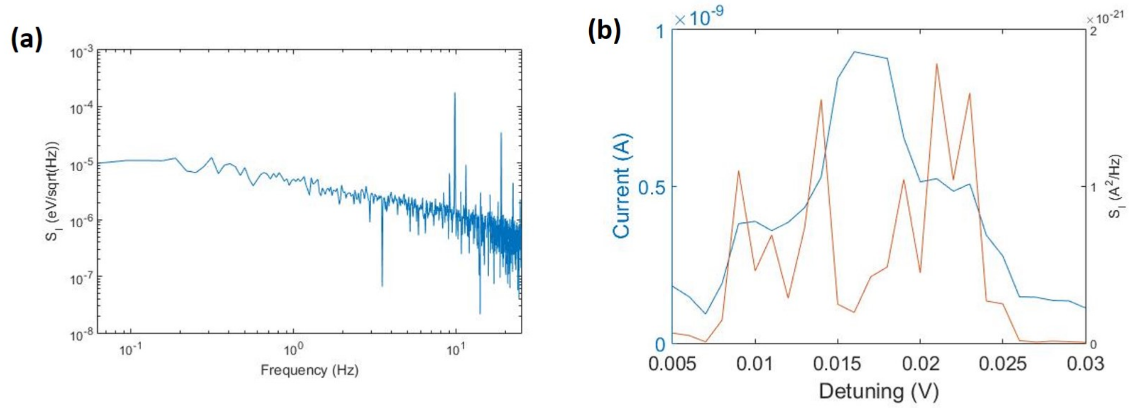

Figure 6.5: Low frequency charge noise measurement of a hybrid mode device. (a) Charge noise spectra from .1 Hz to 10Hz extracted using the techniques discussed in Chapter 3. Noise was measured to be somewhat larger than our depletion mode devices in a limited set of measurements. (b) Current peak at a fixed V_{SD} shown in blue, versus measured current noise spectra at .5 Hz; note how the noise magnitude is proportional not to the current, but to its derivative.

Coulomb diamonds on multiple devices have been produced using transport through the single dot side of a hybrid device. These measurements can be used to extract the lever arm α of the dots local topgate (V_P) and yield values of .02eV/V to 0.04eV/V, similar to the values seen on depletion mode devices.

6.4 Conclusions and Outlook

Moving to a new device architecture can be a difficult endeavor with many unforeseen consequences. Dosage and alignment of the innermost leads have proven to be a challenge. Immediate next steps would include the fabrication of another batch with a modified design shown in Figure 6.6. We believe that most of our issues with the existing hybrid mode devices stem from thin leads and misalignment. The new design significantly improves the alignment tolerances by writing the tunneling barriers as a large single lead covering the local topgates. Successful testing of this design demonstrating a single-dot system of the left side and a double dot system on the right would support the theory that alignment is our primary issue. In any case, hybrid mode structures appear promising and offer a functional alternative to accumulation mode devices, providing tunability alongside reduced fabrication difficulty and a reduced number of control gates. Possible next steps include considering alternative electron beam lithography setups, which may have more consistent alignment and fewer dosage issues.

The study of quantum dots as potential qubits is becoming a mature field, with successful demonstrations of a variety of qubit implementations using multiple architectures and heterostructures. Moving forward most topics of current interest are related not to demonstrating behaviors, but of reproducing them consistently.

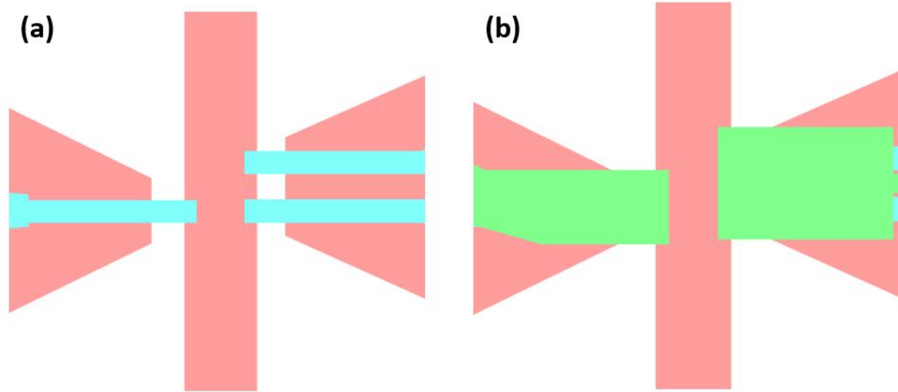

Figure 6.6: Next step in hybrid architecture testing showing the second, (a), and third, (b), device layers. This design would ease alignment requirements and high yield with this design would confirm that alignment is our primary challenge.

We discussed previously the ongoing study of interface valley physics, a better understanding of which may help to consistently produce devices with large valley splittings allowing for either spin to charge readout or valley state based qubits. But many other factors contribute to the relatively poor yield of quantum dot based qubit devices, including fabrication and device architecture. Developing a device architecture that reliably reproduces tunable and functional qubits is a pressing need for the field. With refinement the hybrid architecture has the potential to provide such an architecture.

APPENDIX A

Fabrication Recipes

A.1 Single and Double Layer Positive Photoresist Recipe for AZ5214E

1. **Spin HDMS:** 5 seconds at 500 RPM, 10 seconds at 4000 RPM.

2. **Spin on AZ5214-EIR:** 5 seconds at 500 RPM, 50 seconds at 4500 RPM.

3. **Bake and respin (double layer only):** 60 seconds on a hotplate at 100 C and repeat step 2.

4. **Bake:** 120 seconds on a hotplate at 100 C.

5. **Expose:** 13 second exposure time on Karl Suss MA6 mask aligner, 365 nm radiation at 8.0 mW/cm^2.

6. **Develop:** 30 seconds in 1:3 AZ400K:deionized (DI) water. 1 minute rinse in DI water.

7. **Dry:** Blow dry with N_2.

A.2 Electron Beam Lithography Recipe

1. **Spin on bottom layer PMMA:** PMMA 495 A4, 5 seconds at 500 RPM, 50 seconds at 5000 RPM.
2. **Bake:** 90 seconds on a hotplate at 180 C.
3. **Spin on top layer PMMA:** PMMA 950 A2, 5 seconds at 500 RPM, 50 seconds at 5000 RPM.
4. **Bake:** 90 seconds on a hotplate at 180 C.
5. **Expose:** Exposure using Hitach S-300H SEM modified with NPGS. Electron beam energy of 30 keV and current of 10 pA. Dosages depend on a variety of factors including feature size, feature density and substrate. The following dosages provide a reasonable starting point for dosage testing of new designs:
   - <40 nm: line exposure, 1.3nC/cm.
   - 50-100 nm: area exposure, 700 nC/cm^2.
   - 100-300 nm: area exposure, 550 nC/cm^2.
   - >300 nm: area exposure, 400 nC/cm^2.
6. **Develop:** 40 seconds in 1:3 MIBK:IPA. 60 seconds in IPA.
7. **Dry:** Blow dry with N_2.

A.3 Depletion Mode Quantum Dot Fabrication

1. **Alignment Markers**

- Define alignment marker areas using single layer photolithography.
- Deposit 30nm Cr using thermal evaporation.
- Lift-off in acetone.
- Carefully clean the device, 5 minutes in acetone, 5 minutes in IPA, 5 minutes in DI water.

2. **Ion Implantation**

- Define implant regions using double layer photolithography.
- Implantation of phosphorus ions, $2 * 10^{15}$ dosage at 15 keV.
- Remove photoresist using 20 minute soak in AZ400T photoresist stripper.
- Carefully clean the device, 5 minutes in Acetone, 5 minutes in IPA, 5 minutes in DI water.
- Oxygen plasma ash, 4 minutes in SPI Plasma Prep II.
- Anneal 30 seconds at 750 C in rapid thermal annealer.

3. **Metallization 1 (outer depletion gate leads)**

- Define outer lead regions using single layer photolithography.
- Deposit 5nm Ti, 45nm Au using e-beam evaporation.
- Lift off in acetone.
- Carefully clean the device, 5 minutes in acetone, 5 minutes in IPA, 5 minutes in DI water.

4. **Metallization 2 (inner depletion gate leads)**

- Define outer lead regions using electron beam lithography.
- Deposit 5nm Ti, 45nm Au using e-beam evaporation.
- Lift off in acetone.
- Carefully clean the device, 5 minutes in acetone, 5 minutes in IPA, 5 minutes in DI water.

5. **Aluminum Oxide Layer**

- Deposit 100nm AL_2O_3 using atomic layer deposition (ALD), 910 cycles.
- Carefully clean the device, 5 minutes in acetone, 5 minutes in IPA, 5 minutes in DI water.

6. **Metallization 3 (topgate)**

- Define top gate region using single layer photolithography.
- Deposit 200nm Al using thermal evaporation.
- Lift off in acetone.
- Carefully clean the device, 5 minutes in acetone, 5 minutes in IPA, 5 minutes in DI water.

7. **Etch 1 ALD**

- Define ohmic contact and depletion gate bonding pads using double layer photolithography.
- Etch in Transene Transetch-N for 5 seconds at 155 C (hotplate temperature).
- Stop the etch with a 60 second dunk in DI water.

- Carefully clean the device, 5 minutes in acetone, 5 minutes in IPA, 5 minutes in DI water.

8. **Etch 2 SiO_2 (Si/SiO_2 substrates only)**

   - Define ohmic contact pads using double layer photolithography.
   - Etch in Transene Transetch-N for 5 seconds at 155 C (hotplate temperature).
   - Stop the etch with a 60 second dunk in DI water.
   - Carefully clean the device, 5 minutes in acetone, 5 minutes in IPA, 5 minutes in DI water.

9. **Metallization 3 (ohmic contact pads)**

   - Using a fine tipped soldering iron apply a small amount of indium to each ohmic contact
   - The device is now ready for mounting and wirebonding.

A.4 Hybrid Mode Fabrication

1. **Alignment Markers**

   - Define alignment marker areas using single layer photolithography.
   - Deposit 30nm Cr using thermal evaporation.
   - Lift-off in acetone.
   - Carefully clean the device, 5 minutes in Acetone, 5 minutes in IPA, 5 minutes in DI water.

2. **Ion Implantation**

    - Define implant regions using double layer photolithography.
    - Implantation of phosphorus ions, $2 * 10^{15}$ dosage at 15 keV.
    - Remove photoresist using 20 minute soak in AZ400T photoresist stripper.
    - Carefully clean the device, 5 minutes in Acetone, 5 minutes in IPA, 5 minutes in DI water.
    - Oxygen plasma ash, 4 minutes in SPI Plasma Prep II.
    - Anneal 30 seconds at 750 C in rapid thermal annealer.

3. **Metallization 1 (inner photolithography gate leads)**

    - Define inner lead regions using single layer photolithography.
    - Deposit 5nm Ti, 45nm Au using e-beam evaporation.
    - Lift off in acetone.
    - Carefully clean the device, 5 minutes in Acetone, 5 minutes in IPA, 5 minutes in DI water.

4. **Metallization 2 (precision alignment markers)**

    - Define precision alignment markers using e-beam lithography (1 μm from device area).
    - Deposit 5nm Ti, 45nm Au using e-beam evaporation.
    - Lift off in acetone.
    - Carefully clean the device, 5 minutes in Acetone, 5 minutes in IPA, 5 minutes in DI water.

5. **Metallization 3 (wall layer)**

   - Define wall layer e-beam lithography.
   - Deposit 35nm Al using e-beam evaporation.
   - Lift off in acetone.
   - Carefully clean the device, 5 minutes in Acetone, 5 minutes in IPA, 5 minutes in DI water.
   - Bake 4 minutes on 150 C hotplate to assist in formation of native oxide.

6. **Metallization 4 (local topgate layer)**

   - Define local topgate layer e-beam lithography.
   - Deposit 55nm Al using e-beam evaporation.
   - Lift off in acetone.
   - Carefully clean the device, 5 minutes in Acetone, 5 minutes in IPA, 5 minutes in DI water.
   - Bake 4 minutes on 150 C hotplate to assist in formation of native oxide.

7. **Metallization 5 (local tunnel barrier layer)**

   - Define local tunnel barrier layer e-beam lithography.
   - Deposit 75nm Al using e-beam evaporation.
   - Lift off in acetone.
   - Carefully clean the device, 5 minutes in Acetone, 5 minutes in IPA, 5 minutes in DI water.

8. **Aluminum Oxide Layer**

    - Deposit 100nm AL_2O_3 using atomic layer deposition (ALD), 910 cycles.
    - Carefully clean the device, 5 minutes in acetone, 5 minutes in IPA, 5 minutes in DI water.

9. **Etch 1 ALD**

    - Define ohmic contact and contact regions of inner photolithgraphy leads using double layer photolithography.
    - Etch in Transene Transetch-N for 5 seconds at 155 C (hotplate temperature).
    - Stop the etch with a 60 second dunk in DI water.
    - Carefully clean the device, 5 minutes in acetone, 5 minutes in IPA, 5 minutes in DI water.

10. **Metallization 6 (global topgate and outer photolithography gate leads)**

    - Define top gate region using single layer photolithography.
    - Deposit 200nm Al using thermal evaporation.
    - Lift off in acetone.
    - Carefully clean the device, 5 minutes in acetone, 5 minutes in IPA, 5 minutes in DI water.

11. **Etch 2 SiO_2 (Si/SiO_2 substrates only)**

    - Define ohmic contact pads using double layer photolithography.

- Etch in Transene Transetch-N for 5 seconds at 155 C (hotplate temperature).
- Stop the etch with a 60 second dunk in DI water.
- Carefully clean the device, 5 minutes in acetone, 5 minutes in IPA, 5 minutes in DI water.

12. **Metallization 7 (ohmic contact pads)**

    - Using a fine tipped soldering iron apply a small amount of indium to each ohmic contact
    - The device is now ready for mounting and wirebonding.

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