UNIVERSITY OF CALIFORNIA, SAN DIEGO

# Ultra-Low-Power Integrated Circuits and Systems for Internet of Things Applications

A dissertation submitted in partial satisfaction of the
requirements for the degree
Doctor of Philosophy

in

Electrical Engineering (Electronic Circuits and Systems)

by

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2018

The dissertation of Hui Wang is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

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Chair

University of California, San Diego

2018

# EPIGRAPH

*There is a limit to our life,*

*but to knowledge there is no limit.*

Zhuang, Zhou

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ACKNOWLEDGEMENTS

A good story often times starts with a long time ago. Born in a peaceful and beautiful village in the east coast of China, I lived a childhood filled of joy and fun, chasing the rabbits in the woods, fishing by the river so clear and warm, and getting punished for my skinned elbows. I had plenty of time to picture my future in the sun - flying for over 12 hours across the Pacific Ocean to study in US had never been among them.

It has been quite the journey that began with the unbelievable first impression of the layout of the campus that is everything but elegance, and concluded with the submission of this dissertation and the memorable memories that have everything related to this lively campus. A journey that records the challenge, excitement, and joy on the path to my growth in profession and personality, and the great fortune to receive so much help and support along the way. I'm deeply indebted to my advisor, Professor Patrick Mercier, for providing me the opportunity to expose myself to the state-of-the-art research and the guidance to conduct research to push the boundaries. It has been my great honor to be your first admitted Ph.D. student and first graduated Ph.D. student. Not only your advice on technical issues, but the perspective of creative and innovative thinking and the attitude of being sincere and considerate to others has been invaluable to me. I also would like to extend my sincere gratitude to my Ph.D. dissertation committee members for all their support: Professors Peter Asbeck, Gert Cauwenberghs, Chung-Kuan Cheng, and Drew Hall.

My university life would never have succeeded and been so colorful without the precious lifelong friendship established in this period. I would like to thank Guobi Zhao and Huanhui Zhan for your friendship that is so pure and your optimism towards life that encouraged me to survive the very first two difficult years. To Jianzhi Wu, playing basketball with you was not only fun and a process of learning the fancy dribbling tricks, but a luxurious time to calm myself and refresh myself. Po-Han Wang - it has been an amazing encounter with you. We met in the very first class on the very first day after we arrived at UCSD from different places across the vast Taiwan Strait

(which, I hope, can be narrowed politically in the near future), and worked in the same group after two years passed since then. The free ride to home after taking off from work provided by you has been a pleasant trip of discussing the technical issues, the importance and rareness of integrity, and the philosophy of life. To Cooper Levy - your suggestion has always been very helpful to me and I'm so impressed with your broad scope of knowledge and wisdom; to Li Gao, discussing the technical issues with you has been pleasant experiences and it has been my fortune to have received your help. I would also like to thank Jiwoong Park - you have been a very caring friend and it has been a great pleasure spending time with Sojeong and you; Dhongue Lee - my 'closest' colleague in the *EEMS Group* lab. To the basketball crew: Xiahan Zhou, Haowei Jiang, Da Ying, Chih-Cheng Huang, and Chung-Lun Hsu - the game time with you has been the most welcome. To Alex Sun, it has been a wonderful trip traveling with you to the Europe.

It is important for me to have the help from the members in the *EEMS Group* lab. I would like to thank you for your significant impact on my personal and professional development: Xiaoyang Wang, Jiannan Huang, Julian Warchall, Loai Salem, Somayeh Imani, Bao Lam, Sally Amin. It has been a great pleasure spending time with you. It is an extraordinary experience for me to witness *EEMS Group* growing from only one student to today's scale.

Finally, but definitely not least, I'd like to extend my gratitude to my family for their love, support, and encouragement. To my parents, Xiaoqin and Shujun, you forge my personality with integrity, perseverance, and gratefulness. Educating me with your wisdom, you raise me up to more than I can be. To my lovely younger brother, Ke: I have never felt longly because you are always there for me. To my Uncle Laung-Terng and Auntie Susan: your guidance and support along the way is invaluable to me. If I have been stronger it is by standing on your shoulders. To my beautiful wife, Xiaohong: living half a planet apart for the first two years had never been overwhelming, but instilling our marriage into romance. Company is the longest confession of love - it is my greatest accomplishment to have married you and I can't wait to share the rest of my life with you.

The text of Chapter 2, in part, is a reprint of the material as it appears in "A 51 pW Reference-Free Capacitive-Discharging Oscillator Architecture Operating at 2.8 Hz" by Hui Wang and Patrick Mercier, in Proc. IEEE Custom Integrated Circuits Conference (CICC), Sep. 2015, and "A Reference-Free Capacitive-Discharging Oscillator Architecture Consuming 44.4 pW/75.6 nW at 2.8 Hz/6.4 kHz" by Hui Wang and Patrick Mercier, IEEE Journal of Solid-State Circuits (JSSC), vol. 51, no. 6, pp 1423-1435, Jun. 2016. The dissertation author was the primary investigator and author of both papers.

The text of Chapter 3, in part, is a reprint of the material as it appears in "A 1.6%/V 124.2pW 9.3Hz Relaxation Oscillator Featuring a 49.7pW Voltage and Current Reference Generator" by Hui Wang and Patrick Mercier, in Proc. IEEE European Solid-State Circuits Conference (ESSCIRC), Sep. 2017. The dissertation author was the primary investigator and author of this paper.

The text of Chapter 4, in part, is a reprint of the material as it appears in "A 113 pW Fully Integrated CMOS Temperature Sensor Operating at 0.5 V" by Hui Wang and Patrick Mercier, in Proc. IEEE Sensors Conference, Oct. 2017, and "Near-Zero-Power Temperature Sensing via Tunneling Currents Through Complementary Metal-Oxide-Semiconductor Transistors" by Hui Wang and Patrick Mercier, Scientific Reports, vol. 7, no. 4427, Jun. 2017. The dissertation author was the primary investigator and author of both papers.

The text of Chapter 5, in part, is a reprint of the material as it appears in "A 5.5nW Battery-Powered Wireless Ion Sensing System" by Hui Wang, Xiaoyang Wang, Jiwoong Park, Abbas Barfidokht, Joseph Wang, and Patrick Mercier, in Proc. IEEE European Solid-State Circuits Conference (ESSCIRC), Sep. 2017, and "A Battery-Powered Wireless Ion Sensing System Consuming 5.5 nW of Average Power," by Hui Wang, Xiaoyang Wang, Abbas Barfidokht, Jiwoong Park, Joseph Wang, and Patrick Mercier, IEEE Journal of Solid-State Circuits (JSSC) (In press). The dissertation author was the primary investigator and author of this paper.

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ABSTRACT OF THE DISSERTATION

**Ultra-Low-Power Integrated Circuits and Systems for Internet of Things Applications**

by

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Doctor of Philosophy in Electrical Engineering (Electronic Circuits and Systems)

University of California, San Diego, 2018

Professor Patrick Mercier, Chair

Internet of Things (IoT) have significantly heightened the level of our awareness about the world and extended the dimension of our interaction with it. While creating unprecedented growth opportunities for semiconductor industry in areas such as biomedical and wearable devices and health and environmental monitoring, IoT has revolutionized the design of integrated circuits and systems for such applications  wireless and small for unobtrusive and massive deployment, ultra-low-power for long-term operation, and full integration of all functionalities.

By virtue of low-frequency signals in most of such applications, integrated circuits and systems for IoT nodes are usually heavily duty-cycles and as a result the overall power is usually dominated by the standby circuitry  timers and bias blocks. A reference-free timer structure is

proposed by using capacitive-discharging topology to avoid the necessity of the conventional power-hungry reference generators. Thereby, it is imperative to minimize the power consumption of the bias circuits. A voltage and current reference generator is implemented leveraging gate-leakage transistors to achieve temperature-stabilized voltage and current references with pW power consumption and being able to generate pA low current reference, which is then employed to implement a timer achieving improved temperature- and supply-stability.

Temperature is an important parameter to measure in a variety of IoT applications. A new temperature sensing technique that relies on complementary temperature dependencies of different types of MOSFETs biased in the subthreshold region, together with constant-with-temperature tunneling currents and a capacitive charging-time-to-digital feedback architecture that digitizes temperature is proposed that consumes 113 pW in a fully monolithically-integrated manner. Another important parameter  ion concentration, for example ion homeostasis in sweat, blood, or saliva can potentially provide valuable additional insight into a user's overall health status. An ion sensing platform that integrates ion-selective electrodes with ultra-low-power sensor instrumentation, a wireless transmitter, and power management circuits is proposed to implement complete sensing-to-transmission functionality, achieving a linear near-Nernstian response with a slope of 71 mV/log10[$Na^+$] through in-vitro testing across a NaCl solution concentration range of 0.1-100 mM.

# Chapter 1

# Introduction

Semiconductor effect was first recorded back to the year of 1833 when Michael Faraday investigated the effect of temperature on ”sulphurette of silver” (silver sulfide) in his experimental work in chemistry. He found that the conducting power of silver sulfide increased rapidly with increased temperature by applying a lamp, which is in contrast with the influence of heat upon metallic conductors but typical of semiconductors [1]. More than one hundred years later, the integrated circuit was invented by Jack Kilby and Robert Noyce in late 1950s and ever since then integrated circuit process scaling has followed Moore's Law which states that the number of transistors on a single chip will double approximately every two years. The fast development of integrated circuits has revolutionized the world of electronics, for example: the bulky vacuum-tube-based computer that weighted tens of tons has been replaced by less than 1 kilogram laptop with much faster computation speed and capacity enabled by scaled digital processors; The market of consumer electronics has been growing exponentially and the consumer devices are becoming smarter, more powerful, and more portable; Advances in radio frequency are the forces behind the continuous evolution of wireless communications from one generation to another.

On the other hand, the concept of Internet of Things (IoT) was first introduced by Kevin Ashton in early 2000s as he searched ways to link radio frequency identification (RFID)

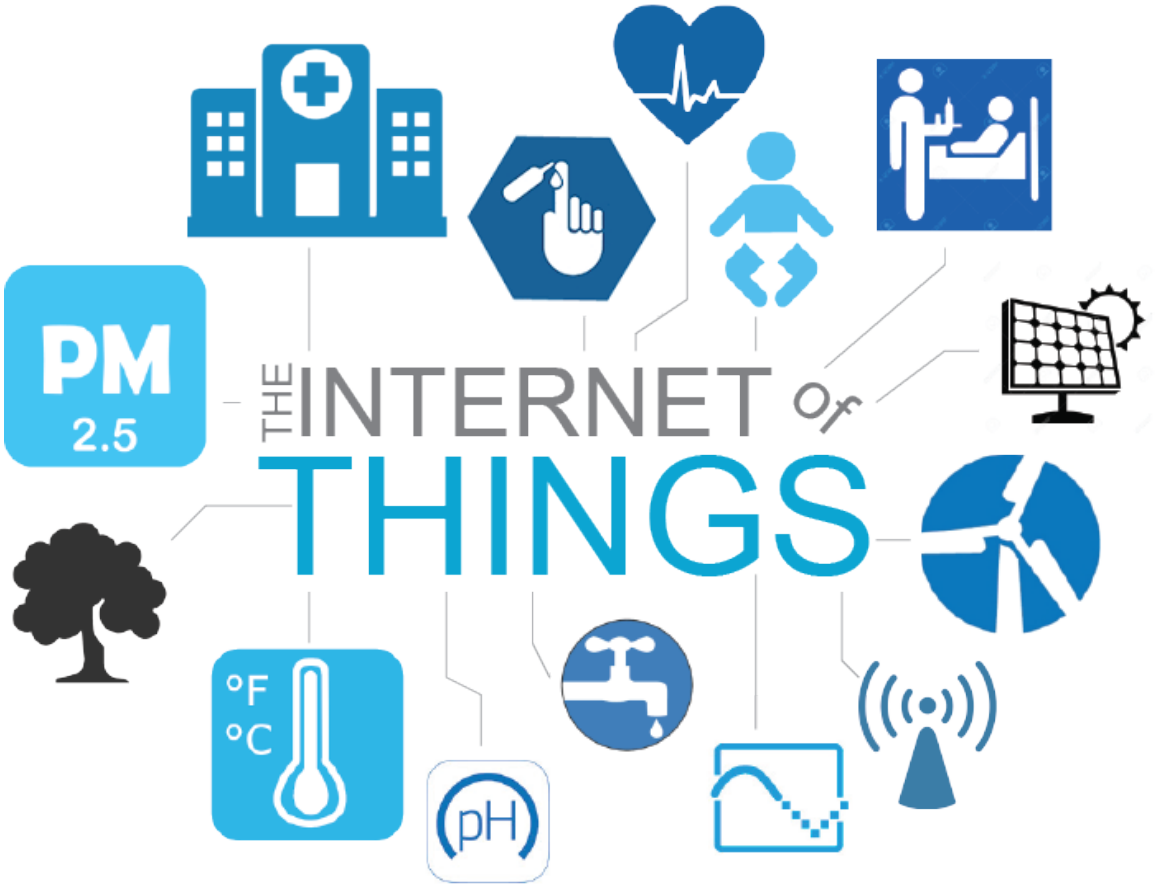


**Figure 1.1**: Applications of Internet of Things in industry and research. IoT has been widely employed in applications such as health care, environmental monitoring, energy harvesting, etc.

information to Internet. Simply yet powerful, the idea was that if all objects in daily life were equipped with identifiers and wireless connectivity, these objects could be communicate with each other and be managed by computers [2], which, however, encountered major technology obstacles at that time. As the design and fabrication technology mature, the integrated circuits are now able to provide low-cost and low-power solutions to enable next-generation IoT: The size and cost of wireless radios has dropped tremendously; IPv6 allows us to assign a communications address to billions of devices. Electronics companies are building Wi-Fi and cellular wireless connectivity into a wide range of devices; Battery technology has improved and energy harvesting methods including solar recharging and on-chip harvester have been built into numerous devices [2]. As a

result, next generation IoT evolves into a network of physical devices, vehicles, home appliances and other items embedded with electronics, software, sensors, actuators, and connectivity that enables these objects to connect and exchange data [3]. The IoT therefore allows the integration of the physical world into computer-based system, enabling more flexibility in terms of optimization for increased accuracy, wider deployment, and improved efficiency and economic benefits and thus creating new opportunities in industry and research.

## 1.1 Example of IoT Applications

As shown in Fig. 1.1, augmented with different types of sensors and actuators, IoT technology finds extensive applications in areas such as infrastructure, health care, environmental monitoring, etc. The following sub-sections will discuss three of the most popular IoT applications, i.e., smart home, infrastructure management, and medical and healthcare, though IoT has been widely employed in a lot of other areas.

### 1.1.1 Smart Home

As part of home automation or domotics, smart home systems usually consist of a hub or a central controller along with many other IoT devices for the controlling of, for example:

- lighting with a more comprehensive controlling of the lambs such as the brightness and color of individual lamp and the remote detecting of lamp failure;
- temperature monitoring and controlling to adjust the temperature of each room easily through a smart phone or other smart devices;
- security systems to control surveillance camera along with other sensors including window sensor, door sensors, motion detector to keep the users informed of the activity and send users alerts (Fig. 1.2).


**Figure 1.2**: Illustration of the applications of Internet of Things in smart home where security, lighting, temperature, humidity, etc., can be controlled via a central controller. Courtesy of IoT Philippines Inc.

The most immediate benefit of the smart home is the easy usability of different functionalities while the long term goal is a smart and user friendly living environment. Through IoT, utilities can be managed much more efficiently by controlling individual appliances based on actual utilization and needs. The combination of different sensors provides unprecedented security. The global smart home market is expected to be valued at over $130 Billion by 2023, growing at a compound annual growth rate (CAGR) of 13.61% between 2017 and 2023 [3].

### 1.1.2 Infrastructure Management

IoT devices have been widely employed to monitor and remotely control the operation of infrastructures such as railway tracks, bridges, and power grids. The IoT infrastructure is utilized to monitor the structural quality to reduce safety risk and, most importantly, can be implemented with a low-cost solution by built a large amount of low-cost wireless sensing nodes into the infrastructure to provide real time structural condition. Further, a lot of other useful information can also be collected from such IoT sensors and stored for cloud computing and extracting insightful information for scheduling repair and maintenance activities in an efficient manner, optimizing urban construction, and the building of a smart city where resources can be managed more efficiently.

### 1.1.3 Medical and Healthcare

It is estimated that by 2030 the number of Americans over the age of 65 will increase to roughly 20% of the overall population, which means frequency access to healthcare [4]. In addition, the spent on healthcare in US is predicted to increase from $2.6 trillion in 2010 to $4.6 trillion 2020, occupying 19.7% of the country's overall GDP [5]. IoT has been making significant impact in field of medical and healthcare. By enabling remote health monitoring, the expensive hospital treatment can be moved to home, significantly reducing the cost. For example, a lot of wearable devices ranging from heart rate and glucose monitors to advanced devices capable of monitoring specialized implants such as ion sensors, enables long-term monitoring of critical physical, electrophysiological, and physiochemical parameters such as pressure, temperature, electrocardiography (ECG), electroencephalography (EEG), and ion homeostasis in sweat, saliva, or blood, providing useful information for general well-being and addition insights into the users' overall health status. Note that such IoT devices can also be employed in the hospital environment. For example, by embedding IoT sensors such as blood pressure monitors or motion detectors,

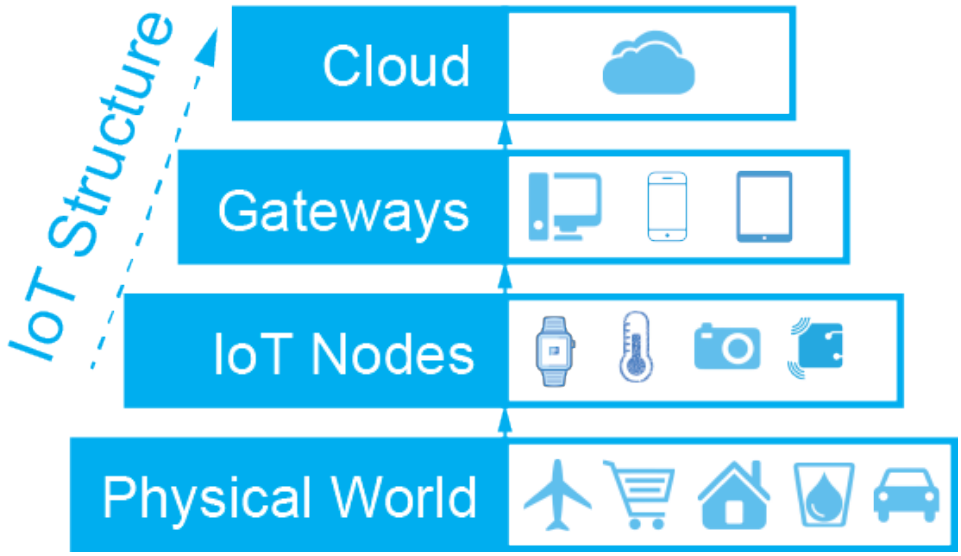


**Figure 1.3**: A simplified structure of the IoT. The bottom layer, IoT nodes, directly interact with the physical world and transmit data to the gateways (concentrators) which then collect and store the data to the cloud. The cloud servers perform computing and analysis, and extract desirable information for the users.

smart beds can keep track of patients' critical physical or electrophysiological status and send alerts to doctors for prompt medical treatment in emergence.

## 1.2 Integrated Circuits and Systems for IoT

### 1.2.1 IoT Structure

As shown in Fig. 1.3, a simplified IoT structure consists of three layers, i.e., IoT nodes, gateways or concentrators, and cloud. In the bottom layer, IoT sensing nodes interact with the physical world to perform sensing or actuating. Gateways or concentrators layer then collect and route the data to the cloud for cloud which perform the cloud computing or analysis and provide interfaces to supply extracted information to the users.

The requirements of the devices in the three construction layers in Fig. 1.3 are very different in terms of deployment scale, form factors, and power method and budget. As sum-

**Table 1.1**: Requirements in terms of deployment numbers, size, power method and budget of the devices in the three construction layers of the IoT.

| | Numbers | Size | Power Method | Power |
|---|---|---|---|---|
| **IoT Nodes** | High | Small | Untethered | Low |
| **Gateways** | Medium | Medium | Tethered/Untethered | Medium |
| **Cloud** | Low | Large | Tethered | High |

marized in Table 1.1, by virtue of their significantly different role in the IoT network and thus the pervasiveness, the number of the deployed IoT nodes in an IoT network is usually orders of magnitude larger than that of the gateways, which is in turn much higher than the number of cloud servers required in the IoT network. Since the IoT sensing nodes are directly interacting with the physical world and usually embedded in the corresponding objects or environment, the form factor of the sensing nodes thus need to be very small to be unobtrusive. On the other hand, such constraints are not valid for the gateways or cloud servers, though the gateways are generally orders smaller than the cloud server [6]. To be unobtrusively embedded in the physical objects, the operation of the IoT sensing nodes need to be performed untethered. The gateways, on the other hand, can be implemented with portable personal electronic devices such as smart phones or routers, can be tethered, while the cloud servers are generally tethered. By the virtue of deployment scale, form factor, and power methods, IoT sensing nodes have very limited power budget while the gateways and cloud servers can consumer orders of higher power.

Therefore, the IoT sensing nodes endure much stricter requirements on the form factor and power budget. The gateways and cloud servers can be implemented with existing electronic devices or servers and special customer needs can be implemented by tailoring the present system around the specification. Therefore, this dissertation focus on the integrated circuits and systems for the wireless sensing nodes.

### 1.2.2 Design Considerations for IoT Nodes

To further sum up, the requirements of the IoT nodes are directly defined by the features of the IoT applications with respect to physical constraints, essence of interactions with physical world, and functionality demands. Specifically:

- *Size:* The size of IoT sensors should be small (e.g., usually on the order of mm or even smaller in dimension) which is dictated by first, the their large number in deployment and cost reduction consideration, and second being unobtrusive which is required by a lot of IoT applications. This translates to a very limited area for circuit design and in return imposes challenges to full integration solutions. It is desirable and also a trend to integrated all functionality blocks from sensing to wireless data transmission. However, for example, the radiation efficiency drops significantly as the size scales.

- *Power:* It becomes impossible to access each of the IoT sensors after deployment considering the number of sensors and the corresponding cost. As a result, the IoT nodes are usually powered by batteries or energy harvesters. For battery powered IoT sensors, to prolong the life time the total power consumption of each IoT nodes should be minimized as the recharging or any other type of maintenance is unavailable. On the other hand, though energy harvesters can continuous provide energy during their life time, the available power from such energy sources is limited (usually on the order of $\mu$W or lower) due to the size constraints of the IoT nodes. Therefore, the available power budget for each IoT sensors is one the order of $\mu$W [6], while next-generation IoT sensors are targeting at nW full integration solutions.

## 1.3 Dissertation Contributions

This dissertation examines the design of ultra-low-power building blocks for next generation IoT applications, including analog, mixed-signal, and radio frequency circuits. The ultimate goal is to implement systems or platforms that integrate functionalities from sensing to wireless transmission and minimize the power consumption to meet the requirements for applications including wearable devices, biomedical sensors, smart homes, and environmental monitoring. This is accomplished primarily by employing low-power design techniques such as ultra-low power voltage and current reference generation by utilizing gate-leakage current, together with system-level innovation for increased energy efficiency. The main contributions of this dissertation are in the following areas:

- *Ultra-low-power voltage and current reference generators and timers for IoT nodes:* To minimize the power consumption, the operation of the IoT nodes is usually heavily duty-cycled since in most of such IoT applications, the signals of interest are usually in very low frequency band. In such systems, the total average power consumption of the IoT sensor is determined by the always-on blocks such as timers and bias circuits. A reference-free capacitive-discharging oscillator structure is presented in Chapter 2, targeting at overcoming the lowest achievable power limitation imposed by limited lowest bias current. By pre-charging two charge-tanks, which can be implemented by temperature-stable MIM capacitors, to $V_{DD}$, and then allowing one to discharge through a temperature-stable resistive path, while the other charge-shares with a pre-purged capacitor to setup an implicit reference voltage, a clock period can be obtained that is independent of $V_{DD}$ without any energy-expensive reference or calibration circuits. Two prototypes were implemented operating at 6.4 kHz and 2.8 Hz, consuming 75.6 nW and 44.4 pW and achieving a temperature accuracy of $\pm 0.74\%$ and 1260 ppm/$^{o}$C, respectively.

To further improve the timer performance and also to minimize the standby power of the IoT sensor, thus the overall average power, an ultra-low-power voltage and current reference generator is presented in Chapter 3. A 4-transistor (4T) self-regulated structure is implemented to generate a temperature- and line-stabilized reference voltage, which is then employed to drive a temperature-compensated gate-leakage array via a self-biased amplifier to achieve a stabilized current reference. The proposed VCRG is then utilized to generate a temperature- and line-stabilized oscillation by charging a swapping pair of MIM capacitors with the reference current and comparing to the reference voltage generated by the same VCRG in a relaxation structure. Measurement results of 13 VCRG samples fabricated in a 65 nm CMOS reveal an average temperature coefficient of 1037 ppm/$^o$C when operating from -40 to 120 $^o$C and an average line regulation of 2.4%/V from 0.4 to 1.2 V, all at an average power of 30.6 pW with a supply voltage of 0.4 V, the lowest reported supply voltage that a current generator can operate with. Measurement results of fourteen 65 nm oscillator samples reveal an average temperature coefficient of 999.9 ppm/$^o$C from -40 to 120 $^o$C and a line regulation of 1.6%/V from 0.6 to 1.1 V, all at a total power consumption of 124.2 pW at 20 $^o$C.

- *A near-zero-power fully integrated CMOS temperature sensor:* Temperature is an important parameter to measure in a variety of IoT applications such as environmental monitoring and wearable biomedical devices. Chapter 4 discusses design techniques that enable transduction and digitization of temperature at very low power levels. An example architecture is presented that transduces temperature in a fully-integrated CMOS chip by charging a pair of digitally-controllable integrated capacitors with a pair of pA current sources that are proportional-to and constant-with temperature, respectively, and digitally controlling the charge time between the two paths via a discrete-time feedback loop for direct temperature digitization. The 0.15 mm$^2$ 65

nm temperature sensor is shown to achieve a resolution of 0.21 $^{o}$C and a maximum inaccuracy of $\pm$1.93 $^{o}$C, all at an average power of 113 pW.

- *A near-zero-power fully integrated CMOS temperature sensor:* Chapter 5 presents a battery-powered wireless ion sensing platform featuring complete sensing to transmission functionality. A 1 mm $\times$ 1.2 mm chip fabricated in 65 nm includes a 406 pW potentiometric analog front end, a 780 pW 10-bit SAR ADC, a 2.4 GHz power-oscillator-based wireless transmitter that consumes an average of 2.4 nW during a 10 sample/sec transmission rate, two timing generation oscillators that each consume 140 pW, and a 3:1 switched-capacitor DC-DC converter with 485 pW of quiescent power that achieves efficiencies of 96.8% and 70.5% at 60 nW and 3.9 nW loads, respectively. The chip connects to a screen-printed ion selective electrode (ISE) responsive to sodium ions, and in-vitro testing across a NaCl solution concentration range of 0.1-100 mM exhibited a linear near-Nernstian response with a slope of 71 mV/log10[$Na^{+}$]. When all blocks are operating, the system consumes an average of 5.5 nW.

# Chapter 2

# An Ultra-Low-Power Reference-Free Capacitive-Discharging Oscillator Architecture

Advances in low-power radios and sensing circuits are enabling new and exciting applications in Internet of Things (IoT) devices, wearable sensors, medical patches, and environmental monitors [7–15]. Many such applications are extremely size constrained, and cannot afford a large battery or energy harvester. Fortunately, many such applications also measure parameters that have low-bandwidths, enabling aggressive duty-cycling of sensor and radio front-ends to push down the *average* power consumption of such devices. The average power consumption in such duty-cycled systems is thus often limited not by the active-mode power consumption of radios and sensor front-ends, but instead by a mix of duty-cycled active mode power and the quiescent power of always-on bias and timing circuitry.

Low-power timing circuits have been shown to operate down to tens of nW at kHz-range frequencies [14] [15], and down to tens of pW at Hz-range frequencies [7–13]. Achieving low quiescent power in a timer circuit is, however, a necessary, yet not sufficient condition to achieve

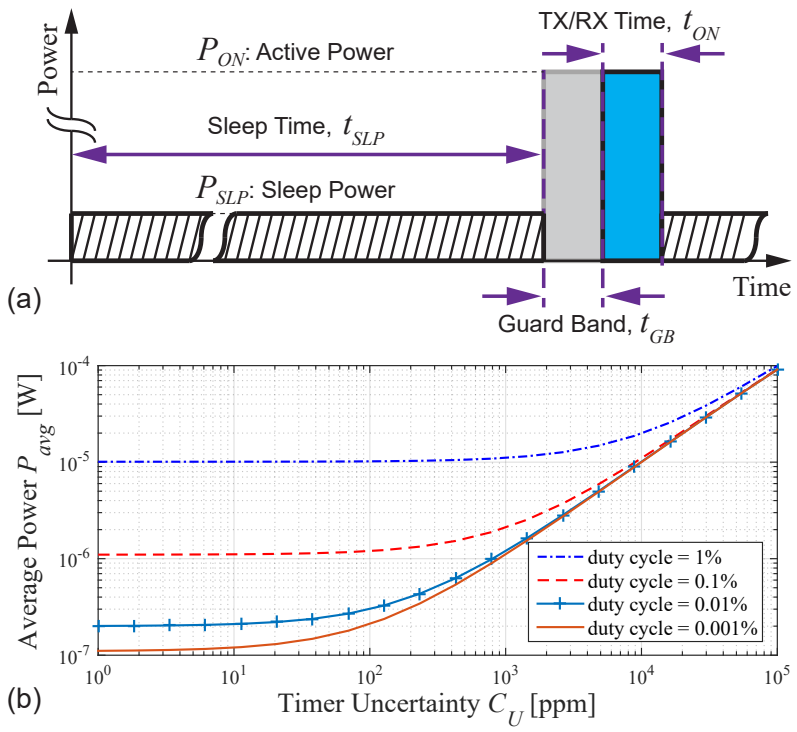


**Figure 2.1**: (a) Example timing profile of a wireless sensing platform that includes guard bands to compensate for timing uncertainty. (b) Average achievable power of a wireless node under varying timer uncertainty and duty cycles for a representative case where $P_{ON}$ = 1 mW, $P_{SLP}$ = 100 nW, $t_{ON}$ = 100 $\mu$s, and $t_{GB}$ is defined as $t_{GB} = C_U t_{SLP}$.

low average system-power in deeply duty-cycled wireless sensing systems. Specifically, the stability of the oscillator frequency across process, voltage, and temperature (PVT) variation introduces uncertainty, $C_U$, in sleep times, which thereby necessitates the radio receivers to turn-on early during a guard band window, $t_{GB}$, to ensure synchronization between wireless nodes. The guard band time $t_{GB}$ is defined as $t_{GB} = C_U t_{SLP}$ [16], resulting in the following equation for the average power consumption,

$$P_{avg} = \frac{P_{SLP} t_{SLP} + P_{ON}(t_{ON} + t_{GB})}{t_{SLP} + t_{ON} + t_{GB}}, \tag{2.1}$$

where $t_{SLP}$ is the sleep time, $t_{ON}$ is the average on-time post guard band, and $P_{SLP}$ and $P_{ON}$ are the sleep power and the active power, respectively (Fig. 2.1(a)). Since the active power of

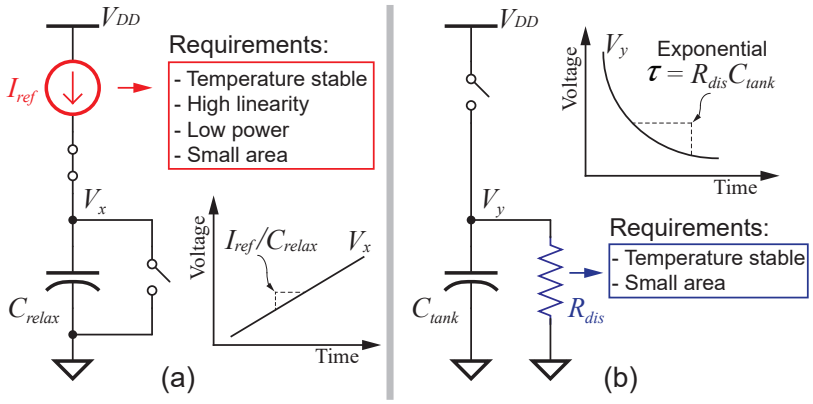


**Figure 2.2**: (a) Linear, low power, and temperature-stable reference currents are required in conventional relaxation oscillators. (b) A pre-charged capacitor is discharged via a temperature-stable resistor in the proposed oscillator architecture.

radios range from hundreds of $\mu$W to tens of mW [17] [18], timing uncertainty, which leads to large guard bands, can significantly increase the average power consumption of wireless sensing nodes. Figure 2.1(b) illustrates the average achievable power of a wireless node under varying timer uncertainty and duty cycles, for a representative case where $P_{ON}$ = 1 mW, $P_{SLP}$ = 100 nW, and $t_{ON}$ = 100 $\mu$s. Fig. 2.1(b) thus illustrates that timers must not only achieve low-power, but also low-uncertainty in order to achieve low overall power in duty-cycled systems. To make matters more difficult, many such IoT, wearable, and environmental monitoring applications are extremely size and/or cost constrained [7–18], and therefore cannot afford an external crystal [19] or additional pins (and/or testing time) to enable expensive post-fabrication calibration routines. Thus, it is imperative to design fully-integrated sleep timers that feature ultra-low quiescent power consumption and good frequency stability over PVT variation, all in an architecture that does not require excessive post-manufacturing trimming or calibration schemes.

Unfortunately, power consumption and frequency stability tend to trade-off with each other, and frequency stability across PVT tends to suffer without calibration, making the design of oscillators for ultra-low-power wireless sensing systems challenging. For example, integrated MEMS oscillator [20] [21] and CMOS harmonic oscillator [22] exhibit excellent

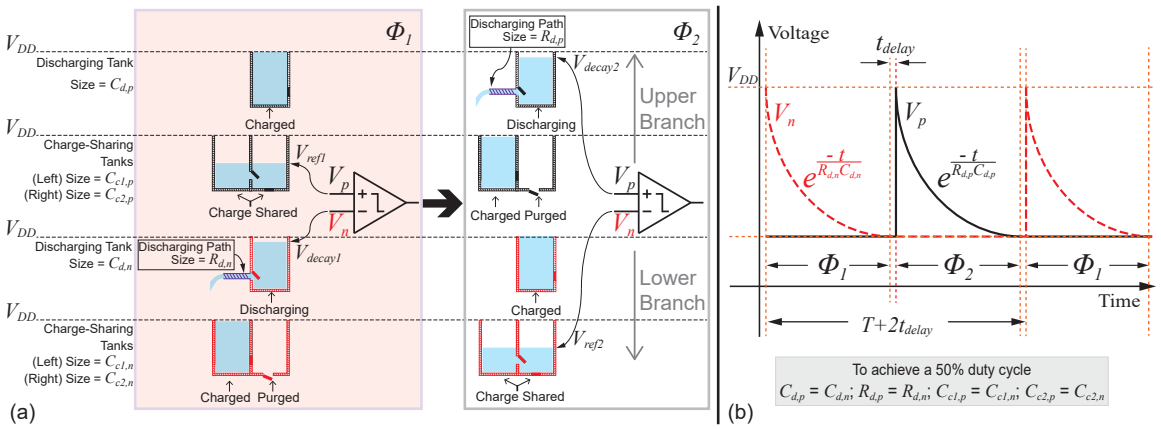


**Figure 2.3**: (a) Charge behavior including charging, charge-sharing, and discharging in six charge tanks and two discharging paths illustrating the operating principle of the proposed reference-free capacitive-discharging oscillator architecture. (b) Timing diagram of the waveforms at the inputs of the comparator over the course of three oscillator cycles.

frequency stability, though at the price of high power consumption in the mW-range [20] [22]. A common fully-integrated low-power oscillator architecture is based on a constant-current relaxation topology, where a temperature-stabilized current source is used to charge a capacitive network as illustrated in Fig. 2.2(a). By exploiting techniques such as feed-forward correction [23], self-chopping [24], comparator offset cancellation [25], mobility-referenced delay generators [26], or modifying the conventional topology and instead employing inverters that are current-starved by a Proportional To Absolute Temperature (PTAT) current source [27], and resistive frequency locking [28], relatively stable relaxation oscillators in the kHz range have been demonstrated. However, temperature-compensated voltage or current generators generally consume area and power overhead to achieve the requisite performance [29], and most prior art requires post-fabrication calibration (or the results of only a single die are reported).

The maximum oscillation period of a conventional relaxation oscillator is principally determined by the capacitance-to-charging current ratio. Achieving a low oscillation frequency in the pursuit of achieving low-power thereby demands either a large capacitor or a small current. Unfortunately, current reference generators operating at low currents typically rely on

a temperature-stabilized voltage reference generator (VRG) that biases a large resistor. Thus, achieving Hz-range frequencies requires either enormous resistance given achievable on-chip capacitor values (e.g., 10 GΩ for 100 pF of on-chip capacitance), or enormous capacitance given achievable on-chip resistor values (e.g., 10 nF with 100 MΩ of on-chip resistance), making fully-integrated, area-efficient designs impractical. To reduce area, gate-leakage-based timers have been shown to operate at Hz-range frequencies by employing gate-leakage transistors as ultra-low-current sources [30] [31]. However, the timer in [30] showed high jitter and temperature sensitivity since the phase transition was determined by the temperature-varying threshold voltage of a Schmitt trigger. To combat this, a multistage structure with a high-gain triggering buffer and boosted capacitance charging was proposed in [31] and a constant charge subtraction scheme was proposed in [32], however, both at the price of increased power consumption. A comparator-less timer structure based on program-and-hold circuit was proposed in [33]. However, it exhibited a large temperature dependency since the phase transition was dependent on device threshold voltages rather than a comparator.

In this work, a capacitive-discharging oscillator architecture is presented where the oscillation frequency is set directly by *RC* time constants via pre-charged capacitors discharged over passively temperature-compensated resistive elements, as conceptually illustrated in Fig. 2.2(b). Importantly, the oscillation frequency is not determined by any explicit reference voltages or currents, thereby reducing area and power overhead while also limiting the number of elements that can contribute to temperature sensitivities. Two separate designs employing this architecture are presented in this chapter: a kHz-range oscillator that employs temperature-stabilized resistors in the discharging path, and a Hz-range oscillator [34] that employs temperature-compensated gate-leakage transistors to effectively serve as large resistors in the discharge path. The first implementation consumes significant area due to the characteristics of the on-chip resistors, but by using gate-leakage transistors this area can be reduced drastically, which is proven in the second design (with an even lower oscillation frequency obtained). The two designs are

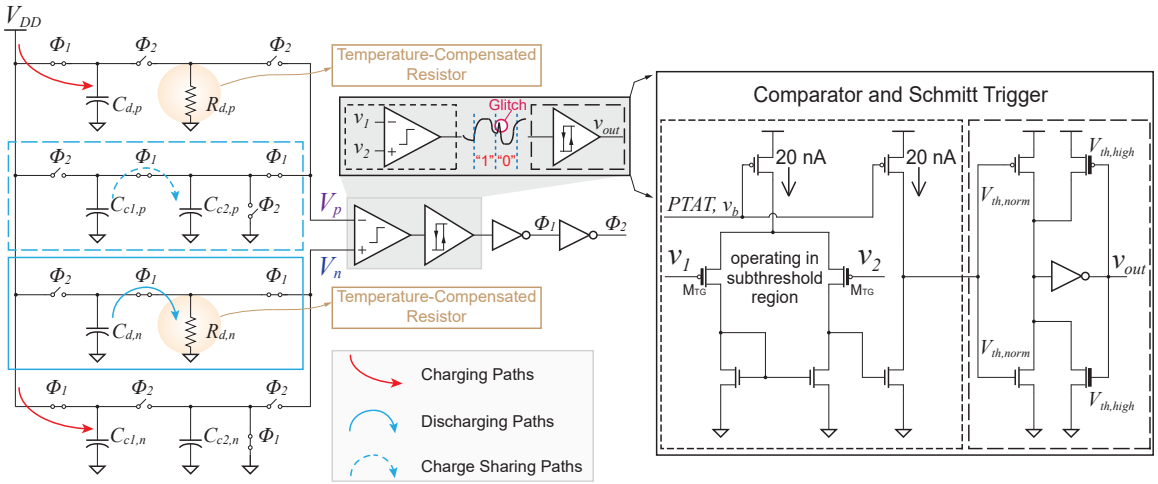


**Figure 2.4**: Schematic of the kHz-range reference-free capacitive-discharging architecture. MIM capacitors and temperature-compensated resistors are employed as charge reservoirs and discharging paths, respectively. Thick-gate transistors ($M_{TG}$) are employed in the comparator as the input stage to minimize leakage. Nominal-$V_t$ and high-$V_t$ transistors are used in the Schmitt trigger.

fabricated in different processes, and are shown to achieve frequency-stable, ultra-low-power operation without requiring any external components. Measurement results are presented without calibration, though one-point calibration may be required in certain practical applications. In some cases, calibration can be avoided since a one-time measurement within a wireless sensing platform may be sufficient for reliable communication by storing the measured frequency so long as the oscillator stays stable during its operation.

This chapter is organized as follows: Section 2.1 describes the proposed architecture; the circuit implementations operating at 6.4 kHz and 2.8 Hz are presented in Section 2.2; the frequency stability is analyzed in Section 2.3; the measurement results of the two designs are presented in Section 2.4; and Section 2.5 summarizes the results.

## 2.1 Ultra-Low-Power Capacitive-Discharging Oscillator

The operating principle of the presented capacitive-discharging oscillator architecture is conceptually illustrated in Fig. 2.3(a). The oscillator contains upper and lower branches that

operate in two phases, $\Phi_1$ and $\Phi_2$. Each branch contains two charge reservoirs: one reservoir is discharging at a known rate via a resistive element, while the other was, via a charge sharing mechanism, set to a known reference potential in the preceding phase for comparison to the discharging reservoir. The phase of the oscillator changes when the potential of the discharging reservoir falls below the charge sharing reservoirs. As illustrated in Fig. 2.3(a), discharging reservoir $C_{d,\{n,p\}}$, which was pre-charged to $V_{DD}$ in the preceding phase, is depleted of its charge at a known, exponentially decaying rate via $R_{d,\{n,p\}}$. In the preceding phase, $C_{c1,\{n,p\}}$ was pre-charged to $V_{DD}$, and in the current phase shares charge with $C_{c2,\{n,p\}}$, which was purged in the preceding phase, resulting in charge sharing that generates a reference potential given by:

$$V_{ref1} = V_{DD}\frac{C_{c1,p}}{C_{c1,p}+C_{c2,p}}. \tag{2.2}$$

The decaying voltage $V_{decay1}$ and the reference voltage $V_{ref1}$ are fed to a comparator, and when the decaying voltage $V_{decay1}$ falls below $V_{ref1}$, the circuit enters the second phase after a comparator delay, $t_{delay}$, at which point the charging, charging-sharing, and discharging roles of the charge-tanks in the upper branch and lower branch are reversed.

The voltages observed at the comparator inputs during three successive cycles are shown in Fig. 2.3(b). In this case, a 50% duty cycle is achieved by sizing upper and lower branch elements the same. The period of the oscillator is given by $T$+2$t_{delay}$, where the ideal period $T$ is twice the time taken by the decaying voltage to fall below the reference voltage. Thus, at the point in time when the decaying voltage is equal to the reference voltage, the following equation holds:

$$\frac{C_{c1,p}V_{DD}}{C_{c1,p}+C_{c2,p}} = V_{DD}e^{-\frac{T/2}{R_{d,n}C_{d,n}}}. \tag{2.3}$$

Therefore, the ideal period $T$ of the capacitive-discharging oscillator architecture is given by:

$$T = 2R_{d,n}C_{d,n}\ln\frac{C_{c1,p}+C_{c2,p}}{C_{c1,p}}. \tag{2.4}$$

Note that apart from different oscillation frequencies, different duty cycles can be obtained without requiring any extra circuitry or calibration cost by sizing the charge-tanks and the discharging path in the upper branch and lower branch differently.

## 2.2 Circuit Implementation

### 2.2.1 kHz-Range Oscillator Implementation

The proposed reference-free capacitive-discharging oscillator is first validated in 250 nm CMOS via the implementation of a kHz-range oscillator. A schematic of this design is shown in Fig. 2.4. Here, inherently temperature-stable MIM capacitors [35] are used as charge reservoirs, and passively-temperature-compensated resistors are employed to serve as temperature-stable discharging paths. Design of the resistive path is discussed in more detail in Section 2.3.

Note that the mismatch between the components in the upper branch and lower branch, for example, $C_{c1,p}$ and $C_{c1,n}$, will affect the duty cycle of the oscillation period, while the mismatch between the components in the same branch, for example, $C_{c1,p}$ and $C_{c2,p}$, will affect the oscillation frequency.

A two-stage analog amplifier forms the core of the comparator. Its inputs are biased in the subthreshold region in order to maximize transconductance efficiency and reduce power consumption. To prevent glitches that nominally occur at the output of the comparator between phase transitions, a Schmitt trigger is employed as the first buffer stage after the comparator. As shown in Fig. 2.4, the transitioning threshold voltage from high to low, $V_{th,high2low}$, and the transitioning threshold voltage from low to high, $V_{th,low2high}$, are now purposely mismatched to each other, thus resulting in a hysteresis voltage of approximately 30 mV.

### 2.2.2 Hz-Range Oscillator Implementation

The proposed capacitive-discharging oscillator can also be employed in applications where lower frequency clocks are required. To validate this, another oscillator is implemented in a 65 nm CMOS process that operates at 2.8 Hz. A schematic of the design is shown in Fig. 2.5.

Similar to the implementation of the kHz-range oscillator, inherently temperature-stable MIM capacitors are used as charge reservoirs. However, operation at Hz-range frequencies requires prohibitively large poly resistors. Fortunately, gate oxide thickness continues to shrink as CMOS technology scales, leading to significant gate-leakage, which is the sum of electron tunneling currents (tunneling from the conduction and valence bands), and hole tunneling current (tunneling from the valence band) [36], which can be exploited to design large resistances. The magnitude of gate-leakage is on the order of fA/$\mu$m$^2$ to pA/$\mu$m$^2$ [30], thereby enabling large, yet compact effective resistances. As a result, gate-leakage transistors are employed as the resistive discharging paths in the proposed Hz-range oscillator. Temperature stability is achieved passively as discussed in Section 2.3.

A detailed circuit schematic of the comparator in the Hz-range oscillator is shown in Fig. 2.7(a). Thick-gate transistors are employed as the input stage to minimize the gate-leakage of the comparator ($< 0.05\%$ of the signal current). The amplifier is biased in the subthreshold region directly with gate-leakage transistors to avoid the requirement for a power and area-expensive current bias generator. To prevent the glitches from propagating from the comparator to the following stages, a Schmitt trigger is employed as the first buffer stage after the comparator.

Since the absolute currents flowing in the circuit are extremely small, charge leakage through phase-transition switches can significantly impact the oscillator frequency. To minimize this effect, ultra-low-leakage switches are employed [37]. As shown in Fig. 2.7(b), transistors $M_1$ and $M_2$ are on when $\phi$ is low and thus $T_2$ and $T_{low\_leak}$ are electrically connected. When $\phi$ is high, $M_1$ and $M_2$ are in the off state, while $M_3$ is on. $M_3$ is employed to bias the source of $M_2$ at a voltage, $V_{b,M2drain}$, which is a replica of the drain voltage of $M_2$ buffered by the low-bandwidth

and ultra-low-power 5-transistor (5T) operational transconductance amplifiers (OTA) shown in Fig. 2.5. As a result, $M_2$'s source, drain, and bulk terminals are all biased at the same voltage, therefore minimizing charge leakage by over 68 dB compared to when no feedback is employed. Note that when $M_3$ is in the off state, it contributes charge leakage which will affect the signal path ($T_2$ to $T_{low\_leak}$). $M_3$ is sized such that the leakage current through $M_3$ ($< 0.5$ fA) is less than 0.05% of the signal current from $T_2$ and $T_{low\_leak}$ (1 pA), thus minimizing the influence on oscillation frequency.

As shown in Fig. 2.5, the series switches connecting $V_{DD}$ and $C_{d,\{n,p\}}$ and $C_{c1,\{n,p\}}$ are implemented with PMOS-type ultra-low-leakage switches while NMOS-type ultra-low-leakage switches are employed as the shunt switches to purge $G_{d,\{n,p\}}$ and $C_{c2,\{n,p\}}$.

It's worth mentioning that when $M_1$ is turned on from preceding off state, there exists a short time during which $M_3$ stays in preceding on state due to the delay of the inverter (Fig. 2.7(b)), thus creating a path from $T_2$ and $T_{low\_leak}$ to $V_{b,M2drain}$. However, during this phase the series switch is turned on (i.e., $T_2$ and $T_{low\_leak}$ are electrically connected) to re-charge the capacitor, for example, $C_{d,p}$. The short-time on state of $M_3$ effectively affects the time required to charge $C_{d,p}$ to $V_{DD}$, which is therefore negligible since it takes a much shorter time than half the oscillation period to charge $C_{d,p}$ as shown in Fig. 2.3(b). The same conclusion applies to the shunt ultra-low-leakage switches during which phase the shunt switches are purging the capacitors.

## 2.3 Frequency Stability Analysis

Sleep timers in next-generation wireless sensing devices should be stable under the presence of temperature and supply voltage variation. The following subsections describe the supply voltage and temperature dependencies of the capacitive-discharging oscillator architecture.

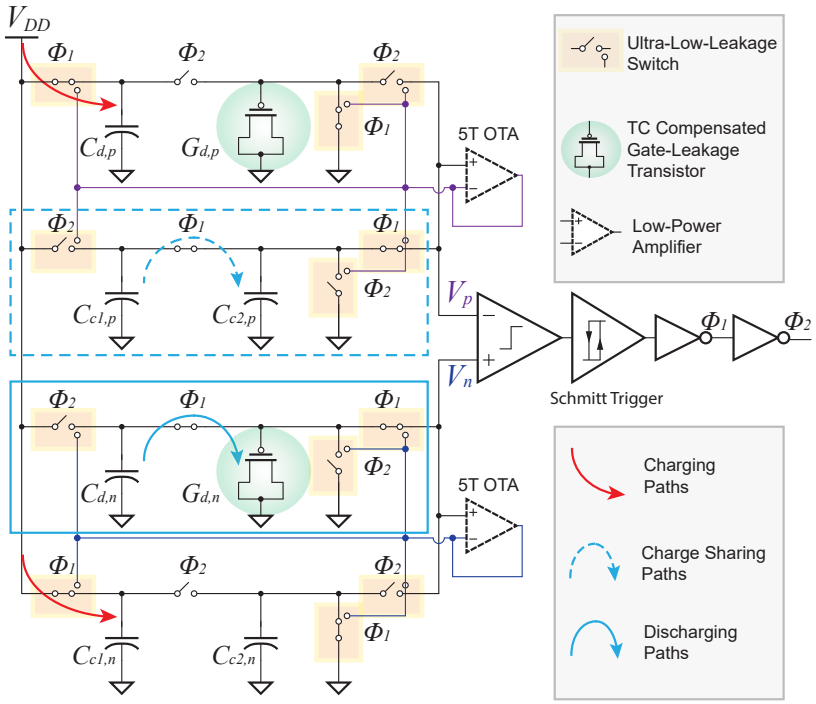


**Figure 2.5**: Schematic of the Hz-range reference-free capacitive-discharging architecture. Gate-leakage transistors were employed to serve as large on-chip resistance.

### 2.3.1 Supply Voltage Dependency

Since the reference voltage generated by the charge-sharing charge-tanks $C_{c1,\{n,p\}}$ and the decaying voltage generated by charge-tanks $C_{d,\{n,p\}}$ are initialized from the same source ($V_{DD}$), supply variation appears as common-mode noise that is, as illustrated in Fig. 2.8, rejected by the common mode rejection ratio (CMRR) of the comparator (80 dB and 75 dB for the kHz-range and Hz-range implementations over the frequency band of interest). Note that in accordance with the first-order model in Equation 2.4, there is no $V_{DD}$ term setting the oscillator period. The frequency stability of the proposed oscillator architecture is therefore primarily affected by the temperature dependencies of the components employed in the charging paths, discharging paths, and charge sharing paths, though second-order effects cause supply variation.

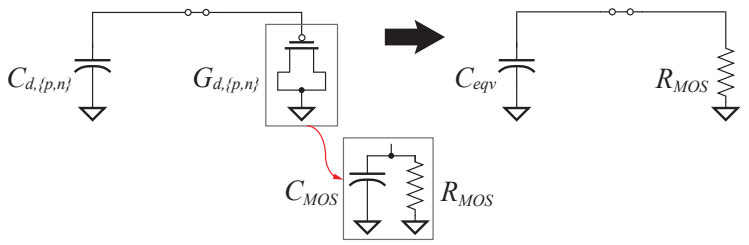


**Figure 2.6**: The equivalent RC discharging model to take into account the parasitic MOS capacitance of the temperature-compensated gate-leakage transistor.

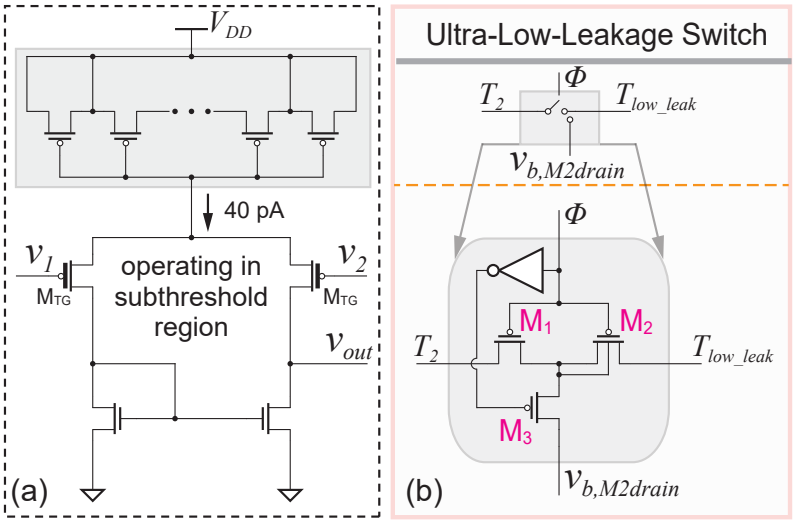


**Figure 2.7**: Detailed circuit schematic of the self-biased comparator using gate-leakage current as bias current where thick-gate transistors ($M_{TG}$) are employed as the input stage to minimize leakage (a), and the ultra-low-leakage switch used in the Hz-range reference-free capacitive-discharging oscillator (b).

### 2.3.2 Temperature Dependency

As shown in Equation 2.4, frequency stability is directly affected by the temperature characteristics of the effective capacitance and the effective resistance of the charge reservoirs and discharging paths. While MIM capacitors do have some temperature dependence due to variation of the dielectric permitivity (15-21 ppm/$^o$C) and due to geometric variation dimensions (5.6 ppm/$^o$C) [35], the overall impact of capacitor temperature variation is relatively low. In fact, both PDKs used in the presented designs do not include a MIM capacitor temperature coefficient.

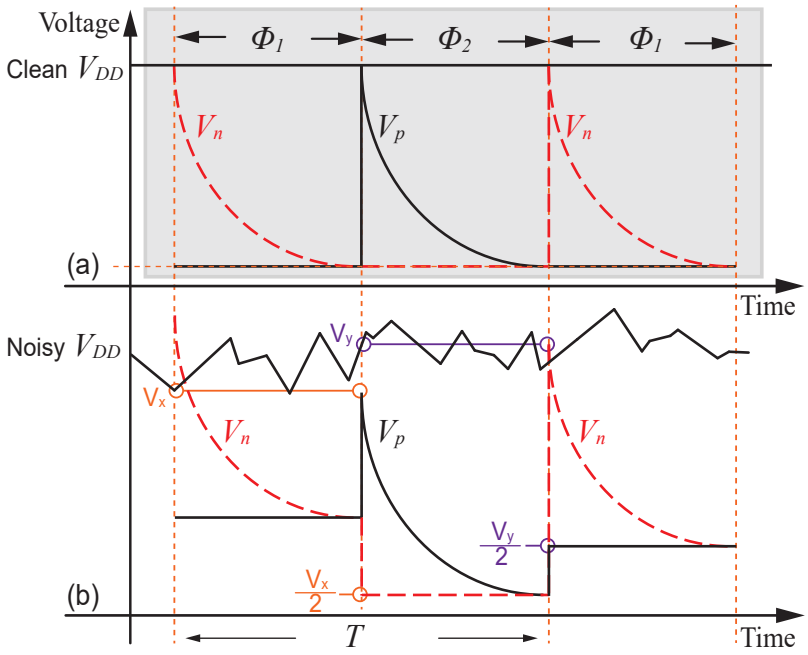


**Figure 2.8**: Waveforms with (a) clean $V_{DD}$ and (b) noisy $V_{DD}$ illustrating that the period based on the decaying exponential is independent of $V_{DD}$. For simplicity, comparator offset is not shown.

For this reason, the frequency stability of the proposed oscillator architecture is likely to be more largely affected by the temperature dependency of the effective resistances of the discharging paths (kHz-range oscillator) and by the comparator (Hz-range oscillator).

### Resistors

Resistors are employed to serve as discharging paths in the kHz-range oscillator. As shown in Fig. 2.9(a), resistors usually show significant temperature dependency. Fortunately, different resistor types can exhibit opposite temperature coefficients, enabling first-order temperature compensation as illustrated in Fig. 2.9(a) [38]. The 250 nm technology used to build the kHz-range oscillator features unsilicided P+ poly resistors, $R_{PTC}$ (with a statistical spread σ/avg = 8.6%), which exhibit a positive temperature coefficient, $TC_{pos}$, of 3800 ppm/°C, while unsilicided N+ poly resistors, $R_{NTC}$ (with a statistical spread σ/avg = 8.2%), exhibit a negative 610 ppm/°C temperature coefficient, $TC_{neg}$. A temperature-stable discharging path is thus achieved by placing

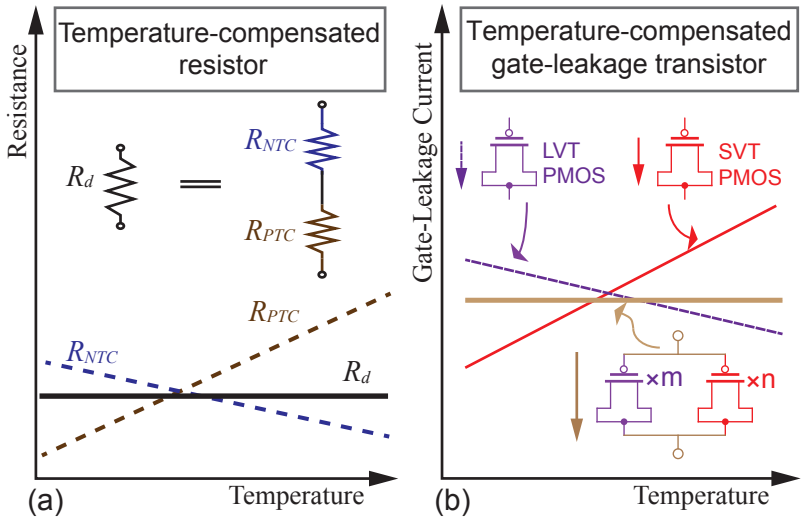


**Figure 2.9**: Temperature compensation by (a) placing resistors of opposite temperature coefficients in series and (b) gate-leakage transistors of opposite leakage temperature coefficients in parallel.

a $R_{PTC}$ in series with $R_{NTC}$ sized according to:

$$\frac{R_{PTC}}{R_{NTC}} = \frac{|TC_{neg}|}{|TC_{pos}|}. \tag{2.5}$$

Unfortunately, resistors typically exhibit non-linear temperature dependencies, which limits the achievable temperature compensation (Fig. 2.10(a)). In addition, the resistance of $R_{PTC}$ and $R_{NTC}$ change due to process variation, which can result in $R_{PTC}$ and $R_{NTC}$ drifting from the optimal point given by Equation 2.5 and therefore further deteriorate the achievable temperature coefficient of the temperature-compensated resistor $R_d$. As shown in Fig. 2.10(b), Monte Carlo simulation shows that the temperature-compensated resistor $R_d$ achieves an average temperature coefficient of 37 ppm/°C with a 3σ deviation of 55 ppm/°C across the temperature range of -20 °C to 80 °C without trimming.

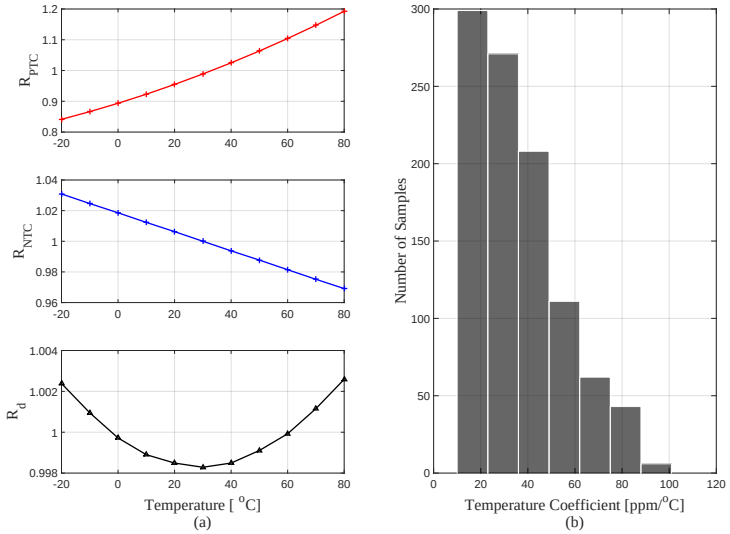


**Figure 2.10**: (a) Normalized resistance versus temperature of the unsilicided P+ poly resistor ($R_{PTC}$), unsilicided N+ poly resistor ($R_{NTC}$), and temperature-compensated resistor ($R_d$). (b) 1000-point Monte Carlo simulation of the temperature-compensated resistor showing an average temperature coefficient of 37 ppm/°C with a 3σ deviation of 55 ppm/°C. For simplicity, absolute value of the temperature coefficient was used in the simulation.

### Gate Leakage Transistors

Gate-leakage transistors are employed as resistive discharging paths for the Hz-range oscillator. While single gate-leakage transistors can implement very large effective resistors, tunneling currents show significant temperature variation [36]. Fortunately, tunneling currents can exhibit different temperature coefficients for different transistor types when identical voltages are applied across the gate oxides. In the 65 nm process used to implement the Hz-range oscillator, SVT and low-$V_T$ (LVT) PMOS transistors show opposite temperature coefficients with gate-leakage current statistical spreads (σ/avg) of 36.1% and 36.2%, and gate-leakage current temperature coefficient statistical spreads (σ/avg) of 8.7% and 6.9%, respectively. Thus, a passively-temperature-stabilized gate-leakage resistance can be obtained by placing appropriately sized SVT and LVT PMOS transistors in parallel as shown in Fig. 2.9(b). Note that the absolute gate-leakage current and the temperature coefficient change when different gate voltages are

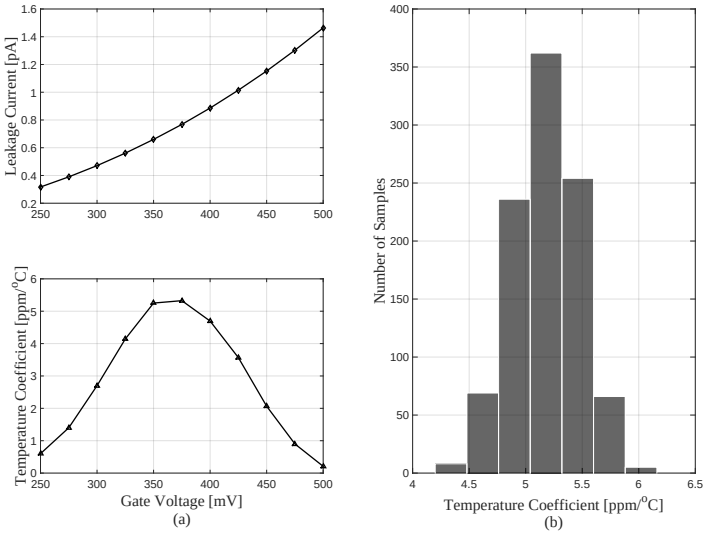


**Figure 2.11**: Simulated gate-leakage current ((a) top) and temperature coefficient ((a) bottom) of the temperature-compensated gate-leakage transistor when biased at different gate voltages. (b) Monte Carlo simulation shows the temperature-compensated gate-leakage current achieves an average temperature coefficient of 5.2 ppm/°C with a 3σ deviation of 1 ppm/°C. Note that in the Monte Carlo simulation, gate voltage was first swept from 0.25 V to 0.5 V and the worst case temperature coefficient was recorded for each Monte Carlo run.

applied (Fig. 2.11(a)). Therefore, SVT and LVT PMOS transistors are sized such that the worst case temperature coefficient is minimized over a single switching cycle. As shown in Fig. 2.11(b), the current of the temperature-compensated gate-leakage transistor achieves an average temperature coefficient of 5.2 ppm/°C with a 3σ deviation of 1 ppm/°C over 1000 Monte Carlo simulations, while the uncompensated LVT and SVT gate-leakage currents show average temperature coefficients of 26 ppm/°C and 129 ppm/°C, respectively. This two transistor design ensures that the temperature stability of gate-leakage devices does not dominate the temperature performance of the overall oscillator, which, as will be shown in the following subsection, is in fact dominated by the comparator performance.

Note that, when discharging the MIM capacitors $C_{d,\{n,p\}}$ through the gate-leakage transistor, both a capacitive division, resulting from the parasitic MOS capacitance of the leakage-gate transistors $G_{d,\{n,p\}}$, and RC discharging occur (Fig. 2.6). As discussed in Section 2.4, capacitors

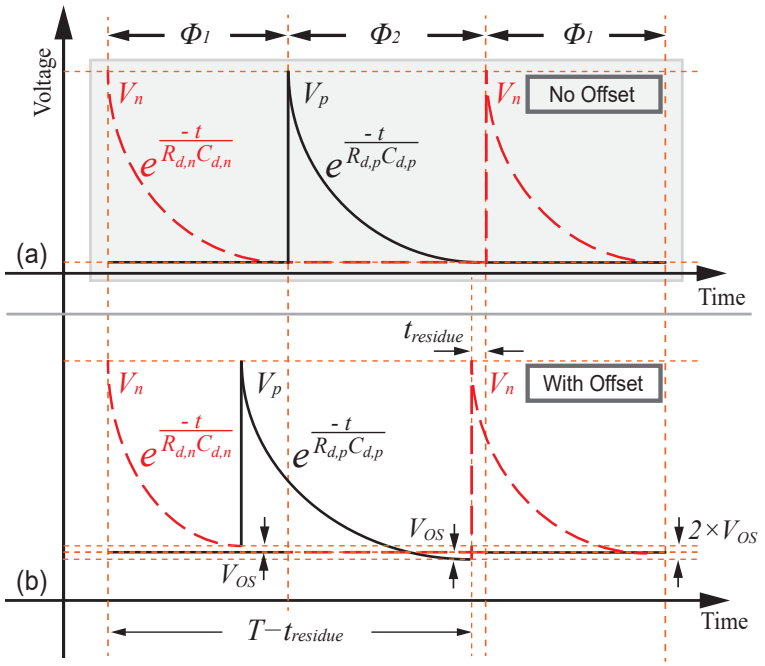


**Figure 2.12**: Waveforms with (a) no comparator offset and (b) a positive offset voltage, $V_{OS}$, at the input $V_p$ of the comparator, illustrating that the proposed architecture is able to cancel the comparator offset through averaging.

$C_{d,\{n,p\}}$ are sized to be 1.1 pF while the temperature-compensated gate-leakage transistor occupies an area of 200 $\mu$m$^2$, showing a MOS capacitance of 0.25 pF with a temperature coefficient of 270 ppm/°C. Therefore, the equivalent total capacitance, $C_{eqv}$, is 1.35 pF with an effective temperature coefficient of 50 ppm/°C, although the leakage and temperature coefficient of the MIM capacitor is negligible [35].

### Comparator

The input-referred offset voltage of a comparator also exhibits temperature dependencies [25], manifesting in lower than desired frequency stability. Fortunately, the capacitive-discharging architecture shows an intrinsic ability to reject comparator offset through the chopping action [26]. As shown in Fig. 2.12, the decaying voltage and the reference voltage alternately apply to the two inputs of the comparator in adjacent clock cycles, thereby cancelling, to a first order,

the comparator offset voltage through averaging. Since the profile of the decaying voltage is exponential, rather than linear, there is a residual error. As shown in Fig. 2.12, the comparator offset voltage, $V_{OS}$, is sampled onto the reference voltage in phase $\Phi_1$, and therefore the half period $T_{\Phi_1}$ can be calculated by:

$$\frac{C_{c1,p}V_{DD}}{C_{c1,p}+C_{c2,p}}+V_{OS}=V_{DD}e^{-\frac{T_{\Phi_1}}{R_{d,n}C_{d,n}}}. \tag{2.6}$$

In this case, the elements in the upper branch and lower branch are sized the same. On the other hand, in phase $\Phi_2$, $V_{OS}$ is sampled onto the decaying voltage, resulting in the other half period $T_{\Phi_2}$, which can be calculated by:

$$\frac{C_{c1,p}V_{DD}}{C_{c1,p}+C_{c2,p}}=V_{DD}e^{-\frac{T_{\Phi_2}}{R_{d,n}C_{d,n}}}+V_{OS}. \tag{2.7}$$

Therefore, with a comparator offset voltage of $V_{OS}$, the oscillation period $T_{OS}$ becomes:

$$T_{OS}=T_{\Phi_1}+T_{\Phi_2}=-R_{d,n}C_{d,n}\{\ln(\frac{C_{c1,p}}{C_{c1,p}+C_{c2,p}}+\frac{V_{OS}}{V_{DD}})+\ln(\frac{C_{c1,p}}{C_{c1,p}+C_{c2,p}}-\frac{V_{OS}}{V_{DD}})\}. \tag{2.8}$$

The period deviation, $\Delta T$, due to the comparator offset can be obtained by subtracting $T_{OS}$ from the ideal period $T$ in Equation 2.4, giving:

$$\Delta T=-R_{d,n}C_{d,n}\{\ln(1+\frac{V_{OS}}{V_{DD}}\frac{C_{c1,p}+C_{c2,p}}{C_{c1,p}})+\ln(1-\frac{V_{OS}}{V_{DD}}\frac{C_{c1,p}+C_{c2,p}}{C_{c1,p}})\}. \tag{2.9}$$

However, if there's no chopping action during the operation of the oscillator, the oscillation period, $T_{OS,NC}$, would otherwise be given by:

$$T_{OS,NC}=-2R_{d,n}C_{d,n}\ln(\frac{C_{c1,p}}{C_{c1,p}+C_{c2,p}}\pm\frac{V_{OS}}{V_{DD}}), \tag{2.10}$$

leading to a period deviation, $\Delta T_{NC}$ of:

$$\Delta T_{NC} = -2R_{d,n}C_{d,n}\ln(1 \pm \frac{V_{OS}}{V_{DD}}\frac{C_{c1,p}+C_{c2,p}}{C_{c1,p}}). \tag{2.11}$$

From Equations 2.9 and 2.11, the ability to reject the comparator offset of the capacitive-discharging architecture can be quantified by:

$$\frac{\Delta T_{NC}}{\Delta T} = \frac{2\ln(1 \pm \frac{V_{OS}}{V_{DD}}\frac{C_{c1,p}+C_{c2,p}}{C_{c1,p}})}{\ln(1+\frac{V_{OS}}{V_{DD}}\frac{C_{c1,p}+C_{c2,p}}{C_{c1,p}}) + \ln(1-\frac{V_{OS}}{V_{DD}}\frac{C_{c1,p}+C_{c2,p}}{C_{c1,p}})}. \tag{2.12}$$

By employing the second order Taylor Series expansion of the natural logarithm, Equation 2.12 can be quantitatively estimated by

$$\frac{\Delta T_{NC}}{\Delta T} \approx \frac{2(\pm(\frac{V_{OS}}{V_{DD}}\frac{C_{c1,p}+C_{c2,p}}{C_{c1,p}}) - \frac{1}{2}(\frac{V_{OS}}{V_{DD}}\frac{C_{c1,p}+C_{c2,p}}{C_{c1,p}})^2)}{-(\frac{V_{OS}}{V_{DD}}\frac{C_{c1,p}+C_{c2,p}}{C_{c1,p}})^2} = 1 \mp 2\frac{V_{DD}}{V_{OS}}\frac{C_{c1,p}}{C_{c1,p}+C_{c2,p}}. \tag{2.13}$$

In the implementation of the Hz-range oscillator, for example, with $C_{c1,p} = C_{c2,p}$, $V_{DD}$ = 500 mV, and an offset voltage of 10 mV ($\approx 1\sigma$ from the mean comparator offset voltage at room temperature at TT corner), Equation 2.13 indicates a frequency variation rejection of 33 dB. Simulations were carried out to validate Equation 2.13. An ideal comparator without any offset was first used to obtain a nominal frequency, $f_0$. With an offset voltage of 10 mV applied to the comparator, the oscillation frequency of the proposed capacitive-discharging architecture shows a deviation of 0.55% with respect to $f_0$, while the oscillation frequency shows a deviation of 10.4% without chopping. Therefore, the simulation results reveal that the Hz-range oscillator is able to reduce the frequency variation due to comparator offset by 25.5 dB, which is in reasonably good accordance with Equation 2.13, though with more realistic non-idealities included. The same analysis applies to the kHz-range oscillator and simulation result shows the kHz-range oscillator is able to reduce the frequency variation by over 38 dB, in good accordance with Equation 2.13

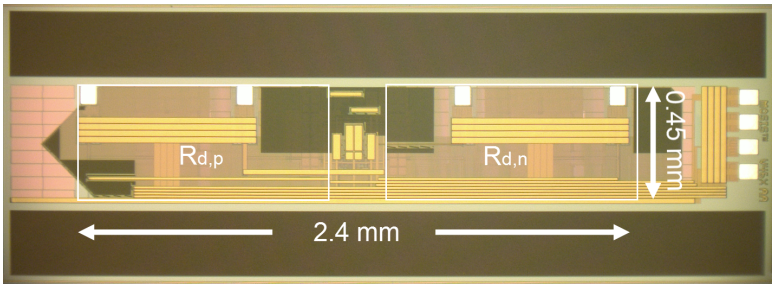


**Figure 2.13**: Micrographs of the kHz-range capacitive-discharging oscillator, occupying an area of 2.4 mm×0.45 mm.

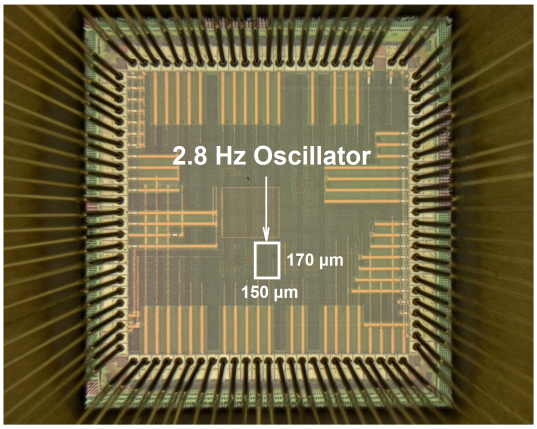


**Figure 2.14**: Micrographs of the Hz-range capacitive-discharging oscillator, occupying an area of 0.15 mm×0.17 mm..

which gives 40 dB when the kHz-range oscillator operates at $V_{DD}$ = 800 mV with $C_{c2,p} = 3C_{c1,p}$ and a comparator offset voltage of 4 mV at room temperature at the TT corner.

Note that the comparator offset voltage is not constant over temperature, and can thus introduce temperature dependencies if $V_{OS}$ is large. To determine the effect of temperature on offset voltage in the presence of variation, 500-point Monte Carlo simulations at TT corner were performed at 10 °C steps from -40 °C to 60 °C for the Hz-range oscillator. As shown in Fig. 2.15, $V_{OS}$ varies across the temperature range of -40 °C to 60 °C by an average of 36 mV (3σ from mean = 30 mV). The frequency variation due to residual comparator offset can be calculated by Equation 2.8, totaling an average of 230 ppm/°C with a 3σ deviation of 477 ppm/°C to the

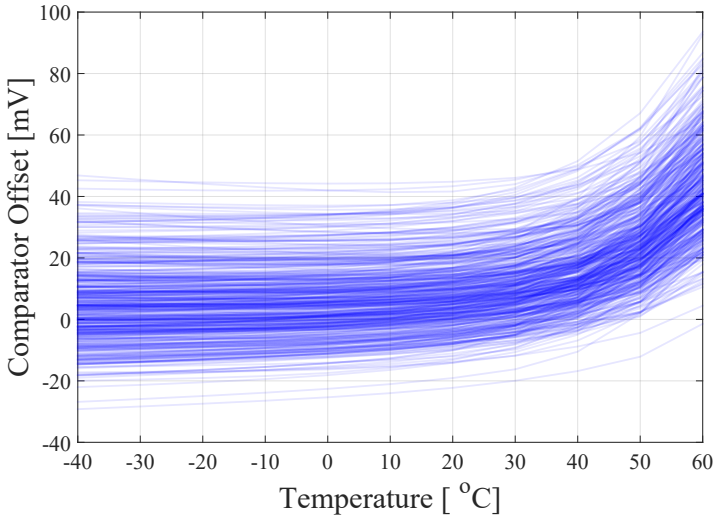


**Figure 2.15**: Simulated offset voltage of the comparator in the Hz-range oscillator showing that $V_{OS}$ varies across the temperature range of -40 °C to 60 °C by an average of 36 mV (3σ from mean = 30 mV) in the Monte Carlo simulations at TT corner.

oscillation frequency of the Hz-range oscillator.

In addition, frequency stability is also affected by variation in the comparator delay, $t_{delay}$. The bandwidths of the comparator is set to be 1.5 kHz such that the delay is nominally less than 0.1 % of the oscillation period for the Hz-range oscillators [39]. However, $t_{delay}$ shows a temperature variation of over 7x across the temperature range of -40 °C to 60 °C, contributing a variation of over 70 ppm/°C to the oscillation frequency. Therefore, after chopping, the residual offset voltage along with comparator delay and the temperature-compensated gate-leakage transistors determines the frequency stability of the Hz-range oscillator. In the other implementation (kHz-range oscillator), the influence of the residual comparator offset is minimized by employing large input-stage transistors for the comparator and therefore obtaining smaller $V_{OS}$, as well as a higher supply voltage (0.8 V) as indicated by Equation 2.8. To minimize the impact of $t_{delay}$ variation across temperature, the bandwidth of the comparator is set to be 550 kHz ($t_{delay} < 0.8$ % of the oscillation period) while a PTAT bias current is employed ($t_{delay}$ varies by less than 24%), totaling less than 19 ppm/°C to the oscillation frequency. Thus, the frequency stability of the kHz-range

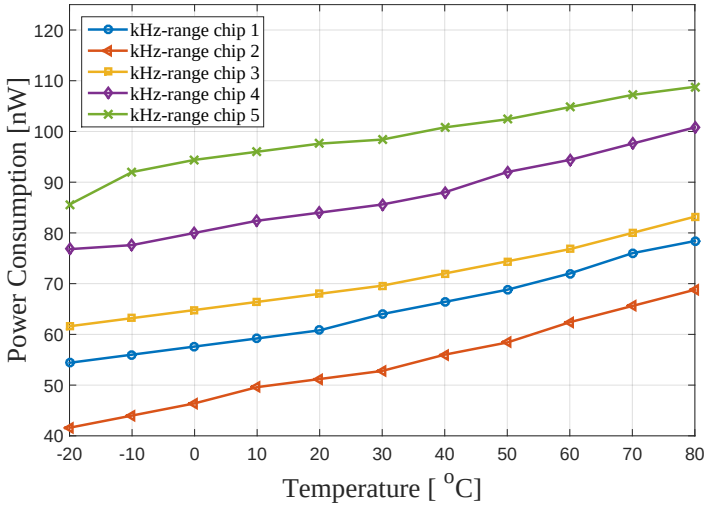


**Figure 2.16**: Measured power of the kHz-range oscillator versus temperature for 5 samples when operating from -20 to 80 $^{o}$C.

**Table 2.1**: Scalability of the Proposed Reference-Free Capacitive-Discharging Oscillator Architecture

| Process | TC (ppm/°C) | | $R_{seg}$ (Ω/□) \| $W_{min}$ | | Chip Area (mm$^2$) |
|---|---|---|---|---|---|
| | $R_{NTC}$ | $R_{PTC}$ | $R_{NTC}$ | $R_{PTC}$ | |
| 250 nm | -610 | 3800 | 200 \| 2 $\mu$m | 1.1k \| 3 $\mu$m | 1.08 |
| 65 nm | -840 | 180 | 264 \| 0.24 $\mu$m | 31k \| 1 $\mu$m | <0.08 |

oscillator is primarily determined by the temperature-compensated resistors.

## 2.4 Experimental Results

The kHz-range and Hz-range reference-free capacitive-discharging oscillators are implemented in 250 nm and 65 nm processes, respectively, and their die photos are shown in Figs. 2.13 and 2.14.

*1) Area*: The kHz-range reference-free capacitive-discharging oscillator occupies an area of 1.08 mm$^2$ and oscillates at a nominal frequency of 6.4 kHz. As shown in Fig. 2.4, capacitors $C_{d,\{n,p\}}$ are sized to be 2.7 pF, to trade off between frequency variation due to leakage and dynamic power. Capacitors $C_{c1,\{n,p\}}$ and $C_{c2,\{n,p\}}$ are sized to be 0.9 pF and 2.7 pF, respectively,

**Table 2.2**: Comparison With Previously Published State-of-the-Art kHz-Range Oscillators

| kHz-Range Timers | [23] VLSI'12 | [24] VLSI'12 | [25] ISSCC'13 | | [26] JSSC'09 | [27] ISSCC'14 | [28] VLSI'15 | **This Work** | |
|---|---|---|---|---|---|---|---|---|---|
| **Process** | 90 nm | 60 nm | 65 nm | | 65 nm | 65 nm | 180 nm | **250 nm** | |
| **Oscillator Principle** | Relaxation | Relaxation | Relaxation | | Relaxation | Relaxation | Relaxation | **Capacitive Discharging** | |
| **Supply Voltage** | 0.8 V | 1.6 V | 1 V | | 1.2 V | 1.25 V | 1.2 V | **0.8 V** | |
| **Frequency [kHz]** | 100 | 32.768 | 18.5 | | 100 | 33 | 70.4 | **6.4** | |
| **Frequency Spread($\sigma$/avg)** | N/A | N/A | N/A | | $< 0.36\%^{*}$ | $2.2\%^{\$}$ | N/A | **2.1%** | |
| **Power [nW]** | 280 | 4480 | $120^{\#}$ | | 20800 | 190 | 99.4 | **For 5 Samples** | |
| | | | | | | | | **avg = 75.6** | **$\sigma$ = 13.3** |
| **Power Efficiency [pJ/Cycle]** | 2.8 | 136.7 | $6.4^{\#}$ | | 208 | 5.7 | 1.41 | **11.8** | |
| **Temperature Accuracy [%]** | $\pm$0.68 | $\pm$0.1 | $\pm$0.25 | $\pm$0.1 | $\pm$1.1 | $\pm$0.21 | 27.4 ppm/$^{o}$C | **For 5 Samples** | |
| | | | | | | | | **avg = $\pm$0.74** | **$\sigma$ = 0.086** |
| **Temperature Range [°C]** | -40 to 90 | -20 to 100 | -40 to 90 | 0 to 90 | -22 to 85 | -20 to 90 | -40 to 80 | **-20 to 80** | |
| **Voltage Accuracy [%/V]** | 9.4 | 0.06 | 1 | | 0.37 | 0.09 | 0.5 | **1.8** | |
| **Voltage Range [V]** | 0.725 - 0.9 | 1.6 - 3.2 | N/A | | 1.12 - 1.39 | 1.15 - 1.45 | 1.2 - 3 | **0.6 - 0.9** | |
| **Area [mm$^2$]** | 0.12 | 0.048 | 0.032 | | 0.11 | 0.015 | 0.26 | **1.08** **<0.08 if scaled to 65 nm** | |
| **Off-Line Calibration Cost** | Not Reported | Not Reported | Not Reported | | One-Point Calib. | One-Point Calib. | Not Reported | **No Calib. Performed** (May need one-point calib.) | |
| **Allan Deviation Floor** | N/A | N/A | < 20 ppm | | $\approx$ 1000 ppm | < 4 ppm | < 7 ppm | < **60 ppm** | |

$^{*}$ Measured over the range from -22 °C to 85 °C.
$^{\$}$ Calculated from Fig. 17.8.3.
$^{\#}$ The power of PTAT current reference that works from a supply voltage of 1.5 V - 3.3 V and draws 25 nA is not included.

**Table 2.3**: Comparison With Previously Published State-of-the-Art Hz-Range Oscillators

| Hz-Range Timers | [30] CICC'07 | [29] ISSCC'09 | [31] JSSC'13 | [32] CICC'14 | [33] VLSI'15 | **This Work** | |
|---|---|---|---|---|---|---|---|
| **Process** | 130 nm | 130 nm | 130 nm | 180 nm | 180 nm | **65 nm** | |
| **Oscillator Principle** | Gate-Leakage Based | Program-and-Hold | Gate-Leakage Based | Relaxation | Program-and-Hold | **Capacitive Discharging** | |
| **Supply Voltage** | 0.45 V | 0.6 V | 0.7 V (1.2 V for $V_{DDH}$) | 1.2 V | 0.6 V | **0.5 V** | |
| **Frequency [Hz]** | 0.09 | 11.11 | $\sim 5$ | 11 | 18 | **2.8** | |
| **Frequency Spread (σ/avg)** | 28% | N/A | N/A | N/A | N/A | **11.8%** | |
| **Power [pW]** | 120[b] | 150[c] | 660 | 5,800 | 4.2 | **For 5 Samples** | |
| | | | | | | **avg = 44.4** | **σ = 6.4** |
| **Power Efficiency [pJ/Cycle]** | 1333 | 13.5 | 132 | 527.2 | 0.23 | **15.8** | |
| **Temperature Accuracy [ppm/°C]** | 1600 | 490 | 31 | 45 | 20,000[d] 4,000[e] | **For 5 Samples** | |
| | | | | | | **avg = 1260** | **σ = 280** |
| **Temperature Range [°C]** | 0 to 80 | 0 to 90 | -20 to 60 | -10 to 90 | -30 to 60[d] -30 to 40[e] | **-40 to 60** | |
| **Voltage Accuracy [%/V]** | 150 | 60 | N/A | 1 | N/A | **160** | |
| **Voltage Range [V]** | 0.4 - 0.5 | 0.55 - 0.65 | N/A | 1.2 - 2.2 | N/A | **0.48 - 0.52** | |
| **Area [$\mu$m$^2$]** | 480 | 19,000 | 15,300[a] | 240,000 | N/A | **25,500** | |
| **Off-Line Calibration Cost** | Not Reported | Not Reported | Multiple-Point Calib. | Not Reported | Not Reported | **No Calib. Performed** (May need one-point calib.) | |
| **Allan Deviation Floor** | N/A | N/A | N/A | $<$ 60 ppm[f] | N/A | $<$ **500 ppm** | |

[a] The area of the Timer and Controller is 10,500 $\mu$m$^2$ and 4,800 $\mu$m$^2$, respectively.
[b] Operates at 450 mV.
[c] 100 pW when refreshed every 4 minutes.
[d] System, $V_{DD}$ = 600 mV, denominator = midpoint of range.
[e] Core, $V_{DD}$ = 600 mV, denominator = midpoint of range.
[f] Read from Fig. 7.

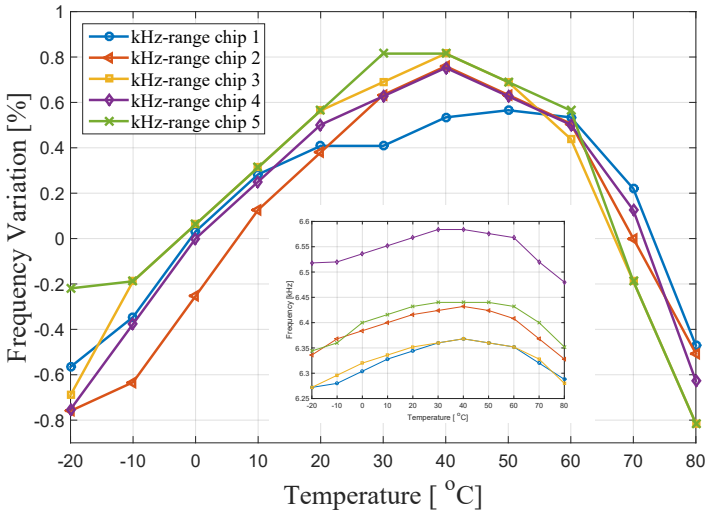


**Figure 2.17**: Measured frequency which is normalized to the mid-point of the range (the small plot shows the unnormalized frequency) of the kHz-range oscillator versus temperature for 5 samples.

while resistors $R_{d,\{n,p\}}$ are sized to be 20 MΩ. The highest impedance resistor available in the employed 250 nm CMOS process that exhibits a negative temperature coefficient, $R_{NTC}$, has a temperature coefficient of -610 ppm/°C, and has a segment resistance of 200 Ω/□ with a minimum width of 2 $\mu$m, i.e., $R_{NTC}$ has a normalized resistance of 50 Ω/$\mu$m$^2$ when employing the minimum width. The highest impedance positive temperature coefficient resistor available in the 250 nm CMOS process, $R_{PTC}$, exhibits a temperature coefficient of 3800 ppm/°C and has a segment resistance of 1.1 kΩ/□ with a minimum width of 3 $\mu$m, i.e., $R_{PTC}$ has a normalized resistance of 122 Ω/$\mu$m$^2$ when employing the minimum width. Therefore, the temperature compensated resistors $R_{d,\{n,p\}}$ together have a normalized resistance of 1 kΩ per 18 $\mu$m$^2$, i.e. 55.6 Ω/$\mu$m$^2$. Thus, as shown in Fig. 2.13, the resistors $R_{d,\{n,p\}}$ occupy a total area of 1.01 mm$^2$, which is 93% of the total die area. Note that the proposed architecture will occupy a much smaller area in scaled technologies. For example, in a 65 nm process, opposite temperature coefficient resistors {180 ppm/°C, -840 ppm/°C} with segment resistances of {31 kΩ/□, 264 Ω/□} and minimum widths of {1 $\mu$m, 0.24 $\mu$m} are available. Therefore a temperature-compensated resistor with an

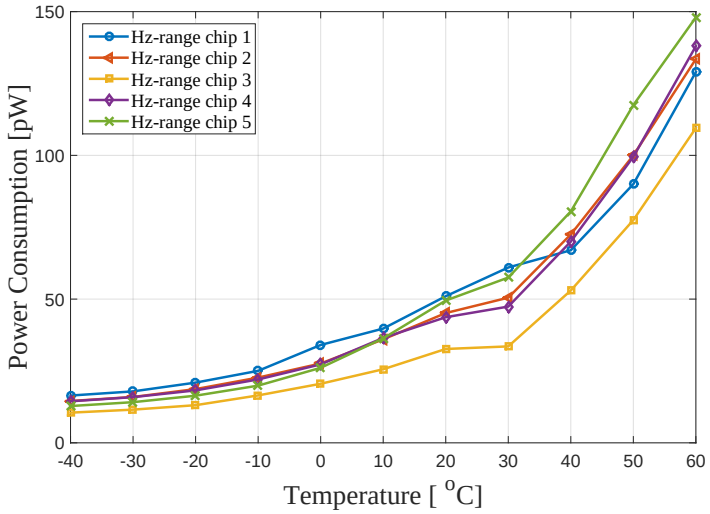


**Figure 2.18**: Measured power of the kHz-range oscillator versus temperature from -40 to 60 $^{o}$C for 5 samples.

equivalent normalized resistance of 15 k$\Omega/\mu$m$^2$ can be obtained, which means the resistors used in the implemented circuit could instead occupy an area of less than 0.003 mm$^2$. Thus, the total area of the kHz-range oscillator can be decreased by more than 93% by also taking into account higher-density capacitors available in scaled technologies. As a result, the proposed architecture shows good scalability with advanced technologies as summarized in Table 2.1. Meanwhile, the Hz-range oscillator occupies an area of 0.0255 mm$^2$ and oscillates at 2.8 Hz. In Fig. 2.5, capacitors $C_{d,\{n,p\}}$ are sized to be 1.1 pF, capacitors $C_{\{c1,c2\},\{n,p\}}$ are sized to be 4.5 pF, and gate-leakage transistors $G_{d,\{n,p\}}$ occupy a total area of 200 $\mu$m$^2$.

The choice of capacitor sizes must satisfy application-dependent trade offs between leakage, dynamic power, and the area of the overall oscillator. For example, in the kHz-range oscillator on-chip resistors and capacitors are used. In order to save area and minimize the dynamic power, $C_{c1,\{n,p\}}$ are thus sized to be as small as possible while keeping the leakage during one operation cycle negligible compared to the total charge stored on $C_{c1,\{n,p\}}$. $C_{c2,\{n,p\}}$ are then sized to be 3$\times$ the size of $C_{c1,\{n,p\}}$ to reduce the total area of $R_{d,\{n,p\}}$ and $C_{d,\{n,p\}}$ (Equation 2.4) while ensuring a common input voltage of 0.2 V for the comparator. Finally, $R_{d,\{n,p\}}$ and

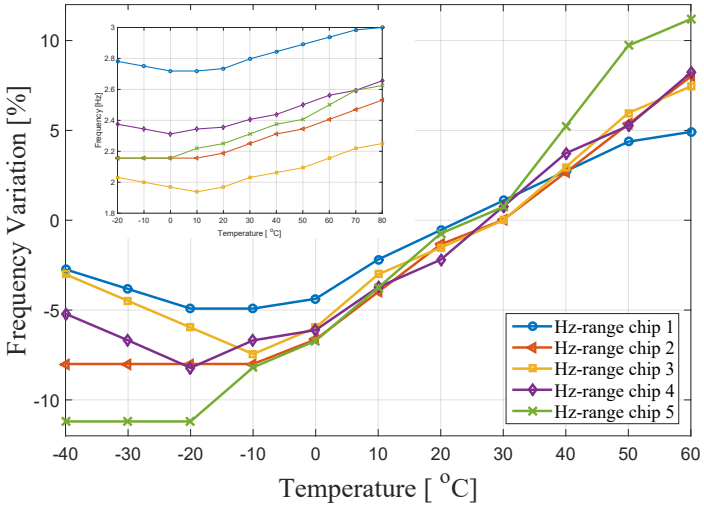


**Figure 2.19**: Measured frequency which is normalized to the mid-point of the range (the small plot shows the unnormalized frequency) of the kHz-range oscillator versus temperature for 5 samples.

$C_{d,\{n,p\}}$ are sized such that the dynamic power is minimized while consuming acceptable area.

Similar analysis applies to the sizing of the components in the Hz-range oscillator. Since the Hz-range oscillator operates with a much longer cycle, the leakage becomes more important and therefore a larger $C_{c1,\{n,p\}}$ is employed to compensate for the leakage. In addition, since it works at a supply voltage of 0.5 V, $C_{c2,\{n,p\}}$ are sized to be the same as $C_{c1,\{n,p\}}$ to ensure a common input voltage of 0.25 V for the comparator.

*2) Power*: Operating from a 0.8 V supply, the kHz-range oscillator, measured across 5 samples, consumes an average power of 75.6 nW at 20 °C as shown in Fig. 2.16, which is the lowest reported power for a frequency-stabilized oscillator operating at kHz-range frequencies. Across a temperature range of -20 °C to 80 °C, the power of the kHz-range oscillator reaches a maximum of 109 nW and a minimum of 41 nW, and a standard deviation of 13.3 nW (or 17.6%).

Operating from a 0.5 V supply, measurements over 5 samples of the implemented Hz-range oscillator reveal an average power of 44.4 pW at 20 °C as shown in Fig. 2.18, which is amongst the lowest power designs previously reported. As shown in Fig. 2.18, the Hz-range

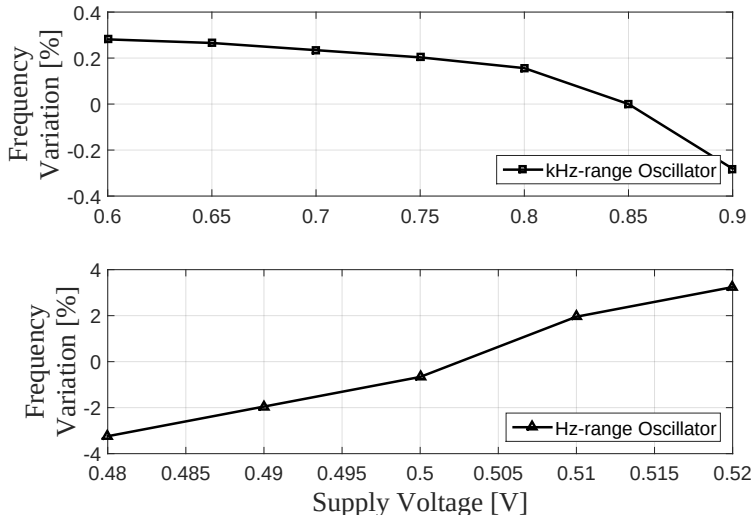


**Figure 2.20**: Measured Frequency variation versus supply voltage of the kHz-range (top) and Hz-range (bottom) oscillators.

oscillator achieves a maximum power of 149 pW, a minimum power of 10.5 pW, and a standard deviation of 6.4 pW (or 14.4%) across a temperature range of -40 °C to 60 °C.

For benchmarking purposes, the power of an oscillator can be divided by its frequency to create an energy-per-cycle figure of merit. When operating at 6.4 kHz, the kHz-range oscillator consumes 11.8 pJ/cycle, while the Hz-range oscillator requires 15.8 pJ/cycle when operating at 2.8 Hz.

*3) Frequency Stability*: Although the capacitive-discharging topology does not employ any temperature-stabilized current or voltage references to set oscillation frequencies, the kHz-range oscillator achieves competitive supply and temperature stability. The oscillator achieves a voltage accuracy better than 1.8%/V (Fig. 2.20), and, as shown in Fig. 2.17 for a temperature range of -20 °C to 80 °C, measurements across 5 samples reveal that the oscillator obtains an average frequency variation of $\pm$0.74% (148 ppm/°C) with a standard deviation of 0.086% (8.6 ppm/°C) without any post-manufacturing calibration or trimming.

Similarly, measurement results reveal that the Hz-range oscillator shows a voltage accuracy of 160%/V (Fig. 2.20), which is dominated by the voltage dependence of gate-leakage current

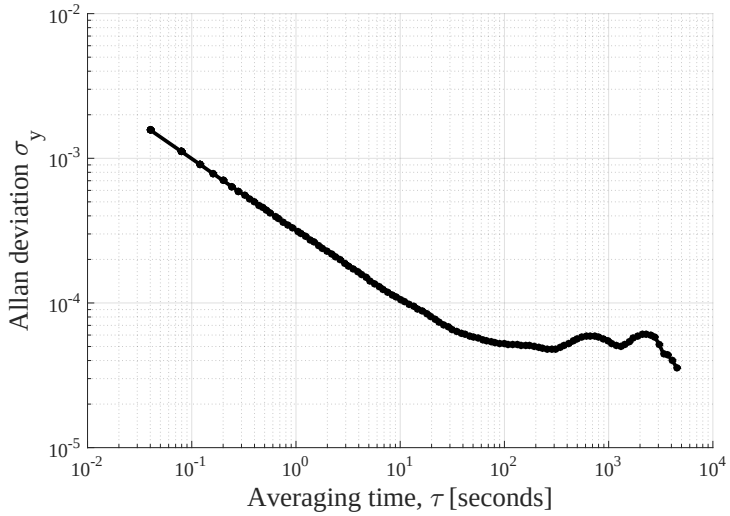


**Figure 2.21**: Measured Allan deviation for the kHz-range oscillator over 32 M periods, showing a floor set by flicker noise of $< 60$ ppm.

and comparator offset. The temperature performance of the Hz-range oscillator is shown in Fig. 2.19. From -40 °C to 60 °C, the oscillator achieves an average frequency variation as low as 1260 ppm/°C with a standard deviation of 280 ppm/°C. Note that the temperature stability can be significantly improved by better optimization of the comparator. For example, simulation result shows that a frequency variation less than 500 ppm/°C can be achieved when the offset of the comparator is less than 4 mV across the temperature range.

Measured across 5 samples, the nominal frequency (measured at 20 °C) of the kHz-range oscillator shows a spread of 2.1% (σ/avg) while the Hz-range oscillator achieves a frequency spread of 11.8%.

When employing the proposed kHz-range oscillator as a wake up timer the wireless node in Fig. 2.1(b) can achieve an average power of 136 nW at duty cycles less than $10^{-6}$. Similarly, the Hz-range oscillator can achieve an average power of 500 nW at duty cycles less than $10^{-9}$. These results indicate that the kHz-range oscillator is suitable for the wireless node in Fig. 2.1(b), while the Hz-range oscillator is more suitable for transmit-only sensor/IoT applications where power is the most important metric and a synchronized integrated received is not required. This is

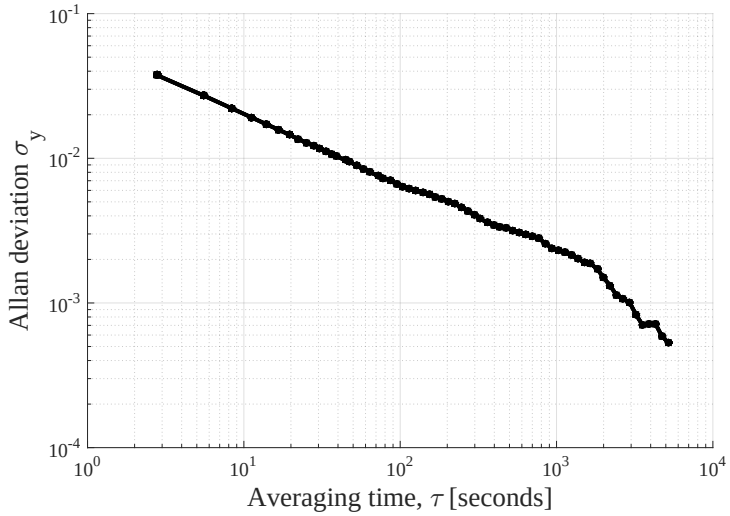


**Figure 2.22**: Measured Allan deviation for the Hz-range oscillator over 14 K periods, showing a floor of 500 ppm at minimum (limited by measurement time due to the slow clock period).

consistent with the performance of other Hz-range pW timers in the literature.

*4) Allan Deviation*: Allan deviation is a statistical measure of the long-term relative frequency instability of an oscillator. Measured over a time-span $\tau$, an Allan deviation of $\alpha$ ppm means that the expected period deviation between two subsequent sleeping periods is below $\alpha$ ppm. Measured over 5000 seconds, the measurement results reveal that the kHz-range oscillator architecture achieves an Allan deviation floor under 60 ppm at room temperature and the Hz-range oscillator exhibits an Allan deviation under 500 ppm, as shown in Fig. 2.21 and Fig. 2.22, respectively, thereby indicating the ability of the proposed reference-free capacitive-discharging topology to wake-up the main circuit after long periods of time.

*5) Post-Manufacturing Calibration Cost*: It should be noted that many state-of-the-art low-power oscillators achieve temperature- and supply-stability via expensive post-manufacturing calibrations. For example, extensive timer calibration across configurations using multiple temperature points was carried out in [31] to achieve a stable frequency. Similarly, one-point post-manufacturing trimming at room temperature is required in [26] [27] to tune resistive temperature dependencies, which also requires testing time, though less severely than two-point

testing. Most other prior-art publications do not reveal if calibration is required or was performed, and often measurement results of only a single die are shown. Although digital trimming of the core resistors would likely result in improved temperature performance and voltage accuracy in the present designs, all of the presented measurements have been carried out with zero-point calibration, i.e., no post-manufacturing calibration at all. Zero-point calibration of designs may become increasingly important in next-generation IoT applications, which may number in the trillions of devices [40], where even simple one-point calibration may be prohibitively expensive. However, the 5 samples measured for both oscillators are from the same wafer, and therefore a high deviation can potentially exist between different runs or wafers. For example, Monte Carlo simulations show that the on-chip resistors and MIM cap have a spread ($\sigma$/avg) of 7% and 3.6%, respectively, which indicates one-point frequency calibration may be required across different runs or wafers.

Tables 2.2 and 2.3 summarize the measurement results of the proposed reference-free capacitive-discharging kHz-range and Hz-range oscillators, and compare these results to state-of-the-art oscillators that can be employed to serve as long-term timers at kHz-range and Hz-range frequencies, respectively.

## 2.5 Summary

This chapter has proposed an oscillator featuring capacitive-discharging architecture that can be employed as long term timers operating at kHz-range to Hz-range frequencies. By pre-charging two charge-tanks, which can be implemented by temperature-stable MIM capacitors, to $V_{DD}$, and then allowing one to discharge through a temperature-stable resistive path, while the other charge-shares with a pre-purged capacitor to setup an implicit reference voltage, a clock period can be obtained that is independent of $V_{DD}$ without any energy-expensive reference or calibration circuits. Powered from a 0.8 V supply, a proposed kHz-range oscillator operates

at 6.4 kHz, consumes an average power of 75.6 nW, and achieves a temperature accuracy of $\pm$0.74% (148 ppm/°C) over a temperature range from -20 °C to 80 °C by employing temperature-compensated resistors as discharging paths. A second design operating at Hz-range frequencies was implemented by employing temperature-compensated gate-leakage transistors as discharging paths. Measurements across 5 samples reveal an average power consumption of 44.4 pW and a temperature stability of 1260 ppm/$^o$C. The measured Allan deviations of the kHz-range and Hz-range oscillators are under 60 ppm and 500 ppm, respectively. All of the measurements are carried out without any post-manufacturing calibration or trimming, ensuring an ultra-low-power, low-cost, and robust timer solution for next-generation wireless sensing applications.

The text of Chapter 2, in part, is a reprint of the material as it appears in "A 51 pW Reference-Free Capacitive-Discharging Oscillator Architecture Operating at 2.8 Hz" by Hui Wang and Patrick Mercier, in Proc. IEEE Custom Integrated Circuits Conference (CICC), Sep. 2015, and "A Reference-Free Capacitive-Discharging Oscillator Architecture Consuming 44.4 pW/75.6 nW at 2.8 Hz/6.4 kHz" by Hui Wang and Patrick Mercier, IEEE Journal of Solid-State Circuits (JSSC), vol. 51, no. 6, pp 1423-1435, Jun. 2016. The dissertation author was the primary investigator and author of both papers.

# Chapter 3

# A 30.6 pW 0.4 V Voltage and Current Reference Generator and A 1.6%/V 124.2 pW Relaxation Oscillator for Always-On Circuits

Advanced wireless platforms are keeping pushing power consumption boundaries to extremely low levels, commonly by aggressively duty-cycling the active circuitry. Except in the case where architecture innovations avoid their use [41], voltage and current reference generator (VCRG) is an indispensable component for most of such applications, which biases the active circuitry and therefore determines the power consumption of the active circuity. Fig. 3.1(a) shows a simplified block diagram of such platforms where the power-expensive active circuit is power-gated by the always-on circuit (e.g., watchdog timers and wakeup analog blocks) with a duty-cycle ratio of $k$ that is calculated by:

$$k = \frac{t_{wake}}{t_{wake} + t_{sleep}}, \tag{3.1}$$

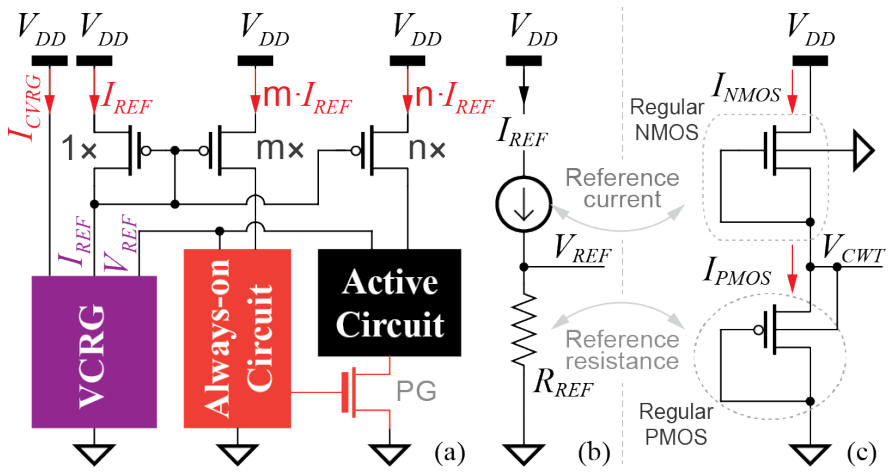


**Figure 3.1**: (a) Principle of operation of a general voltage reference generator. (b) Schematic of a regular-transistor 2T VRG core.

where $t_{wake}$ and $t_{sleep}$ are the time that the active circuit is in wake-up mode (including guard-band [41]) and sleep mode, respectively. Biased by an on-chip VCRG that generates a reference current $I_{REF}$ and a reference voltage $V_{REF}$, the current consumption of the always-on circuit and the active circuit can be readily represented by $mI_{REF}$ and $nI_{REF}$, respectively, resulting in an overall system power consumption $P_{total}$ that can be calculated by:

$$P_{total} = [I_{VCRG} + (1 + m + kn)I_{REF} + (1 - k)I_{SLP}]V_{DD}, \tag{3.2}$$

where $V_{DD}$ is the supply voltage, $I_{VCRG}$ is the current consumption of the VCRG, and $I_{SLP}$ is the sleep mode supply current of the active circuit. Note that in deeply duty-cycled systems, the duty-cycle ratio can be as low as 10 ppm [41], rendering $kn \ll (m+1)$. In addition, with careful power gating, $I_{SLP}$ can be very small and negligible. Therefore,

$$P_{total} \approx [I_{VCRG} + (1 + m)I_{REF}]V_{DD}. \tag{3.3}$$

As a result, the overall system power consumption $P_{total}$ is limited by the reference current $I_{REF}$ of the VCRG and the supply current of the VCRG and the always-on circuit ($m$ in (3.3)) at a

given supply $V_{DD}$. On the other hand, in such applications, the overall system is usually powered by an energy storage component, e.g., a battery or an energy harvesting device [7], which has very limited energy and power density, and often generate output voltage that can be small (e.g., $< 1$ V) and importantly, can vary rather significantly with charge depletion and/or environmental energy change. Note that regulated supplies are not available to help this problem since a clean voltage reference is required to establish the regulated supply in the first place. Therefore, it is imperative to design fully-integrated ultra-low-power temperature- and line-stabilized VCRGs that operate with low supply voltages and can generate ultra-low reference current (sub-nA) and low reference voltage ($< 1$ V), which can further enable temperature- and line-stabilized ultra-low-power always-on circuit (e.g., timers).

To achieve near-zero-power consumption from a sub-1V supply while minimizing temperature and line-dependence in a small area with regular CMOS transistors, a gate-leakage-based current reference circuit is presented and discussed in details in Section 3.1 [42]. Then a relaxation oscillator based on the proposed VCRG is presented in Section 3.2. Measurement results presented in Section 3.3 and 3.4 reveal that the proposed oscillator achieves the best line regulation and lowest power for comparable temperature performance, and demonstrate the significance of the proposed VCRG in the design of high-performance ultra-low-power always-on circuit.

## 3.1 Architecture of the VCRG

### 3.1.1 State-of-the-Art VCRG

The most commonly used fully-integrated VCRGs are implemented via a band-gap reference topology based on bipolar junction transistors (BJTs) [43] or parasitic vertical BJTs in standard CMOS technologies. However, band-gap reference generators typically produce 1.25 V, and thereby must operate from supply voltages higher than that. To combat this problem, alternative topologies sum PTAT and CTAT currents instead of voltages, thus enabling band-

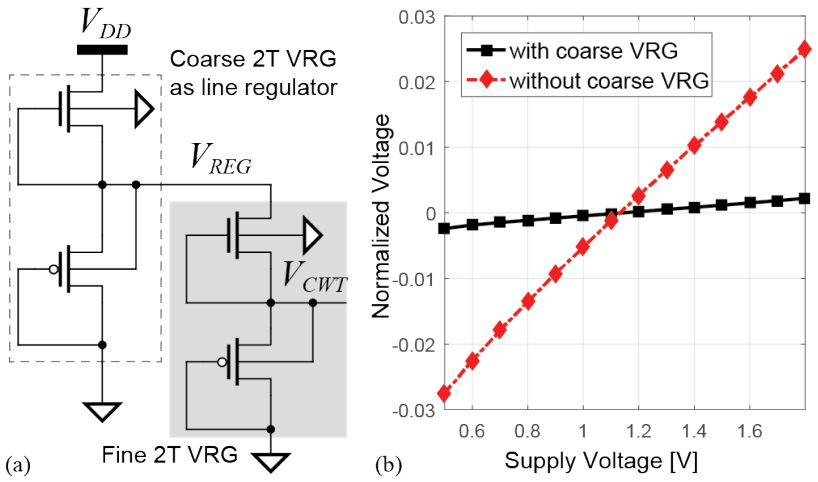


**Figure 3.2**: (a) Schematic of the self-regulated 4T voltage reference generator. (b) Simulation results of the line regulation of the reference voltage.

gap-based VCRGs operating at sub-1 V supplies [44]. However, the lowest power consumption that band-gap-based VCRGs can achieve is $>$ 1 nW [45] [46], precluding their use in sub-nW systems.

Alternative approaches have tried to implement voltage reference generator (VRG) and current reference generator (CRG) separately instead, attempting for a sub-1 V and sub-nW operation. A 2-transistor (2T) VRG structure where a native NMOS transistor is mounted on a diode connected thick-oxide NMOS transistor was presented in [47] and achieved a power consumption of 240 pW when operating at 0.5 V. However, the requirement for native NMOS tends to increase manufacturing cost since not all CMOS technologies support native devices, and those that do require extra process steps (masks). In addition, the structure does not guarantee sufficient line stability for many application, especially in scaled CMOS technologies due to strong short-channel effect. A 35 pW VRG with improved line regulation and scalable outputs was introduced in [48], however, limited by a high supply voltage (1.4 V) and the requirement of native devices. On the other hand, the most commonly used fully-integrated CRGs are based on a $\beta$ multiplier [49–51] by exploiting, e.g., self-cascode MOSFETs (SCM) [49], different temperature characteristics of different carrier mobility [50], and a modified $\beta$ multiplier that uses

a MOS resistor [51]. However, all such topologies consume above nW level power. In addition, start-up circuits are required for all such CRGs, adding area and power overhead. On the other hand, [52] achieves pW power consumption and generates pA-level current reference through use of a 2T voltage reference [47]. However, it can only operate with a supply voltage of 1.2 V or above.

### 3.1.2 sub-nW VCRG Operating at Sub-1 V

A sub-nW VCRG architecture that achieves a sub-1 V voltage and a pA-level current temperature- and line-stabilized references simultaneously, and operates from a sub-1 V supply down to 0.4 V is introduced in this section. A 4T self-regulated VCR in a push-pull topology is first presented, followed by the description of the pA-level reference current generation utilizing gate-leakage transistors.

#### 2T Regular CMOS Push-Pull CWT VRG

In general, by passing a known reference current, $I_{REF}$, through a known reference resistance, $R_{REF}$, a reference voltage can be generated, as illustrated in Fig. 3.1(b). The generated voltage can be made to be constant with temperature (CWT) by either employing temperature stabilized $I_{REF}$ and $R_{REF}$, or by utilizing an $I_{REF}$ and a $R_{REF}$ with opposite TC [53]. A schematic of a 2T CWT VRG structure is shown in Fig. 3.1(c). Here, a regular NMOS transistor and a regular PMOS transistor are configured in a push-pull-like arrangement, where the NMOS is employed to effectively act as a reference current source by connecting the gate to the source, and the PMOS is diode connected to effectively serve as a reference resistance [42]. Operating in subthreshold region, the drain current of a MOSFET is given by:

$$I_{sub} = \mu C_{ox} \frac{W}{L} (n-1) \phi_t^2 e^{\frac{V_{gs}-V_{th}}{n\phi_t}} (1 - e^{\frac{-V_{ds}}{\phi_t}}), \tag{3.4}$$

where $\mu$ is the electron/hole mobility, $C_{ox}$ is oxide capacitance, $W$ and $L$ are the transistor width and length, respectively, $n$ is subthreshold slope factor, and $\phi_t$ is thermal voltage. In the saturated subthreshold region where the drain-source voltage $V_{ds} > 4\phi_t$, the last expression in parentheses can be ignored, introducing $\sim$0.3% error [48]. Thus, the drain current of the transistor can be simplified to:

$$I_{sub} = \mu C_{ox} \frac{W}{L} (n-1) \phi_t^2 e^{\frac{V_{gs}-V_{th}}{n\phi_t}}. \tag{3.5}$$

Therefore, the drain currents of the NMOS and PMOS transistors, $I_{NMOS}$ and $I_{PMOS}$ can be calculated by (3.6) and (3.7), respectively,

$$I_{NMOS} = \mu_1 C_{ox1} \frac{W_1}{L_1} (n_1 - 1) \phi_t^2 e^{\frac{0-V_{th1}}{n_1\phi_t}}, \tag{3.6}$$

$$I_{PMOS} = \mu_2 C_{ox2} \frac{W_2}{L_2} (n_2 - 1) \phi_t^2 e^{\frac{V_{CWT}-V_{th2}}{n_2\phi_t}}. \tag{3.7}$$

Since $I_{NMOS} = I_{PMOS}$, the generated reference voltage $V_{CWT}$ can be computed by:

$$V_{CWT} = n_2 \phi_t ln \frac{\mu_1 C_{ox1} (n_1 - 1) W_1 L_2}{\mu_2 C_{ox2} (n_2 - 1) W_2 L_1} + \frac{n_1 V_{th2} - n_2 V_{th1}}{n_1}. \tag{3.8}$$

Therefore, an optimal aspect ratio of the NMOS and PMOS transistors can be calculated by (3.8) where a zero temperature coefficient is obtained,

$$\frac{\partial V_{CWT}}{\partial T} = 0 \Rightarrow \frac{(\frac{W_1}{L_1})}{(\frac{W_2}{L_2})} = \frac{\mu_2 C_{ox2} (n_2 - 1)}{\mu_1 C_{ox1} (n_1 - 1)} e^{\frac{q(n_2 \zeta_{V_{th1}} - n_1 \zeta_{V_{th2}})}{n_1 n_2 k}}, \tag{3.9}$$

where $\zeta_{V_{th1}}$ and $\zeta_{V_{th2}}$ are the temperature coefficients of the threshold voltages of the NMOS and PMOS transistors, respectively.

**Body Effect in VRG**

Note that the body and source terminals of the PMOS in the 2T VRG (Fig. 3.1(c)) are electrically connected and thus the body effect can be ignored. However, the body terminal of the NMOS is grounded while the source terminal is biased at $V_{CWT}$. Therefore, the body effect on $V_{th1}$ should be considered, which can be calculated by:

$$V_{th1} = V_{th1,0} + \gamma(\sqrt{2\phi_f + V_{CWT}} - \sqrt{2\phi_f}), \tag{3.10}$$

where $V_{th1,0}$ is the threshold voltage of the NMOS without the body effect, $\gamma$ is a body effect coefficient, and $\phi_f$ is the Fermi level. Therefore, $\zeta_{V_{th1}}$ can be calculated by

$$\zeta_{V_{th1}} = \zeta_{V_{th1,0}}\,\textcircled{1} + \gamma[\frac{1}{\sqrt{2\phi_f + V_{CWT}}}(\zeta_{\phi_f} + \zeta_{V_{CWT}})\,\textcircled{2} - \frac{1}{\sqrt{2\phi_f}}\zeta_{\phi_f}].\textcircled{3} \tag{3.11}$$

where $\zeta_{V_{th1,0}}$, $\zeta_{\phi_f}$, and $\zeta_{V_{CWT}}$ are the temperature coefficients of $V_{th1,0}$, $\phi_f$, and $V_{CWT}$, respectively. The impact of the body effect is reflected in the expression of ② in (3.11). The temperature coefficient of $\phi_f$ can be given by [54]:

$$\zeta_{\phi_f} = -\frac{1}{T}(\frac{E_g}{2q} - \phi_f), \tag{3.12}$$

where $E_g$ is then band gap of silicon at $T$ = 0 $^o$K, and $q$ is the elementary charge. As shown in (3.12), $\phi_f$ is $\sim$ 0.3 V and exhibits a temperature coefficient of $\sim -0.9$ mV/$^o$C [54]. On the other hand, A representative value of $V_{CWT}$ and temperature coefficient of $V_{CWT}$ is about 150 mV and 200 ppm/$^o$C ($\zeta_{V_{CWT}}$ = 0.03 mV/$^o$C), respectively, which is justified by the measurement results. Since: 1) $\zeta_{V_{CWT}} \ll \zeta_{\phi_f}$; 2) across a 160 $^o$C temperature range $V_{CWT}$ exhibits a change $\Delta V_{CWT}$ = 4.8 mV and results in less than 0.3% variation of ②, the body effect indicated by ② in (3.11) is minimized and can be ignored.

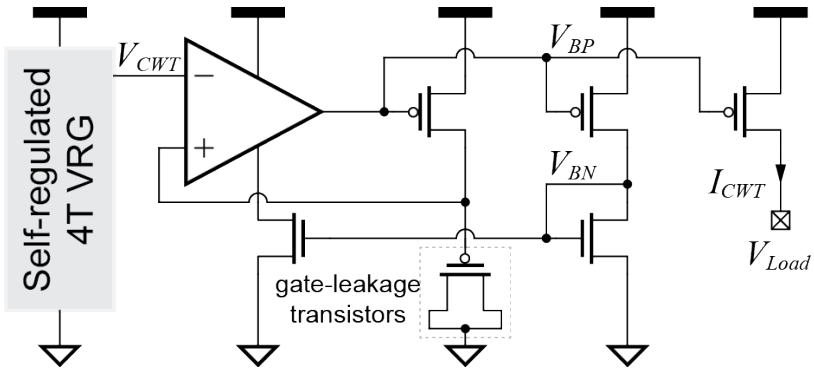


**Figure 3.3**: Schematic of the proposed ultra-low-power voltage and current reference generator operating with low supply voltage.

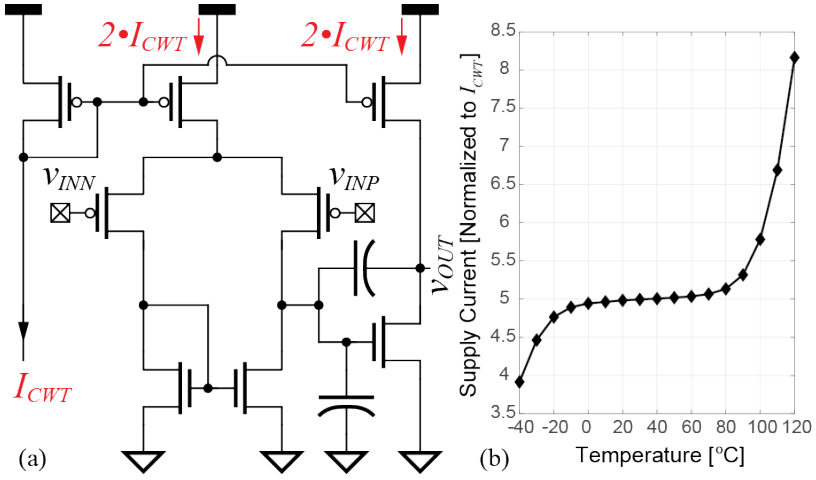


**Figure 3.4**: (a) Schematic of the 2-stage amplifier employed as voltage buffer in the VCRG. (b) Simulated supply current of the amplifier (normalized to $I_{CWT}$ when operating from -40 to 120 $^{o}$C.

### Self-Regulated 4T Architectures

A temperature- and line-stabilized $V_{CWT}$ is thus desirable for the generation of line-stable current reference. However, as CMOS technology scales, a single transistor exhibits limited supply rejection due to increased leakage between drain, source, and bulk terminals as well as other short channel effects such as DIBL. To increase the line regulation of $V_{CWT}$, a self-regulation structure is proposed where a 2T VRG is employed as a line regulator which provides a much more stable regulated supply $V_{REG}$ to a second accurate 2T VRG, as shown in Fig. 3.2(a).

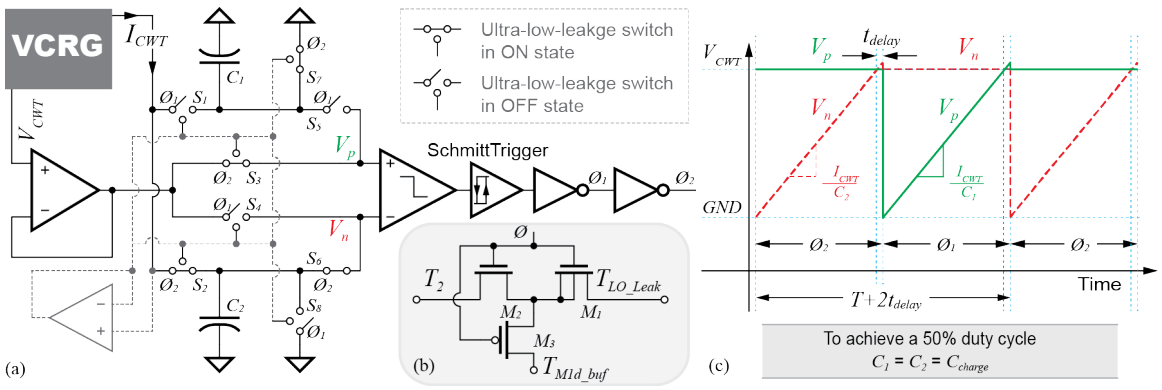


**Figure 3.5**: (a) Simplified schematic of the area efficient VCRG based oscillator (start up circuit not shown). (b) Schematic of the ultra-low-leakage switch. (c) Transient waveforms of $V_p$ and $V_n$ at the input of the comparator.

Simulation results in Fig. 3.2(b) reveal that the proposed 4T structure improves line regulation by over 11× compared the 2T VRG.

### Compact pA Current Reference Generation

Tunneling current through gate becomes prominent in scaled CMOS technology, which can be employed to effectively serve as a large on-chip resistor [41]. To further minimize the temperature dependence of the tunneling current, transistors of opposite gate-leakage TC (e.g., standard threshold and low threshold PMOS transistors in the implementation) are employed to operate in parallel [42]. As shown in Fig. 3.3, the proposed current reference architecture consists of a 4T VRG, a self-biased buffer composed of a two-stage amplifier, and a temperature-compensated gate-leakage array. The gate-leakage array is employed as the current core, which is biased by the temperature- and supply-stabilized reference voltage $V_{CWT}$ generated by the 4T VRG, via the low-power self-biased buffer, thereby resulting in a low-power, compact architecture that can operate from low supply voltages with inherent temperature- and supply-stability.

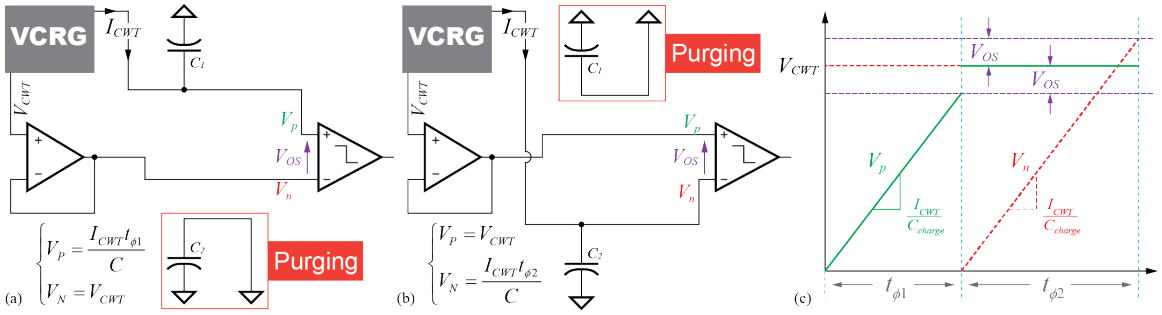


**Figure 3.6**: (a) Simplified schematic of the oscillator in $\phi_1$. (b) Simplified schematic of the oscillator in $\phi_2$. (c) Transient waveforms of $V_p$ and $V_n$ at the input of the comparator considering the comparator offset. For simplicity, the delay is not shown in the plot.

### Self-Biased Amplifier

Since the drain currents flowing through the NMOS and PMOS transistors are required to be the same for temperature-stable $V_{CWT}$ and are on pA-level, $V_{CWT}$ cannot be utilized to drive a resistive load directly. Therefore, a self-biased amplifier is employed to serve a voltage buffer. As shown in Fig. 3.4(a), a 2-stage amplified is biased by the generated pA-level current reference, $I_{CWT}$, thus ensuring an ultra-low power consumption (current consumption $\approx 5I_{CWT}$). As shown in Fig. 3.4(b), the current consumption remains constant across the temperature range from -40 to 100 $^o$C since $I_{CWT}$ is temperature-stable. However, at temperatures above 100 $^o$C, the supply currents increase exponentially (from $5I_{CWT}$ to $8.2I_{CWT}$) due to drastically increased static leakage current at high temperature, which is in good accordance with the measurement results. The self-biased amplifier is designed with a unity gain bandwidth of 1.3 kHz and a DC gain higher than 90 dB, ensuring a voltage resolution higher than 32 ppm.

## 3.2 Architecture of the VCRG-Based Oscillator

Prior-art on sub-nW oscillator structures will first be studied in this section. A relaxation oscillator based on the proposed VCRG that achieves sub-nW operation and a 37.5× improved line regulation is then described [55].

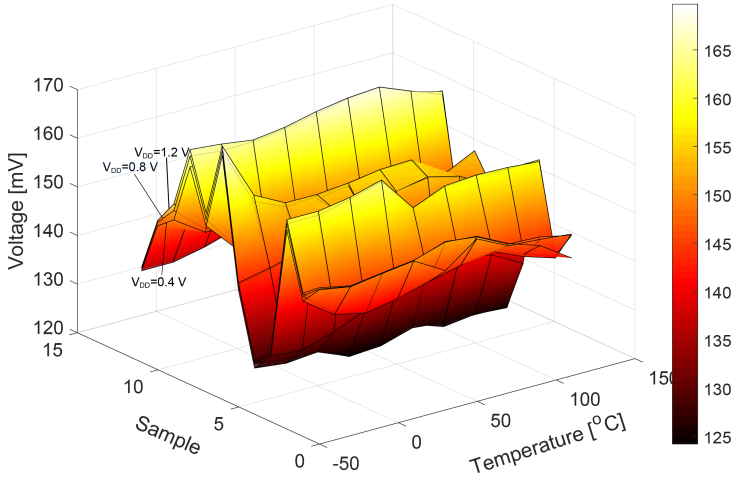


**Figure 3.7**: Measured reference voltage $V_{CWT}$ across a temperature range from -40 to 120$^o$C of 13 samples at 0.4, 0.8, and 1.2 V.

### 3.2.1 State-of-the-Art Sub-nW Oscillator

Prior work in low-power oscillators have utilized gate-leakage as current sources [30], program-and-hold structures [56], multistage structures with boosted capacitance charging [31], comparator-less structures based on program-and-hold topologies [33], and reference-free structures based on capacitive-discharging [41]; many of these have demonstrated sub-nW fully-integrated solutions for Hz-range oscillation. However, these structures suffer from severe line dependence due to the lack of line-regulated references. For example, the best reported line regulation of state-of-the-art is 60%/V and is able to operate across only a small supply range from 0.55 to 0.65 V [56].

### 3.2.2 VCRG-Based Area-Efficient Line-Stable Oscillator

The proposed relaxation oscillator architecture is shown in Fig. 3.5(a). Here, $I_{CWT}$ from the VCRG charges $C_1$ during $\phi_1$, generating a ramp voltage $V_{ramp}(t) = I_{CWT}t/C_1$ at the positive input of the comparator. At the same time, $V_{CWT}$ from the VCRG is applied to the negative input

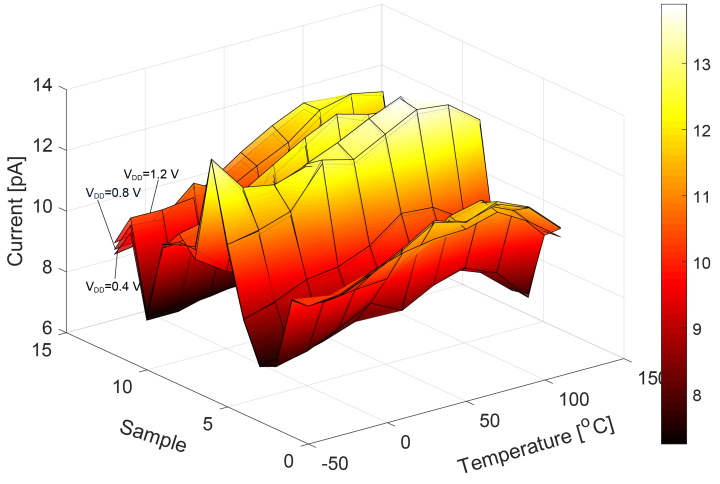


**Figure 3.8**: Measured reference current $I_{CWT}$ across a temperature range from -40 to 120$^o$C of 13 samples at 0.4, 0.8, and 1.2 V.

of the comparator via $S_4$. When $V_{ramp}(t)$ reaches $V_{CWT}$, the output of the two-stage continuous time amplifier flips, and the oscillator enters the second phase ($\phi_2$) where the opposite occurs. The frequency of oscillation is given by:

$$T_{osc} = \frac{V_{CWT}C_1}{I_{CWT}} + \frac{V_{CWT}C_2}{I_{CWT}} + t_{delay}, \tag{3.13}$$

where $t_{delay}$ is the delay from the comparator, Schmitt trigger, and inverters. To achieve 50% duty cycle, $C_1 = C_2 = C_{charge}$ and the oscillation period can be calculated by:

$$T_{osc} = \frac{2V_{CWT}C_{charge}}{I_{CWT}} + t_{delay}. \tag{3.14}$$

**Ultra-Low-Leakage Switches**

Since the absolute current flowing through the circuit is in the pA-range, the leakage of the switches can significantly impact the oscillation frequency. To minimize this effect, ultra-low-leakage switches are employed [41]. As shown in Fig. 3.5(b), when the ultra-low-leakage switch

is in the on state ($\phi$ is high), the transistors $M_1$ and $M_2$ are on and terminals $T_2$ and $T_{LO\_Leak}$ are electronically connected while the transistor $M_3$ is off. When $\phi$ is low, $M_1$ and $M_2$ are in the off state and $M_3$ is off, which is employed to bias the source of $M_1$ at a voltage of a replica of the drain voltage of $M_1$. As a result, the source, drain, and bulk terminals are biased at the same voltage, thus minimizing the leakage in the off state down to $< 5$ fA which is less than 0.05% of the signal current (10 pA) flowing from $T_2$ and $T_{LO\_Leak}$ at room temperature and less than 200 fA ($< 2\%$ of the signal current) across the temperature range from -40 to 120 $^o$C, and therefore the influence on oscillation frequency.

**Comparator Design**

Comparator offset can significantly impact the frequency characteristics if not carefully addressed [41]. In phase $\phi_1$, as shown in Fig. 3.6(a) where the comparator shows an input offset voltage of $V_{OS}$, the ramp voltage $V_{ramp}(t)$ is applied at the positive input of the comparator and the negative input of the comparator is set at $V_{CWT}$. For simplicity, the delay is not shown here. Therefore, the time that the oscillator takes to enter phase $\phi_2$, $t_{\phi 1}$, can be calculated by:

$$V_P = V_N + V_{OS}. \tag{3.15}$$

Thus, $t_{\phi 1}$ is given by:

$$t_{\phi 1} = \frac{C_{charge}}{I_{CWT}}(V_{CWT} - V_{OS}). \tag{3.16}$$

In phase $\phi_2$, $V_{ramp}(t)$ and $V_{CWT}$ are applied to the negative and positive inputs of the comparator, respectively (Fig. 3.6(b)). As $V_{ramp}(t)$ rises and eventually (3.15) holds, the time $t_{\phi 2}$ that is required for the oscillator to flip back into phase $\phi_1$ can be calculated by:

$$t_{\phi 2} = \frac{C_{charge}}{I_{CWT}}(V_{CWT} + V_{OS}). \tag{3.17}$$

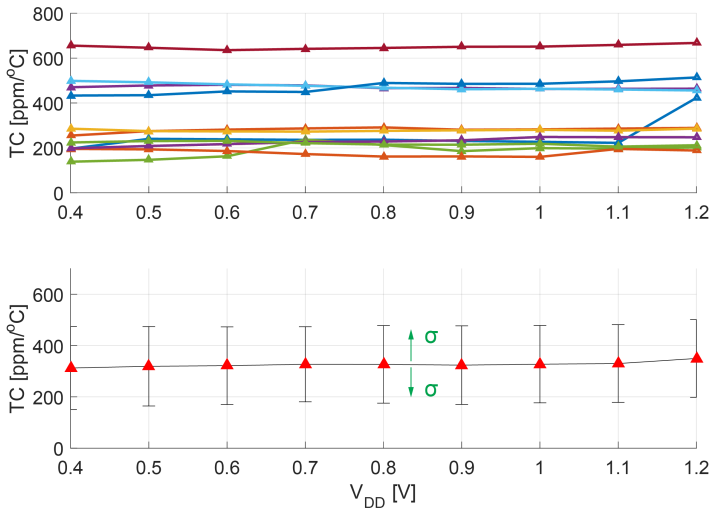


**Figure 3.9**: Measured TC (top) and average TC (bottom) of $V_{CWT}$ when operating at different supply voltages from 0.4 to 1.2 V.

Fig. 3.6(c) shows the transient waveforms observed at the inputs of the comparator during consecutive oscillation phases. The oscillation period when considering the comparator offset, $T_{osc,os}$, is achieved by summing $t_{\phi 1}$ and $t_{\phi 2}$ and $T_{osc,os} = 2V_{CWT}C_{charge}/I_{CWT}$. Therefore, the comparator offset is, to a first order, chopped away by alternating the ramp voltage sequentially between $C_1$ and $C_2$ between phases $\phi_1$ and $\phi_2$ in the proposed relaxation oscillator [25, 34].

The comparator is designed with a 2-stage amplifier achieving a unity gain bandwidth (UGB) of 4.8 kHz and a delay of 1.25 ms which is $<$1.2% of the oscillation period, and therefore the impact of the comparator delay is negligible. To minimize the frequency variation due to the comparator offset [41], careful layout design was performed achieving a comparator offset less than 1.2 mV across the operating temperature range.

## 3.3 Measurement Results of the VCRG

The proposed VCRG was fabricated in a 65 nm CMOS process, occupying 65$\times$75 $\mu$m$^2$ of core area, over 7$\times$ reduction in area compared to prior sub-nA VCRGs.

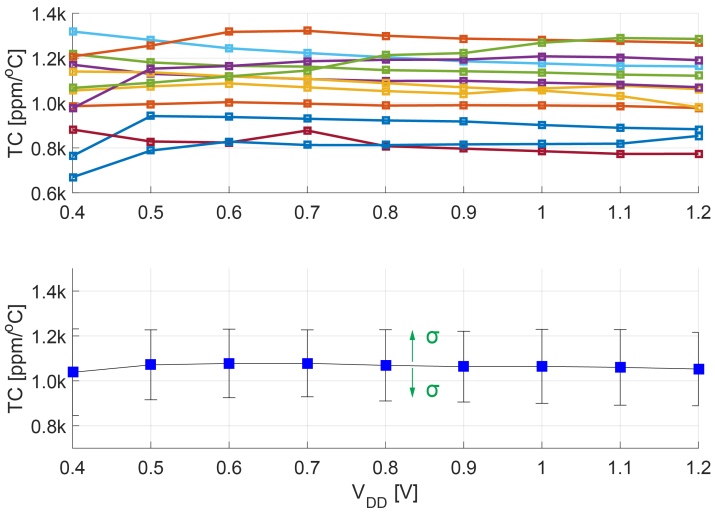


**Figure 3.10**: Measured TC (top) and average TC (bottom) of $I_{CWT}$ when operating at different supply voltages from 0.4 to 1.2 V.

### Temperature Coefficient

The output reference voltage $V_{CWT}$ and reference current $I_{CWT}$ were measured for 13 samples. Measurement results of $V_{CWT}$ and $I_{CWT}$ for all samples across the temperature range from -40 to 120 $^{o}$C at 0.4, 0.8, and 1.2 V are shown in Fig. 3.7 and 3.8, respectively. Across 13 samples, $V_{CWT}$ was measured to be on average 147.0 mV (min/max = 124.3/164.6 mV) when operating from 0.4 V at 20 $^{o}$C, with a standard deviation σ = 10.9 mV (σ/avg = 7.4%). The measured average reference current $I_{CWT}$ across 13 samples was 10.3 pA (min/max = 7.8/12.9 pA) when operating from 0.4 V at 20 $^{o}$C with σ = 1.5 pA (σ/avg = 14.5%). Across -40 to 120 $^{o}$C, the average TCs of $V_{CWT}$ and $I_{CWT}$ when operating at 0.4 V were measured to be 312.4 and 1037 ppm/$^{o}$C and better than 350 and 1070 ppm/$^{o}$C when operating at a supply voltage from 0.4 to 1.2 V, as shown in Fig. 3.9 and 3.10, respectively.

### Line Regulation

The measured reference voltage, $V_{CWT}$, and reference current, $I_{CWT}$, when operating from 0.4 to 1.2 V for 13 samples are shown in Fig. 3.11 and 3.12. As shown in Fig. 3.11 and

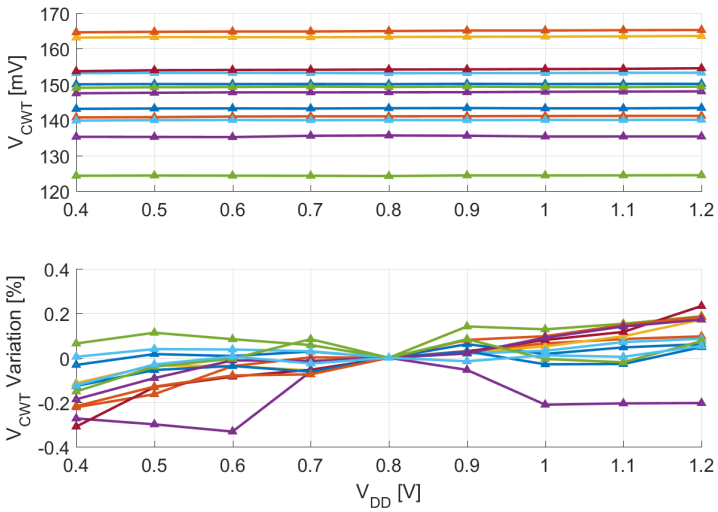


**Figure 3.11**: Measured reference voltage $V_{CWT}$ when operating from 0.4 to 1.2 V at 20$^o$C of 13 samples (top) and variation normalized to 0.8 V (bottom).

3.12, the average measured line regulation of $V_{CWT}$ and $I_{CWT}$ at 20 $^o$C were 0.3%/V and 2.4%/V, respectively.

### Load Regulation

The reference current, $I_{CWT}$, when operating with a load voltage ($V_{Load}$ in Fig. 3.3) from 0 to 0.25 V for 13 samples at 20 $^o$C is shown in Fig. 3.13. The average measured load regulation was 3.4%/V.

### Power Consumption

The VCRG consumed an average power of 30.6 pW at 20 $^o$C measured from 13 samples when operating from a supply voltage of 0.4 V, the lowest reported supply voltage for a CRG. As shown in Fig. 3.14, the VCRG was measured to consume a power less than 200 pW across the temperature range from -40 to 120 $^o$C.

Fig. 3.15 shows the previously reported CRGs in terms of TC, lowest output reference current, and lowest supply voltage, and Table.3.1 summarizes the performance of the proposed

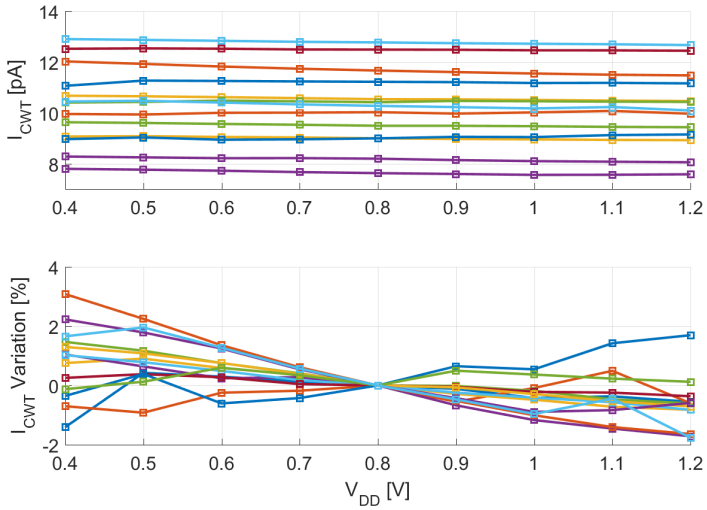


**Figure 3.12**: Measured reference current $I_{CWT}$ when operating from 0.4 to 1.2 V at 20$^o$C of 13 samples (top) and variation normalized to 0.8 V (bottom).

VCRG and compares to state-of-art. The proposed VCRG reduces area by over 7$\times$ for pA-level current generation and reduces supply by over 2$\times$, for the first time enabling sub-1 V pA-level reference current generation in an ultra-low-power and compact fully-integrated design. Fig. 3.22 shows the die photo.

## 3.4 Measurement Results of the VCRG-Based Oscillator

The proposed-VCRG based oscillator was fabricated in 65 nm CMOS, occupying a core area of 9100 $\mu$m$^2$ (including the VCRG). On-chip MIM capacitors $C_{1,2}$ were sized to be 2 pF each. Fourteen die from a single lot were tested, and no calibration was performed on any die.

### VCRG based Oscillator

Figure 3.17 shows the measured oscillation frequency over temperature for 14 samples. The proposed oscillator achieved an average oscillation frequency of 9.3 Hz (min/max = 6.2/12.8 Hz) when operating at 0.6 V at 20 $^o$C. As shown in Fig. 3.18, the oscillator achieved an average

**Table 3.1**: Performance Summary and Comparison with Prior Current Reference Generator

| | TCAS-II'05 | JSSC'08 | ESSCI-RC'10 | JSSC'12 | ESSCI-RC'14 | This Work avg (sigma) | This Work X‡ |
|---|---|---|---|---|---|---|---|
| **Process [nm]** | 1500 | 500 | 350 | 180 | 180 | 65 | |
| **Min. Supply [V]** | 1.1 | 2.3 | 1.3 | 1£/1.2† | 1.2 | 0.4 | |
| $I_{REF}$ | 410 pA | 16 - 50 $\mu$A | 9.95 nA | 7.81 $\mu$A | 20 pA | 10.3 (1.5 pA) | 8.9 pA |
| **Power** | 2 nW | 31 $\mu$W | 88.5 nW | 32.7 $\mu$W† | 23 pW | 30.6 (5.8 pW) | 27.3 pW |
| **Temp. Range [$^o$C]** | -20 to 70 | 0 to 80 | -20 to 80 | 0 to 100 | 0 to 80 | -40 to 120 | |
| **TC [ppm/$^o$C]** | 2500 | 130 | 1190 | 24.9£ | 780 | 1037 (193.1) | 669 |
| **Line Reg. [%/V]** | 6 | N/A | 0.046 | 0.13† | 0.58 | 2.4 (1.2) | 2.5 |
| **Load Reg. [%/V]** | N/A | 1 | N/A | N/A | 0.25 | 3.4 (3.2) | 2.3 |
| **Chip Area [$\mu$m$^2$]** | 46k | 15k | 120k | 123k† | 38.2k* | 4.9k | |
| **# of Samples** | 10 | 5 | 15 | 10 | 1 | 13 | |
| **Trimming** | No | Multi-temp. | Multi-temp. | No | No | No | |

†With Bandgap reference; £Core only; *48.4k with current level selector; ‡Sample with best TC.

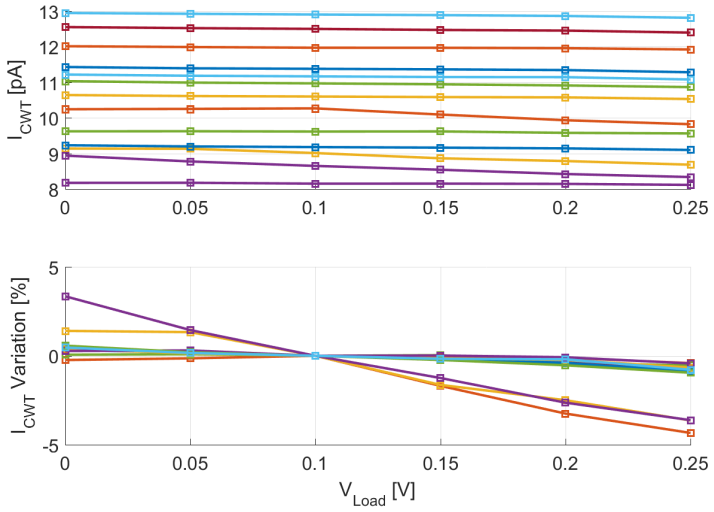


**Figure 3.13**: Measured $I_{CWT}$ when load voltage varied from 0 to 0.25 V at 20$^o$C of 13 samples (top) and variation normalized to 0.1 V (bottom).

temperature coefficient of 999.9 ppm/$^o$C (min/max = 217.6/1685.6 ppm/$^o$C) when operating at 0.6 V, all without any calibration or trimming. When operating between 0.6 to 1.1 V, the oscillator achieved an average line regulation of 1.6%/V (min/max = 0.6/3.8%/V), which improves state-of-the-art, shown in Table 3.2, by at least 37.5×, noting that the prior best metric in [56] only operated over a 100 mV supply range, and only measured a single die. The die with the best sensitivity in this work was measured to achieve a 50× higher supply stability than [56]. The proposed oscillator achieved an Allan deviation floor $<$ 220 ppm, which also exceeds state-of-the-art Hz-range oscillators, thereby indicating its long-term stability. Over 14 samples, the average power consumption of the overall system was measured to be 124.2 pW (min/max = 34/281.6 pW) at 20 $^o$C and 0.6 V.

## 3.5 Summary

A near-zero-power CWT VCRG operating at a supply voltage as low as 0.4 V, the first sub-1 V CRG, has been proposed in this chapter. By employing gate-leakage array as current core,

**Table 3.2**: Comparison with Previously Published State-of-the-Art sub-nW Oscillators.

| | CICC'07 | ISSCC'09 | ISSCC'11 | VLSI'15 | JSSC'16 avg ($\sigma$)$^{\dagger}$ | **This Work avg ($\sigma$)$^{\dagger}$** | **X$^{*}$** |
|---|---|---|---|---|---|---|---|
| **Process [nm]** | 130 | 130 | 130 | 180 | 65 | **65** | |
| **Oscillator Principle** | Gate-Leakage | Program and Hold | Gate-Leakage | Program and Hold | Capacitive Discharging | **Relaxation** | |
| **Supply Voltage [V]** | 0.45 | 0.6 | 0.7 (1.2) | 0.6 | 0.5 | **0.6** | |
| **Frequency [Hz]** | 0.09 | 11.11 | $\sim 5$ | 18 | 2.8 | **9.3 (1.6)** | **12.8** |
| **Freq. Spread [$\sigma$/avg]** | 28% | N/A | N/A | N/A | 11.8% | **17.2%** | |
| **Power [pW]** | 120 | 150c | 660 | 4.2 | 44.4 (6.4) | **124.2 (66.1)** | **114.2** |
| **Power Eff. [pJ/Cycle]** | 1333 | 13.5 | 132 | 0.23 | 15.8 | **13.3** | **8.9** |
| **Line Reg. [%/V]** | 150 | 60 | N/A | N/A | 160 | **1.6 (0.9)** | **1.19** |
| **Voltage Range [V]** | 0.4 - 0.5 | 0.55 - 0.65 | N/A | N/A | 0.48 - 0.52 | **0.6 - 1.1** | |
| **Temp. Coeff. [ppm/$^{o}$C]** | 1,600 | 490 | 31 | 20,000 | 1,260 (280) | **999.9 (392)** | **217.6** |
| **Temp. Range [$^{o}$C]** | 0 to 80 | 0 to 90 | -20 to 60 | -30 to 60 | -40 to 60 | **-40 to 120** | |
| **Area [$\mu$m$^2$]** | 480 | 19,000 | 15,300 | N/A | 25,500 | **9,100** | |
| **Off-Line Calib. Cost** | N/A | N/A | Multiple-Point | N/A | No | **No** | |
| **Allan Dev. Floor [ppm]** | N/A | N/A | N/A | N/A | $<$500 | $<$**220** | |
| **Chips Measured** | 25$^{\pounds}$ | 1 | 1 | 1 | 5 | **14** | |

$^{\dagger}$Parameters measured with multiple samples.

$^{\pounds}$For frequency measurement.

$^{*}$The sample with best temperature dependence.

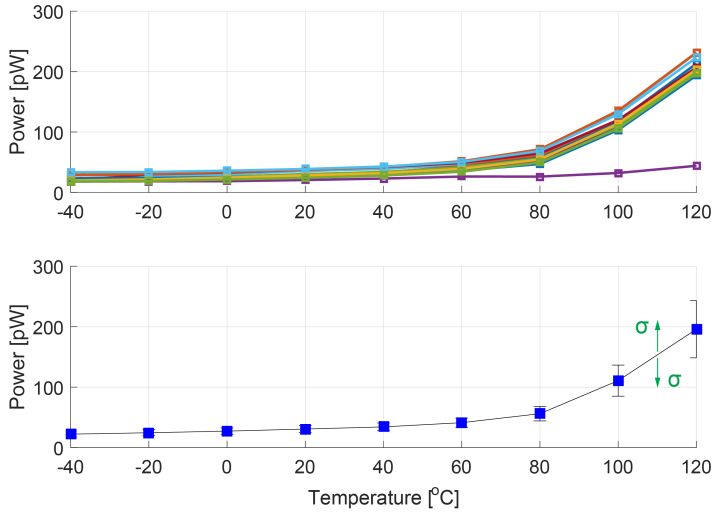


**Figure 3.14**: Measured power consumption (top) and average power consumption (bottom) of the proposed VCRG across -40 to 120$^o$C of 13 samples at 0.4 V.

the proposed VCRG enables a over 7$\times$ reduction in area. Measurement results of thirteen 65 nm prototypes revealed that the reference current $I_{CWT}$ achieved an average temperature coefficient of 1037 ppm/$^o$C and consumed 30.6 pW at 20 $^o$C.

The text of Chapter 3, in part, is a reprint of the material as it appears in "A 1.6%/V 124.2pW 9.3Hz Relaxation Oscillator Featuring a 49.7pW Voltage and Current Reference Generator" by Hui Wang and Patrick Mercier, in Proc. IEEE European Solid-State Circuits Conference (ESSCIRC), Sep. 2017. The dissertation author was the primary investigator and author of this paper.

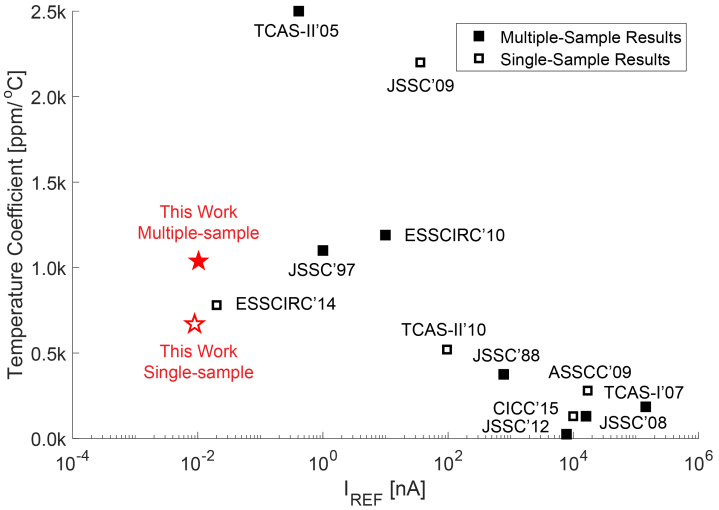


**Figure 3.15**: Temperature coefficient of reported current reference generators over reference current.

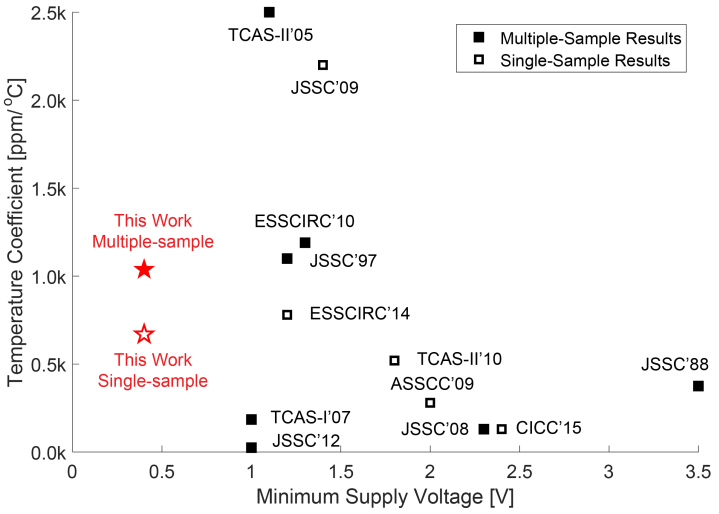


**Figure 3.16**: Temperature coefficient of reported current reference generators over minimum supply voltage.

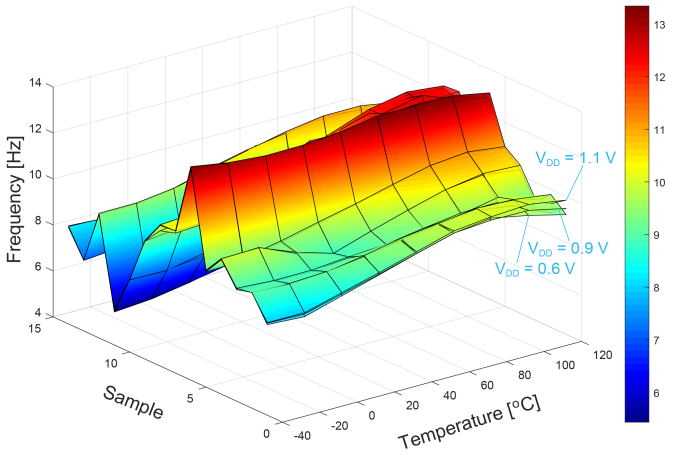


**Figure 3.17**: Measured oscillation frequency over the temperature range from -40 to 120 $^{o}$C at 0.6, 0.8, and 1.1 V for 14 samples.

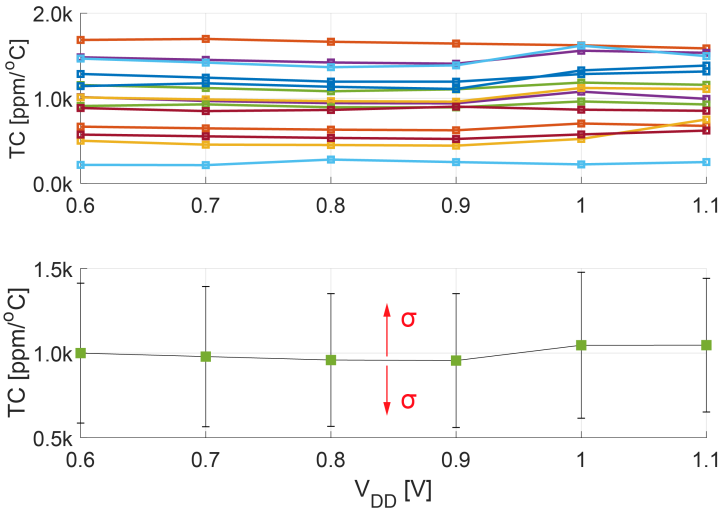


**Figure 3.18**: Measured temperature coefficient (top) and average temperature coefficient (bottom) of the oscillation frequency at different supplies from 0.6 to 1.1 V for 14 samples.

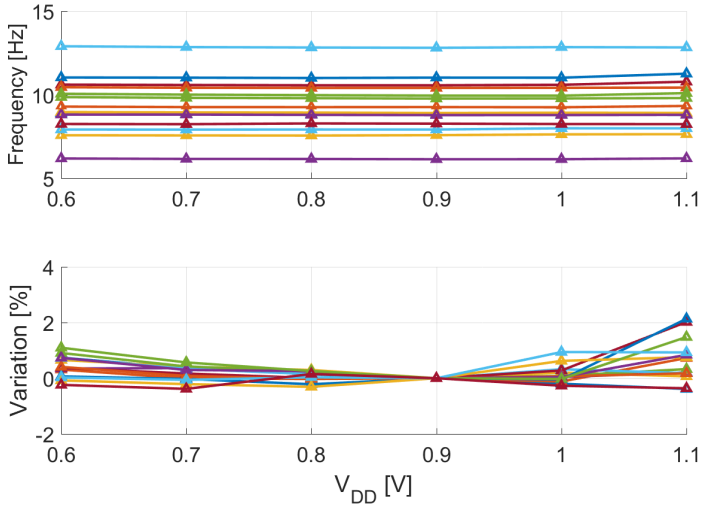


**Figure 3.19**: Measured oscillation frequency when operating from 0.6 to 1.1 V at 20 $^{o}$C of 14 samples (top) and variation normalized to 0.9 V (bottom).

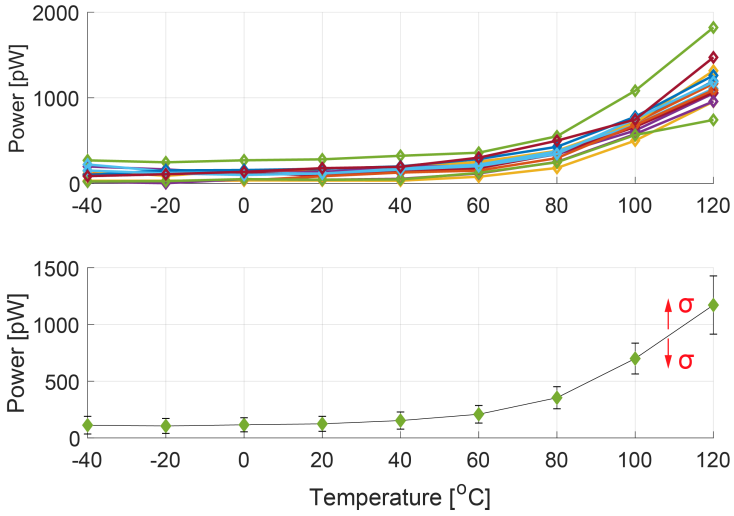


**Figure 3.20**: Measured power consumption (top) and average power consumption (bottom) of the proposed VCRG-based oscillator when operating from -40 to 120 $^{o}$C at 0.6 V of 14 samples.

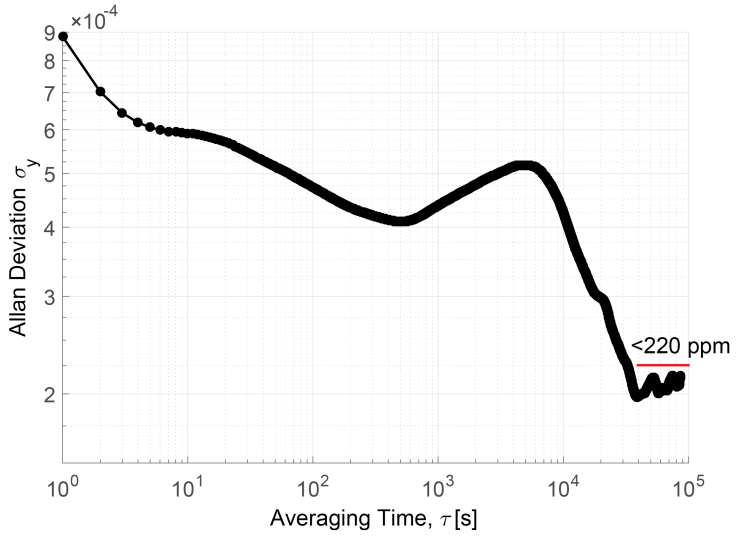


**Figure 3.21**: Measured Allan deviation of the proposed oscillator for over 2 M periods, showing a floor $< 220$ ppm.

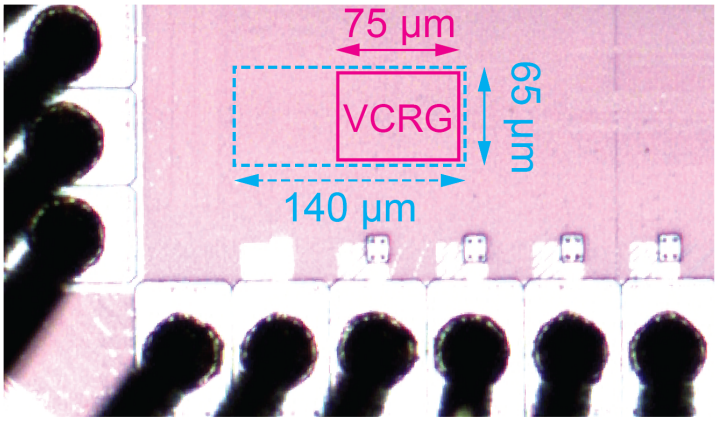


**Figure 3.22**: Micrograph of the proposed VCRG (dashed-line box) and VCRG-based oscillator (solid-line box).

# Chapter 4

# A 113 pW Fully Integrated CMOS Temperature Sensor Operating at 0.5 V

Temperature is an important parameter to measure in a variety of applications such as environmental monitoring, wearable biomedical devices, smart homes, and industrial internet-of-things equipment. Since devices employed in such applications often need to be ultra-small and/or unobtrusive, there is often little room for a battery or energy harvesting source. Thus, the overall power available for such systems is limited, in some cases to below 1 nW [7], in order to support long system lifetime in a wide variety of applications [57–60]. To reduce the power of temperature sensing, prior-art has suggested carefully measuring the temperature characteristics of bipolar junction transistors (BJT) integrated on silicon microchips. In such cases, temperature is transduced by comparing the proportional to absolute temperature (PTAT) characteristic of the difference between two base-emitter voltages of a vertical NPN BJT (VBE) with the complementary to absolute temperature (CTAT) characteristic of the base-emitter voltage (VBE), or with a co-integrated constant with temperature (CWT) voltage reference [61–63]. However, biasing BJTs in the forward-active region with sufficiently low noise properties usually demands currents in the nA-A range that, coupled with supply voltages on the order of a few volts and

the power overhead of biasing, control, and analog-to-digital conversion circuits, still exceeds the power demands of ultra-small sensing nodes. To further reduce power consumption, other prior-art has suggested exploiting the temperature-dependency of electron/hole mobility, threshold voltage, and drain currents of MOSFETs [61]. Since most modern electronic devices used for amplification, analog-to-digital conversion, digital processing, and wireless telemetry utilize complementary metal-oxide-semiconductor (CMOS) technology, low-cost homogenous integration of temperature sensing and all other device functionality is possible. Since MOSFETs have several different temperature dependencies, there are many possible ways to create PTAT, CTAT, or CWT references. For example, by connecting the gate, bulk and drain of a p-channel MOSFET together, the characteristic of the drain current with respect to the gate voltage approximates a pn-junction and thus can be employed to detect temperature in a similar way to conventional BJT-based transducers [63]. The temperature-encoded analog signals (currents or voltages) can then be digitized by voltage-, current-, frequency-, or time-to-digital conversion [64–66]. However, all prior-art MOSFET-based techniques still require at least tens of nW of power [32, 67], and often require external CWT frequency sources for digitization that are not included in the quoted power number. There are thus no current temperature sensing techniques that achieve the sub-nW power consumption necessary to enable next-generation near-zero-power sensing nodes.

Here we present a new temperature sensing technique that relies on complementary temperature dependencies of n- and p-type MOSFETs biased in the subthreshold region, together with CWT tunneling currents and a capacitive charging-time-to-digital feedback architecture that digitizes temperature at 113 pW in a fully monolithically-integrated manner, which represents a 628 reduction in power over prior-art [67]. Specifically, a 2-transitor (2T) subthreshold PTAT voltage reference generator16 (VRG) was implemented to serve as the temperature sensing element, while another temperature-stabilized 2T subthreshold VRG18 was employed as a CWT reference, replacing conventionally power-hungry band-gap VRGs. The PTAT and CWT analog voltages were then converted to pA-level currents via self-biased current generators based on

**Table 4.1**: Comparison of Different Temperature Sensing Methods in terms of power budget, accuracy, and minimum required supply.

| | Power | Accuracy | Minimum Supply |
|---|---|---|---|
| **Thermistor/RTD** | Medium | Low | Medium |
| **BJT** | High | High | High |
| **MOSFET** | Low | Medium | Low |

tunneling effects. Temperature was then digitized by charging digitally-controllable monolithic MIM capacitors with the pA-level currents and matching the charging time between the PTAT and CWT paths via feedback-driven tuning of the MIM capacitors for direct ultra-low-power digital readout.

## 4.1 Temperature Sensor Architectures

Temperature sensors are typically constructed by first transducing temperature into a parameter measurable by an electronic circuit (e.g., voltage, current, resistance, or time), processed by an analog conditioner, and then digitized. In on-chip scenarios, temperature is commonly measured by observing the temperature-dependent characteristic of devices such as a thermistor (resistor), BJT, or MOSFET, followed by amplification, then digitization via a precision analog-to-digital converter (ADC), usually a successive approximation register (SAR)- or sigma-delta ($\Sigma\Delta$)-ADC, a time-to-digital converter (TDC), or a frequency-to-digital converter (FDC). A digital controller and a reference generator circuit is often required to coordinate the operation of the overall temperature sensor system and generate necessary references such as voltage/current references and/or time/frequency references.

#### Thermistor/RTD-Based Temperature Sensor

Thermistors or resistance temperature detectors (RTDs) are implemented with ceramic, polymer, metal, or doped semiconductor (e.g., well-, diffusion- and poly-resistors in CMOS) that exhibit temperature-dependent resistance that can be measured, for example, by passing a known

current through the resistor and measuring the voltage. While conceptually simple, it is generally difficult to build precise, yet ultra-low-power temperature sensors using thermistors, as the precise resistance of on-chip resistors are non-linear and have a rather large spread (e.g., 20-30%), which thus requires multi-point calibrations and precision (and power-expensive) analog compensation circuits.

**BJT-Based Temperature Sensor**

In BJT-based temperature sensors, temperature is measured by comparing the proportional to absolute temperature (PTAT) characteristic of the difference between two base-emitter voltages of a BJT, $\Delta V_{BE}$, with the complementary to absolute temperature (CTAT) characteristic of the base-emitter voltage, $V_{BE}$, or, with a constant with temperature (CWT) voltage reference. The accuracy of BJT-based temperature sensors relies on the precision readout circuitry combined with thermal calibration. Therefore, $\Sigma\Delta$-ADC has been widely used in such sensors, at the penalties of increased power overhead (can consume up to 80% of the overall power). On the other hand, the simplicity of circuitry and power efficiency make SAR-ADC an attractive alternative, however, at the price of reduced accuracy.

Such temperature sensors often have high power consumption ($\sim\mu$W), since: 1) large currents (in the nA-$\mu$A range) are required to achieve low noise when operating in the forward-active region; and 2) a supply voltage above 1 V is often needed due to the high $V_{BE}$ ($\sim$0.6 V at room temperature).

**MOSFET-Based Temperature Sensor**

Since most modern electronic devices, including amplification, digital processing, and wireless telemetry, are implemented in CMOS technology, MOSFET-based temperature sensors are becoming popular because it enables low-cost homogeneous integration of temperature sensing with all other functionality.

There are several temperature-dependent characteristic of MOSFETs that can be exploited to generate temperature-dependent parameters. For example, the characteristic of the drain current with respect to the gate voltage of dynamic threshold metal-oxide-semiconductor transistors (DTMOSTs) implemented by connecting the gate, bulk, and drain of the p-channel MOSFET together, approximates a pn-junction and thus can be employed to transduce temperature in a similar way to BJT-based temperature sensors. In addition, the supply voltage can be significantly reduced, to below 1 V, since lower $V_{gs}$ ($\sim$0.3 V at room temperature) is utilized to encode temperature instead of $V_{BE}$ in BJT-based sensors. In such sensors, the temperature-encoded analog signals are usually digitized power efficiently by voltage-, current-, time-, or frequency-to-digital converters, enabling low-power temperature sensing.

The trade-offs between power consumption, accuracy, and minimum supply voltage of the three described temperature sensor architectures is summarized in Table. 4.1.

## 4.2 Near-Zero-Power Fully Integrated Temperature Sensor

MOSFET-based architecture enables sub-1 V operation and significant reduction in power consumption. However, all prior-art still require at least tens of nW of power [32], and often require external CWT voltage/current or frequency sources that add power overhead and cost, and thus are not compatible with near-zero-power sensing systems. Here, we present a temperature sensing architecture that exploits the gate tunneling current prevalent in advanced CMOS technology alongside a capacitive charging-time-to-digital feedback architecture [53]. The presented architecture, when married with careful low-power design techniques and application-driven sampling rate selection, digitizes temperature at 113 pW in a fully monolithically-integrated manner.

In this work, we introduce a CWT voltage reference circuit that utilizes only two conventional n- and p-type MOSFETs (NMOS and PMOS) in a two transistor (2T) push-pull

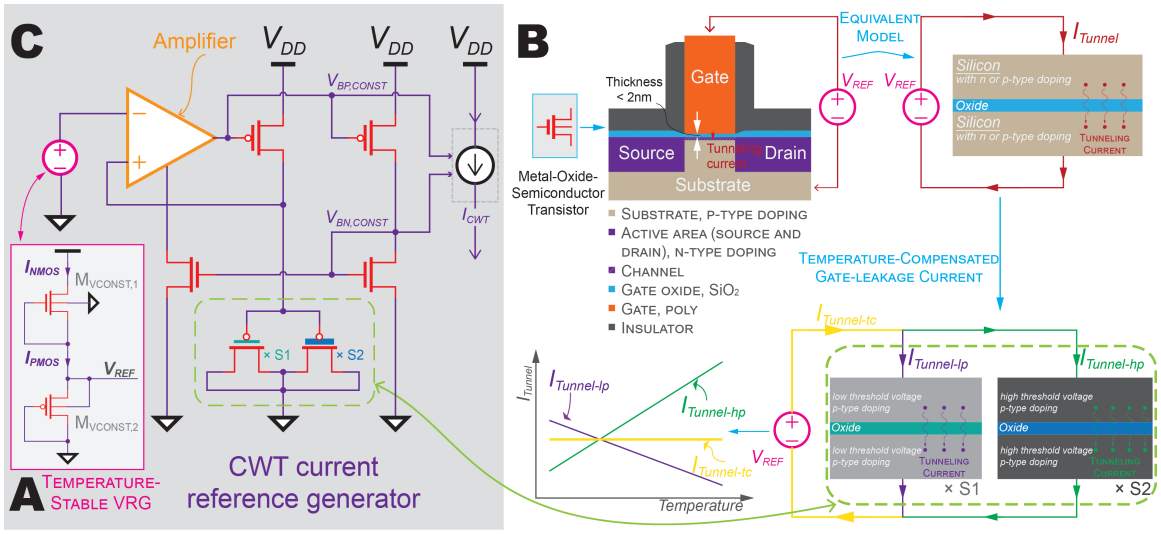


**Figure 4.1**: Temperature-stabilized voltage and current reference generators in 65 nm CMOS technology. (a) Temperature-stabilized 2T pW VRG operating in saturated subthreshold region. (b) Tunneling current in thin-gate CMOS transistors and temperature-compensated gate-leakage current. (c) Monolithic implementation of the pA-level CWT current reference generator.

arrangement18, as shown in Fig. 4.1(a). When biased in the subthreshold or weak-inversion regime (i.e., $|V_{gs}$ ¡ $V_{th}|$ where $V_{gs}$ is the gate to source voltage and $V_{th}$ is the threshold voltage of the transistors), the drain current of each transistor is given by:

$$I_{sub} = \mu C_{ox} \frac{W}{L} (n-1) \phi_T^2 e^{\frac{V_{gs}-V_{th}}{n\phi_T}} (1 - e^{\frac{-V_{ds}}{\phi_T}}), \tag{4.1}$$

where $\mu$ is mobility, $C_{ox}$ is oxide capacitance, W and L are the transistor width and length, respectively, $n$ is subthreshold slope factor, $T$ is thermal voltage, and Vds is the drain to source voltage. In saturated subthreshold region where $V_{ds}$ ¿ $4T$, the drain current of the transistor can be calculated by:

$$I_{sub} = \mu C_{ox} \frac{W}{L} (n-1) \phi_T^2 e^{\frac{V_{gs}-V_{th}}{n\phi_T}}. \tag{4.2}$$

By equating currents between the NMOS and PMOS, the output reference voltage can be computed, and its temperature sensitivity can be, to a first order, zeroed by appropriate sizing. Unlike prior work, which required zero-threshold transistors to make a similar transistor

arrangement work [47], the proposed circuit utilized only conventionally-available MOSFETs and was thus implemented at low cost with no additional mask sets required. Implemented in 65 nm CMOS, the VRG generated $V_{REF}$ = 345 mV with 260.8 ppm/$^o$C measured variation from -20 to 60 $^o$C and power varying from 0.1 pW (-20 $^o$C) to 7 pW (60 $^o$C) over the same temperature range. A similar 2T arrangement, though in this case utilizing two NMOS transistors, was employed to generate a PTAT voltage reference. The 2T PTAT VRG generated a PTAT reference, $V_{REF}$, PTAT, with a temperature coefficient of 0.76 mV/$^o$C over the temperature range from -20 to 60 $^o$C. The measured power varied from 0.1 pW (-20 $^o$C) to 62.9 pW (60 $^o$C) over the same temperature range.

While temperature could be transduced by amplifying the difference between the CWT and PTAT VRGs and digitizing with a voltage-mode ADC, the power overhead of doing so would be large. Instead, we utilized these voltage references to build ultra-low-power current references, whose outputs can be more easily digitized using a novel charging-time-to-digital feedback scheme (described later). Generation of current sources from voltage references typically relies on applying the voltage reference across a CWT resistance via an analog feedback network. However, the pA current levels required here necessitates TΩ resistors given the low VRG voltage levels, which are not conventionally possible to implement on- or off-chip in a small area.

Fortunately, it is possible to generate effectively large resistors in a small on-chip area by exploiting tunneling currents through thin gate oxides available in many modern CMOS processes. For example, the 2 nm $SiO_2$ thickness in 65 nm technology facilitates electron tunneling from the conduction band and valence band, and hole tunneling from the valence band, to the point where such gate conduction becomes non-negligible [34]. This tunneling current is a function of process parameters (gate oxide thickness and effective mass, barrier height, etc., [36]) and direct current (DC) bias condition. Transistors doped differently to support, for example, differing threshold voltages, can have opposite temperature coefficients that can be exploited to design CWT tunneling currents. For example, the tunneling current of low threshold (LVT) and standard

threshold (SVT) PMOS transistors show opposite temperature dependences26. Therefore, the temperature dependence of the gate-leakage current can be minimized by placing appropriately sized LVT and SVT PMOS transistors in parallel with a size ratio of 11:1 and biasing them with a temperature-stabilized reference voltage $V_{REF}$, therefore enabling temperature-stable pA-level current generation (Fig. 4.1(b)).

The monolithically-integrated CWT current reference generator is shown in Fig. 4.1(c), where a self-biased ultra-low-power operational amplifier18 provides the feedback path. The total measured power consumption of the CWT current generator was measured to be 3.2 pW. Using a similar topology, a PTAT current generator was implemented employing a 2T PTAT VRG, and consumed 5.8 pW during operation.

The overall architecture of the proposed monolithically-integrated CMOS temperature sensor is shown in Fig. 4.2. Here, the CWT current reference, $I_{CWT}$, charges capacitor $C_{REF}$, generating a ramp voltage $V_{ramp,CWT}$ (Fig. 4.2(a)), which serves as the Reference Sensing Unit (RSU). The capacitor is purged (reset) once $V_{ramp,CWT}$ reaches $V_{REF}$, a temperature-stabilized voltage reference, thus generating an intrinsic temperature-stabilized oscillator. The period of the intrinsic oscillator is:

$$T_{OSC} = \frac{V_{REF} C_{REF}}{I_{CWT}} + T_{delay}, \tag{4.3}$$

where $T_{delay}$ is the delay of the loop. At the same time, in the Temperature to Current Conversion Unit (TCCU) shown in Fig. 4.2(b), a PTAT current reference, $I_{PTAT,SUB}$, charges a binary-weighted MIM capacitor, $C_{DAC}$, generating another ramp voltage, $V_{ramp,PTAT}$. The temperature-encoded voltages are then conditioned by the Analog Processing Unit (APU) (Fig. 4.2(c)) where an arbiter (Fig. 4.2(d)) was employed to determine which of the two ramp voltages crossed $V_{REF}$ first. The arbiter output is then used as the input of the Digital Processing Unit (DPU) (Fig. 4.2(e)) to determine if $C_{DAC}$ should be incremented or decremented to match the charging time of $V_{ramp,CWT}$ in the RSU, rendering a 10b output code proportional to temperature via discrete time digital feedback control. Fig. 4.2(f) shows an example operation of the DPU.

The current from the PTAT reference is given by $I_{PTAT} = kT + I_o$, where $k$ is the temperature coefficient, $T$ is the absolute temperature, and $I_o$ represents an offset. Therefore, at steady state:

$$\frac{I_{CWT}}{C_{REF}} = \frac{I_{PTAT}}{C_{DAC}} = \frac{kT + I_o}{C_{DAC}}. \tag{4.4}$$

Across the temperature range from $T_{min}$ to $T_{max}$, the minimum and maximum required $C_{DAC}$ can be calculated by (4.5) and (4.6), respectively,

$$C_{min} = (kT_{min} + I_o)\frac{C_{REF}}{I_{CWT}}, \tag{4.5}$$

$$C_{max} = (kT_{max} + I_o)\frac{C_{REF}}{I_{CWT}}. \tag{4.6}$$

The temperature-to-digital conversion resolution $T_{LSB}$, therefore, can be calculated by:

$$T_{LSB} = \frac{T_{max} - T_{min}}{C_{max} - C_{min}} = \frac{1}{k}\frac{I_{CWT}}{C_{REF}}. \tag{4.7}$$

As shown in (4.5) and (4.6), the area of the capacitor $C_{DAC}$ (which can dominate the chip size) is proportional to $I_o$, while (4.7) indicates that the achievable temperature-to-digital conversion resolution is inversely proportional to $k$. Thus, to achieve a large resolution in small area, a current subtractor was employed (Fig. 4.3), whereby $n \times I_{PTAT}$ is subtracted from $m \times I_{CWT}$ to generate $I_{PTAT,SUB}$, effectively multiplying the temperature coefficient (and therefore resolution) by $n$ ($n$ = 3 in this implementation and is trimmable), while reducing the required capacitor $C_{DAC}$ area by a factor of $n - m \times I_{CWT}/I_o$ (2.2 in this implementation).

## 4.3 Measurement Results

The presented temperature sensor was fabricated in a standard 65 nm CMOS and occupied 0.15 mm$^2$. Four samples of the temperature sensor were tested and the output codes were

**Table 4.2**: Performance Summary of the Proposed Temperature Sensor and Comparison with Prior sub-$\mu$W Fully Integrated Sensors

| | [32] | [67]† | [53] This Work |
|---|---|---|---|
| **Technology** | 0.18 $\mu$m | 0.18 $\mu$m | 65 nm |
| **Area [mm$^2$]** | 0.09 | 0.22 | 0.15 |
| **Supply Voltage [V]** | 1.2 | 1.2 | 0.5 |
| **Temperature Range [$^o$C]** | 0 to 100 | -20 to 80 | -20 to 40 |
| **Resolution** | 0.3 $^o$C* | 0.09 $^o$C* | 0.21 $^o$C |
| **Sampling Rate [S/s]** | 33 | 125 | 0.208 |
| **Inaccuracy [$^o$C]** | +1.5/-1.4 | +0.76/-0.76 | $\pm$1.93 |
| **Relative Inaccuracy$^{£}$** | 2.9 | 1.52 | 6.4 |
| **Power [nW]** | 71 | 570 | 0.113 |
| **Energy/Conversion [nJ]** | 2.2 | 4.56 | 0.54 |
| **FoM$^{‡}$[nJ·K$^2$]** | 0.19 | 0.0369 | 0.023 |

*Degree RMS value; †System measurement results;
£100·Max error/Temperature range; ‡Energy/Conversion·Resolution$^2$.

measured to be stable across the temperature range from -20 to 40 $^o$C. The intrinsic oscillator alone occupied an area of 0.038 mm$^2$, and oscillated at 0.208 Hz and consumed 11.8 pW at 20$^o$C. The oscillator achieved a temperature coefficient of 772 ppm/$^o$C and line regulation was measured to be 6%/V from 0.4 V to 1.0 V.

At 0.5 V, the temperature sensor output codes were measured to be stable across the temperature range. The accuracy of temperature sensing was measured by ramping ambient air temperature at a rate of 0.2$^o$C/minute from -20 to 40$^o$C, and comparing the digital sensor output to the readings of a proximal platinum resistance thermometer. As shown in Fig. 4.4(a), the temperature sensors achieved a worst-case inaccuracy of $\pm$1.93 $^o$C after a second order polynomial fit to their average characteristic. Measured from 1500 consecutive conversions, the temperature sensing resolution was 0.21 $^o$C at 20 $^o$C. At 0.5 V, as shown in Fig. 4.4(b), the four temperature sensor samples consumed 113 pW at 20 $^o$C without any external components required, which improves the state-of-the-art by 628$\times$. The power of the DPU, which consists of control logic, counters, etc., dominates the system-level power consumption (80% of the overall power), as indicated by the power breakdown in Fig. 4.4(c). The temperature sensor

required 4.8 s of conversion time, resulting in 540 pJ/conversion, which is $> 4\times$ lower than prior fully-integrated temperature sensors. The temperature sensor was packaged in a 48-pin Quad-Flat No-leads (QFN-48) package and a die photograph of the fully integrated near-zero-power temperature sensor is shown in Fig. 4.4(d). Table. 4.2 summarizes the performance and Fig. 4.5 compares the proposed near-zero-power temperature sensor to prior-art in terms of power versus worst-case inaccuracy.

## 4.4 Summary

The sensor described in this work enables transduction and digitization of temperature at $628\times$ lower power than prior-art without a significant reduction in sensing accuracy. By combining the generation of CWT and PTAT voltages via subthreshold-biased 2T circuits with tunneling-current-based CWT resistances to generate CWT and PTAT currents, and using these currents in a feedback circuit that normalizes charging time via a digitally-controlled capacitor bank, temperature was directly digitized at ultra-low-power. With a relaxation oscillator intrinsically built into the proposed architecture, no external references, biases, clocks, or any other components are required for temperature-to-digital transduction. The proposed sensor enables a new class of devices that can monitor their environments with nearly zero power, enabling ultra-long battery life, or energy harvesting from low-power sources towards energy-autonomous operation. While measurements across the four chips presented in this chapter gives an idea of the accuracy of the proposed temperature sensor in the presence of process variation, more die-to-die, wafer-to-wafer, and lot-to-lot measurements would be needed in future work to validate accuracy for volume manufacturing.

The text of Chapter 4, in part, is a reprint of the material as it appears in "A 113 pW Fully Integrated CMOS Temperature Sensor Operating at 0.5 V" by Hui Wang and Patrick Mercier, in Proc. IEEE Sensors Conference, Oct. 2017, and "Near-Zero-Power Temperature Sensing via

Tunneling Currents Through Complementary Metal-Oxide-Semiconductor Transistors" by Hui Wang and Patrick Mercier, Scientific Reports, vol. 7, no. 4427, Jun. 2017. The dissertation author was the primary investigator and author of both papers.

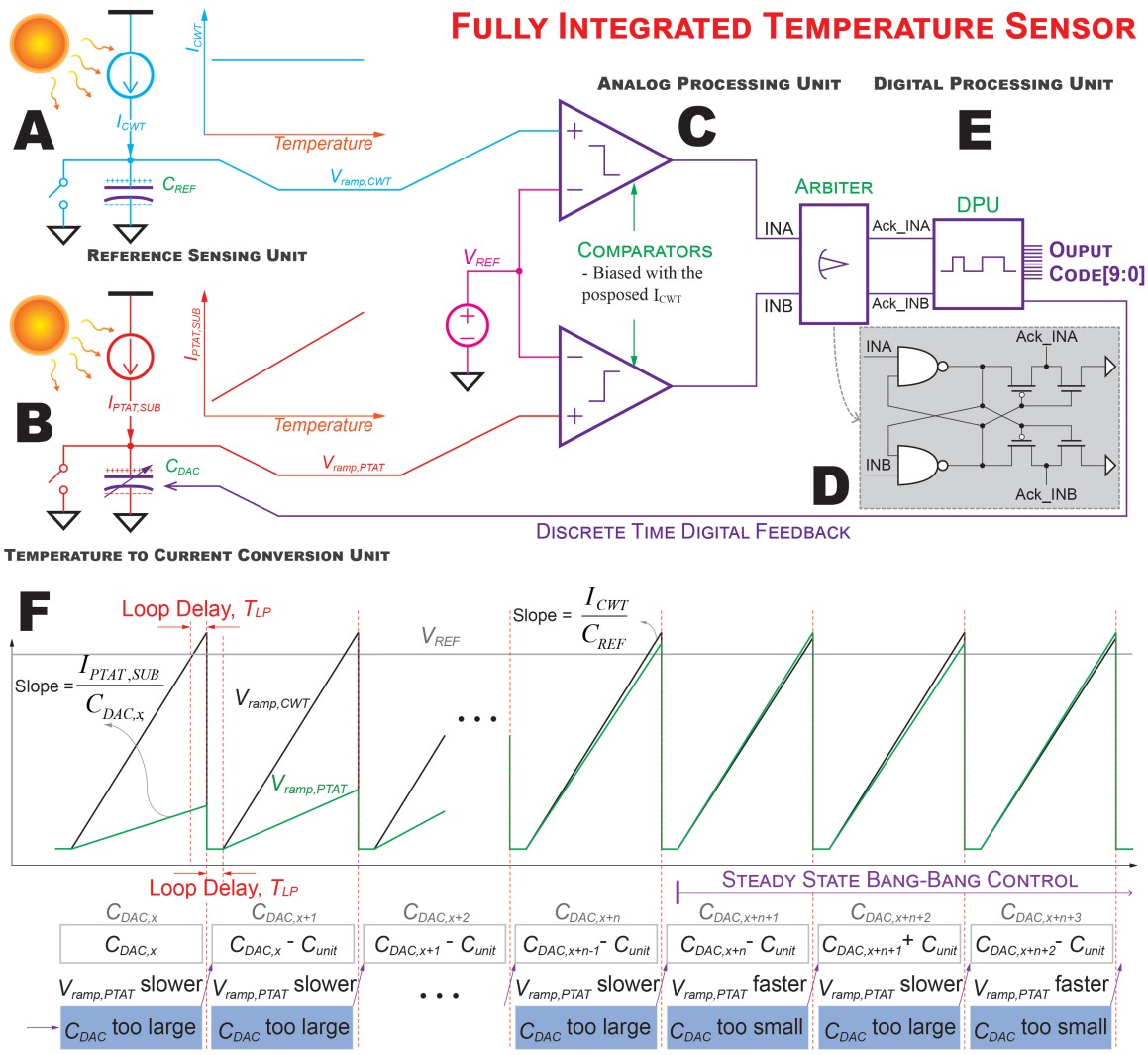


**Figure 4.2**: Architecture of the proposed temperature sensor. (a) A temperature-stable current source was employed to generate a CWT ramp voltage, $V_{ramp}$, CWT, by charging capacitor CREF. (b) A PTAT current source was employed as the temperature sensing core by converting temperature to a corresponding current and generated a PTAT ramp voltage, $V_{ramp}$, PTAT, by charging a digitally-controllable bank of capacitors CDAC. (c) An analog processing unit consisting of a temperature-stabilized VRG, comparators, and an arbiter was implemented to translate the temperature-encoded analog voltages to digital signals. (d) Schematic of the Arbiter. (e) A digital processing unit processes the information, controls CDAC, and generates the digital codes corresponding to the ambient temperature. (f) An example operation of the DPU illustrates that CDAC was tuned via discrete time digital feedback to match the rising time of $V_{ramp}$, CWT in RSU.

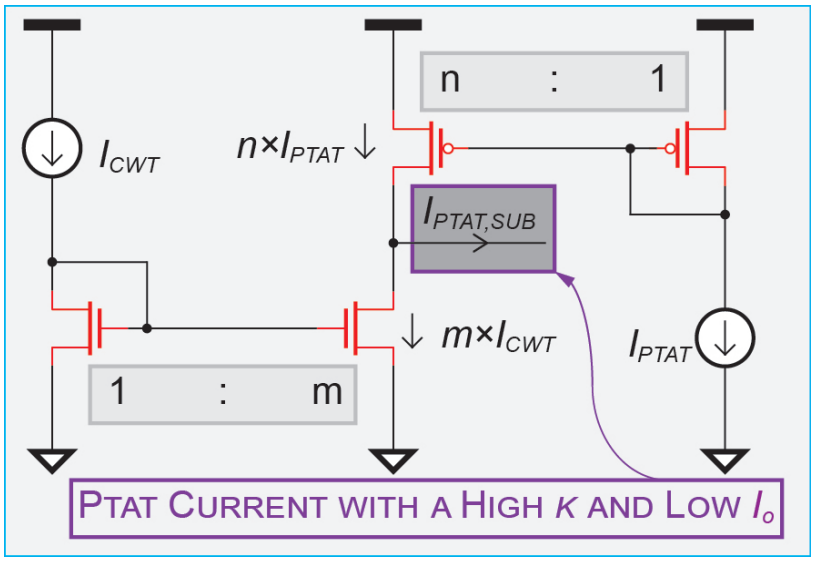


**Figure 4.3**: Implementation of the current subtractor employed to increase temperature conversion resolution by increasing the effective temperature coefficient $k$, where $m = 1$ and $n = 3$.

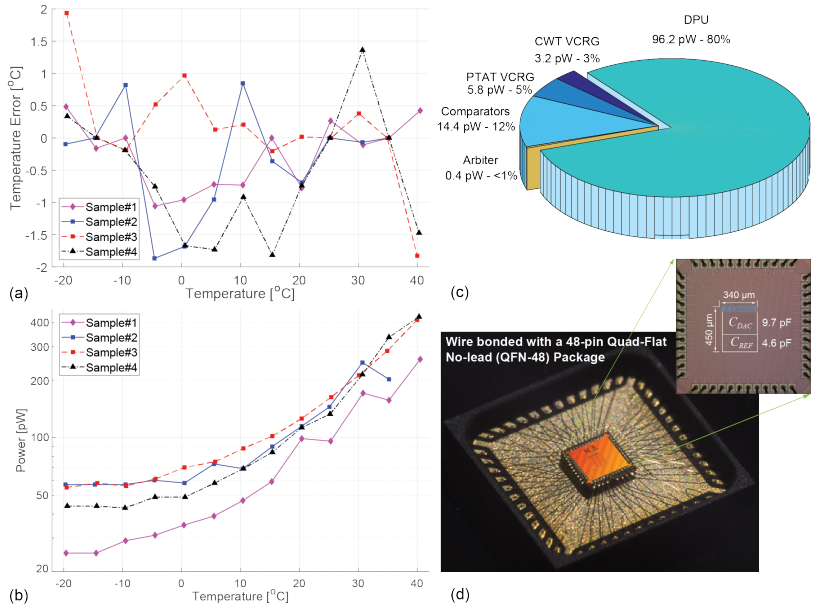


**Figure 4.4**: Measured temperature error (a) and power (b) of the temperature sensor. Power breakdown (c) and die micrograph (d) of the temperature sensor.

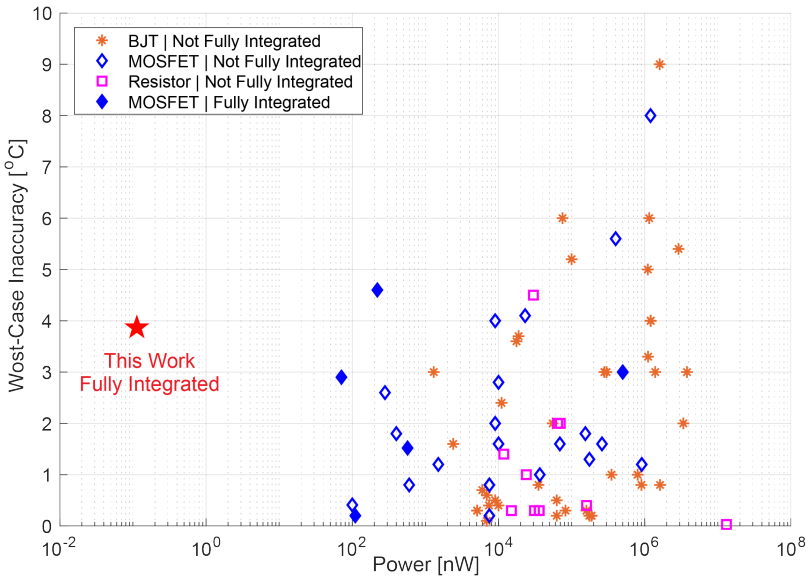


**Figure 4.5**: Power consumption versus worst-case inaccuracy revealing that the proposed temperature sensor consumes the lowest reported power while obtaining comparable worst-case inaccuracy.

# Chapter 5

# A Battery-Powered Wireless Ion Sensing System Consuming 5.5 nW of Average Power

Advances in sensors and wireless technologies have enabled new and exciting classes of wearable devices for applications in precision athletics, health, and wellness. However, growth in the wearables market has been slower than many expected, in part due to challenges related to device size, battery life, and sensing capabilities. For example, many current wearables with relatively sophisticated capabilities are larger than desired, in part due to the requirement of a large battery, which is necessary to have acceptable battery life given the relatively high power consumption of underlying circuits. In addition, many wearable devices currently measure only a small handful of physical or electrophysiological parameters such as pressure [68], motion [69], temperature [46], electrocardiography (ECG) [70], or electroencephalography (EEG) [71]. While such parameters might be useful for general well-being or for very specific medical use-cases, more sophisticated sensing functionality is desired to make information derived from wearables more actionable and/or impactful across a wide range of applications.

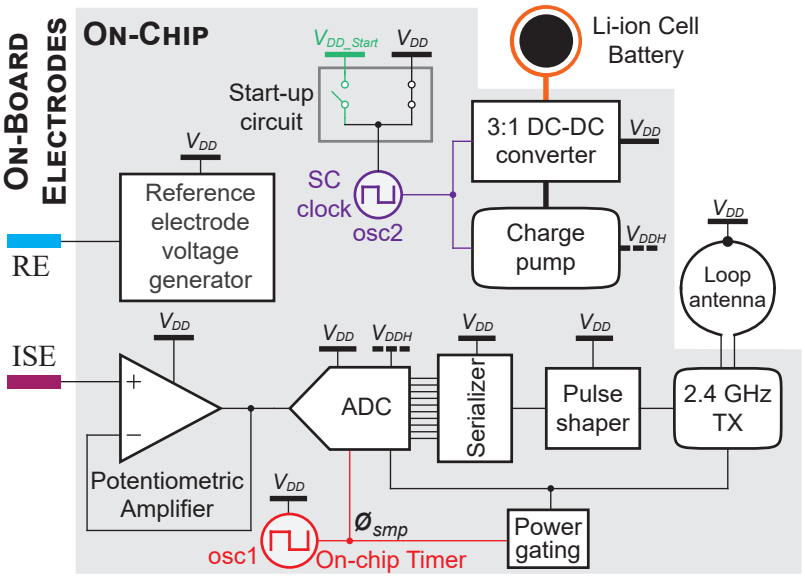


**Figure 5.1**: Block diagram of the wireless ion sensing system featuring complete sensing to transmission functionality.

Measurement of physiochemical parameters, for example ion homeostasis in sweat, blood, saliva, or tears, can potentially provide valuable additional insight into a user's overall health status. For example, measurement of sodium together with heart rate may enable real-time assessment of the risk of congestive heart failure, while monitoring of sodium and calcium may enable diagnosis or monitoring of syndrome of inappropriate anti-diuretic hormone secretion (SIADH) or hyponatremia. While previous work has demonstrated real-time sensing of ion concentration is possible on the body via low-cost patches, temporary tattoos, and other form factors [72–74], such sensors were not integrated with small, ultra-low-power sensing instrumentation and/or wireless communication functionality.

This chapter presents the design of a sensing system that integrates ion-selective electrodes with ultra-low-power sensor instrumentation, a wireless transmitter, and power management circuits [75]. A block diagram of the system is shown in Fig. 5.1. All circuit blocks, described in detail in Section 5.1, are carefully designed and optimized to consume nW power levels (or lower) in order to ensure ultra-long operation under battery power, or in future implementations

via small energy harvesters (e.g., [7,76]). Measurement results presented in Section 5.2 reveal the nW-level power consumption with acceptable system-level performance, including in-vitro results of sodium ion sensing.

## 5.1 Wireless Ion Sensing Platform

The proposed ion sensing system, shown in Fig. 5.1, comprises an ion selective electrode (ISE) that interfaces to a high-impedance potentiometric amplifier. A co-fabricated reference electrode (RE) is driven by a reference voltage generator, and is used to set the solution potential. The output of the potentiometric amplifier is digitized by a 10 S/s reference-free charge sharing analog-to-digital converter (ADC). Digital samples are then serialized, shaped, and then sent to a 2.4 GHz RF transmitter. The overall wireless sensing system is powered from a 1.8 V supply, for example from a small on-board battery, which is divided by a 3:1 switched-capacitor DC-DC converter to generate a 0.6 V supply voltage, $V_{DD}$, used by the majority of the circuits on-chip. A second supply voltage, $V_{DDH} = 1.2$ V, is generated by an on-chip charge pump for the purposes of increasing the $I_{ON}/I_{OFF}$ ratio of critical transistors via boosted gate driving or super cut-off gating. A start-up circuit is employed to ensure the DC-DC converter is clocked during cold-start before the switched-capacitor output is stabilized. Power gating, implemented with thick-gate transistors, is utilized to minimize the leakage current of the critical blocks during the off-state. A Serial Peripheral Interface (SPI) bus is implemented to perform benchtop calibration to characterize each block in Fig. 5.1. Design considerations and implementation details of each block are presented in the following sub-sections.

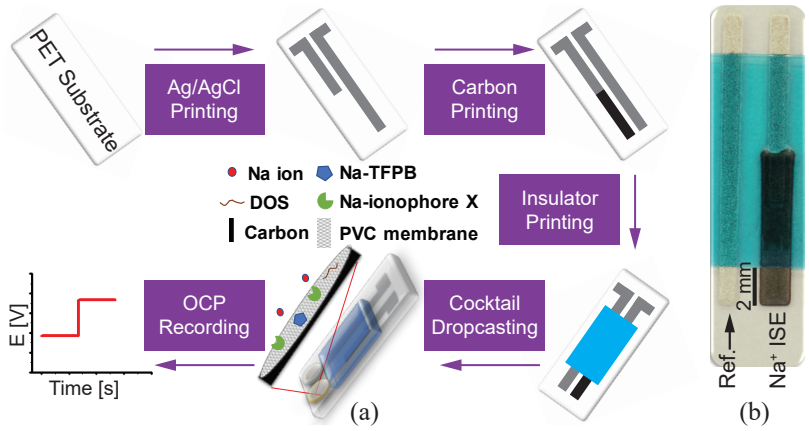


**Figure 5.2**: Fabrication procedure of the ISE (a) and photo of a fabricated ISE consisting of a working electrode and a reference electrode (b).

### 5.1.1 Fabrication of ISEs and Implementation of the Potentiometric Front End

The ISE and RE were fabricated utilizing screen-printing technology by employing a MPM-SPM semi-automatic screen printer (Speedline Technologies, Franklin, MA). Figure 5.2(a) outlines the overall fabrication procedure. A sequence of a silver/silver chloride (Ag/AgCl) and graphite layers followed by an insulator layer were printed on a polyethylene terephthalate (PET) substrate, followed by a curing step in a convection oven after the printing step of each layer. Specifically, the Ag/AgCl ink was cured at 85 $^{o}$C for 10 minutes, the carbon ink at 80 $^{o}$C for 10 minutes, and the insulator layer at 90 $^{o}$C for 15 minutes.

The ISE was then modified with a membrane consisting of 1 mg of sodium ionophore X, 0.55 mg of sodium tetrakis (3,5-bis[triuoromethyl]phenyl) borate (Na-TFPB), 33 mg of polyvinyl chloride (PVC), and 65.45 mg of bis (2-ethylhexyl) sebacate (DOS), all dissolved in 660 mL of nitrogen-purged tetrahydrofuran (THF). Up to 4 $\mu$L of the sodium ion ($Na^{+}$) selective membrane cocktail was then drop-cast on the carbon indicator electrode and left overnight to dry under ambient conditions.

The reference membrane, containing electrolytes and forming a nanoporous structure that

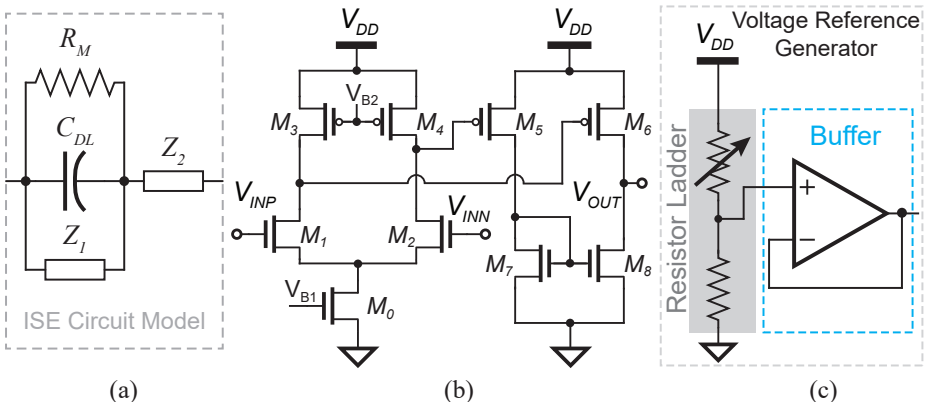


**Figure 5.3**: (a) Equivalent circuit model of the ISE. (b) Schematic of the potentiometric amplifier. (c) Schematic of the reference voltage generator.

allows the exchange of electrolytes with the solution and provides a stable potential insensitive to changes in the ion concentration over a large concentration range, was prepared by dissolving 78.1 mg of Polyvinyl butyral resin BUTVAR B-98 (PVB) and 50 mg of NaCl in 1 mL methanol. Then, the reference electrode was modified by 3 $\mu$L of PVB membrane and left to dry overnight alongside the ISE in ambient conditions.

As shown in Fig. 5.2(b), the fabricated ISE consists of a pseudo reference electrode, driven by the on-chip reference voltage generator, and a working carbon electrode, which interfaces with the on-chip potentiometric amplifier. A blue insulator was screen printed over the surface of the electrode pattern to confine the electrode and contact areas and prevent contamination leakage. The electrodes are disposable and an equivalent circuit model [77] is shown in Fig. 5.3(a), where $R_M$ is the membrane resistance, $C_{DL}$ is the double-layer capacitance, $Z_1$ is the Warburg diffusional element, and $Z_2$ represents mobile cation and anion transport through a hydrated film.

To handle the $\sim$0.2$-$0.5 V input range from the $\sim$G$\Omega$ ISE (dominated by $R_M$ in Fig. 5.3(a)) under the constraints of a 0.6 V supply voltage, a two-stage differential-to-single-ended amplifier with at most 3 stacked transistors is employed with a 0.3 V output swing, a 50 dB gain, and a 57 Hz unity-gain bandwidth, as shown in Fig. 5.3, and configured in unity gain feedback to operate as an impedance buffer. Simulation results show that the potentiometric amplifier

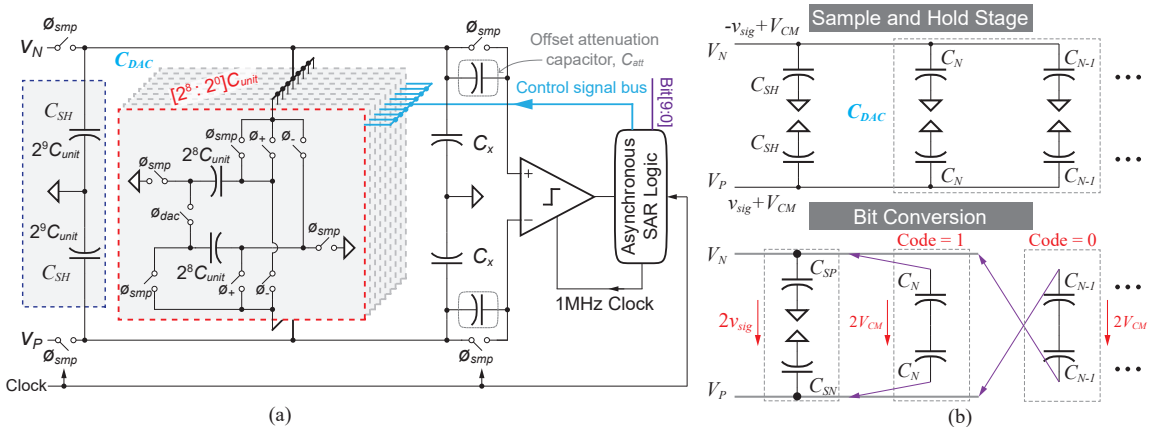


**Figure 5.4**: (a) Schematic of the reference-free charge-sharing ADC with offset attenuation and (b) charge-sharing during sample/hold and bit conversion.

achieves ∼TΩ input impedance, sufficiently large for interfacing with the ∼GΩ ISE, and an output noise of 40 $\mu$V. A MOS-bipolar pseudoresistor-based ladder with a tuning step of 10 mV is implemented to generate a reference voltage, with a simulated 380 $\mu$V variation across 0 to 100$^o$C and a standard deviation of 4.8 mV due to process variation. This voltage is then buffered by a two-stage amplifier, which directly drives the reference electrode (Fig. 5.1).

### 5.1.2 Implementation of the ADC and Digital Processing Unit

The output of the potentiometric amplifier interfaces directly to a fully-integrated SAR ADC with all necessary peripheral circuitry included. Though previous works have demonstrated SAR ADC structures that achieve power efficient operation, most such solutions require external blocks such as reference generators which can consume even more power than the ADCs. In addition, most of the state-of-the-art ADC structures operate at higher frequencies than what is desired here (e.g., $>$ 1 kHz). Simply scaling down the clock frequency of such approaches will likely yield deteriorated energy efficiency due to increased leakage energy consumption over the longer clock cycles [78]. On the other hand, the charge sharing SAR ADC shows a good capability of scaling the operating frequency while achieving an area-efficient, low-complexity,

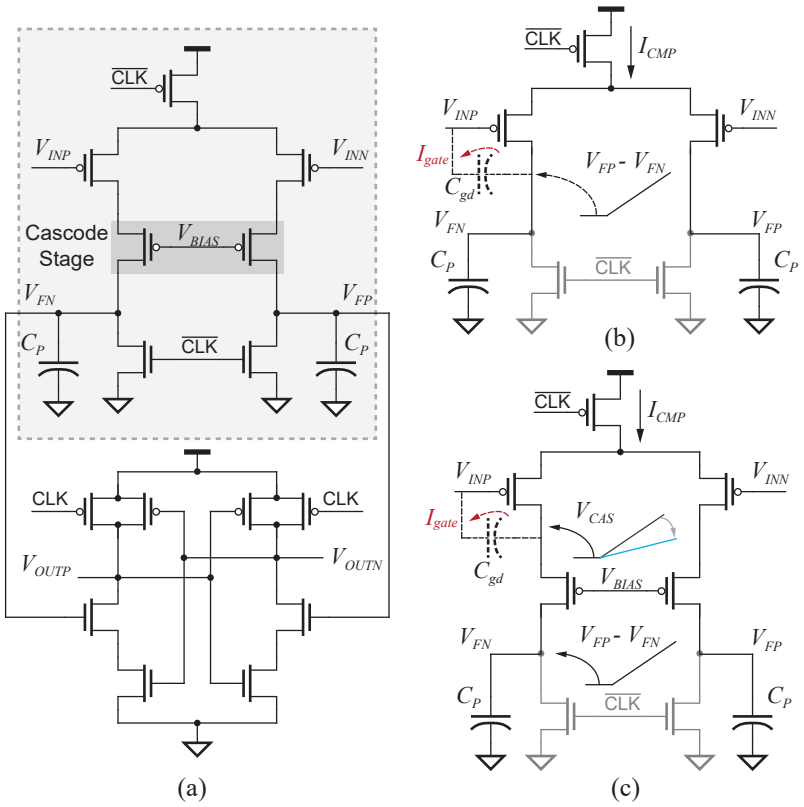


**Figure 5.5**: (a) Schematic of the energy-efficient two-stage comparator. (b) Differential kick-back current to the comparator input without cascode stage. (c) Differential kick-back current to the comparator input with cascode stage.

and power efficient design. A reference-free charge-sharing SAR ADC architecture [79] is utilized for digitization in the proposed ion sensing system, where energy from the signal itself is bottom-plate sampled and then charge-shared across the capacitive DAC during bit cycling. The overall schematic of the SAR ADC is shown in Fig. 5.4(a). Here, the input signals, $V_N$ and $V_P$, which can be represented by $-v_{sig}+V_{CM}$ and $+v_{sig}+V_{CM}$, respectively, are first sampled onto both the sample and hold capacitors, $C_{SH}$, and the binary-weighted DAC capacitors, $C_1$ to $C_N$. During bit conversion, as shown in Fig. 5.4(b), the differential signal, $2v_{sig}$, is mapped to a charge signal, $Q_{sig} = 2v_{sig}C_{SH}$. In the meantime, $V_{CM}$ is extracted and converted to reference charge, ($Q_N = 2V_{CM}C_N$). The binary weighted $Q_N$ are then successively connected to $V_P$ and $V_N$ to approximate $Q_{sig}$ until the residual charge between $V_P$ and $V_N$ converges to zero.

The comparator was implemented with an energy-efficient dynamic two-stage topology [80], and is shown in Fig. 5.5(a). The first stage (indicated by the dashed box in Fig. 5.5(a)) amplifies the differential input signals from $V_{\{INP,INN\}}$ to $V_{\{FP,FN\}}$, while the second stage consists of both a simple voltage amplification stage and a positive feedback loop to achieve rail-to-rail outputs, $V_{\{OUTP,OUTN\}}$. The input referred noise, $\sigma_V$, of the comparator, which is dominated by the input pair of the first stage, is given by:

$$\sigma_V = \frac{8kT}{C_P}\frac{\phi_t}{V_{threshold}}, \tag{5.1}$$

where $C_P$ is the parasitic capacitance at the output nodes of the first stage, $\phi_t$ is the thermal voltage, and $V_{threshold}$ is the threshold voltage at which the first stage stops and the second stage takes over. To achieve a 10-bit resolution at 0.6 V, $C_P$ was designed to be larger than 40 fF as indicated by (5.1), and tunable for comparator offset calibration.

Kick-back noise can also be very significant in dynamic comparators. Conventionally, the magnitude of the kick-back noise can be minimized by employing a large capacitor at the comparator input, $C_{cmp,in}$, which effectively creates a low input impedance. However, in the proposed structure, $C_{cmp,in}$ consists of $C_{att}$ in series with $C_{DAC}$. With a gate-drain capacitance $C_{gd}$ $> 5$ fF in the input stage of the comparator, significant kick-back noise (hundreds of $\mu$V) can be observed at the input of the comparator and thus must be carefully considered in this design. As shown in Fig. 5.5(b), when the clock signal is high (i.e., when the first stage is in voltage amplification phase), voltages that approximate ramps, $V_{\{rampN,rampP\}}$, are generated at the output nodes of the first stage, which can be given by:

$$V_{\{rampN,rampP\}} = \frac{I_{CMP}}{2C_P}t, \tag{5.2}$$

where $I_{CMP}$ is the DC operating current of the first stage of the comparator. $V_{\{rampN,rampP\}}$, in return, introduce a kick-back current, $I_{gate}$, via the drain-to-gate capacitor, $C_{gd}$, of the input

transistor pair, which can be computed as:

$$I_{gate} = \frac{I_{CMP}}{2C_P} C_{gd}. \tag{5.3}$$

During each comparison cycle, the first stage operates for a period of $T_{int}$ before the second stages begins to work. $T_{int}$ is given by:

$$T_{int} = \frac{2C_P}{I_{CMP}} V_{threshold}. \tag{5.4}$$

As a result, the total charge variation introduced by the kick-back current during one comparison cycle can be calculated by:

$$Q_{var} = V_{threshold} C_{gd}. \tag{5.5}$$

Though, to the first order, $Q_{var}$ can be canceled out since it shows on both inputs as a common mode signal, it can effectively introduce an offset due to the mismatch in the input pair as well as in the DAC. More concerning, however, is that signal-dependent charge variation can be observed during the comparison, which would introduce non-linearities. To address kick-back related issues, in the proposed ADC a cascode pair was implemented to isolate the output node from the inputs of the first stage, thus minimizing the signal-dependent charge variation [81], as illustrated in Fig. 5.5(c). Simulation results reveal a greater than $3\times$ reduction in signal-dependent charge variation by reducing the differential voltage amplitudes at the drain of the input pair.

Since the operation of the charge-sharing ADC is based on the redistribution of the signal charge, $Q_{SIG}$, sampled during the sample and hold phase plus an error charge, $Q_{ERR}$ during bit conversion phase, nonlinearities will be introduced if $Q_{ERR}$ changes as bit conversion proceeds. On the other hand, comparator offsets, due to transistor-matching issues or unequal kick-back, can lead to time-varying $Q_{ERR}$ and thus nonlinearities in charge-sharing SAR ADCs [82]. The proposed design employs, in addition to capacitive comparator offset calibration and cascode kick-back reduction transistors, an offset-attenuation capacitor, $C_{att}$, to isolate the comparator

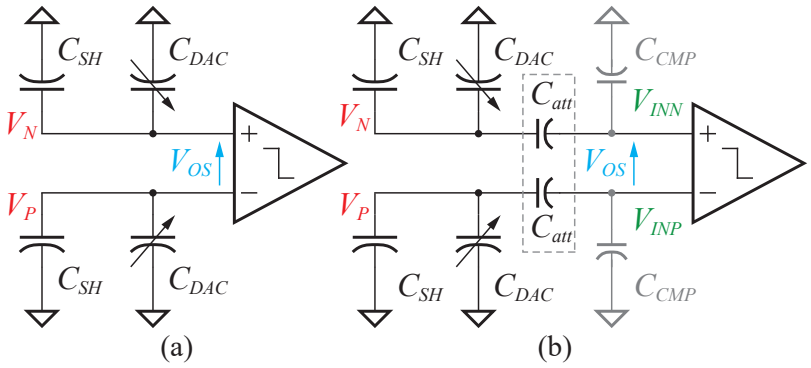


**Figure 5.6**: Comparator offset in charge-sharing SAR ADC without $C_{att}$ (a) and with $C_{att}$ to isolate the sampling and hold, and DAC capacitors from the comparator (b).

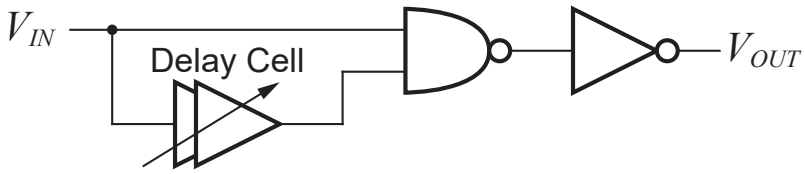


**Figure 5.7**: Schematic of the pulse shaper logic with tunable delay employed to minimize the quiescent power of the DC-DC converter.

input from the DAC and the sample and hold capacitor. Fig. 5.6(a) shows a simplified block diagram of the charge-sharing ADC and the input offset voltage of the comparator ($V_{OS}$) without an attenuation capacitor. Here, offset charge, $Q_{OS}$, can be calculated by:

$$Q_{OS} = V_{OS}(C_{SH} + C_{DAC}). \tag{5.6}$$

As shown in (5.6), while $V_{OS}$ is manifested as a fixed voltage, the charge domain offset, $Q_{OS}$, changes during bit conversion as $C_{DAC}$ alters, thereby introducing signal-dependent offset and deteriorating linearity. The offset-attenuation capacitor, $C_{att}$, employed in this work, on the other hand, isolates $V_{OS}$ from $C_{DAC}$. As shown in Fig. 5.6(b), the offset charge at $V_{\{P,N\}}$ becomes:

$$Q_{OS,att} = V_{OS}\frac{C_{att}(C_{SH} + C_{DAC})}{C_{att} + C_{SH} + C_{DAC}}. \tag{5.7}$$

For fast prototyping, $C_{att}$ is implemented with a 3 pF Metal-Insulator-Metal (MIM) capacitor, while the total capacitance of the $C_{SH}$ and $C_{DAC}$ ($C_{unit}$ = 44 fF) is 45 pF, though techniques such as placing capacitors in series or customized metal capacitors can render a smaller $C_{unit}$. Therefore, $C_{SH} + C_{DAC} \gg C_{att}$ and (5.7) becomes:

$$Q_{OS,att} \approx V_{OS} C_{att}. \tag{5.8}$$

The offset charge observed at $V_{\{P,N\}}$ thus becomes constant during bit conversion, as indicated by (5.8), thereby minimizing the nonlinearity introduced by the input offset voltage of the comparator. On the other hand, the decision making of the comparator is performed at the input of the comparator in voltage domain, $V_{\{INP,INN\}}$. As shown in Fig. 5.6(b), $C_{att}$ can also divide $V_{\{P,N\}}$ via $C_{CMP}$, the input capacitance of the comparator. However, since $C_{att} \gg C_{CMP}$ ($C_{CMP}$ = $\sim$10 fF), the input voltages at the comparator inputs $V_{\{INP,INN\}} \approx V_{\{P,N\}}$, indicating that $C_{att}$ has negligible impact on the dynamic input signal to the comparator. Simulation results reveal a DNL of +2.1/-1 LSB with a 2 mV comparator offset without attenuation capacitors (Fig. 5.6(a)), while a DNL of +0.7/-0.7 LSB is achieved by employing the attenuation capacitor, $C_{att}$, indicating an over 2$\times$ linearity improvement, in good accordance with the above analysis. The switches in the DAC are designed with minimum size to reduce charge injection, yet to increase on-conductance and minimize non-linearities, they are activated by the charge pump supply, $V_{DDH}$ (Fig. 5.1), for a 3$\times$ improvement in $R_{off}/R_{on}$.

To further minimize power at low sampling rates, the ADC is primarily implemented with long-length and high-$V_t$ transistors, and is asynchronously controlled. Specifically, despite requiring a sampling rate of only 10 S/s, the ADC runs instantaneously during bit cycling at a clock rate of 1 MHz. After bit cycling is complete the ADC is clock-gated and placed into a low-power sleep state until the next 10 Hz sample clock edge. The 1 MHz clock is generated by the asynchronous unit as the SAR logic ripples through the 10 controlling slices [83]. The 10 Hz

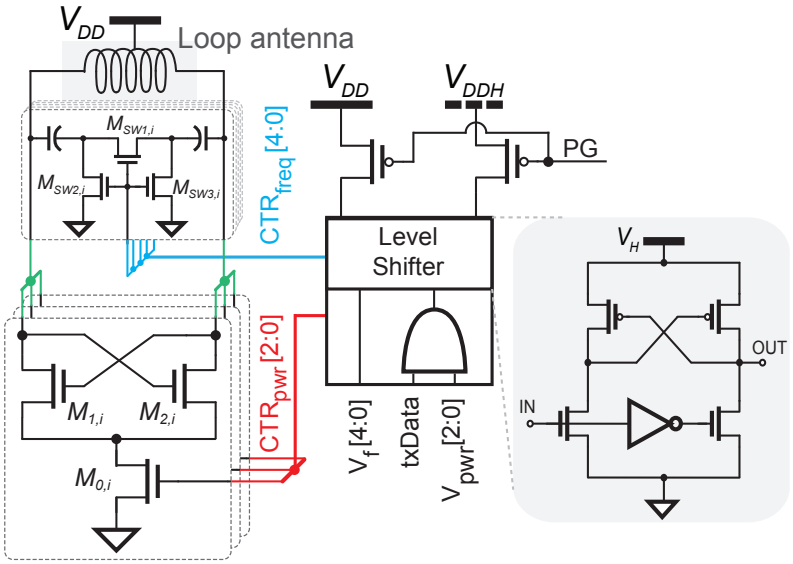


**Figure 5.8**: Schematics of direct-RF power oscillator transmitter where the conventional tail current sources were replaced with triode-region switches to maximize the gate to source voltage of the cross-coupled transistors.

sampling clock is generated by a low power capacitive-discharging on-chip oscillator ('osc1' in Fig. 5.1) [41], whose power consumption is 140 pW when operating at 10 Hz. To the best of our knowledge, no prior-art SAR ADCs achieve sub-nW power levels at 10s of samples per second when including all biasing, clocking, and other necessary peripheral circuits; prior-art that does report sub-nW power of the ADC core (e.g., [84] which consumes 650 pW at 50 S/s) does not include the power of such peripheral circuits.

Since the transmitter is active during a logic '1', and as described below the TX active power dominates system power budget, the 10-bit ADC output is serialized and passed through pulse-shaping logic to reduce the pulse width for a logic '1'. The delay cell in the conventional pulse shaper shown in Fig. 5.7 to minimize the active time of the TX, thus saving TX power overhead.

### 5.1.3 Implementation of the 2.4 GHz RF Transmitter

The 2.4 GHz TX utilizes a direct-RF power oscillator architecture, shown in Fig. 5.8, using an on-board 2.8 mm diameter loop antenna as both a radiative and resonant element. Such direct-RF power oscillator structures provide inherent impedance matching to loop antennas and can be readily gated down to very low leakage power levels [10].

In this design, a center tap in the loop antenna is connected to $V_{DD}$, which provides power to the negative resistance generator. Conventionally, negative resistance is achieved via a cross-coupled pair with a tail current source, whose current can be controlled via a binary-weighted current-mirror approach. Current control is useful to control oscillation amplitude, and therefore the amount of radiated power. However, operation of a current mirror transistor requires $V_{DS} > V_{sat,sub-Vt} \approx 100$ mV in subthreshold to maintain operation in saturation. This $V_{DS}$ requirement degrades the gate-to-source voltage headroom of the cross-coupled transistors. When more tail current transistors are turned on to increase current, the gate-to-source voltage of the cross-coupled transistors need to be increased accordingly, which is difficult under a fixed supply. At a low supply voltage (e.g., 0.6 V in this design), the increased gate-to-source voltage squeezes $V_{DS}$ of the tail current transistor and therefore degrades the effects of current tuning due to channel length modulation.

In the proposed design, the tail current sources in [10] are replaced with three triode-mode switches and each of them controls a pair of binary-weighted cross-coupled devices. By turning on and off the switch transistors, different weight cross-coupled devices are activated, thus controlling the value of current injected into the LC tank. Since the switch transistors are completed turned on and off, $V_{DS,M0,i}$ is near zero when it's on. Therefore, the gate-to-source voltage of the cross-coupled pair is maximized, eliminating the conflict between $V_{DS,M0,i}$ and $V_{GS,M1(or\ 2),i}$ when increasing the current. The current tuning range of the TX is thereby increased by 41%, as shown in Fig. 5.9.

Increasing the number of the cross-coupled pairs will provide better control ability and

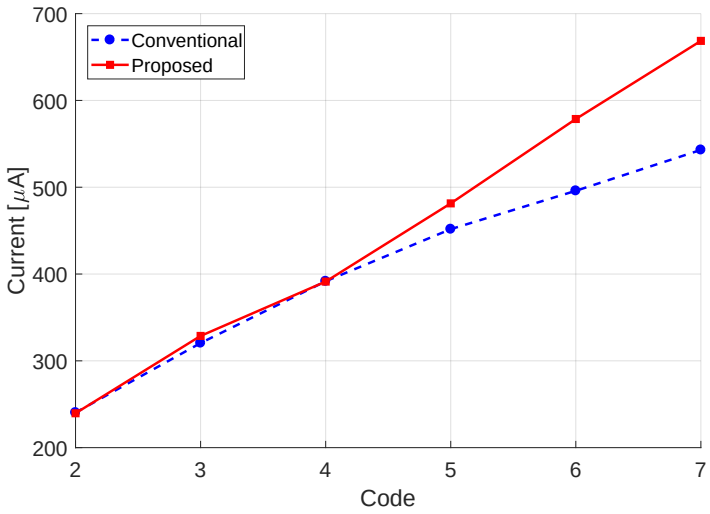


**Figure 5.9**: Simulated current tunning ability of the proposed (triode-mode) and conventional (saturation-mode) tail devices in an RF power oscillator.

higher resolution, but the leakage current will also increase proportionally. As the TX is deeply duty-cycled, the standby power matters here. Since three pairs can fulfill the requirements in this application, the number of controlling bits is set to be three to achieve a good trade-off between tuning ability and standby power.

While the TX in this design is on-off keying (OOK) modulated by turning on a fixed number of tail switches completely on and off, the improved linearity of the triode-mode switches may be useful in future designs that employ at amplitude-modulated signals. The triode-mode switches also decrease the transistor size and parasitic capacitance by 84% by maximizing the gate-source voltage $V_{GS}$ of the cross-coupled devices. For the same radiation frequency, the reduced parasitic capacitance permits a larger antenna (0.3 mm larger in diameter) and therefore increases the radiation efficiency (by 16.6% from simulation) and transmitter output power. To further minimize the parasitic capacitance introduced by the cross-couped devices, $M_1, i$ and $M_2, i$ are implemented with low-$V_t$ devices so that they can conduct the same current with 20$\times$ less size than the high-$V_t$ devices. On the other hand, $M_0, i$ does not have a size limitation, and is thus implemented with high-$V_t$ transistors, which, when sized up for the equivalent on-conduction of a

thin-oxide low-$V_t$ transistor, achieves 100$\times$ lower leakage current in the off mode.

The center frequency of the TX is controlled by the value of inductance and capacitance. The capacitor is implemented using a 5-bit binary-weighted array of digitally-activated MIM capacitors, totaling 590 fF, and the inductor is implemented using a single-turn circular loop of copper on the board, which are both fairly temperature insensitive. The parasitic capacitance of the transistor may vary by a small amount with temperature, however, which is negligible compared to the 590 fF MIM capacitor. The relatively stable environment temperature of the application (wearable devices) of this design further ensures the frequency stability. To reduce the on-resistance of the digital switches and minimize the impact on the quality factor of the antenna, level shifters operating from $V_{DDH}$ are used to drive the differential switches that connected to the capacitors.

The TX is deeply duty-cycled, and activated once every 100 ms, transmitting at an instantaneous data rate of 4 Mbps. Between transmissions, the TX is set to an ultra-low-power sleep state by gating the tail transistors and power gating the control signals and level shifters, the latter of which reduces leakage power by 4$\times$.

(This chapter was a cooperated work with Xiaoyang Wang.)

### 5.1.4 On-board Antenna Design

The power oscillator's loop antenna was implemented as a single-turn circular loop of 1 oz (i.e., 35 $\mu$m thick) copper on an FR-4 substrate. In many cases, antennas for small portable electronic devices are electrically small, and their radiation efficiency increases with the physical size of the antenna [85]. Generally, the largest antenna permissible under application-driven size constraints is chosen. In the present application, the antenna should be made to be no larger than the size of a $\sim$3$-$5 mm coin cell battery. In addition, $\eta_{rad}$ of electrically small antennas increases with frequency, and thus the antenna should support a self-resonant frequency as high as possible, though in close proximity to an Industrial, Scientific, and Medical (ISM) band (e.g., 2.4 GHz).

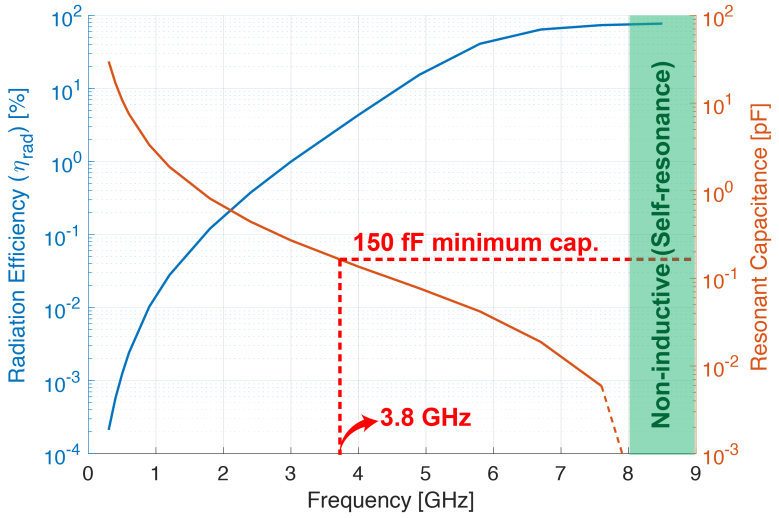


**Figure 5.10**: $\eta_{rad}$ and the required capacitance for resonance of a 2.8 mm diameter TX antenna with two 4 mm bond wires.

Figure 5.10 illustrates simulated $\eta_{rad}$ of a circular coil with a trace width of 0.4 mm and a diameter of 2.8 mm, when this antenna is connected to the power oscillator via two 4 mm bonding wires and the parasitics of a $9 \times 9$ mm$^2$ QFN package. Here, it can be seen that operating at higher frequencies offers improved $\eta_{rad}$. However, the power oscillator requires the antenna to look inductive, and thus it is forbidden to choose the carrier frequency beyond the self-resonant frequency (8 GHz in Fig. 5.10). In addition, the parasitic capacitance of the bonding pads and electrostatic discharge diodes restricts the maximum resonant frequency since it decides the minimum resonant-tuning capacitance. Based on the layout-extracted parasitic capacitance (150 fF), a maximum resonant frequency of 3.8 GHz is achieved, as shown in Fig. 5.10, which offers sufficient margin to safely operate in the 2.4 GHz ISM band. If the size of the antenna were increased to afford increased $\eta_{rad}$, the resulting required resonant capacitance would decrease, as shown in Fig. 5.11. This helps set a bound on the maximum tolerable tuning capacitance for the present size, and a guideline for how much tuning capacitance would be needed if future designs were to use a slightly larger antenna size.

Note that while an on-chip antenna could have provided a fully integrated solution [86], on-

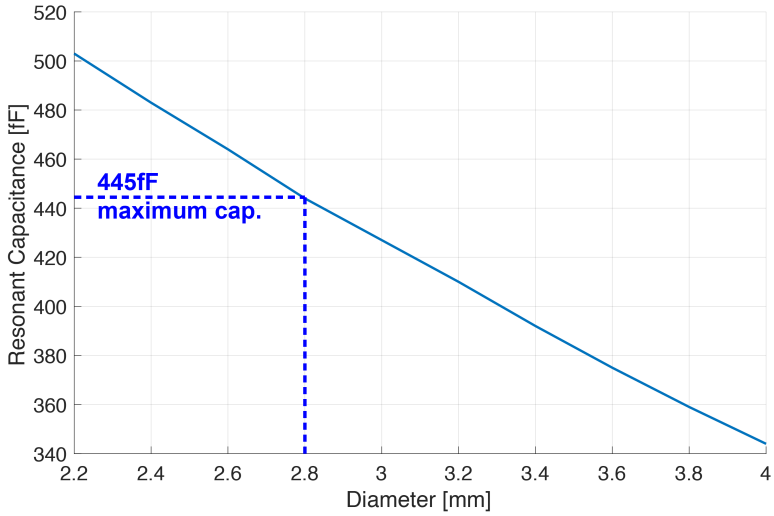


**Figure 5.11**: Required resonant capacitance for different size of antennas connected with minimum-estimated parasitic inductance (6.3 nH from two 4 mm bond wires).

chip antennas tend to suffer from: 1) low radiation efficiency, $\eta_{rad}$, due to the limited dimension, thus usually requiring operation at high frequencies (e.g., $>$ 10 GHz) which is not suitable for low-power applications; 2) larger capacitors to tune an on-chip antenna which will occupy a large core area and make it difficult to control the resonance at a fine step. On the other hand, in the proposed application the form-factor of the overall system is determined by the source device, for example, a battery. Therefore, an on-board antenna can achieve higher $\eta_{rad}$ and provides more design flexibility, and is thus employed here.

### 5.1.5 Implementation of the Power Management Unit

The overall system is powered by a 1.8 V battery, which is converted to 0.6 V via a 3:1 switched-capacitor DC-DC converter. Since the switching frequency is low (10 Hz) and load power is only a few nW, careful consideration must be taken to minimize leakage power. Amongst possible switched-capacitor DC-DC converter topologies, the Dickson topology can achieve 6.3$\times$ and 1.8$\times$ lower leakage power than the Ladder and Fibonacci topologies when configured for a similar ratio and with the same on resistance. In addition, the Dickson topology

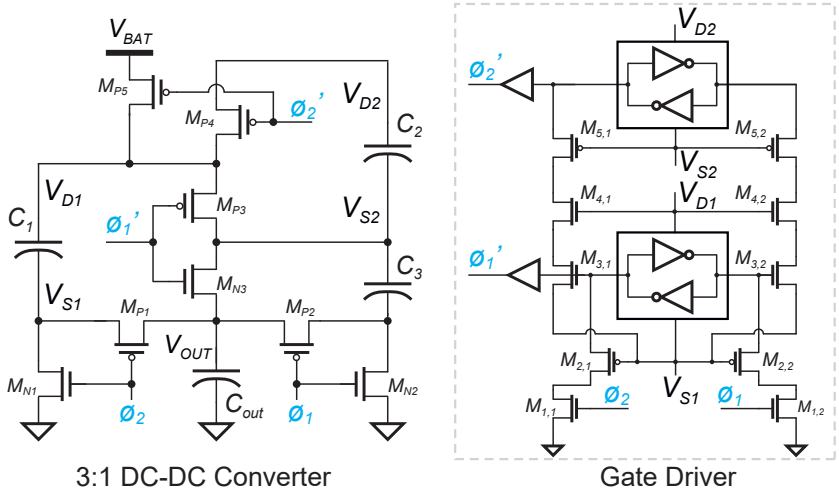


**Figure 5.12**: Architecture and gate driver of the nW power switched-capacitor DC-DC converter employed in the proposed ion sensing platform.

has low short-circuit current and good slow-switching limit (SSL) performance metrics [87], and is thus chosen for this design. The implemented converter is shown in Fig. 5.12 along with its gate driver and states during its two phases of operation (Fig. 5.13). The employed power switches are implemented using thin-oxide standard-$V_t$ transistors, which for the same on-resistance, offer 19$\times$ lower leakage than low-$V_t$ devices. Off-chip ceramic capacitors (each 1$\mu F$ and 1$\times$0.5 mm$^2$) are employed to support the large instantaneous current draws from the TX, while also enabling a low SSL impedance during continuous operation. To ensure proper operation, the main ESD supply voltage is connected to the battery voltage. In addition, multiple diodes are stacked to prevent breakdown and reduce the leakage and turn-on current.

At steady state, the three flying capacitors divide the supply voltage into several voltage domains. To reduce leakage power and the risk of breakdown, the circuit is driven by cascode level-shifters, which are powered from the local power capacitor connected to the relevant switch in each voltage domain. For example, the terminals across capacitor $C_1$ provide the power rails for the driver to switch transistors $M_{N3}$ and $M_{P3}$. To do so, clock signals $\phi_2$ and $\phi_1$, which are referenced between GND and 0.6 V, drive NMOS transistors $M_{1,1}$ and $M_{1,2}$ in the gate driver, respectively, which generate two pull-down signals connected to the sources of $M_{2,1}$ and $M_{2,2}$,

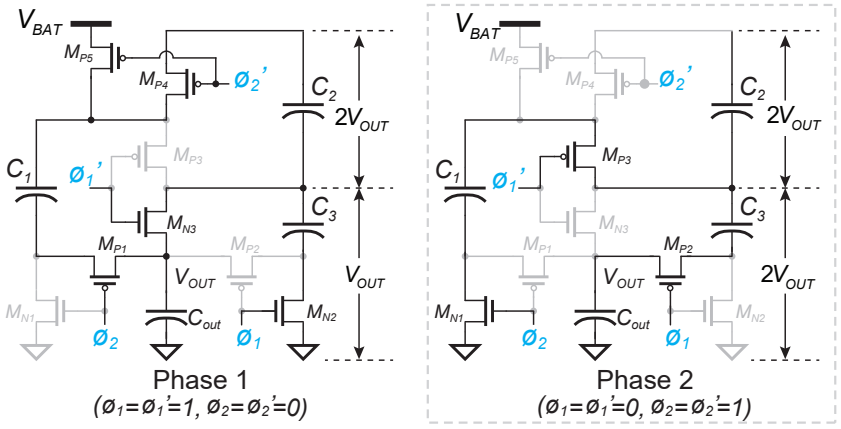


**Figure 5.13**: Connection during phase one ($\phi_1$=$\phi_1'$= 1, $\phi_2$=$\phi_2'$= 0) and phase two ($\phi_1$=$\phi_1'$=0 and $\phi_2$=$\phi_2'$= 1) of the nW power switched-capacitor DC-DC converter.

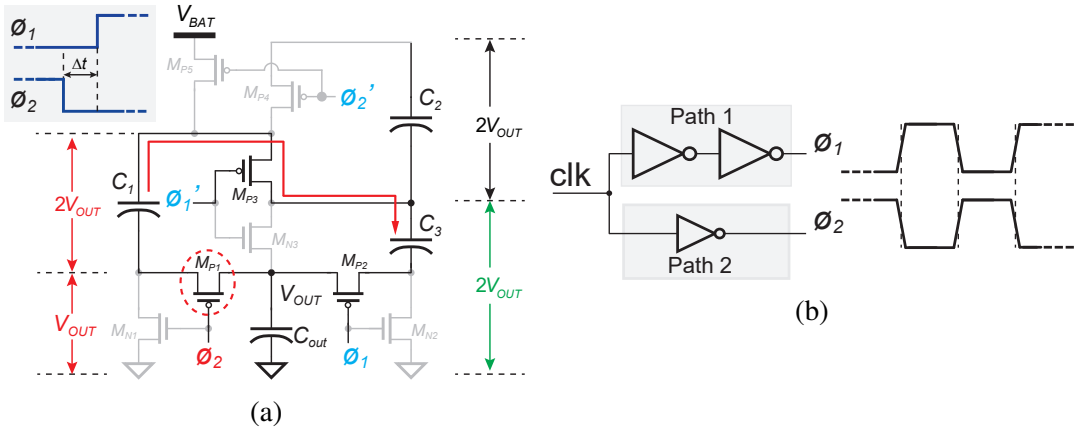


**Figure 5.14**: (a) Power dissipation introduced by the delay of $\phi_1$ and $\phi_2$ (b) Circuit to generate the aligned $\phi_1$ and $\phi_2$.

which toggle the latch formed by a pair of cross-coupled inverters to either the on or off position. The output of the latch is then buffered and then used to drive $M_{N3}$ and $M_{P3}$ (signal $\phi_1'$). Similarly, NMOS transistors $M_{3,1}$ and $M_{3,2}$ in the gate driver reproduce these signals to drive the level-shifter above them, whose voltage is generated via the rails of capacitor $C_2$, and used to drive $M_{P4}$ (signal $\phi_2'$). Since $C_1$ and $C_2$ provide a two times larger voltage to the driver than $C_{out}$, transistors $M_{N3}$ and $M_{P3-5}$ are sized accordingly smaller to reduce parasitic capacitance and leakage power.

During switching, delay of the two differential clock signals can introduce unnecessary short-circuit power dissipation. For example, if $\phi_2$ switches from "1" to "0" earlier than $\phi_1$ at

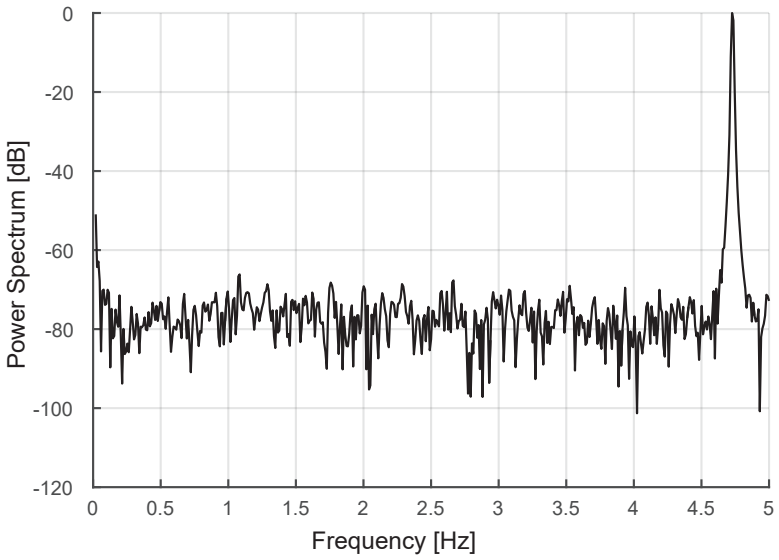


**Figure 5.15**: Measured 128-time averaged 1024-bin FFT plot of the charge-sharing ADC revealing an effective number of bits of 8.3b.

**Table 5.1**: Power Breakdown of the Ion Sensing System (The power of AFE, Buffer, ADC, Timer in pW).

| AFE | Buffer | ADC | Timer | TX | DC-DC Eff. | Total |
|---|---|---|---|---|---|---|
| 406 | 15×2 | 780 | 140×2 | 2.4 nW | 70.5% | 5.5 nW |

the end of phase 2 (when $\phi_1 = 0$ and $\phi_2 = 1$), as illustrated in Fig. 5.14(a), $M_{P1}$ would turn on and cascade $C_1$ and $C_{out}$, generating a voltage of $3V_{OUT}$ at the top plate of $C_1$. Since $M_{P3}$ would still be on in this situation, the voltage difference between the top plate of $C_1$ and $C_3$ generates a short-circuit current. Simulations of a baseline design without short-circuit current optimizations reveals a short-circuit power can be larger than the rest of the DC-DC converter's power. To minimize short-circuit current, the circuit in Fig. 5.14(b) is used to generate differential aligned clock signal to drive the switched-capacitor circuit. Faster inverters with even numbers are used in path 1 and slow inverters with odd number are used in path 2 to keep the delay the same while generating the differential clock signal. In this manner, quiescent power is reduced by at least 21%.

(This chapter was a cooperated work with Xiaoyang Wang.)

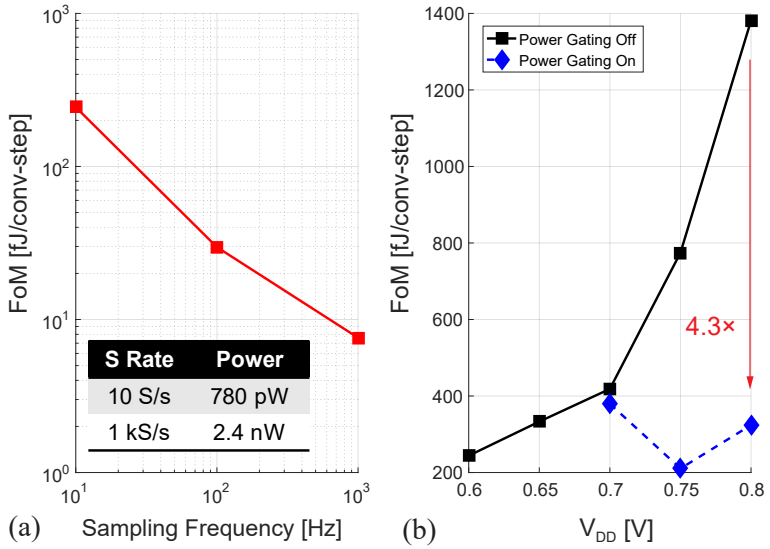


**Figure 5.16**: Measured FoM of the ADC when operating at different sampling frequency (a) and when operating from different supply voltages at 10 S/s (b), achieving an FoM better than 379 fJ/conv-step.

## 5.2 Measurement Results

The wireless ion sensing chip was implemented in a 1 mm $\times$ 1.2 mm 65 nm CMOS chip, and was packaged and soldered to a FR-4 substrate PCB with a 2.8 mm on-board loop antenna. For testing and debugging purposes, a 9$\times$9 mm$^2$ QFN package was employed. In a future design iteration, many of the chip pads could be left unconnected, and a chip-on-board bonding strategy would significantly reduce the occupied chip footprint. Small diameter batteries (e.g., down to 4.8 mm) could also be used to provide power in a very small form factor. During testing, the DC-DC converter provided a 0.6 V supply to all load circuits.

### 5.2.1 Benchtop Measurements

Benchtop measurement results show the potentiometric amplifier consumed 406 pW when operating from a 0.6 V supply. This includes the power required to drive the capacitors in the SAR ADC. At 10 S/s, the reference-free SAR ADC was measured to consume 780 pW, including

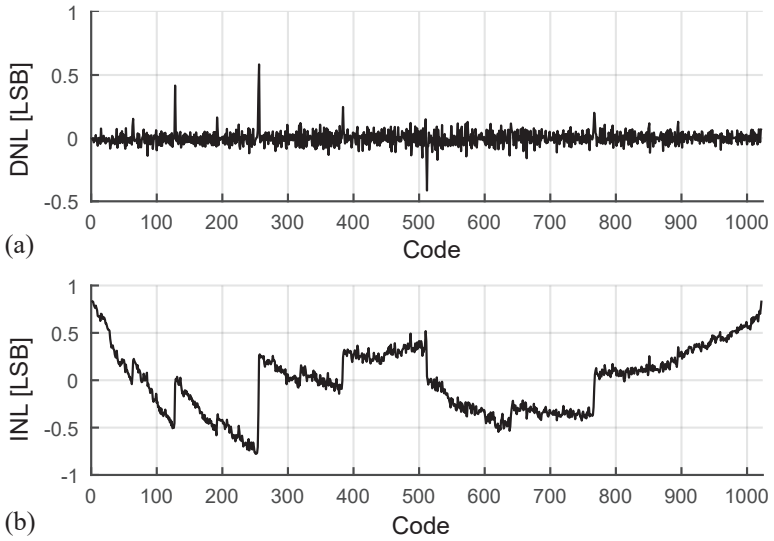


**Figure 5.17**: Measured DNL (a) and INL (b) of the reference-free charge-sharing ADC employed in the ion sensing platform.

the power of the 4.2 pW charge pump (Fig. 5.1), which, to the best of our knowledge, is the lowest power 10-bit 10 S/s ADC with all peripheral circuits integrated. The measured input referred noise of the comparator was 350 $\mu$V.

Since different spectrum tests were required to characterized the performance of the ADC in different environment while the ADC was operating at very low frequency (down to a few Hz), to accelerate the measurement a 1024-point FFT was calculated. However, since the frequency band of interest was only 0 to 5 Hz, a 1024-bin FFT provided a frequency resolution better than 0.005 Hz, which is good enough for the purpose of benchmarking the ADC ENOB. To achieve an accurate noise floor measurement, as shown in Fig. 5.15, a 128-times averaged 1024-point FFT with Hanning windowing was performed, and an ENOB of 8.3 bits was measured (ENOB degradation was mainly introduced by comparator noise and DAC parasitics), for an energy efficiency of 244 fJ/conv-step. At such a low sampling frequency, measured efficiency was dominated by leakage power. Figure 5.16(a) shows the measured figure-of-merit (FoM) at different sampling frequencies. At 1 kS/s, the ADC power was 2.4 nW and the measured ENOB was 8.31 bits, resulting in an efficiency of 7.6 fJ/conv-step, further illustrating the leakage

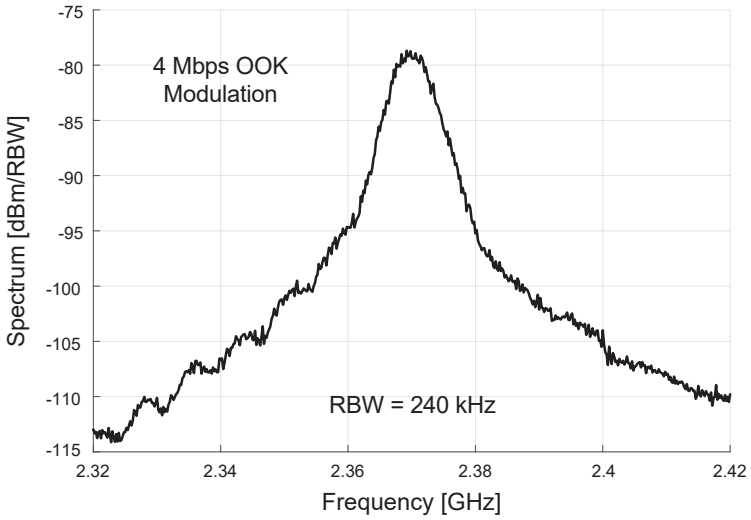


**Figure 5.18**: Spectrum measured using a λ/4 whip antenna placed ∼10 cm from the on-board loop antenna with 4 Mbps OOK modulation.

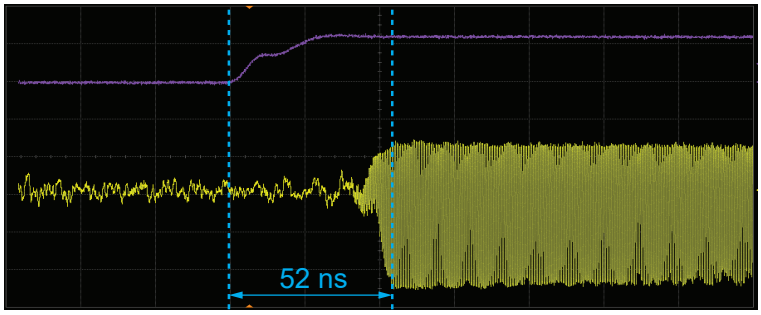


**Figure 5.19**: Measured TX start-up time indicating the proposed TX employing in the ion sensing platform can start up within 52 ns.

dominance at low sampling rates. When operating from 0.6 to 0.8 V with a sampling rate of 10 S/s, the measured FoM varied from 244 fJ/conv-step at 0.6 V to 1381.2 fJ/conv-step at 0.8 V without power gating, as shown in Fig. 5.16(b). Power gating, which could be enabled when $V_{DD} > 0.7$ V, improved the FoM significantly (e.g., 4.3× at 0.8 V) by reducing leakage in the sleep mode, and ensured an FoM better than 379 fJ/conv-step across the supply ranges from 0.6 to 0.8 V. The measured DNL and INL were -0.36/0.58 LSB and -0.77/0.84 LSB, respectively, as shown in Fig. 5.17.

At 1 m distance, the TX radiated -64.6 dBm of power as measured by a λ/4 whip antenna.

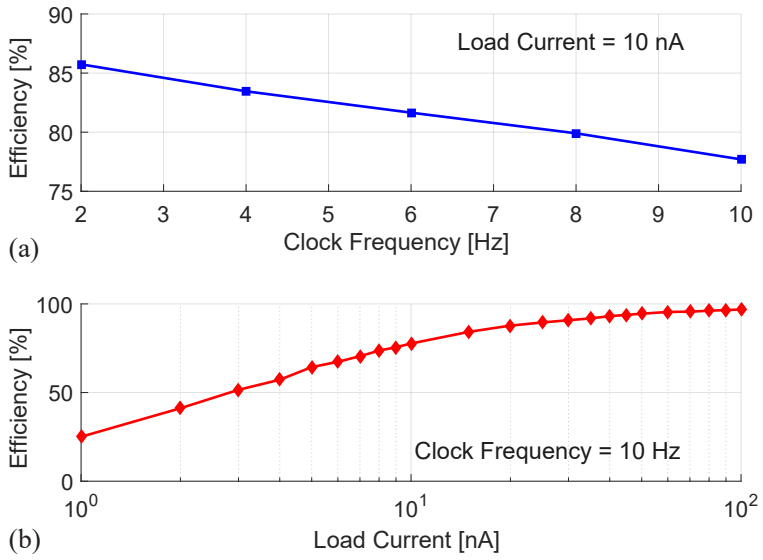


**Figure 5.20**: Measured efficiency of the DC-DC converter versus clock frequency (a) and load current (b).

Fig. 5.18 shows the measured output spectrum measured at ∼10 cm with a λ/4 whip antenna when operating with 4 Mbps OOK modulation. When transiently powered by $C_{out}$, a 1 $\mu$F 1×0.5 mm$^2$ capacitor, the TX consumed 154.5 $\mu$W of instantaneous power, corresponding to a bias current of 257 $\mu$A, set by the default power control code "010". The start-up time of the TX was measured to be $<$ 52 ns, as shown in Fig. 5.19. The measured sleep-mode power of the TX was 500 pW, thus achieving an average power of 2.4 nW after duty-cycling to 100 bps (i.e., 10 S/s).

Clocked by the reference-free relaxation oscillator, the switched-capacitor DC-DC converter operated between 2-10 Hz. The measured efficiency of the DC-DC converter at different frequencies with 10 nA load current is shown in Fig. 5.20(a), while Fig. 5.20(b) shows measured efficiency with different load current when operating at 10 Hz. As shown in Fig. 5.20(b), the DC-DC converter achieved a peak efficiency of 96.8% when operating with a load current of 100 nA.

Table 5.1 shows the power breakdown of the whole ion sensing system. Together, all of the load circuits in the wireless ion sensing system consumed 3.9 nW. At this load, the DC-DC

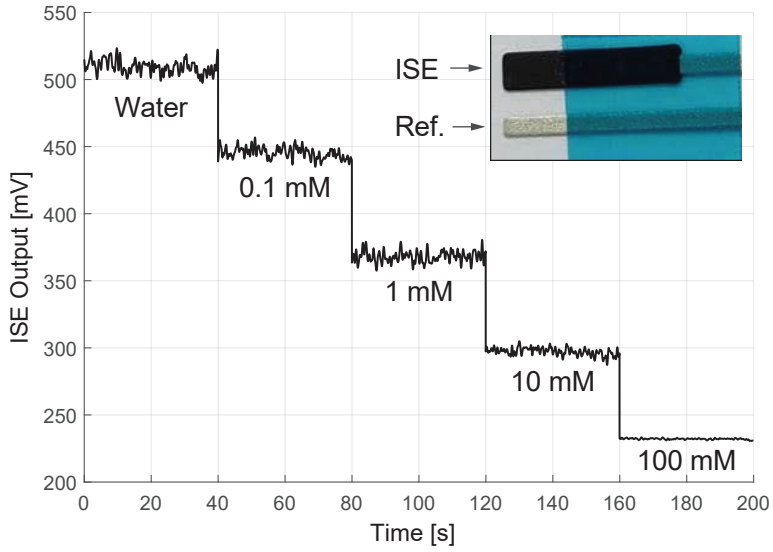


**Figure 5.21**: In-vitro ion concentration measurements with $Na^+$-selective electrode and 0.1 mM to 100 mM NaCl concentration.

converter achieved an efficiency of 70.5%, for a total system power consumption of 5.5 nW.

### 5.2.2 In-vitro Tests

The ion sensing system was measured in-vitro with 0.1-100 mM NaCl concentration with the SPI configured to the default tuning set. The Ag/AgCl reference electrode, consisting of a polymeric PVB membrane, was biased by the ladder-based reference generator at 500 mV to provide a stable, mid-supply solution potential for the ISE output recording (Fig. 5.21). The ADC was configured as pseudo-differential structure: the input $V_N$ in Fig. 5.4, was connected to the output of potentiometric amplifier while $V_P$ was biased through a voltage buffer (Fig. 5.2(b)) at mid supply, resulting in a 0.7 LSB DNL degradation. The charge-sharing ADC, when operating at 10 S/s, required an input switching power less than 16 pW ($\sim$2% of the total ADC power [88]), which was well within the sourcing capability of the potentiometric amplifier. In addition, an on-board ceramic capacitor was utilized after the potentiometric amplifier to minimize the large instant current spikes that might occur during sampling. The in-vitro test

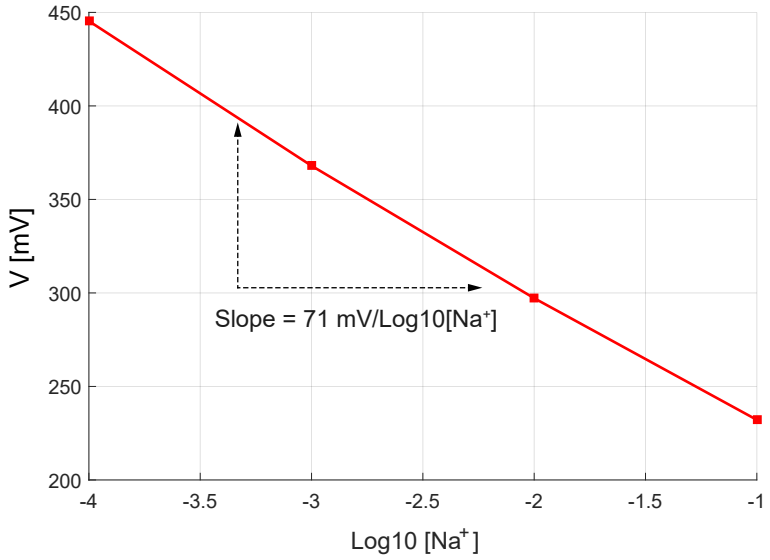


**Figure 5.22**: In-vitro measurements demonstrates that the wireless sensing platform achieves a linear response to the ion concentration.

was performed by first using pure water as background, giving ∼510 mV output as shown in Fig. 5.21. Samples with different NaCl concentrations were then dropped onto the electrode and recorded for approximately 40 seconds before additional solution was added. Note that the variation on the reference voltage shows as a common-mode voltage and thus can be rejected. On the other hand, the systematic error will affect the reference voltage for digitization in ADC and therefore effectively introduces an ADC offset error which, however, does not matter in the proposed application since, for example, as shown in Fig. 5.21, the offset error will only effectively shift the y-axis, which can be calibrated out during normal system operation. The in-vitro measurements shown in Fig. 5.21 exhibit a linear, near-Nernstian response with a response slope of 71 mV/log10[$Na^+$], as better shown in Fig. 5.22, thereby indicating the ability of the proposed system to accurately detect and wireless transmit ion concentration with only 5.5 nW of power. Note that the proposed ion sensing system can be adapted to measure other ions such as potassium, chloride, etc., by using different ionophores. A table summarizing system performance is shown in Fig. 5.23, and the die and PCB photos are shown in Fig. 5.24.

| | |
|---|---|
| **Technology** | 65 nm CMOS |
| **Chip area** | 1 mm × 1.2 mm |
| **TX frequency** | 2.37 GHz |
| **TX output power** | -64.6 dBm @ 1 m |
| **TX start-up time** | 52 ns |
| **ADC ENOB** | 8.3 bits |
| **ADC FoM** | 244 fJ/conv @10 S/s<br>7.7 fJ/conv @1 kS/s |
| **SC DC-DC eff.** | 96.8% @100 nA<br>70.5% @6.5 nA |

| **Power consumption [pW]** | |
|---|---|
| **Pot. Amp.** | 406 |
| **ADC** | 780 @ 10 S/s |
| **TX** | 500 (standby)<br>154 µW (active)<br>2.4 nW (average @ 100 bps) |
| **Oscillator** | 140 @ 10 Hz |

**Figure 5.23**: Tables summarizing chip measurement results. When operating at 10 S/s the proposed ion sensing platform consumes an average power of 5.5 nW.

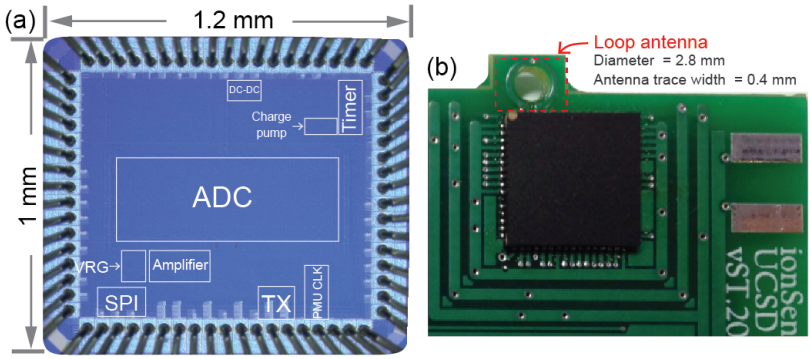


**Figure 5.24**: Die photo of the proposed ion sensing chip (a) and PCB photo (b). A loop antenna was implemented on board with a trace width of 0.4 mm and a diameter of 2.8 mm.

## 5.3 Summary

An ultra-low-power battery-connected wireless ion sensing system has been presented in this chapter. The platform comprises ISEs, a potentiometric amplifier, a reference-free charge-sharing SAR ADC with offset attenuation, a digital processing unit including a serializer and a pulse shaper, a 3:1 Dickson switched-capacitor DC-DC converter, a direct-RF power oscillator employing triode-mode switches, and low-power relaxation oscillators for clock generation. Measurements reveal a total system power consumption of 5.5 nW, resulting in the lowest power wireless ion sensing system to date. In-vitro testing shows a near-Nernstian response to varying $Na^+$ concentrations, indicating the ability of the proposed system to accurately detect and wireless transmit ion concentration at near-zero power levels.

The text of Chapter 5, in part, is a reprint of the material as it appears in "A 5.5nW Battery-Powered Wireless Ion Sensing System" by Hui Wang, Xiaoyang Wang, Jiwoong Park, Abbas Barfidokht, Joseph Wang, and Patrick Mercier, in Proc. IEEE European Solid-State Circuits Conference (ESSCIRC), Sep. 2017, and "A Battery-Powered Wireless Ion Sensing System Consuming 5.5 nW of Average Power," by Hui Wang, Xiaoyang Wang, Abbas Barfidokht, Jiwoong Park, Joseph Wang, and Patrick Mercier, IEEE Journal of Solid-State Circuits (JSSC) (In press). The dissertation author was the primary investigator and author of this paper.

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