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LOW COST PULSE SHAPER FOR USE WITH SILICON PIN DIODES

M. Ciric, J. Friese, H. J. Körner (Technische Universität München) M. R. Maier (Lawrence Berkeley Laboratory)

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LOW COST PULSE SHAPER FOR USE WITH SILICON PIN DIODES

M. Ciric, J. Friese, H. J. Körner (Technische Universität München) M. R. Maier (Lawrence Berkeley Laboratory)

ABSTRACT

We have developed a flexible, small and low cost analog pulse shaper and amplifier circuit for Silicon PIN photodiode detectors. The shaping amplifier produces both a "fast" negative output signal with less than 10 ns rise time for timing measurements and a "slow" positive output signal with peaking times from 500 ns to 10 μ s for energy measurements. The gain for the two signals can be set independently. The maximum output amplitude for the fast signal is -1.5V and +10V for the slow signal. The resolutions for the energy channel was <10 keV electronic contribution giving a total of 17 keV with α particles. The resolution for the timing channel was < 1ns electronics with a total of 2 ns with α particles. The price is \$200 per channel. The whole circuit fits on a board of 7.5 cm x 3.5 cm.

INTRODUCTION

Since low cost silicon PIN diodes have become widely used as charged particle detectors, one of the remaining high cost items has been the analog signal processing electronics. For detector setups of $N \ge 100$ channels in nuclear physics applications commercial shaping amplifiers are too expensive, as they have many features making them universal. Pulse processing electronics developed for high energy physics experiments, on the other hand, are devoted to very specific experimental requirements and do not have any flexibility in gain adjustment, shaping time variation etc. Although they are quite inexpensive, they are in general not well suited for high energy heavy ion experiments.

We have therefore developed a flexible, small, and low cost analog pulse amplifier for silicon Plin photodiode detectors. The amplifier produces both, a "fast" negative output signal with a rise time = ≤ 10 ns for timing requirements, and a "slow" positive output pulse for energy measurements. The peaking times of the "slow" signal are adjustable within 0.5 µsec $\leq t_p \leq 10$ µsec. The gain can be varied for both signals independently. The maximum output amplitude for the "fast" signal is U = 1.5 V and U = +10 V for the slow one, both channels terminated by a series resistor R = 50 Ω . The whole circuitry fits on a board of 7.5 cm x 3.3 cm (Fig. 1).





ELECTRONICS

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The board holds a charge sensitive preamplifier using two stages. (1) This design allows to take out a fast "loop error" signal in addition to the slow charge signal. This "loop error" signal is amplified and used as a fast signal for timing. The slow signal gain is determined by the RC feedback combination.

After proper differentiation this signal is passed through a four-pole active filter using a dual operational amplifier and a line driver. The time constants can be varied to produce output pulses with peaking times ranging from 0.5μ s (using a fast dual operational amplifier like the AD827) to >10 μ s (using the AD746).

DESIGN



Fig. 2. Preamplifier Schematic

The preamplifier (Fig. 2) uses a FET at the input, which should be matched to the detector capacitance. We are using the InterFET NJ903 for large (>300pF) and the NJ450 for moderate (~50pF) detector capacitances. The FET drain feeds the emitter of a cascode npn transistor. whose base potential determines the operating voltage of the FET. The operating current of the FET is determined by the 100Ω resistor in the collector of the cascode npn. The voltage level there is determined by the voltage applied to the base of the pnp transistor in the complementary differential amplifier. The collector of the npn transistor of this pair is fed to the "fast" channel feeding the emitter of another npn transistor. Its collector drives a UHF amplifier MAR-6 through an emitter follower. The rise time is determined by the frequency response of the FET. For best timing performance a low pass filter cutting off at 30 MHZ is recommended at the output.

The collector of the PNP transistor in the complementary differential amplifier feeds a unity gain follower IC. EL2001, the load resistor is a 3mA current regulator diode. This is a standard configuration.



Fig. 3. Shaper Amplifier Schematic

The shaper (Fig. 3) differentiates the preamplifier signal with "pole zero" compensation.(2) Then follow two active low pass filter stages. The first one is a non inverting Sallen Key stage. The actual gain is set by the 6.2K resistor. However the performance of this stage starts to degrade at high gains limiting the maximum resistance at that point to 10K. The next stage is an inverting two pole integrator where the gain is determined by the 1K resistor from the first stage to the second. Again the maximum gain is limited. The shaping times are determined by the 100p 10K and 3.3K 100p RC The peaking time is combinations. approximately 4RC i.e., 4µs for the quoted RC values.

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Shorter times have to be accomplished by decreasing the 10K resistors, otherwise stray capacitance will cause problems. Also the faster response requires a faster operational amplifier as mentioned above.

RESULTS

Figure 4 shows measured pulse shapes obtained with Am241 α -particles. Figure 5 shows a spectrum of the Am242 α -particles. The energy resolution is 17KW FWHM. In experiment at SIS-GSI Darmstadt time resolutions of 150 ps FWHM have been obtained with 100 GeV Xe¹²⁹ particles traversing a silicon PIN diode.



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Fig. 5. Measured spectrum of α -particles emitted by a ²⁴¹Am source. The detector was a 1 cm₂ PIN diode. The energy resolution is $\Delta E = 17$ keV (fwhm). The structure at channel 2600 results from α -particles hitting the detector edges

The maximum usable amplification is about 200 resulting in an overall gain of 10V/MeV for shircon.

The maximum output amplitude of the slow channel is 10V in series with 50 Ω , the maximum output amplitude of the fast channel is -1.5V into 50 Ω .

CONCLUSION

We have shown that using standard modern components one can design low cost signal processing electronics for silicon detectors. We have built about 100 of these shapers for experiments at SIS-GSI Darmstadt. We have assembled these in modules containing 8 shapers. Versions with gains ranging from 2V/MeV TO 25 mV/MeV have been built and used.

In the future we intend to use a modified version of these shapers for pulse processing the signal from SISWICH detectors (3). For high rates baseline restoration will be needed.

Even further miniaturization can be achieved by using SMD technology.

ACKNOWLEDGMENT

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