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Design, Automation, and Test for Low-Power and Reliable Flexible Electronics

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Contents

Abstract

Flexible electronics are emerging as an alternative to conventional Si electronics for smart sensors, disposable RFID tags, and solar cells. By utilizing inexpensive manufacturing methods such as ink-jet printing and roll-to-roll imprinting, flexible electronics can be made on low-cost plastic films just like printing newspapers. However, the key elements of flexible electronics, thin-film transistors (TFTs), have slower operating speeds and are less reliable than their Si electronics counterparts. Furthermore, TFTs are usually mono-type – either p- or n-type – devices. Making air-stable complementary TFT circuits is very challenging or sometimes not feasible to most TFT technologies. Existing design methodologies for Si electronics, therefore, cannot be directly applied to flexible electronics. Other factors such as high supply voltage, large process variation, and lack of trustworthy device modeling also make designing larger-scale and robust TFT circuits a significant challenge.

The objective of this article is to provide an in-depth overview of flexible electronics from their applications, manufacturing processes, device characteristics, to circuit and system design solutions. We first introduce the low-cost fabrication methods for flexible electronics, including ink-jet printing, screen printing, and gravure printing. The device characteristics and compact modeling of several major TFT technologies will be illustrated. We will then give an overview of digital and analog circuit design from basic logic gates to a microprocessor, as well as design automation tools and methods, for designing flexible electronics. We also describe a reliability simulation framework that can predict TFT circuits' performance degradation under bias-stress. This framework has been validated using the amorphous-silicon (a-Si) TFT scan driver for TFT-LCD displays. Finally, we will give an overview of flexible thin-film photovoltaics using different materials including amorphous silicon, CdTe, CIGS , and organic solar cells.

1

Introduction

In 1947, Shockley, Bardeen, and Brattain invented the first transistor at Bell Labs, which opened the era of solid-state electronics. In 1958, Jack Kilby of TI invented the first integrated-circuit (IC) in which he successfully assembled several electronic components to form a miniature circuit. In 1965, Intel co-founder Gordon Moore published a paper in the Electronics magazine which predicted that the number of transistors per IC would double about every two years, later known as the Moore's Law Moore [April 19, 1965]. In 1971, Federico Faggin of Intel successfully demonstrated the world's first microprocessor, Intel 4004, running at a clock rate of 108 KHz with 2,300 transistors in a 10-μm pMOS technology. In the last 40 years, we have witnessed the tremendous impact of the IC technology that has brought to the world since its debut. The abundant computing power that comes from faster and cheaper transistors has made our world today very different from what it was 40 years ago. For the future of the semiconductor industry, the ongoing debate has been centered around questions like: "Is the Moore's law going to continue?" and "Will the rigid and disc-like silicon wafer and the printed circuit-board (PCB) continue to be the dominant ways to make electronics for future applications?"
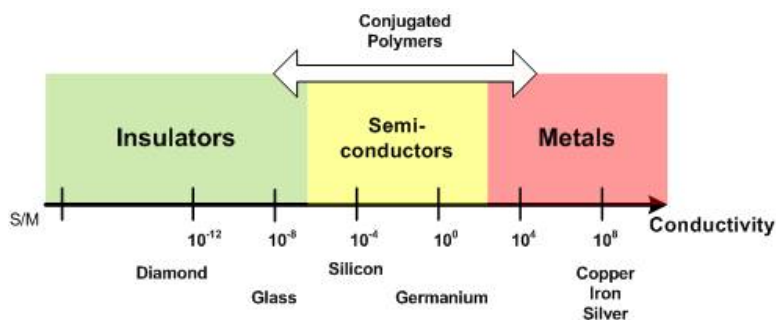
Figure 1.1: Conductivity of conjugated polymers

1.1 Plastic Electronics Revolution

In 1977, 30 years after the first transistor was invented, Heeger, MacDiarmid, and Shirakawa published their discovery of conductive polymer in Shirakawa et al. [1977] and received their Nobel Prize in Chemistry in 2000. Plastic, which is made of polymer, is usually viewed as an insulator and not conductive to electron transportation. In their discovery, however, by proper doping or oxidation, polymers can also be as conductive as metals if the conjugated chains can be properly aligned. The conductivity of polymers is shown in Figure 1.1. This discovery creates alternatives of making electronics, which is not limited to hard and rigid silicon wafers and PCBs. As of today, thousands of semiconducting materials are suitable to make flexible electronics, which brings our imagination of many sci-fi gadgets closer to reality. For example, amorphous-Si, organic and transparent metal-oxide thin-film transistors (TFTs) are considered promising candidates for flexible electronics. We will give an in-depth overview of TFTs in Chapter 3. Although the carrier mobility of organic materials is still significantly slower ($10^{-2} \sim 10^{-3}$X) than that of crystalline and poly-crystalline Si, the steady pace of improvement to their mobility has made organic digital and analog circuits feasible, which can complement to, or may eventually compete with, silicon electronics for certain applications.

1.2   Large-Area Applications

One of the key advantages of flexible electronics is its low manufacturing cost on large-area substrates. Since most organic materials can be converted to a liquid phase, which can be used as functional "inks", manufacturing organic circuits is similar to printing newspapers for which roll-to-roll or ink-jet printing can be used. An overview of the manufacturing methods will be described in Chapter 2. For these low-cost manufacturing methods, several kinds of flexible substrates, such as thin-glass, metal foil, and plastic films, can be used. The manufacturing cost per unit area can be as low as one hundredth of that of silicon electronics. On the other hand, in contrast to silicon electronics that often require sophisticated heterogeneous integration of silicon VLSI chips, discrete passive elements, and ceramic packages on rigid epoxy-resin glass fabric printed circuit boards (PCBs), flexible electronics can be made through homogeneous integration of active printed circuits, encapsulation, and thin-film ($< 100 \ \mu$m in thickness) substrates, which can be fabricated with a much simpler process and material treatment. This advantage in integration can significantly reduce manufacturing costs. Furthermore, since semiconductor materials for flexible electronics do not require high process temperature and high vacuum that are indispensable for conventional silicon electronics, the energy consumption and the material cost of fabricating flexible electronics are much lower than those for silicon electronics. Sakurai(2007) shows a comparison of cost per unit area between organic and silicon VLSIs indicating that the manufacturing cost of organic ICs is only one hundredth of silicon VLSIs for a 10cm by 10cm area and it can be even lower for high-volume production.

 The low manufacturing cost on large-area flexible substrates enables many applications that are not economically practical or mechanically infeasible with conventional silicon electronics. Figure 1.2 shows several applications of flexible electronics, ranging from low-cost RFID tags, flexible displays, artificial skins for robotics, solar cells, to large-area wireless power-sheets. Instead of using multi-billion-dollar foundries for fabrication, electronics for these applications can be mass-produced
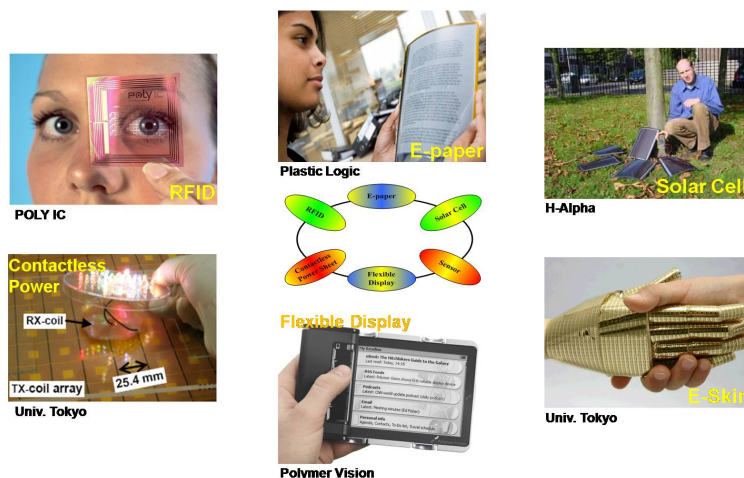
Figure 1.2: Typical applications of flexible electronics

on large-area flexible substrates using simple printing facilities. This is particularly advantageous for those applications that require fast prototyping, demand customization, or have a small volume such as wearable sensors, disposable biochemical testers as well as personalized healthcare devices. With low capital investment and high flexibility in configuring printing facilities, the manufacturers will be able to easily adjust their production lines as simple as changing the printed contents and quickly deliver new electronic products to meet fast-changing tastes of the consumers.

1.3 Differences from Silicon Electronics

Thin-film transistors (TFTs), the key elements of flexible electronics, can be fabricated using simple process steps (usually less than 5 masks) at a low process temperature on inexpensive flexible substrates such as Polyethylene Terephthalate (PET) plastic films, which help lower the manufacturing costs. An overview of TFT technologies will be described in Chapter 3. Compared with MOSFETs, printed TFTs have larger feature sizes ($\sim 10^3$X) due to their low-cost printing processes, which inevitably introduce larger layout-dependent parasitic resistance and
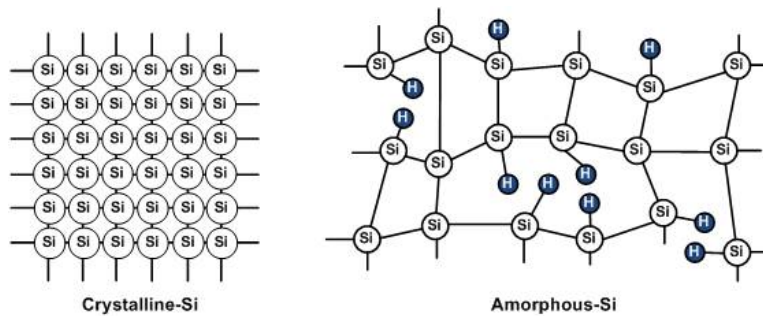
Figure 1.3: Atomic structure of single crystalline-Si and amorphous-Si
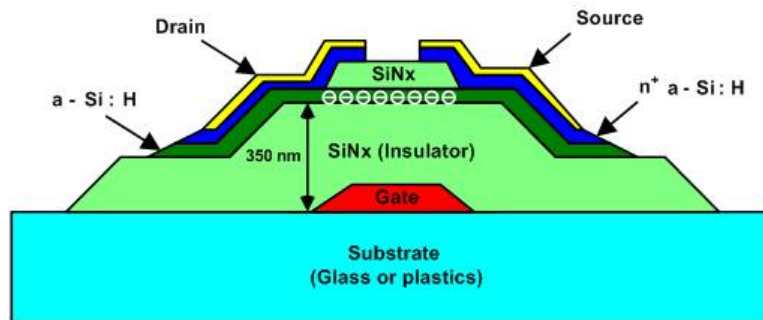
Figure 1.4: Device structure of a hydrogenated amorphous silicon (a-Si:H) TFT. (The white circles show that the high density of defects can trap carriers near the semiconductor and insulator interface).

capacitance and therefore limit their operating speeds. On the other hand, although low process temperature can reduce the manufacturing cost and energy consumption, semiconductor materials made with this low process temperature are usually amorphous and have many dangling bonds as illustrated in Figure 1.3. This amorphous atomic structure limits the carrier mobility and causes reliability concerns during the operation because the carriers could be trapped in the dangling bonds and alter the device properties.

1.4 Challenges for Circuit and System Design

In addition to the reliability concerns, the high supply voltage ($> 20V$) and mono-type device (only either p- or n-type, but not both, is available) also make designing low-power TFT circuits a challenging task. Figure 1.4 shows a typical device structure of a-Si:H TFT, in which the gate insulator material is hundreds-nanometer thick amorphous silicon-nitride (a-SiNx). The a-SiNx material has many advantages in manufacturing such as low process temperature, high uniformity across a large area with plasma-enhanced chemical-vapor-deposition (PECVD), and a relatively high dielectric constant ($\epsilon_r \sim 7$). In order to suppress the gate leakage problem, however, the a-SiNx layer needs to be kept sufficiently thick due to its inferior quality to the thermally-grown SiO_2 gate insulator in Si-MOSFET. As a result, a high supply voltage is required. On the other hand, unlike Si-MOSFET, in which the device-type (p- or n-type) can be determined by doping either p-type (ex. Boron) or n-type (ex. Phosphorus) materials into intrinsic Si, the device-type of TFTs is determined by the majority carrier of the material. For instance, a-Si:H and metal-oxide materials (ex. InGaZnO and ZnO) are n-type, in which the majority carrier is the electron, while most organic materials, including small-molecule and polymer, are p-type and their major carrier is the electron hole. With only mono-type TFTs, the widely-used CMOS design cannot be directly applied to TFT circuit design. This attribute causes many challenges in circuit design for achieving high noise margin and low leakage power which are required for large-scale circuits.

Furthermore, unlike mature single crystalline-Si manufacturing of which the process variation is well-controlled (often less than 5%), process variation of flexible electronics using these low-cost manufacturing methods is very significant. This adds extra challenges for designing flexible circuits and a fabricated circuit could have substantial deviation from its target performance. Other factors such as the process-temperature dependent dimension deformation (ex. shrinking or expanding) of flexible substrates and environmental instability (ex. chemical degradation due to moisture or oxygen contents in the ambient air)

also make realizing a robust flexible circuit a very challenging task.

For flexible electronics applications, system-level solutions to build a reliable system based on unreliable devices are equally important to, if not more important than, device- and circuit-level solutions. For example, a system-level solution to electronic textiles (*e*-textiles) was proposed in Park et al. [2002], Marculescu et al. [2003], Stanley-Marbell et al. [2003]. *E*-textiles are computational fabrics that form a large-area, flexible, and conformable information system for both consumer electronics and aerospace/military applications. A *Model of Colloidal Computing* Marculescu and Marculescu [2002] is introduced to provide mechanisms for extracting useful work out of the unreliable elements. Two techniques, *code migration* and *remote execution*, are proposed to provide feasible means of adapting to failures in the presence of redundancy Marculescu et al. [2003], Stanley-Marbell et al. [2003].

1.5   Summary

With rapid advances of flexible semiconducting materials, the performance of TFT circuits has been improving significantly and the concerns of their ambient stability have been alleviated to a great extent in the past few years. After a brief introduction to flexible electronics, this chapter highlights its key difference from silicon electronics, and the challenges and opportunities of circuit design for emerging applications such as wearable electronics, personalized healthcare, and flexible displays. While the main objective of this overview article is on the design, EDA and test issues, we also offer brief technical reviews on TFT technologies, manufacturing methods, and flexible photovoltaics for the purpose of providing a more comprehensive introduction of this emerging field.

2

Manufacturing Methods for Large-Area Flexible Electronics

To realize inexpensive printed circuits on large-area flexible substrates, many patterning techniques that were used to print newspaper can also be good candidates to deposit the functional material (ex. liquid-phase organic semiconductor) onto flexible substrates to pattern desired features. Most of these patterning/printing methods can be used under the room temperature without any vacuum chamber required. To successfully apply these printing techniques for flexible electronics, however, many details in ink preparation such as ink viscosity and surface tension play critical roles in the final quality of the printed circuits. However, discussions of such issues are beyond the scope of this article. In this chapter, we give a brief overview of three different printing methods that are considered promising and suitable for mass-production of large-area flexible electronic circuits.
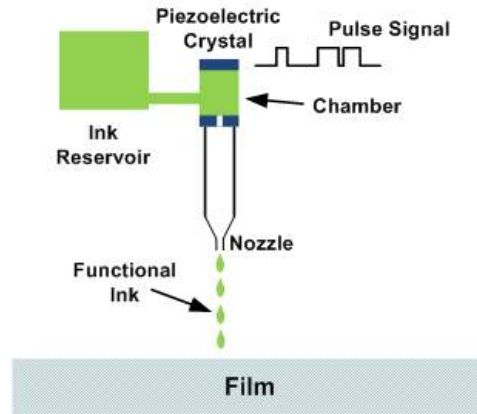
Figure 2.1: The drop-on-demand (DOD) ink-jet printing system

2.1   Ink-Jet Printing

2.1.1   Principle of Operation

An ink-jet printing system used to make flexible electronics is essentially the same as an ink-jet printer used for paper-printing at home or office. The industrial material ink-jet printer today can achieve the precision of and the droplet size of 1 pico-liter(pl). The typical specifications of an industrial-level material printing system is listed in Table 2.1. Similar to a paper-printing ink-jet printer, the material ink-jet printing system is connected to a computer that controls the printer head to move around according to pre-defined patterns. Figure 2.1 shows the typical setting of an ink-jet printing system. There are a wide variety of applicable "inks", ranging from many water-based solvents to liquid-phase gold or silver-nanoparticles that can form the interconnects after a drying process. The piezo-electric crystal (PZT) is a material that can expand or contract depending on the electric potential applied on PZT. In the "droplet-on-demand (DOD)" ink-jet printing system, the droplet can be produced by applying electric pulses to PZT, which will then expand or contract to eject the ink from the chamber through the nozzle hole. The electric pulses are generated

Table 2.1: Typical specifications of a material ink-jet printing system Fujifilm [2008]

Ink-Jet Printing System	Specifications
System footprint (mm)	650 x 600 x 400
Printable area (mm)	200 x 320
Operation temperature (°C)	ambient ~ 60
Cartridge capacity (ml)	1.5
Number of nozzles	128 (max.)
Diameter of nozzle (μm)	20
Droplet size (pl)	1 (min.)
Precision (μm)	± 25
Throughput (μl/s)	5

from the computer; therefore, changing the deposited patterns is similar to printing different contents with the paper-printing ink-jet printers. Depending on the hydrophilic property of the substrates and the evaporation rate of the solvents, the deposited patterns will be slightly different from each other. To increase the throughput of an ink-jet printing system, more than one nozzles can operate simultaneously to reduce the printing time. For instance, an industrial ink-jet printing system that is used to produce the color-filters for the TFT-LCD displays has 128 nozzles working together with a precision as high as tens of micro-meters.

2.1.2   Advantages

Additive Process

Ink-jet printing is an "additive" process, which is different from the "subtracting" process used in silicon electronics manufacturing. For instance, spin-coating is a common technique to deposit the material (ex. photo-resist) on the top of the silicon wafer with good uniformity. During this process, however, only 5% of the material is left on the wafer and 95% of the material is wasted, which inevitably causes the water pollution problem. On the other hand, the ink-jet printing system only

deposit a required amount of materials at each target location and the process leaves more than 95% of the materials on the substrates. Such a process not only reduces the manufacturing cost, but also is more environmental friendly.

Flexibility

By changing the "inks" in the cartridge, we can deposit virtually any materials required to make flexible circuits. Together with the precision-control on the printed patterns from the computer, every single circuit can be made different from each other if an unique bit-map file is applied. Therefore, it is very suitable for one-time use or for disposable applications such as tickets or a biological tester, which also can be made recyclable after use if we can wash away the deposited patterns.

Surface Compatibility

Since the substrates used in this ink-jet printing system do not have interaction with the deposited materials, the applicable substrates can virtually be any surfaces such as low-cost plastics or papers. On the other hand, the printable area can be as small as a business card or as large as a poster. This means that for the same printing system, we can produce a wide variety of circuit or substrate combinations for various applications and obtain a similar printing quality.

Scalability to Mass-Production

For an ink-jet printing system, the more nozzles it has, the faster it can produce the printed circuits. As long as the desired pattern for printing can be divided into independent segments, multiple nozzles can deposit simultaneously to complete the desired pattern collaboratively. Furthermore, if different nozzles are linked to different ink cartridges, then different types of inks can be deposited simultaneously at different locations or even mixed together if multiple nozzles deposit inks at

the same location. Therefore, the ink-jet printing system has a good scalability from a laboratory use to mass-production such as the color-filter manufacturing in TFT-LCD business.

2.1.3 Disadvantages

Cross-Contamination

Since the ink-jetted materials are in the liquid-phase, the materials compatibility between different layers becomes critical to ink-jetted TFT performance. Special care should be taken in order to avoid the chemical reaction between the deposited and subsequent materials. The quality of interface between different functional layers of the TFTs will directly affect the reliability and performance. This could also result in degraded performance (ex. carrier mobility μ) in ink-jetted TFTs.

Via-Less Process

In modern VLSI, vias are used to connect different layers of metal wires vertically. To make a via in printed electronics, a material that can etch through the insulating layer without damaging the other layers would be required. By additively ink-jetting the conductive material in a well-controlled manner, a VIA sized by tens of micro-meter in diameter can be created for vertical connection between differen layers. Or alternatively we can use a CO_2 laser to drill through the insulating layer for vias. A via made with these methods, unfortunately, has a poor quality (ex. high resistivity) and a large size. Therefore, it is very challenging to make complex circuits that require many layers of vias.

Coffee-Ring Effect

The so called "coffee-ring" can be observed in a drying droplet. Instead of leaving a uniform spot, a drying droplet will leave a ring of the solute of deposits on the surface. This phenomenon is known due to the Marangoni flow Hu and G. [2006]. This coffee-ring effect makes
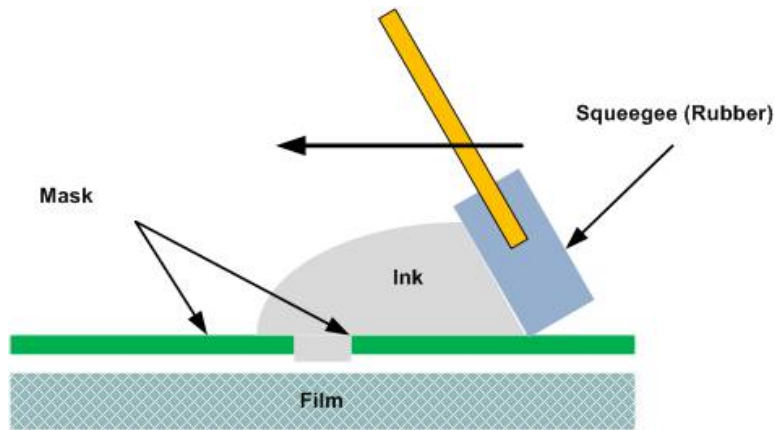
Figure 2.2: A schematic cross-section view of screen printing process

the deposited materials such as conductive polymers non-uniform and leaves uneven edges to subsequent ink-jetted materials. Therefore, the ink-jetted pattern must be carefully designed to make it smooth and straight to avoid non-uniformity due to the coffee-ring effect.

2.2 Screen Printing

2.2.1 Principle of Operation

Figure 2.2 shows the screen printing process that utilizes a "screen" as the mask to define the desired patterns for the material deposition. There are three elements in a screen printing process including: 1) a screen, 2) a squeegee, and 3) the ink. The screen is used to carry the image to the substrate. The squeegee is usually made from polyurethane compound and is used to generate necessary hydrodynamic pressure to transfer the ink flow through the screen. The ink is deposited on the upper surface of the screen before the printing process. During the printing process, the screen is held slightly above the substrates as shown in Figure 2.2, which is known as the *off contact gap* Claypole [2004]. To print, the squeegee blade is brought down forcing the screen into contact with the substrate. The movement of the squeegee
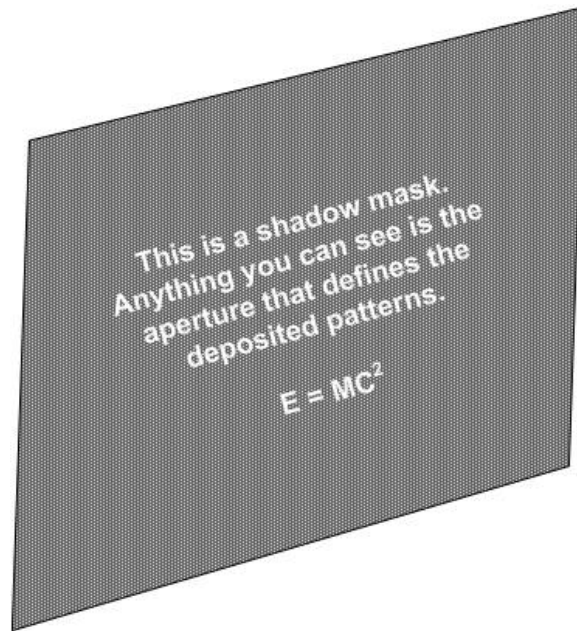
Figure 2.3: A shadow mask for material deposition

over the screen surface forces the ink through the screen onto the substrates. At the end of the printing process, the squeegee blade is raised and returned to its starting position. This technique has been used in manufacturing printed wiring boards (PWBs) for electronic components. A typical shadow mask made of metal foil to define the desired patterns of deposition is shown in Figure 2.3.

2.2.2 Advantages

Flexibility

The biggest advantage of the screen printing is the flexibility of the process. The screen printing method can be used from a low volume laboratory samples to a high volume industrial production under the clean room conditions. Depending on the resolution of the screen, the screen printing can be used to print the desired patterns down to a

micrometer range. The ink films can also range from sub-micrometer to hundreds of micrometer thick.

Wide Range of Printable Inks

Unlike other printing techniques that have certain criteria for printable inks, the ink that can be used in the screen printing process has a wide range of viscosity, from 0.5 to 50 poise, compared with 0.01 to 0.012 poise for ink-jet printing (a larger number means more viscous). Therefore, most functional material inks can be used in screen printing with various resolutions and throughput, depending on the screen resolution and ink-viscosity.

2.2.3 Disadvantages

Solvent Absorption

Since most squeegees are made from polyurethane compound, it is possible that when the surface of the squeegee is abraded, the organic ink materials can diffuse into the squeegee. This can cause the hardening or softening of the squeegee and affect the printing quality. This problem can be addressed by utilizing a more chemically-resistant polyurethane compound to make the squeegee.

Squeegee Bending

Since the squeegee is used to force the ink flow onto the substrates, the rigidity of the squeegee must be able to withstand the hydrodynamic and drag forces imposed on the squeegee. On the other hand, the squeegee must also be sufficiently compliant to absorb the stresses created by the substrates and the screen surface roughness. If excess force is applied to the squeegee, the tip of the squeegee will deform and result in a change in the hydrodynamic pressure and hence ink transfer Claypole [2004]. Various squeegee designs have been developed to enhance the robustness of the squeegee tip for less process variations.
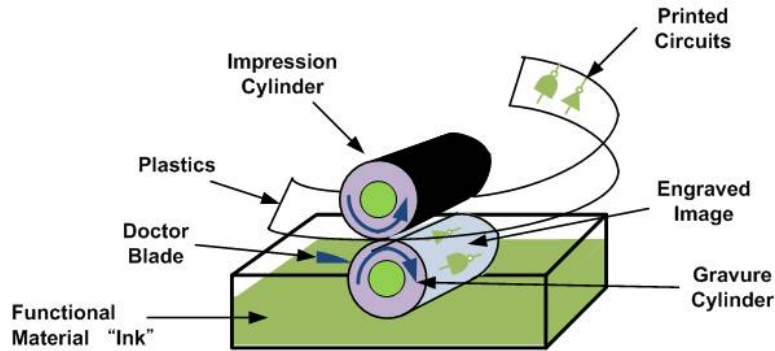
Figure 2.4: A typical gravure printing unit

2.3 Gravure Printing

2.3.1 Principle of Operation

The gravure printing system is comprised of an engraved metal image carrier (an engraved cylinder), a rubber covered impression cylinder, a sharp blade called "doctor blade", and an ink tank.

The system setting is shown as in Figure 2.4. The engraved cylinder is wetted with the ink and the desired pattern or image can be transferred onto the substrate (ex. plastics) by pressing the substrate against the impression cylinder. Before physical impressing, the doctor blade wipes out excess inks from the engraved cylinder and leaves only inks in the recessed image that will then be transferred as desired patterns on the substrates. Since the gravure printing process is more robust compared with other printing processes and can have a very high throughput, it has been widely used in printing magazines, stamps, and folding cartons, etc. The ways to engrave cylinders to create desired patterns/images include: 1) chemical etching, 2) electromechanical engraving, and 3) laser engraving. Among these engraving methods, electromechanical engraving is the most commonly used and the laser engraving has the fastest engraving speed ($\sim$10X) of any other engraving methods.

Table 2.2: Typical specifications of a gravure printing system Brollier [2004]

Gravure Printing	Specifications
Film thickness (μm)	30
Minimum line resolution (μm)	50 (typical)
Ink viscosity (Pa.s)	$0.05 \sim 0.20$
Substrates	Paper, board, plastics
Speed (fpm)	Up to 3,000
Cost of gravure press (USD)	$> \$150,000$
Cost of gravure cylinder (USD)	$\$1,000 \sim \$10,000$
Typical registration tolerances (μm)	± 50

2.3.2 Advantages

Consistency and High Quality

Since the gravure printing process is accomplished in a fashion that only the cylinder rotation is the required movement, the printing quality can be easily controlled and the consistency can also be guaranteed. This advantage makes gravure printing robust to variations in surface roughness and ink viscosity and is suitable for mass production.

High Throughput

Table 2.2 shows the typical specifications of a gravure printing system. The speed of printing can be up to 3,000 films per minute (fpm), compared with a single digit for an ink-jet printing system ($\sim 5 fpm$).

2.3.3 Disadvantages

High Capital Investment

As shown in Table 2.2, the capital investment for an industrial-level gravure printing press is high. To fill each ink reservoir for a larger gravure printing unit requires 20-30 gallons of inks. For expensive ma-

terials, this will be a considerable amount of costs. In addition to the ink cost, the cost of engraving cylinders is not cheap ($> \$1,000$) which will be a significant factor for applications that require frequent updates of the contents.

Inflexibility

The gravure printing can only be used in high-volume printing because the preparation process before printing such as ink-filling, cylinder engraving, and substrate registration incurs a considerable amount of time and cost. Therefore, gravure printing is not suitable for experimental samples that usually will require frequent changes of the inks and engraved images.

Difficulty in Large-Area Printing

For printing a larger-size image/pattern onto the substrate, the cylinder must be engraved accordingly. The current engraving techniques such as chemical etching and electromechanical engraving, however, are unable to make a large-size image while maintaining the resolution. These patterns, therefore, must be divided into smaller cells and assembled later when applied to the engraving cylinder. These assembled patterns, unfortunately, are usually not continuous. This is fine if only a coarse resolution is required such as wiring in a printed circuit. To print a fine structure of transistors, however, the un-even edges and not-so-straight lines could induce large variations among transistors.

Cross-Contamination

Since the printing of transistors requires many layers that are comprised of several different functional layers, the same substrate will then pass through several different gravure printing units in which the inks are different. During the printing process, the substrates and the engraving cylinders will have physical contact and one functional material is likely to be carried through this mechanism to another ink

reservoir. This causes the cross-contamination problem between different ink reservoirs. If the purity of the materials affects the performance of the transistors, such as organic semiconducting materials, then this cross-contamination can cause detrimental effects to the manufactured transistors.

2.4   Summary

This chapter introduces three types of low-cost patterning methods on large-area flexible substrates. Each of these methods has its advantages and limitations, and thus the best choice depends on the target applications. For rapid prototyping of early-stage products or laboratory samples, ink-jet printing and screen printing are viable solutions with the advantages of low-cost and flexibility. For mass production, ink-jet printing is limited by the number of nozzles that can work collaboratively, which in turn limits its throughput to a single digit of films per minute (fpm). Screen printing can achieve a greater throughput but the pattern resolution is usually limited by the shadow mask. It is challenging to make fine features (<10 μm) with screen printing. On the other hand, gravure printing can achieve a much greater throughput (ex. >1000 fpm) but with little flexibility for minor adjustment. It is therefore most suitable for mass-production of high-volume products such as RFID tags and flexible displays.

3

Thin-Film Transistors

Thin-film transistors (TFTs) first appeared in 1960s Weimer [1962] and competed with the single crystalline-Si MOSFET. Due to the rapid advancement in MOSFET and the difficulty in consistently producing high-quality TFTs, TFTs were not a serious contender for integrated circuits at that time. However, the research on TFTs for displays was never stopped. With tremendous improvement of large-area manufacturing of TFTs in 1980s and 1990s, the hydrogenated amorphous silicon (a-Si:H) TFTs began to be widely used for mass-producing the pixels of liquid-crystal (LC) displays Luo [1981], Matsuura et al. [1982]. Besides a-Si:H TFTs, research on various kinds of TFTs has revived recently because of the strong demand on thin-film, low-cost and flexible applications in consumer electronics. With the advancement of organic materials and printing technologies, low-cost large-area printing techniques as stated in Chapter 2 can be used to manufacture TFTs as alternatives to the standard clean-room manufacturing. The key features of major types of TFTs are revisited in Table 3.1.

Table 3.1: Comparison between different TFT technologies

Device type (TFT)	a-Si:H	Metal-Oxide	Organic
Process temperature	$\sim 200°C$	$\sim 150°C$	Room temp.
Process technology	lithography	roll-to-roll(r2r)	r2r & ink-jet
Minimum size (μm)	10	8	50
Substrates	glass/plastics	wafer/plastics	wafer/plastics
Device type	N-type	N-type	P-type
Supply voltage (V)	20	20	40
Mobility (cm^2/Vs)	1	10	0.5

3.1 Hydrogenated Amorphous Silicon (a-Si:H) TFT

The device structure of a-Si:H TFTs is shown in Figure 3.1. The gate is located at the bottom because of the consideration of structural compatibility for TFT-LCD displays. The a-Si:H TFT behaves as a parallel plate capacitor in which the carriers (electrons) are accumulated by applying positive gate voltage V_{GS} to the gate terminal. The conduction current between source and drain metals is dependent of the applied gate voltage V_{GS}. Since the negative charges are accumulated close to the gate terminal (at the bottom side of a-Si:H layer), the carriers need to flow through the vertical thickness of the a-Si:H layer to form a conduction channel between source and drain terminals. This inevitably increases the channel resistance and lowers the conduction current, in comparison with the crystalline MOSFET. Figure 3.2 Servati and Nathan [2002] shows a typical relationship between the drain current (I_D) in the log scale and the applied gate voltage (V_{GS}).

For the gate dielectrics, since the high process temperature to grow a good quality SiO_2 layer exceeds the glass transition temperature T_g, the gate dielectric layer (SiN_x) is usually deposited using plasma-enhanced chemical-vapor-deposition (PECVD). This dielectric layer has many defects that can trap charges particularly near the interface between the a-Si:H and SiNx layers, which causes the reliability concerns that will be discussed in a later section.
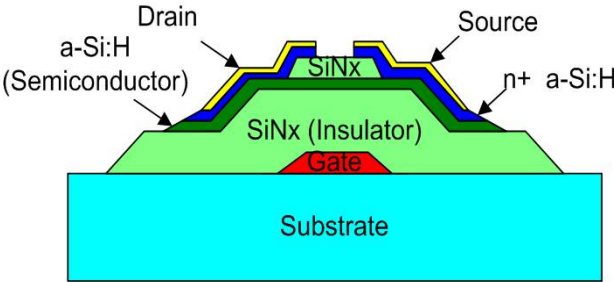
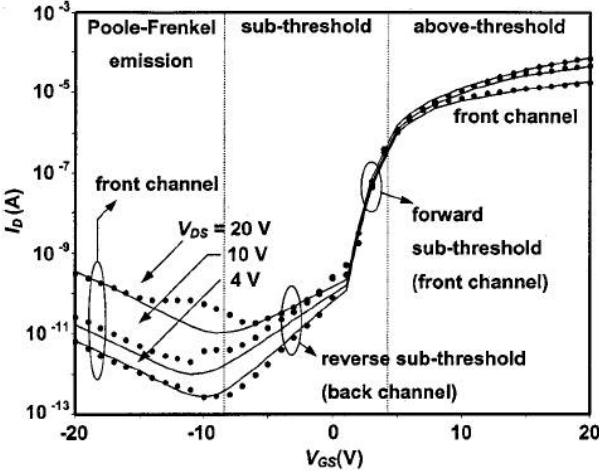**Figure 3.1:** A typical bottom gate structure of a-Si:H TFTs

Figure 3.2: Log-scale plot of drain current versus gate voltage Servati and Nathan [2002]

3.1.1   Device Basics

3.1.2   Device Manufacturing

Figure 3.3 shows a 5-mask fabrication process of a typical bottom gate a-Si:H TFT. Mask 1 is used to define the gate metal made of tungsten molybdate (MoW) . After the gate metal deposition, the insulator (SiNx) is then deposited using plasma-enhanced chemical-vapor-deposition (PEVCD) because of its fast deposition speed and no requirement for high vacuum and process temperature. SiNx is also a passivation material that is not active to many chemical solvents used in the process. The semiconductor a-Si:H is then deposited using mask 2 on top of the insulator SiNx layer and then the heavily doped n-type a-Si:H layer with PECVD. The purpose of this heavily doped a-Si:H layer to form an ohmic contact between the semiconductor a-Si:H layer and the source/drain contacts. The source/drain metal layer made of Al-Nd is deposited using mask 3. Finally SiNx is deposited again on top of the source/drain metal layer as a protection layer. For driving display pixels, another layer of transparent metal made of Indium-Tin-Oxide (ITO) will be deposited as the last layer using mask 5. The details of TFT-LCD displays manufacturing can be found elsewhere (ex. Kagan and Andry [2003], Kuo [2004], Tai [2006]).

3.1.3   Device Modeling

The drain-source current I_{DS} of a-Si:H TFTs can be recognized to have four regimes depending on the bias: above threshold, forward sub-threshold, reverse subthreshold, and front subthreshold (Poole-Frenkel) as shown in Figure 3.2. The details of these different operation regimes can be found in Servati and Nathan [2002]. In the above-threshold regime, when $V_{DS} < \alpha_{sat}(V_{GS} - V_{TH})$, the TFT operates in the linear region, in which I_{DS} depends on the both V_{GS} and V_{DS}. On the other hand, when $V_{DS} \geq \alpha_{sat}(V_{GS} - V_{TH})$, the TFT operates in the saturation region in which the mobile carriers at the drain side of the channel reduces to zero (the pinch-off condition). The equation for above-
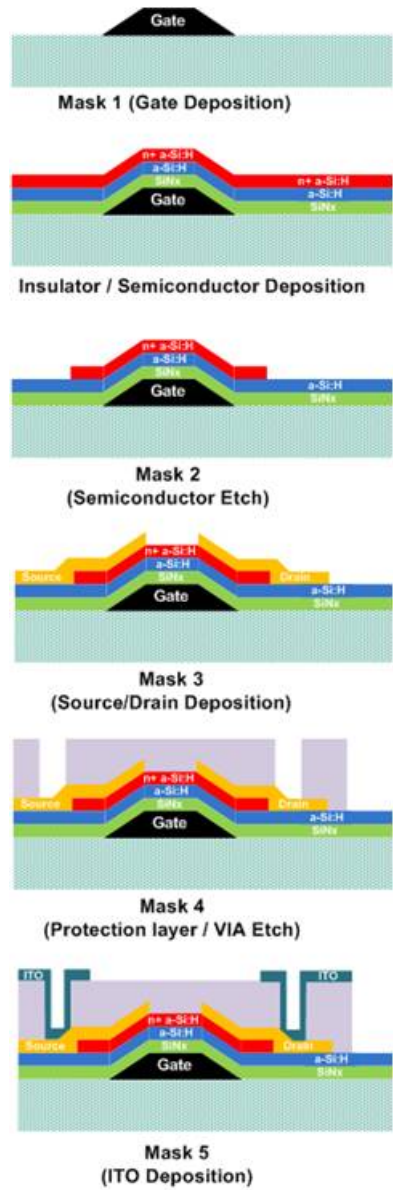
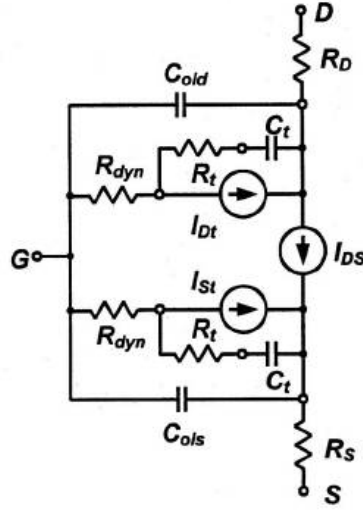**Figure 3.3:** A typical 5-mask fabrication steps of a-Si:H TFTs

Figure 3.4: An equivalent model for a-Si:H TFTs Servati and Nathan [2002]

threshold linear and saturation regions can be found in Equations 3.1 and 3.2. A complete a-Si:H TFT model for both static and dynamic characteristics is shown in Figure 3.4. In this model, R_S and R_D are used to model the contact resistance of S/D contacts and the series resistance of the conduction channel. Other capacitance and resistance are responsible for a-Si:H TFT's dynamic characteristics.

$$I_{DS} = \left\{ \mu_{FET} C_i \frac{W}{L} \left(V_{GS} - V_{TH} - \frac{V_{DS}}{2\alpha_{sat}} \right) \cdot V_{DS} \right\} \qquad (3.1)$$

$$when \ \ V_{DS} < \alpha_{sat}(V_{GS} - V_{TH})$$

$$I_{DS} = \left\{ \mu_{FET} C_i \frac{W}{L} \left(V_{GS} - V_{TH} \right)^2 \cdot \frac{\alpha_{sat}}{2} \right\} \qquad (3.2)$$

$$when \ \ V_{DS} \geq \alpha_{sat}(V_{GS} - V_{TH})$$

where μ_{FET} is the field effect mobility, C_i is the gate insulator capacitance per unit area, V_{TH} is the threshold voltage, and α_{sat} is the saturation parameter, typically $\alpha < 1$.

3.1.4 Degradation Mechanism

Unlike crystalline-Si MOSFETs, a-Si:H TFTs exhibit a bias-induced metastability phenomenon that causes both threshold voltage (V_{TH}) and subthreshold slope (S.S.) to change over time Powell [1983], Jackson and Moyer [1987]. There are two mechanisms that are responsible for this electrical instability. First is carrier trapping in the gate insulator SiNx layer. This is due to the high density of defects of the PECVD-grown SiNx layer in which the charges are easily trapped when the gate undergoes a bias-stress. The charges are initially trapped within the interfacial states at the a-Si:H/a-SiNx:H boundary and then thermalize to deeper energy states inside the insulator layer. Another mechanism responsible for this electrical instability is point defect creation in the a-Si:H layer or at the a-Si:H/a-SiNx:H interfaces. The defects are created when weak silicon-silicon bonds break into silicon dangling bonds in the presence of a bias-stress. This phenomenon is similar to photo-generated carriers that result in dangling-bond creations Kuo [2004], Stutzmann et al. [1985]. Both mechanisms cause a positive shift in the threshold voltage (ΔV_{TH}). The charge-trapping mechanism manifests itself in high gate bias-voltages and long stress times while defect state creation happens at lower stress voltages and shorter stress time.

3.2 Ink-Jetted Organic TFT

3.2.1 Device Basics

The device structures of an organic TFT (OTFT) have several variants as shown in Figure 3.5. Because the organic semiconducting material is much more fragile than the insulating material, it is easier to deposit the semiconductor layer on top of the insulator layer than the converse Klauk [2006]. In the bottom contact structure, the S/D contacts are deposited on top of the insulator. Since the conduction channel is formed at the bottom side of the semiconductor layer, which is closer to the S/D contacts, the contact resistance is usually less than the that of top contact structure as shown in Figure 3.5. On the other hand, in
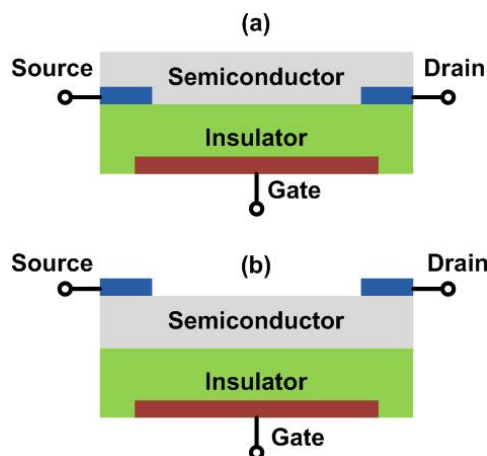
Figure 3.5: A schematic view of the structure of organic TFTs. (a)Bottom Contact; (b)Top Contact.

the top contact structure, the S/D contacts are deposited on top of the semiconductor layer, which inevitably causes larger contact resistance between the source and drain terminals. The merit of this structure is a cleaner interface between the organic semiconductor layer and the insulator layer, which helps improve the alignment of the organic molecules of the semiconductor layer for better conductivity and carrier mobility.

Many low-cost printing methods such as ink-jet printing can be used to fabricate organic TFTs. The device structure of an ink-jetted organic TFT (OTFT) is shown in Figure 3.6. The typical drain current I_{DS} versus gate voltages of an ink-jetted organic TFT (OTFT) can be found in Figure 3.7 and the I_{DS} versus drain voltages plot is also shown in Figure 3.8. Although the charge transport mechanism of organic TFTs is still under active research, a popular model has been proposed by Vissenberg and Matters Vissenberg and Matters [1998]. They assume that the variable range hopping in an exponential distribution of traps is the major mechanism of charge transport in the organic semiconductor. This model explains the well-known mobility dependence on the gate voltages for organic TFTs. When the gate voltage increases, the injected charge-carriers fill more traps in the semiconductor that makes the charge-trapping less efficient and improves the charge transport.

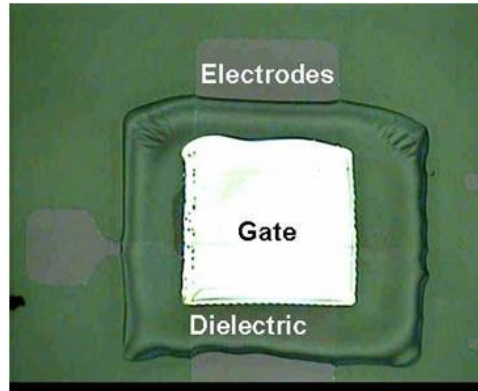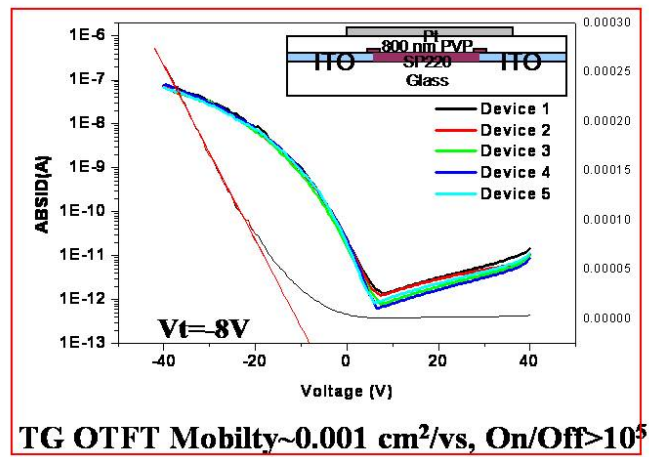**Figure 3.6:** A device photo of an ink-jetted OTFT (photo courtesy of ITRI-FETD)

Figure 3.7: A log scale plot of drain current I_{DS} versus gate voltage V_{GS} of a ink-jetted OTFT. In this figure top-gate structure is used. Pt is for GATE contact and ITO is for SOURCE and DRAIN metal contacts. SP220 is a commercially available organic semiconducting material. (courtesy of ITRI-FETD)
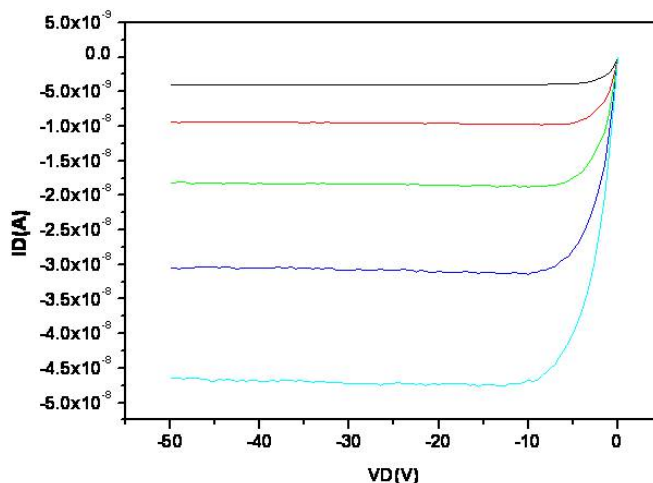
Figure 3.8: A linear scale plot of drain current I_{DS} versus drain-source voltage V_{DS} of a ink-jetted OTFT (courtesy of ITRI-FETD)

3.2.2   Device Manufacturing

Ink-jet printing is considered as a promising candidate for manufacturing organic TFTs and has been used for making organic light-emitting diodes (OLEDs) Hebner et al. [1998] and full-color displays Yokoyama [2003]. In this particular ink-jetted OTFT, the device is accomplished by using a material ink-jet printer, which can achieve a 20um resolution, to deposit different functional and liquid-phase "inks" on the desired locations. Due to the high sensitivity of the semiconducting material (ex. SP220) to the ambient air (ex. oxygen and water vapor), the top-gate structure is applied in which the gate dielectrics will be deposited on top of the semiconductor layer and form a protection layer to prevent the semiconductor layer from exposing to the ambient air. Since most soluble materials for ink-jet printing is polymers and the complete ink-jet printing process is accomplished under the room-temperature, the semiconducting material is usually amorphous and has lower carrier mobility (0.001 cm^2/vs) than small-molecule organic materials.
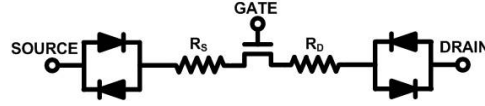
Figure 3.9: An equivalent circuit model of organic TFTs. R_S and R_D are used to model contact resistance and the diode-pairs are for non-linearity of contact resistance.

3.2.3 Device Modeling

Figure 3.9 shows the equivalent circuit model of organic TFTs, in which only DC model is shown here. Similar to a-Si:H TFTs, the organic TFTs can be modeled as a parallel plate capacitor that accumulates holes (p-type) as charge carriers. The device model of organic TFTs can be described using the percolation model Vissenberg and Matters [1998]for charge transport in the accumulation channel. Equation 3.3 describes the drain current I_{DS} in the saturation region when $|V_D| > |V_G - V_T|$ while Equation 3.4 describes the drain current in the sub-threshold region when $|V_G - V_T| \sim 0V$ Klauk [2006].

$$I_{DS}^{acc,1} = -\frac{\mu_0 W C_i}{L(2+\gamma)}[[[-V_G + V_T]]^{2+\gamma} - [[-V_G + V_T + V_D]]^{2+\gamma}]$$

$$I_{DS}^{acc,2} = I_{DS}^{acc,1} \cdot min\left(1 + \kappa[[V_D]], 1 + \kappa[[-V_G + V_T]]\right)$$

$$I_{DS}^{acc,total} = I_{DS}^{acc,2} + \lambda\frac{W^{\frac{1}{3}}}{L}\left([[V_G - V_T - V_D]] \cdot |I_{DS}^{acc,2}|_{V_D=V_G-V_T}\right)^{\frac{2}{3}}$$

(3.3)

$$I_{DS}^{sub} = I_0|V_D|^{\sigma} \cdot exp\left[\frac{ln10}{S}[[V_G - V_T]]\right]$$
(3.4)

where μ_0 is the carrier mobility, C_i is the gate capacitance, W is the gate width, L is the gate length, γ is the mobility exponent, κ is the linear correction parameter, λ is the channel-shortening term, S is the inverse subthreshold slope, and I_0 and σ are fitting terms.

3.2.4   Degradation Mechanism

There are two major instability mechanisms – electrical and chemical instabilities – that can cause the device characteristics to shift over time. Oxygen, for instance, is the major cause of chemical instability. Oxygen is suggested as a dopant for a variety of semiconducting polymers such as P3HT and PQT-12 and will interact with the semiconductor materials to change their properties. Encapsulation methods to prevent semiconducting polymers from exposing to the ambient air are available and proven useful to extend the shelf-lifetime of polymeric TFTs in practical applications. The chemical instability, therefore, seems to be a solvable problem.

On the other hand, the electrical instability caused by bias-stress is much harder to get rid of. In most organic TFTs, which are p-channel accumulation devices, negative shifts of threshold voltage (ΔV_{TH}) can be observed after applying negative gate voltages (i.e. bias-stress) to TFTs. Charge-trapping is the major mechanism to be responsible for this phenomenon and is proportional to $C_{OX}|V_G - V_T|$. Charge-trapping can happen in the gate dielectric, in the localized states at the semiconductor-dielectric interface, or in the deep states in the semiconductor. These immobilized charges shield the gate voltages to accumulate mobile charges and hence reduce the conduction currents Salleo and Street [2003]. An analytical model of the threshold voltage shift of PQT-12 polymeric TFTs is shown in Equation 3.5.

$$|\Delta V_T| = A(V_G - V_T^0)^n \cdot t^\gamma \tag{3.5}$$

where A, n, and γ are fitting parameters, V_T^0 represents the initial threshold voltage of the TFT, and t is the bias-stress time.

3.3   Self-Assembled-Monolayer (SAM) OTFT

3.3.1   Device Basics

The high operation voltage is one of the major challenges for organic TFTs. To explore a low-voltage operation capability, a research group in University of Tokyo has demonstrated 2V organic TFTs that can share
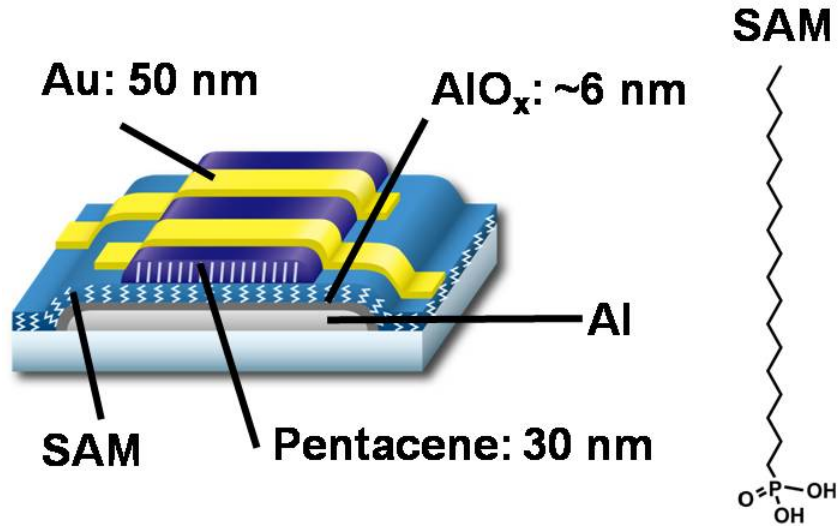
Figure 3.10: A schematic sideview of a 2V SAM OTFT. (photo courtesy of Someya group, Univ. of Tokyo)

the same voltage source with the 0.18um CMOS ICs Ishida et al. [2009]. Self-assembled-monolayer (SAM) dielectric is an organic solution that can help form a good quality semiconductor-dielectric interface for organic TFTs. With SAM-modified gate dielectrics, the gate leakage can be improved significantly, which opens the opportunity of using thin dielectric layers. As shown in Figure 3.10, a thin layer ($\sim$6nm) of thermally-grown aluminum-oxide AlO_X is applied as the gate dielectric and the interfacial control is accomplished by immersing the whole substrate into the SAM solution to form a thin SAM layer. The air-stable organic semiconductor *Pentacene* is then thermally-evaporated on top of the SAM-modified dielectric layer. This thin-layer gate dielectric enables a low-voltage operation ($\sim$2V) without introducing the gate leakage problem. Figure 3.11 shows a typical multi-finger SAM OTFT that is used to build integrated circuits that will be discussed in Chapter 4.
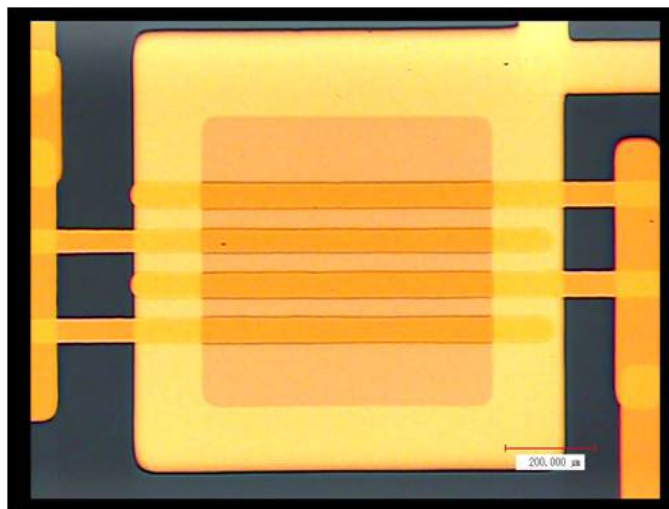
Figure 3.11: A device photo of a 2V SAM OTFT with multiple fingers. Center yellow part is the GATE metal, orange part is semiconductor Pentacene, and yellow fingers on the two sides are S/D metals. (photo courtesy of Someya group, Univ. of Tokyo)

3.3.2   Device Modeling

To perform circuit simulation for SAM-OTFT based circuits, Verilog-A based device models have been developed that can be integrated into major circuit simulators such as *HSPICE* and *Cadence Virtuoso*. The model is evolved from the model of field-effect transistors and has taken into account the carrier mobility dependence on the gate voltage V_{GS}. The comparison of I_{DS} and V_{GS} relationship between measurement and simulation can be found in Figure 3.12. Likewise, the I_{DS} and V_{GS} relationship can also be found in in Figure 3.13. To examine the model for multiple-finger devices, larger-size SAM OTFTs (W = 1500 um) are also used for comparison and can be seen in Figures 3.14 and 3.15. The mobility dependence on the gate overdrive voltage $(V_{GS}-V_T)$ is described in Equation 3.6 and the saturation drain-source current I_{SAT} is shown in Equation 3.7. Similar to silicon field-effect transistors, in the saturation region, the drain-source current I_{DS} has quadratic dependence on the overdrive voltage but is independent of the drain-

Figure 3.12: (a) A log scale plot of drain current I_{DS} versus gate voltage V_{GS} of a 2V SAM OTFT.(courtesy of Someya group, Univ. of Tokyo);(b) ID-VGS SAM OTFT device model using verilog-A.

source voltage V_{DS}. In the linear region, the drain-source current I_{DS} is dependent on V_{DS} as can be seen in Equation 3.8.

$$\mu = \mu_0 \cdot |V_{GS} - V_T|^{\gamma} \tag{3.6}$$

$$V_{GTE} = \frac{S}{2}\left|1 + \frac{V_{GS} - V_T}{S} + \sqrt{\delta^2 + \left(\frac{V_{GS} - V_T}{S} + 1\right)^2}\right|$$

$$I_{SAT} = \frac{1}{2}\mu C_{ox}\frac{W}{L}V_{GTE}^{2+\gamma} \tag{3.7}$$

$$V_{DSE} = \left[1 + \left(\frac{\mu C_{ox}\frac{W}{L} \cdot V_{DS}}{I_{SAT}}\right)^{\alpha}\right]^{\frac{1}{\alpha}}$$

$$I_{DS} = \mu C_{ox}\frac{W}{L}V_{GTE}^{1+\gamma} \cdot \left(1 + \frac{\lambda V_{DS}}{V_{DSE}}\right) \cdot V_{DS} \tag{3.8}$$

where V_{GTE} is the V_{GS} smoothing function, S, δ, and α are fitting parameters, μ_0 is the mobility pre-factor, γ is the mobility exponent, C_{ox} is the gate capacitance, and λ is the channel-shortening term.

Figure 3.13: (a) A linear scale plot of drain current I_{DS} versus drain-source voltage V_{DS} of a 2V SAM OTFT (courtesy of Someya group, Univ. of Tokyo); (b)ID-VDS SAM OTFT device model using verilog-A.
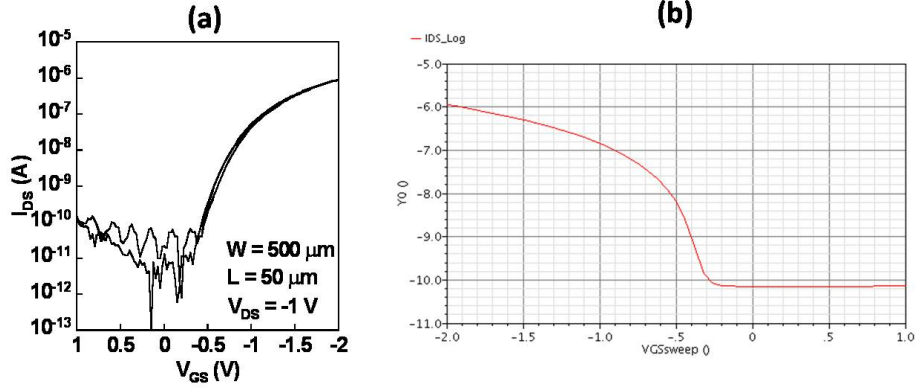

Figure 3.14: (a) A log scale plot of drain current I_{DS} versus gate voltage V_{GS} of a 2V SAM OTFT (W=1500 um).(courtesy of Someya group, Univ. of Tokyo);(b) ID-VGS SAM OTFT device model using verilog-A.
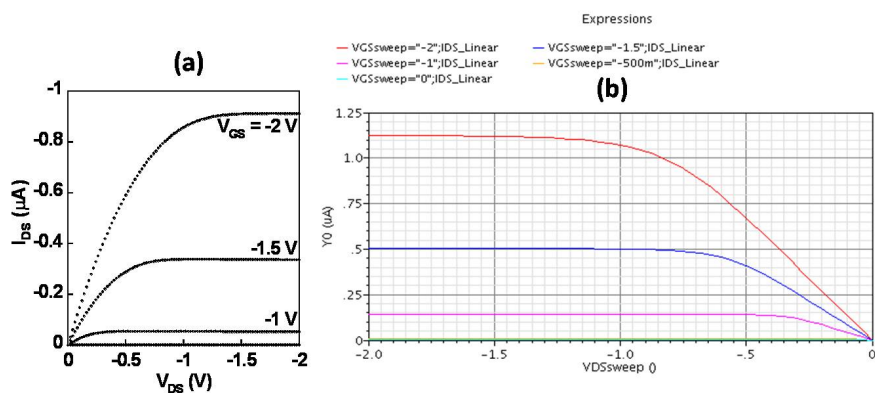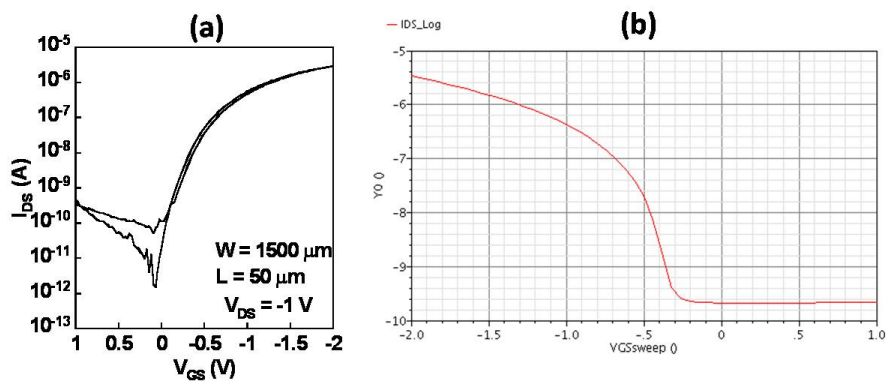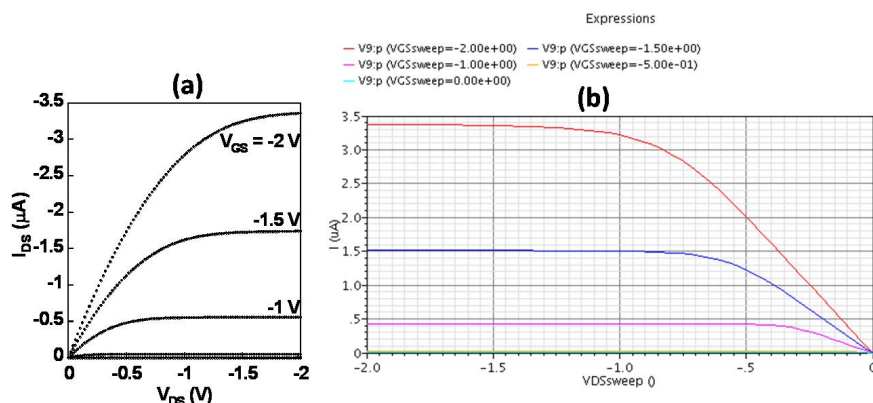
Figure 3.15: (a) A linear scale plot of drain current I_{DS} versus drain-source voltage V_{DS} of a 2V SAM OTFT (W=1500 um). (courtesy of Someya group, Univ. of Tokyo); (b)ID-VDS SAM OTFT device model using verilog-A.

3.4 Metal-Oxide TFT

3.4.1 Device Basics

Figure 3.16 shows IGZO TFTs on low-cost flexible substrates such as polyimide plastics. Metal-oxide TFTs such as IGO TFTs are emerging as a promising candidate in replacement of a-Si:H TFTs in display and imaging applications because of the following reasons: 1) higher carrier mobility, 2) better transparency, and 3) better reliability. Metal oxide TFTs have higher carrier mobility ($\sim$10 cm^2/Vs) than a-Si:H TFTs ($\sim$1 cm^2/Vs). This means that as a pixel switch, it can switch faster to provide a better quality of dynamic images or videos than conventional a-Si:H TFT-LCDs. It can also provides higher conduction current to support future-generation organic LED (OLED) displays that usually need a higher driving current to provide a better contrast ratio and dynamic response than conventional LCD displays. Thanks to the wide bandgap of the semiconductor materials ($\sim$3eV), most of the visible light can pass through the device, which makes the metal-oxide such as ZnO and IGZO TFTs transparent to human eyes. This is beneficial for display applications since metal-oxide TFTs can provide a better

Figure 3.16: A device photo of transparent metal-oxide (IGZO) TFTs. (Photo courtesy of ITRI-FETD)

aperture ratio that lets more back-light pass through and therefore less light-intensity is needed for the same brightness than conventional a-Si:H TFT-LCD displays. This also saves a significant amount of energy. Threshold voltage shifts (ΔV_{TH}) is common for a-Si:H TFTs and limits a-Si:H TFTs from being used in a wider spectrum of applications than display pixels. (other applications such as a scan driver for displays require a careful design style to prevent significant degradations over a short period of time). Recent reports of metal-oxide TFTs stability Cross and Souza [2006], Oh et al. [2008] suggest that with proper treatments in the device fabrication (ex. annealing), the metal-oxide TFTs can exhibit excellent stability and can fulfill reliability and lifetime requirements. Figures 3.17 and 3.18 show the relationship of drain-source currents (I_{DS}) versus gate voltage V_{GS} in the log-scale and versus V_{DS} in the linear scale for IGZO TFTs. As we can find in Figure 3.17 that the threshold voltage V_{TH} of this test device is slightly negative, which suggests that this TFT is a n-type depletion-mode device. The uniformity data of IGZO TFTs on a 6-inch wafer-shape plastic can be found in Figure 3.19.

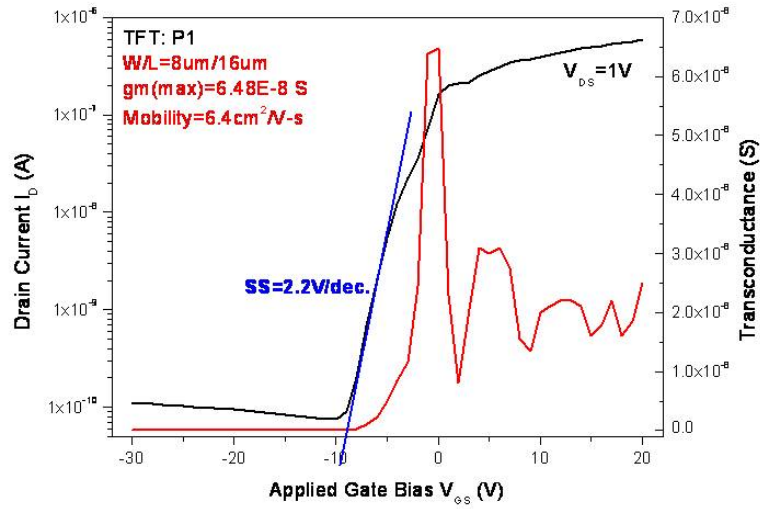**Figure 3.17:** A log scale plot of drain current I_{DS} versus gate voltage V_{GS} of a IGZO TFT (courtesy of ITRI-FETD)
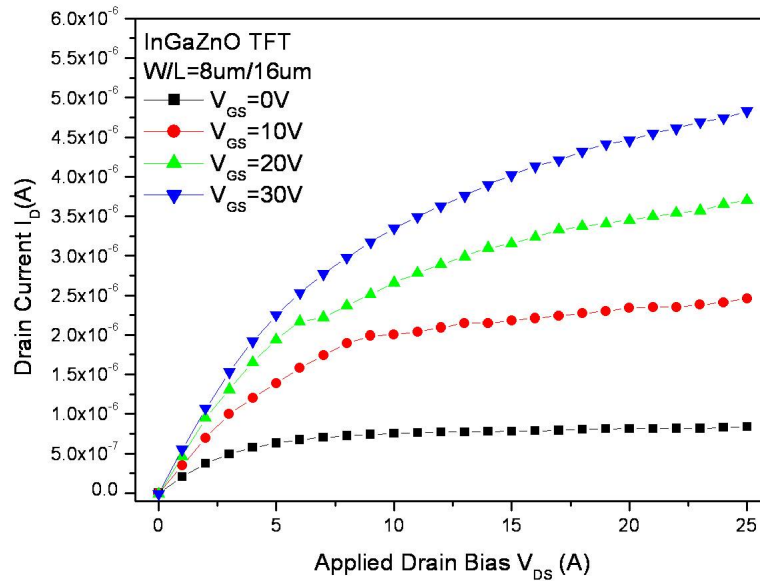
Figure 3.18: A linear scale plot of drain current I_{DS} versus drain-source voltage V_{DS} of a IGZO TFT (courtesy of ITRI-FETD)
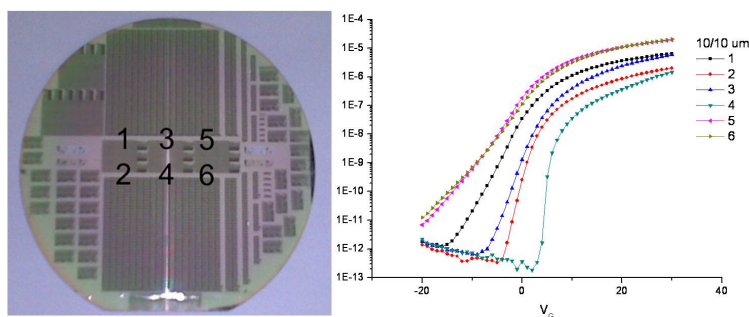
Figure 3.19: IGZO TFT testkeys on a 6-inch wafer-shape plastic and their IDS-VGS curves in log-scale. Number 1 to 6 represent testkeys on different locations. (Courtesy of ITRI-FETD)

3.4.2   Device Manufacturing

Figure 3.20 shows the process flow of IGZO TFTs. The standard photo-lithography is utilized to define the desired patterns of TFT circuits. To be compatible with flexible substrates such as polyimide and PET plastics, the process temperature is controlled within 150 degree C by using RF magnetron sputtering with a low vacuum chamber to deposit gate dielectrics and semiconductors (ex. ZnO and IGZO). To ease the sample handling, the plastic substrate is first attached to a 6-inch silicon wafer as the base throughout all process steps. This plastic substrate can then be detached from the silicon wafer after circuit fabrication and the silicon wafer can be re-used for next samples.

3.5   Impact of Physical Strains

Flexible electronics are subject to bending; it is important to understand the TFT performance during and after mechanical stress.

In Gleskova et al. [2002], the electrical performance of back-channel etch a-Si:H TFTs fabricated on 25-μm thick Kapton foil is evaluated. The transistors are strained by either bending or stretching. Inward cylindrical bending (Figure 3.21a) produces compression (neg-
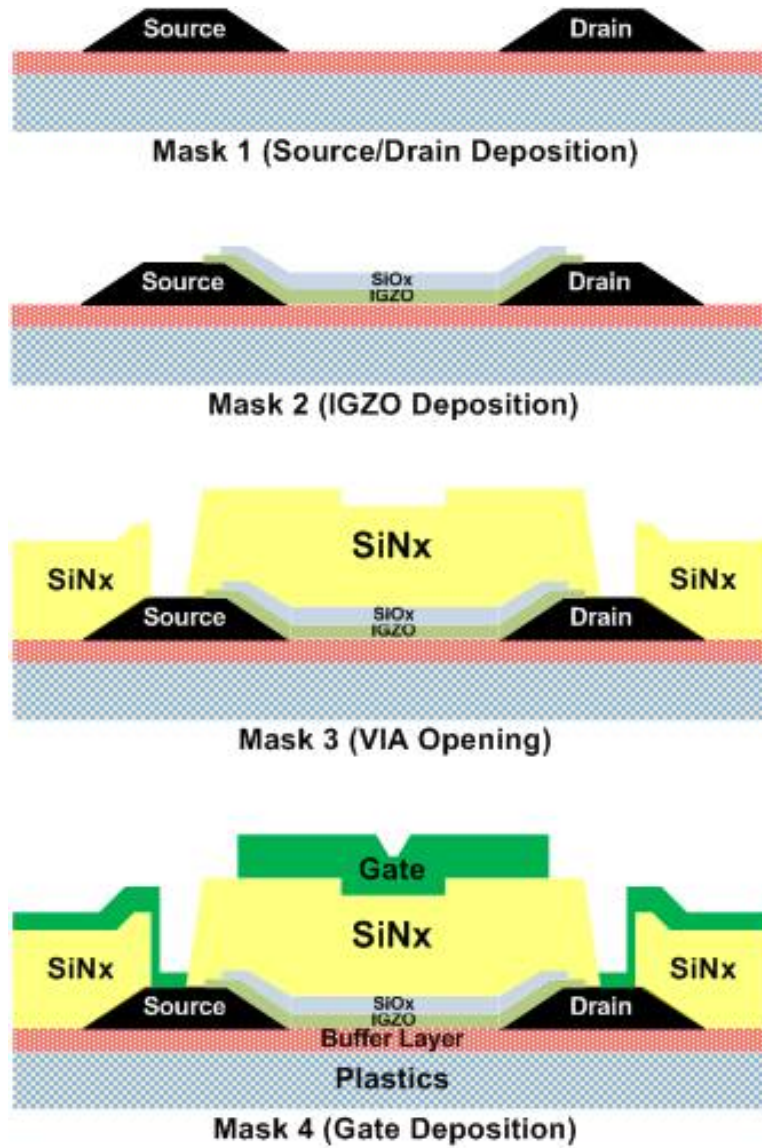
Figure 3.20: IGZO TFT process flow with 4 photo masks
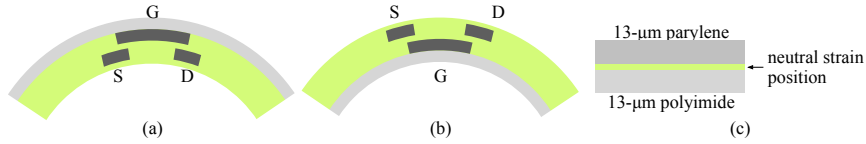
Figure 3.21: The inward (a) and outward (b) bending, and the neutral strain position (c).
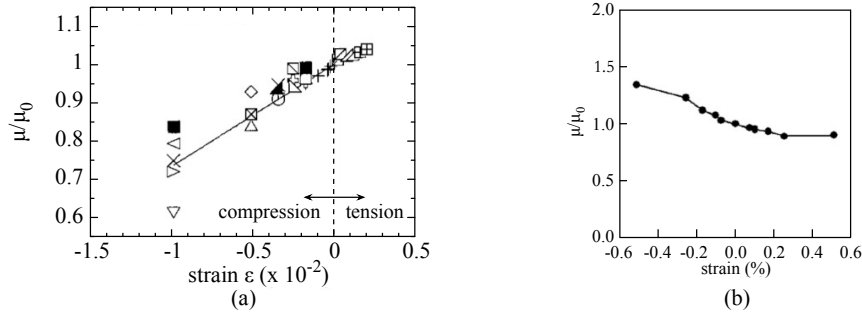
Figure 3.22: Relative mobility under different strains: (a) Gleskova et al. [2002], (b) Cheon et al. [2008].

ative strain), and outward bending (Figure 3.21b) produces tension (positive strain). Stretching, on the other hand, only produces tensile strain due to the tester setup. Figure 3.22a shows the relative mobility (μ/μ_0) under different strain (ε) — μ and μ_0 correspond to the linear mobility under the imposed strain and the initial linear mobility, respectively, and ε ranges from a compressive strain of -0.01 (at the bending radius of 1.6 mm) to a tensile strain of 0.002. It is observed that the mobility decreases under compression but increases under tension; a linear fit of the measurements gives

$$\mu/\mu_0 = 1 + 26 \times \varepsilon. \tag{3.9}$$

It is also concluded that the on and leakage currents did not change.

Cheon et al. [2008] investigated the performance of strained poly-Si TFTs that are fabricated on 50-μm flexible metal foil. Figure 3.22b shows the impact of strain on relative mobility; the trend is opposite to that in Gleskova et al. [2002] and can be expressed by

$$\mu/\mu_0 = 1 - 0.44 \times \varepsilon \tag{3.10}$$

when the strain is $|\varepsilon| \leq 1\%$. It is observed that the threshold voltage and gate voltage swing remain unchanged under mechanical strain. In Münzenrieder et al. [2011], the impact on flexible IGZO TFTs on 50-μm Kapton foil is studied. When measured in the darkness, the measured parameters, including mobility, threshold voltage, and the subthreshold swing change linearly with the applied strain, from -0.003 (at about 9 mm bending radius) to 0.003. Among them, the normalized linear mobility can be expressed by

$$\mu/\mu_0 = 1.005 + 0.062 \times \varepsilon. \tag{3.11}$$

Note that the impact of bending increases substantially when the TFTs are illuminated.

One way to relieve the mechanical strain induced performance variation is to embed the TFT's at a neutral strain position Sekitani et al. [2005]. In Sekitani et al. [2005], the pentacene FETs are fabricated on a 13-μm polyimide film and encapsulated by passivation layers of polychloro-para-xylylene with the same thickness; this places the FETs at the neutral strain position (Figure 3.21c). With a bending radius as small as 2 mm, the change in mobility is less than 3% on compressive and tensile strains which exhibits a significant reduction compared to cases without the encapsulation layer.

3.6 Summary

In this chapter, we give an overview of several TFT technologies, ranging from conventional amorphous silicon TFTs, organic TFTs, to transparent metal-oxide TFTs, and discuss their device characteristics, models, and degradation mechanisms. In general, inorganic TFT technologies, such as amorphous silicon and metal-oxide TFTs, have better carrier mobility, smaller feature size, and greater ambient stability, while require a higher process temperature and have worse physical flexibility than the organic TFT counterparts. These TFTs are therefore more suitable for applications that require long-term reliability and fine features such as high-resolution displays used in consumer electronics such as TVs, tablets and smartphones. Organic TFTs usually have much better physical flexibility and lower capital investment for

printing facilities. Among organic TFT technologies, the carrier mobility of SAM-organic TFT is an order of magnitude or better than that of ink-jet printed organic TFT, but it requires a vacuum deposition process for the organic semiconductor. This inevitably increases the manufacturing costs and reduces the throughput. Studies of new organic materials, that are suitable for ink-jet printing and can achieve sufficiently high performance for emerging applications such as electronics in wearable sensors and smart tags, have been an active research subject with significant progresses.

4

Circuit Design

Thin-film transistors (TFTs) are an essential element of circuit design for flexible electronics. The major technological challenges for TFTs, however, are their lack of complementary type devices Klauk et al. [2007], poor long-term stability Gomes et al. [2004], and the requirement of a high supply voltage. To address some of these challenges, significant innovations in device and material engineering have been made Umeda et al. [2007], Ling et al. [2007], Wager [2007] to improve TFT performance. However, relatively less research efforts have been made at higher levels of design abstraction, including the circuit, architecture and system levels, which are equally critical for addressing such challenges. In this chapter, we describe some advances in TFT-based circuit design. Although there are many types of TFT technologies that can also used to construct flexible circuits, this chapter emphasizes organic and metal-oxide TFT circuits since they attract the majority of recent research efforts to solve the circuit design challenges.

4.1   Digital Circuit

Conventional mono-type digital design styles such as the diode-load and resistive-load designs Rabaey et al. [2003] often suffer from high static power consumption and poor noise margin due to their ratioed-logic nature. NMOS-logic had been widely used for designing Si digital circuits in 1980s when PMOS was not yet mature for implementing CMOS-logic Rabaey et al. [2003]. In the past ten years, inverter designs using mono-type TFTs Cantatore et al. [2007], Gamota et al. [2004], Myny et al. [2009, 2010] have been proposed by several groups to resolve this problem but they usually require dedicated TFT characteristics and manipulations (ex. depletion-mode Cantatore et al. [2007], dual-gate Myny et al. [2010, 2011], and dual-V_T TFTs Nausieda et al. [2009]). Complementary TFT inverters have been demonstrated using both p- and n-type organic TFTs De Vusser et al. [2006], Blache et al. [2009], Klauk et al. [2007] or inorganic-organic hybrid channel integration such as a combination of n-type solution-processed metal-oxide and p-type organic semiconductors Oh et al. [2007], Myny et al. [2012, 2014] to achieve low-power consumption and high noise-margin for complex digital circuits such as microprocessors on a plastic film Myny et al. [2014]. In order to achieve excellent noise-margin without increasing process complexity such as dual-gate or dual-V_T TFTs, a novel design style *Pseudo-CMOS* Huang et al. [2011] using only mono-type single-V_T TFTs was proposed in which a level-shifter is built-in to the digital circuits such as inverters to shift V_{TRIP} (trip point) by means of a tuning voltage *VSS*. This unique feature provides several advantages including post-fabrication tunability and better noise-margin as well as higher small-signal gain Huang et al. [2011], Ishida et al. [2011, 2013]. The schematic and measured transfer functions of *Pseudo-CMOS* inverters are shown in Figures 4.1 and 4.2. *Pseudo-CMOS* inverters show the record-high small-signal gain for organic circuits (>300) and the ring-oscillator shows capability of the low-voltage operation (0.5V) Fukuda et al. [2011], Yokota et al. [2012]. Further analysis can be found in Cantatore et al. [2007], Huang and Cheng [2009], Myny et al. [2010], Huang et al. [2011], Fukuda et al. [2011], Yokota et al. [2012].
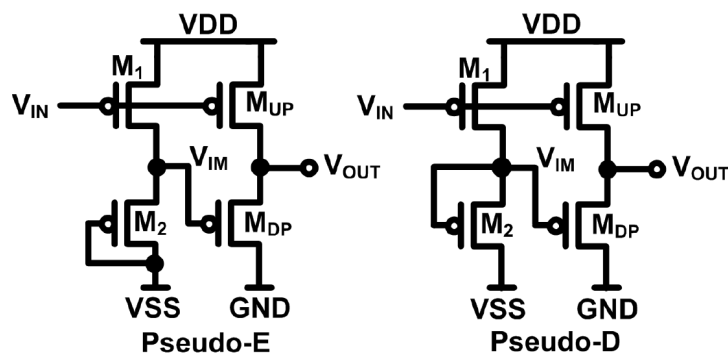
Figure 4.1: Two varieties of Pseudo-CMOS inverter designs using only p-type single-V_T TFTs. The differences between Pseudo-E and Pseudo-D inverters are the gate connection of M_2 and the M_1/M_2 pair channel width sizing ratio $\frac{W_1}{W_2}$. Huang et al. [2011]

4.1.1 Zero-VGS Inverter

The inverter design with zero-VGS load has been implemented for RFID tags in Cantatore et al. [2007], Myny et al. [2008] because of its low power consumption. Figure 4.3 shows the zero-VGS inverter using either only p-type or only n-type TFTs. In order to increase the pull-down force and improve the asymmetric characteristics, these p-type TFTs are engineered to have positive V_T, i.e. $V_T > 0$V, and the output voltage is determined by the sizing ratio between W_1 and W_2. When the input level is high (i.e. GND), due to positive V_T, both W_1 and W_2 are conducting and the output level is gradually pulled to close to low (i.e. -VDD) because of a large W_2/W_1 ($W_2 \gg W_1$) sizing ratio. When the input level is low, M_1 provides a strong pull-up force and pulls the output level to close to high. Despite the advantages such as low-power consumption and simplicity of the design, the drawbacks for this design include: 1) poor noise margin due to asymmetric transfer characteristics, 2) slow switching speed, 3) V_T engineering required to have normally-on TFTs, and 4) output voltage level dependence on the W_2/W_1 sizing ratio.
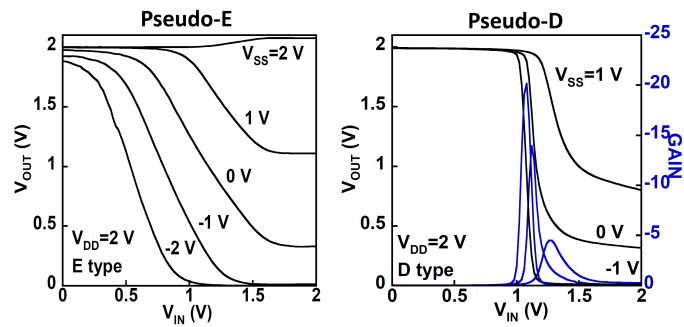
Figure 4.2: Measured inverter voltage transfer curve (VTC) of the Pseudo-E and Pseudo-D inverters based on 2V self-assembly-monolayer (SAM) organic TFTs. Each curve represents VTC with different tuning voltage *VSS*. The maximal achievable inverter gain is tunable and can reach >20 for Pseudo-D inverters in this case and the highest gain > 300 is reported in Fukuda et al. [2011].
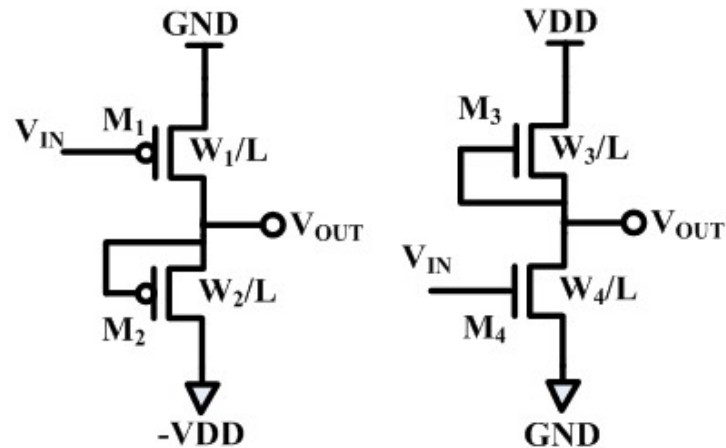
Figure 4.3: Inverters with zero-V_{GS} load using p- or n-type TFTs.

(a)   (b)
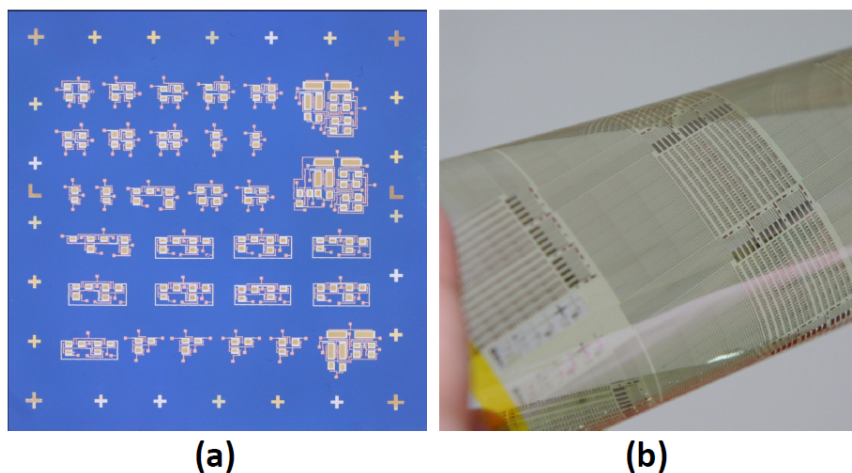
Figure 4.4: Pseudo-CMOS circuits implemented in (a) 2V SAM OTFTs on a silicon wafer, and (b) transparent IGZO TFTs on a plastic substrate. Huang et al. [2011]

4.1.2 Pseudo-CMOS Inverter

Figure 4.4 shows the fabricated Pseudo-CMOS cell-library based on 2V p-type SAM-organic TFTs on a silicon wafer and 20V n-type metal-oxide TFTs on a plastic film. Characteristics of these TFTs have been discussed in Chapter 3.

While being used to build larger digital building blocks such as a frequency divider or a binary counter for a complete system such as in Ishida et al. [2011, 2013], the high noise-immunity and robustness against process variations of *Pseudo-CMOS* provides a superior circuit yield particularly under low-voltage operations.

4.1.3 Dual-Gate Inverter

Since large process variations are inherent in low-cost printing process and difficult to minimize, new TFT structures such as dual-gate organic TFTs that consist of both top and bottom gate TFTs are proposed to control V_T Myny et al. [2010, 2011] even after the circuit fabrication, which is an effective method to improve the overall circuit
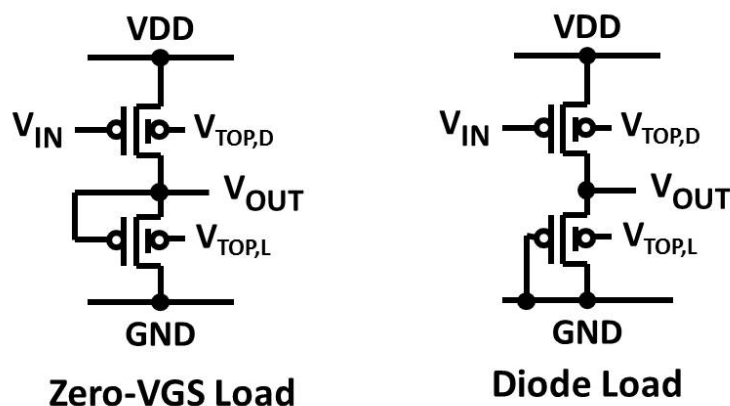
Figure 4.5: Dual-gate inverters with Zero-VGS and diode loads.

yield while fabricating large-scale organic circuits such as RFID tags or microprocessors with thousands of organic TFTs. Figure 4.5 shows the dual-gate inverters with Zero-VGS and diode loads. While the bottom gate acts as the normal gate terminal, the top gate is used as the tuning knob to control V_T. The 64b organic RFID can be operated at maximum 4.3kb/s data rate with the dual-gate diode-load design and at 522b/s data rate with the dual-date Zero-VGS load with 20V supply voltageMyny et al. [2010].

4.1.4   Complementary Inverter

While complementary design, i.e. with both p- and n-type devices, is prevailing in modern silicon VLSI, it is not the case for flexible TFT circuits since not both types of TFTs are readily available with equivalent performance and long-term reliability. P-type organic TFTs, for example, have better carrier mobility ($\sim 10X$) as well as long-term material reliability than their n-type counterparts. Instead of directly constructing complementary organic TFT circuits, recent advances in solution-processed n-type metal-oxide TFTs make the hybrid integration of n-type metal-oxide and p-type organic TFTs to implement large-scale complementary TFT circuits an attractive solution. In Myny et al.

[2012], an HF hybrid organic/solution-processed metal-oxide RFID tag that consists of 368 metal-oxide and 365 organic pentacene TFTs is reported to achieve 1200 bits/s data rate. The same group also reports an 8b microprocessor that consists of 1752 metal-oxide and 1752 organic TFTs with more than 400 inkjet-printed organic TFTs in a P^2ROM memory Myny et al. [2014].

4.2 Analog and Mixed-Signal Circuit

Analog TFT circuitry is inherently more challenging than its digital counterpart because the analog circuit performance is strongly dependent on the TFT characteristics that have high parametric variability of the TFT printing process. Key design parameters in analog circuits such as transconductance g_m and cut-off frequency f_T is also severely limited in TFT technologies due to its low carrier mobility and large parasitic capacitance. Various design techniques Marien et al. [2010], Xiong et al. [2010], Abdinia et al. [2013], Fuketa et al. [2013, 2014], Raiteri et al. [2013] as well as novel floating-gate TFT structures Ishida et al. [2011], Yokota et al. [2012] are proposed to mitigate the impact of process variations to the circuit performance. In the following, we focus on key analog building blocks such as analog-to-digital converters (ADCs) and operational amplifiers to illustrate recent advances in analog TFT circuits.

4.2.1 Analog-to-Digital Converter (ADC)

In Huang et al. [2008], to explore the feasibility of high-speed analog and mixed-signal circuit design, a 3b 1.25KS/s Flash ADC based on amorphous silicon TFTs has been implemented. The flash ADC architecture is advantageous in its fast conversion speed for sensing and display applications. The comparator core is composed of a *Pseudo-CMOS* latch by which the high small-signal gain can provide shorter regeneration time and better signal resolution than conventional negative-g_m comparator core. In order to tackle the process variations to ADC performance deviations, a successive-approximation (SAR) ADC Xiong

et al. [2010] is proposed by incorporating complementary organic TFT inverters as the comparator core, the C-2C architecture for digital-to-analog converters (DACs), and an external FPGA for SAR logic. The impact of the device mismatch to the ADC accuracy is mitigated by using a two-phase operation for the inverter-based comparator core, for which the static offset is zeroed by shorting the inverter input to the output in the reset phase. It demonstrated a maximum DNL of -0.6 LSB and a maximum INL of 0.6 LSB at 10Hz sampling frequency. A fully printed 4b ADC is first appeared in Abdinia et al. [2013] based on 40V organic complementary TFTs. In this work, in order to accommodate limited TFT yield with the given printed TFT technology, a simplifier ADC architecture that consists of a comparator, a 4b R-2R DAC, and a counter is proposed. Similar to Xiong et al. [2010], the comparator in this work also applies a self-biased complementary inverter with a reset phase to cancel static offsets. An ADC sample rate of 2.05Hz with 19.6dB signal-to-noise distortion ratio (SNDR) is demonstrated.

4.2.2   Operational Amplifier

The high-gain operational amplifier serves as a key analog component for analog building blocks such as $\Delta\Sigma$ ADC Marien et al. [2010]. The operational amplifier is composed of three stages of differential amplifiers that apply common-mode feedback (CMFB) to cancel DC offsets due to device mismatch and bootstrapped gain enhancement to achieve a 15dB signal gain with around 1KHz 3dB bandwidth. The input offset due to device mismatches at the input differential pair, however, is not addressed in this work. In order to minimize the input offsets at the differential amplifiers, the floating-gate (FG) organic TFT technology is proposed and applied to an organic operational amplifier Ishida et al. [2011]. By applying high compensation voltages to the FG organic TFTs, the V_T mismatch at the differential amplifier due to process variations can be altered and minimized as demonstrated in Ishida et al. [2011]. In addition to applying CMFB or FG-OTFT technology to address the DC offset variations or device mismatch at the input differential pair, a self-biased inverter can also serve as a singled-ended

high-gain amplifier. In Yokota et al. [2012], a *Pseudo-CMOS* based self-biased inverter is used as a high-gain amplifier with a 130 V/V (42dB) signal gain of a singled-stage amplifier up to 50Hz is demonstrated. The FG-OTFT technology is also applied to the input TFT of the amplifier that shows the capability of minimizing the variations by 20X.

4.3 Summary

In this chapter, we illustrate several design solutions for both digital and analog circuits. Owing to unavailability of complementary-type TFTs, large process variations, and a low carrier mobility, the performance of TFT circuits is significantly slower than that of their silicon electronics counterparts. Despite these limitations, TFT circuits are indispensable to realize monolithic system integration for applications ranging from flexible displays to smart bandages. Heterogeneous system integration to include both flexible sensors and silicon chips and pattern transferring from a silicon chip to a flexible substrate are other alternatives for implementing flexile electronics. However, the disadvantages of these alternatives are higher manufacturing costs and their limited scalability for large-area electronics.

5

Design Automation and Test

Electronics design automation (EDA) plays a crucial role in the success of the semiconductor industry. As the design complexity continues to grow, designers rely heavily on EDA tools to solve well-defined and well-modeled design problems, such as equivalence checking, logic synthesis, physical design, and test pattern generation, which allows them to spend a greater portion of their design efforts on addressing new challenges and focusing on innovations that can differentiate their products from others.

Compared to CMOS circuits, flexible electronics suffer process variations, performance degradation over time, and are very often subjected to physical strains. Proper modifications to current EDA tools are necessary to better handle these differences.

This chapter starts with a brief review on the CMOS design and test automation flow and flexible electronics features. It's then followed by overview of flexible electronics EDA, including timing analysis, cell placement, manufacturing testing, and circuit optimization.
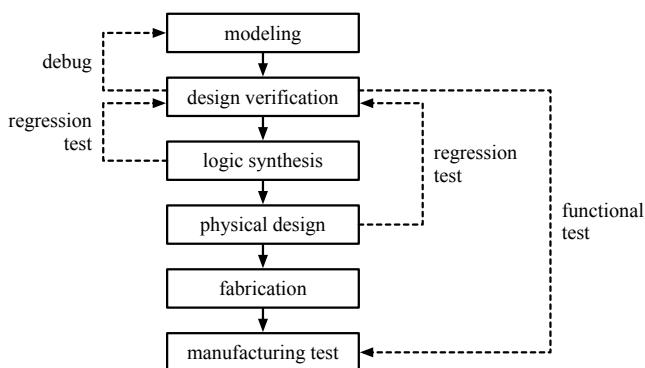
Figure 5.1: A typical CMOS design and test automation flow

5.1 Need of Design and Test Automation

Figure 5.1 depicts a typical EDA flow for digital CMOS designs Wang
et al. [2009]. It begins with the design modeling and verification loop,
which continues until the design model processes the necessary details,
ex. the register-transfer-level (RTL) design, to proceed to logic synthe-
sis. In the logic synthesis stage, the logic function specified by the RTL
description is realized by interconnecting digital building blocks (stan-
dard cells) including primitive gates (NOR, NAND, inverter, DFF, etc.)
and complex gates (AOI, OAI, etc.). The following physical design stage
then determines the locations of the standard cells, i.e., placement, and
realizes the specified interconnections, i.e., routing. The layout informa-
tion is eventually converted to the GDSII stream format for fabrication.
Starting from logic synthesis, the flow has been highly automated. Nev-
ertheless, one usually includes in the test suite the functional stimuli
and responses obtained from the design verification stage to enhance
the manufacturing test quality.

Currently, the level of design automation for flexible electronics is
low and most tools are used for designing regular structures such as
display pixel circuits, sensor arrays, or scan drivers Costa and Martin
[1994]. For these applications, the designers spend most efforts on op-
timizing the basic building blocks and the need for automation is often

limited to device characterization and circuit simulation only.

Today's TFT technologies have made possible highly integrated flexible circuits, for example, the Z80 CPU Lee et al. [2003], the 8-bit microprocessor Karaki et al. [2005], and the fixed-coefficient FIR filter Bai et al. [2008]. Also, analog/mixed-signal circuits that use TFT devices have been reported in Tarn et al. [2010]. It is foreseeable that complex flexible systems-on-panel that integrate the digital and analog/mixed-signal circuits with the pixel, sensor, or photovoltaics arrays will be realized in the future, and EDA will be the key to success.

In the following sections, we will discuss EDA tools and methodologies developed to meet the flexible electronics design challenges. Our discussion covers the following categories:

Timing analysis. Flexible electronics are suitable for large area applications because they can withstand bending and have low cost per unit area. However, physical stress causes TFT mobility shift and may eventually lead to timing violations for a larger scale of digital circuits. The static timing analyzer proposed in Hsu et al. [2010] enables the designers to analyze the potential bending-induced timing violations and apply necessary fixes.

Placement. One solution to the physical stress induced timing violations is bending-aware cell placement Liu et al. [2011], Lin et al. [2013] which properly distribute the cells on timing critical paths to prevent the aggregate delay variations from causing timing violations.

Yield optimization. Ensuring high manufacturing yields for flexible analog/mixed-signal circuits is complicated due to large process variations, aging, and bending. In Chen et al. [2013, 2014], circuit optimization techniques are developed to maximize the fresh and lifetime yields in the presence of process variations and bending.

Manufacturing test. Burn-in with elevated temperature and voltage stress is effective in screening out unreliable circuits; however, the incurred cost and the destructive nature make it unsuitable for flexible circuits. In Shen et al. [2010], it is shown that very

low voltage testing is a promising alternative to burn-in. For test application, Cheng and Li [2011] presented an asynchronous scan flip-flop design as asynchronous design may be a more robust design style for flexible circuits.

5.2 Timing Analysis

For flexible electronics, bending induced TFT mobility variations are a critical concern; this is depicted in Table 5.1 for three different TFT technologies. It is evident that negligence of the mobility variations can easily result in timing violations in flexible synchronous circuits.

The authors of Hsu et al. [2010] proposed a bending-aware static timing analyzer for flexible TFT circuits (STAF) which identifies vulnerable regions in a flexible circuit which, when being bent, will cause timing violations. As shown in Figure 5.2, STAF first derives, via circuit simulation, the cell delays with respect to different mobility and load combinations.

Then, STAF can be applied to analyze the circuit delays. For a flexible TFT circuit, a *region under bending* (RUB) is an area within which all cells are bent by a specific radius. To assess the timing impact associated with a bent RUB, STAF replaces all the cells in the target RUB with their *bent* versions and derive the delays of the long and short paths. After applying this procedure to all RUB's, a map can be plotted to show to what extent bending each RUB affects the circuit timing.

Figure 5.3a shows the decrease of the shortest path delay for the benchmark circuit s38584 (in 8 μm a-Si technology). In the plot, each square corresponds to a 0.1-by-0.1 cm^2 RUB, and the injected mobility variation is 10%; the color of each square indicates its impact on timing, ranging from 0 (white) to 30% (black). Figure 5.3b shows the increase in the longest path delay for stripe-type RUB's (of 0.1 cm width); the injected mobility variation is -25%. The results clearly show that some RUB's impact the circuit timing more than others. STAF empowers the designers to identify the problematic regions but it is still left to the designers to apply necessary fixes to meet the timing specifications.

Table 5.1: Mobility Change due to Inward and Outward Bending

technology	inward bending	outward bending
a-Si TFT (Gleskova et al. [2002])	-26%	7.6%
organic TFT (Sekitani et al. [2005])	20%	-30%
poly-Si TFT (Cheon et al. [2008])	44%	-44%
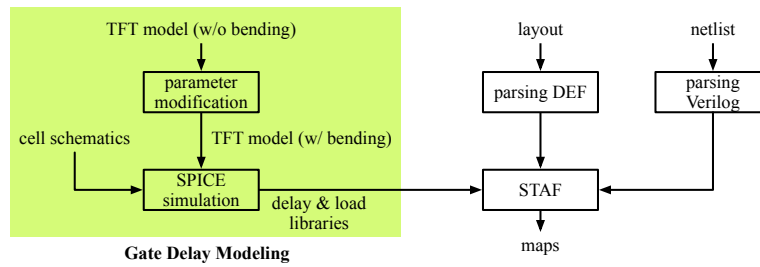
Figure 5.2: The overall STAF flow
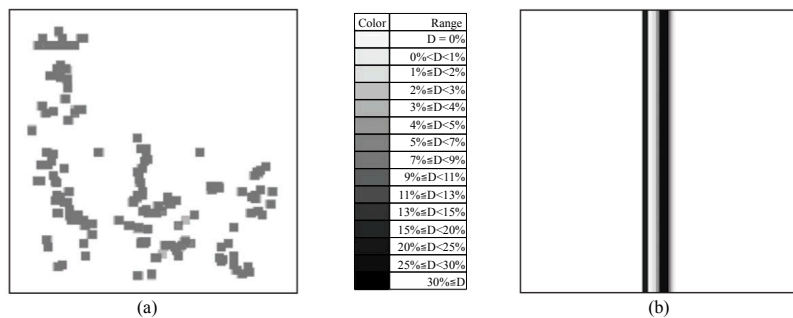
Figure 5.3: STAF simulation results: shortest path delay reduction (a) and longest path delay increase (b)
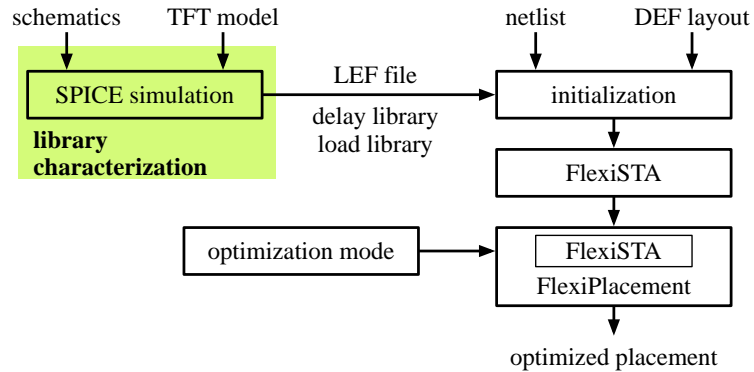
Figure 5.4: The bending-aware placement algorithm in Liu et al. [2011]

5.3 Cell Placement

Bending-aware cell placement algorithms, proposed in Liu et al. [2011], Lin et al. [2013] attempt to re-distribute the timing critical cells of a digital TFT circuit so as to reduce the possibility of bending induced timing violations.

5.3.1 FlexiPlace (Liu et al. [2011])

Figure 5.4 depicts the bending-aware placement flow proposed in Liu et al. [2011]. The first step is standard cell library characterization; the outcome includes a delay library and a load library (in library exchange format, LEF) with respect to different output load and mobility variations. In the initialization step, the circuit netlist as well as layout information (in data exchange format, DEF) are parsed. A first call to the static timing analyzer (FlexiSTA) then analyzes the circuit timing and reports the problematic regions (FlexiMap) prior to optimization.

Three optimization modes are considered in FlexiPlace: (1) *even-distribution* when all parts are equally likely to be bent, (2) *keep-in* when there is a small part, the keep-in zone, that won't be bent, and (3) *keep-out* when there is a part, the keep-out zone, that is frequently bent while the other parts won't be bent.

FlexiPlace is based on the simulated annealing algorithm. During

the annealing process, perturbation is realized by selecting two cells and swapping their locations. How the gates are selected depends on the optimization mode. Random selection is common to the three modes — two cells are randomly selected for perturbation. For the keep-in and keep-out modes, with a probability of 0.75, the heuristic will select one cell that is inside the fixed regions (the keep-in zone or outside the keep-out zone) and the other cell that is inside the potentially bent regions and on the path that causes largest increase in the critical path delay. The cost function is

$$\text{cost} = \alpha \times (\text{timing degradation}) + (\text{routing overhead}) \qquad (5.1)$$

where the weight factor α is set to 100 in their experiment and the timing degradation is the largest percentage of critical path delay increase.

Simulation results for s38417 in 20-μm OTFT technology are shown in Figure 5.5; the grey scale of each square (an RUB) indicates the induced increase of critical path delay (ICPD). In the original placement (Figure 5.5a), there are several risky high-impact RUB's (on ICPD). The even-distribution mode (Figure 5.5b) successfully redistributes the timing impact into a larger number of low-impact RUB's. On the other hand, the keep-in and keep-out modes move the high-impact RUB's into the keep-in zone (the left hand side rectangle in Figure 5.5c) or out of the keep-out zone (the center rectangle in Figure 5.5d) to remove the bending induced ICPD. For the simulated benchmark circuits, ICPD is reduced from the original 11.13% to 2.58% for the even-distribution, 0.36% for the keep-in, and 0% for the keep-out mode. The drawback is routing overhead, which on average is 24.06% for the even-distribution, 16.04% for the keep-in, and 3.43% for the keep-out mode.

5.3.2 Strain and Temperature Aware Cell Placement (Lin et al. [2013])

In addition to mechanical strain, the mobility of organic TFT's is also sensitive to temperature Zhu et al. [2005], Shin and Jang [2012]; this calls for a cell placement methodology that considers both mechanical strain and temperature variations.
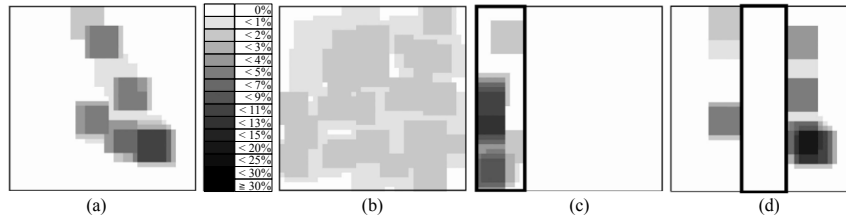
Figure 5.5: Bending induced ICPD for s38417: pre-optimization (a), even-distribution (b), keep-in (c), and keep-out (c)
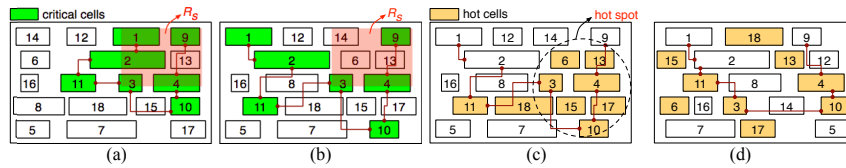
Figure 5.6: The need of temperature aware placement Lin et al. [2013]

For example, Figure 5.6a shows a typical wire-length driven placement which tends to place critical path cells (green blocks) closely; however, this placement suffers dramatic performance degradation when the region R_S is bent. A bending-aware placer like Liu et al. [2011] will evenly distribute the critical cells (Figure 5.6b); nevertheless, the resulting design may contain hot spots (Figure 5.6c) that introduce unwanted performance variations. A flexible electronics placer should consider mechanical strain and power dissipation; Figure 5.6d shows a possible placement that alleviates both the bending and temperature induced performance variations.

Figure 5.7 illustrates the bending and temperature aware placement flow in Lin et al. [2013]. It first identifies critical cells, i.e., the ones on the critical paths. The algorithm then distributes the cells to the RUB's. Distributing non-critical cells is based on K-way graph partitioning; the procedure is as follows.

1. Construct the circuit graph in which each vertex corresponds to a cell and edges correspond inter-cell interconnections. For temperature awareness, each vertex is associated with the power density of the corresponding cell.

```
┌─────────┐   ┌─────────────┐   ┌──────────────┐   ┌──────────────────┐   ┌──────────┐
│ initial │──▶│    cell     │──▶│ multi-level  │──▶│ row-based detail │──▶│ STA with │
│  STA    │   │distribution │   │global placement│  │   placement      │   │ mobility │
└─────────┘   └─────────────┘   └──────────────┘   └──────────────────┘   └──────────┘
              └──────────────── **hotspot-aware placement** ────────────────┘
```

Figure 5.7: The mechanism strain and temperature aware placement algorithm

2. Partition the graph into n subgraphs (n is the number of RUB's) with minimal cut cost (for wire length consideration) and balanced sum of vertex weights (for hotspot consideration).

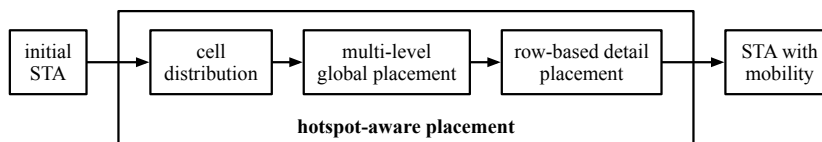For critical cells, the placer concurrently (1) distributes the ones on the same critical path evenly to the RUB's while minimizing the total wire length, and (2) maximizes the total number of non-critical cells that are assigned to the same RUB as the critical cells that they are adjacent to.

After the cell distribution, multi-level global placement is performed to determine the actual locations of each RUB with the objective of minimizing the total wire length and avoiding hotspots. Cell positions within each RUB are decided by row-based detail placement. The cells are first distributed into the available rows in each RUB considering cell connectivity as well as row capacity. Then, for temperature consideration, each cool cell is placed adjacent to a hot cell to reduce the temperature, where cells are classified as hot or cool according to their power densities.

Simulation results on ISCAS'89 benchmark circuits show that Lin et al. [2013] outperforms Liu et al. [2011] in (1) circuit performance, with 2.14 times less ICPD, (2) maximum chip temperature, with an average reduction of 17.3%, and (3) wire length, with a total half-perimeter wire length (HPWL) reduction by 23%. In their experiments, chip temperatures were obtained using the HotSpot thermal simulator HotSpot. The thermal simulation results of this work and Liu et al. [2011] are shown in Figure 5.8a and b, respectively; the two plots show significant temperature reduction by Lin et al. [2013].
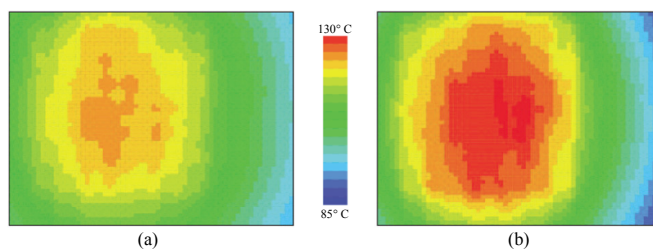
Figure 5.8: HotSpot simulation results of s38584: Lin et al. [2013] (a) and Liu et al. [2011] (b)

5.4 Manufacturing Testing

For digital CMOS circuits, full-scan is the industry standard. In a full-scan design, all flip-flops are replaced with scan flip-flops so that the automatic test equipment (ATE) can fully control and observe the flip-flips (via the shift operations) outputs to achieve a high fault coverage. In general, full-scan design and test pattern generation have been widely used and highly automated, which can also be readily applied to flexible circuits.

5.4.1 Asynchronous Scan Designs

Flexible electronics are suitable for large area applications whose clock skew problem could be much more significant than silicon CMOS due to greater differences in clock wire lengths in a circuit with a larger area. Asynchronous design is therefore an attractive solution to alleviating this problem. Various versions of asynchronous scan designs have been proposed Wey et al. [1993], Petlin and Furber [1995], Kang et al. [1999], Cheng and Li [2011]; among them, Cheng and Li [2011] was implemented and validated in an 8-μm a-Si technology.

5.4.2 Reliability Screening

The threshold voltage (V_{TH}) shift and imperfect gate nitride are two major threats to flexible circuits reliability Shen et al. [2010]. For
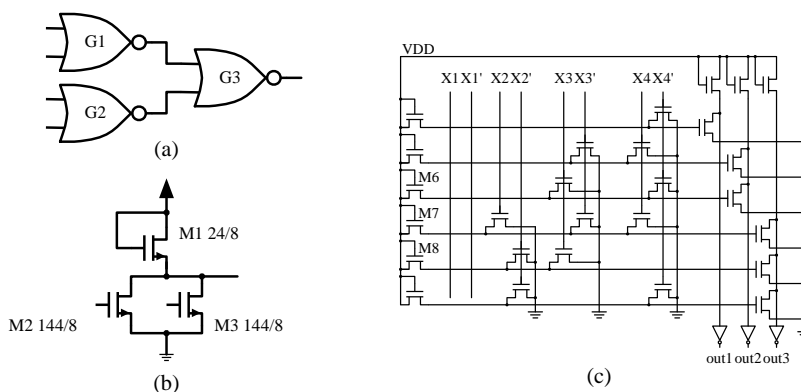
Figure 5.9: Schematics of NR3 (a), NOR (b), and M3P (c)

bulk CMOS technology, reliability screening is conducted by burning-in the circuit under test (CUT) under elevated temperature and voltage stress. However, burn-in is unsuitable for low-cost flexible circuits because it is expensive and destructive.

In Shen et al. [2010], the authors addressed the reliability screening issues of flexible circuits. They evaluated two alternate approaches to burn-in, including very-low voltage (VLV) testing and I_{DDQ} testing. (I_{DDQ} testing was shown to be ineffective and is not discussed here.) Two flexible circuit designs are implemented in 8-μm a-Si process on a glass substrate, including a pseudo-NMOS two-level NOR-NOR logic (NR3 in Figure 5.9a) and a multiplied-by-three programmable logic array (M3P in Figure 5.9c). Figure 5.9b depicts the transistor-level schematic of the NOR2 logic gate with the transistor W/L values (μm) shown.

The test flow in Figure 5.10a was applied to 140 circuit instances (70 for both designs) to validate the capability of VLV testing in capturing weak devices. The flow starts with normal voltage (pre-stress NV) followed by VLV testing. Then, a voltage stress of 30 V is applied to all CUT's for 200 seconds; the stress is expected to cause a V_{TH} shift of 1 V and not supposed to damage the CUT's. Note that post-stress NV testing is used as the golden test results.

Figure 5.10b shows the simulation results of injecting various gate
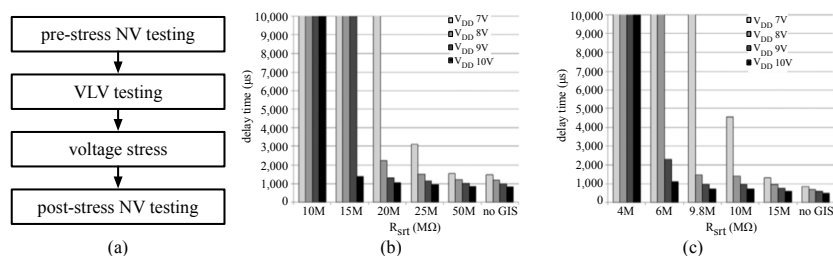
Figure 5.10: The VLV test validation flow (a) and the gate insulator shorts simulation results for NR3 (b) and M3P (c)

insulator shorts between the gate and source of the transistor M3 of gate G2 in NR3. For NV testing (V_{DD} = 10 V), there is hardly any change in delay for short resistance less than 15 MΩ. On the other hand, decreasing V_{DD} makes the changes to delay more significant. The simulation results for M3P (by injecting gate insulator short to M6) are shown in Figure 5.10c. Results for both circuits show that VLV testing is more effective than NV testing in differentiating defect-free and defective CUT's.

Figure 5.11 shows NR3 measurement results. In Figure 5.11a, each triangle represents a CUT; the x and y-axes correspond to the NV delays before and after voltage stress, respectively. (The two dash lines are the test upper bounds.) Note that there are six NV escape circuits, i.e., circuits that pass the pre-stress but fail the post-stress NV testing. In Figure 5.11b, the VLV testing results are shown — the x and y-axes correspond to the delay times of VLV testing and post-stress NV testing, respectively. The results show that VLV testing is more sensitive to defects than NV testing. This can be seen by projecting all the triangles onto the x-axis and observing that the VLV testing results spread a wider range than NV testing. VLV testing is also more effective in reliability screening — there is only one VLV escape. However, VLV testing also adversely incurs eleven overkills, i.e., circuits that pass the post-stress NV testing but fail the VLV testing.
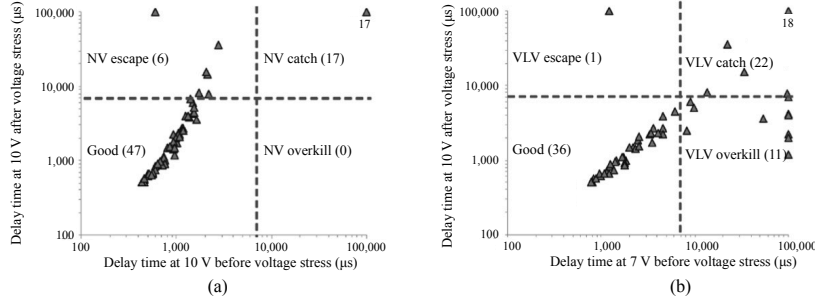
Figure 5.11: NR3 delay times before and after voltage stress for NV (a) and VLV (b) testing

5.5 Yield Optimization for Flexible Analog/Mixed-Signal Circuits

For analog/mixed-signal circuits, yield optimizing by adjusting circuit parameters, ex. device widths and lengths, is crucial to profitability.

In Antreich et al. [1994], the concept of worst case distance (WCD) is introduced to provide a quick estimate of yield. Given the nominal deterministic parameter set d_0, ex. the transistor widths and lengths, and a specification $f_i \leq B_i$, ex. power consumption, the corresponding worst case distance, denoted by $\beta_{w,i}$, is the shortest distance between s_0 and the surface $f_i = B_i$. Figure 5.12 illustrates an example with two normally distributed statistical parameters s_1 and s_2. The dashed line consists of parameter sets such that $f_i = B_i$ under the worst case operating condition $\boldsymbol{\theta}_{w,i}$; the ellipse is the tolerance body and its perimeter is an equi-probability contour. In this example, $\boldsymbol{s}_{w,i}$ is the worst case statistical parameter set for $f_i \leq B_i$ and $\beta_{w,i}$ is the distance between $\boldsymbol{s}_{w,i}$ and $\boldsymbol{s}_0$.

Based on WCD, parametric yield optimization of the circuit performance, yield, and robustness can be achieved by maximizing the worst-case distances over the nominal values of d_0 for all properties simultaneously:

$$\max_{\boldsymbol{d}_0, \boldsymbol{s}_0} \; \text{sign}\,(\alpha_i) \cdot \beta_{w,i}. \tag{5.2}$$

where $\text{sign}\,(\alpha_i)$ returns 1 if f_i is satisfied or 0 otherwise. In McConaghy
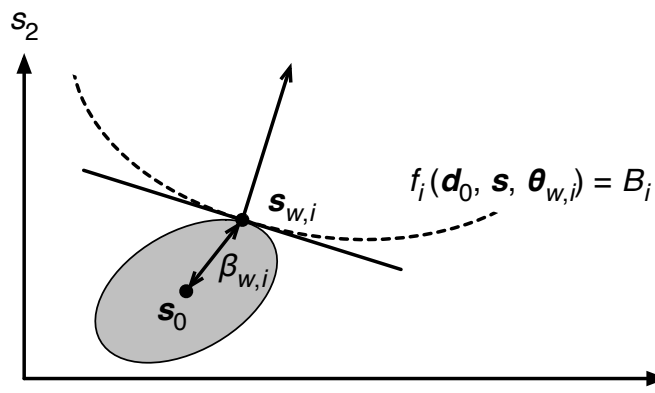
Figure 5.12: The worst case point s_i and the worst case distance β_i with respect to property f_i
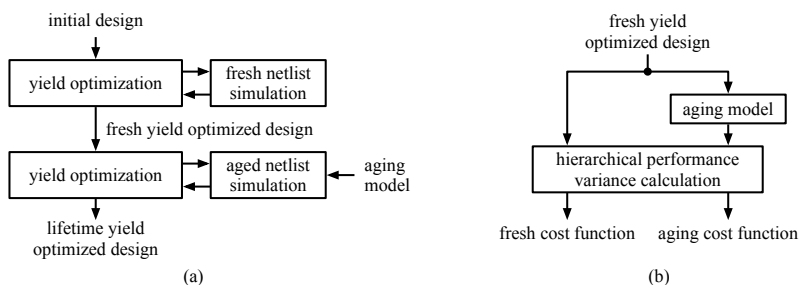
Figure 5.13: The two-stage lifetime yield optimization flow (a) and the simultaneous fresh and lifetime yield optimization flow

and Gielen [2009], the authors proposed a similar concept that uses *process capability Cpk* for yield evaluation.

In Chen et al. [2013], the authors reported a yield optimization technique for flexible circuits which takes into account the bending incurred mobility variation, in addition to the inevitable process variations. Simulation results on an operational amplifier Tarn et al. [2010] in 8-μm a-Si technology show that, under -25 to 20% mobility variation, -20 to 20% threshold voltage variation, and -3 to 3% of width and length variation, the technique is capable of achieving 100% yield.

Most yield optimization techniques consider the fresh yield, i.e., the

manufacturing yield. For flexible circuits, optimizing the fresh yield is insufficient. Due to the significant device degradation over time, lifetime yield must be considered as well to ensure product quality. In Pan and Graeb [2009, 2010, 2011], a two-stage approach, as shown in Figure 5.13a, to lifetime yield optimization for CMOS analog circuits was proposed. The technique starts from fresh yield optimization; the resulting design is optimized again for lifetime yield (using the degraded device parameters). One potential problem to this two-stage approach is that the lifetime yield optimized design may fail to meet the fresh yield requirement.

In Chen et al. [2014], the authors extended their work in Chen et al. [2013] to optimize the fresh and lifetime yields simultaneously. As shown in Figure 5.13b, this technique computes both the fresh cost function and the aging cost function which uses the exponential model proposed in Liu et al. [2009]. In the yield optimization engine, both cost functions are considered to optimize the fresh and lifetime yields concurrently. Optimization results for the same operational amplifier under the same process variations as Chen et al. [2013] are shown in Figure 5.14a where three approaches are compared: WCD_{fresh} optimizes the fresh yield, $WCD_{lifetime}$ optimizes the lifetime yield using the quadratic aging model Pan and Graeb [2010], and CSP simultaneously optimizes both yields. While WCD_{fresh} achieves 100% fresh yield, the lifetime yield at time $= 1,000$ drops to zero. The $WCD_{lifetime}$, on the other hand, achieves 100% yield at time $= 1,000$ at the cost of fresh yield loss (97.4%). The simultaneous optimization technique achieves 100% fresh and lifetime yields. The results clearly show the advantage of concurrent optimization. However, lifetime yield improvement is not without cost. Compared to WCD_{fresh}, CSP incurs 12.3% power overhead and 2.8% area overhead. Figure 5.14b shows the results for a 4-bit DAC (Tarn et al. [2010]). The CSP technique again achieves 100% fresh and lifetime yields; the power and area overheads, compared to WCD_{fresh} are 8.9% and 2.9%, respectively.
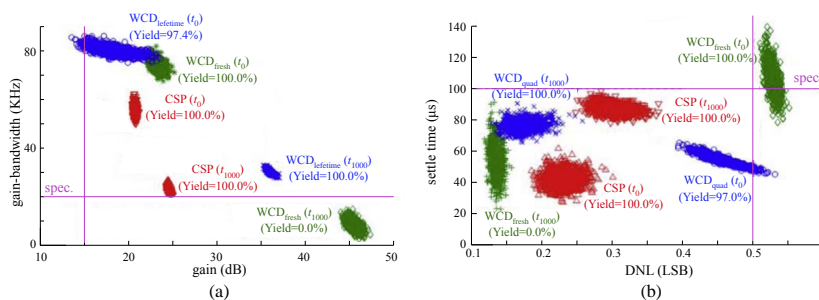
Figure 5.14: Performance distributions of the operational amplifier (a) and the 4-bit DAC (b)

5.6 Summary

As the TFT technologies advance, systems-on-panel that integrate digital and analog/mixed-signal circuits with large area displays or sensors will soon become reality. Successful deployment of these flexible electronics systems will largely rely on EDA (electronics design automation) models, tools, and methodologies.

In this chapter, research results that concern design and test automation for flexible electronics are discussed, which include timing analysis, physical design, manufacturing testing, and yield optimization. Due to the unique device characteristics and application environment, the current EDA flow and tools must be modified and enhanced to improve the flexible electronics design efficiency and quality, especially for device degradation and bending induced performance variation and reliability issues. These pioneering studies as well as their further development will play an important role in the future success of flexible electronics.

6

Reliability Simulation

According to their atomic structures and manufacturing processes, TFTs can be generally categorized into three different types: amorphous hydrogenated silicon (a-Si:H) TFTs, polycrystalline silicon (poly-Si) TFTs, and organic TFTs (OTFTs). This chapter focuses on reliability analysis of a-Si:H TFT which is chosen for this study based on the following observations: (1) it has good uniformity for large-area fabrication with relatively low cost; (2) it is mature, commercially available and also compatible with a low temperature process (ex. 200°C) used on flexible substrates such as polyimide Yeh et al. [2007]; (3) it shares many common features with the emerging ink-jetted OTFT and exhibits no significantly different characteristics on glass or flexible substrates Yeh et al. [2007]; (4) it is air-stable (i.e., stable under ambient O_2 and H_2O) while ink-jetted OTFT is still not. This alleviates the concern of chemical degradation and mainly manifests the electrical degradation phenomenon.

There have been extensive studies on the electrical instability of a-Si:H TFTs Chaji et al. [2006], Chiang et al. [1998], Huang et al. [2000], Libsch and Kanicki [1993], Powell [1983], Powell et al. [1987, 1989]. Two major mechanisms, carrier trapping and point defect creation, can

explain the phenomenon of a-Si:H TFTs' electrical instability. Carrier trapping usually occurs in the gate insulator due to material defects, while point defect creation typically occurs at or near the interface between the gate insulator and semiconductor.

As a result, these material defects cause reliability problems in the operation of flexible circuits using a-Si:H TFTs and, therefore, require careful analysis for designing more reliable flexible circuits. Particularly, transistor degradation of a-Si:H TFTs is strongly affected by the bias stress (i.e. switching activity) of an individual transistor. Different transistors can be exposed to different degrees of degradation. Therefore, the input/output characteristics of a degraded transistor could deviate from its expected behavior and further affect its neighboring transistors. This problem makes a-Si:H circuits less stable than crystalline-Si circuits and also poses great design burdens on circuit designers to ensure reliable operation throughout the expected lifetime. In this chapter, we give an overview of reliability simulation for flexible circuits based on a-Si:H TFTs. Such a simulation methodology can analyze the degradation profile for each TFT, perform reliability simulation and predict the circuit lifetime accordingly by incorporating simulation using a transient simulator such as SPICE. A scan driver circuit using a-Si:H TFTs, which is used to drive the active-matrix liquid-crystal display (AMLCD), was implemented, fabricated, and measured as a test circuit to evaluate the accuracy of the simulation results. To further assess the effectiveness of such reliability simulation as a design aid, several a-Si:H TFTs scan drivers Chen et al. [2007], Edo et al. [2006], Jang and Han [2006] were analyzed for their circuit reliability and lifetime.

6.1 Transistor Degradation

In this section, we briefly explain the physical mechanism of transistor degradation and then show an analytical model for estimating the transistor property (ex. V_{TH}) shifts under different bias-temperature-stress (BTS) conditions.

6.1.1   Electrical Degradation

The a-Si:H structure exists in a state of metastable equilibrium among weak Si-Si bonds, Si dangling bonds, and hydrogen passivated bonds. This equilibrium could be broken by applying external energy such as prolonged gate bias which results in more dangling bonds. This degradation process, fortunately, is reversible by annealing and the dangling bonds can be passivated by hydrogen mediation Kuo [2004]. For a-Si:H TFTs, the mechanisms responsible for electrical instability are: (1) carrier trapping under the higher positive-bias and negative-bias regimes; and (2) point defect creation under the lower positive bias regime. Carrier trapping occurs in the gate insulator, the a-SiNx:H layer, and arises from the high density of material defects generated during the deposition process such as Plasma-Enhanced Chemical Vapor Deposition (PECVD). The magnitude of ΔV_{TH} due to this carrier trapping mechanism has a strong dependence on the nitrogen composition of the a-SiNx:H thin film layer. On the other hand, point defect creation occurs in the semiconductor a-Si:H layer, at or near the interface, between the gate insulator and the semiconductor layers. These defects are bias-induced dangling bonds and the ΔV_{TH} attributed to this mechanism has dependence on the defect density. The higher defect density causes V_{TH} to shift toward the positive direction while an opposite effect on V_{TH} can be observed if the defect density is reduced in the a-Si:H layer.

On the other hand, the annealing process of an a-Si:H TFT, which takes place during the off-state of the TFT operation, helps recover the degraded TFT characteristics (ex. V_{TH} & V_{FB}) to a certain degree. This also explains that TFTs in the pixel circuits of AMLCD have a much longer lifetime than those TFTs used in scan drivers, since the fraction of active time of a pixel TFT is normally less than 1% of the total operating period of a display panel. Therefore, TFTs in AMLCD have much better chances to recover from bias-induced degradation. In addition, TFTs in AMLCD act as independent switches controlling the transmissive light intensity from the backlight modules to human eyes, which implies that the degraded TFTs have negligible influence on the neighboring TFTs and the pixel circuit achieves high reliability
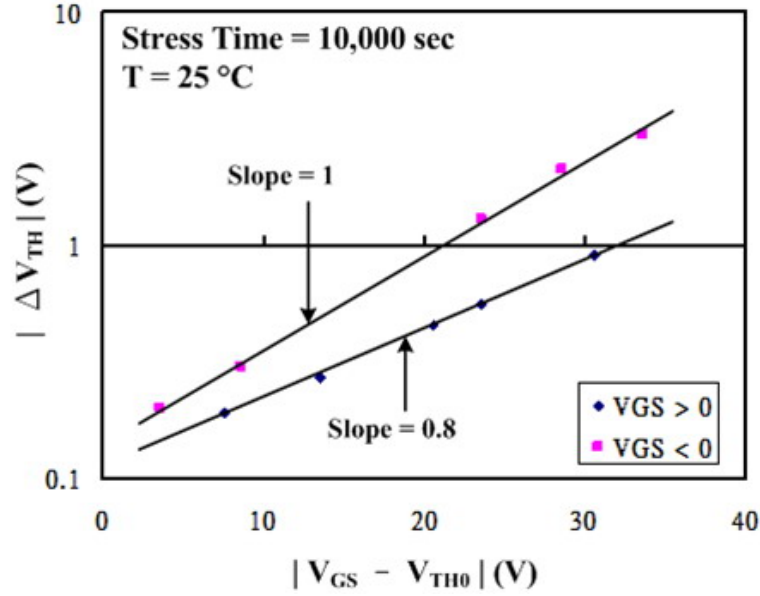
Figure 6.1: ΔV_{TH} as a function of stress voltage $|V_{GS} - V_{TH0}|$.

throughout the expected lifetime.

6.1.2 Analytical Model of ΔV_{TH}

Empirically, the magnitude of ΔV_{TH} can be estimated by a stretched-exponential function Chiang et al. [1998] shown as:

$$|\Delta V_{TH}| = |\Delta V_{eff}| \cdot \left\{ 1 - \boldsymbol{exp}\left[-\left(\frac{t_{ST}}{\tau}\right)^{\beta}\right]\right\} \tag{6.1}$$

where ΔV_{eff} is approximately the effective voltage drop across the gate insulator; t_{ST} is the effective stress time; τ is a temperature-dependent time constant; and β is a stretched-exponential exponent. The measurement results in Figure 6.1 show ΔV_{TH}'s power-law dependence on ΔV_{eff} ($=|V_{GS} - V_{TH0}|$), which can be described in Equation 6.2:

$$|\Delta V_{TH}| \propto |V_{GS} - V_{TH0}|^{\alpha} \tag{6.2}$$

where V_{TH0} is the initial threshold voltage and α is a process-dependent exponent. This observation is consistent with the results reported in

Chiang et al. [1998], Huang et al. [2000], Powell [1983]. For negatively pulsed V_{GS}, ΔV_{TH} exhibits pulse-width dependence and can be explained by the effective carrier concentration at the interface between the insulator and the semiconductor layers Chiang et al. [1998]. Taking into account this pulse-width dependence in a negative V_{GS} scheme, Equations 6.1 and 6.2 can be further combined to generate a more comprehensive model:

$$\begin{aligned}
\Delta V_{TH}(t) =& \Delta V_{TH}^{+}(t) - \Delta V_{TH}^{-}(t) \\
=& |V_{GS+} - V_{TH0}|^{\alpha+} \cdot \left\{ 1 - \boldsymbol{exp}\left[-\left(\frac{t \cdot D_c}{\tau^+}\right)^{\beta+} \right] \right\} \\
& - |V_{GS-} - V_{TH0}|^{\alpha-} \cdot \left\{ 1 - \boldsymbol{exp}\left[-\left(\frac{t \cdot (1 - D_c)}{\tau^-}\right)^{\beta-} \right] \right\} \cdot f(PW)
\end{aligned}$$

$$(6.3)$$

where t is total operation time; D_c is the duty-ratio of the bias pulses; $t \cdot D_c$ represents the effective bias-stress time for the positively pulsed bias-stress; $t \cdot (1 - D_c)$ represents the effective bias-stress time for the negatively pulsed bias-stress; the minus sign between positive and negative $\Delta V_{TH}(t)$ reflects the fact that V_{TH} shifts in opposite directions for positively and negatively pulsed bias-stress; $f(PW)$ is a function characterizing the pulse-width dependence under negatively pulsed bias. The techniques of calculating the effective bias-stress in the irregular waveforms derived from SPICE simulation will be discussed in Section 6.2. In Equation 6.3, it should be noted that only V_{GS} dependence was described and characterized. This characterization is adequate for the TFT operation in the pixel circuits of the AMLCD, since V_{DS} is kept at a fixed value for most of the AMLCD operational time Chiang et al. [1998], Libsch and Kanicki [1993], Powell [1983]. To further characterize ΔV_{TH} for typical circuit operations (ex. a scan driver), this model needs to be extended to include the dependence on V_{DS}. Based on the transistor measurement results in Figure 6.2, a formula was derived to fit the measurement data, which showed that under positive V_{GS},
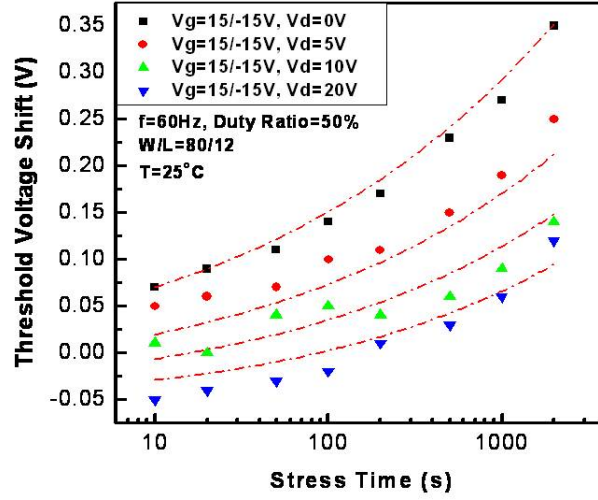
Figure 6.2: ΔV_{TH} as a function of drain voltage V_{DS} and stress time.

ΔV_{TH}^{+} (t) can be expressed as:

$$\Delta V_{TH}^{+}(V_{GS+}, V_{DS}, t) = \Delta V_{TH}^{+}(V_{GS+}, t) \cdot f^{+}(V_{DS}) \tag{6.4}$$

$$f^{+}(V_{DS}) = \frac{2}{3} \cdot \frac{(V_{GS+} - V_{TH0})^3 - (V_{GS+} - V_{DS} - V_{TH0})^3}{(V_{GS+} - V_{TH0})^2 - (V_{GS+} - V_{DS} - V_{TH0})^2} \tag{6.5}$$

$$\cdot (V_{GS+} - V_{TH0})^{-1}$$

where $f^{+}(V_{DS})$ represents the dependence on V_{DS} under the positive V_{GS} regime. On the other hand, for the negative V_{GS} regime, $V_{TH}^{-}(t)$ can also be expanded from Equation 6.3 by incorporating the dependence on V_{DS} and the pulse width as:

$$\Delta V_{TH}^{-}(V_{GS-}, V_{DS}, PW, t) = \Delta V_{TH}^{-}(V_{GS-}, PW, t) \cdot f^{-}(V_{DS}) \tag{6.6}$$

$$f^{-}(V_{DS}) = 1 + \frac{V_{DS}}{2 \cdot (V_{TH0} - V_{GS-})} \tag{6.7}$$

Based on Equations 6.1 through 6.7, a comprehensive analytical model can be expressed as:

$$\Delta V_{TH}(V_{GS}, V_{DS}, PW, t)$$

$$= |V_{GS+} - V_{TH0}|^{\alpha+} \cdot \left\{ 1 - \boldsymbol{exp}\left[- \left(\frac{t \cdot D_c}{\tau^+}\right)^{\beta+} \right] \right\} \cdot f^+(V_{DS})$$

$$- |V_{GS-} - V_{TH0}|^{\alpha-} \cdot \left\{ 1 - \boldsymbol{exp}\left[- \left(\frac{t \cdot (1 - D_c)}{\tau^-}\right)^{\beta-} \right] \right\} \cdot f(PW) \cdot f^-(V_{DS})$$

$$(6.8)$$

where temperature-dependent terms are involved in τ^+ and τ^-. All curve-fitting parameters (α, β, τ) are process-dependent and should be characterized accordingly for different manufacturing processes.

6.2 Reliability Simulation

Reliability analysis is required to help designers identify transistors that could be subject to significant degradation and predict performance of those degraded circuits. Based on the analytical model described in Section 6.1, the degradation profile of each individual TFT can be calculated and iterative SPICE simulations can also be performed for mimicking physical degradation mechanisms.

6.2.1 Existing Reliability Simulation Tools and Limitations

Reliability simulation tools such as Cadence Virtuoso UltraSim and Mentor Graphics Eldo Cadence [2007], Karam et al. [2000] have been widely available for simulating circuit reliability of nano-scale CMOS due to HCI/NBTI degradation. These tools, originated from the BERT (Berkeley Reliability Tool) Tu et al. [1993], use the Age parameter modeling concept. The model parameters for fresh and pre-stressed devices can be extracted from device characterization using parameter analyzers. The Age parameter can be calculated using interpolation and extrapolation from a table of pre-stressed device parameters. With the aged model parameters for all devices in a circuit, SPICE-like circuit

simulators can predict the circuit lifetime with high accuracy and compare the waveforms of the fresh and degraded circuit accordingly.

The $I_{SAT}/\Delta V_{TH}$ due to HCI/NBTI for CMOS, however, does not have the same strong dependence on operational conditions as a-Si:H TFTs. In addition, the correlation of $I_{SAT}/\Delta V_{TH}$ between neighboring transistors is negligible for CMOS. For these reasons, the reliability simulation tools designed for nano-CMOS are not suitable for flexible circuits. On the other hand, in order to reduce the long simulation time due to the multi-step iterative nature of BERT-like reliability simulators, an integrated environment using AHDL for a-Si:H TFT was proposed GadelRab et al. [1995], Gadelrab and Barby [1998]; however, this environment is not SPICE-compatible and the accuracy of this method is still a matter of concern. As a result, neither of these reliability simulators could meet the needs. In the following, we describe a methodology for simulating the reliability of flexible circuits which takes advantage of the high accuracy of these BERT-like tools.

6.2.2 Effective Pulse Formation

For the transistor measurement environment, we can apply ideal pulses to transistor terminals and extract the required parameters accordingly; however, in the real circuit operation, the bias-stress waveforms applied to each transistor terminal are often irregular. Therefore, how to calculate and convert these irregular waveforms into effective pulse-widths and voltages for Equation 6.8 becomes an important factor that can significantly affect the accuracy of ΔV_{TH} calculation.

The charge-trapping mechanism that causes TFT degradation (ex. ΔV_{TH}), depends on the energy levels and quantities of electron charges transported in the channel layer. Therefore, a simple, yet effective way to estimate this phenomenon is to calculate the total effective area of bias-voltage-and-time waveforms in SPICE transient simulation. In Figure 6.3, areas A, B, and D are considered effectively positive bias areas, while area C is considered an effectively negative bias area for estimating the charge-trapping and de-trapping phenomena. Here, $V_{GSP-EFF}$ and $V_{GSN-EFF}$ represent the effective peak voltages
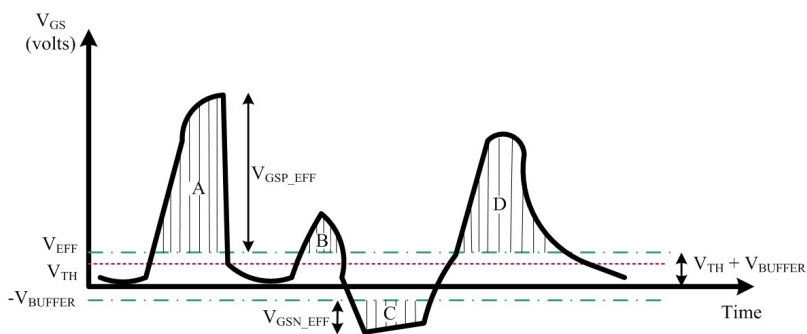
Figure 6.3: Example voltage waveform of calculating effective bias-stress for each TFT

for positive and negative bias-stress. V_{BUFFER} represents the regime in which the TFT just starts to conduct current with low-energy electrons, and its voltage level depends on the magnitude of $V_{GSP-EFF}$ and $V_{GSN-EFF}$. The total effective pulse-widths and average pulse-voltages that will be used in Equation 6.8 can then be derived, as in Figure 6.3.

6.2.3   Simulation Flow

A methodology for reliability simulation of TFT circuits is summarized in Figure 6.4. The control console acts as an external pre- and post-processor for the SPICE-like simulator (ex. HSPICE). The internal component device analyzer in the control console selects an appropriate analytical model for ΔV_{TH} and its fitting parameters for each transistor based on the pre-stressed device characterization and its input patterns. It also collects data from the transient output extractor for calculating effective bias-stress time (ex. total pulse widths) and bias voltages (ex. V_{GS}, V_{DS}) for each transistor and then computes ΔV_{TH} degradation accordingly. The component optimizer, which plays a central role in the data processing flow, is designed for performing time-series analysis of V_{GS} and V_{DS} in Equation 6.8 for each transistor and, based on this analysis, for predicting the future values accordingly for next SPICE run. The time-step between two consecutive SPICE runs can
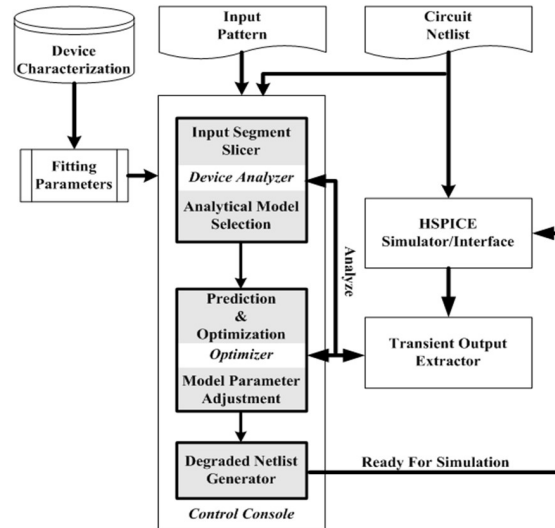
Figure 6.4: Methodology of reliability simulation

be adaptive and maximized to reduce required total simulation time. More importantly, the prediction error can be well controlled under predefined error boundaries. Finally, the optimizer collects information of each transistor degradation profile and then the degraded netlist generator generates the netlist of a degraded circuit instance, including degraded model parameters for each transistor. The degraded netlist is then used in the next run of SPICE transient simulation in the Age domain. This process repeats until a specified time stamp is reached. It should be noted that the operational condition for each transistor is assumed to be unchanged during each SPICE run of short-period (ex. 5ms) transient simulation.

6.2.4 Test Case: Scan Driver Circuit

A single module of a scan driver used for the AMLCD is shown in Figure 6.5. An experimental circuit consisting of eight such modules serially connected was implemented for a case study. A scan driver is typically designed with a 60Hz scanning signal, which scans the TFT pixel array of AMLCD one-line-at-a-time to sequentially turn on each
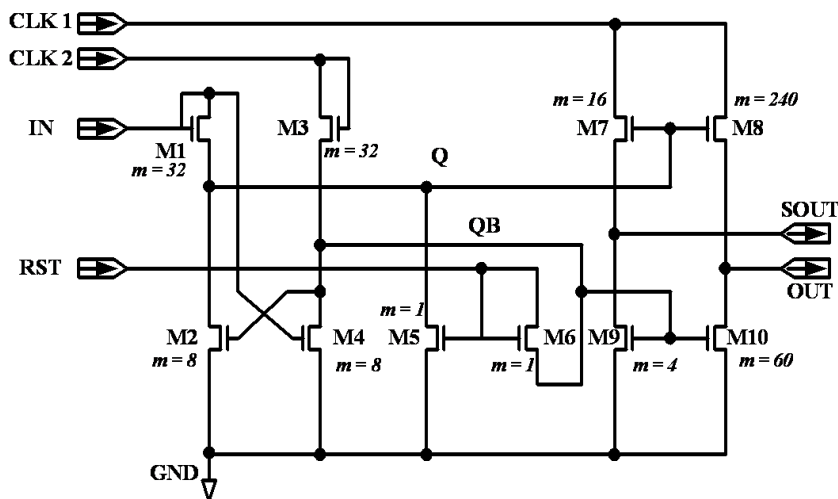
Figure 6.5: One of eight modules in the scan driver (test chip)

horizontal scan line. Based on the aforementioned methodology, BTS information for each transistor is used for calculating ΔV_{TH} profiles. The derived ΔV_{TH} profiles from modules 1 to 5 are shown in Figure 6.6. The analysis reveals that M2, M9 and M10 are the most degraded TFTs. The reason is straightforward - these transistors are directly connected to CLK2 and continuously operated under pulsed bias-stress. Figure 6.6 shows that the ΔV_{TH} of the most degraded transistors exceeds nine times of their initial V_{TH} in this case (V_{TH0}=1.41V) and can significantly deteriorate the functionality of the scan driver. This reliability simulation indicates that the scan driver circuit shown in Figure 6.5 requires modifications in order to ensure reliable operations throughout the desired lifetime.

6.3   Simulation Time Reduction

The methodology described in Section 6.2 attempts to mimic the physical degradation process of bias-stressed TFTs; however, due to strong correlations of ΔV_{TH} between neighboring transistors, the degradation simulation inevitably requires running a circuit simulator, such as
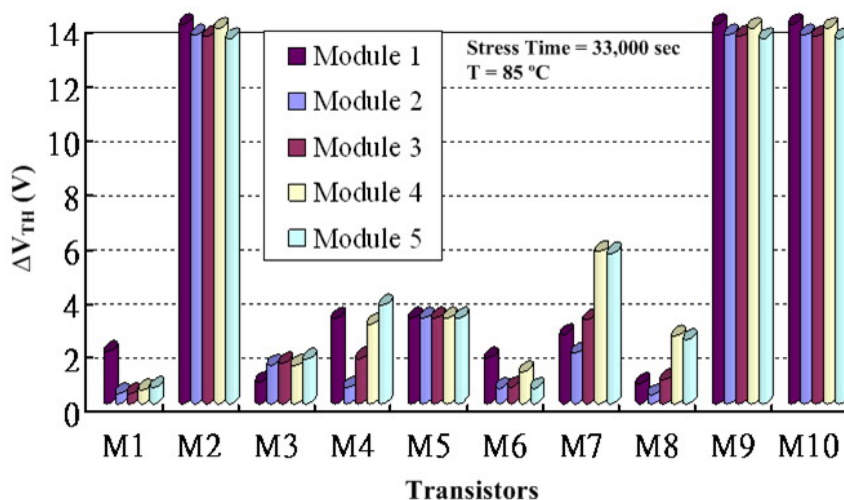
Figure 6.6: ΔV_{TH} profiles of individual transistors in the first five modules

SPICE, iteratively. The large number of iterations and long SPICE simulation time for each iteration make such a method expensive. Hence, it is necessary to minimize the number of required SPICE runs to make such an approach practical. A simulation time reduction algorithm based on time-series analysis to minimize the number of required iterations was discussed in Huang et al. [2008].

6.4 Experimental Results

To assess the accuracy of the methodology and analytical models described above, the output waveforms of SPICE simulation and actual stressed-circuit measurements are compared. It should be noted that simply comparing the ΔV_{TH} with respect to the stress time cannot reflect the complete picture because ΔV_{TH} is not the only degraded transistor parameters. The experimental circuit used for evaluation is the scan driver with eight modules, as shown in Figure 6.5.

6.4.1   Waveform Comparison

Unstressed Circuit

Based on the analytical model, we analyzed ΔV_{TH} profiles for the scan driver circuit and simulated a degraded circuit accordingly. To get a quick assessment of circuit degradation, simulation was performed without the extraction of layout-related parasitics and thus the layout-related noise/crosstalk was neglected. We first evaluated the circuit that has never been stressed before (i.e. in the very beginning of its life cycle). The comparison of the simulation and actual measurement results is shown in Figure 6.7. We observed in Figure 6.7(a) that the simulation successfully identifies some undesirable signal spikes in the simulation waveforms, which also appeared at the same locations in the measurement waveforms of Figure 6.7(b). These undesirable spikes identified by the simulation, shown in Figure 6.7(a), are due to the signal currents from CLK1 through M8 (Figure 6.5), which has a larger size. Other signal spikes in Figure 6.7(b) which do not appear in Figure 6.7(a) are mainly due to certain layout-related parasitics that were not accurately considered in the pre-layout SPICE simulation.

Stressed Circuit

With continuous bias-stress on the test circuit, we observed in Figure 6.8 that the signal spikes that also appeared in Figure 6.7 became more significant in both amplitudes and widths. These expanded spikes could cause malfunction of the AMLCD and are mainly due to a large ΔV_{TH} increment of M2 (Figure 6.5) under the considerable bias-stress. In the normal circuit operation, CLK2, which is activated right after CLK1, should be able to switch on M2 and pull the voltage level of Q to be low; however, with significant ΔV_{TH} of M2, the voltage level of Q is stuck at high and cannot be pulled down to low. This results in malfunction of M8, which relies on the voltage level of Q to switch on/off the signal current from CLK1. This phenomenon was successfully predicted by SPICE simulation, as shown in Figure 6.8(a). We observed

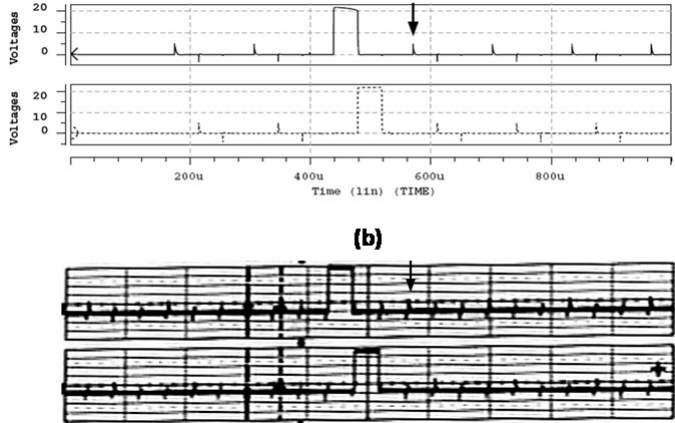**Figure 6.7:** Comparison of output waveform from the first two modules of an unstressed circuit: (a) SPICE simulation; (b)actual measurement (the scale is 5V/div(vertical) and 100 μs/div (horizontal))
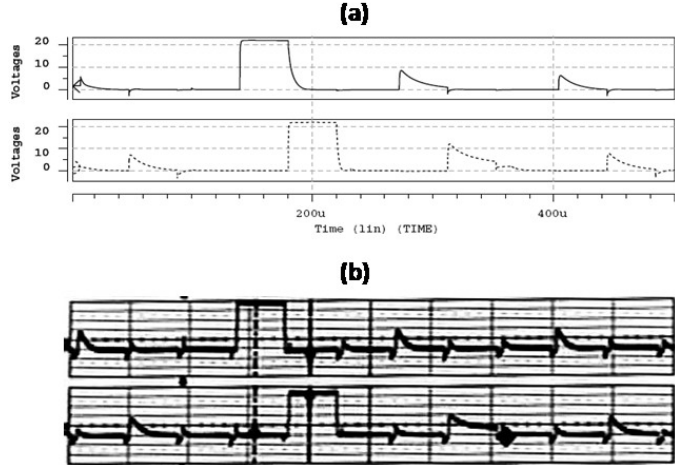

Figure 6.8: Comparison of output waveform from the first two modules of the stressed circuit for 33,000 sec: (a) SPICE simulation; (b)actual measurement (the scale is 5V/div(vertical) and 50 μs/div (horizontal))

highly consistent results between the simulation and actual measurement in Figures 6.8(a) and (b). In the case of Figure 6.8, the stress time (=33,000 sec) is the point at which the circuit might accidentally turn on the pixel circuit of the AMLCD due to excessively expanded output signal spikes. In the simulation results shown in Figure 6.8(a), the extrapolation techniques have been applied for predicting BTS conditions of individual transistors. This predicted BTS information (ex. average V_{GS}) for each SPICE run is then used to generate ΔV_{TH} accordingly.

6.5   Summary

In this chapter, we elaborate the reliability issues and a reliability modeling and analysis framework for hydrogenated amorphous silicon (a-Si:H) TFT circuits. After illustrating the degradation mechanisms, we describe device modeling and simulation methodologies, followed by assessment of their accuracy using measurement data. While the framework should be applicable to a wide range of TFT technologies including organic and metal-oxide TFTs, this chapter limits the discussion on a-Si:H TFT circuits which is the most mature TFT technology with well-developed process control and trustworthy device models.

While there have been several viable design techniques available to mitigate degradation of a-Si:H TFT circuits Edo et al. [2006], Jang [2006], Jang and Han [2006], Chen et al. [2007], most of them have only been demonstrated for special types of circuits such as integrated display drivers. For applications in which other types of TFT circuits are under prolonged bias-temperature-stress (BTS), there are still significant room, ranging from materials, devices, to circuits, for reliability improvement.

7

Flexible Photovoltaics

Solar cells and solar photovoltaic generation systems are utilizing photovoltaic effects to convert solar energy into electricity. The photovoltaic effect was first discovered by the French physicist Alexandre-Edmund Becquerel in 1839 and the first solar cell was made by the American inventor Charles Fritts in 1883 using Selenium (Se) with only 1% conversion efficiency. The modern silicon-based solar cell was first developed by D.M. Chapin of Bell Labs in 1954 with 6% efficiency using P-N junctions. In this chapter, we give a brief introduction to the second generation thin-film photovoltaic technologies such as a-Si, CdTe, and CIGS solar cells, and the third generation organic and plastic solar cells on flexible substrates. The physics and process details of these photovoltaic technologies are beyond the scope of this chapter and can be found in related literatures.
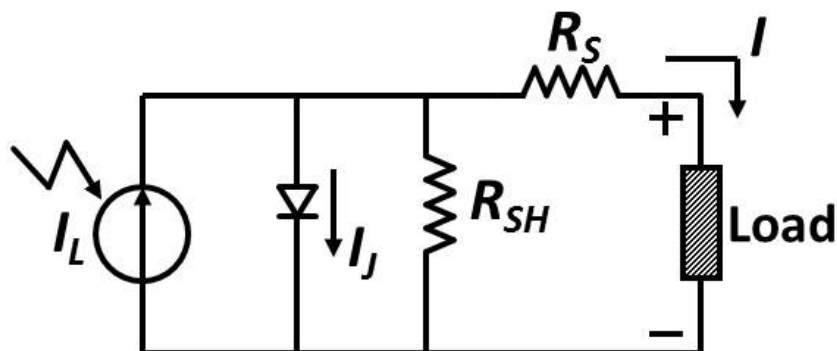
Figure 7.1: The equivalent circuit of a solar cell

7.1 The Basic Principle

7.1.1 Equivalent Circuit

The equivalent circuit of a solar cell is shown in Figure 7.1, where I_L is the light-induced current, I_J is the junction current, I is the load current, and V_J is the junction voltage. Equations 7.1 and 7.2 show the relationship of the load current, junction voltage and temperature:

$$I = I_L - I_J \tag{7.1}$$

$$= I_L - I_0(e^{\frac{qV_J}{kT}} - 1) \tag{7.2}$$

where q is the charge of an electron, I_0 is the reverse bias saturation current, and T is the junction temperature. Further taking into account the parallel resistance R_{SH} and the series resistance R_S in an actual solar cell due to parasitic resistance, the load current can be expressed by Equation 7.3 as below:

$$I = I_L - I_0[e^{\frac{q(V_J+IR_S)}{AkT}} - 1] - \frac{V_J - IR_S}{R_{SH}} \tag{7.3}$$

where A is a curve fitting parameter.

7.1.2 Band Diagram and IV Curve

Figures 7.2 and 7.3 show the band diagram of the P-N junction and the IV curve of a solar cell. As shown in Figure 7.2, the photon-induced electron-hole pair generates a current flow if connected with a load to form a closed loop. When a solar cell is in a dark environment without sunlight, and current-to-voltage (IV) relationship is similar to a diode, shown as curve *b* in Figure 7.3. On the other hand, its IV curve under the sunlight is different, illustrated by curve *a* where I_{SC} is the short-circuit current, and V_{OC} is the open-circuit voltage. When a load resistance is present, the shaded area in Figure 7.3 illustrates the relationship between output current and voltage with a linear load resistance, where V_m and I_m are the maximum output voltage and current respectively. The fill-factor (FF) of a solar cell therefore can be defined in Equation 7.4 as:

$$FF = \frac{V_m I_m}{V_{OC} I_{SC}} \tag{7.4}$$

The conversion efficiency η of a solar cell under the sunlight is defined as:

$$\eta = \frac{P_m}{P_{in}} \tag{7.5}$$

$$= \frac{FF \cdot V_{OC} \cdot I_{SC}}{P_{in}} \tag{7.6}$$

where FF is the fill-factor, P_m is the maximum output power that equals to the product of the maximum voltage V_m and the maximum current I_m, and P_{in} is the incident solar power to the solar cell. The conversion efficiency depends on the material properties as well as the device structure of the solar cell, which can range from less than 10% for an organic solar cell to greater than 20 % for a crystalline-silicon solar cell.

7.2 Silicon Solar Cell

The cost per watt of crystalline-silicon solar cells used to be in the range of a few tens of dollars. With the advances of manufacturing technolo-
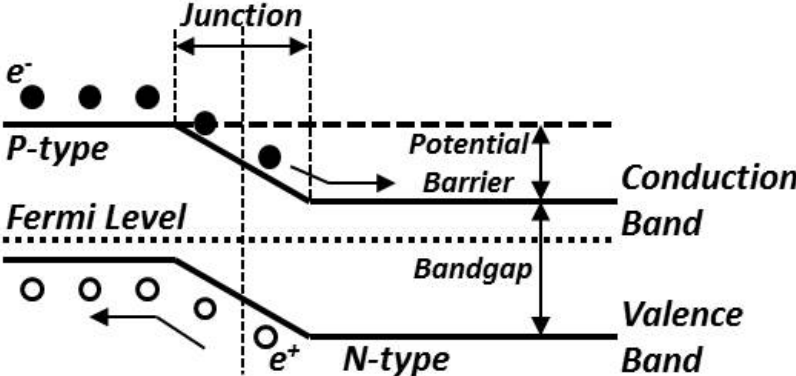
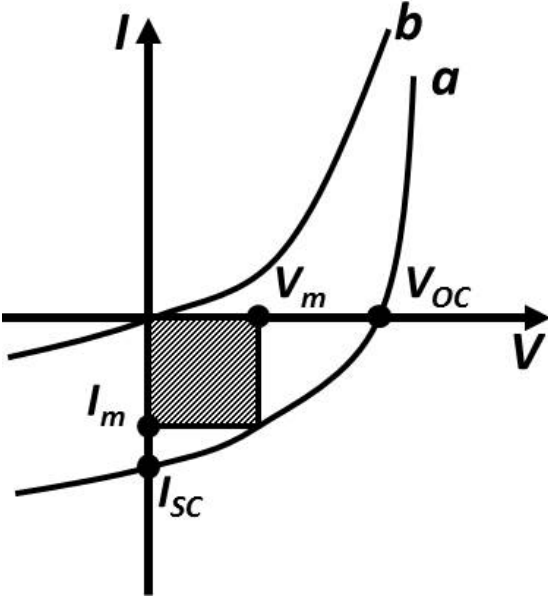**Figure 7.2:** The band diagram of a P-N junction solar cell

Figure 7.3: The IV Curves of a solar cell with and without sunlight

gies, the cost per watt has dropped significantly and now reaches as low as five dollars. However, due to the relatively high cost of material and manufacturing process, it is challenging to further reduce the cost per watt for crystalline-silicon solar cells to the level of, say, less than one dollar per watt. Amorphous silicon solar cells, which have many benefits including low manufacturing cost, high absorption coefficient to solar energy, and environmental safety, are considered a viable candidate for driving further cost reduction.

7.2.1 Amorphous Silicon (a-Si) Solar Cell

Amorphous silicon (a-Si), compared with crystalline silicon (c-Si), has many advantages for making solar cells. The manufacturing process of a-Si solar cells is relatively simple and inexpensive, and for the same layer thickness, the a-Si structure can absorb 10X or more solar energy than c-Si in the visible light spectrum because of its wider bandgap. Much less material ($\sim$ 1%) is therefore required for a-Si thin-films, resulting in lighter and cheaper a-Si cells than their c-Si counterparts. However, due to a large number of dangling bonds in the a-Si structure that can be attributed to the fabrication process of a-Si thin-films using Silane (SiH_4) gas, the recombination rate of light-induced electron-hole pairs is much higher than that in c-Si or poly-Si structures. This characteristic inevitably lowers the collectable photo-currents as well as the conversion efficiency of a-Si solar cells. Based on a low-temperature ($< 300°C$) chemical vapor deposition (CVD) process, an a-Si thin-film can be deposited on a wide range of substrates, including plastic films and metal foils. This advantage makes light-weight and flexible a-Si solar cells widely adapted as a portable charger.

The device structure of a triple-junction amorphous silicon solar cell is shown in Figure 7.4. The high electric-field generated by the p-type and n-type a-Si thin-film layers in Figure 7.4 can separate the incident-light generated electron-hole pair in the intrinsic a-Si layer. This effectively reduces the recombination rate of the electron-hole pair and therefore improves the conversion efficiency. To further enhance the light-absorption and conversion efficiency, a multiple junction tandem
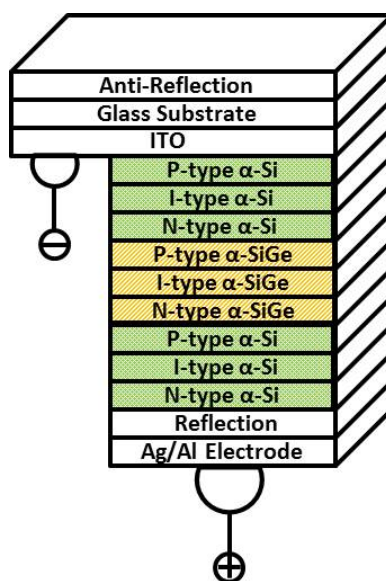
Figure 7.4: The device structure of an amorphous silicon (a-Si) solar cell.

structure in which multiple layers are stacked together, as shown in Figure 7.4, is a popular choice Yang et al. [1997], Soderstrom et al. [2012], Schuttauf et al. [2014]. Commercial a-Si solar cells with double and triple-junction tandem structures can reach conversion efficiency of 7% and 8% respectively. However, this approach is not applicable to c-Si solar cells because the thick c-Si cells become opaque to the incident light if stacked together.

a-Si solar cells are inferior to c-Si solar cells in a couple of aspects. In addition to lower conversion efficiency ($\sim 10\%$ v.s $\sim 20\%$ for c-Si), a-Si solar cells incur a significant decline in efficiency during the first few hundred hours of illumination. This efficiency decline is called Staebler-Wronski effect Wronski [1977] whose root cause can be attributed to the increase of the defect density with light soaking. The illumination provides sufficient energy required to push hydrogen away and creates dangling bonds. These dangling bonds will then capture the electrons created by photons and cause a decline in the efficiency. After about 1,000 hours of steady illumination, the efficiency decline in an a-Si solar cell will reach a steady state.

A flexile thin-film photovoltaic harvesting system is proposed in Rieutort-Louis et al. [2014] which includes a-Si solar cells, a thin-film battery, thin-film power management circuitry, and contact-less power delivery. This exemplar system which integrates $240cm^2$ flexible a-Si solar cells with 240 $\mu W/cm^2$ efficiency can generate DC power around 1mW and ac power around 10mW.

7.3 Compound Semiconductor Solar Cell

Compound semiconductor solar cells utilize II-VI or III-V direct-bandgap semiconductors such as Gallium-Arsenide (GaAs), Cadmium Telluride (CdTe), Copper Indium Gallium Selenide (CIGS) to absorb the photons from the incident light and generate photo-currents. The bandgap of these materials is around 1 to 1.6 eV, which matches well with the solar spectrum and can therefore absorb most of the solar energy with a thin-film layer of only a few nanometer thickness. The material cost can thus be minimized with adequate conversion efficiency. It is therefore considered as a strong candidate to realize the next-generation photovoltaics generation system with the promise of reducing the cost per watt to less than one dollar.

7.3.1 Cadmium Telluride (CdTe) Solar Cell

The Cadmium Telluride (CdTe) solar cell, a hetero-junction device, was first developed by RCA in 1956 with 2% conversion efficiency. In 1963, Dr. Cusano Cusano [1963] in GE created a hetero-junction solar cell with Cadmium Telluride (CdTe) and Copper Telluride (Cu_2Te), and reported 6% conversion efficiency. The CdTe thin-film is a p-type semiconductor that has direct bandgap ($1.44 \sim 1.45$ eV) matching well to the distribution of photons in the solar spectrum in terms of optimal conversion to electricity. It serves as an absorber layer and has high light-absorption coefficients. Its conversion efficiency can therefore reach $10 \sim 15$ % with theoretical efficiency up to 30%. The key merits of CdTe thin-films include compatibility of the large-area deposition with a fast deposition rate. Because of high conversion efficiency and low

manufacturing cost, currently CdTe photovoltaics is the only technology employed in multi-kilowatt generation systems that can achieve a cost per watt lower than that of crystalline-silicon photovoltaics. It also accounts for more than half thin-film solar cells market in 2013. The prominent CdTe photovoltaics manufacturer, *FirstSolar*, has recently reported its module efficiency reaching 17% and device efficiency reaching 21%. A recent literature Gloeckler et al. [2013] also shows record-high 19% efficiency and suggests a near-term target of $19 \sim 22$ %.

There are two different device structures for CdTe solar cells: superstrate and substrate. Figure 7.5 shows the PN junction device structure of a superstrate CdTe solar cell that is made under a $300 \sim 500 \ ^{\circ}C$ process temperature. Because of its better conversion efficiency, most CdTe solar cells are based on the superstrate structure and the CdTe thin-film can be made by deposition, screen printing, or sputtering. To date, the typical efficiency is around $10 \sim 15\%$ for a CdTe solar cell and around $8 \sim 13$ % for a CdTe solar module.

There are, however, some safety concerns regarding CdTe solar cells. First, Cadmium itself is considered as a hazardous heavy-metal waste. In addition, in order to increase the cell's overall conversion efficiency, a thin-layer coating uses toxic Cadmium Chloride ($CdCl_2$) during the manufacturing process. To ease the concerns, commercial CdTe solar cells usually have glass plates surrounding CdTe materials that prevent CdTe from release even during a fire.

7.3.2   Copper Indium Gallium Selenide (CIGS) Solar Cell

The Copper Indium Gallium Selenide (CIGS) is a I-III-VI$_2$ semiconductor material that has direct bandgap of $1.02 \sim 1.68$ eV, whose exact value is dependent of the ratio of Indium to Gallium. CIGS has an exceptionally high absorption coefficient of 10^5/cm for 1.5eV of higher energy photons. Mainly used as a polycrystalline thin-film, a CIGS solar cell has recently reached 20% conversion efficiency, claimed by U.S. National Renewable Energy Laboratory (NREL), which is the current world record for any types of thin-film solar cells.

Figure 7.6 shows the CIGS solar cell structure. The Molybdenum

Incident Light

Glass Substrate

Transparent Conductive Oxide (SnO2:F)

N-type Cadmium Sulfide (CdS)

P-type Cadmium Telluride (CdTe)

Buffer Layer (Zn$_2$SnO4)

Contact Electrode

Metal Substrate
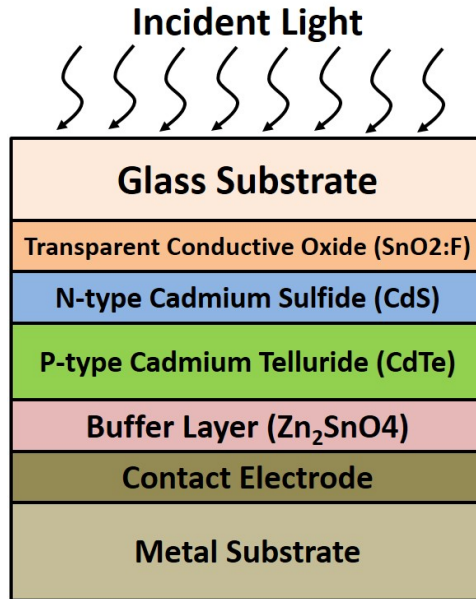
Figure 7.5: The device structure of a superstrate CdTe solar cell

Incident Light

Ni/Al Grid

Ni/Al Grid

Anti-Reflective (AR)

Zinc Oxide (ZnO)

N-type Cadmium Sulfide (CdS)

P-type CuInGaSe$_2$

Molybdenum (Mo) Electrode
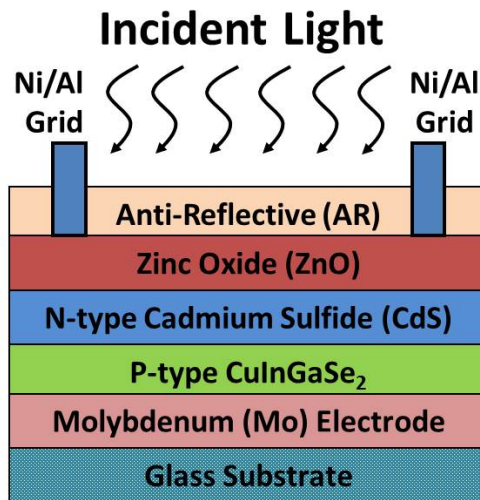
Glass Substrate

Figure 7.6: The device structure of a CIGS solar cell

(Mo) is selected as the back electrode material because it has a high light-reflection rate and can form a good ohmic contact with the CIGS thin-film for achieving high conversion efficiency. The material quality, such as the defect density and the ohmic contact resistance of the p-type CIGS light absorber layer, determines the conversion efficiency. Compared with CdTe solar cells, CIGS solar cells have less amount of toxic material Cadmium, which is mainly used as the n-type buffer layer to form a P-N junction with the p-type CIGS layer.

7.4   Organic Solar Cell

An organic solar cell or a plastic solar cell is the third generation photovoltaic technology that uses conductive organic polymers or small organic molecules for light absorption and charge transport to produce electricity from sunlight. Its conversion efficiency is usually lower than other types of solar cells due to its low carrier mobility, and its long-term reliability is also inferior to other types of solar cells. The key advantages of organic solar cells include low production costs in high volumes, lightweight, and compatibility with large-area rollable substrates such as plastic films. Low-cost deposition methods such as screen printing, doctor blading, inkjet printing, and spray deposition for organic solar cells enable low cost per kilo-watt-hour (kWh), which shows great potential for reaching a level as low as conventional coal-fired power plants. Currently the highest conversion efficiency of organic solar cells is 12 % set by a German company *Heliatek* using a vacuum-deposition process. In order to further improve the conversion efficiency while maintaining a low manufacturing cost, hybrid solar cells that incorporate both inorganic and organic materials recently attract great interests.

In Nagamatsu et al. [2014], the researchers demonstrated an orgaznic solar cell with a record of 12% efficiency. The cell uses a heterojunction between crystalline silicon and the organic polymer Poly(3,4-ethylenedioxythiophene) poly(styrenesulfonate) (PEDOT:PSS) and is made by spin-coating under a room temperature. The Si/PEDOT interface serves as a low-temperature alternative to the diffused P-N

junction that blocks the dark current from moving to the anode. This method takes advantages of the light absorption and transport properties of silicon and combines it with the simplicity of fabrication, which demonstrates the promise of the silicon/organic heterojunction (SOH) as an attractive solution for the next-generation solar cells. The types of organic solar cells include organic semiconductor based and dye-sensitized. Here we will briefly discuss each type of organic solar cells.

7.4.1 Organic Semiconductor Solar Cell

In 1979, Kodak developed the first small-molecular organic solar cell, in which the small-molecular organic material was used as the active layer for light absorption Tang [1986]. In 1993, Prof. Heeger and his research group at UC-Santa Barbara developed the first polymer solar cell based on MEH-PPV/C60 active layer Kraabel et al. [1993]. In this work, a double-heterojunction tandem cell was also demonstrated. Currently the most prominent polymer solar cell manufacturer is *Konarka* with 3-5% conversion efficiency on flexible substrates.

Figure 7.7 shows the device structure of a polymer tandem cell and Figure 7.8 shows its band diagram. The working principle of a polymer solar cell can be illustrated as follows: 1) when the carriers in the light-absorption layer (P_3HT) are excited by incident light, they will move from the highest occupied molecular orbital (HOMO) to the lowest unoccupied molecular orbital (LUMO) and form Excitons, and 2) the light-induced holes are transported to Anode while the electrons are transported to Cathode. These free carriers form the photo-currents through the external circuit.

7.4.2 Dye Sensitized Solar Cell (DSSC)

A dye-sensitized solar cell (DSSC) is a type of thin-film solar cells and has recently attracted much attention because of its low-cost, high conversion efficiency, compatibility with flexible substrates such as plastic films, and tunable optical properties such as tunability for color and transparency. A modern type of DSSC, known as the *Gratzel Cell*, was
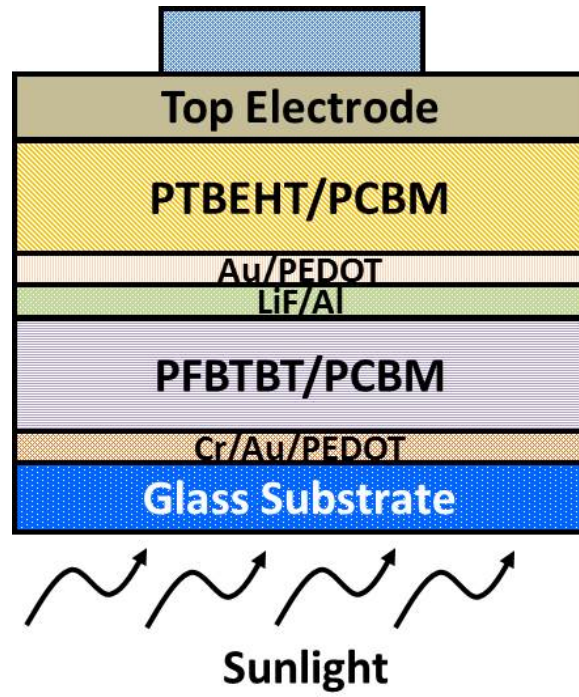
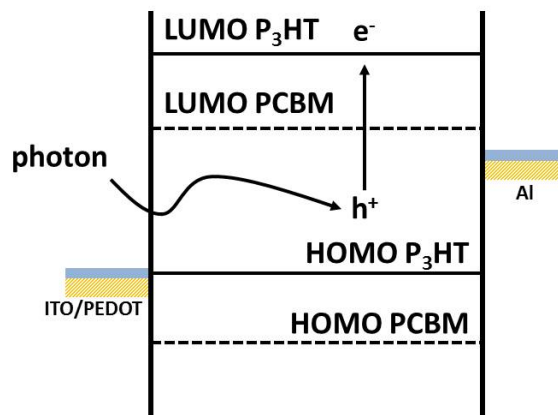**Figure 7.7:** The device structure of a polymer tandem cell.

Figure 7.8: The band diagram of a polymer tandem cell.

originally co-invented by Brian O'Regan and Michael Graztel at Swiss Federal Institute of Technology O'Regan and Gratzel [1991]. The device structure of a *Gratzel Cell* is shown in Figure 7.9. A semiconductor is formed by a photo-sensitized anode and an electrolyte. The photosensitized anode consists of a transparent conducting oxide (TCO) that is fluoride-doped tin dioxide (SnO_2:F) coated with ~ 10 μm thick titanium dioxide (TiO_2) nano-particles. The diameter of these TiO_2 nano-particles is around 10 - 30 nm. The TiO_2 coated porous electrode can effectively increase the surface area so as to improve the light absorption as well as the conversion efficiency. Currently the peak efficiency is around 13-15% Burschka et al. [2013], Mathew et al. [2014]

The band diagram of a *Gratzel Cell* can be illustrated in Figure 7.10, where LUMO represents the lowest unoccupied molecular orbital and HOMO represents the highest occupied molecular orbital. The working principle of a DSSC can be illustrated by the following four steps: 1) the photosensitizer is excited from the ground state (S_0, HOMO) to the excited state (S^*, LUMO). The excited electrons in the photosensitizer are injected into the conduction band of TiO_2, which also results in the oxidation of the photosensitizer ($S^* -> S^+$). The light absorption spectra of most photosensitizers are around 400-800 nm that are within the visible light spectrum. 2) The electrons are transported from TiO_2 to the TCO. The electrons then form photo-currents through the external circuit and finally reach the counter catalytic electrode in Figure 7.9. 3) The oxidized photosensitizer S^+ accepts the electron from redox mediator I^- leading the regeneration to the ground state S_0, and I^- is oxidized to the oxidized state I_3^-. 4) The oxidized redox mediator I_3^- diffuses to the counter catalytic electrode and accepts the electrons, which makes I_3^- reduce to I^-. The open circuit voltage ($V_{OC} \sim 0.7$V) depends on Fermi level of the TiO_2 electrode and the redox potential of the mediator (I^-/I_3^-) in the electrolyte.

7.5 Summary

In this chapter we briefly introduce several types of thin-film photovoltaic technologies including a-Si, CdTe, CIGS, and organic solar
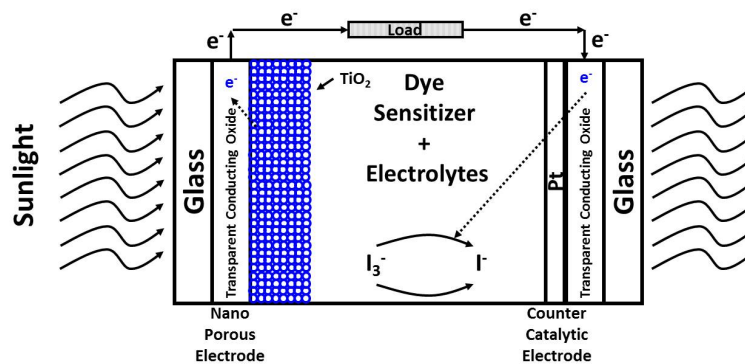
Figure 7.9: The device structure of a *Graztel Cell*. The TiO_2 nano-particles are shown as blue bubbles.
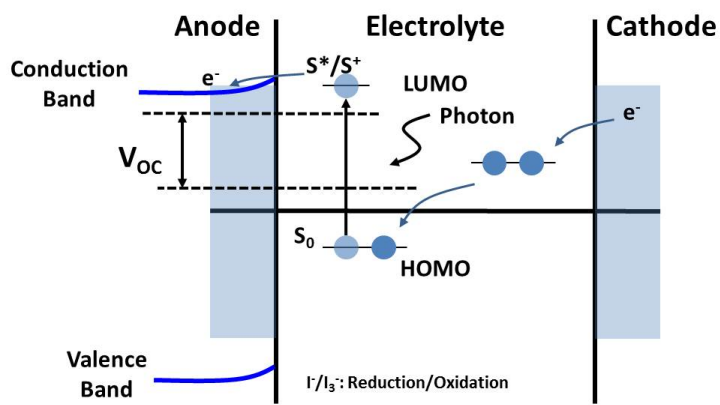
Figure 7.10: The band diagram of a *Graztel Cell*.

cells. In comparison with conventional crystalline silicon solar cells, thin-film solar cells in general have lower manufacturing and material costs. They are also compatible with flexible substrates for rollable and portable photovoltaics. Among all thin-film photovoltaics technologies, an a-Si solar cell is the most mature and the safest to the environment, but its low conversion efficiency prevents it from wide adoption for megawatt photovoltaic systems. Compound semiconductor solar cells such as CdTe and CIGS have the advantages of high conversion efficiency and low cost, but the use of toxic Cadmium contents in these solar cells cause safety concerns. Organic solar cells, including organic semiconductor based and dye-sensitized, have recently attracted great attention due to their inherent low-cost and nontoxicity to the environment. They can also be manufactured using continuous fabrication methods such as roll-to-roll printing, which can further reduce the cost. The main drawback of organic solar cells is their inferior conversion efficiency. However, with rapid advances in organic materials, their efficiency and manufacturing cost undoubtedly can be further improved.

8

Conclusion

Flexible electronics is an alternative to conventional Si-electronics for large-area and low-cost applications such as displays, sensors, and disposable electronics. As the TFT technology advances, systems that integrate digital and analog/mixed-signal circuits with a large-area display and/or with sensors are emerging. Due to the unique TFT characteristics and application scenarios, The current circuit design methodologies and the EDA (electronics design automation) flow, which are mature for Silicon-based CMOS designs, must be re-evaluated and modified to address the unique design requirements and limitations of flexible electronics for optimizing the circuit performance and improving the design productivity.

In this paper, we introduce the applications of flexible electronics and their printing processes, which include ink-jet printing, screen printing, and gravure printing. We also elaborate in detail major TFT technologies such as a-Si:H, ink-jet organic, SAM organic, and metal-oxide TFTs. In-depth device modeling and experimental model validation based on actual fabricated devices are shown. For circuit design, we illustrate techniques for digital and analog/mixed-signal circuits ranging from microprocessors to ADCs. We also give an overview of recent

research results that concern automation of design and test for flexible electronics, which include timing analysis, physical design, manufacturing testing, and yield optimization. We further elaborate the analysis for long-term reliability and show the results of a case study for an a-Si scan driver used in flexible displays. Finally, we give an overview of flexible photovoltaics, which is a key application of flexible electronics and thus should be of great interest to the readers.

The significant research results produced in the past decades have made flexible electronics sufficiently mature and deployable in several emerging applications such as smart homes, smart health, and ubiquitous electronics. With the rapid and consistent improvement of TFT reliability and performance in the past several years, we have observed its growing deployment in low-cost, large-area wearable and disposable systems. For the foreseeable future, we should be able to see its presence in a broader range of systems, ranging from smart contact lenses to structural health monitors for cars, bridges or airplanes.

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