UNIVERSITY OF CALIFORNIA SAN DIEGO

Ultrawideband Front-End Circuits and 6-32 GHz Phased-Array Beamformer for Tri-Band SATCOM

A dissertation submitted in partial satisfaction of the
requirements for the degree Doctor of Philosophy

in

Electrical Engineering (Electronic Circuits and Systems)

by

Oguz Kazan

Committee in charge:

Professor Gabriel M. Rebeiz, Chair
Professor Gert Cauwenberghs
Professor Drew Hall
Professor William Hodgkiss
Professor Tzu-Chien Hsueh

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The Dissertation of Oguz Kazan is approved, and it is acceptable in quality and form for publication on microfilm and electronically.

University of California San Diego

2022

DEDICATION

To my mother Nurten Kazan and my father Murat Fatih Kazan

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Chapter 2 is, in full, a reprint of the material as it appears in: O. Kazan and G. M. Rebeiz, "A 10–110 GHz LNA with 19-25.5 dB Gain and 4.8-5.3 dB NF for Ultra-Wideband Applications in 90nm SiGe HBT Technology," *2021 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2021, pp. 39-42.

Chapter 3 is, in full, a reprint of the material as it appears in: O. Kazan and G. M. Rebeiz, "A 10-130 GHz Distributed Power Amplifier Achieving 2.6 THz GBW with Peak 13.1 dBm Output P1dB for Ultra-Wideband Applications in 90nm SiGe HBT Technology," *2021 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)*, 2021, pp. 1-4.

Chapter 4 is, in full, to be submitted for publication of the material as it may appear in: O. Kazan, Z. Hu, L. Li, A. Alhamed and G. M. Rebeiz, "An 8-channel 5-33 GHz Transmit Phased Array Beamforming IC With 10.8-14.7 dBm Psat for C, X, Ku and Ka-band SATCOM," *IEEE Transactions on Microwave Theory and Techniques*.

Chapter 4, in part, has been submitted for publication of the material as it may appear in: O. Kazan, Z. Hu, A. Alhamed and G. M. Rebeiz, "A 5-33 GHz 8-Channel Transmit Beamformer with Peak Power of 14 dBm for X/Ku/Ka-band SATCOM Applications" in *2022 IEEE International Symposium on Phased Array Systems and Technology*, 2022.

VITA

2014	Bachelor of Science in Electrical and Electronics Engineering, Middle East Technical University - Northern Cyprus Campus, Guzelyurt, Turkish Republic of Northern Cyprus
2014-2016	Integrated Circuit Design Engineer in Mikro-Tasarim, Ankara, Turkey
2018	Master of Science in Electrical and Electronics Engineering, Middle East Technical University, Ankara, Turkey
2022	Doctor of Philosophy in Electrical Engineering (Electronic Circuits and Systems), University of California San Diego

PUBLICATIONS

O. Kazan, Z. Hu, L. Li, A. Alhamed and G. M. Rebeiz "An 8-channel 5-33 GHz Transmit Phased Array Beamforming IC With 10.8-14.7 dBm Psat for C, X, Ku and Ka-band SATCOM," in *IEEE Transactions on Microwave Theory and Techniques*, to be submitted.

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A. Alhamed, O. Kazan, G. Gültepe and G. M. Rebeiz, "A Multiband/Multistandard 15-57 GHz Receive Phased-Array Module Based on 4×1 Beamformer IC and Supporting 5G NR FR2 Operation," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 70, no. 3, pp. 1732-1744, March 2022.

O. Kazan and G. M. Rebeiz, "A 10-130 GHz Distributed Power Amplifier Achieving 2.6 THz GBW with Peak 13.1 dBm Output P1dB for Ultra-Wideband Applications in 90nm SiGe HBT Technology," *2021 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)*, 2021, pp. 1-4.

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A. A. Alhamed, O. Kazan and G. M. Rebeiz, "A Multi-Standard 15-57 GHz 4-Channel Receive Beamformer with 4.8 dB Midband NF for 5G Applications," *2020 IEEE/MTT-S International Microwave Symposium (IMS)*, 2020, pp. 1011-1014.

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ABSTRACT OF THE DISSERTATION

Ultrawideband Front-End Circuits and 6-32 GHz Phased-Array Beamformer for Tri-Band SATCOM

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Oguz Kazan

Doctor of Philosophy in Electrical Engineering (Electronic Circuits and Systems)

University of California San Diego, 2022

Professor Gabriel M. Rebeiz, Chair

The demand for communications is increasing and this requires higher data transmission and better global coverage. Wideband circuits enable high data rate communications for wireless and wireline applications. Also, they simplify the hardware by replacing several circuits or systems covering narrower bandwidths. This thesis presents three different wideband designs addressing wideband circuits and systems. The circuits presented in this thesis are all implemented using 90 nm SiGe BiCMOS process.

Firstly, a 10-110 GHz low noise amplifier is presented. The circuit is composed of four differential cascode stages. The measured small-signal gain is 19-24.5 dB with a noise figure of

4.8-5.3 dB. Highest figure of merit is achieved with conventional cascode amplifier topology. The circuit is very small compared to the distributed amplifier designs in the literature and consumes less power.

Second, a 10-130 GHz distributed power amplifier (DPA) is presented. The circuit is composed of three stages each with multiple cascode amplifier sections. The amplifier achieves small-signal gain of 18-23 dB at 10-30 GHz and increasing to 33 dB at 98 GHz, resulting in a record gain-bandwidth product of 2.6 THz. The circuit has a peak output 1-dB compression point (OP1dB) of 13.1 dBm at 22 GHz. The proposed amplifier achieves the largest gain-bandwidth product in SiGe DPAs while providing relatively high power.

Finally, an 8-channel 5-33 GHz transmit phased array RFIC for C, X, Ku and Ka-band SATCOM applications is presented. The 4×2 beamformer is implemented in a 90nm SiGe HBT process. Each channel has a wideband two-stage power-amplifier (PA), a phase-shifter (PS), a variable gain amplifier (VGA) and single-ended to differential converter (S2D). The input RF power is distributed to the 8-channels using a two-stage lumped-element Wilkinson network and active dividers. The measured electronic gain is 24-27 dB at 5-33 GHz with 5-bit phase-shifter operation and $>$20 dB gain control. A peak OP1dB and OPsat of 10.8-14 dBm is achieved over the entire frequency range. The chip is then implemented in a wideband phased-array using tapered-slot (Vivaldi) antennas. The 16-element phased array achieves ±60° scanning at C, X and Ku bands and ±30° scanning at Ka band with a broadside EIRP of 16-38.5 dBm at 8-32 GHz. QPSK, 8 PSK and 16-QAM waveform are delivered to the phased array for performance evaluation, and $<$4-4.8% EVM is achieved C to Ka-band at P1dB (EIRP) operation. Application areas are C/X/Ku/Ka-band ground terminals for satellite communications.

Chapter 1

Introduction

1.1 Modern Communications and Their Call for Wide Bandwidth Systems

Dr. Guglielmo Marconi built the first radio telegraphy which can transmit Morse code with radio signals in the late nineteenth century. Since then, our communication technology has developed rapidly, and we now live in a world where our smartphones and computers are changing our lives by shaping how we communicate, do business, and do shopping. These are made possible by the advancements in our modern wireless communications technology.

Our wireless technology is supported by ever more complex cellular networks by going through tremendous advancements over the past 40 years. In 1979, the first analog cellular system was launched in Japan. In North America, the Advanced Mobile Phone Service was introduced in 1983. Today, we categorize these systems as first generation (1G - analog cellular), and they suffered from consuming a lot of spectrum. The second-generation cellular technology (2G) was launched in Finland in 1991. This technology employed digital communications and hence used the spectrum more efficiently than 1G. With the success of digital communications, higher data rate demand has increased and 3G and then 4G technologies have evolved from the 2G systems. The goal of 5G today is to enable ultra-high data transmission rate, low latency, and massive connectivity. One of the ways achieving the goal of high data transmission rate of is to utilize more spectrum and hence the need for wideband systems has increased.

Another wireless technology which is shaping our world is satellite communications (SATCOM). It was predominantly used for maritime and military ground systems, and now, it is becoming available to the public as an affordable terminal for high speed communications allowing internet access around the globe. Geosynchronous Earth Orbit (GEO) satellites are the most widely used since the satellites are fixed on the ground and therefore, the ground terminals are also fixed when pointing to the satellite (no moving parts). This is because the angular velocity of the satellites at the GEO orbit is the same as that of Earth, and hence the satellites appear fixed in space. However, the GEO orbit is at 35,786 km away from the equator which results in $\sim$240 ms round trip latency, and this is not acceptable for many internet connections. Also, the satellites require high power transmitters and large atnennas due to their distance from the earth, resulting in very complex and expensive satellites ($300-500M each). Low Earth Orbit (LEO) satellites with orbits at 500-1200 km, and Medium Earth Orbit (MEO) satellites with orbits of 6000-8000 km, are becoming feasible solutions to the cost and latency problem since they are much smaller than GEO satellites, much easier to launch, and can be built in large quantities. Also, their latency is 30-100 times shorter than GEO systems and this allows for high speed internet without any issues. However, LEO satellites are not stationary in the sky and are constantly moving in specified orbits over the user, and thus, they need to be constantly tracked. Phased-arrays, also called electronically scanned arrays, provide a reliable solution to this tracking problem for LEO and MEO satellites as they do not require moving parts and can hop from satellite to satellite in few ms. There are multiple frequencies used for SATCOM as approved by ITU (International Telecommnications Union) and the FCC (Federal Communications Commission). Transmit frequencies are 6, 8, 14 and 29 GHz, and the receive frequencies are 3.8, 7, 12 and 20 GHz. Traditionally, SATCOM systems are narrowband and most of them cover only one frequency range. However, using a wideband system which covers all SATCOM frequencies would simplify the hardware and cost.

These are just two examples showing the need for wideband systems. Wireline communication links, high resolution imaging and high frequency instrumentation are among others.

Therefore, the need for wideband circuits is increasing and becoming a hot topic in literature, and this thesis focuses on wideband circuits and systems. An ultra-wideband low-noise amplifier, a distributed power amplifier and a beamforming integrated circuit for SATCOM phased array systems are proposed. The circuits are built using 90nm SiGe HBT technology and all of them beat the state-of-the-art performance.

1.2 Thesis Overview

This thesis presents fully integrated ultra-wideband circuits for low noise, high power and phase array systems.

Chapter 2 presents a broadband differential low-noise amplifier (LNA) at 10-110 GHz. The four-stage LNA is realized using 90 nm SiGe BiCMOS process having a 300 GHz f_T HBT. Resistive feedback is used for operation at 10-50 GHz, and a wideband collector load with a linear impedance increase versus frequency compensates for the transistor output capacitance and guarantees a monotonic increase in the gain from 60 to 100 GHz. The LNA has a measured small-signal gain of 19-25.5 dB and the measured noise figure (NF) is 4.8-5.3 dB at 10-50 GHz. The LNA also achieves an output-referred 1dB compression point (OP1dB) of 3.3 dBm at 66 GHz. The differential LNA consumes 96 mW (48 mW half circuit) with an active circuit area of 1.3×0.6 mm^2. Application areas are in wideband receivers and in wideband microwave and millimeter wave instrumentation systems.

Chapter 3 presents a 10-130 GHz ultra-wideband distributed power amplifier (DPA) with 2.6 THz gain-bandwidth product (GBW). The DPA is composed of 3 stages each with multiple cascode amplifier sections. The circuit is realized using 90 nm SiGe BiCMOS process having a 255 GHz fT HBT. The amplifier achieves small-signal gain of 18-23 dB at 10-30 GHz and monotonically increasing to the peak of 33 dB at 98 GHz. The return losses are better than 10 dB covering more than 140 GHz. The circuit has a peak OP1dB of 13.1 dBm at 22 GHz. The proposed amplifier achieves the largest GBW in SiGe DPAs while providing relatively high

power. Applications areas are in wireline communications, high frequency instrumentation and high resolution imaging.

Chapter 4 presents an 8-channel 5-33 GHz transmit phased array RFIC for C, X, Ku and Ka-band SATCOM applications. The 4×2 beamformer is implemented in a 90nm SiGe HBT process. Each channel has a wideband two-stage power-amplifier (PA), a phase-shifter (PS), a variable gain amplifier (VGA) and single-ended to differential converter (S2D). The input RF power is distributed to the 8-channels using a two-stage lumped-element Wilkinson network and active dividers. The measured electronic gain is 24-27 dB at 5-33 GHz with 5-bit phase-shifter operation and >20 dB gain control. A peak OP1dB and OPsat of 10.8-14 dBm is achieved over the entire frequency range. The chip is then implemented in a wideband phased-array using tapered-slot (Vivaldi) antennas. The 16-element phased array achieves ±60° scanning at C, X and Ku bands and ±30° scanning at Ka band with a broadside EIRP of 16-38.5 dBm at 8-32 GHz. QPSK, 8 PSK and 16-QAM waveform are delivered to the phased array for performance evaluation, and <4-4.8% EVM is achieved C to Ka-band at P1dB (EIRP) operation. Application areas are C/X/Ku/Ka-band ground terminals for satellite communications.

This thesis concludes with Chapter 5. A summary of the chapters is given and future work is discussed.

Chapter 2

A 10-110 GHz LNA with 19-24.5 dB Gain and 4.8-5.3 dB NF for Ultra-Wideband Applications in 90nm SiGe HBT Technology

2.1 Introduction

Due to the ever-increasing 5G frequencies, starting from 24 GHz extending to 52 GHz, and with possible extensions down to the 10 GHz range and up to 94 GHz range, it is important to develop wideband receivers and instrumentation capable of developing covering the entire 10-110 GHz range. Previously, distributed amplifiers (DA) have been shown to cover such a range (DC-105 GHz, etc.) but were designed mostly for wireline applications and with relatively high-power consumption [1, 2, 3, 4, 5]. Also, distributed amplifiers normally occupy a large area which is not suitable for wideband phased arrays.

In this paper, an ultra-wideband LNA at 10-110 GHz is demonstrated. The circuit is composed of 4 differential common-emitter amplifier stages, and the wide bandwidth is achieved using a multi-stage wideband load and resistive shunt feedback. The amplifier area is very small and results in state-of-the-art performance.

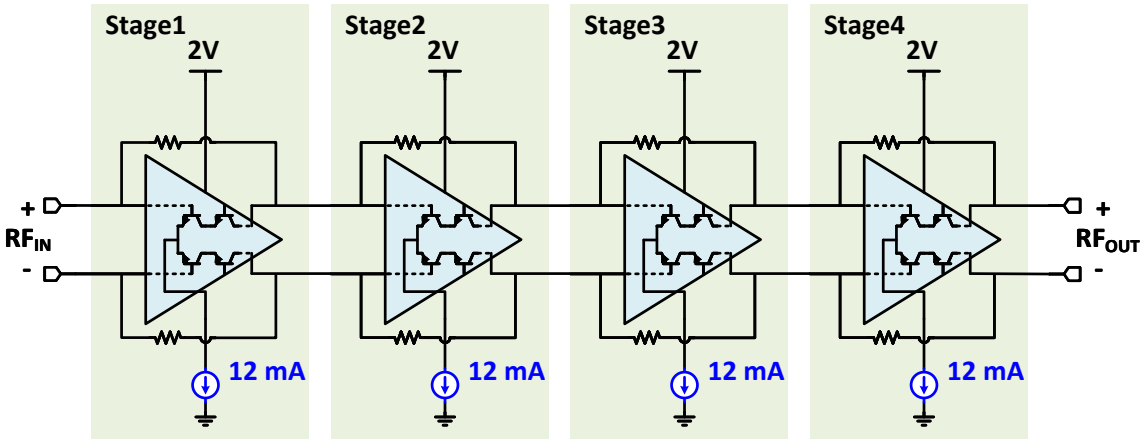


Figure 2.1: Schematic of the 4-stage wideband LNA.

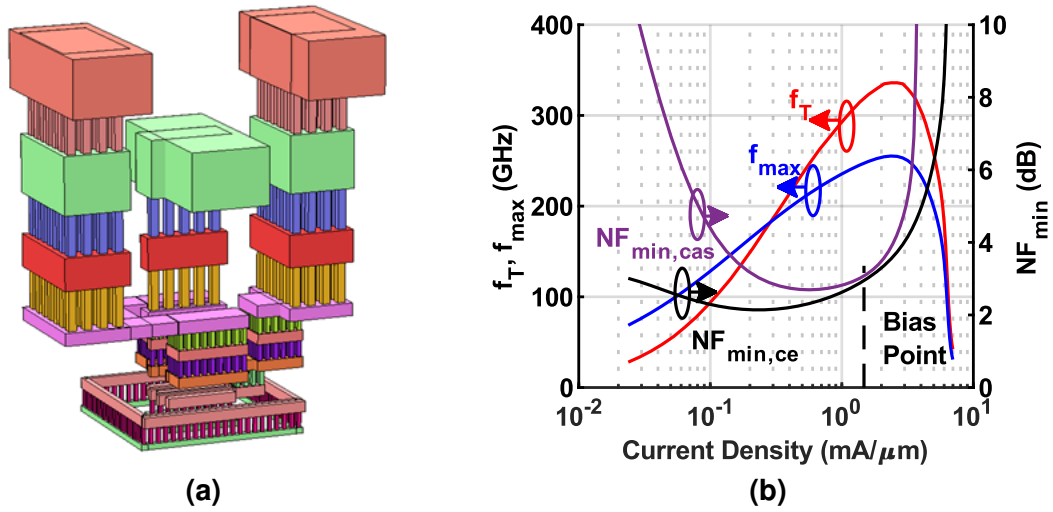


Figure 2.2: (a) Physical layout of a transistor, (b) 4µm transistor performance. Black, red, and blue curves show single transistor performance. Purple curve shows two cascode connector transistors performance. NFmin results are for 60 GHz operation.

2.2 Technology

The wideband LNA is implemented in the Tower Semiconductor 90 nm SiGe BiCMOS platform with all-aluminium backend and a 7-metal stack. For most of the inductors, the top layer is used, and a ground plane is placed at M1/M2 to increase the inductor Q. All the inductors and metal capacitors are modelled using Integrand Software, EMX.

Fig. 2.2 presents a transistor layout and simulations in the TowerSemi SBC18S5 tech-

nology for the common-emitter and cascode configurations with 4 μm emitter length. The common-emitter transistor has an NFmin of 2.1 dB at 0.21 mA/μm (60 GHz). However, if the transistors are connected in a cascode configuration, the achievable NFmin becomes 2.7 dB at 0.56 mA/μm (60 GHz). However, in this design, the first stage is biased at 1.5 mA/μm with an NFmin penalty of 0.3 dB to increase the first-stage gain by 2 dB and to lower the noise contribution of the subsequent stages. The second, third and fourth stages are biased at 0.56 mA/μm for lowest NF and to conserve DC power.

2.3 Design

The proposed wideband LNA is shown in Fig. 2.1. It is composed of 4 cascode differential stages to achieve the desired gain and noise figure (NF) at 10-110 GHz and to match well with a wideband differential antenna. For the tail current sources, HBT devices are used due to their lower parasitics compared to the 0.18μm CMOS devices available in this technology, to improve the common-mode rejection. The current-source device size is chosen as a compromise between the transistor parasitics and the voltage headroom. The common mode rejection is further improved by tying the bases of the cascode devices.

A large amplifier bandwidth is generally achieved using light resistive feedback and also inductive loads with wideband impedance characteristics. One of the essential problems in wideband amplifier design is that the load inductor which is chosen to operate well at the lower frequency range, will resonate at the higher band resulting in a severe drop in amplifier gain. If the inductor is chosen for operation at high frequencies, then the amplifier gain is low at the lower frequency band. One solution is high resistive feedback, but this greatly lowers the gain per stage and increases the total amplifier power. Another solution is using a resistor in series with a high value inductor, (commonly called a low-Q load), but this results in low voltage headroom, and does not compensate for the transistor capacitance as the frequency increasing resulting again in a gradual gain drop as the frequency increases. The final solution is of course,

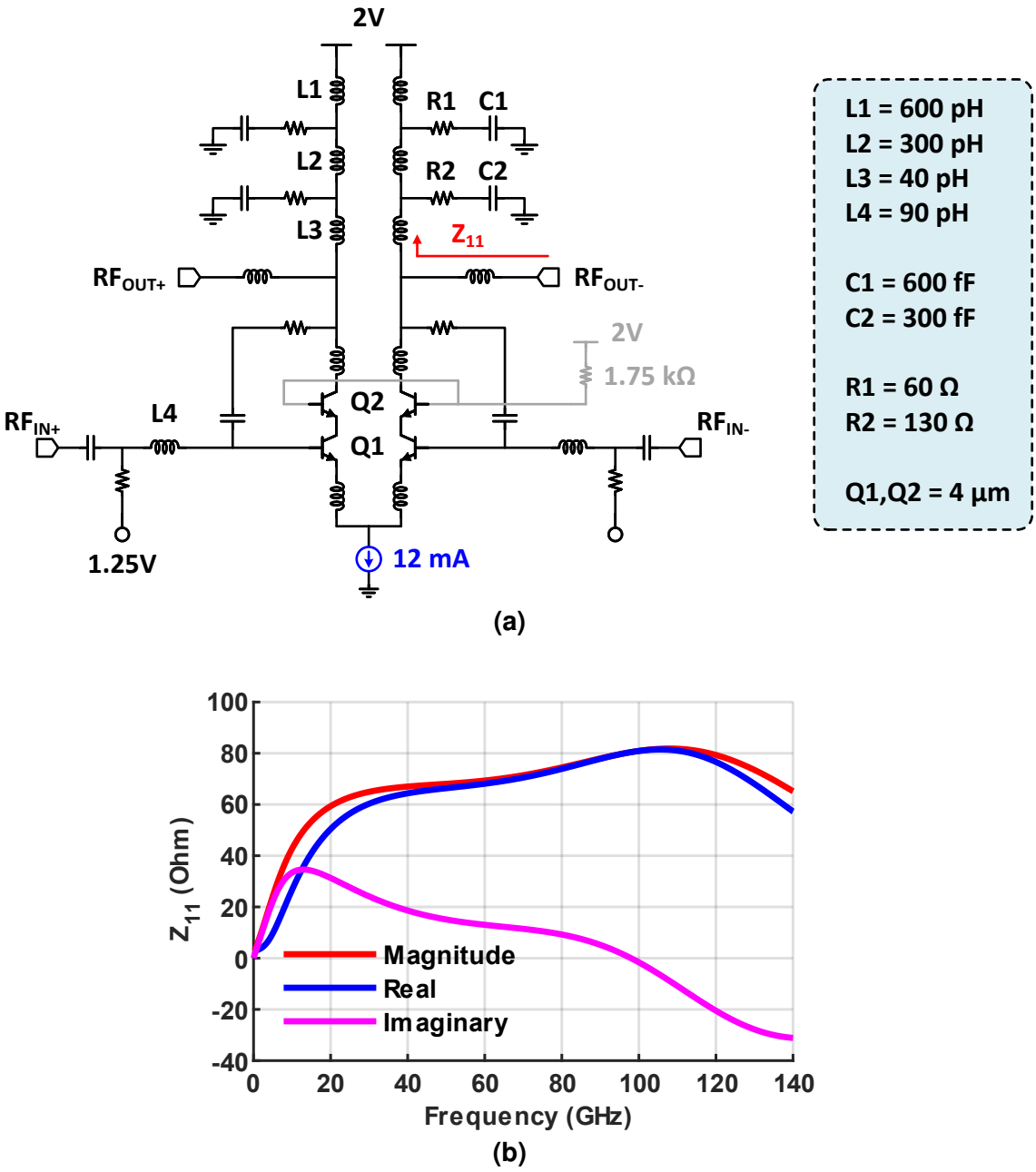
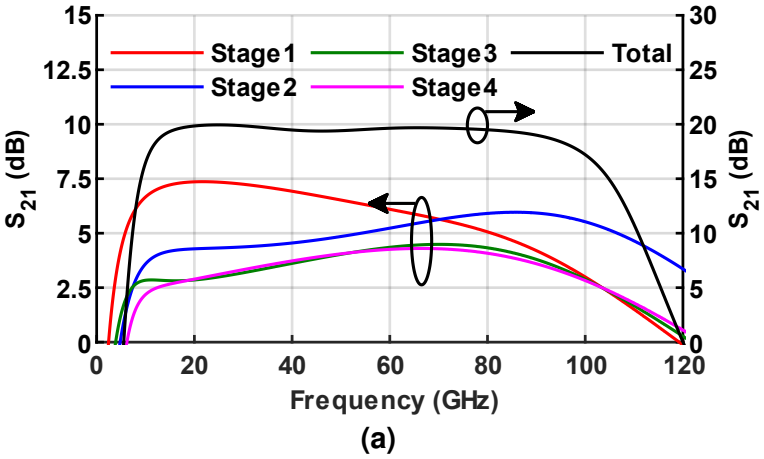


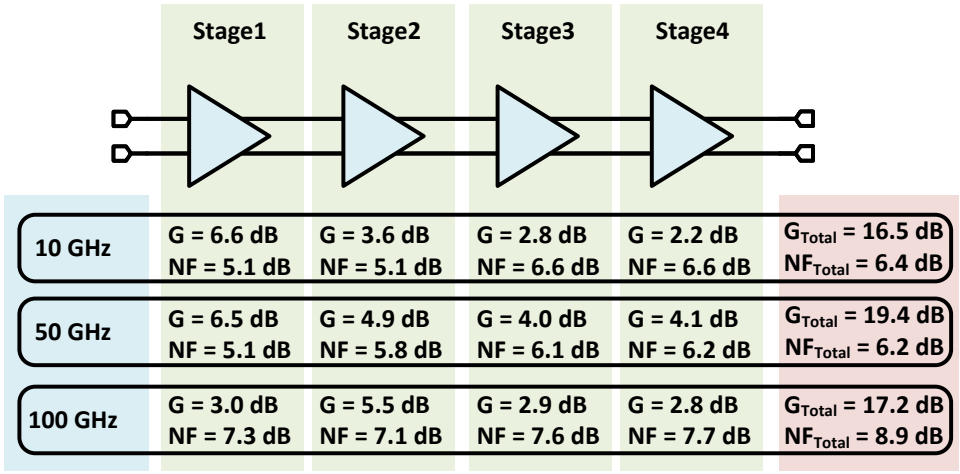
Figure 2.3: (a) First stage of the wideband LNA (other stages are similar but with different L and C values), (b) Simulated impedance of the first stage load.

the distributed amplifier design technique which is excellent but consumes a lot of power.

This work introduces an innovative multi-stage load composed of L1/L2/L3 and C1R1/ C2R2 with the specific purpose of generating an increasing load impedance versus frequency without going into resonance (Fig. 2.3a). At the lower frequency range, C1 and C2 are nearly



(a)



(b)

Figure 2.4: (a) Gain response of individual stages, (b) Simulated gain and noise figure at 10, 50 and 100 GHz.

open circuited and the load is composed of L1+L2+L3. At mid-frequencies, the load is composed of L3+L2, and the resonance in L1 is dampened by R1. At the highest frequencies, the load is composed mostly of L3 and the resonance in L2 is dampened by R2. The multi-stage load occupies a small area and has an effective impedance which increases from 40 Ω at 10 GHz to 80 Ω at 100-110 GHz while still being inductive over the entire frequency range. The effect of RC section on the self-resonant frequency of the load is presented in Fig. 2.5 . The load also has a near-zero impedance at DC to reduce the power consumption. The load network is simulated with EMX.

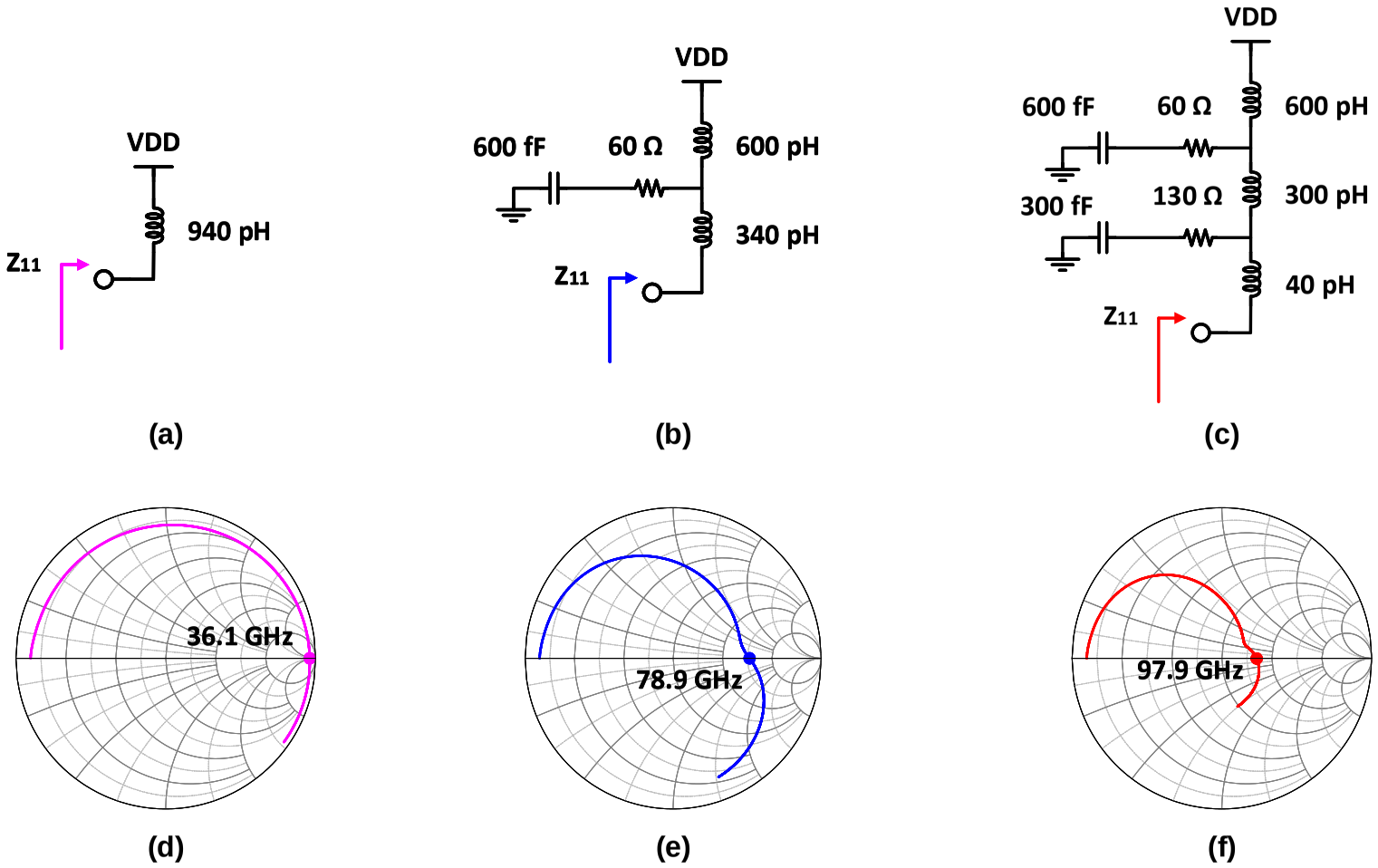


Figure 2.5: The effect of RC section on the self-resonant frequency of the load: (a)(d) without RC section, (b)(e) one RC section is added, (c)(f) two RC sections are added.

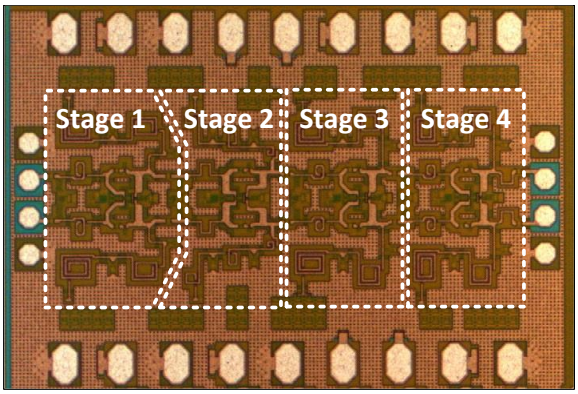


Figure 2.6: Die photo of the wideband differential LNA. The size is 1.5×1.0 mm^2 including the pads, and 1.3×0.6 mm^2 excluding the pads.

Fig. 2.4b presents the simulated gain and NF of every stage in the 4-stage LNA. The values are in power gain assuming a load of 100 Ω, but the final gain is higher than the added block gain (in dB) due to the inductive match at each base. At the midband frequency of 50 GHz, the first stage has a gain of 6.5 dB and a NF of 5.1 dB, with all other stages having a gain of 4-4.8 dB. The gain is nearly equally distributed for near-optimal P1dB performance, and to result in wideband performance for all four stages, and thus for the entire LNA.

2.4 Measurements

The LNA die photo is shown in Fig. 2.6, with chip dimensions of 1.5×1.0 mm^2, including the pads, and 1.3×0.6 mm^2, excluding the pads. To our knowledge, this is the smallest 10-110 GHz LNA reported and is much smaller than distributed amplifier designs. The amplifier employs a GSSG input and output pads and all measurements are calibrated to these ports.

For gain measurements, a GSSG probe was used up to 40 GHz (Fig. 2.8a). Also, LNAs with Marchand baluns at their input and output ports were also placed on the tapeout and covering the frequencies of 10-30 GHz, 20-50 GHz, 45-100 GHz, and these circuits are for measurement purposes (Fig. 2.7). The Marchand baluns result in an LNA with GSG ports and allow for NF measurements to be possible up to 100 GHz. One of the LNAs with Marchand baluns is depicted in Fig. 2.6b. Back-to-back baluns are also placed on the tapeout for de-embedding.

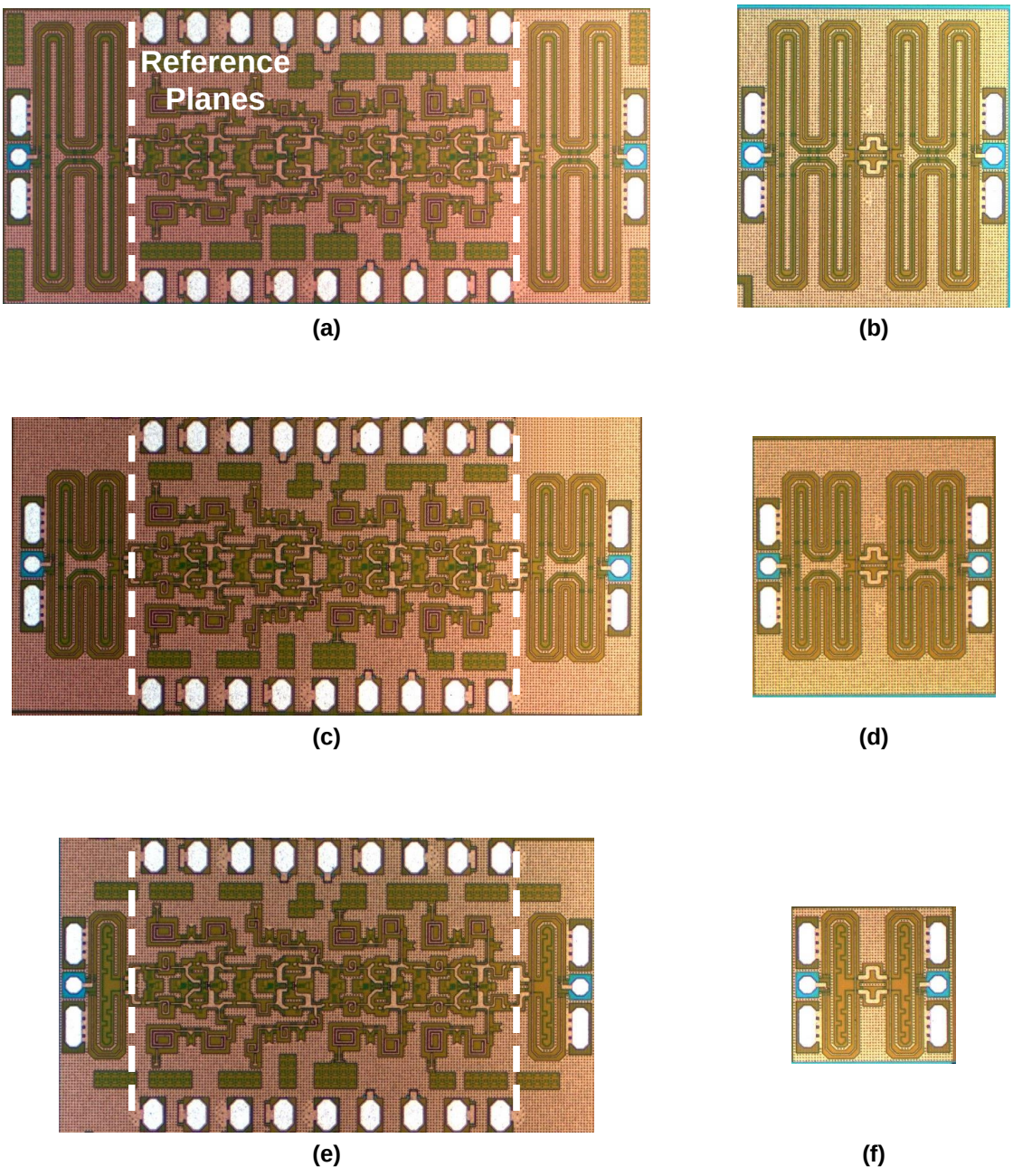


Figure 2.7: Die photo of the LNA with input and output Marchand baluns and die photo of back-to-back baluns for operation at (a)(b) 10-30 GHz, (c)(d) 20-50 GHz, (e)(f) 45-100 GHz.

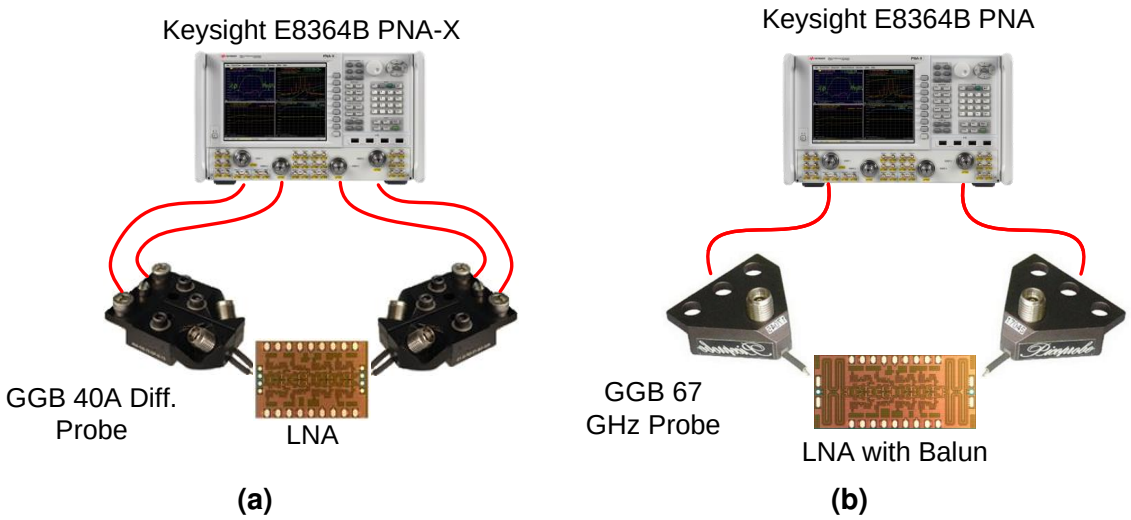


Figure 2.8: Measurement setup for small-signal performance: (a) s-parameter up to 40 GHz; (b) s-parameter up to 70 GHz and NF up to 50 GHz.

Small-signal S-parameters and linearity performances are evaluated up to 70 GHz, and NF is evaluated up to 50 GHz using a Keysight N5247A PNA-X Network Analyzer (Fig. 2.8b). This setup is used for both single-ended 2-port measurements and differential 4-port measurements. Small-signal S-parameters between 70-110 GHz are obtained using a setup containing a Keysight E8364B PNA Network Analyzer, a Keysight N5260A Millimeter Head Controller, and Virginia Diodes WR-10 75-110 GHz extenders (Fig. 2.9).

Fig. 2.10a presents the small-signal performance. S_{21} is 18-19 dB at 20-30 GHz and increases to 25.5 dB at $\sim$97 GHz, which is desirable for our purposes as the blocks connected at the output of the LNA have higher loss and need a bit of additional gain (mixers, phase shifters, etc.). The gain is higher than simulated at 70-100 GHz and is most probably due to the wideband network having an even higher impedance. The LNA has a reverse isolation (S_{12}) $<$-40 dB at 70-110 GHz.

The measured noise figure is shown in Fig. 2.10b. The NF is obtained by de-embedding the input and output balun losses, and is 4.8-5.5 dB up to 50 GHz, with a mean of 5.3 dB. NF measurements at higher frequencies are not performed due to the unavailability of the noise

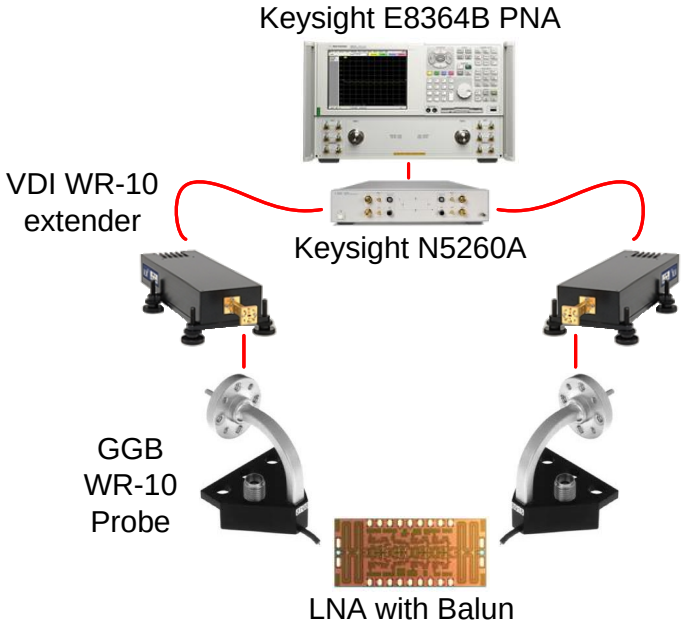


Figure 2.9: Measurement setup for small-signal performance for S-parameters up at 70-110 GHz.

source for 60-90 GHz. It is seen that the measured NF is close/lower than simulations and this is due to the use of early models in this technology (seen on different circuits). The measured OP1dB performance is -9 dBm to -4 dBm at 10-60 GHz and agrees well with simulations (Fig. 2.11a). The measured OIP3 is $\sim$9 dB higher than the OP1dB and agrees with simulations (Fig. 2.11b).

The wideband LNA is compared to the state of the art in Table 2.1, and the figure-of-merit (FoM) is given by [9]:

$$FoM = 20\log_{10}\left(\frac{Gain[lin.] \times BW[GHz]}{P_{DC}[mW] \times (NF[lin.]-1)}\right), \tag{2.1}$$

State-of-the-art-gain, bandwidth, power consumption and NF has been achieved, resulting in a large FoM.

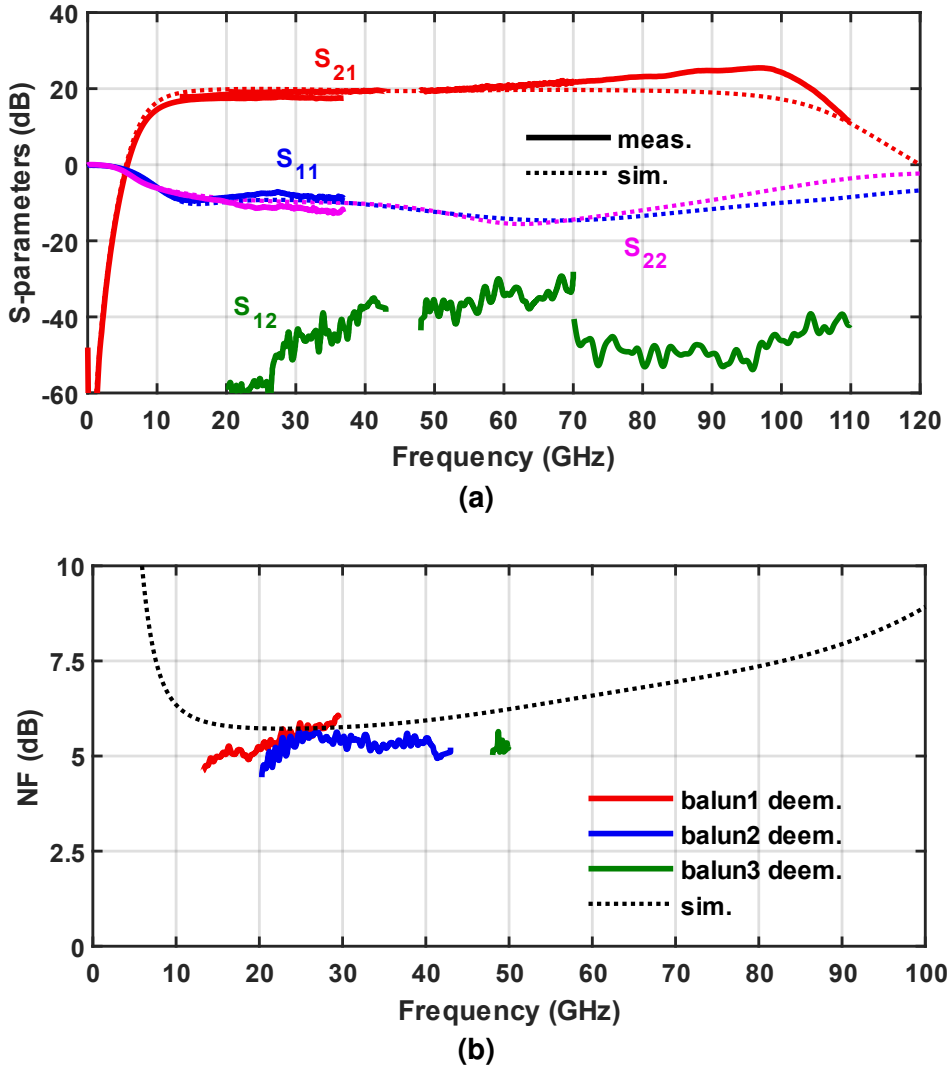


Figure 2.10: Measured and simulated: (a) S-parameters; (b) noise figure.

2.5 Conclusion

A 10-110 GHz LNA is presented in this paper. The circuit employs a wideband multi-stage L/C/R load and resistive shunt feedback to achieve an ultra-large bandwidth. The measurements indicate that the LNA exhibits high performance and is unconditionally stable. The proposed LNA is a very good candidate for ultra-wideband applications.

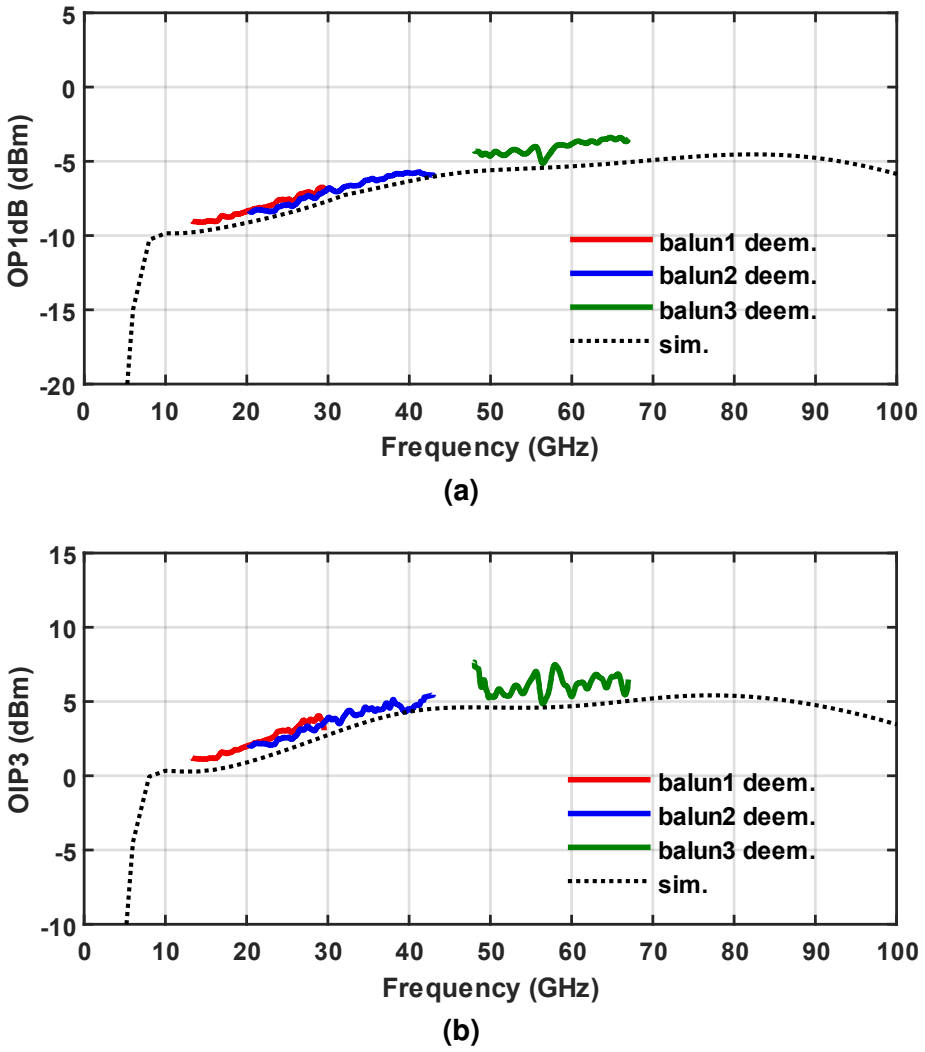


Figure 2.11: Measured and simulated: (a) OP1dB, (b) OIP3.

2.6 Acknowledgement

This work was supported by the DARPA T-MUSIC program. The authors thank Integrand Software for the use of EMX.

Chapter 2 is, in full, a reprint of the material as it appears in: O. Kazan and G. M. Rebeiz, "A 10–110 GHz LNA with 19-25.5 dB Gain and 4.8-5.3 dB NF for Ultra-Wideband Applications in 90nm SiGe HBT Technology," *2021 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2021, pp. 39-42. The dissertation author was the primary investigator and primary author of this paper.

Table 2.1: Comparison with State-of-the-Art Wideband Amplifiers

Reference	Technology	Topology	Frequency (GHz)	Gain (dB)	NF (dB)	P_{DC} (mW)	Area (mm^2)	FoM
[5] ISIC 2016	130-nm SiGe BiCMOS	DA with Stacked HBTs	10-170	19	N.R.	560	0.91	-
[6] TMTT 2015	28-nm CMOS	2 Stage Cascode	54.5-72.5	13.8	4	24	0.38	7.7
[7] JSSC 2017	65-nm CMOS	3 Stage Cascode	62.5-92.5	18.5	5.5	27	0.24	11.3
[8] MWCL 2016	65-nm CMOS	5 Stage Cascode	88.5-110	16.7	7.2	48.6	0.29	-2.9
[9] APMC 2015	65-nm CMOS	6 Stage Cascode	73.5-93.5	22	6.8	21	0.45	10
[10] TMTT 2020	22-nm CMOS FD-SOI	3 Stage Cascode	70-100	18.2	5.8	16	0.43	15
This work	90-nm SiGe BiCMOS	4 Differential Stage Cascode	10-110	19-25.5	4.8-5.3	48[a]	0.78[b]	22.7

N.R. = Not Reported
[a] Single-ended half-circuit
[b] Differential circuit area

Chapter 3

A 10-130 GHz Distributed Power Amplifier Achieving 2.6 THz GBW with Peak 13.1 dBm Output P1dB for Ultra-Wideband Applications in 90nm SiGe HBT Technology

3.1 Introduction

Broadband distributed power amplifiers (DPAs) can process ultra-narrow pulses, which makes them attractive for wireline communication links, high-frequency instrumentation, and high-resolution imaging. In literature, there several DPAs implemented in SiGe BiCMOS, CMOS SOI and InP HBT. The DPAs reported in SiGe technologies either have low gain and high output power [11, 12] or are wideband and with low output power [13]. Also, state-of-the-art SiGe DPAs have a gain-bandwidth product (GBW) of $\sim$ 1.6 THz [11, 12, 13, 14, 15, 16, 17].

In this work, an ultrawideband 10-130 GHz DPA in 90 nm SiGe HBT technology is demonstrated. The circuit is composed of three cascaded distributed amplifier stages, each having 5, 6 and 16 gain sections. The amplifier has ultra-wideband characteristics while providing high power. To the best of authors' knowledge, the proposed DPA has the largest GBW of 2.6 THz among other SiGe distributed amplifiers.

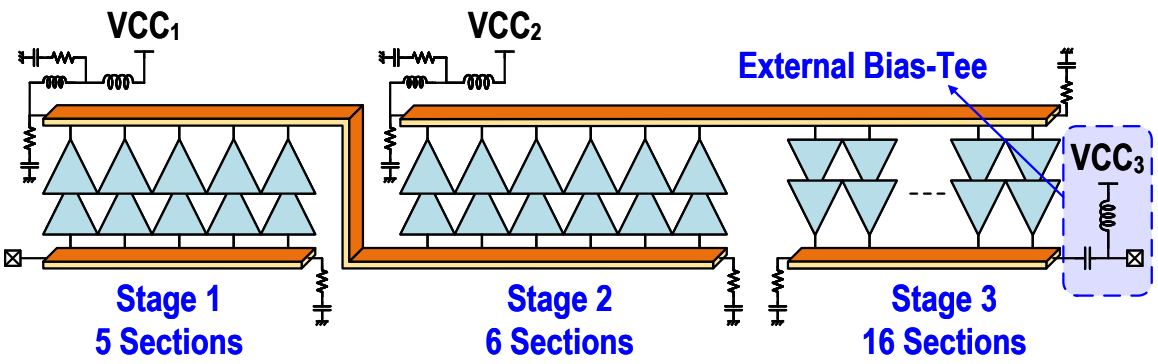


Figure 3.1: A 3-stage wideband distributed power amplifier using 90nm SiGe.

3.2 Technology

The wideband DPA is implemented using Tower Semiconductor 90 nm SiGe BiCMOS platform (SBC18S5L). The process has HBTs having a peak f_T of 255 GHz. The backend is composed of an all-aluminium seven metal layer stack with metal-insulator-metal (MiM) capacitors and TiN resistors.

Inductors employ the top M7 layer, and for the ground, merged M1/M2 layers are used to increase the inductor Q. All the inductors, capacitors and HBT interconnects are modelled using Integrand Software, EMX.

3.3 Design

In conventional power amplifiers, high output power is obtained by using large transistors and high supply voltages to create large voltage and current swings governed by the transistor maximum I-V relationship. In distributed power amplifiers, however, the transistors are distributed between the input and output ports, and the number sections are chosen according to the input transmission line losses. As the wave travels through the input transmission line, it will be reduced due to the transmission-line loss, and the section gain will not be sufficient to contribute to the output power. This sets the upper limit on the number of sections which are used.

To provide high power, a 16-section DPA stage is used at the output, considering the

input transmission line loss of that stage (Fig. 3.1), and the supply voltage of 2.8 V is fed from the RF output port using an external bias-tee.

The first and second stages are used as a driver amplifier to increase the small-signal gain while consuming a low amount of DC power. Each stage can deliver sufficient power to drive its succeeding stage so that the ultimate overall OP1dB is not deteriorated. Since the output power which is delivered from the first and the second stage are much lower than the output stage, a lower supply voltage of 1.8 V and 2.0 V are used, respectively, to reduce the overall power consumption. These supply voltages are delivered using a two-section DC feed as shown in Fig. 3.2. The DC feed structures provide a very low DC resistance to conserve power consumption. They also provide a wideband impedance of $\sim$35 Ω up to 90 GHz. The bandwidth at high frequencies are not limited by the DC feed.

At the output stage, a DC-feed is not used as in the first and second stages. This is mainly due to the lossy characteristics of the on-chip aluminum metallization which would result in a voltage drop at the collector of the output section reducing the output power delivered and the efficiency.

In distributed amplifiers, the maximum achievable bandwidth is dictated by the cutoff frequency of the artificial transmission lines (ATLs) which is expressed as:

$$f_c = \frac{1}{\pi\sqrt{L \cdot (C + C_{par})}}, \tag{3.1}$$

where L and C are the inductance and capacitance of the ATL and C_{par} is parasitic capacitance induced by the transistor sections. To increase the cut-off frequency, the capacitive load introduced by the ATL inductors themselves must also be minimized. In the design, most of the ATL employ narrow 5 μm width inductors having sufficient margin for electro migration rules and providing low additional capacitance. However, for the output ATL for stage 3, 7.5 μm-width inductors are used due to the higher current. Also, to reduce the HBT capacitive loading, small 3 μm emitter length devices are used throughout the design for wide bandwidths.

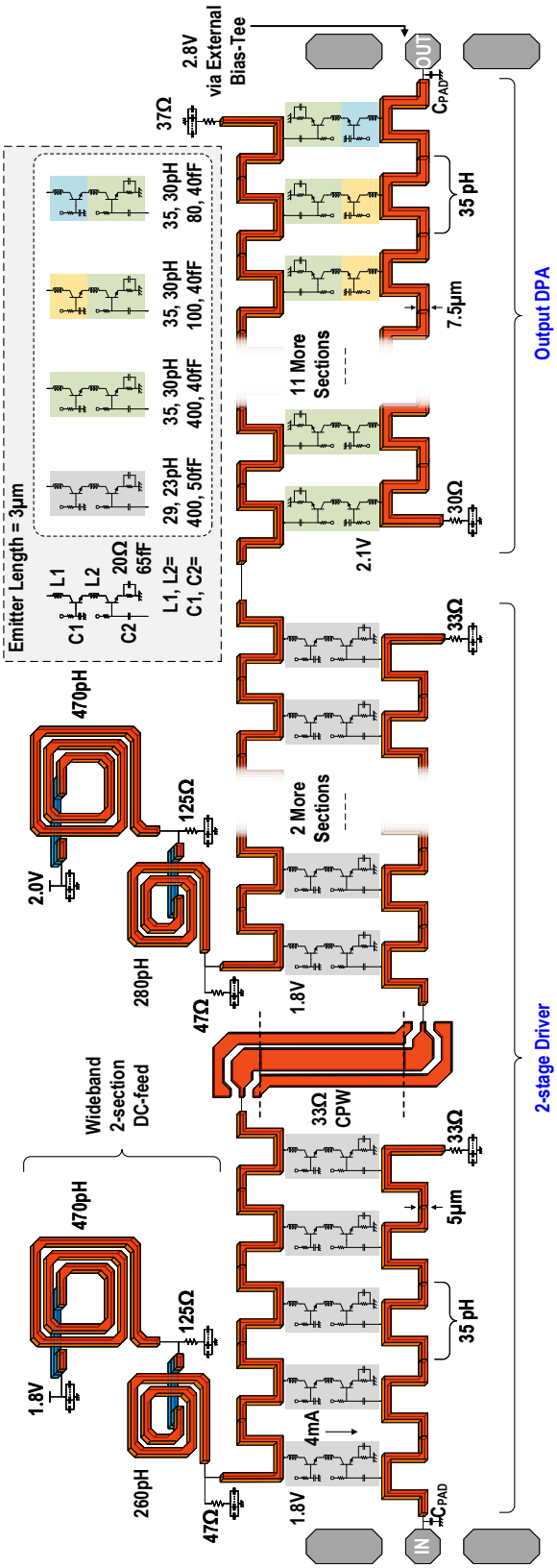


Figure 3.2: Schematic of the wideband 3-stage DPA

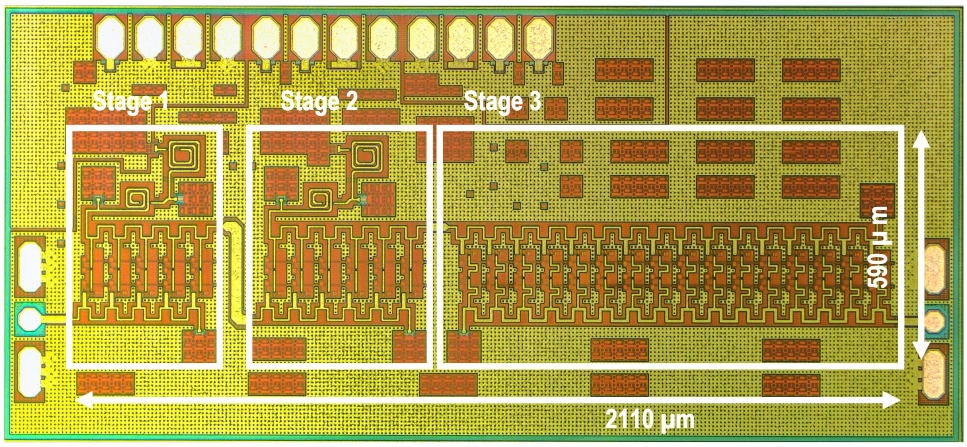


Figure 3.3: Die photo of the wideband DPA.

The ATL characteristic impedance is chosen considering the power delivered by the sections and the input and output return losses. The characteristic impedance is determined by:

$$Z_0 = \sqrt{\frac{L}{C + C_{par}}}. \tag{3.2}$$

With L=35pH and C+C_{par}=25fF, a Z0 and fc of ∼37 Ω and 340 GHz are obtained.

Since the single HBT devices have a finite Cbc capacitance, the stage sections employ cascode topology to improve the isolation between the input and the output ATLs. The ATL loss are compensated by adding inductors, L1/L2, at the collectors of the cascode HBTs [18]. To reduce the loading effect of the base-emitter capacitances, 40-50 fF series capacitors (C2) are also added between the HBT bases and the ATL. Also, RC (20 Ω and 65 fF) emitter degeneration networks are used to reduce the resistive and capacitive loading, and they also work as a peaking network to further enhance the bandwidth.

3.4 Measurements

Fig. 3.3 presents the DPA with chip dimensions of 2.4×1.0 mm^2 including the pads. The active circuit size is 2.11×0.59 mm^2. The amplifier employs a GSG input and output pads, and all measurements are calibrated to the probe tips.

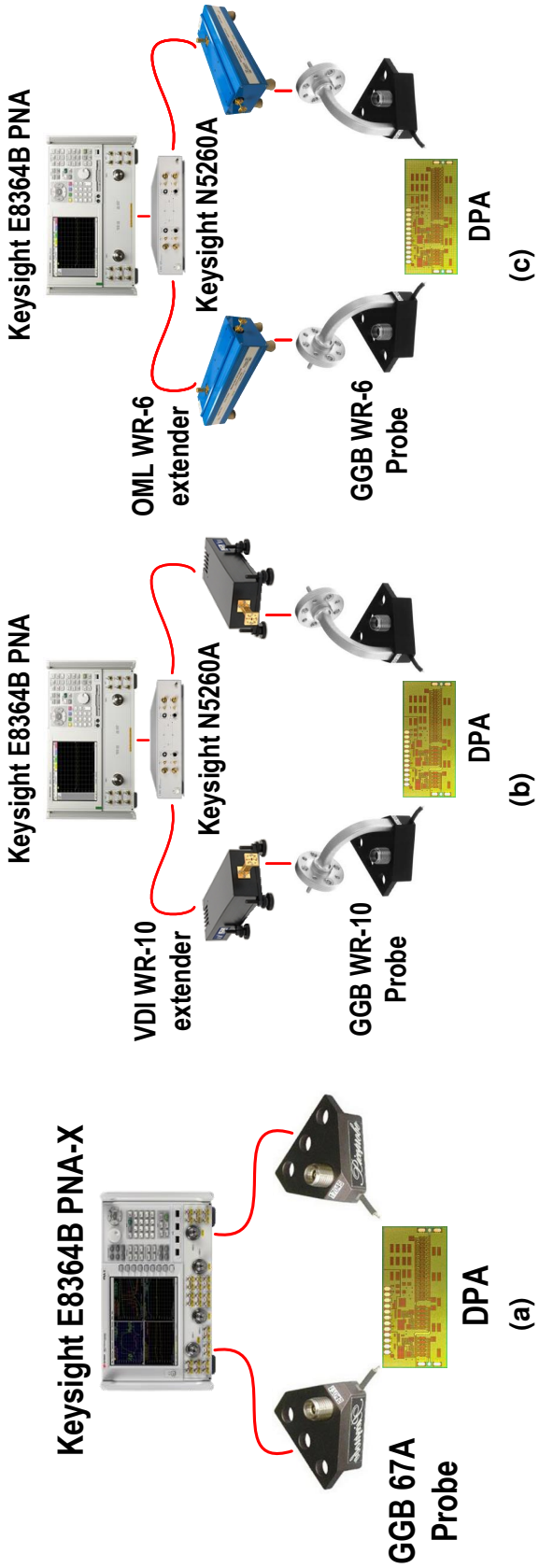


Figure 3.4: Small-signal mesurement setup for the DPA: (a) up to 70 GHz, (b) 70-110 GHz, (c) higher than 110 GHz

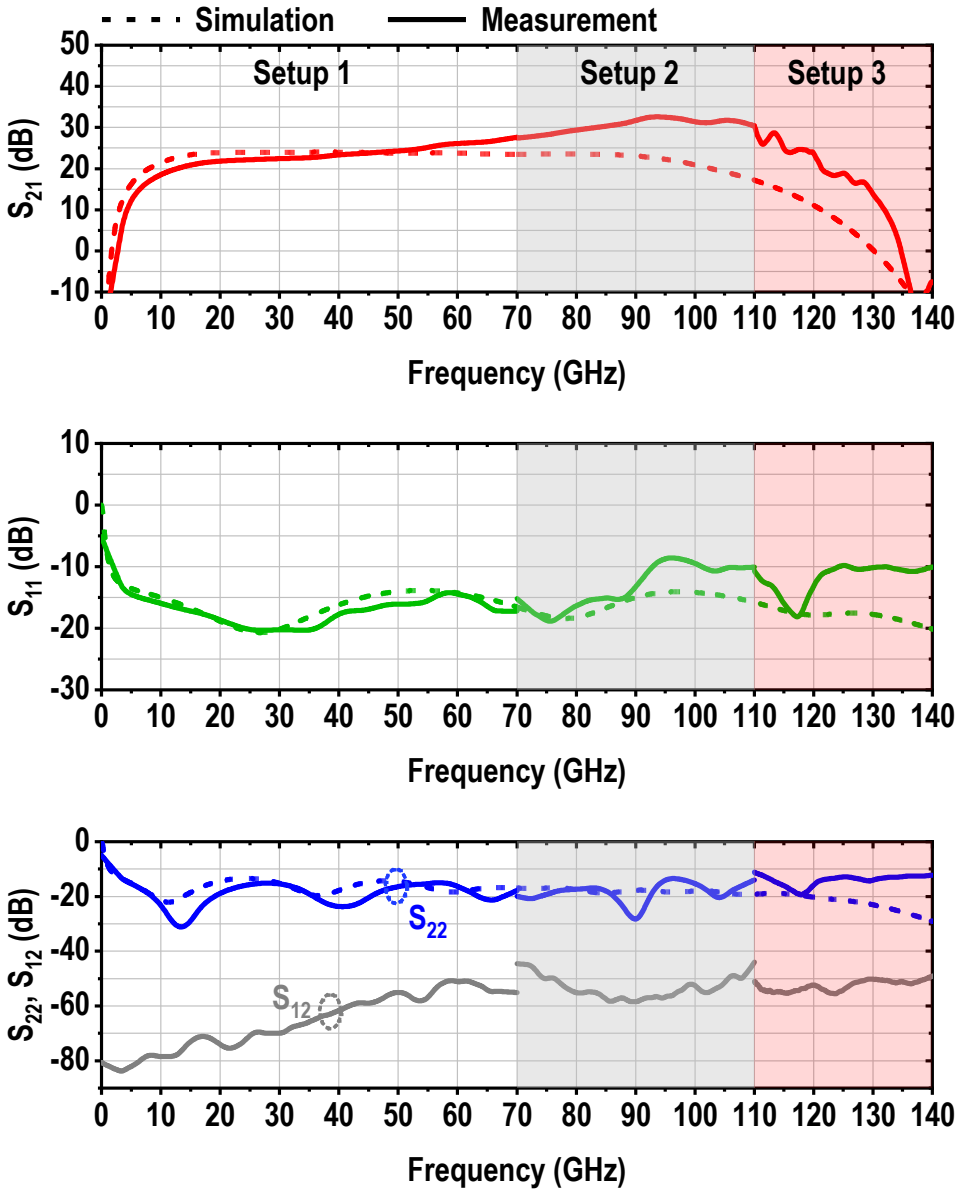


Figure 3.5: S-parameter performance of the DPA

Small-signal and power measurements are performed using a Keysight N5247A PNA-X Network Analyzer. With this setup, the DPA performance up to 70 GHz is evaluated (Fig. 3.4a). Small-signal performance for 70-110 GHz is evaluated using a setup containing a Keysight E8364B PNA Network Analyzer, a Keysight N5260A Millimeter Head Controller, and Virginia Diodes WR-10 75-110 GHz extenders (Fig. 3.4b). For frequencies higher than 110 GHz, OML WR-6 frequency extenders are used (Fig. 3.4c).

The measured S_{21} is 18-23 dB at 10-30 GHz and monotonically increases to a peak of 33 dB at 93 GHz. The circuit has average gain of $\sim$27 dB between 10-130 GHz. Considering the average gain, the circuit has the largest GBW (2.6 THz) compared to the other state-of-the-art SiGe DPAs. The return losses are better than $\sim$10 dB up to 140 GHz. Also, the reverse isolation is greater than the gain of the amplifier, ensuring the unconditionally stable operation. Measurements of k ($>$1) and mu (not shown) confirm unconditional stability at all frequencies, even at 90-110 GHz in the region of peak gain.

There is a discrepancy between the simulated and measured results at frequencies higher than 60 GHz. This is due to the improper modelling of the inductors inside the gain section, causing peaking at high frequencies. The peaking might also be caused by the RC network used for the emitter degeneration. We are currently investigating this with additional electromagnetic analysis to take into accounts multiple sections and multiple couplings between inductors.

Large-signal performance is evaluated using the measurement setup shown in Fig. 3.6. High frequency power is generated using a VDI AMC-334,335 multiplier chains and that power is monitored using Keysight W8486A power sensor. The output power of the DPA is monitored using VDI PM4 power meter.

The OP1dB and OIP3 performance is shown in Fig. 3.7. The circuit achieves a an OP1dB of 11.5-13.1 dBm at 10-67 GHz. As a sanity check for the measured OP1dB, the OIP3 is also measured, and it is around 10 dB higher. Both agree well with simulations.

Fig. 3.8 shows measured OP1dB and OPsat on another sample, and it also reports power added efficiency (PAE) at specific frequencies. The circuit achieves a PAE of 7.33% at 22.4 GHz at OP1dB of 13.1 dBm, and a PAE of 10.9% at OPsat of 14.5 dBm. The average PAE at P_{sat} is $\sim$10% up to 50 GHz.

The DPA is compared to other state-of-the-art SiGe DPAs in Table 3.1. The proposed DPA achieves the largest GBW of 2.6 THz among other SiGe distributed amplifiers with acceptable OP1dB and Psat and a high PAE up to 50 GHz.

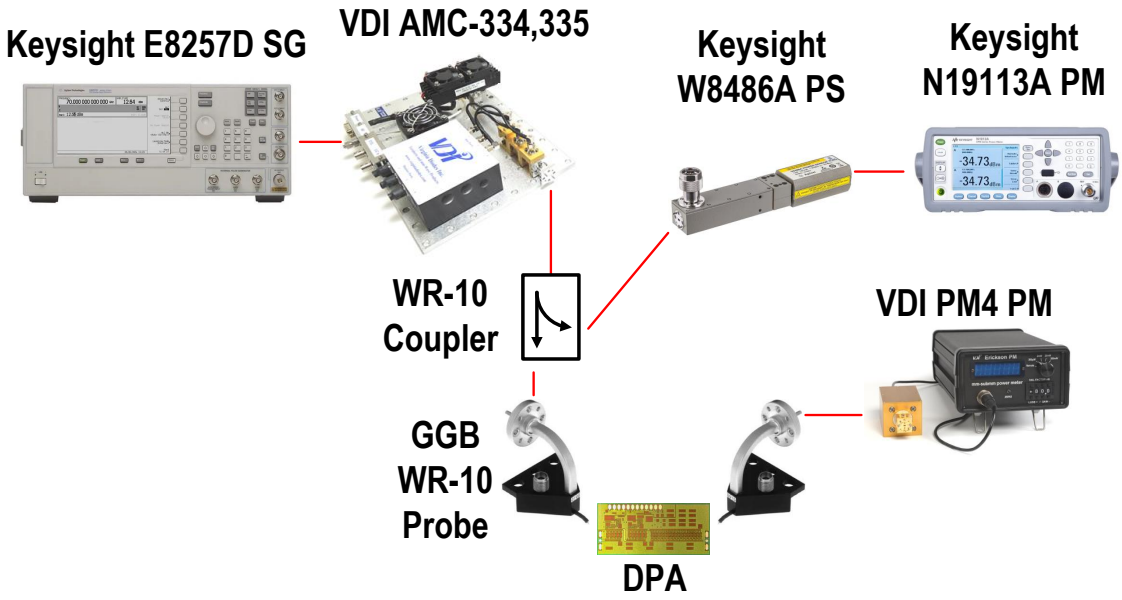


Figure 3.6: Large-signal mesurement setup for the DPA.

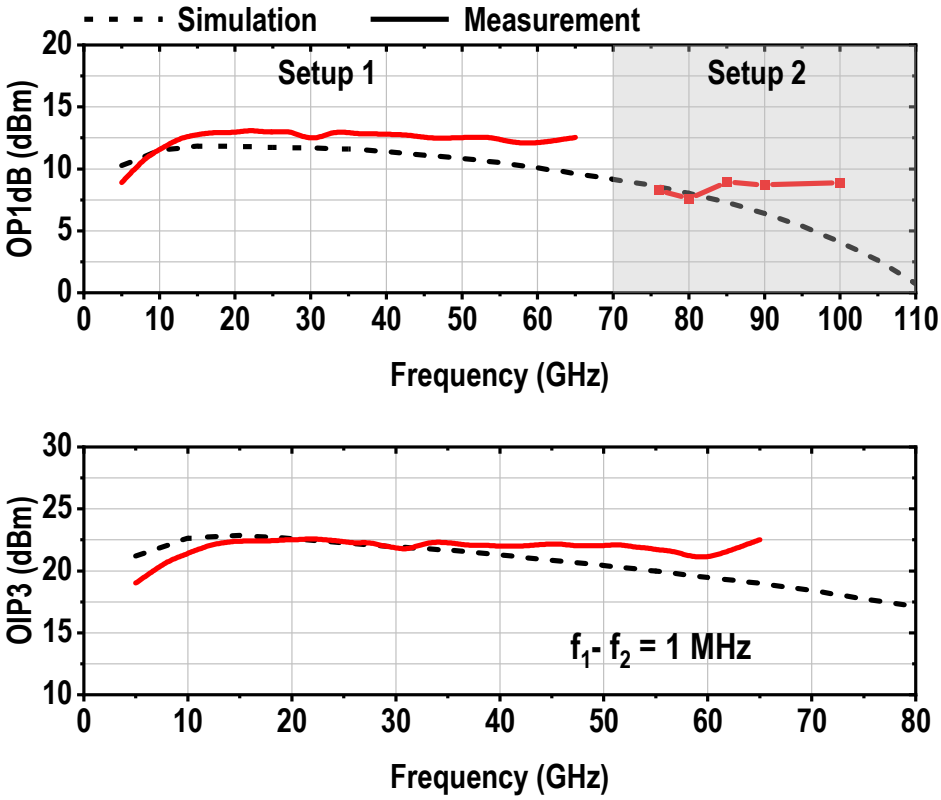


Figure 3.7: Measured and simulated DPA OP1dB and OIP3.

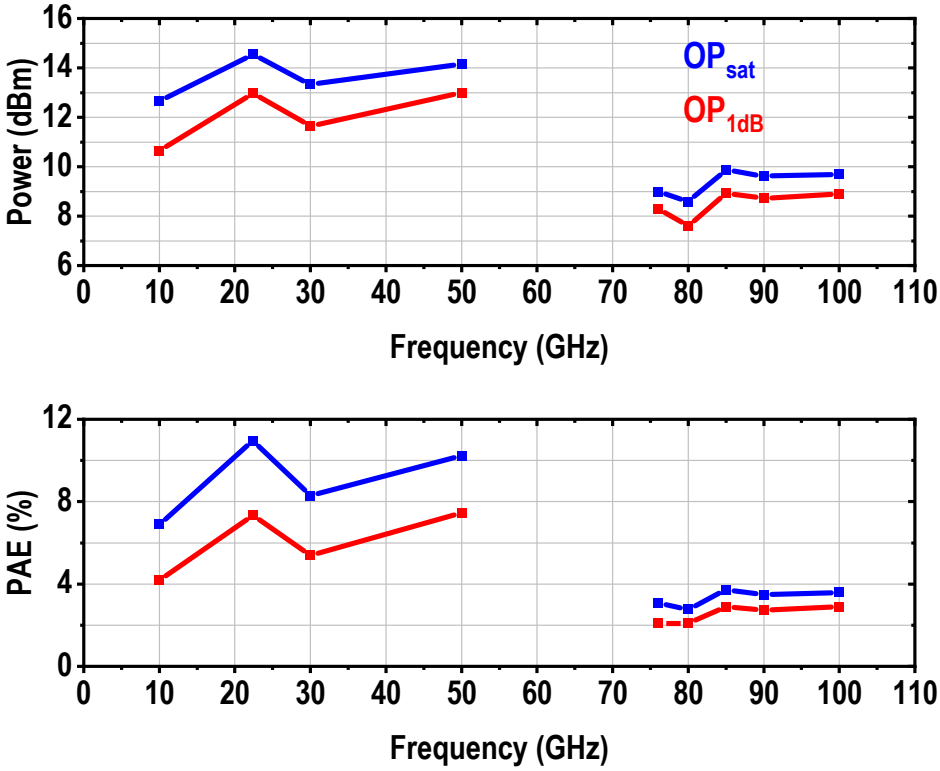


Figure 3.8: OPsat and PAE performance of the DPA.

Table 3.1: Comparison with State-of-the-art SiGe DPAs

Reference	Process	Gain (dB)	BW (GHz)	GBW (GHz)	Peak OP1dB (dBm)
[11]	90nm SiGe	12	91	362	14.9
[12]	130nm SiGe	10	110	348	16.7
[13]	130nm SiGe	10	170	537	8.2[a]
[14]	130nm SiGe	24	95	1500	N.R.
[15]	130nm SiGe	19	160	1515	N.R.
[16]	130nm SiGe	13	170	759	N.R.
[17]	130nm SiGe	18.7	180	1550	N.R.
This work	90nm SiGe	27	120	2577	13.1

N.R. = Not Reported
[a] Estimated from plots

3.5 Conclusion

A 10-130 GHz DPA is presented. To enhance the bandwidth, peaking inductors and parallel RC degeneration are used on every stage. Measurements indicate that the DPA exhibits the largest GBW product compared to the state-of-the-art SiGe DPAs, while delivering a relatively high power and high PAE.

3.6 Acknowledgement

This work was supported by the DARPA T-MUSIC program. The authors thank Tower Semiconductor for the chip fabrication, Integrand Software for the use of EMX and Keysight for the measurement equipment and software.

Chapter 3 is, in full, a reprint of the material as it appears in: O. Kazan and G. M. Rebeiz, "A 10-130 GHz Distributed Power Amplifier Achieving 2.6 THz GBW with Peak 13.1 dBm Output P1dB for Ultra-Wideband Applications in 90nm SiGe HBT Technology," *2021 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)*, 2021, pp. 1-4. The dissertation author was the primary investigator and primary author of this paper.

Chapter 4

An 8-channel 5-33 GHz Transmit Phased Array Beamforming IC With 10.8-14.7 dBm Psat for C, X, Ku and Ka-band SATCOM

4.1 Introduction

The demand for communications is increasing worldwide leading to the necessity for better coverage and the availability of internet access across the globe. This also include terminals on planes and ships, where satellite systems, with their ubiquitous coverage over oceans, are used.

Current satellite communication (SATCOM) systems enable high data rate and low latency communications with low Earth-orbit (LEO) and medium Earth-orbit (MEO) satellites, and allow for a feasible solution for underserved areas. Ground terminals for LEO and MEO satellites need to constantly track the satellite as it moves across the sky, and this is best done using electronically scanned phased arrays as compared mechanical solutions such as dishes on motorized pedestials. There are multiple frequencies used for SATCOM transmit systems: C-band (5 GHz), X-band (8 GHz), Ku-band (14 GHz) and Ka-band (29 GHz) (Fig. 4.1). A ground terminal which covers all satellite bands in a single system simplifies the hardware complexity, allows for worldwide operation over multiple providers, and reduces the overall

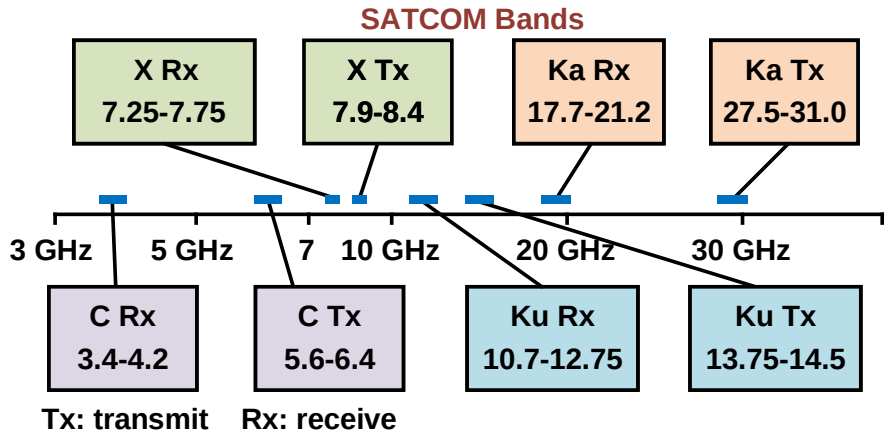


Figure 4.1: C, X, Ku and Ka-band SATCOM frequencies for commercial and defense systems.

terminal cost.

Single-band phased-arrays were demonstrated before at Ku and Ka-band with high performance [19, 20, 21, 22]. This work targets wideband beamformer chips and phased-arrays, and is an expanded version of [23]. The beamforming IC covers the C, X, Ku and Ka SATCOM bands in a single chip for next-generation phased-array systems. The 8-channel chip is compact (3.9×4.7 mm^2) with 0.4 mm chip scale-package and fits well in a 2×2 (quad) phased-array grid up to 32 GHz.

To author's knowledge, the beamforming IC and phased-array demonstrator achieve the widest Tx bandwidth covering C, X, Ku and Ka SATCOM frequencies.

4.2 Eight-Channel Wideband Beamformer

Fig. 4.2 presents the wideband 8-channel Tx beamformer. The input power is distributed to the channels using a wideband two-section Wilkinson network, followed by a single-ended to differential converter (S2D). The channels are all differential to improve isolation, and contain a wideband variable gain amplifier (VGA), a 5-bit phase shifter and a wideband two-stage power amplifier (PA). The outputs are also differential which improves the stability over a wide frequency range. Also, wideband antennas are differential in nature, and differential output ports

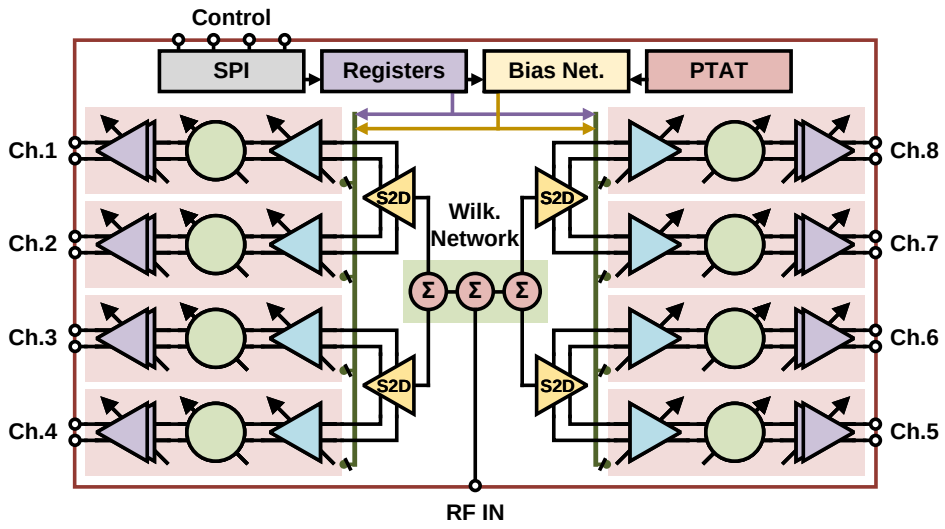
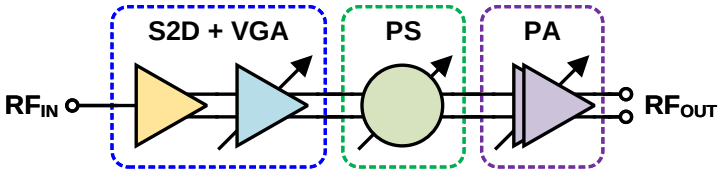


Figure 4.2: Block diagram showing the SATCOM wideband beamforming IC.



	S2D + VGA	PS	PA	Channel	Chip*
Gain (dB)	12	-2	28.5	38.5 dB	28.5 dB
IP_{1dB} (dBm)	-16	-4	-14	-25 dBm	-15 dBm
OP_{1dB} (dBm)	-5	-7	13.5	12.5 dBm	12.5 dBm

*includes Wilkinson network division and ohmic loss

Figure 4.3: Gain and output compression point assignment for each block in the phased-array transmit channel.

eliminate the use of wideband baluns and result in a more efficient system.

The overall chip electronic gain is targeted to be 24 dB including the Wilkinson network division and the ohmic loss. Also, a maximum OP1dB of 12 dBm is aimed. With these goals, the small-signal gain and the OP1dB assignments to the individual channel blocks are determined as in Fig. 4.3. The channel gain is designed to be 38.5 dB which translates to a chip electronic gain (Pout-channel/Pin common port) of 28.5 dB when 6 dB of Wilkinson division loss and 4 dB of ohmic loss are taken into account in the passive power distribution network.

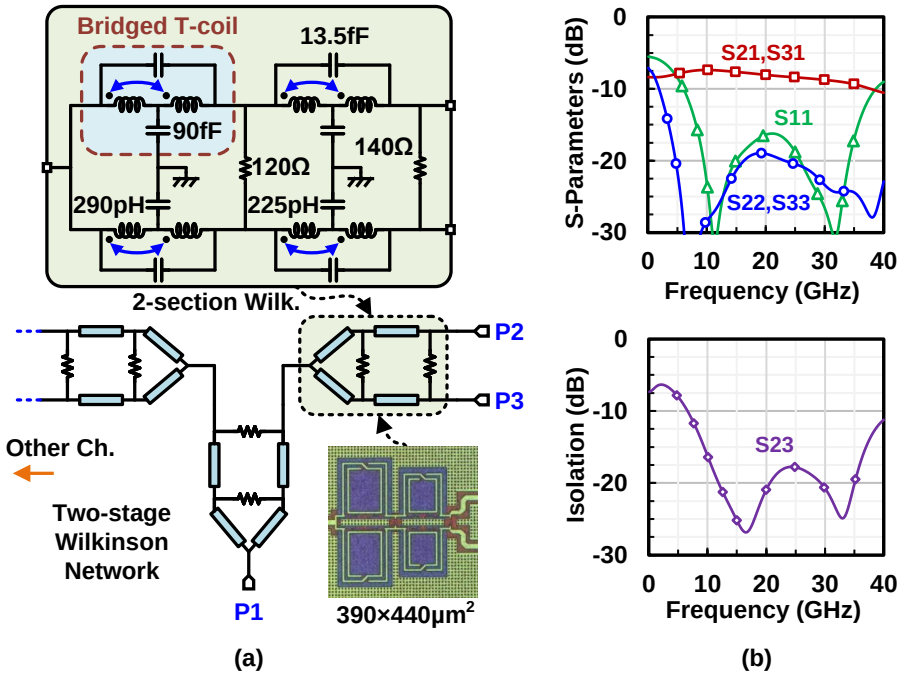


Figure 4.4: (a) Lumped Wilkinson network and (b) simulation results.

4.2.1 Technology

The chip is implemented in the Tower Semiconductor 90 nm SiGe BiCMOS process (SBC18S5) with 7 aluminum metal layers [24]. The top two metal layers (M7/6) are used for high Q inductors (Q $\sim$ 16 at 25 GHz). There are also MIM capacitors with density of 2.8 fF/μm^2 in the process. All the inductors, capacitors and the transmission lines (TLs) are modelled using Integrand Software EMX with the Cadence Suite. The simulated f_T and f_{max} of a 3μm emitter length HBT are 245 GHz and 304 GHz, respectively, at 1.5-2.0 mA/μm current density.

4.2.2 Wilkinson Network and Active Balun

The input power is first distributed using a 1:4 Wilkinson network (Fig. 4.4). To reduce size and meet the wide bandwidth requirement, two-section Wilkinson network with lumped bridged T-coils are used instead of distributed $\lambda/4$ transmission line sections [25]. The 1:4 divider network insertion loss (ohmic loss) is 1.8-3.8 dB at 5-33 GHz and does not include the 6 dB division loss. The isolation between neigboring ports (S_{23}) is >8 dB at 5 GHz and >12 dB at

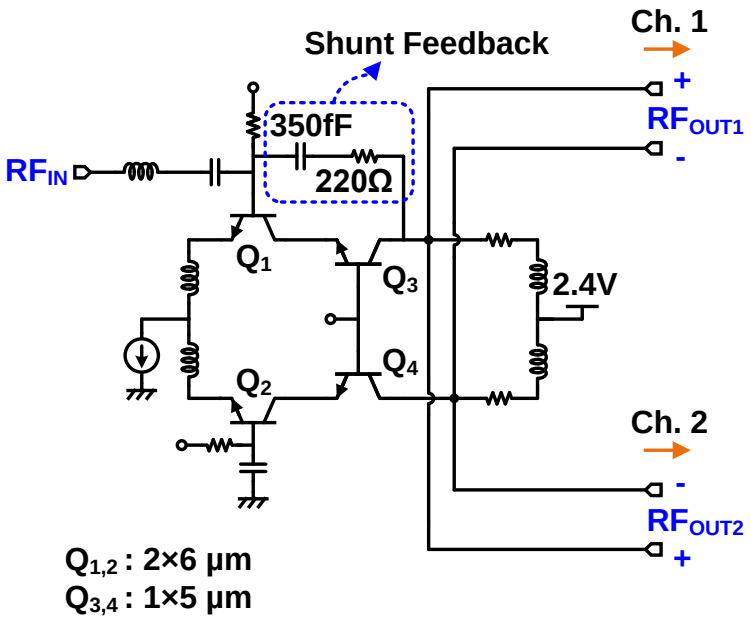


Figure 4.5: Wideband active balun with two output ports.

8-33 GHz. This is acceptable as the S2D is well matched at low frequencies. The increase in the insertion loss from 1.8 dB to 3.8 dB at 5-33 GHz is compensated by increasing the channel gain at high frequencies, resulting in a nearly flat response.

The Wilkinson network is followed by an active balun (Fig. 4.5). The active balun employs a fully differential cascode amplifier topology with one input being AC-grounded. The single-ended to differential conversion is ensured by the common-mode rejection of the tail bias current source. The wide bandwidth is achieved by employing a shunt 220 Ω and 350 fF feedback. The common-mode rejection is 16.2-18.6 dB at 5-33 GHz.

4.2.3 Variable Gain Amplifier

The variable gain amplifier employs current steering topology with ∼15 dB gain control using a 4-bit DAC (Fig. 4.6). A 200Ω/400fF mismatch compensation network is added to one polarity of the RF input. These mitigate the effect of the imbalance induced by the shunt feedback in the S2D block.

The VGA and the S2D are designed as a single block, and the differential and common-

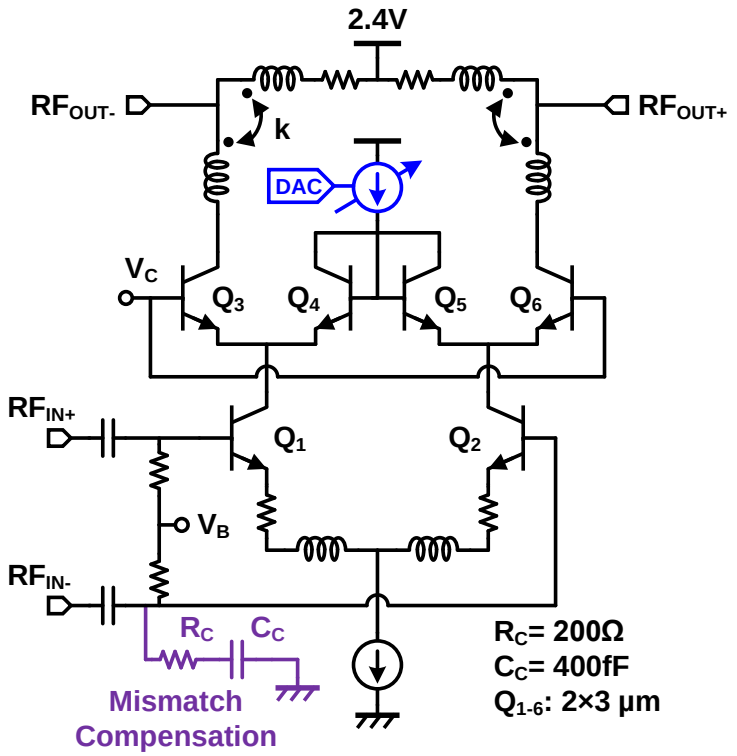


Figure 4.6: Wideband current-steering variable gain amplifier.

mode gain of the S2D+VGA are 5-10.2 dB and -17 to -7.4 dB at 5-33 GHz, respectively, resulting in a common-mode rejection of 21-17.6 dB, and ensuring a reasonable purity for the differential signal.

4.2.4 Active Phase Shifter

The active phase shifter employs a vector modulator architecture with a quadrature all-pass filter (QAF) (Fig. 4.7). The I/Q signals are generated by the QAF network and fed to two variable gain amplifiers with current-steering topology, and the output signals are added in the current mode.

For wideband operation, de-Q series resistors are used for the inductors in the QAF network [27]. This degrades the noise figure (NF) and gain by $\sim$3 dB but is required for wideband operation with low I/Q errors. The QAF network is followed by an LC compensation network to introduce a nearly resistive interface to the VGAs. Note that the VGAs employ an

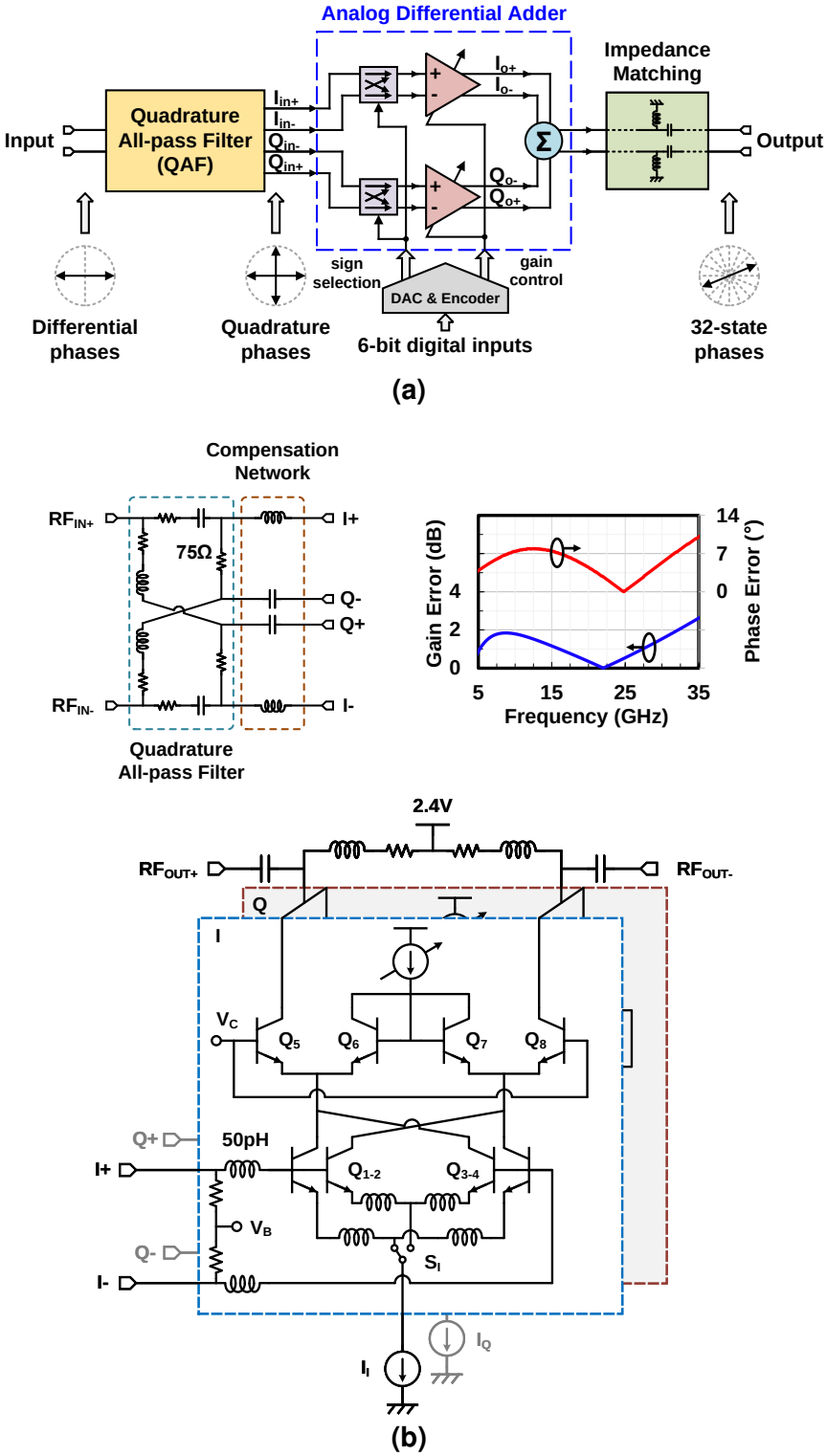


Figure 4.7: (a) Vector modulator architecture [26], (b) wideband phase shifter with emitter inductors for low noise operation.

emitter inductor to lower their noise figure and increase their input impedance (and make it resistive)[28]. The bottom HBT devices are activated by turning on the bottom current mirrors using quadrature switches. These enable changing phase states to all four different quadrants.

The phase shifter has simulated small-signal gain of 1.6-4.5 dB and an NF of 8.4-11 dB at 5-33 GHz. An I/Q error of up to 2.2 dB and 8.3° is present over the entire bandwidth, which is relatively high. This is due to the use of a single-stage LC I/Q network for a 6.5:1 bandwidth design, and a better response can be achieved using a 2-stage LC I/Q network. Therefore, a 6th bit is employed in the VGA current steering to compensate for the I/Q error, and this results in true 5-bit operation at 5-33 GHz (different 32 phase shifter states are chosen for different frequency bands). The circuit consumes 52 mW ($\sim$10 mA in each branch) and has a peak OP1dB of -7.1 dBm at 5-33 GHz.

4.2.5 Power Amplifier

The wideband power amplifier is designed as two conventional differential cascode amplifiers due to the small size requirement for the phased-array channel (Fig. 4.6a). The driver stage and output stage both employ resistive shunt feedback to increase the bandwidth of operation. A tail current source is not implemented in the PA design to improve the voltage headroom and to increase the output power, leading to a pseudo-differential operation and a class AB design.

The common-emitter HBT devices also include 200/100Ω resistors ($R_{b1/2}$) at their base feeds. These are effectively shunted to ground in RF operation and intentionally reduce the small-signal gain to improve the wideband stability. Also, shunt RC networks ($R_{a1/2}$ and $C_{a1/2}$) are added at the input to degrade the small-signal gain at $>$40 GHz, again for stability. Without this network, the PA would have gain up to 60 GHz resulting in potential instabilities when packaged. The RC and 200/100Ω stability-improvement networks are implemented only at the input sideof the driver and output stage amplifiers so as not to degrade the output power level but do reduce the amplifier efficiency by 3-5%.

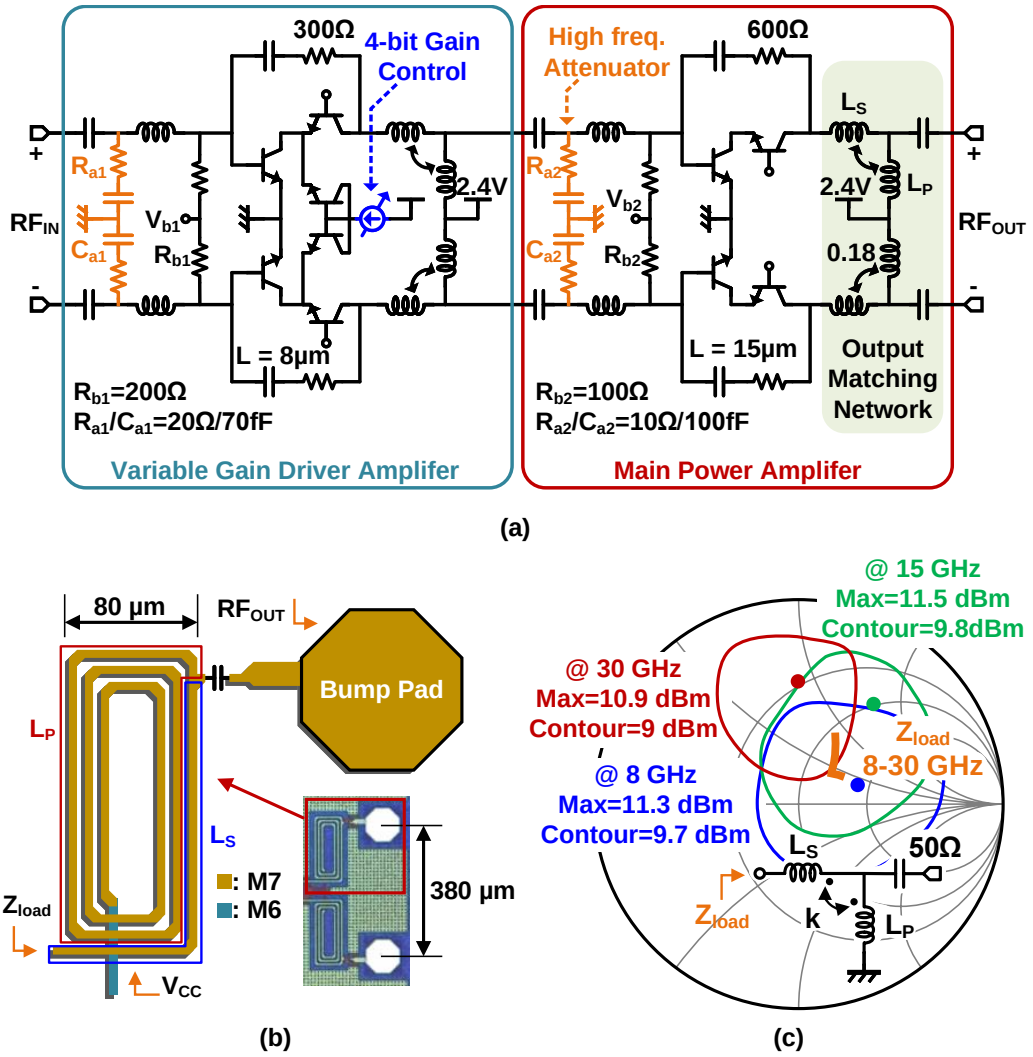


Figure 4.8: (a) Schematic of the wideband two stage differential power amplifier (b) Layout of the output stage load inductor (c) Load-pull analysis of the output transistor.

Bridge T-coil loads are implemented at the output of both the driver and power amplifiers. The inductor L_S eliminates the usage of an extra transmission line (and hence extra loss) to the pad from the PA output and contributes to the wideband match. The T-coil at the output stage is designed to result in a wideband load impedance to within ∼2 dB from the optimum OP1dB load impedance at 8, 14 and 30 GHz, ensuring a wideband power match (Fig. 4.8c).

A breakout PA testcell is measured on a probe station with the on-chip transmission line losses deembedded (Fig. 4.9a). The measured two-stage power amplifier has a small-signal gain of 19.2-23.8 dB at 5-33 GHz, and an OP1dB of 9.1-14.8 dBm as shown in Fig. 4.9(a)-(c).

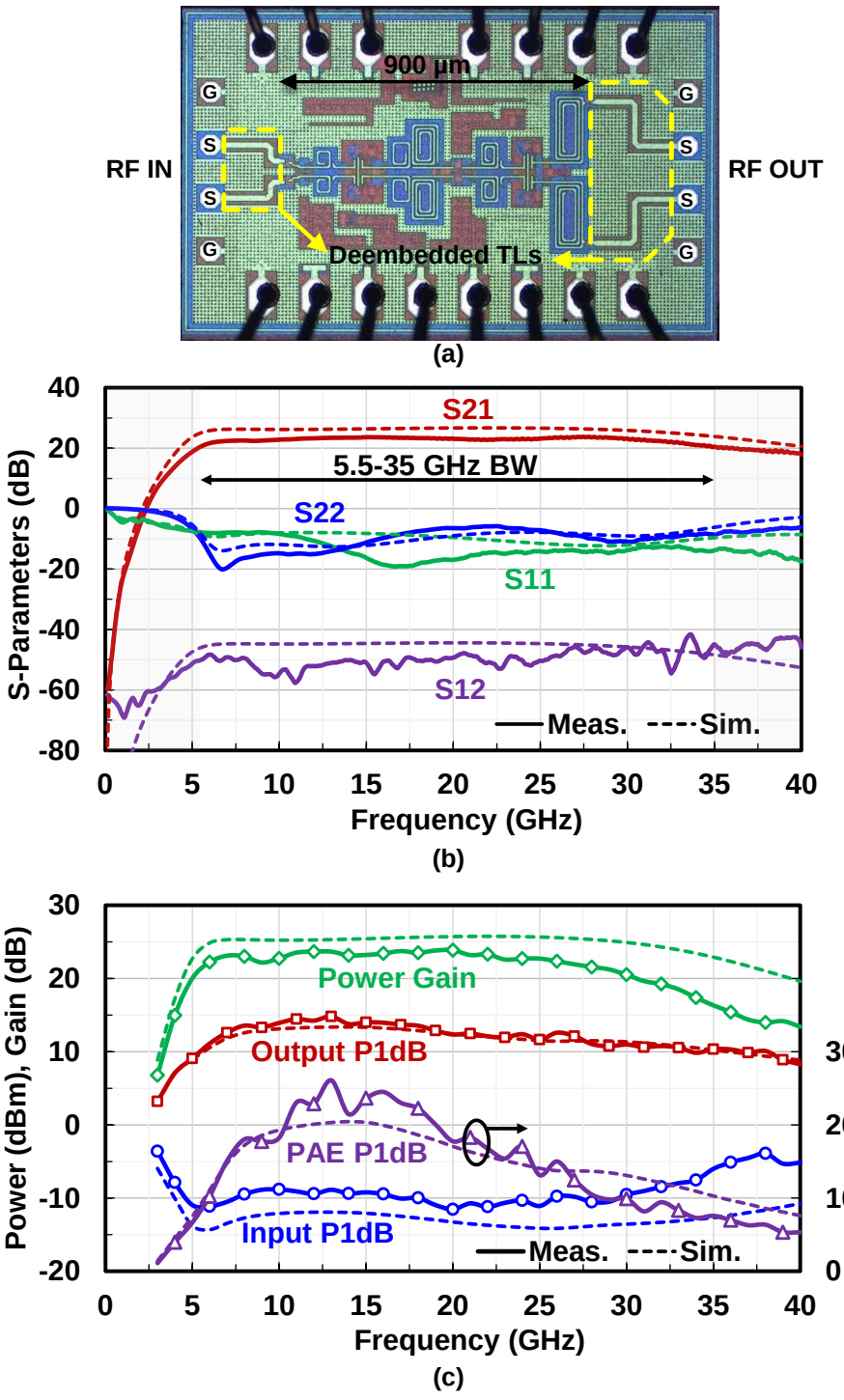


Figure 4.9: (a) Die photo of the wideband PA breakout cell (chip size: 1.45 by 0.86 mm^2), (b) small-signal performance of the PA, (c) large-signal performance of the PA.

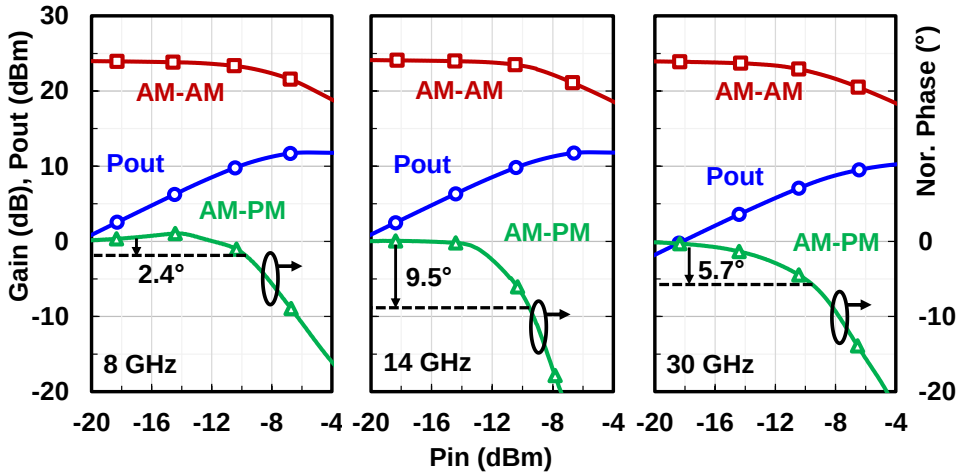


Figure 4.10: Measured PA breakout cell: 8, 14 and 30 GHz AM-AM and AM-PM distortion performance.

The PA consumes 115 mW from a 2.4 V supply at PAE, resulting in a maximum PAE of 26.1% at 13 GHz. The PAE is >9% from 5-33 GHz, which is acceptable for wideband low-power amplifiers. AM-AM and AM-PM distortion versus input power are shown in Fig.4.10. AM-PM distortions at P1dB are 2.3°, 9.5° and 5.7° at 8, 14 and 30 GHz, respectively, which is acceptable for SATCOM applications (5 GHz results are similar to 8 GHz). The two stage PA is compact and occupies an area of 0.43 mm^2.

4.3 Eight-Channel Beamformer Measurements

The 8-channel transmit beamformer is shown in Fig. 10 with SAC305 bumps and 380 µm pitch. The chip size is 3.9×4.7 mm^2 and is limited by the chip-scale package pitch. The small-signal and large-signal performance are obtained using a 4-port PNA-X (Keysight N5245B to 50 GHz) with a single-ended input (port 1) and differential outputs (port 2). The PCB traces and connector losses are de-embedded, and the reference planes are at the chip input and output ports (on the PCB). For the optimum gain/phase control and best PAE, the chip is operated at 80% of its nominal current bias and consumes 1.8 W with a 2.4 V supply at small signal. The power increases to 1.9 W at P1dB resulting in 240 mW per channel.

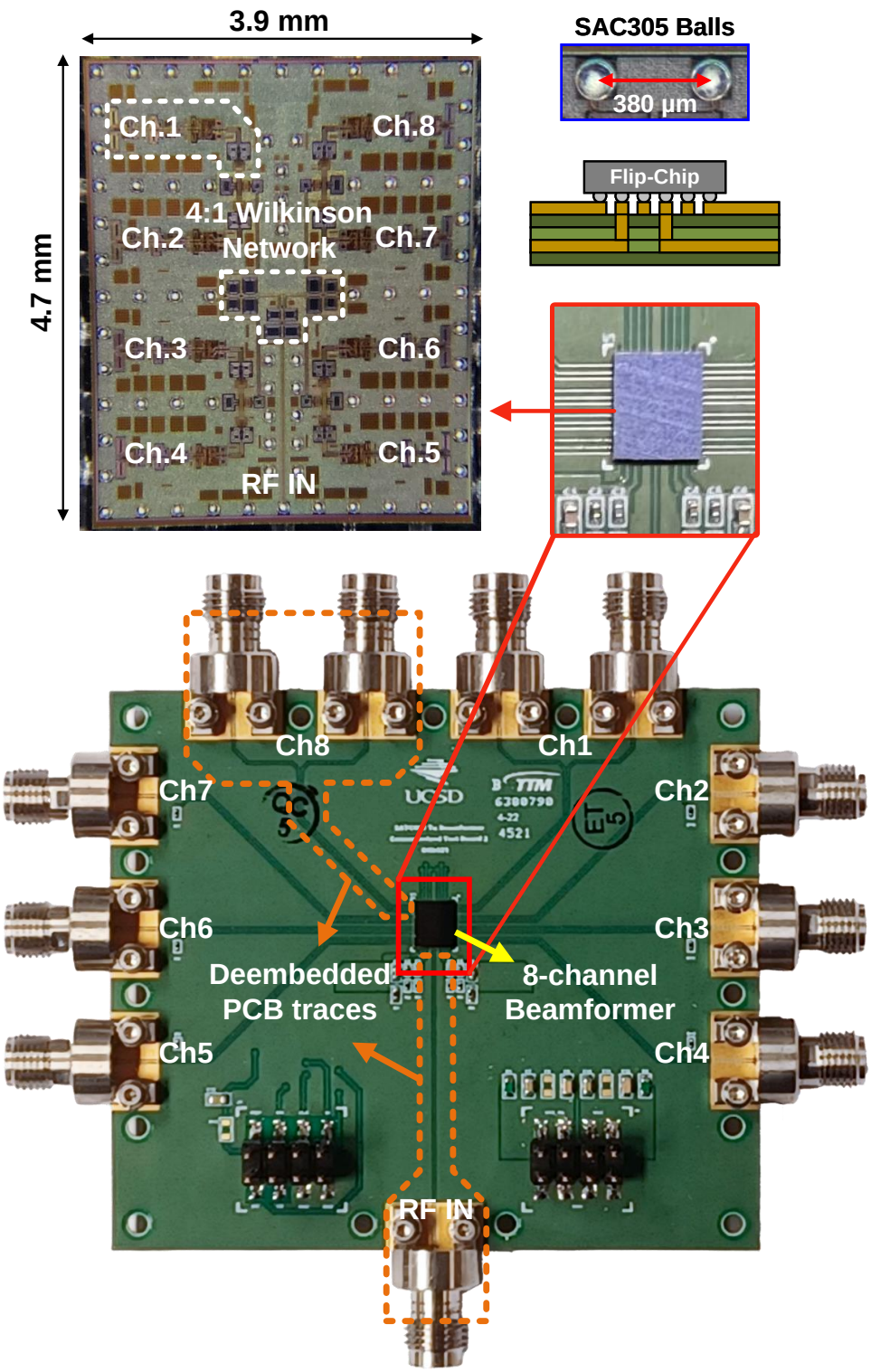


Figure 4.11: Beamformer die photo and beamformer evaluation PCB.

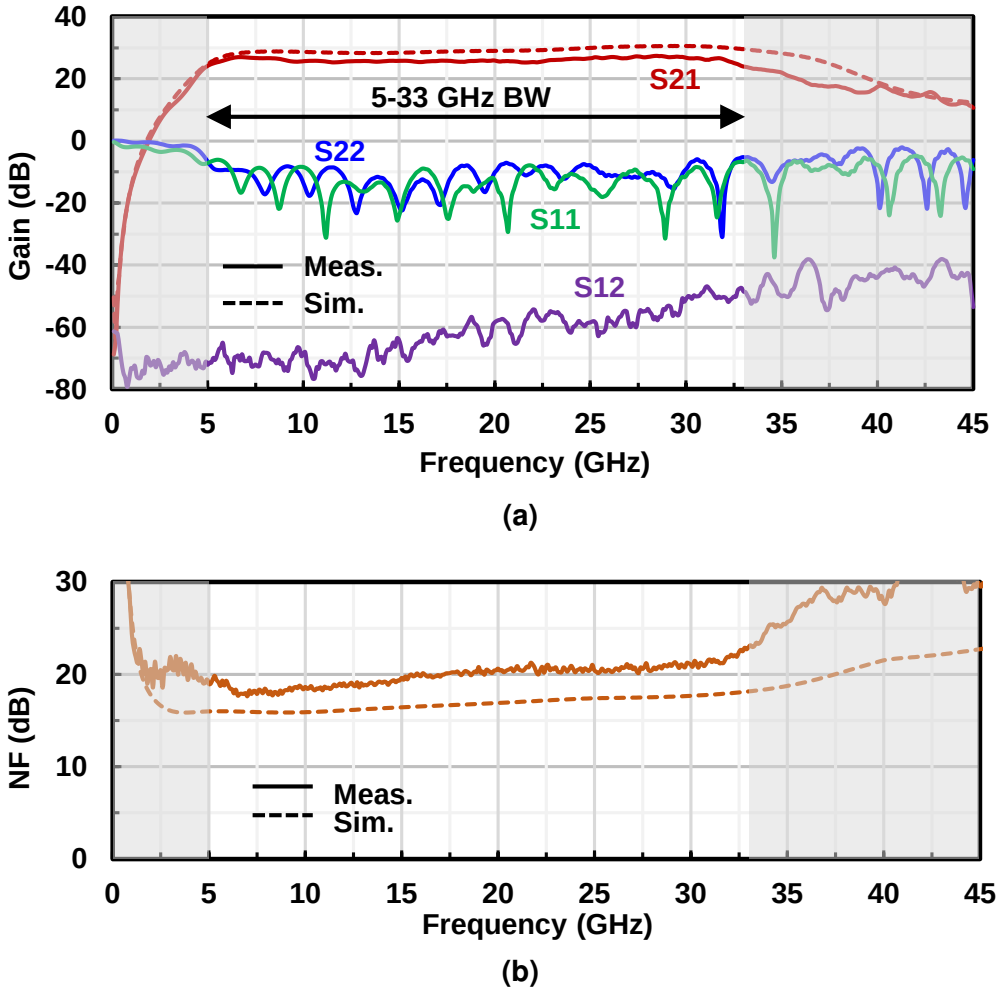


Figure 4.12: (a) S-parameters, (b) Noise Figure.

Fig. 4.12a presents the S-parameters of the 8-channel beamformer. The maximum electronic gain is 27.4 dB with a 3-dB bandwidth of 5-33 GHz, and all channels are within +/-1 dB of each other. The reverse isolation (S_{12}) is -48 to -70 dB at 5-33 GHz, ensuring unconditionally stable operation. The measured noise figure is 17.6-21 dB at 5-31 GHz (Fig. 4.12b) which is 1.6-3.6 dB higher than simulations. This is partly beacuse the Wilkinson network has higher loss than the simulated results which increases the input noise figure and reduces the electronic gain (see Fig. 4.13). The measured output noise at midband is -174+21+26=-127 dBm/Hz, which is excellent for phased-arrays, and agrees well with simulations of -174+17+29=-128 dBm/Hz (simulations have higher gain and lower NF resulting in the same output noise).

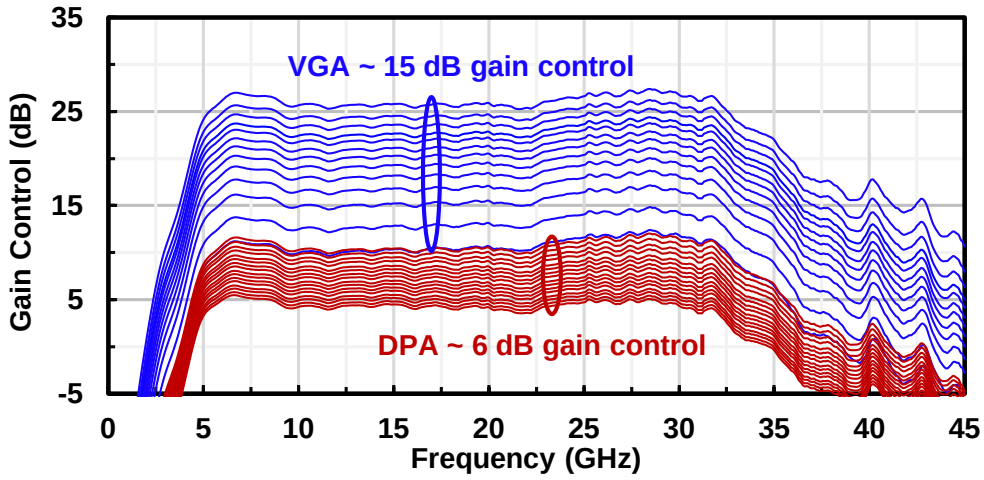


Figure 4.13: Gain control.

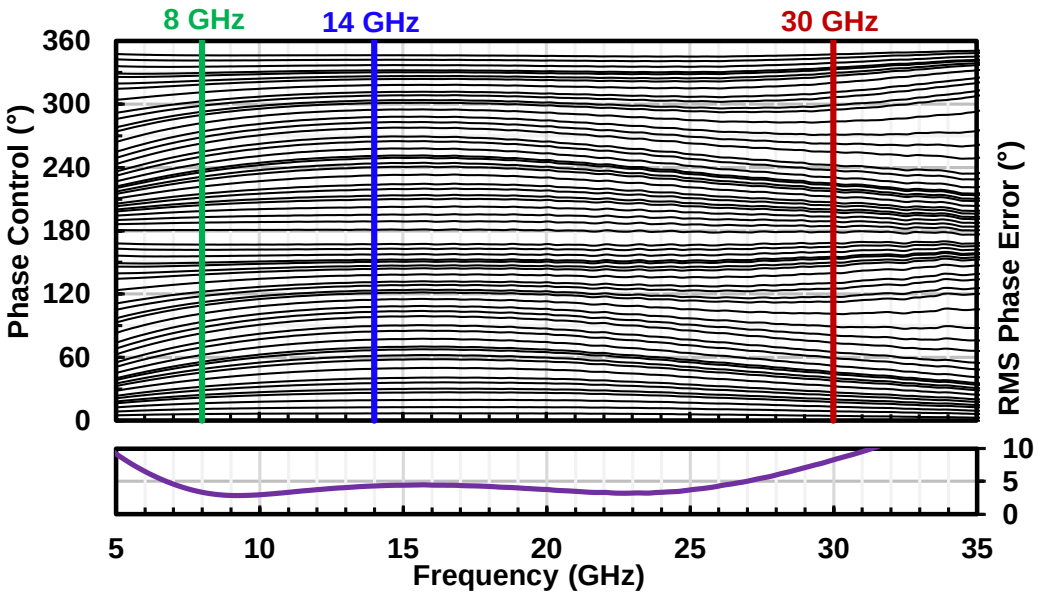


Figure 4.14: Phase control with 6 bits.

The gain control is shown in Fig. 4.13. The VGA and DPA (driver for the PA) have 15 dB (4 bits, 0.6-2 dB steps) and 6 dB (4 bits, 0.4 steps) gain control, respectively, resulting in 21 dB of gain control. The channel phase change is <1.4-4.7° at 5-30 GHz for 10 dB of gain control ensuring orthogonality between gain control and phase control.

Fig. 4.14 presents the measured phase performance over 64 phase states. The RMS phase error is 9.2/3.3/4.3/8.3° at 5/8/14/30 GHz and therefore, the phase shifter does not have a 6-bit

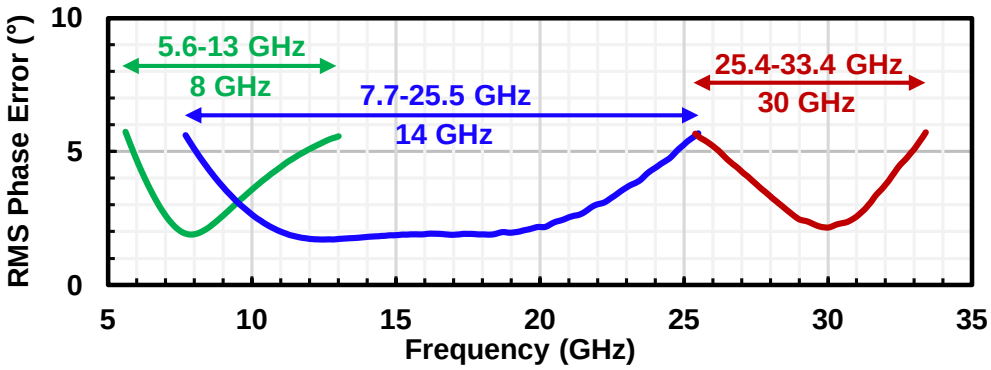


Figure 4.15: RMS phase error for 3 different phase-shifter settings.

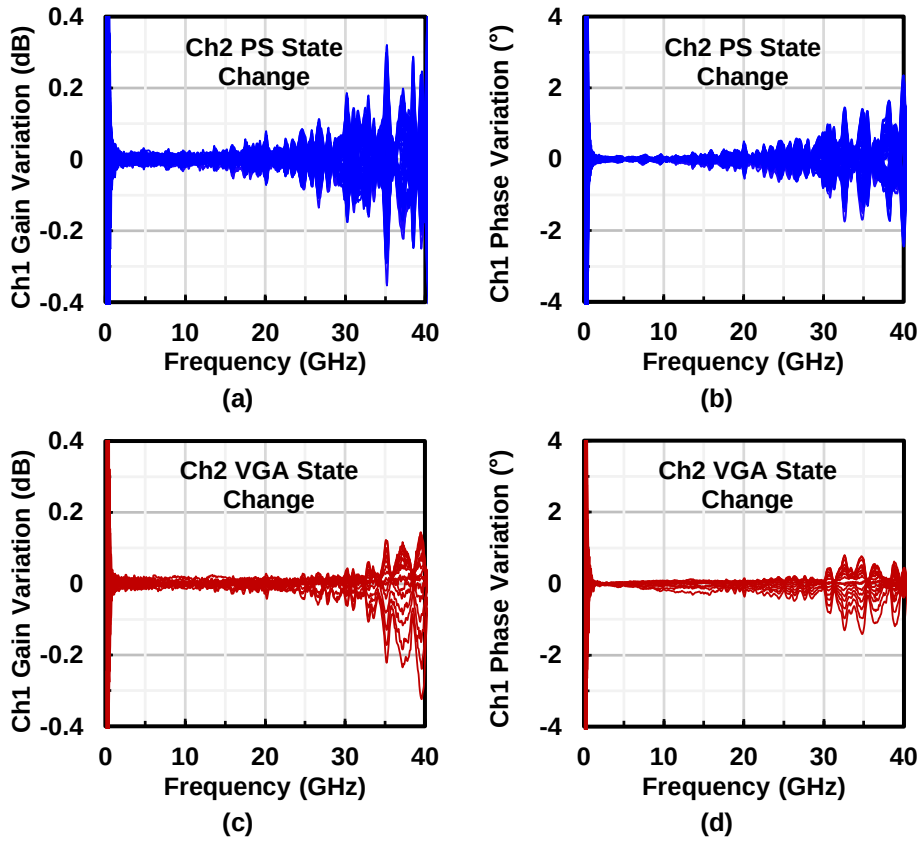


Figure 4.16: Channel 1 gain and phase variation due to Channel 2: (a)(b) phase shifter rotation at 0 to 360° and (c)(d) VGA change over 20 dB of gain control.

response over the entire band. The native 6-bit performance can be trimmed to 32 states at 8 GHz, 14 GHz and 30 GHz, and the RMS phase error is plotted in Fig. 4.15. One can see that 5-bit operation is achieved with an RMS error of <5.2° for each setting. The corresponding

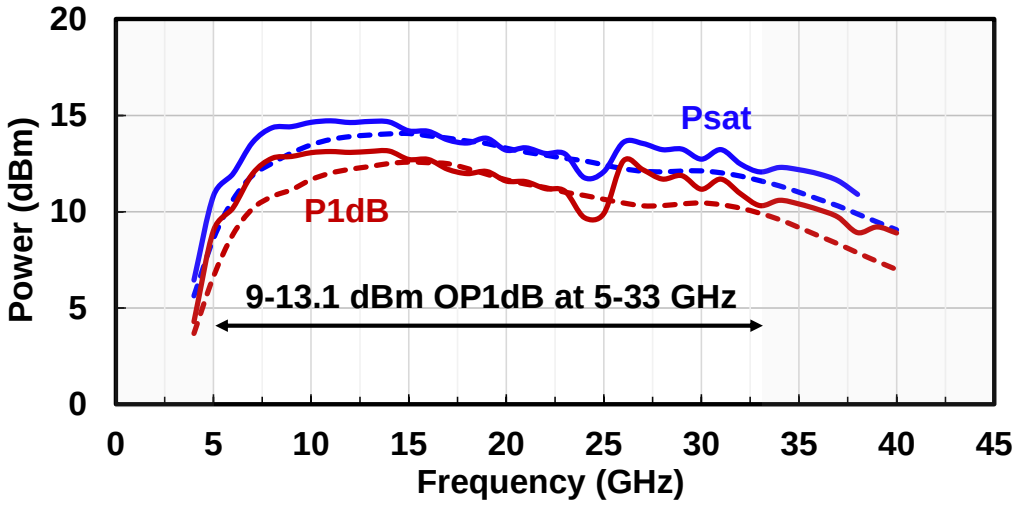


Figure 4.17: Measured P1dB and Psat performance of a beamformer channel.

RMS amplitude error is ∼1 dB for each case. Therefore, the phase shifter can operate in different frequency regions, each with wide bandwidth, with the selection of different 32 states out of the 64 phase states available in the response.

The channel-to-channel isolation is shown in Fig. 4.16. In this measurement, the worst-case scenario is considered where channel 1 response is measured while changing channel 2 gain and phase setting. Channel 1 and channel 2 are adjacent to the each other and are connected to the same S2D with potential coupling issues (Fig. 4.3). As can be seen, Channel 1 shows ±0.2 dB gain variation and ±1° phase variation up to 33 GHz when channel 2 is varied. This translates to a coupling of <-33 dB [34]. Note that this includes the chip, the transition to PCB and the close transmission-lines on the PCB. The channel-to-channel coupling on the chip alone was also measured using probes and is <-45 dB.

The beamformer chip delivers an OP1dB of 9-13.1 dBm at 5-33 GHz per channel with the peak occuring at 10-14 GHz (Fig. 4.17). In this measurement, the saturated output power (OPsat) is defined when the beamformer is driven 3 dB higher than the input 1dB compression point, and the output Psat is 11-14.1 dBm at 5-33 GHz with the peak also occuring at 10-14 GHz. The peak PAE is 8.5% at P1dB and 11.5% at Psat (10-14 GHz) and is >6% at 8-30 GHz (4.8% at 5-6 GHz). The kink around 25 GHz does not affect the intended SATCOM operating

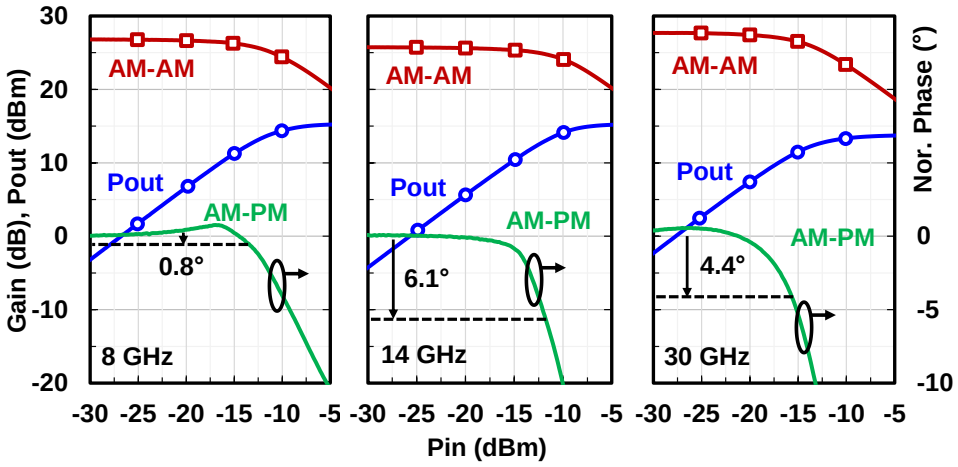


Figure 4.18: 8, 14 and 30 GHz AM-AM and AM-PM distortion performance.

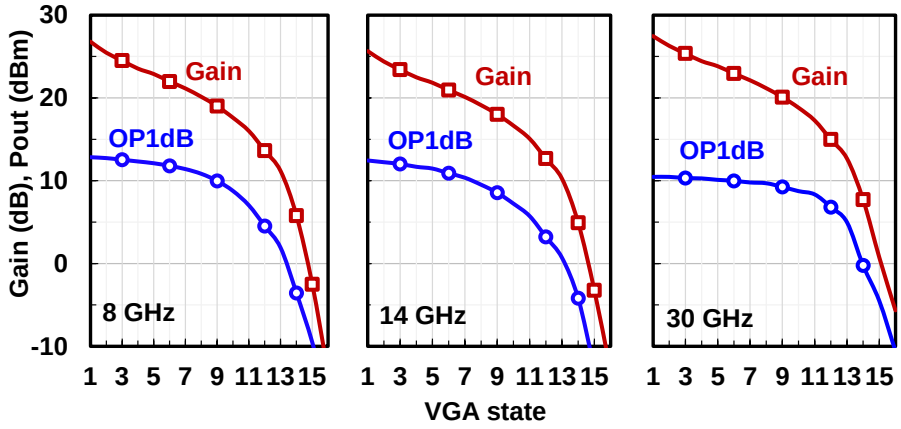


Figure 4.19: Measured gain and Pout vs. the VGA state at 8, 14, and 30 GHz.

frequencies. We have traced this to the interstage matching network between the driver and the power amplifier. The wideband matching networks do not have harmonic terminations and can affect operation at certain frequencies. Fig. 4.18 present the measured output power vs input power and related AM-PM performance of the entire channel. The results at 5-6 GHz are similar to 8 GHz and are not shown.

Fig. 4.19 show the OP1dB reduction due to the VGA gain setting changes. OP1dB slope is lower than the power gain slope, indicating that OP1dB is relatively insensitive the VGA gain changes. This is important especially for the array calibration where gain settings are changed.

4.4 16-Element Linear Phased Array

4.4.1 Wideband SATCOM Phased Array Demonstrator

The phased array employs Vivaldi antennas built on a multilayered printed circuit board for wideband operation [30]. EIRP (dBm) of a phased array can be calculated as

$$EIRP = 10\log_{10}(N) + G_{ANT} + P_{OUT}, \tag{4.1}$$

where N is the number of antenna elements, P_{OUT} is the output power delivered by the channel of the beamformer IC (dBm) and G_{ANT} is the gain of the antenna (dBi), which is estimated as

$$G_{ANT} = 10\log_{10}\left(\frac{4\pi N d^2}{\lambda^2}\right) + L_{ANT}, \tag{4.2}$$

where d is the antenna pitch, λ is the wavelength and L_{ANT} is the ohmic loss of the antenna and the PCB traces between the beamformer output port and the antenna (dB).

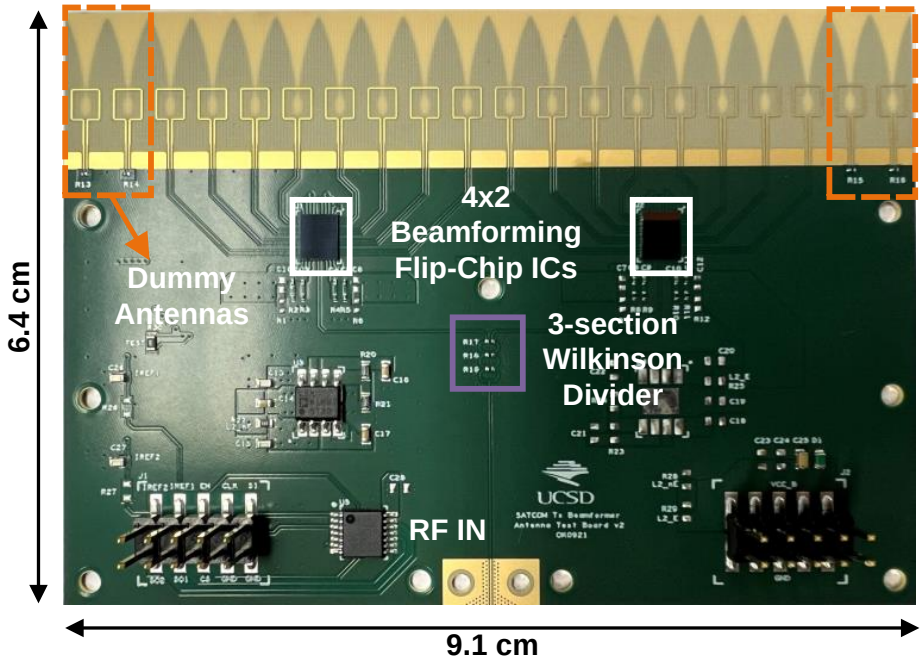


Figure 4.20: 16-element linear phased array.

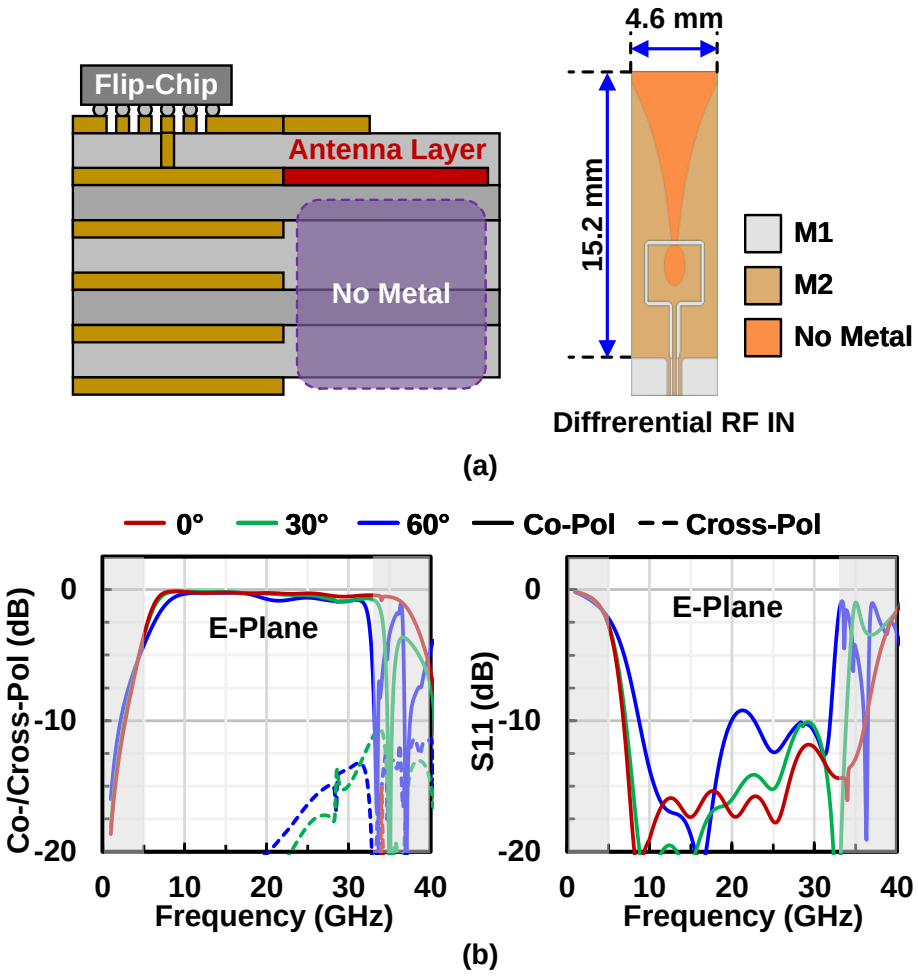


Figure 4.21: (a) Vivaldi antenna layout, (b) antenna simulated E-plane performance.

SATCOM systems normally employ dual polarized antennas to deliver radiation in rotated linear or circular polarization. To demonstrate the performance of the beamforming IC, however, a linearly polarized Vivaldi antenna is used for simplicity.

4.4.2 PCB, Antenna and Wilkinson Network Design

Two 5-33 GHz beamforming ICs are used to build the 16-element phased array. The chips are flipped on a 6-layer PCB (Tachyon 100G, ε_r = 3.1, t=28 mils) as close as possible to the Vivaldi antennas to minimize the transmission-line loss (0.3-1.5 dB at 5-33 GHz) (Fig. 4.20). Since the beamforming ICs are designed for a 2×2 quad antenna layout, the transmission lines have different lengths in a linear array configuration.

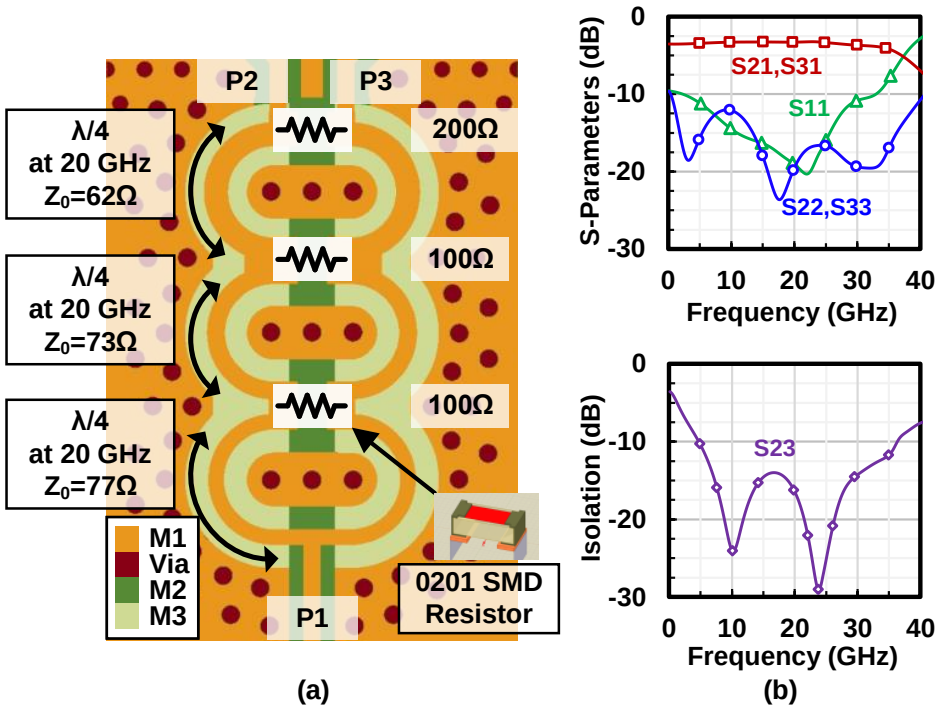


Figure 4.22: (a) 3-section Wilkinson network and (b) simulated performance.

The Vivaldi antenna spacing is 4.6 mm (0.46 λ at 30 GHz) to accommodate 60° scanning up to 30 GHz. The antenna is located on M2, but the differential ring feed is on M1 as shown in Fig. 4.21a. The antenna is simulated using Ansys HFSS, and the simulated E-plane co-pol, cross-pol and S_{11} for the Vivaldi antenna are plotted in Fig. 4.21b. The cross-pol performance is better than -13 dB up to 30 GHz when scanning to 60° in E-plane. In this frequency range, the return loss (S_{11}) is better than $\sim$10 dB. The gain of the antenna array is 6.7-19.4 dBi and the unit antenna gain is -5.3 to 7.4 dBi at 5-33 GHz including the differential feed ohmic loss.

Note that the unit cell is only 0.076-0.1λ at 5-8 GHz resulting in low element gain. Also, the 16-element array is 1.22-2λ at 5-8 GHz. This is the nature of wideband arrays designed to be on a $\sim$0.5λ grid at the maximum frequency. Still, the antenna element can be co-designed together with its neighboring elements and related mutual coupling to result in $S_{11}<10$ dB at 5-33 GHz and over all scan frequencies.

The RF power to the beamforming ICs is distributed using a three section Wilkinson network built using M1-M3 to allow for high impedance lines (Fig. 4.22a). Commercially

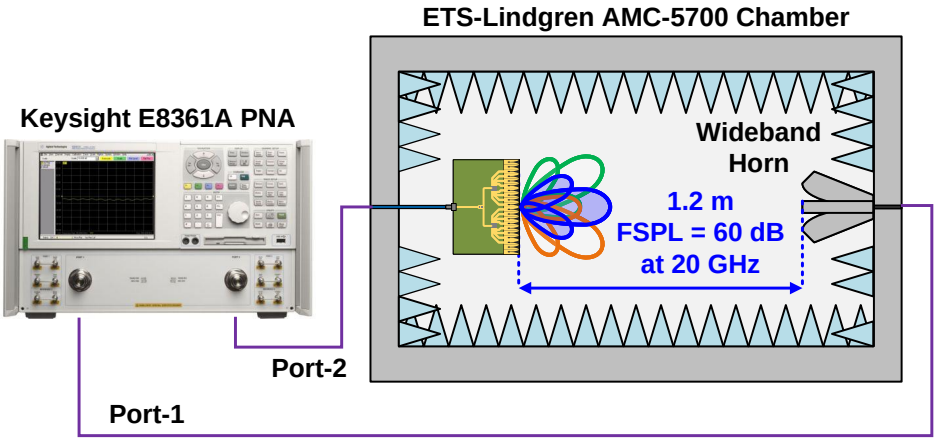


Figure 4.23: Measurement setup for array patterns.

available 100/200 Ω resistors are used between the TL arms. The simulated performance of the Wilkinson network is shown in Fig. 4.22b. The return loss is <-10 dB up to 33 GHz and the isolation (S_{23}) is >15 dB up to 33 GHz.

4.4.3 Pattern Measurements

Pattern measurements are performed using a Keysight E8361A PNA and the ETS-Lindgren AMC-5700 anechoic chamber with a wideband 5-50 GHz (Fig. 4.23). The phased array is placed 1.2 m (FSPL = 60 dB at 20 GHz) distance from the horn and is in the far field at all frequencies. Array calibration data is first done at 8, 14, 24 and 30 GHz, by turning on the channels one at a time and measuring S_{21} for every channel at all frequencies. The phase shifter and VGA are then used to equalize the channels before pattern measurements and the residual amplitude and phase error are shown in Fig. 4.24a. It is hard to do calibration with wideband arrays since when a single element is turned on and all others are off, the electromagnetic environment (and hence S_{11} and S_{21}) of a single element is very different than when the array is all ON. This is due to the strong mutual coupling between the elements leading to a different active impedance and radiation pattern for the all-ON case than for the single-ON case. Still, the RMS errors after single-element calibration are <0.6 dB and <10° at 5-33 GHz, which is acceptable for demonstration purposes. In the future, a better way is to turn-on all elements

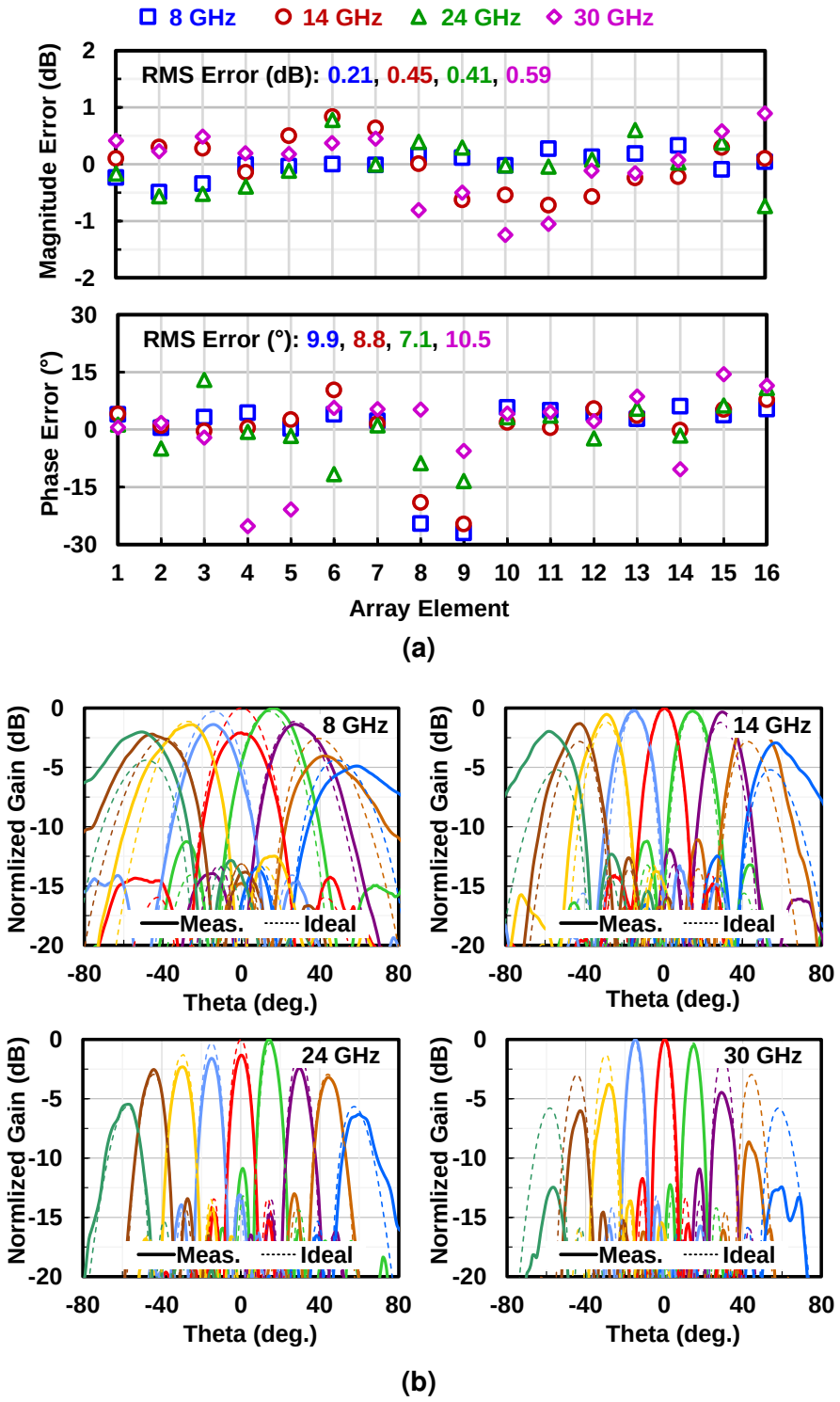


Figure 4.24: (a) Residual amplitude and phase error, (b) pattern measurements for the wideband phased array.

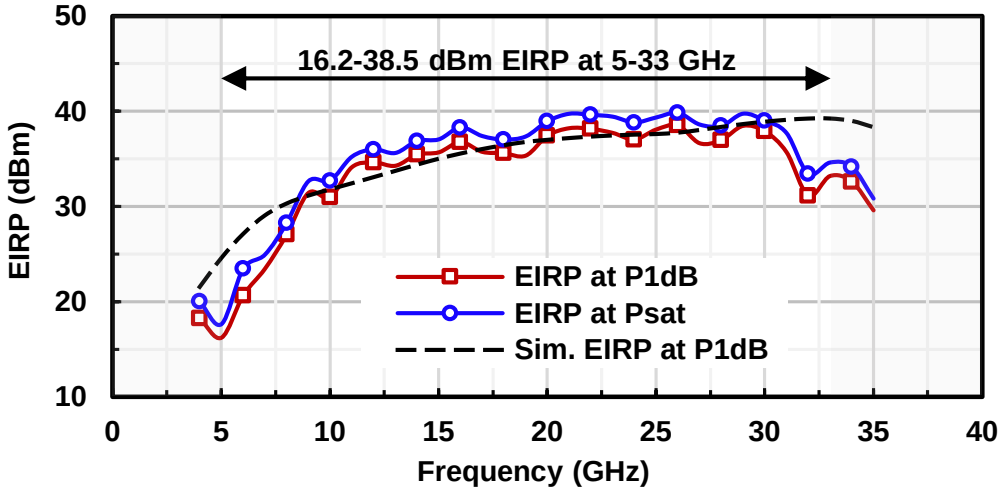


Figure 4.25: EIRP versus frequency at broadside.

together each with a different orthogonal code, and use orthogonal CDMA techniques to extract the response of each element [31].

The pattern measurements are presented in Fig. 4.24b. The array can scan up to 60° at 8, 14 and 24 GHz, and the sidelobes are ∼10 dB lower than the main lobe. At 30 GHz, the array can scan to ±30° and then falls off sharply afterwards. This is due to the substrate thickness and to perhaps a higher ε_r. While simulations in Fig. 4.21 show that the antenna operates well at 30 GHz with 60° scanning, it is just at the edge and any increase in ε_r or substrate height can seriously affect the antenna performance.

4.4.4 EIRP Measurements

EIRP measurements are performed using the same anechoic chamber and the same calibration data. At each frequency (4-35 GHz with 1 GHz steps), the calibration data is loaded to the beamforming ICs and the array measured at broadside (Fig. 4.25). The simulated EIRP result in the figure is calculated using (4.1) with the data of the OP1dB simulation of the beamforming IC, gain simulation of the 16-element Vivaldi array, estimated PCB TL loss and OP1dB reduction due to the gain setting changes (Fig. 4.16). The measured EIRP is 16.2-38.5 dBm at 5-33 GHz and has a good agreement with simulations. Fig. 4.26 presents the measured

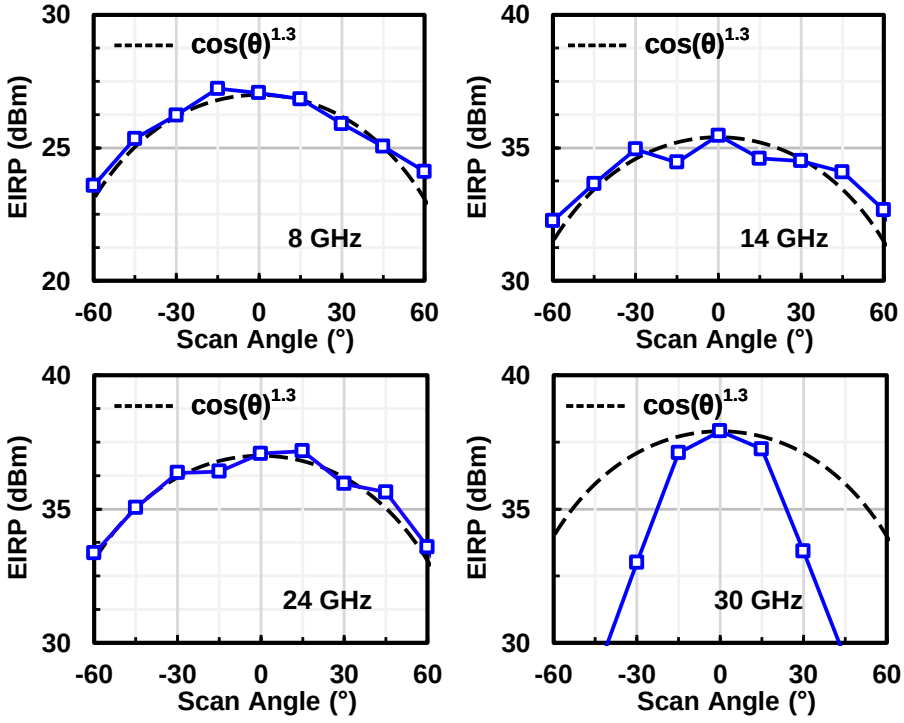


Figure 4.26: EIRP versus scan angle at 8, 14, 24 and 30 GHz.

EIRP versus scan angle. EIRP follows a $\cos\theta^{1.3}$ curve, which is expected from the Vivaldi antenna. EIRP degradation when scanning at 30 GHz is again due to the scan blindness of the Vivaldi array.

4.4.5 EVM Measurements

The same 1.2m link setup is used to measure the EVM performance of the phased array for SATCOM constellations. Complex modulated signals are generated using an RF signal generator (Keysight M9384B VXG) and the output is measured using the Keysight N9040B UXA spectrum analyzer. SATCOM waveforms of QPSK, 8-PSK and 16-QAM are given at 8, 14, 24 and 30 GHz (200 and 400 MHz symbol rates). Fig. 4.27 presents the measured constellations, spectrum and EVM results of the QPSK and 8-PSK (PAPR=4 dB, α=0.35) waveforms at 200 MHz symbol rate. Fig. 4.28(a)-(b) present the EVM of QPSK and 8-PSK waveforms at different scan angles (P1dB). Fig. 4.22(c)-(d) demonstrate the EVM of QPSK and 8-PSK waveforms at different EIRP levels at broadside. 16-QAM (PAPR=6.6 dB, α=0.35) waveform performance is

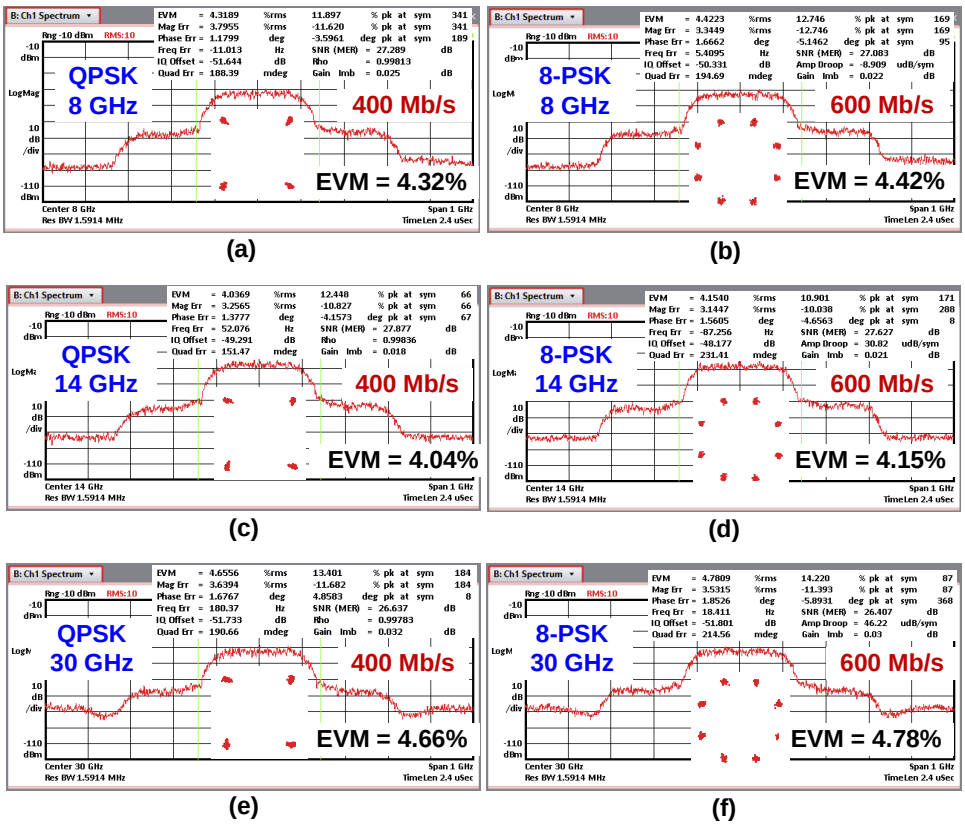


Figure 4.27: Measured constellation and spectrum for QPSK and 8-PSK waveforms at (a)(b) 8, (c)(d) 14 and (e)(f) 30 GHz at 1-dB compression point.

also evaluated at 400 MHz symbol rate. The measured constellations at 400 MHz symbol rate at broadside are summarized in Fig. 4.29.

As can be seen from Figs. 4.27-4.29, the measured results show excellent performance for SATCOM waveforms with low EVM (<4-4.8%) up to P1dB operation, proving the phased array performance at X, Ku bands for ±60° scan angle and Ka-band for ±30° scan. The C-band results are very similar to X-band and are not shown.

Table 4.1 presents a comparison with state-of-the-art beamformers and phased arrays. This work achieves widest bandwidth covering C, X, Ku and Ka SATCOM bands.

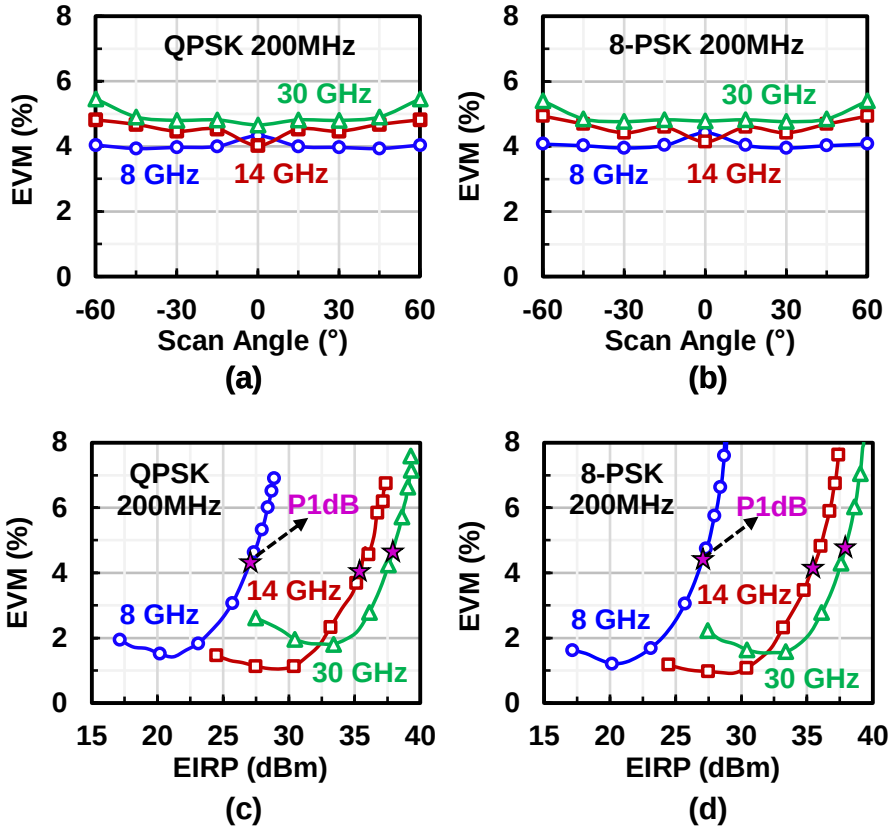


Figure 4.28: EVM versus scan angle for (a) QPSK and (b) 8-PSK waveforms at 1-dB compression point, and EVM versus EIRP for (c) QPSK and (d) 8-PSK waveforms (Symbol rate = 200 MHz).

4.5 Conclusion

This article presented a wideband SiGe transmit beamformer chip covering C, X, Ku and Ka band SATCOM. The chip consists of 8 channels, which is suitable for 2×2 quad antenna approach for SATCOM applications. A 16-element linear phased array is built using the two beamformer chips on a low-cost PCB to demonstrate the chip performance. The phased array shows ultra-wideband operation with QPSK, 8-PSK and 16-QAM waveforms for SATCOM applications.

Future work will be to expand the phased array designs to wideband dual polarized arrays.

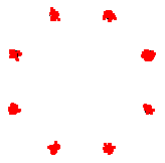
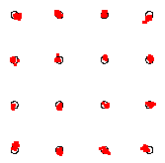
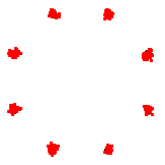
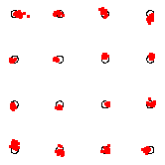
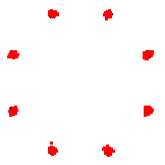
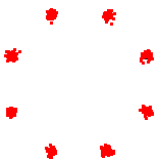
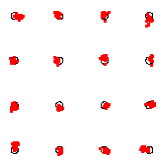
Modulation	QPSK	8-PSK	16-QAM
BW (MHz)	400	400	400
8 GHz			
EVM (%)	4.37	4.39	4.70
EIRP (dBm)	27.1	27.1	24.03
14 GHz			
EVM (%)	4.09	4.23	5.61
EIRP (dBm)	35.5	35.5	33.2
24 GHz			
EVM (%)	3.25	3.33	4.55
EIRP (dBm)	37.1	37.1	34.7
30 GHz			
EVM (%)	4.64	4.74	5.08
EIRP (dBm)	38	38	35.3

Figure 4.29: Summary of the performance for QPSK, 8-PSK and 16-QAM constellation measured over-the-air (OTA) (Symbol rate = 400 MHz).

4.6 Acknowledgment

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Chapter 4 is, in full, to be submitted for publication of the material as it may appear in: O. Kazan, Z. Hu, L. Li, A. Alhamed and G. M. Rebeiz, "An 8-channel 5-33 GHz Transmit Phased Array Beamforming IC With 10.8-14.7 dBm Psat for C, X, Ku and Ka-band SATCOM," *IEEE Transactions on Microwave Theory and Techniques*. The dissertation author was the primary investigator and primary author of this paper.

Chapter 4, in part, has been submitted for publication of the material as it may appear in: O. Kazan, Z. Hu, A. Alhamed and G. M. Rebeiz, "A 5-33 GHz 8-Channel Transmit Beamformer with Peak Power of 14 dBm for X/Ku/Ka-band SATCOM Applications" in *2022 IEEE International Symposium on Phased Array Systems and Technology*, 2022. The dissertation author was the primary investigator and primary author of this paper.

Table 4.1: Performance Comparison of Wideband Beamformers and Phased Arrays

Beamformer Measurements				
	This Work	**JSSC'21 [32]**	**TMTT'22 [33]**	**JSSC'2007 [34]**
Technology	90nm SiGe BiCMOS	90nm SiGe BiCMOS	90nm SiGe BiCMOS	SiGe BiCMOS
Frequency (GHz)	5-33	15.25-50.5	16-50.5	6-18
Fractional Bandwidth (f_{min}/f_{max})	1:6.6	1:3.3	1:3.2	1:3
Architecture	4×2 Tx	4×1 Tx	4×1 Tx	4×2 Rx
Gain Control (dB)	21	16.2	16.2	-
Phase Resolution (bit)	5	5	5	4 (accuracy>5-bit)
OP1dB (dBm)	9-13.3	13.5-14.7 (20-50 GHz)	13.5-14.7 (20-50 GHz)	-
OPsat (dBm)	10.8-14.7	14.4-15.3	14.4-15.3	-
P_{DC}/Channel (mW)	240 at P1dB	250 at P1dB	250 at P1dB	70
Phased Array Measurements				
	This Work	**JSSC'21 [32]**	**TMTT'22 [33]**	**TMTT'21 [35]**
Frequency (GHz)	5-33	15.25-50.5	16-50.5	23.5-29.5
Array Size	16×1 Tx	8×1 Tx	16×4 Tx	8×8 Tx
Polarization	Single	Single	Single	Single
Peak EIRP (dBm)	38.5	34	51.7	54.8
OTA Distance (m)	1.2	1.2	1.2	1.3
Azimuth Scan	±60° (C, X, Ku) ±30° (Ka)	±60°	±60°	±60°
Constellation	8-PSK	64-QAM	64-QAM	64-QAM
Data Rate	1.2 Gb/s	2.4 Gb/s	2.4 Gb/s	1.2 Gb/s
EVM (%)	4.7 38 dBm EIRP at P1dB (30 GHz)	2.5 25 dBm EIRP at 6dB backoff (29 GHz)	2.9 39 dBm EIRP at 8.5dB backoff (25GHz)	5 46 dBm EIRP at 8dB backoff (29 GHz)

Chapter 5

Conclusion and Future Work

5.1 Conclusion

This thesis presented wide band integrated circuits. The circuits design details were given, and the measured performances were demonstrated.

In chapter 2, an ultra-wideband low noise amplifier operating at 10-110 GHz was presented. The LNA is composed of four differential cascode stages. To achieve wide bandwidth, an innovative inductive load is used at the collectors of the HBT devices, and resistive shunt feed is implemented. The stability over the wide bandwidth is improved by using small HBT devices as a current mirror and by tying the bases of the cascode devices by high value resistor. The small-signal and large-signal performances are evaluated with measurements. The LNA achieved a measured small-signal gain of 19-25.5 dB and the measured noise figure (NF) is 4.8-5.3 dB at 10-50 GHz. It is also demonstrated that the LNA can deliver OP1dB of 3.3 dBm at 66 GHz. Moreover, the power consumption of the proposed circuit is 96 mW with a circuit area of 1.3x0.6 mm^2 (Fig. 5.1). The circuit is proved to have the highest figure of merit in the literature.

In chapter 3, an ultra-wideband distributed power amplifier operating at 10-130 GHz was presented (Fig. 5.2). The DPA is composed of three stages, and each stage has multiple sections. To improve the bandwidth, series RC feedback is used, and a small series base capacitor are used. The DPA achieves 18-23 at dB at 10-30 GHz and increasing to the peak of 33 dB at 98 GHz. The circuit can deliver a peak OP1dB of 13.1 dBm at 22 GHz. With these, the largest

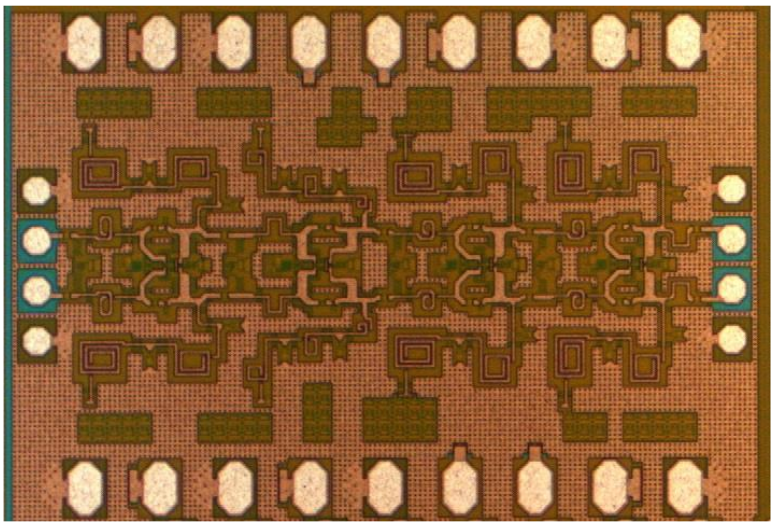

Figure 5.1: Die photo of the wideband differential LNA. The size is 1.5×1.0 mm^2 including the pads, and 1.3×0.6 mm^2 excluding the pads.

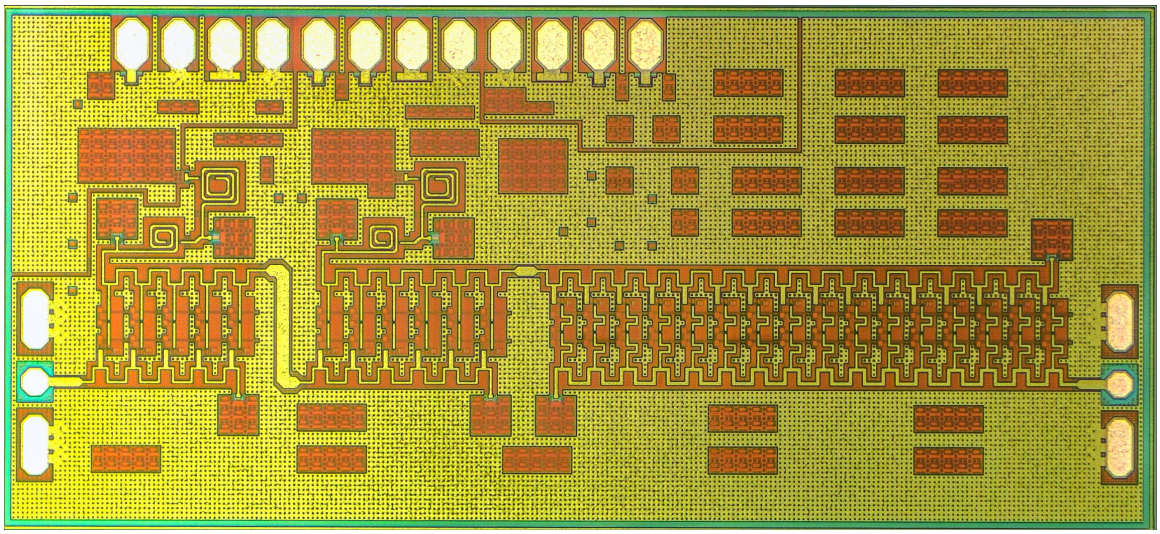

Figure 5.2: Die photo of the wideband DPA. The size is 2.4×1.0 mm^2 including the pads. The active circuit size is 2.11×0.59 mm^2.

gain-bandwidth product is achieved while providing relatively high output power.

In chapter 4, a 6-32 GHz transmit phased array and a beamforming IC were presented. The applications areas are in X, Ku and Ka-band SATCOM. The phased array has 16 Vivaldi antennas and two beamforming ICs. The ICs have 8 channels and each of them has an active balun, a variable gain amplifier, a phase shifter and a power amplifier. Two-stage lumped Wilkinson network is used to distribute the input RF power to the channels. The chip performance

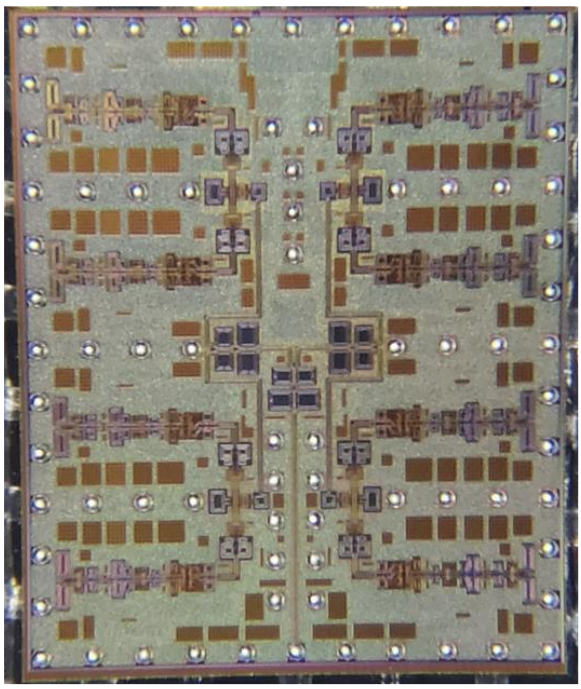

Figure 5.3: Die photo of the wideband beamformer. The chip size is 3.9×4.7 mm^2.

(Fig. 5.3) and the phased array (Fig. 5.4) performance are evaluated. The chip has a small-signal gain of 24-27 dB at 5-33 GHz. It can perform 5-bit phase shifter operation and has more than 20 dB gain control. The chip can also deliver a peak OP1dB and OPsat of 13-14 dBm at Ku-band. The phased array can scan to ±60-degree at X and Ku bands and to ±45-degree at Ka band. QPSK, 8-PSK and 16-QAM waveform are given to the array for its performance evaluation. Less than 5.6% EVM is achieved having a peak EIRP of 37.9 dBm at Ka-band. With these, the phased-array and the beamforming IC achieve the widest Tx bandwidth in literature.

5.2 Future Work

5.2.1 Low Noise Amplifier

The low noise amplifier is proved to have great performance. Although the power consumption is low and circuit size is small compared to the distributed amplifier topologies. The LNA is still too large for beamforming ICs. In addition to the size, the noise figure can be improved. The key to achieving these might be using:

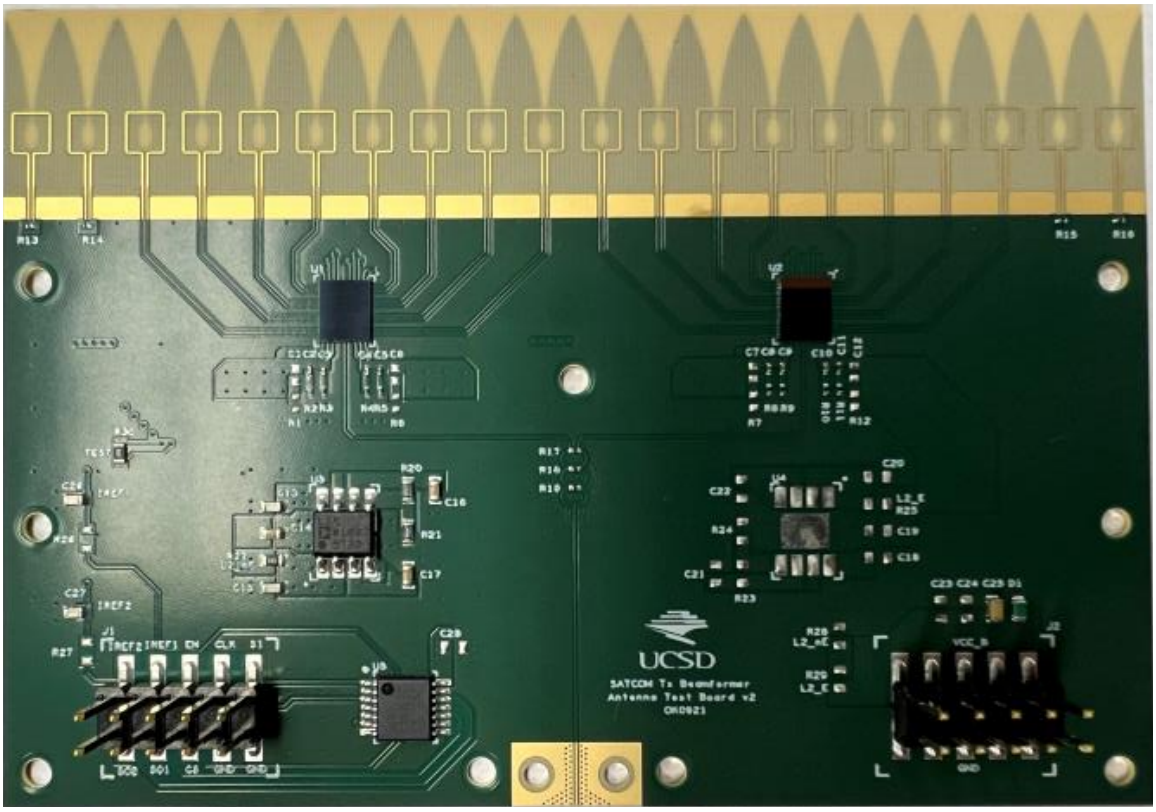

Figure 5.4: Photo of the 16-element wideband phased array employing the wideband beamformers. The PCB size is 9.1×6.4 mm^2.

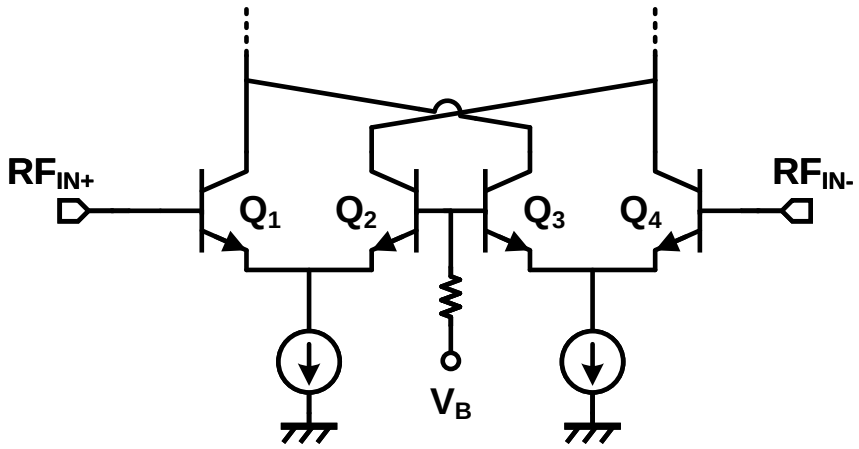

Figure 5.5: f_T doubler topology.

1. Larger emitter length HBT devices

   The larger devices reduce the base noise resistance, and hence increase the size of the noise figure circles [36]. Therefore, the wideband noise figure performance can be improved.

2. f_T doubler topology

   The schematic of the topology is shown in Fig. 5.5. With a topology like this, gain per stage can be increased. Therefore, a smaller number of stages will be needed (smaller circuit size). The noise figures of this system as compared to the traditional common-emitter topology for wideband circuits should be investigated.

5.2.2 Wideband Beamformer

As indicated in chapter, future work will be to design a dual-beam receiver beamformer, and to expand the phased array designs to wideband dual polarized arrays. There are further ways to expand the work:

1. Increasing the bandwidth

   The LNA and DPA designs presented in this thesis can be implemented in wider band beamformer designs. The only bottleneck is the phase shifter in the bandwidth expansion. To improve the bandwidth of that block, quadrature phase generator topologies with wider

band should be investigated. One possible way could be to cascade multiple QAF network sections to add more poles.

2. Designing a Tx/Rx wideband beamformer

   The beamformer presented in this thesis can only be used as transmitter. Combining transmit and receive functions into a single system would further simplify the SATCOM ground terminal system. The channel sizes should be shrunk so that these functions can be integrated into $\sim 5 \times 5$ mm^2 size, which can be used for $\lambda/2$ pitch 2×2 quad antennas.

Appendix A

Active Balun Improvement for the SATCOM Tx Beamformer

In sections 4.2.2 and 4.2.3, the active balun and variable gain amplifier design details are given. However, some of the details are restated here. To improve bandwidth, the active balun employs a shunt feedback, but this introduces phase imbalance between the differential output ports of the active balun. This is mitigated by using a mismatch compensation network at the input of the VGA. The schematics for the active balun and the variable gain amplifier are redrawn in Fig. A.1 for convenience.

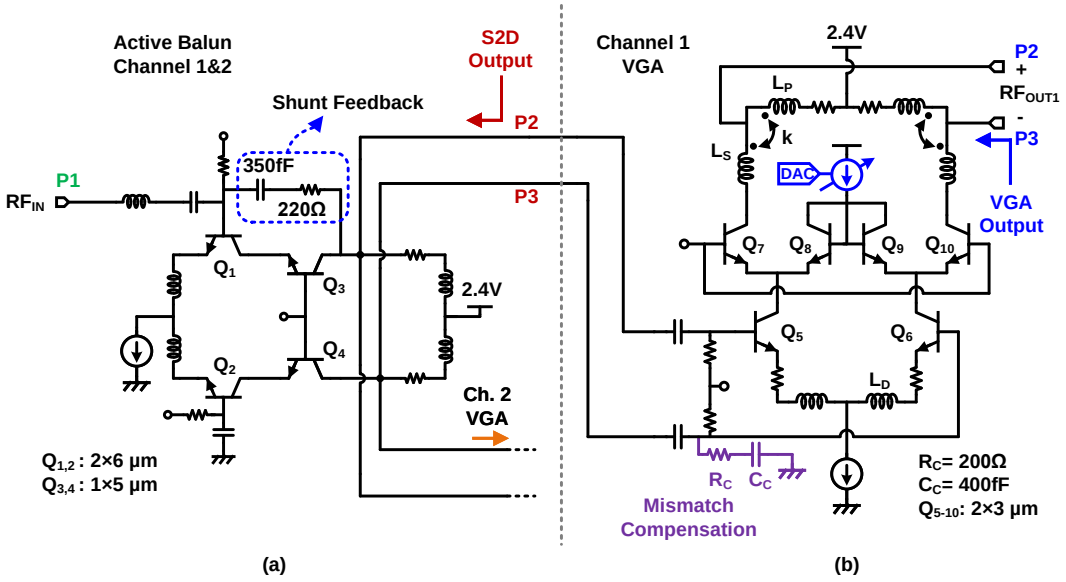

Figure A.1: Schematic of (a) active balun and (b) variable gain amplifier implemented in SATCOM Tx beamformer (Chapter 4).

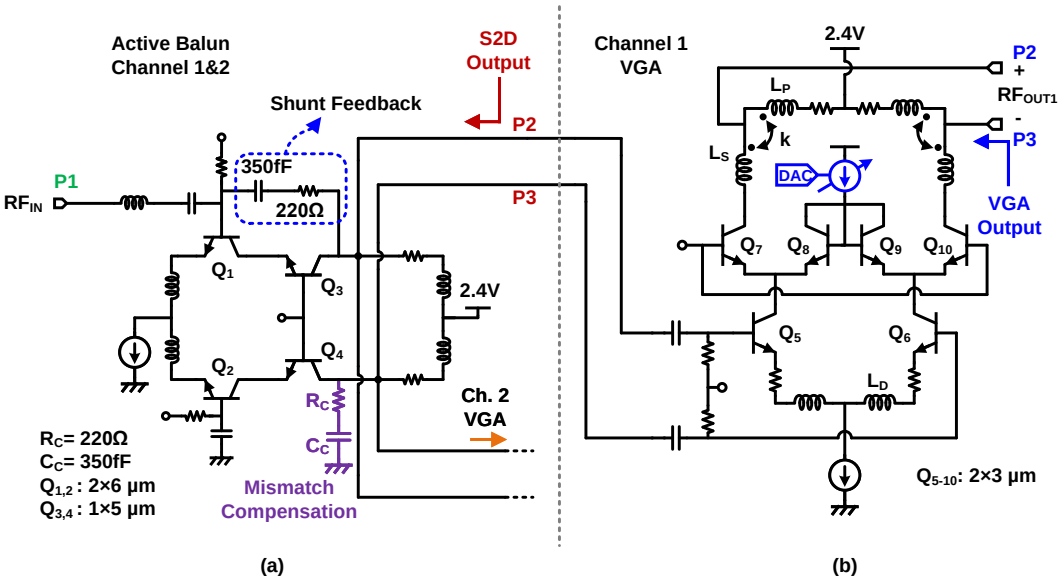

Figure A.2: Schematic of (a) active balun and (b) variable gain amplifier for improvement of S2D output imbalance.

The feedback network employed in the active balun results in a shunt load at one of the output ports due to the Miller effect. A better approach to compensate this loading would be to introduce a shunt load at the other output port of the active balun as shown in Fig. A.2.

The performance of the improved circuit is simulated and compared with the performance of the circuit implemented in the beamformer. Fig. A.3 presents the output imbalance comparison of the active balun and the variable gain amplifier between the new approach and the circuit implemented in the thesis. The differential phase improvement is insignificant with the modified version of the circuit (Fig. A.3a-A.3c). However, the magnitude imbalance is $\sim$1 dB better (Fig. A.3b-A.3d). Fig. A.4 presents OP1dB and OPsat of the new circuit and the implemented circuit. The new approach has higher linearty below 15 GHz. For the future generations of the SATCOM Tx bemformer, this modified circuit can be implemented to improve the differential channel RF signal.

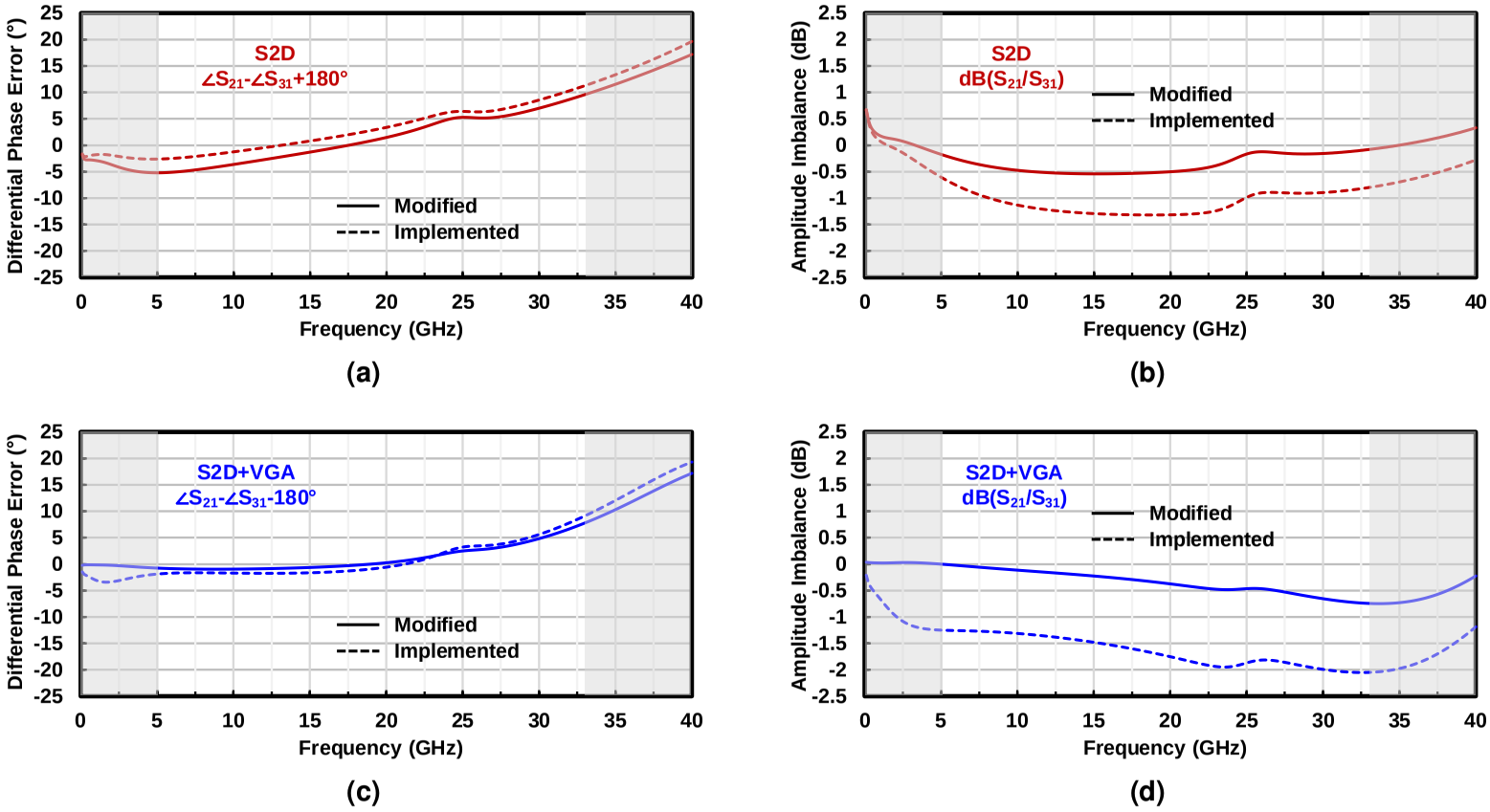

Figure A.3: Simulation results of: (a) amplitude imbalance for S2D, (b) differential phase error for S2D, (c) amplitude imbalance for S2D+VGA, (d) differential phase error for S2D+VGA

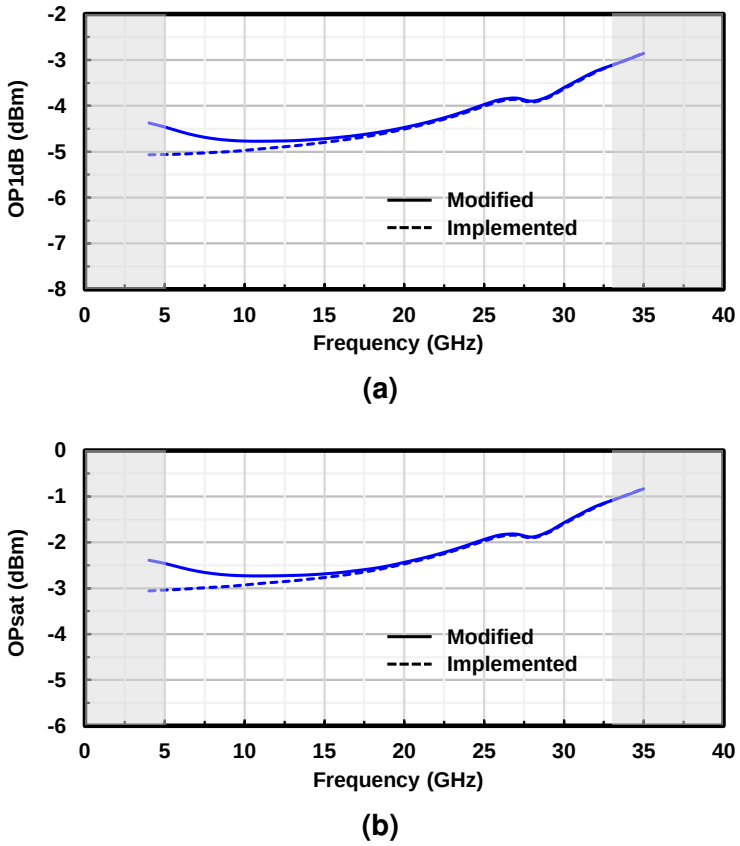

Figure A.4: Simulation results of: (a) OP1dB for S2D+VGA, (b) OPsat for S2D+VGA.

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