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Gating a Quantum Dot through the Sequential Removal of Single Electrons from a Nanoscale Floating Gate

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We use the tip of an atomic force microscope (AFM) to charge floating metallic gates defined on the surface of a Si/SiGe heterostructure. The AFM tip serves as an ideal and movable cryogenic switch, allowing us to bias a floating gate to a specific voltage and then lock the charge on the gate by withdrawing the tip. Biasing with an AFM tip allows us to reduce the size of a quantum dot floating-gate electrode down to approximately 100 nm. Measurements of the conductance through a quantum dot formed beneath the floating gate indicate that its charge changes in discrete steps. From the statistics of the single-electron leakage events, we determine the floating-gate leakage resistance $R \sim 10^{19}$ Ohm—a value that is immeasurable by conventional means.

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I. INTRODUCTION

Spin qubits in gate-defined quantum dots (QDs) have recently demonstrated two-qubit gates with fidelities exceeding fault-tolerant thresholds [1–3]. Spin qubits have also been integrated with microwave cavities, enabling dispersive spin-state readout, coherent spin-photon coupling, and microwave-mediated spin-spin interactions [4–8]. Long coherence times [9], compatibility with industrial fabrication techniques [10,11], and the potential for integration with classical silicon electronics [12] make them one of the most promising platforms for quantum computing [13,14].

As quantum processors increase in complexity, many solid-state qubit platforms will soon face the challenge of delivering a growing number of room-temperature control signals to the cryogenic environment of the chip. Since most quantum error-correction protocols require qubits to be arranged in two-dimensional (2D) arrays [15], qubit interconnect crowding is an outstanding issue [16]. For semiconductor spin qubits, where qubits are only separated by approximately 100 nm, the interconnect challenge is further exacerbated [17,18].

A primary approach that is being pursued to reduce the number of room-temperature control lines is charge locking [19–21]. Charge locking is conceptually related to classical dynamic random-access memory [22]. In the case of gate-defined QDs, the concept is to electrically detach the QD gate electrode from the control line. If the electrical isolation of the gate is high, it will retain its charge for a sufficiently long time, allowing other gates on the device to be manipulated with the same room-temperature control line. In the perfect case, the so-called "sample-and-hold" circuit [23], a zero-resistance switch is desired to dynamically charge and lock the floating node, as shown in Fig. 1(a). In practice, it is quite challenging to realize a mechanical switch for mesoscopic devices. To date, only field-effect transistors (FETs), integrated both on chip and off chip, have been used to isolate gates from room-temperature signals in GaAs [21,24], Si/SiGe [25,26], and CMOS [27,28] QDs.

Interconnect crowding in 2D qubit arrays can be significantly eased by vertically bringing electrical connections out of the device plane. Air bridges [29] and through-silicon vias with indium bumps have been successfully implemented for superconducting qubits [30,31]. Flip-chip bonding is being pursued for cavity-coupled Si spin qubits [32]. A CMOS-compatible device architecture incorporating nanoscale vias has recently been introduced [33] but its application has so far been limited to small linear arrays of Si/SiGe QDs [34].

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Inspired by the potential of via-based three-dimensional (3D) integration [33,34], we explore the nanoscale limit of the floating-gate approach by fabricating isolated gates with an approximate diameter of 100 nm. We attempt to realize the ideal sample-and-hold circuit by using the tip of an atomic force microscope (AFM) as a movable voltage node [35,36]. The floating gate can then be electrically charged by contacting it with a voltage-biased AFM tip. Withdrawing the AFM tip locks the charge on the floating gate. We probe the charge retention of the floating gate by measuring the conductance through a QD defined in a Si quantum well beneath the floating gate. The true floating-gate design and its small diameter of approximately 100 nm eliminates problems typical of FET-based charge locking, such as charge leaking through the FET channel due to a finite on-off ratio [27].

We first demonstrate that the AFM tip can be used as a stationary vertical gate while in continuous electrical contact with the metallic floating gate. By sweeping the dc tip voltage, V_T, we can tune the QD charge occupancy as in a conventional QD device. Then, by withdrawing the biased tip, we show that the electric charge is locked on the floating gate over a time scale set by the leakage resistance R to other gates on the device. We confirm the nondestructive character of the injection and/or locking process by repeating it multiple times on a single gate and obtaining a reproducible charge-sensor response down to individual electron-tunneling events.

The nanoscale dimensions of our floating gate allow us to explore an intriguing "second quantized" operating regime, since the voltage resolution of the gate is fundamentally limited by the quantization of electric charge [37]. We demonstrate how this fact leads to a biasing imprecision (approximately 1 mV) of the plunger gate of the QD. Due to the subfemtofarad total capacitance C_g of the gate, only a few hundred electrons have to be removed from the gate to induce a few-electron QD beneath it. In addition, we directly probe the retention time of the charge locked on the floating gate. We utilize the QD induced in the quantum well under the floating gate as a highly sensitive charge sensor [38,39] to extract values of C_g and R. In devices with a single layer of gates, we show that charge can stay locked for several hours.

II. EXPERIMENTAL SETUP

Our accumulation-mode device is fabricated on an undoped Si/SiGe heterostructure consisting of a 5-nm-thick Si quantum well (QW) that is buried under a 50-nm-thick layer of $Si_{0.7}Ge_{0.3}$ and a 2-nm-thick Si cap. To form a QD in the plane of the QW, we utilize a gate stack consisting of three overlapping layers, as shown in Figs. 1(c) and 1(d). Two Al layers form barrier (B1 and B2) and accumulation (S and D) gates, while the Pd disk on top serves as a floating plunger gate. Pd is used for the final layer, as it enables good electrical contact to the AFM tip [40]. In this work, we focus on a small section of the device, indicated

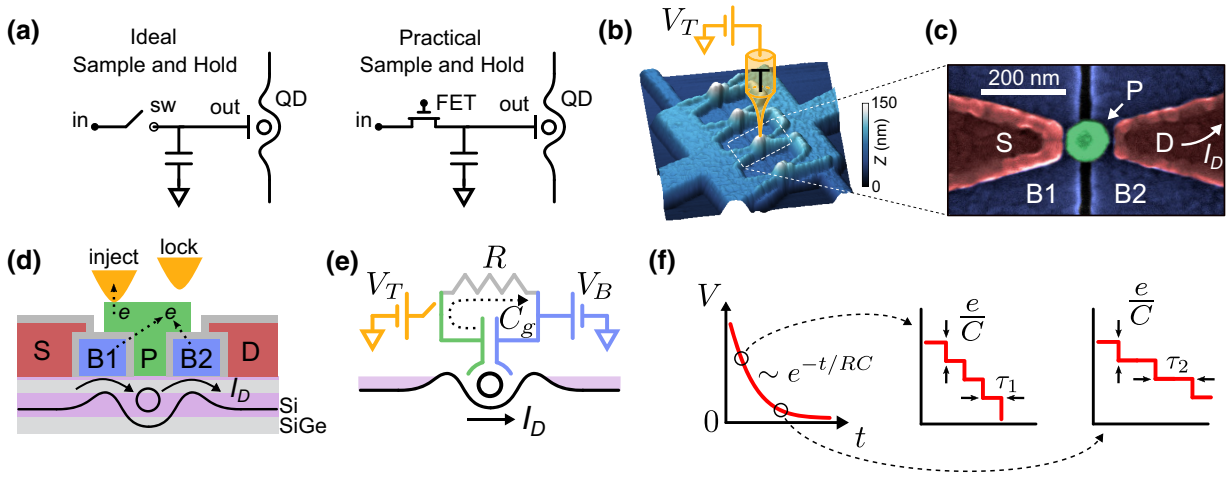

FIG. 1. (a) Ideal and practical sample-and-hold circuits for locking charge on a QD gate electrode. (b) A low-temperature topographic AFM image of the device, which consists of four identical sections, each containing a floating metallic gate. The dc-biased tip (T) is used to charge a metallic floating gate. (c) A false-color scanning electron microscope image of a section of the device, with Al source-drain (S-D) accumulation gates, Al barrier gates (B1 and B2), and a floating Pd gate (P). I_D is the current through the charge detector QD formed beneath the P gate. (d) A cross section of the device. The tip is used as a switch (sw) to inject and lock the charge on the floating gate. (e) The equivalent circuit. The colors correspond to the sketch in (d): switch tip, yellow; resistance or gate-oxide layer, gray; barrier gates, blue; P floating gate, green; and QD induced in the Si quantum well, black. (f) The RC discharge curve in the quantum limit allows the independent extraction of the capacitance C and resistance R by utilizing the quantization of electric charge. R is related to the average waiting time $\langle\tau\rangle$ between two uncorrelated tunneling events as $I = e/\langle\tau\rangle = V/R$, while C is determined from the size of the discrete voltage steps e/C.

by the white dashed line in Fig. 1(b), while other sections of the device show similar behavior.

During charge injection [Fig. 1(d)], the tip stays in contact with the floating gate and $V_T = V_P$. Charge locking takes place when the biased tip is lifted away from the device (approximately 200 nm above the gate). After the AFM tip is withdrawn, the charge trapped on the floating gate can leak to the Si/SiGe substrate or the Al barrier gates (B1 and B2). We measure the current I_D through the QD induced beneath the P gate to sense the real-time dynamics of the locked charge. The equivalent circuit is shown in Fig. 1(e), where the switch denotes the tip, while the tunnel junction (TJ) between the floating gate and barriers is depicted as an RC circuit capacitively coupled to the Si/SiGe QD.

In a classical discharging circuit, the RC time constant can be extracted from the exponential decay of voltage V across the capacitor as shown in the left panel of Fig. 1(f). However, the individual values of R and C remain unknown. Nevertheless, R and C can be extracted independently if the electrometer is sensitive and fast enough to resolve single-electron tunneling events, as sketched in Fig. 1(f) [41]. The capacitance is directly related to the size of the discrete voltage steps e/C. At the same time, the resistance can be extracted from the electric current $I = e/\langle\tau\rangle = V/R$, where $\langle\tau\rangle$ is the average waiting time before the next tunneling event. Note that in this model, $\langle\tau\rangle$ increases linearly as V decreases.

III. AFM-BASED CHARGE-LOCKING

We begin by measuring Coulomb peaks with the tip in contact with the floating gate, such that $V_T = V_P$. Figure 2(a) shows I_D through the QD induced in the QW as a

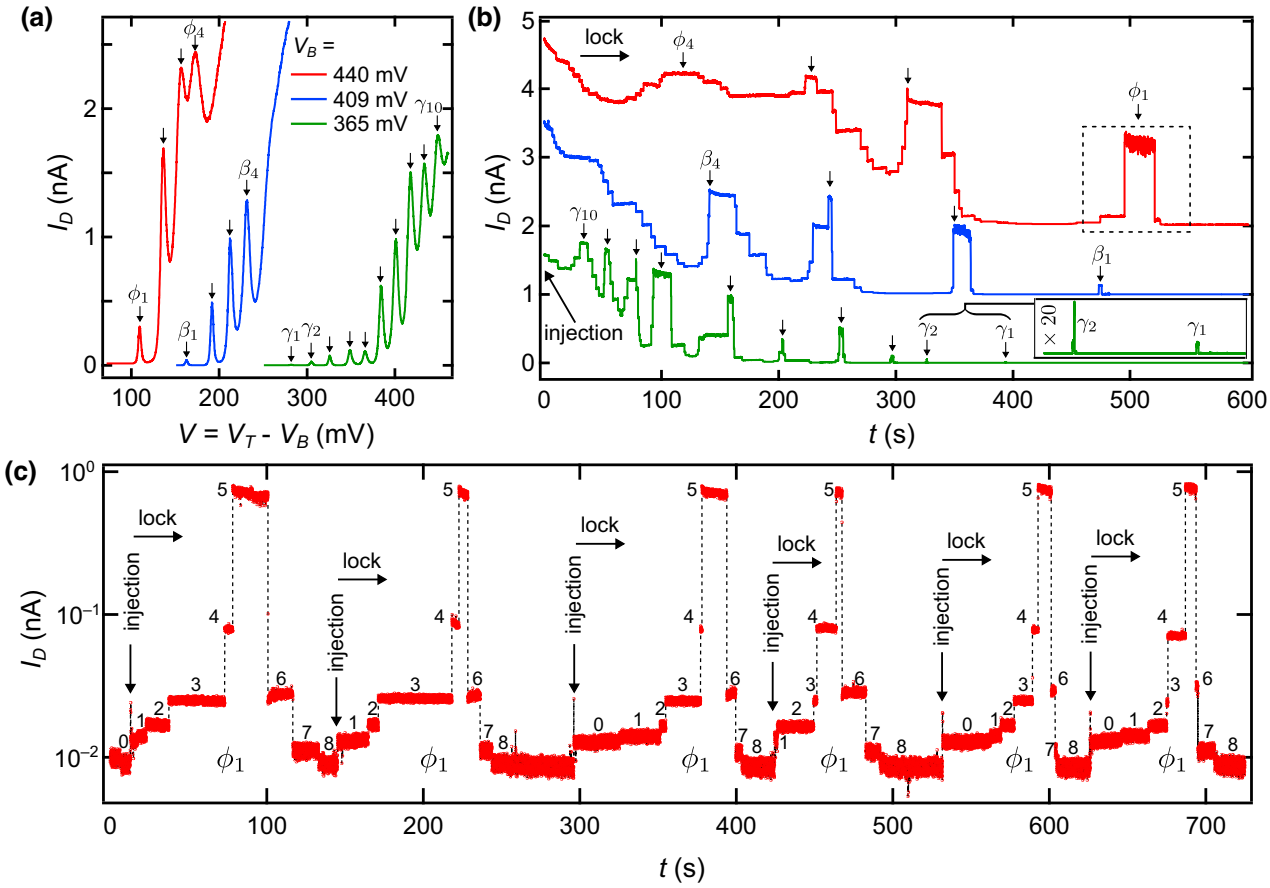

FIG. 2. (a) Continuous injection. Coulomb blockade peaks (CBPs) are measured as a function of the differential voltage $V = V_T - V_B$ while the AFM tip continuously touches the floating gate. The three traces are taken at different barrier voltages ($V_B = 365$, 409, and 440 mV) to cover a wider range of differential voltage. For each curve, the series of visible Coulomb blockade peaks (CBPs) is marked as ϕ_i, β_i, and γ_i. (b) Charge locking. The current measured as a function of time after the biased tip is moved away from the floating gate. Each step corresponds to a single electron tunneling from a barrier gate to the floating gate. The curves are color matched to corresponding current traces from (a) and vertically offset by 1 nA for clarity. (c) The reproducibility of the discrete current steps around Coulomb peak ϕ_1 over six repetitive injection cycles. The count of electrons tunneled after injection is indicated for each cycle by numbers from 0 to 8. In the second and fourth cycles, the first step is missing because the waiting time between injection and the first tunneling event is shorter than the integration time.

function of the voltage difference between the floating gate and barrier gates, $V = V_T - V_B$. For these experiments, the barrier gates are kept at the same potential $V_B = V_{B1} = V_{B2}$. Three traces are acquired with different V_B to cover a broader range of V and $\langle\tau\rangle$. We mark each visible Coulomb peak: ϕ_i, β_i, and γ_i for the red, blue, and green curves, respectively.

By suddenly lifting the tip from the floating gate and monitoring I_D, we study the retention of the locked charge for three values of V_B as shown in Fig. 2(b). These data sets are color matched to a corresponding curve in Fig. 2(a). Just before the tip is lifted around $t = 0$ s (injection), V for each curve is slightly exceeding the last prominent CBP in Fig. 2(a) (ϕ_4, β_4, and γ_{10}). As time passes, the floating gate discharges and I_D retraces the series of Coulomb peaks shown in Fig. 2(a). In contrast to continuous injection, where the AFM tip is in contact with the floating gate, discharge occurs in discrete steps. In Fig. 2(c), we show that single-electron tunneling is the dominant process here and that the jumps are solely related to the electrostatic environment around the QD and are not just random measurement artifacts due to $1/f$ noise. Here, we sequentially repeat injection and locking of charge around the CBP ϕ_1, as highlighted by the dashed square in Fig. 2(b). After each injection, the current I_D evolves through the same sequence of discrete steps marked from 0 to 8, the number of additional electrons that have tunneled to the floating gate. The reproducibility of the plateaus in I_D implies that the rates of all higher-order tunneling processes are much slower. Note that we work at differential voltages that are much larger than the superconducting gap $\Delta \approx 200$ μeV of Al. However, very rarely [e.g., for 2 out of 50 events in Fig. 2(c)], the waiting time between two tunneling events appears to be shorter than the integration time (approximately 10 ms), making these events indistinguishable from two-electron tunneling. As a result, the measured total capacitance C_g of the floating gate, which can be extracted directly from the time traces [42] as described below, acquires imprecision due to these counting errors.

IV. CAPACITANCE MEASUREMENT BY COUNTING ELECTRONS

In Fig. 3(a), we plot side by side the pair of CBPs β_3 and β_4 as a function of $V = V_T - V_B$ (top axis) and time (bottom axis). The amplitude of the Coulomb oscillations during the continuous tip-voltage sweep (solid line) is reduced compared to the case of free discharge (dashed line and dots). We attribute this difference to the increased electron temperature caused by the tip being in contact with the floating gate. The voltage difference between the peaks ΔV can be covered by N electrons tunneling to the floating gate such that $N - 1 < \Delta V C_g/e < N$. By definition, the total capacitance can be measured through single-electron counting. We repeat the injection-locking

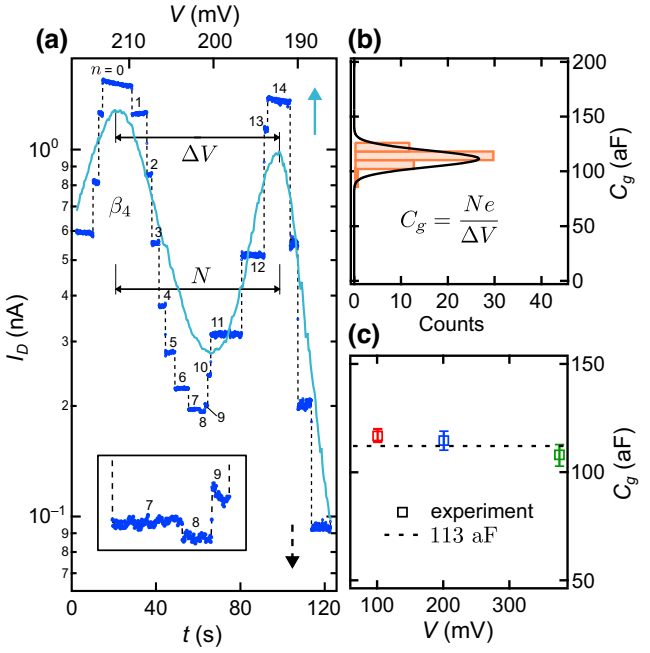

FIG. 3. (a) The current I_D between the β_3 and β_4 CBPs, plotted as a function of the differential voltage (solid, top axis) and the time after injection (dashed, bottom axis). The number of tunneling events starting from the local current maximum is numbered by n. The total number of electrons to cover the voltage difference ΔV between two CBPs is denoted as N. The inset shows an enlargement of the data in the dip between the Coulomb peaks. (b) The histogram shows the distribution of the floating-gate capacitance C_g due to random errors over all collected data sets. (c) The averaged C_g as a function of the differential voltage.

cycle multiple times for three different differential voltages between ϕ_1 and ϕ_2, γ_6 and γ_7, and β_3 and β_4 from Figs. 2(a) and 2(b) and plot the histogram of measured C_g values in Fig. 3(b). The narrow distribution implies that tunneling of single electrons is the dominant process and is slightly widened toward lower capacitance by two-electron processes and toward higher capacitance by large $1/f$ charge-noise events that are interpreted as electron-tunneling events. A recent study links $1/f$ noise to the amount of doping disorder in a Si/SiGe heterostructure [43].

The extracted $C_g = 113 \pm 4$ aF is plotted as a function of the differential voltage in Fig. 3(c). As expected, C_g shows almost no dependence on V, since the capacitance is primarily set by the size of the floating gate. The minor decrease of C_g at the largest V may be due to the lower barrier voltage leading to a smaller dot and therefore a lower C_g. The error in C_g originates from both the confidence interval of the mean value in Fig. 3(b) and from the systematic one-electron uncertainty between $N - 1$ and N. It should be noted that the measured value is the total capacitance of the floating gate, which can be further broken into the sum of the TJ and floating-gate-to-QD capacitances:

$C_g = C_{TJ} + C_{QD}$. The latter can be estimated simply as $C_{QD} = e/\Delta V \approx 10$ aF.

AFM-based charge locking allows us to reduce the footprint and stray capacitance $C_g = 113$ aF of the floating node by a factor of 700–7000 times compared to previous FET-based experiments [26,27]. From a metrological perspective, our approach allows a direct measurement of the subfemtofarad total capacitance of an isolated object by counting electrons using a QD charge sensor. In previous work [42], the capacitance standard based on counting electrons has been 16000 times larger.

V. TUNNELING STATISTICS AND RESISTANCE

From time traces similar to the one shown in Fig. 3(a), we can directly extract the statistical properties of sequential electron transport to the floating gate [39] and confirm its uncorrelated nature. In Figs. 4(a)–4(c), we plot probability density functions (PDFs) of the waiting-time distribution between adjacent tunneling events at various differential voltages. As expected for the uncorrelated transport of particles through the highly nontransparent TJ [44], the waiting times are distributed exponentially [45], $P(\tau) = \langle\tau\rangle^{-1} e^{-\tau/\langle\tau\rangle}$, where $\langle\tau\rangle$ is the mean time interval between tunneling events. Additionally, we can extract the time-correlation transport properties as shown in Figs. 4(e)–4(g). Here, we plot the distribution of the number n of events during a given time window t_0, which is chosen to fit roughly the same average number of events, $\langle n\rangle \approx 3$. We check that this choice does not affect the results. The theoretical Poisson distributions (solid lines), $P(n) = \lambda^n e^{-\lambda}/n!$, where the occurrence rate $\lambda = t_0/\langle\tau\rangle$ is determined experimentally by the mean time, match the experimental data very well, given that no fitting parameters are used. The second central moment (shot noise) of the distribution, $F = \langle(n - \langle n\rangle)^2\rangle/\langle n\rangle$, known as the Fano factor [45], closely fits the TJ limit of $F = 1$ [44,46], as shown in Fig. 4(h).

The extracted mean time interval $\langle\tau\rangle$ between tunneling events can be converted [47] to the average electrical current $I = e/\langle\tau\rangle$, plotted in Fig. 4(d) as a function of the differential voltage. The resulting I-V curve originates at the origin, confirming the statement that the charge leaks solely through the barrier gates. From the linear fit, we can extract the resistance of the TJ: $R = 6.8 \times 10^{18}\Omega$. Such a high value is immeasurable by conventional means and the FET-based charge-locking technique. The latter is because even a lower estimate of the typical FET stray capacitance of $C_{stray} \sim 100$ fF [26,28] (i) results in an almost infinite time constant $RC_{stray} \approx 700\,000$ s ≈ 8 days (acquiring the data for Fig. 4(d) would take months) and (ii) the QD sensor must be highly sensitive to catch the voltage jumps of $e/C_{stray} \approx 1.5$ μV. We address this limitation by dramatically reducing the stray capacitance of the floating gate (by 1000 times) to achieve a feasible time constant of approximately 700 s.

To cross check our findings about the origin of the charge leakage in multilayer devices, we fabricate a single-layer device. Here, seven floating gates sit strictly on the Si/SiGe substrate, which is now the only path for charge to

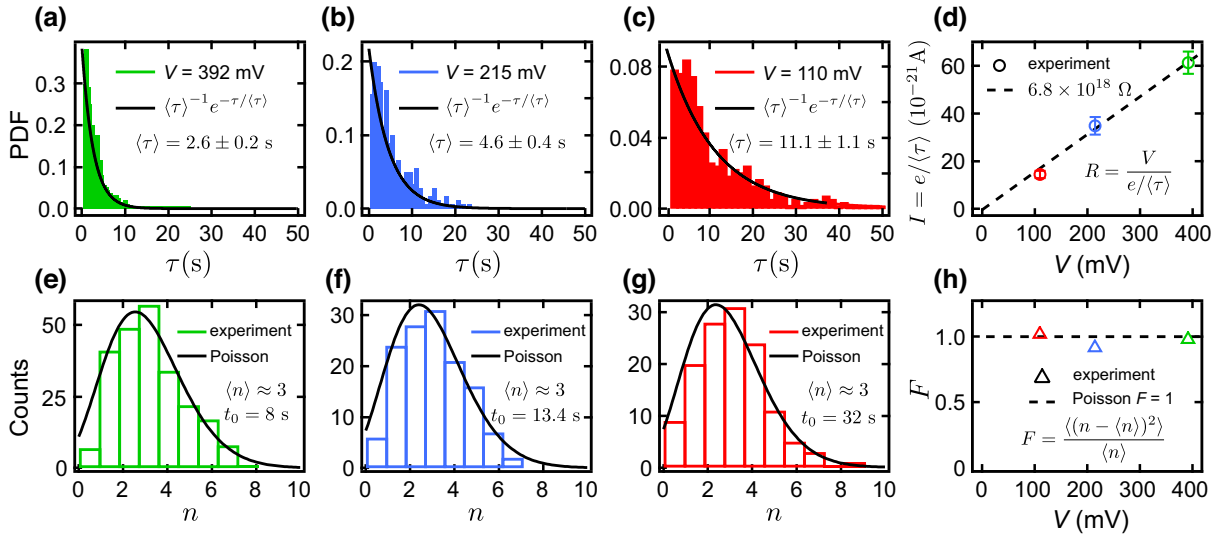

FIG. 4. (a)–(c) The PDF of the waiting-time distribution measured between consecutive tunneling events for various differential voltages. The solid lines correspond to exponential distribution fits with a mean value of $\langle\tau\rangle$. (d) The junction resistance can be extracted from a plot of the current $I = e/\langle\tau\rangle$ as a function of the differential voltage. The dashed curve corresponds to $R = 6.8 \times 10^{18}\Omega$. (e)–(g) The statistical distribution of the number $n = 3$ of electrons tunneling to the floating gate during a given time t_0. Three panels and their colors correspond to three differential voltages. The time t_0 is chosen to have the same mean number of events $\langle n\rangle \approx 3$. The solid lines show Poissonian fits with an expected occurrence rate of $\lambda = t_0/\langle\tau\rangle$. (h) The Fano factor plotted as a function of the differential voltage. The dashed line corresponds to the expected value $F = 1$ for an uncorrelated Poisson process.

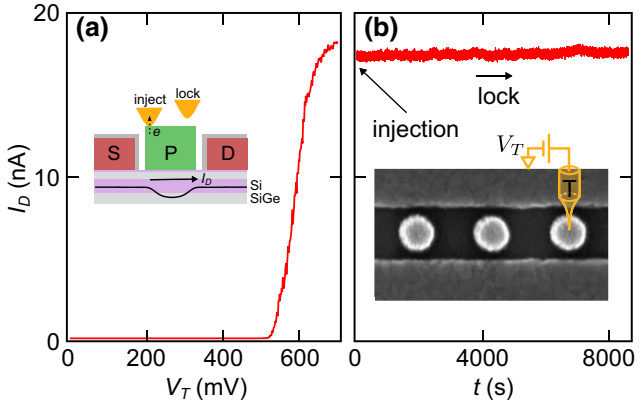

FIG. 5. (a) The single-layer device. The current through the device I_D measured as a function of the tip voltage V_T with the tip continuously touching the floating gate. The inset shows a cross section of the device. (b) I_D measured as a function of the time after the tip is withdrawn. The inset shows an SEM image of the device.

leak. Since all floating gates behave similarly, we present charge-retention data from one of them, as shown in the inset of Fig. 5(b).

We start in the continuous-injection mode sketched in Fig. 5(a), when the tip constantly touches the floating gate. As before, we measure the current I_D between the two ohmic contacts under the wide accumulation gates while applying a positive voltage V_T to the floating gate. The transistorlike turn-on curve shown in Fig. 5(a) lacks Coulomb oscillations due to the limited control of the confinement potential in single-layer devices. Figure 5(b) shows the current measured as a function of time after the charge is locked with $V_T = 700$ mV. In contrast to the multilayer-device data presented above, we do not observe any substantial charge leakage (tens of electrons) over several hours. As expected, the tunneling rate to the Si substrate is orders of magnitudes slower than the tunneling rate between overlapping gate layers.

VI. CONCLUSIONS AND OUTLOOK

In conclusion, we realize the ideal sample-and-hold circuit with a floating metallic gate fabricated on the surface of a Si/SiGe heterostucture. Utilizing the AFM tip as a switch allows us to reduce the plunger-gate footprint down to approximately 100 nm. The resulting stray capacitance of the floating gate is 2–3 orders of magnitude lower than in previous FET-based charge-locking studies. The reduction of the stray capacitance allows us to probe much higher junction resistances through single-electron counting than in previous studies. We find the average gate discharge tunneling rate to be of the order of one electron every few seconds in the overlapping gate architecture and multiple hours for single-layer devices. Thickening the Al oxide layer between the gates using atomic layer deposition could potentially improve the charge-retention time for overlapping devices. State-of-the-art high speed AFM scanners, however, can move laterally at only approximately 10 kHz and this value is limited by the resonant frequency of the cantilever [48]. This is too slow for coherent manipulation or readout of a spin qubit. Nevertheless, parts of the array that do not require fast pulsing, such as charge sensors, could be biased using the AFM-assisted sample-and-hold approach. Looking forward, the AFM charging approach demonstrated here could be combined with tip-based dispersive readout [49], enabling us to *in situ* tune and drag tip-induced QDs across the chip [50].

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