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Hardware for voice conferencing

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HARDWARE FOR VOICE CONFERENCING

Dean Romein

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Department of Information and Computer Science  
University of California, Irvine

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Institute of the Future, Menlo Park, California

### HARDWARE FOR VOICE CONFERENCING

The goal of the project was to design for the Institute For the Future a system for telephone conferencing via computer control. The system was to have up to 32 participants able to switch onto one of 8 conference lines at any time. It was assumed that each participant also had a terminal connected to a central computer which controlled the state of the conference. The participant was either in the talk or monitor mode on a conference line.

The system consists of 3 subsystems, the receive state control, the telephone line control, and the send state control. To the computer, the whole system is viewed as a terminal. Because of long lead times experienced in acquiring parts, much of the system was designed using small scale integration. The parts count could be reduced through the use of medium scale integration. The send state control and the automatic telephone answering have not been thoroughly been debugged, but it is believed few modifications need to be made. All physical layouts assume a 6 1/2 by 4 1/2 inch, 32 connector vector board.

The receive state control receives two characters, the first being the state in which the line is to be and the second character the telephone line affected. The sequence of the steps are:

1.) The leading edge of the start bit turns on the start flip flop which allows the rest of the system to see the clock.

2.) The clock is divided by 32. In the middle of the bit timing, the bit is sampled onto the shift register.

3.) After the time for 9 bits has been counted, if the first bit of the last character received is a one, the address is decoded and a pulse is sent to the proper line board, which then switches to the proper state. The state of the device is communicated through pins T12-T16. To address lines 17-32, the address undecoded is sent to another board using board pins T3-T7. Board pin T11 sends the strobe for the time to sample the address lines.

4.) After all of the above occurs, one clock time, the divide by 32 flip flops are cleared, the start stop flip flop is turned off, and the count 9 flip flops are cleared.

The code for the address character is:

Bit 1 0

Bit 2  $2^0$

Bit 3  $2^1$

Bit 4  $2^2$

Bit 5  $2^3$

Bit 6  $2^4$

Bit 8 not used

The code for the state character is:

Bit 1 1

Bit 2  $2^0$  Party Line Number

Bit 3  $2^1$  Party Line Number

Bit 4  $2^2$  Party Line Number

Bit 5 ENABLE

Bit 6 0 is monitor mode, 1 is talk mode

Bit 8 not used

For both characters, bit 7 is used to start sending state of system. The state of the system sent by the transmit subsystem tells whether or not a line has been accuated by the automatic telephone answering unit. The board connections are:

1 +5 Volts

2 GND

3-7 Undecoded Line Address

9 Send System State

10 TTY Input Line

11 Change State Pulse

12-16 Party Line State Change

17-32 Telephone Address Lines

The telephone line control consists of one board as described per telephone line. Because not all of the parts were ever received, an actual layout is not presented, nor

is the automatic answering system. It is assumed that a line could not be answered unless the line was enabled and that a line would be hung up by disenabling the line. The one of eight switch is a LM3705 analog switch, the talk-monitor switch is a Siliconix DG172CJ, and the amplifiers are LM307Ds. The transformer is a UTC SO-1 with a 200/50 ohm primary connected to the network and a 250k/62.5k ohm secondary connected to the telephone line board. The values of the capacitors and resistors are critical because of impedance considerations. Capacitor C3 is especially critical. The specifications are:

R1	1.0 Mohms
R2	100 Kohms
R3	91 Kohms
R4	2.4 Kohms
R5	2.4 Kohms
R6	1.0 Mohm pot
C1	.12 mfd.
C2	.27 mfd.
C3	.082 mfd.
C4	.68 mfd.

The board connectors are:

- 1 +5. Volts

2	GND
3	+15. Volts
4	-15. Volts
5	Talk or Monitor
6	Party Line Enable
7	$2^0$ Party Line
8	$2^1$ Party Line
9	$2^2$ Party Line
10	Addressed Change State Pulse
12	Telephone Line White Wire
13	Telephone Line Black Wire
14	Telephone Line Red Wire
15	Telephone Line Green Wire

The send state control is initialized by a 1 in the seventh bit of a received character. This is send board pin T9. Initially a start pulse turns on the start flip flop which allows the clock to be run through a ripple counter. At the initial time, the states of 16 telephone conference lines are parallel shifted into a shift register. The state of a telephone line tells whether the automatic answering mechanism has been accuated by someone calling in onto a particular line. Then the start bit and eight state bits

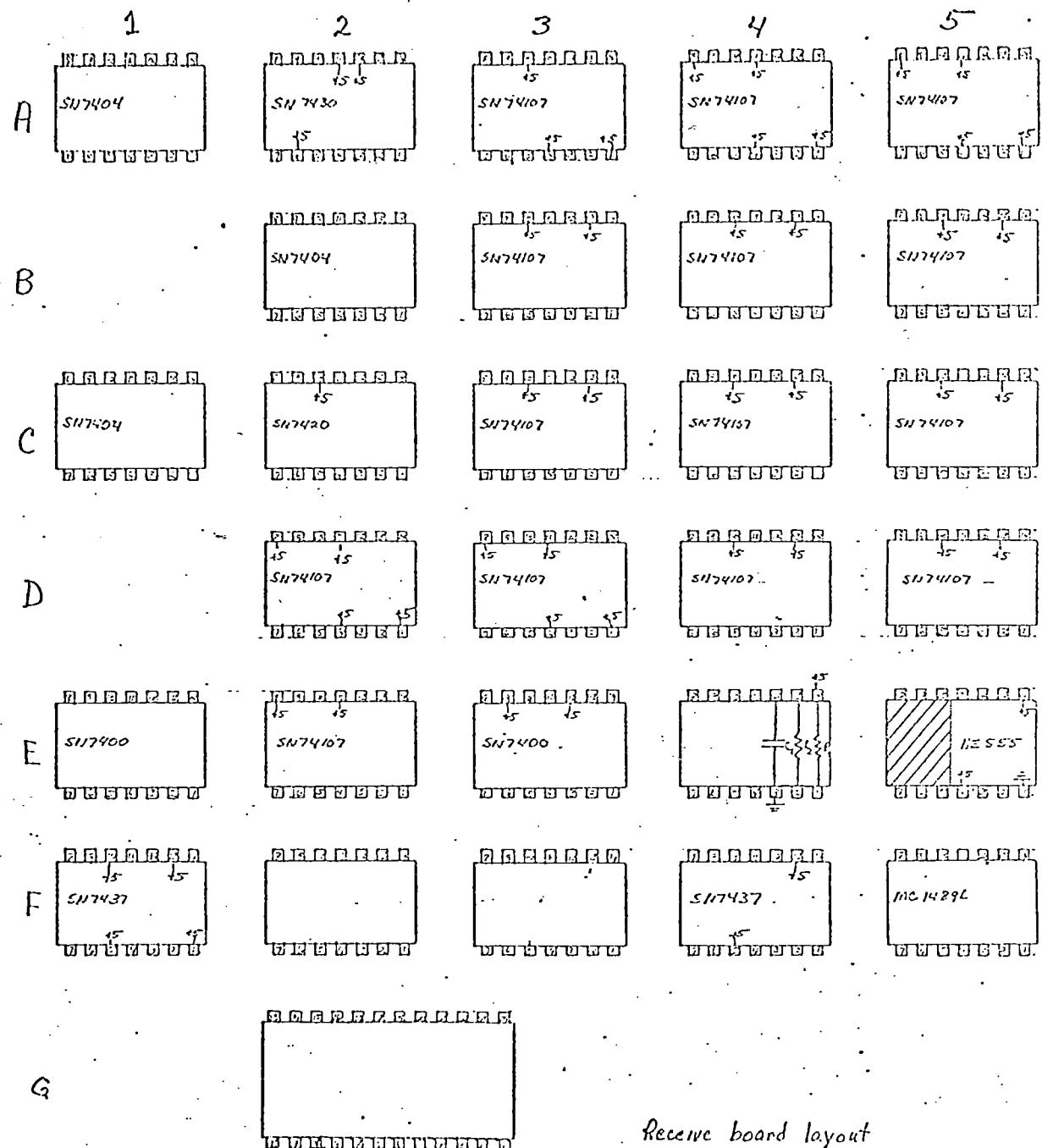
are sent out followed by a wait of five bit times and then the next character is sent. As it is presently arranged, the same telephone conferencing lines are again sampled and the information broadcast again. The transmit state subsystem then turns off until the next start strobe is received. It is planned that this plan is expandable to 32 lines by a signal at board pin T5. This pin signals when the first two characters have been sent. With the addition of more boards, the input to pins T17-T32 could be changed at this time. The board connectors are

- 1 5. Volts
- 2 GND
- 3 +15. Volts
- 4 -15. Volts
- 5 End of sending first two characters.
- 6 TTY transmit line
- 17-32 telephone line states

The clock chip on this board and the receive board is a NE555. For 110 baud lines, the RC constant requires

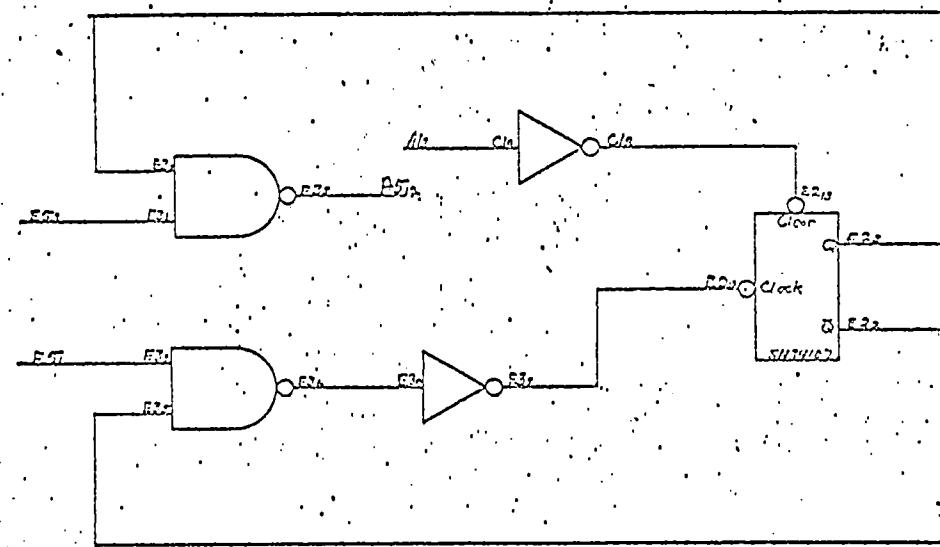
- R1 1.3kohms
- R2 2490 ohms
- C1 .0656 mfd.

All components have 1% tolerances.



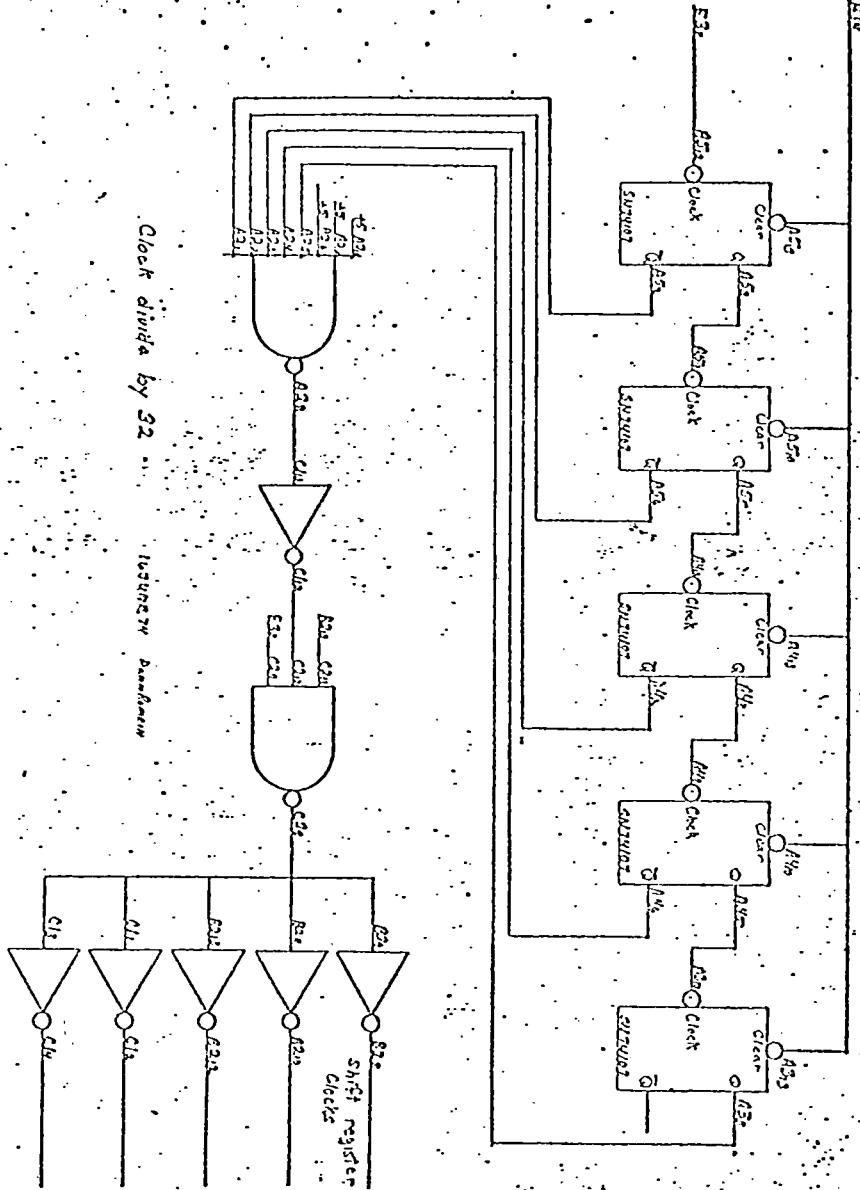
32 terminal board

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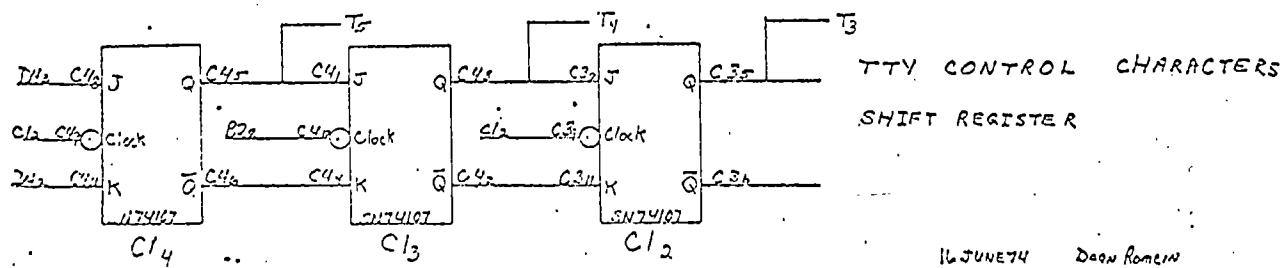
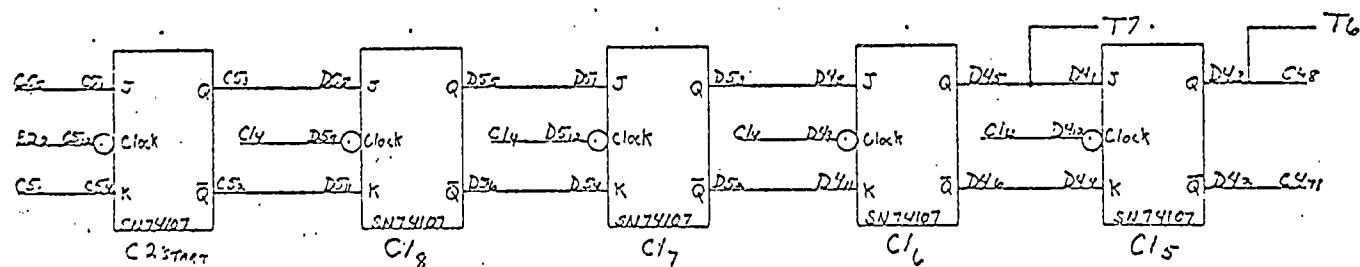
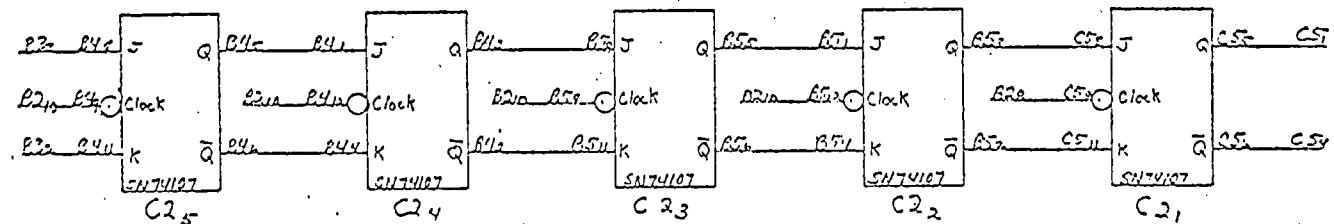
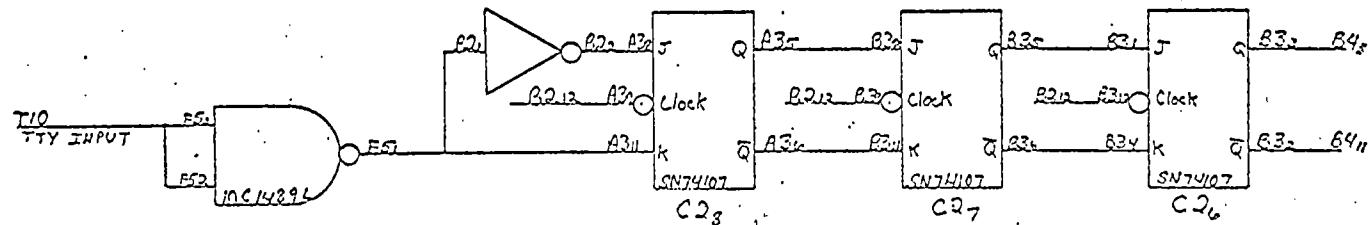


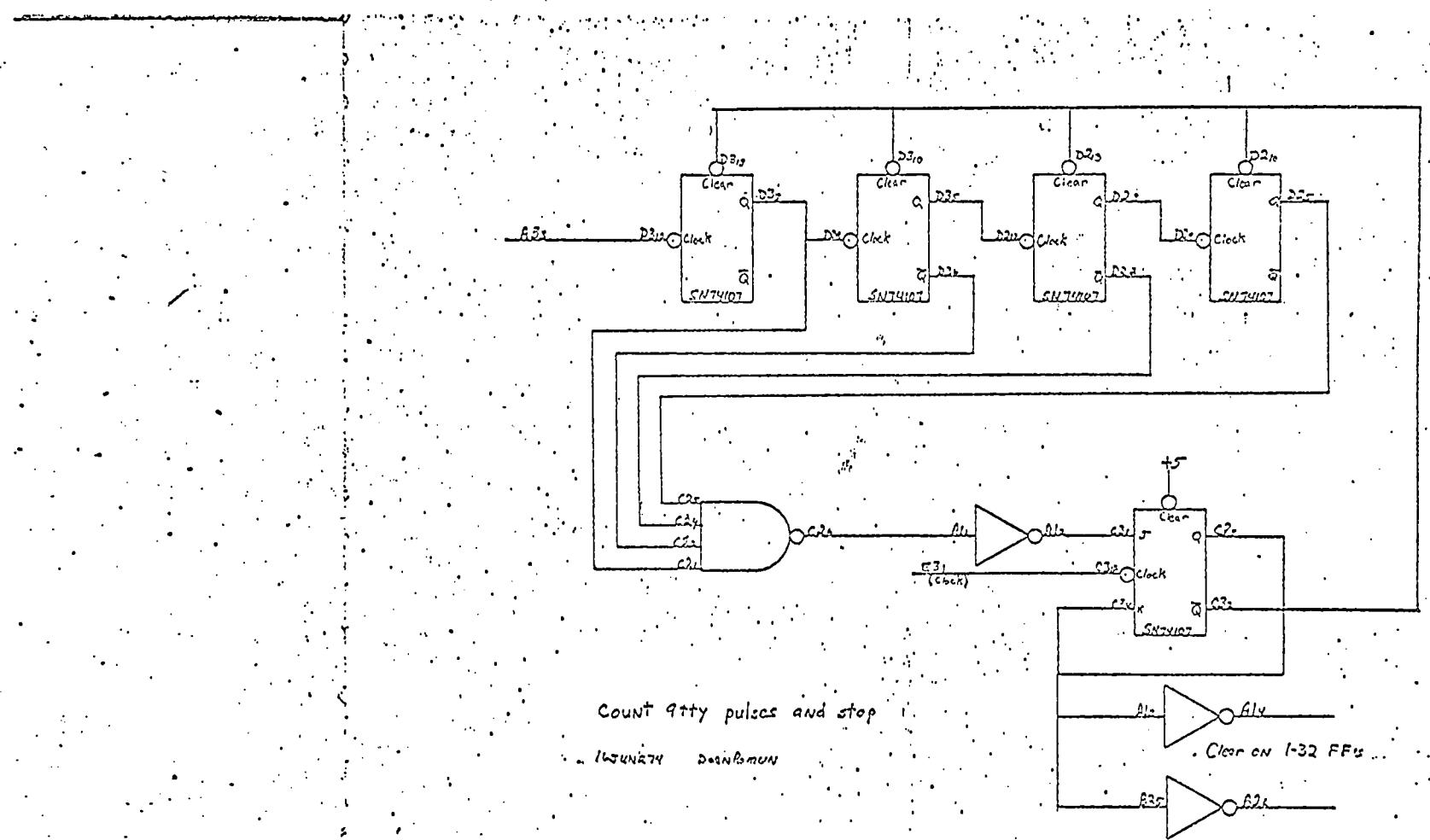
Start Stop Flip Flop

Inverting Outputs



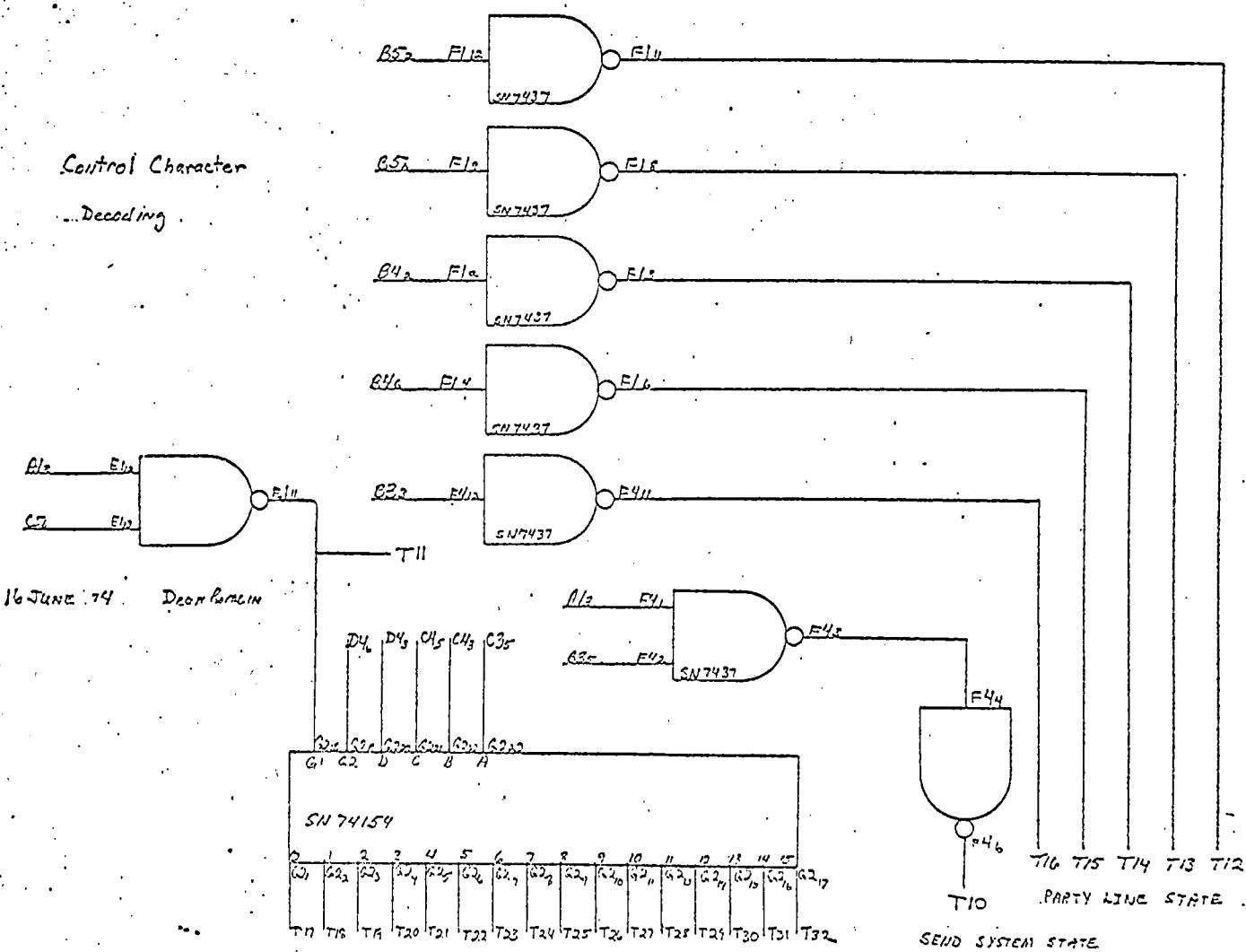
Clock divide by 32  
16000274 diagram



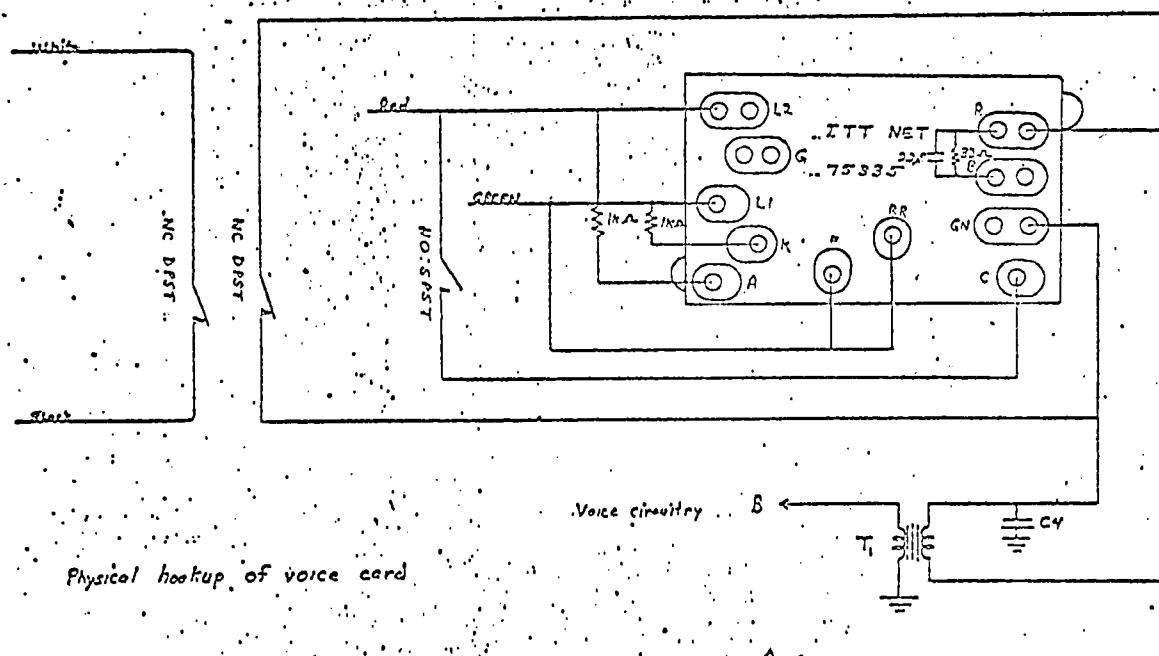


*Control Character*

*Decoding*



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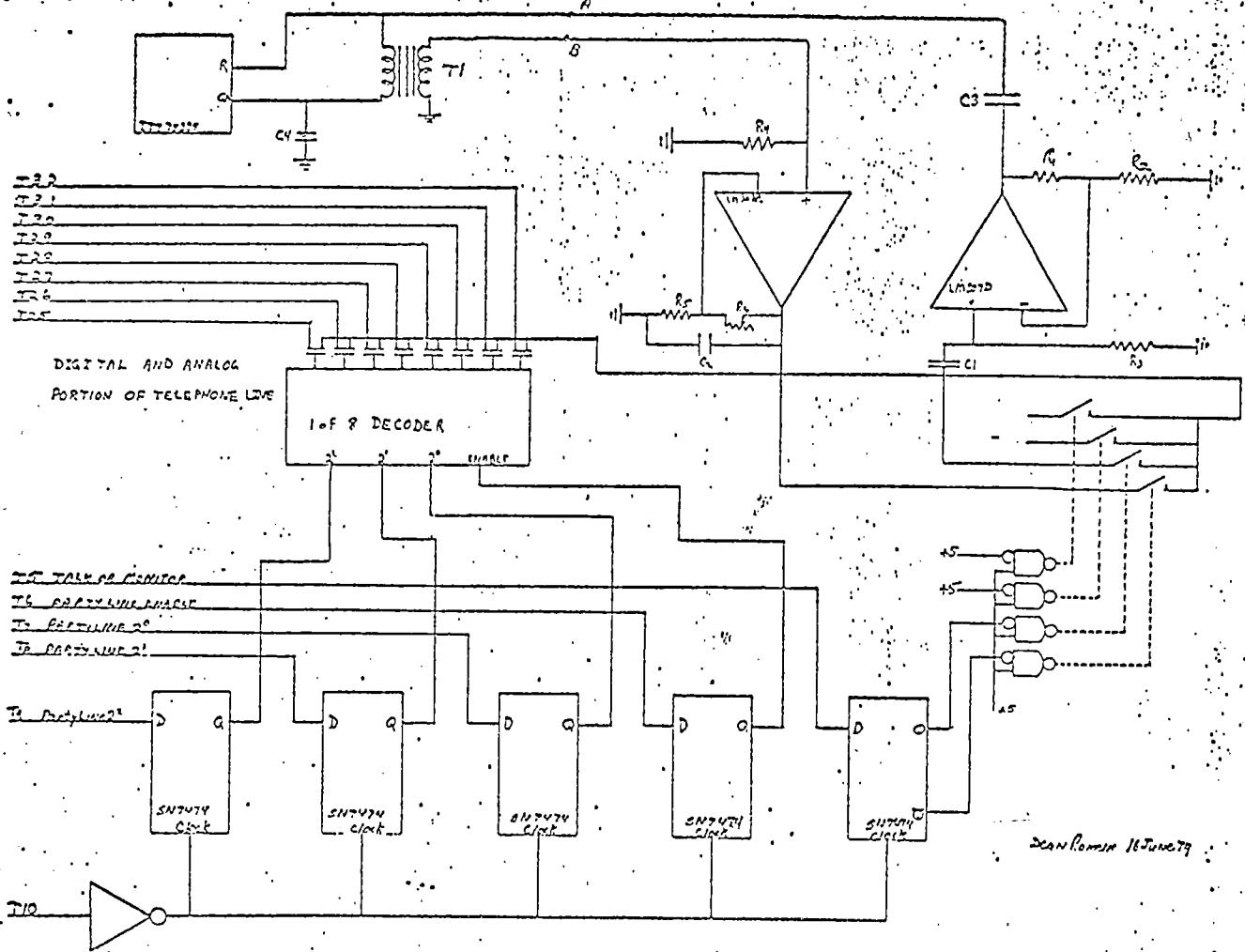


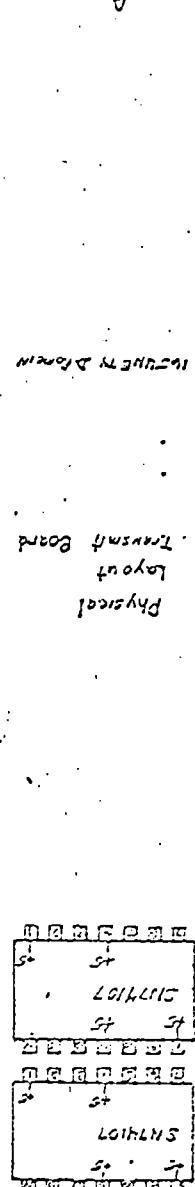
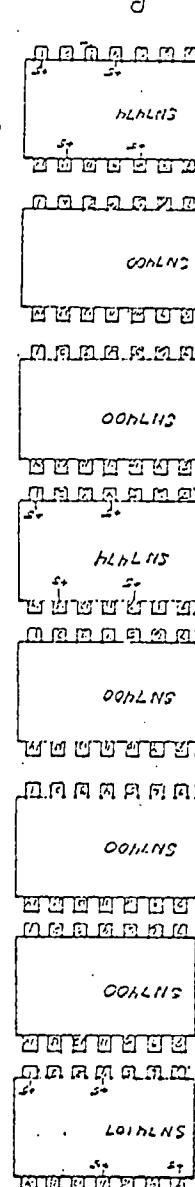
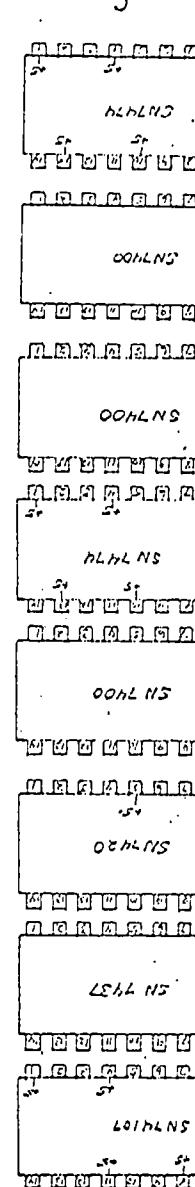
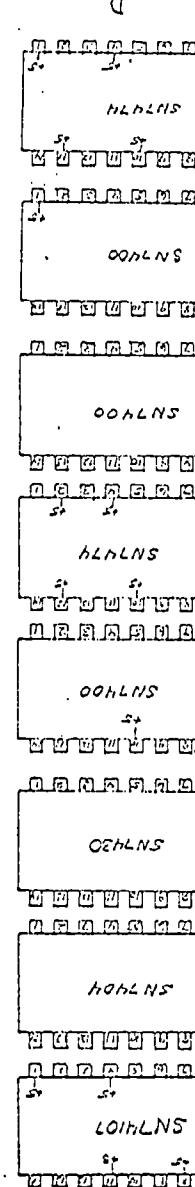
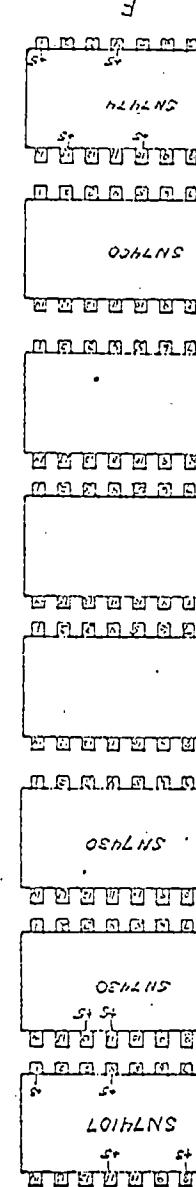
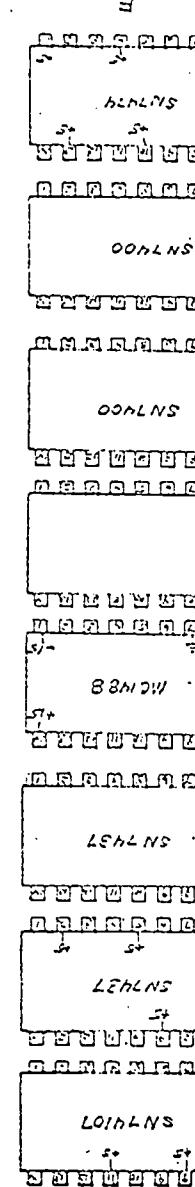
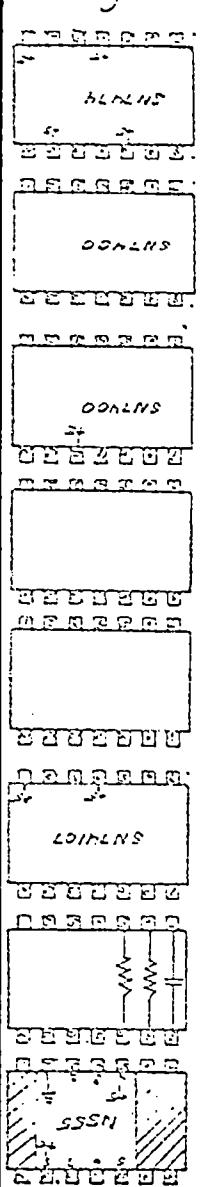
Physical hookup of voice card.

to telephone line

Ring detection done on Red-Green lines.

16 June 74, Dean Berlin





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L

- LAYOUT DESIGN

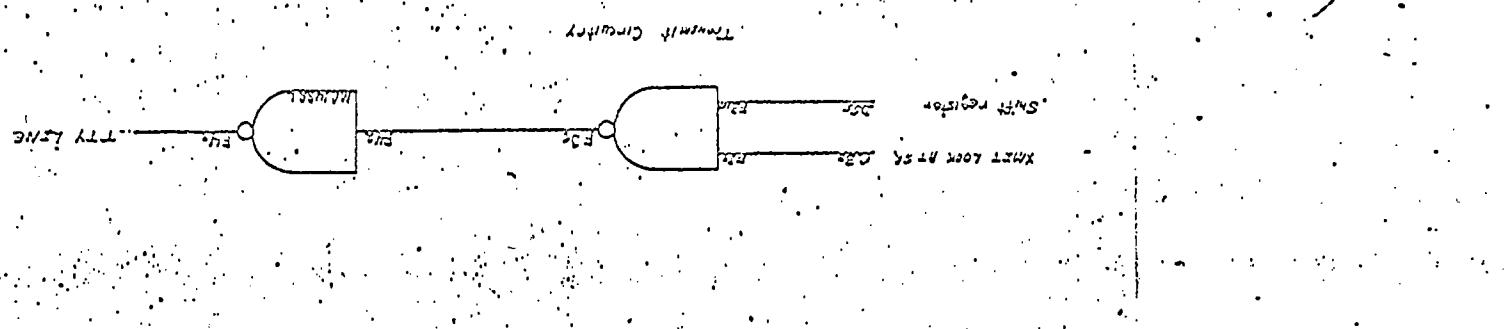
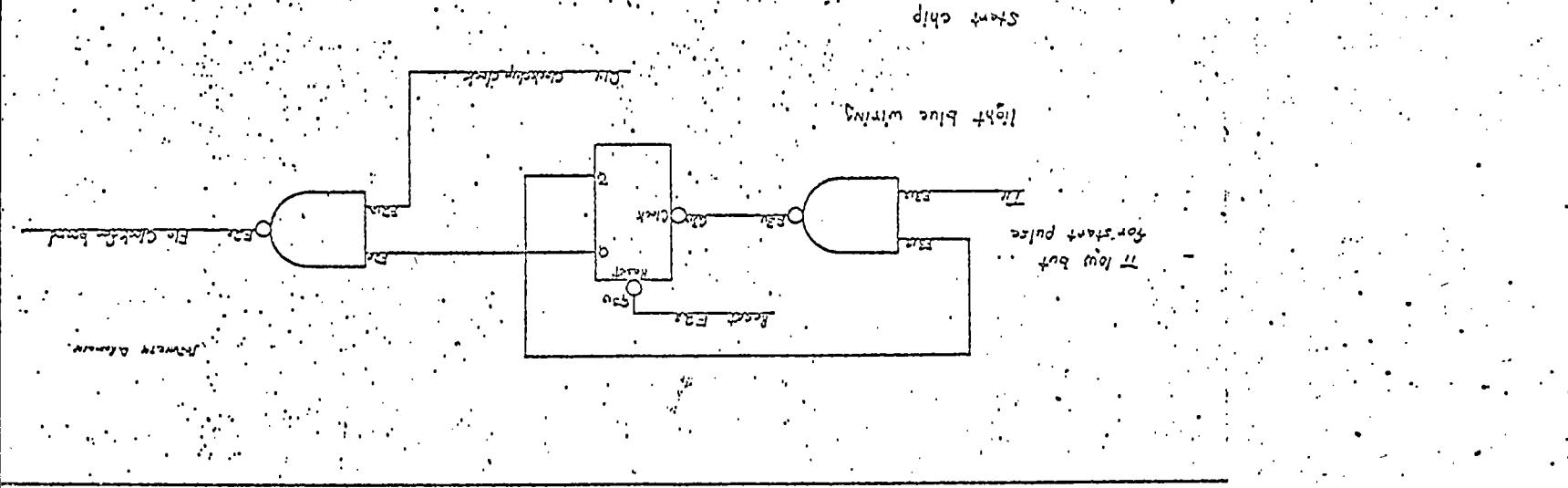
9

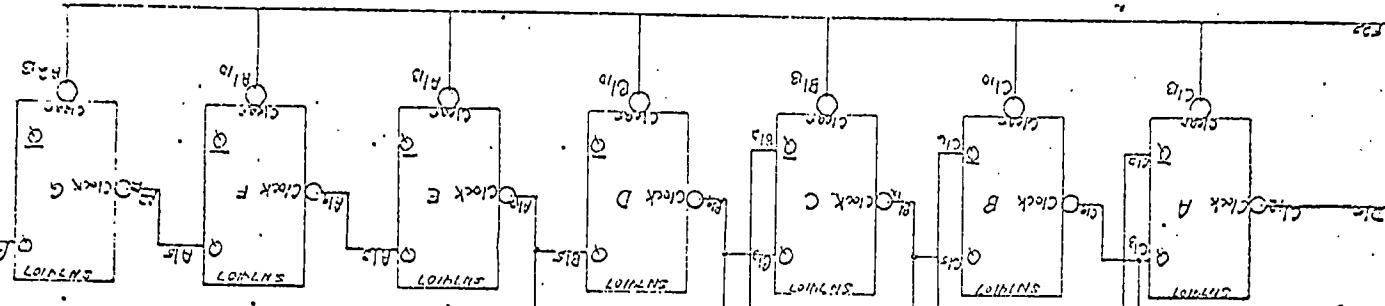
5. Layout Board  
Physical

4

3

2





stage N in diagram

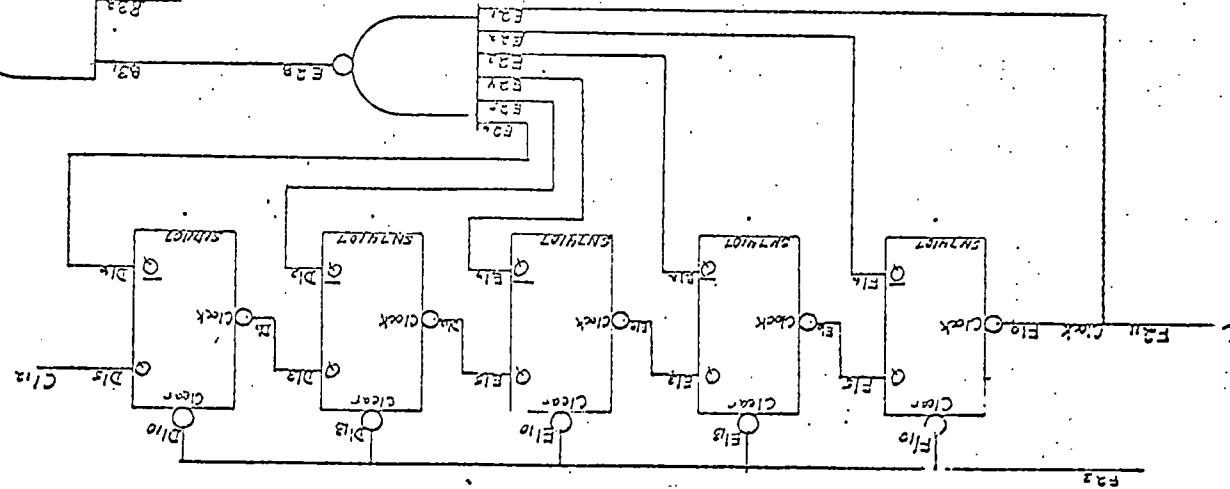
Ripple counter Clock

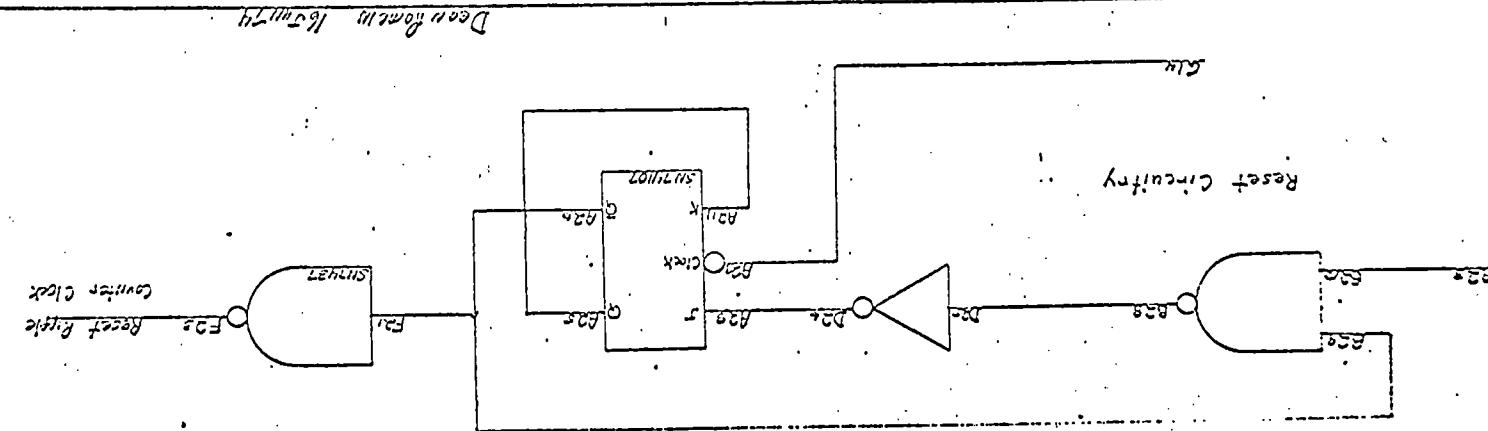
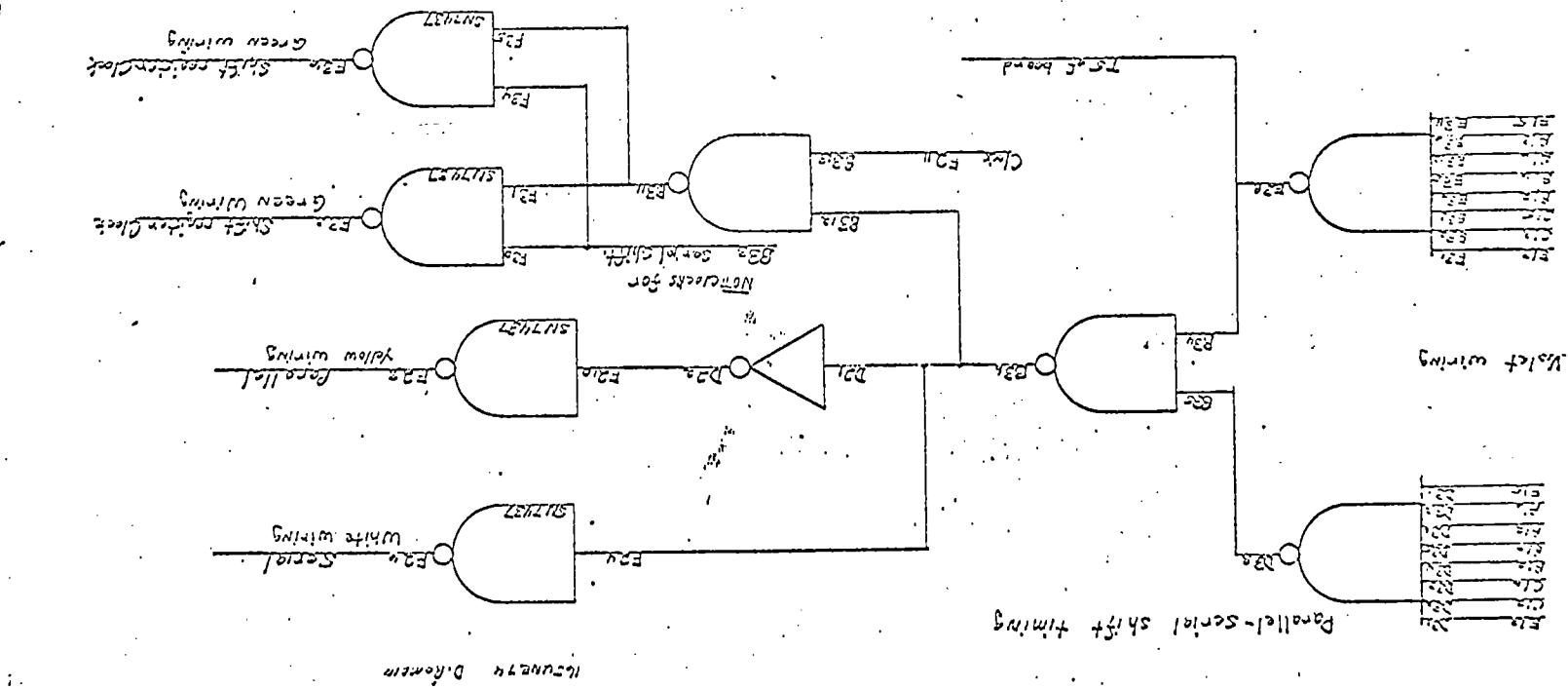
Next logic - write

Ripple counter-Output

stage R in diagram

stage S in diagram





F26      serial

Dear Homer 16 June 74



G603  
G61  
G62  
G70  
G71  
G72  
G73  
G74

Q61  
Q62  
Q63  
Q64  
Q65  
Q66  
Q67  
Q68

C70  
C71  
C72  
C73  
C74

E3  
E3  
E3  
E3  
E3

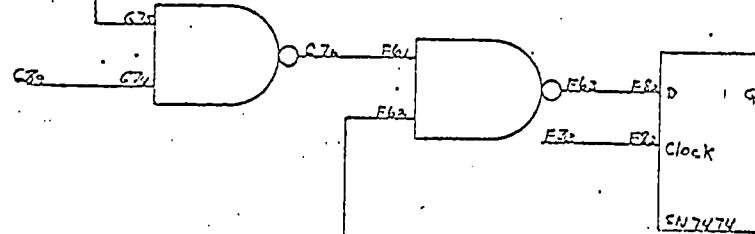
FF1  
FF2  
FF3  
FF4  
FF5

SN7474  
SN7474  
SN7474

F27      parallel

Green wiring      FF clocks  
white wiring      Serial shift enable  
yellow wiring      Parallel shift enable  
brown wiring      Parallel input  
gray wiring      all other

F28      serial



E61  
E62  
E63  
E64  
F61  
F62  
F63  
F64

Q61  
Q62  
Q63  
Q64  
Q65  
Q66  
Q67  
Q68

C70  
C71  
C72  
C73  
C74

E3  
E3  
E3  
E3  
E3

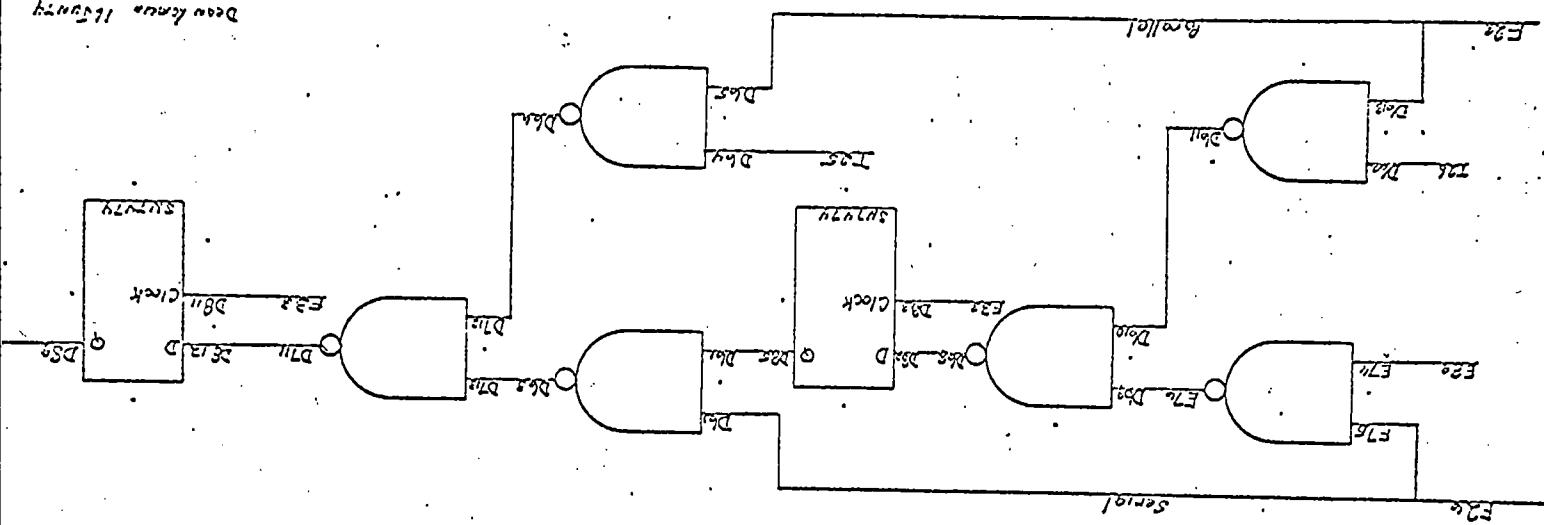
FF1  
FF2  
FF3  
FF4  
FF5

SN7474  
SN7474  
SN7474

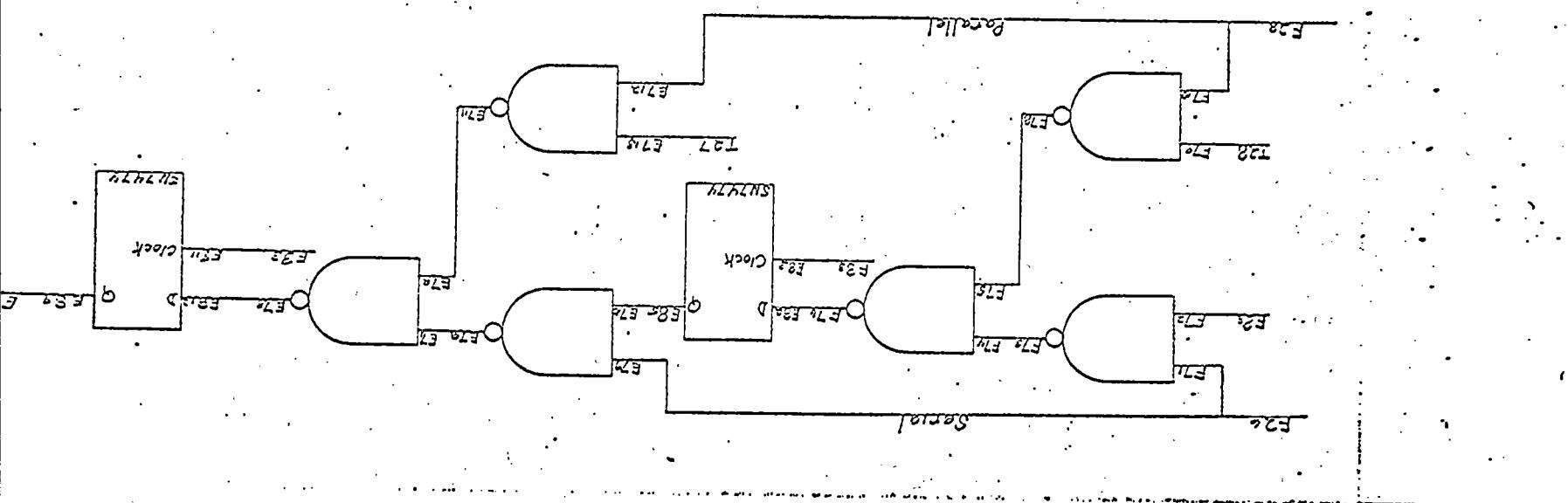
F29      parallel

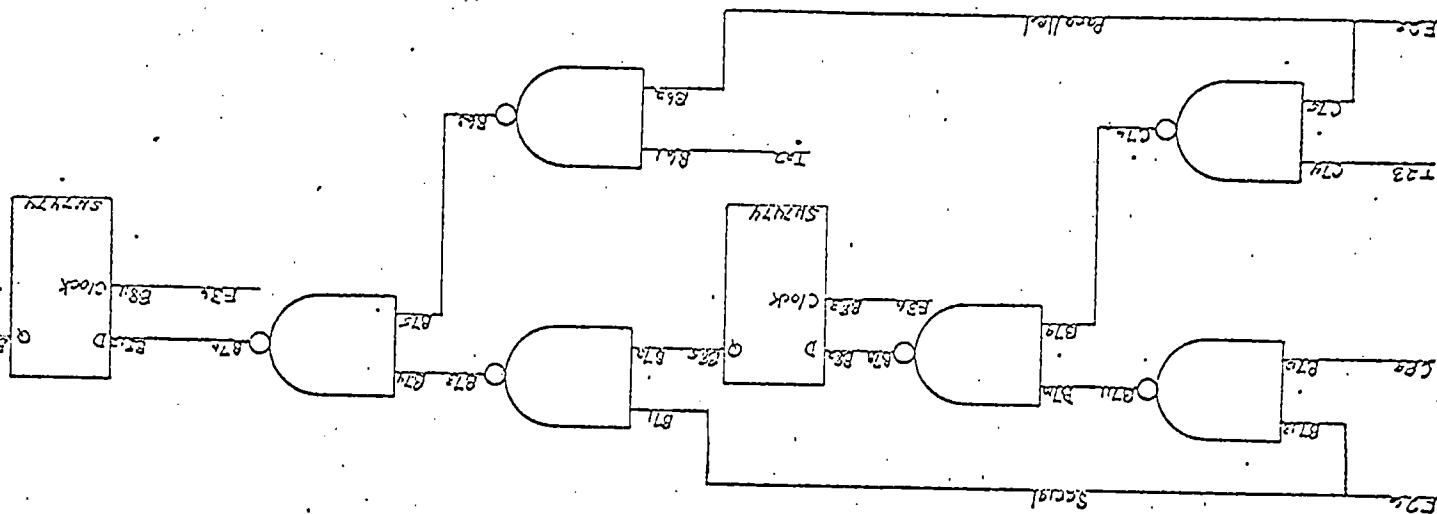
Shift register page 1

Debounce circuit

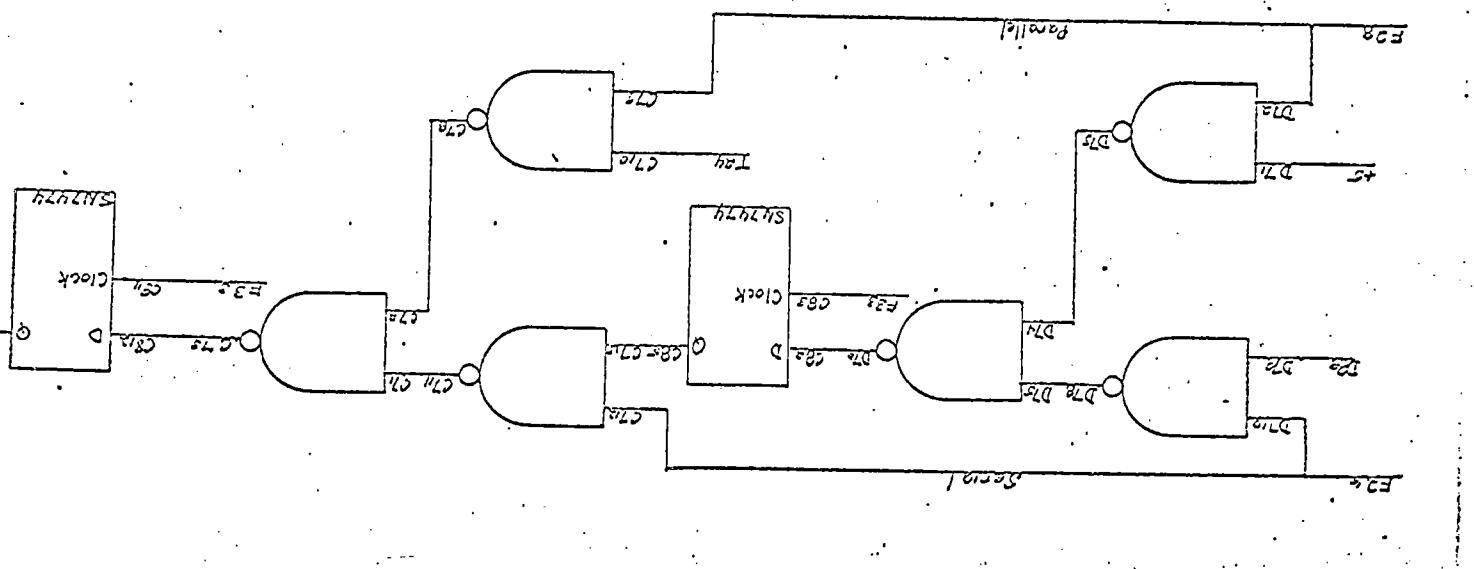


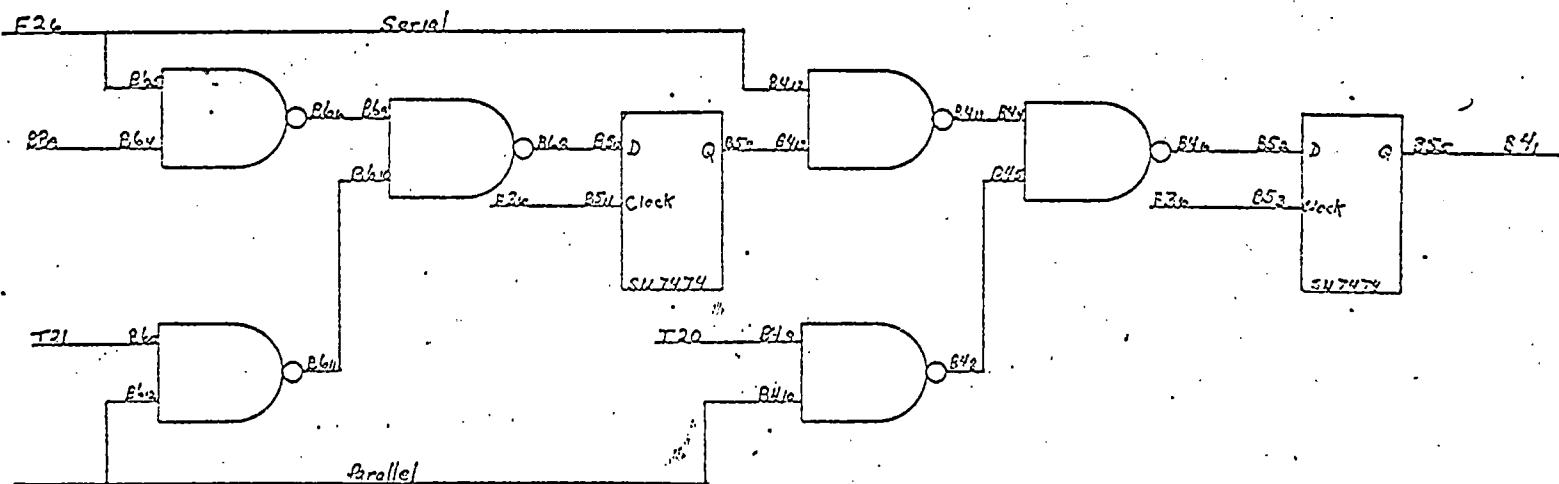
Program 2 shift register



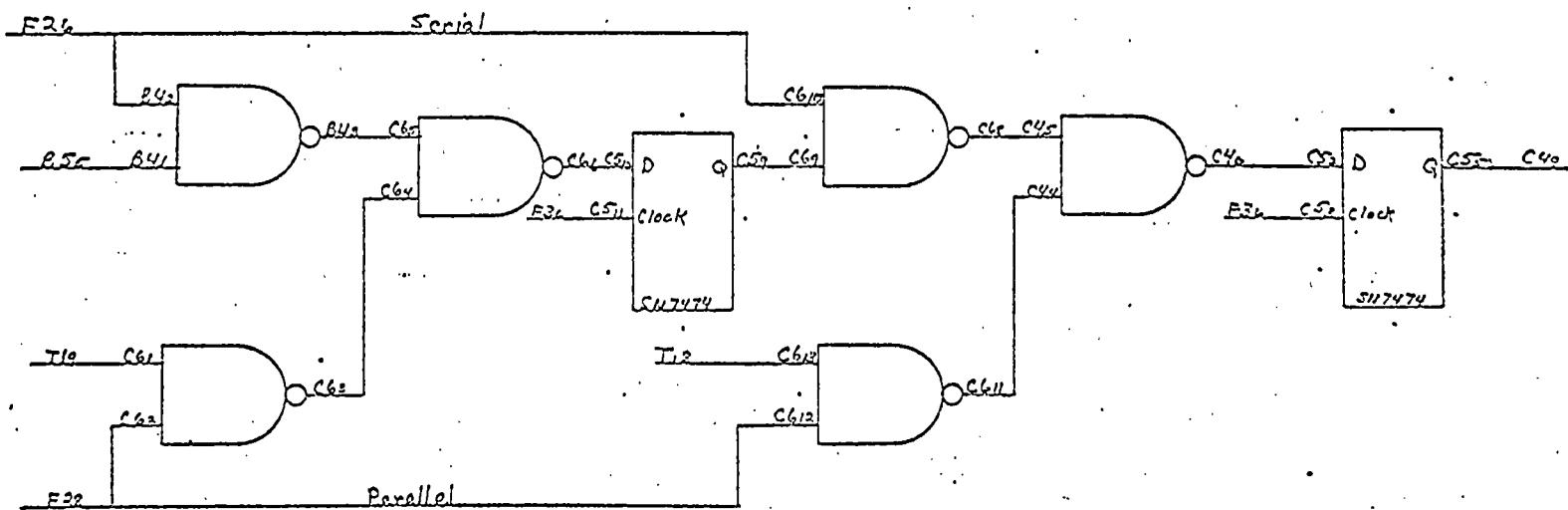


Shift register Page 3



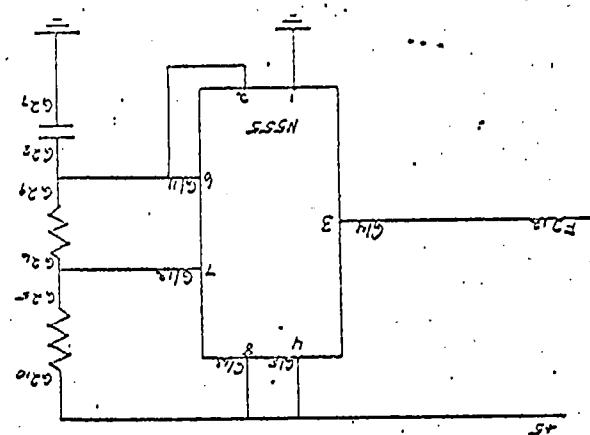


SHIFT Register Page 4



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Clock circuitry



Debounce / latching

Shift register pass

