CMP Modeling as a part of Design for Manufacturing

Shantanu Tripathi, Adrien Monvoisin, Prof. David Dornfeld, Prof. Fiona M. Doyle
University of California, Berkeley CA 94703 USA

E-mail: shantanu@berkeley.edu

CMP faces numerous challenges, as we move towards 45-nm and 32-nm nodes. The most important of these, as identified by ITRS [1], are: a) reliably predicting and controlling post-CMP topography (dishing and erosion loss should be limited to within 10% of the interconnect height throughout the die); b) Integration of ultra low-K dielectric materials, including predicting stresses and damage, and designing very low stress polishing processes; and c) designing new planarization processes for new materials and new requirements.

To address these, a multi-scale (feature/die/wafer) CMP modeling framework is being developed for enabling Design for Manufacturing (DfM) and Manufacturing for Design (MfD). Topographic evolution has been studied for Shallow Trench Isolation CMP and is now being extended to copper CMP. A detailed, quantitative understanding of the mechanism(s) of CMP is being elucidated, using fundamental experiments and a mechanistic model based on physical data. Stress issues in low-K dielectric during copper CMP, which can lead to fracture and delamination, are being studied using Finite Element Modeling.

Keywords: Chemical-mechanical Polishing, Design for Manufacturing (DfM), CMP Mechanism, Multi-scale modelling, Stress Analysis.

1. Introduction

International Technology Roadmap for Semiconductors (ITRS) identifies numerous challenges facing the Chemical Mechanical Planarization (CMP) process and its use in engineering manufacturable interconnect structures: reliably predicting and controlling post-CMP topography (dishing and erosion loss should be limited to within 10% of the interconnect height throughout the die); integration of ultra low-K dielectric materials, including predicting stresses and damage, and designing very low stress polishing processes; designing new planarization processes for new materials and new requirements; lack of fundamental physical data & mechanisms; and lack of interconnect/architecture design optimization tool. CMP models capable of predicting the effect of slurry additives on polish rates, the lifetime of consumables (e.g., pads, conditioners) and their impact on polishing uniformity are in their infancy. Basic process characterization is poorly understood and more systematic and fundamental approaches to characterize these systems are required [1].

In this paper, we try to address some of these CMP issues. A multi-scale (feature/die/wafer) CMP modeling framework is being developed for enabling Design for Manufacturing (DfM) and Manufacturing for Design (MfD). In Section 2, we look at pattern dependent topographic evolution. In Section 3, a detailed, quantitative understanding of the mechanism(s) of CMP is elucidated, using fundamental experiments and a mechanistic model based on physical data. In Section 4, stress issues in low-K dielectric during copper CMP, which can lead to fracture

and delamination, are being studied using Finite Element Modeling. In Section 5, the framework for multiscale modeling is illustrated, followed by its possible application for an optimization example in Section 6.

2. Pattern Dependent Topography Evolution

CMP of patterned wafers leaves defects like dishing & erosion. These defects cause problems in: a) STI CMP: nitride erosion damages underlying silicon in active areas; b) Copper CMP: dishing & erosion increase RC circuit delay, and erosion can also cause open-circuit. Post CMP pattern dependent defects are a result of non uniform material removal. The main source of pattern dependency in CMP is the non uniform contact pressure between the polishing pad and the micro topographies on the wafer [2]. The local polishing pressure depends on the effective local pattern density which a weighted sum of pattern density surrounding the point on the wafer under study.

Utilizing this idea modeling approaches has been developed: an empirical full-chip model at MIT [3]; a physical local model [4]; and a physical-semi-empirical full-chip model at Berkeley [2]. In the Berkeley model, the layout dependant chip scale variation in CMP is captured as a function of the physical properties of consumables and process parameters. The local material removal rate is expressed as a function of asperity height distribution, asperity size, abrasive size, hardness of the polishing material, and the pattern density. This approach has been successfully applied for predicting CMP topography evolution for ILD CMP [5] and a modified model has been used for STI CMP evolution [6].

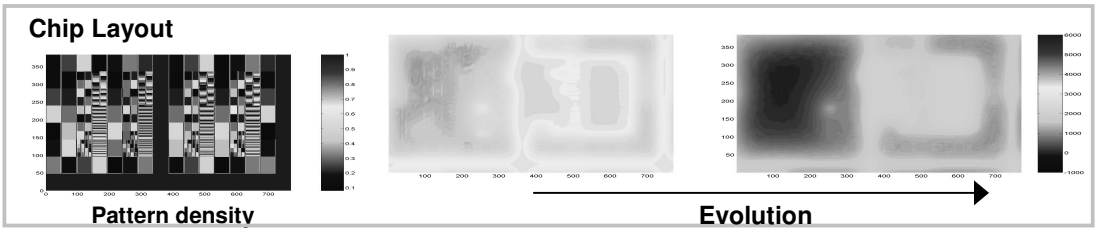

Fig. 1 Topography Evolution Prediction during STI CMP

3. CMP Mechanism

Extensive modeling and analysis of CMP process has been done from a purely mechanical or a purely chemical perspective, without explicitly addressing their synergism. CMP, particularly copper CMP, is a transient chemical process with intermittent mechanical phenomena. We are developing an integrated tribo-chemical model of copper CMP that considers abrasive and pad properties, process parameters (speed, pressure etc.), and slurry chemistry to predict material removal rates.

During CMP, abrasive particles interact intermittently with a particular point on copper being removed. The chemical action of the slurry passivates the surface of copper. The removal of passive films by abrasive action makes the surface temporarily more reactive. The oxidation rate of copper when stripped of the passive film is fairly high and it progressively decreases. Thus a comprehensive mechanistic study of copper CMP has three important components: 1) passivation kinetics of copper (oxidation rate of copper as a function of thickness of passive film); 2) mechanical properties of passive films (the ease with which abrasives can remove

passive film, exposing bare copper and thus enhanced reaction rates); and 3) abrasive-copper interaction force and frequency.

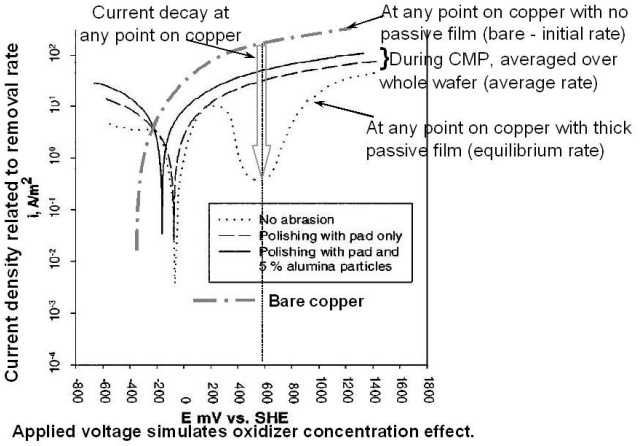

Fig. 2 Passivation Kinetics of Copper

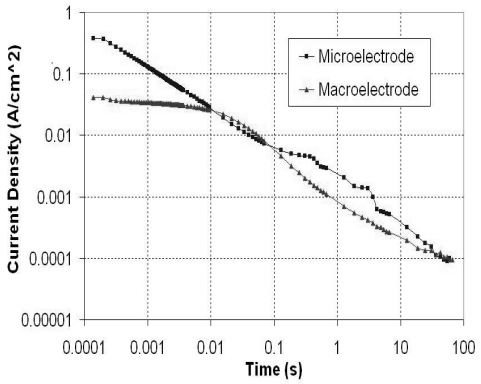

Fig. 3 Current Decay Post Potential Step

Passivation kinetics of copper is being studied using potential step repassivation and scratch-repassivation techniques. The figures (2 and 3) above show the polarization curves of copper under different conditions and the current decay post a potential step experiment [7]. The mechanical properties of passive films are being studied using an atomic force microscope (AFM). An AFM tip of roughly the same tip radius as an abrasive particle is made to act like an abrasive. It is used to scratch the surface of copper in presence of slurry chemicals. The contact force and the scan frequency are also varied during these scratching experiments. An AFM image of an area scratched using the AFM tip is shown within Figure 4 (in the box titled – Mechanical Response of Passive Films). The abrasive concentration, pad properties and process conditions are used to calculate the frequency and force of interaction of abrasive particle with the film.

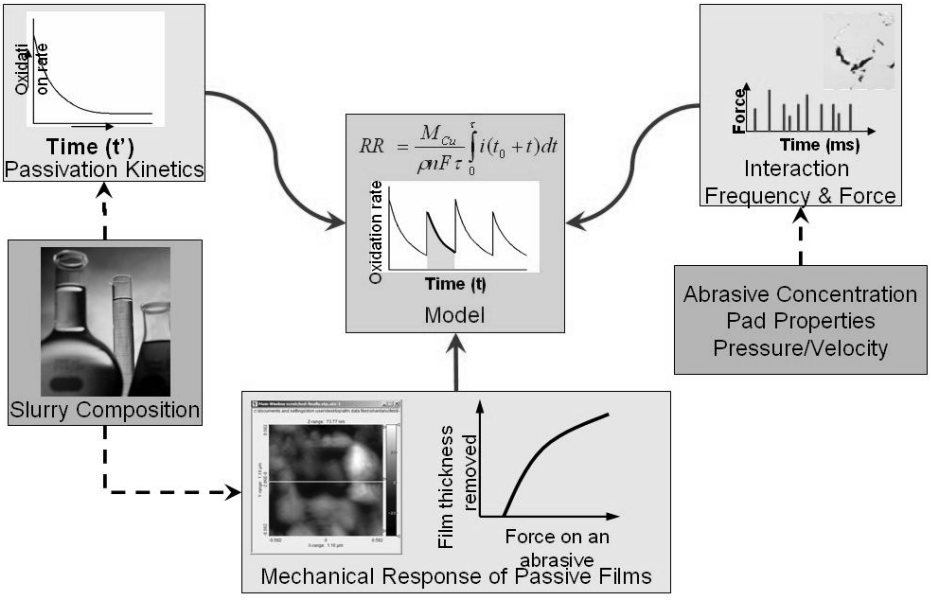

Fig 4. Integrated Removal Rate Model considering Passivation Kinetics, Mechanical Properties & Interaction Frequency

4. Stress Analysis during CMP

Use of low-K dielectric materials would help reduce interconnect delays significantly, but most of the potential low-K dielectric materials are mechanically very weak, with low Young moduli. CMP process can result in high stresses in the layers of low-K dielectrics and can lead to fracture and delamination. Stress fracture related issues during CMP are being studied using Finite Element Modeling (FEM). The analysis of the Von Mises stresses, from the FEM results, can indicate the likelihood of the propagation of cracks in the sub layers polished.

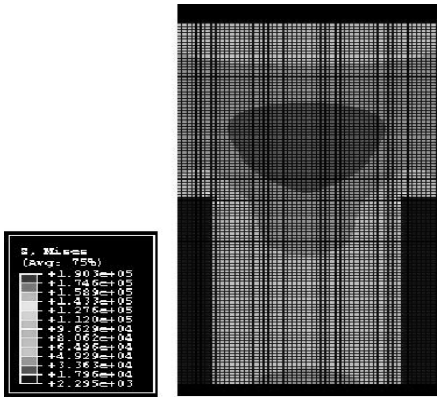

Fig 5. Von-Mises Stress on a Structure with 200nm Copper Layer over a low-K Dielectric

5. Multi-scale CMP Modeling

The pattern evolution approaches illustrated in Section 2 have proved successful for predicting defects on large features for a fixed CMP process; it cannot be extended for a different process recipe. In the empirical MIT approach [3], test pattern wafers (with features similar to final product wafer) are polished under fixed processing conditions. Measurements after CMP yield certain parameters (particularly the range of effect of surrounding features) which feed into the CMP evolution model. Starting from a preliminary product design layout, this model is used to predict topography post CMP. If the defects in a certain region are large, then product design is modified, primarily by adding dummy features. This method helps to decrease design related CMP defects to an extent, but does not try to optimize the process at all. In fact the model is blind to the CMP process and treats it like a black box. This is because of the lack of process understanding, and only the best guess process is chosen while design optimization. Ideally we would want to be able to optimize the design and process together.

The CMP model has further drawbacks. Current models treat the CMP pad as a flat surface, and that is one reason for them being unable to predict pattern evolution correctly. Even for a fixed process it is unable to predict evolution of small features, because the model captures only 1 source of pattern dependency. The source of pattern dependency is two fold: 1) Pad hard layer flexion due to soft layer compression (partially addressed by previous models): mm scale; and 2) Asperity contact area (not addressed yet): 10µm scale (the pad touches the wafer at very few points called pad asperities. The size of these contacts is typically about 10µm)

The resolution of above models is fairly coarse, of the order of 10-20 µm. For combined process-design optimization we require to have a detailed process understanding. In fact CMP process is usually much less rigid than other microfabrication processes and there is an opportunity to have considerable design specific process optimization. To develop a model

that can do such an optimization we require that we capture multiscale CMP phenomena at considerable resolution and speed

One approach for the new framework is illustrated in Figure 6. We start by integrating the process & consumable information into the existing model using a robust material removal rate model (mechanistic model developed in Section 3). We also introduce the impact of asperity contact area in addition to the pad flexion effect. In order to be able to resolve topography evolution at the fine feature scale we would require that a new kind of data structure be developed to capture the large amount of information for a full chip scale model.

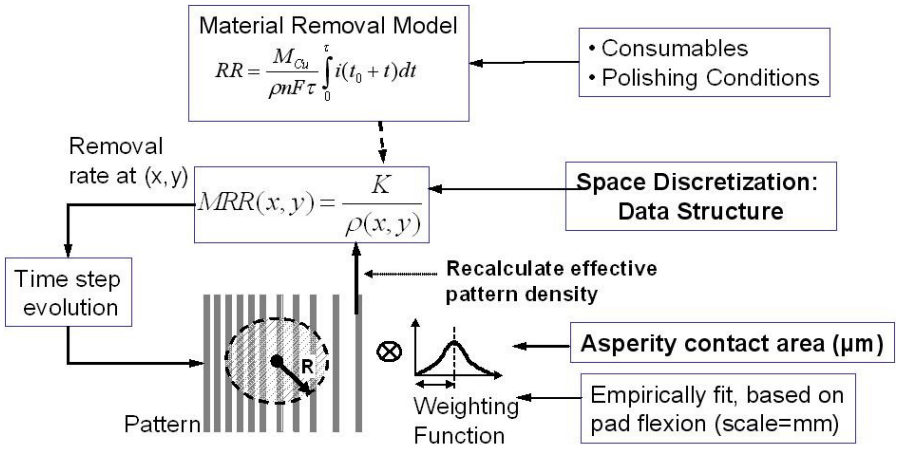

Figure 6. Proposed Multiscale Pattern Evolution Framework

Work is in progress to develop a data structure that will capture the multiscale behavior during CMP process. A tree based multi-resolution adaptive mesh (data structure) is proposed. This data structure is much more physically based and powerful as compared to the pixel based data structure in existing models. The different levels of the tree correspond to different length scales at different kinds of physical phenomena during CMP.

6. Multi-scale CMP Optimization

The process-design optimization model of the previous section, once fully developed, could be utilized to fix CMP defects. As an example, suppose we want to decrease the within die non-uniformity (WIDNU) of nitride thinning during STI CMP (Figure 7, center). At present this is done primarily using dummy fill, but this usually has severe design restrictions. Using the multiscale model we can try to fix this at different levels (corresponding to the tree data structure). We can try to reduce WIDNU at level 1 (pad/wafer), by increasing the hardness of the polishing pad – this can be done by altering the pad structure and pad material. But this could have restrictions from pad suppliers or by scratch defect generation (harder pad usually cause more scratch defects).

We can also try to address this at the feature level by changing the incoming topography from the deposition process (but this would be restricted by deposition process limitations). At the abrasive level we can try to alter the fundamental material removal phenomena by changing the chemical reactions (slurry constituents) and the number and size of abrasive particles. The above provides a much more holistic and powerful approach to address defect issues during CMP.

The computational performance for such a model based on adaptive meshes also seems very promising. There is potential of 1000 time reduction in storage space requirements and a 100 fold reduction in processing times over existing pattern evolution models for same scale resolution (based on [8]). For device designers who need to analyze numerous design options, a fast robust CMP model will be very useful.

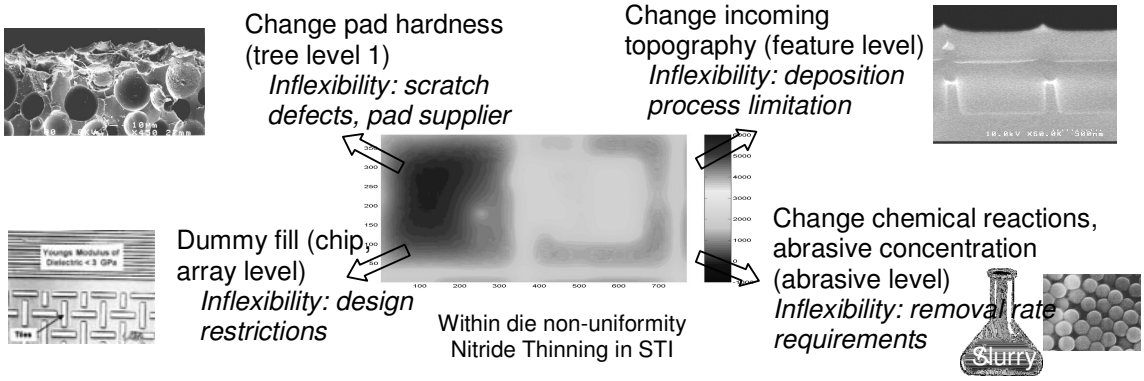

Figure 7. Multiscale Optimization Example: Address WIDNU (Within die non-uniformity) at different levels depending on available flexibility

7. Conclusion

Different concerns over the CMP process: pattern related defects, stress fracture of low-K materials, design-process optimization, understanding and developing new polishing processes – are being addressed using an integrated approach as illustrated in this paper. A better understanding of the mechanism of the CMP process and obtaining the related physical parameters is central to such an approach, but it needs to be supported by powerful and multi level software simulation tools so that it can be utilized optimally by device and process designers.

References

[1] International Technology Roadmap for Semiconductors : Interconnect, Modeling (2005, 2006 update)
[2] J. Choi, PhD Dissertation, UC Berkeley (2006)
[3] D. Boning et al., IEEE Trans. Semiconductor Manufacturing, 232 (2002)
[4] J.J. Vlassak, Journal of Mechanics and Physics of Solids, 847 (2004)
[5] J. Choi, D. Dornfeld, Proc. MRS Spring meeting (2004)
[6] J. Choi, S. Tripathi et al., Proc 11th CMP-MIC, 2006
[7] S. Tripathi et al., Manuscript under preparation (2007)
[8] T. Udeshi et al., J. Computing & Information Science (2004)