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UNIVERSITY OF CALIFORNIA SAN DIEGO

Design of an Accelerated and Inexpensive Testing Enclosure for Perovskite Solar Cells

A Thesis submitted in partial satisfaction of the requirements for the degree Master of Science

in

Mechanical Engineering

by

Andrew Zakoor

Committee in Charge:

Professor Renkun Chen, Chair Professor David Fenning, Co-Chair Professor John Hwang

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University of California San Diego

2022

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Oliver Wendel Holmes

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ABSTRACT OF THE THESIS

Design of an Accelerated and Inexpensive Testing Enclosure for Perovskite Solar Cells

by

Andrew Zakoor

Master of Science in Mechanical Engineering University of California San Diego, 2022 Professor Renkun Chen, Chair Professor David Fenning, Co-Chair

Perovskite photovoltaics hold promise to accelerate the world's transition to renewable energy by greatly reducing the cost of solar energy. While promising, perovskite commercialization is hindered by short cell lifetimes, and thus researchers use accelerated degradation testing to quickly engineer improvements. However, commercial test equipment is cost prohibitive, and many research groups instead design custom systems. This work presents the novel design of an accelerated and inexpensive testing enclosure for perovskites, and describes the engineering challenges of light, temperature, and electrical tests. Currently, the system is designed for a capacity of 45, 1 cm² cells, capable of illuminating at 7.2 times the sun's peak intensity, up to 85°C, with a leak rate of 0.3%/hr, and 4-point electrical connection to a custom maximum power-point (MPP) circuit. Total cost of the system is ~\$2.5k and is compact; cells can be transferred directly within a glovebox. This paper presents the thermal design, modeling, and challenges of high temperatures. We then present the structural and electrical design and conclude with a cost and failure analysis. The broader goal of this work is to contribute design guidelines for laboratories designing inexpensive, custom enclosures, in hopes of accelerating perovskites' commercialization.

Chapter 1

Introduction

1.1 Demand for Renewable Energy

As global temperatures rise from anthropogenic emissions, it is increasingly imperative to transition the world's electricity generation to renewable sources. Up to 40% of global emissions are from burning fossil fuels for electricity generation, which renewable energy is poised to replace ^[1-2]. However, the rate of change to renewable energy is not fast enough – at our current rate of progress, the world is on track for 2.9 degrees Celsius of warming ^[3-4]. Scientists warn at our current rate, this level of warming will multiply and intensify droughts, heat waves, and storms, cause sea-levels to rise from melting glaciers and have catastrophic effects around the world, from livelihoods to ecosystems. Estimated global costs are \$10-25 trillion reduction in GDP by 2050 ^[5-6], with the White House predicting \$2 trillion per year for the U.S. alone ^[7]. To keep warming below the "safe" 1.5 °C level ^[8], the transition to renewable energy must accelerate significantly. This will not only require governments internationally to enact sweeping regulation, but also for the cost of renewable energy to plummet further below fossil-fuel prices. While renewables have accomplished grid parity to fossil fuels in California, China, and parts of Europe, and although costs have decreased significantly over the last decades, they remain more

expensive in many countries ^[9]. Thus, reducing the cost of renewable energy presents a significant opportunity to reduce global emissions.

According to the International Energy Agency, a collaboration of 31 OECD countries that publishes data on climate change, renewables are the fastest growing energy source in the world ^[10]. Of this growth, solar energy represents 60% of renewable installations, and is the cheapest source of new electricity, for a "significant majority" of countries ^[10]. Solar constitutes 3.6% of world electricity generation and is the third largest fraction of renewable energy generation behind hydropower and wind ^[10]. However, despite this promising growth, the IEA's 2021 report still maintains that solar is "off-track", and displays the staggering gap between current solar implementation and the amount necessary to be on track for 1.5 °C, "net-zero emissions (NZE)" by 2030 ^[11].

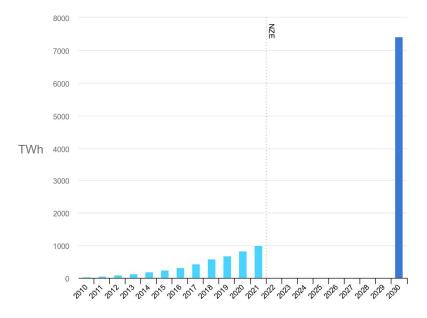


Figure 1.1: The IEA's 2021 report illustrates that 25% year-over-year growth is required for solar over the next decade to stay on track for 1.5 °C. This would increase solar installations 7.5x in 9 years. The current growth rate (2020-2021) is 22%, which implies if this rate of growth is held, the 2030 goal would be nearly met.

The annual growth rate in 2019 and 2020 was 22%, which is close to the required 25%. This implies growth percentage must be maintained and increased to meet the 2030 goals. Equivalently, capacity additions must continue to increase threefold, annually, until 2030 ^[11]. Notably, the cost of photovoltaics decreased by 82% from 2010-2020, largely due to efficiency improvements and increased economies of scale ^[11]. Scientists predict however, that for today's solar panels, further efficiency and scale improvements are nearing their limits. Thus, the photovoltaics of the future need to be fundamentally different – and cheaper – than those of today.

1.2 Potential of Perovskite Photovoltaics

The solar industry is currently dominated by monocrystalline silicon photovoltaics ^[11], which uses thin wafers of atomically repeating silicon atoms. Decades of research and development, as well as significant economies of scale, have created their relatively low cost, high efficiencies, and long lifetimes. Costs have decreased by orders of magnitude in previous decades, which brought solar panels to the mass market, and decreased costs 82% from 2010-2020 ^[11]. However, the National Renewable Energy Laboratory reports that silicon photovoltaic costs have finally begun to level-off ^[12].

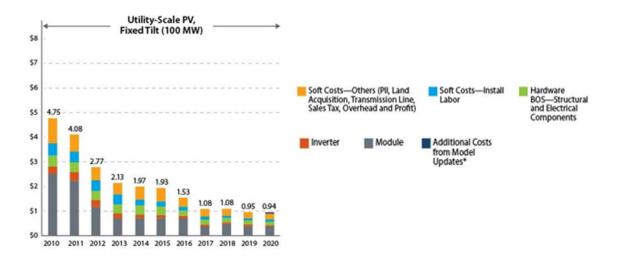


Figure 1.2: Illustration of the rapid decline and subsequent plateau in monocrystalline silicon photovoltaic prices. While prices have declined 82% from 2010 to 2020, prices have only declined 13% from 2017.

Reasons for this plateau include that the monocrystalline silicon is now engineered to near its theoretical efficiency, and the cost benefits from scale increasing further may be approaching their limit as solar expands its global markets. Therefore, to have a significant effect on reducing photovoltaic costs, many scientists and governments are now investing heavily in a novel, inexpensive class of photovoltaics: perovskites.

Perovskite photovoltaics are an emerging and exciting option for their potential to reduce solar costs. Perovskites are named for their crystal structure, which follows the form ABX₃, and can be made from many different atoms and compounds. Their efficiency is comparable with silicon, and was achieved in a fraction of the time. Perovskites' key to low costs resides in their much lower processing temperatures than silicon solar cells. Perovskites are solution-processed at temperatures of ~150 °C, which involves depositing and then evaporating a thin, liquid film. On the contrary, silicon wafers require purifying silicon-dioxide (often sand) at very high processes temperatures (up to 2000 °C) and slowly (expensively) extracting a monocrystalline ingot. Perovskites' low temperatures and relatively simple manufacturing drive its low cost.

However, while perovskites are of comparable efficiency to silicon, their lifetimes are much lower, which prevents their grid-scale deployment. Typically, silicon panels are warrantied for 25 years, while research perovskites often last for less than 1 year.

Perovskites degradation is accelerated by temperature, illumination, humidity, oxygen, and current output, among others ^[13]. To increase the lifetime of perovskites, it is essential to expose perovskites to these stressors and quantify their response, to understand degradation mechanisms, the role of specific stressors, and device performance over time. Additionally, the nature of perovskite's variable ABX₃ composition and sensitivity to processes parameters means that laboratories worldwide are iterating through thousands of perovskite prototypes. The plethora of samples, combined with global demand to quickly reduce renewable energy costs, requires accelerated testing. Thus, lifetime and accelerated degradation testing is needed to engineer longer-lasting perovskites.

1.3 Lack of Available Testing Systems

Despite this market need, to our knowledge there is no commercially available degradation test equipment for perovskite solar cells. Individual components (solar simulators, temperature controllers, gas-sealed enclosures) are expensive and often not integrable. Perovskite testing is still in early stages, unlike silicon photovoltaics, and testing apparatuses usually need to be customized for each laboratory due to unique device geometry. This is especially true since only recently have perovskites reached silicon cell efficiencies, and the push for lifetime testing increased ^[14]. Additionally, perovskite testing differs from silicon; tests use more and smaller cells, the environment must have a gas-seal, and the market share is much lower. As a result,

many labs resort to designing custom fixtures, or contracting engineers to design one ^[15-17]. As such, there is a clear need for inexpensive and accelerated perovskite degradation equipment.

1.4 Scope of Work – Enclosure Design

Thus, the goal of this work is to successfully design and document an inexpensive, accelerated testing enclosure for perovskite solar cells, capable of high-throughput, light, temperature, and electrical tests in a sealed environment – aptly named 'LiTE'. This work will explore the challenges of uniformly heating and illuminating 25 perovskite solar cells. It will also present a parametric thermal model for predicting heat transfer, and for designing thermal components. Additionally, the design will consider space constraint and sealing challenges, to be compact enough to be transferred into a glovebox. In summary, this work will detail the design, modeling, and testing of LiTE that is custom to the Solar Energy Innovation Lab's (SOLEIL) solar cells at UCSD. While the system is designed for 1 cm² cell substrates, to complement the lab's spin-coated, automated perovskite manufacturing, this work aims to provide a generalized framework for laboratories designing custom fixtures of varying cell sizes. The CAD design, available on GitHub, is parameterized in SolidWorks, such that upon inputting device geometry, the parts update automatically.

1.5 Design Requirements for ISOS Tests

To compare perovskite testing data across laboratories, test conditions must be consistent and accurate. Thus, a standardized set of procedures was developed by the International Summit on Organic Photovoltaic Stability (ISOS) ^[18] that is broadly accepted by the perovskite community. These tests aim to identify and isolate perovskite-specific stressors, namely light, temperature, and maximum power-point testing within a sealed environment. LiTE is designed to perform these tests. LiTE successfully meets the requirements for ISOS tests T1-3, L1&2, and LC-1&2. With further testing of the MPP circuit, LiTE is also expected to meet -V test standards. Specifically, the maximum ISOS requirements are:

Table 1.1: ISOS Testing Specifications^[18].

Stressor	Light	<u>Temperature</u>	Electrical	Environment
Value	1 sun (1000 W/m ²)	85 °C	MPP (Maximum Power Point)	Inert, e.g. N ₂

The maximum light intensity specified by the ISOS tests is 1-sun equivalent (1000 W/m^2), which is the total radiant power from the well-accepted standardized AM1.5G spectrum. This corresponds to a representative sample of solar radiation across the U.S. However, since accelerated degradation tests are achieved at multiples of 1-sun intensities, LiTE was designed to at least double the illumination intensity to 2-suns at room temperature.

Chapter 2

Design

2.1 Summary

LiTE is a thin aluminum enclosure retrofitted with light and thermal components. Within the aluminum halves, an array of 45, 1cm² perovskite solar cells rest on a glass sheet, illuminated by an array of high-power LEDs. The cells are contacted by an aluminum heat spreader and electrically conductive spring-loaded contacts. Both the LEDs and perovskites are cooled by heat sinks and fans, with thermal interfacing to facilitate heat transfer.

For simplicity and lower costs, a commercially available, aluminum "clamshell" enclosure is selected. Through a rubber gasket, the enclosure protects the sensitive perovskites by preventing moisture and oxygen ingress. The aluminum enclosure, assisted by stacked aluminum layers and thermal interface materials, conducts heat away from the cells and LEDs. Heat sinks and fans precisely maintain cell temperature by dissipating heat to the environment. Held in plane by an aluminum stencil, each cell is individually illuminated by a single highpower LED, whose light is columnized by a grid of aluminum reflectors. Spring-loaded pogo pins conduct current from each perovskite solar cell (PSC), which monitored and maximized by a custom-designed maximum power point (MPP) circuit.



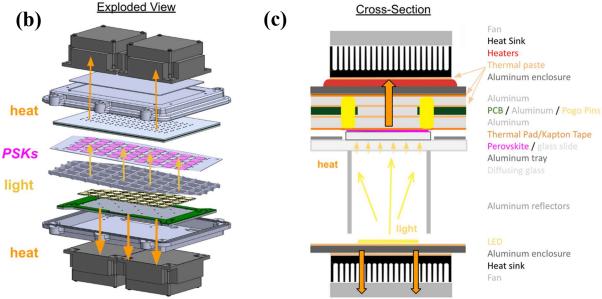


Figure 2.1: (a) LiTE complete assembly. The thin "clamshell" aluminum enclosure consists of two halves, sealing the cells and LEDs inside. Visible modifications to the halves, from left to right, include fastener holes, electrical connectors, mounted heat sinks, and two gas inlet valves – with space for two additional heat sinks. (b) Exploded view of the internals – LEDs, perovskites, and heat spreaders. (c) Detailed cross-section of heat transfer. Stacked layers of thin aluminum sheets and thermal interface material conduct heat from the cells and LEDs.

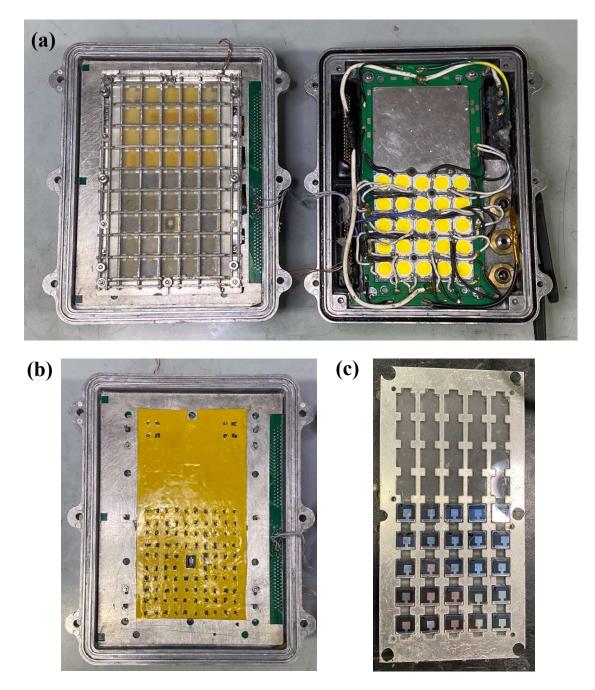


Figure 2.2: (a) LiTE's halves, the cell assembly on the left, and array of yellow LEDs on the right. (b) The cell half of LiTE with the tray assembly removed, revealing the yellow-taped thermal pad, with holes for a tightly-packed array of pogo pins. A small, silicon photodiode in the center continuously monitors light output. (c) Top-view of the tray assembly, in which 25 perovskite cells rest on a glass diffuser, within an aluminum stencil.

2.2 Thermal Design

For the cell's temperature to be precisely maintained while illuminated, heat must be transferred from the cells. This is chosen to be through conduction, to control temperature more precisely than is practical with radiative or convective cooling. For conductive heat transfer, the contacting heat spreader plate should be thin with high thermal conductivity, to increase temperature uniformity, decrease the system's heating time, and decrease cost. As a result, we selected thin, planar, aluminum sheets for heat transfer from the cells and LEDs. Aluminum has a high thermal conductivity, is easily machined, and is relatively cheap. Between each of the aluminum layers is a thermal interface material, of either silicone grease, non-silicone grease, or a non-silicone pad. Whenever possible, silicone grease is used, as it has the lowest thermal resistance of any available thermal interface material (TIM). However, silicone grease is prone to leaking silicone oil at extended use, and therefore for all components in contact with the cells, or where oil could leak, non-silicone TIMs are used. For repeatable cell-contact, a non-silicone pad is used with Kapton tape. This combination provides many favorable attributes, including compliance for ensuring thermal contact to all cells, non-stickiness for assembly, electrical insulation, chemical inertness, and high thermal conductivity.

2.2.1 Thermal Model

The thermal design of the enclosure presented the primary challenge of this work. The objective is to test solar cells at 85°C and 1-sun intensity, for 1000 hours. To design for this requirement, it is desirable to construct a model describing the system's heat transfer, allowing for predictions of thermal performance from design choices. A thermal resistance network was

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chosen for its simplicity, relative high accuracy for this system, and lack of transient complications.

A thermal resistance network, analogous to an electrical resistance network, follows the general equation: T = QR, (V = IR). To estimate the steady-state cell temperature from this model, the resistance values of all heat transfer elements must be known or tested for. These values are simple to calculate for uniform, planar sheets with known conductivities. For thermal interface materials, the resistances must be provided or experimentally measured, since it is dependent on air exposure, surface roughness, and applied pressure.

To further simplify the model, planar surfaces are assumed to be isothermal. This assumption is validated through the Biot number, which is a dimensionless quantity that compares the rate of internal conduction to external heat transfer. All aluminum sheets have a Biot number of less than 0.1, which allows a "thermally thin," isothermal assumption within 5% error ^[19]. Additional validation comes from comparing aluminum's vertical and horizontal resistances to the much higher thermal paste resistances – this also results in an isothermal assumption. Therefore, we can assume the temperature to be roughly isothermal within planes parallel to the cells, and the model dimensionality is reduced from 2D to 1D. This implies that conduction at each layer occurs near-uniformly over the planar area, and that each thermal resistance should use the full area value.

The thermal resistance network is straightforward to construct from each element of the design. Air and PCB parallel heat transfer through conduction are neglected due to high resistances. Upon calculating thermal resistances, it becomes clear that the impedance is dominated by the thermal interface materials and the heat sink's forced convection. However, at higher temperatures (>65 °C) radiation and natural convection play a larger role.

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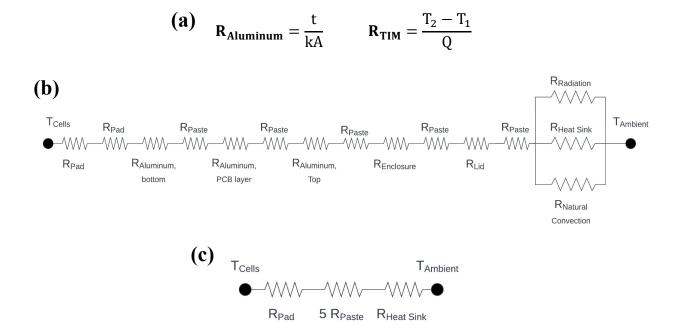


Figure 2.3: (a) Thermal resistances equations for thin sheets (left) and tested TIMs (right), in $^{\circ}$ C/W. For the non-silicone thermal paste and pad, the resistance was experimentally confirmed by placing the TIM material between two thin sheets of aluminum and measuring the temperature drop from a known heat source and heat sink. The temperature at each plate was measured with a thermocouple, and the thermal resistance is calculated as in R_{TIM} (left). (b) Complete and (c) simplified thermal model, where R_{pad} and R_{paste} refer to thermal pad and thermal pastes.

Each paste resistance varies slightly, as conductivity changes with composition (nonsilicone vs. silicone), and total contact area (e.g. PCB aluminum layer has ~1/3 contact area of other aluminum layers). Notably, at steady-state cell temperature, the net heat transfer of the cells must be zero. However, a range of heat fluxes and temperatures are desired, which requires a range of $R_{heat-sink}$ values. To find the maximum and minimum acceptable thermal resistance, consider the highest cell temperature with the lowest heat flux at natural convection, $R_{max} = 85/(1$ sun), and the lowest cell temperature with the highest heat flux at forced convection, $R_{min} = 65/(2$ suns). This thermal resistance range is designed for and accomplished by using a heat sink with a bang-bang controlled fan; the fan is turned on below a setpoint, and off above it. After summing the resistances of aluminum layers, thermal interface materials, and fan & heat sink, the steady state temperature is estimated as a function of the average light intensity incident on the sample active area. This corresponds to the system's minimum thermal resistance and maximum light intensity for a specified temperature. The model considers conductive, convective, and radiative heat transfer to estimate the cell temperature. Heat loss to the environment through natural convection and radiation is calculated as:

 $\mathbf{Q}_{radiation} = \epsilon \sigma A (T_s^4 - T_{env}^4)$

$$\mathbf{Q_{nat.\ conv.}} = \frac{\text{Nu} * \text{k}}{\text{L}}, \qquad \begin{cases} \text{Nu} = 0.54 \text{Ra}^{\frac{1}{4}}, 1e4 < \text{Ra} < 1e7\\ \text{Nu} = 0.15 \text{Ra}^{\frac{1}{3}}, 1e7 < \text{Ra} < 1e11 \end{cases}, \qquad \text{Ra} = \frac{\text{g}\beta(\text{T}_{\text{s}} - \text{T}_{\text{env}})\text{L}^{3}}{\nu^{2}} \text{Pr}^{\frac{1}{2}}$$

Where T_s is the lid surface temperature, σ is the Stefan-Boltzmann constant, ϵ is the emissivity of aluminum (0.1 for unpolished, 0.8 for anodized heat sink), $\beta = 1/T_{env}$, ν is the kinematic viscosity of air, and Pr is the Prandtl number.

The light output from the LED is estimated by converting input power to lumens, and using the supplier provided conversion from lumens to radiant watts. The model accounts for the effects of LED output as a function of temperature and current draw. Higher temperatures increase the equilibrium carrier concentration, thus increasing Auger recombination and decreasing LED efficiency. This reduced efficiency through Auger also occurs through increased current draw. As a result, radiative efficiency decreases from ~60% at 25 °C, 75 mA to ~50% at 85 °C at 250 mA. Total light absorbed by the cell assembly is estimated through an application of Snell's law for incident reflection.

$$\frac{I_{\rm R}}{I_0} = \alpha_{\rm light} \approx 1 - 4 \left(\frac{n_{\rm glass} - n_{\rm air}}{n_{\rm glass} + n_{\rm air}}\right)^2$$

Where $n_1 = 1$ for air, and $n_2 = 1.52$ for glass. This results in a 4% reflection for each glass-air interface, amounting to ~16% estimated total reflection, or $\alpha = 0.84$. The experimental values are the average temperature of the corner and center of the cell-planar surface.

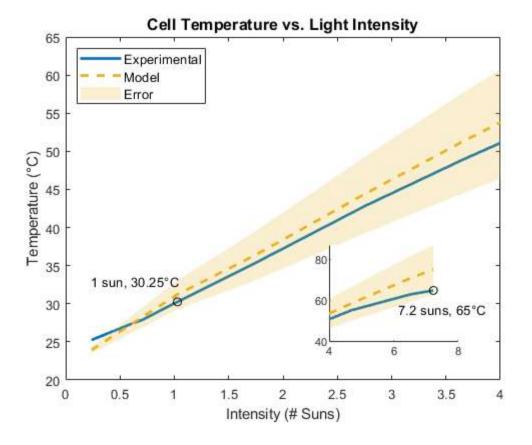


Figure 2.4: Thermal model overlay with experimental data for illumination intensity at cell level, showing high correlation. Inlay shows the characteristics at higher intensity, notably the decay in slope.

As shown, the model successfully and accurately predicts the measured temperatures up to ~6 suns and estimates at higher intensities are within a reasonable error bound of less than 10%. To gain further confidence in our estimation, compare the total thermal resistance of LiTE to that of a solar module cooled by natural convection. Data of installed module temperatures shows that for an insolation of 700 W/m², the average temperature is 44 °C, corresponding to a temperature rise of 22 °C (PV Education), and a thermal resistance of 31.4 °C*m²/W. For an

approximate comparison, by dividing LiTE's 0.60 °C/W resistance over its area gives an estimate of 3.2 °C*m²/W, almost an order of magnitude less than module natural convection. This demonstrates why LiTE's steady state temperature is much lower than solar modules.

The error bound of the model is +/- 21%, and accounts for the +/- 0.25 °C accuracy of the thermocouple, as well as temperature and manufacturing variations in each LED. Additionally, the top bound assumes full absorption after the glass diffuser, and the lower bound assumes perovskite absorption with otherwise full reflection. Beyond 4 suns, the error percentage between experiment and model begins to increase, shown by the experimental slope decaying faster than the model's slope. This discrepancy is accounted for in the error bound, however it might also be due to increased convective heat transfer coefficients at higher temperatures. The heat sinks' thermal resistance decays with temperature, data which is not provided in the heat sinks specifications. The neighboring airflow from the nearby fan may also increase the overall heat transfer coefficient by inducing turbulent flow over the flat plate. This effect may be amplified since the measurements were conducted within a fume hood, that induces a constant flow rate.

2.2.2 Silicon Photodiode Calibration

A silicon photodiode was used to calibrate LED voltage and spectrum to 1 sun of radiant flux. The photodiode's output current is linearly proportional to the input radiant watts, with varying sensitivity to different wavelengths. Using a spectrometer, the LED spectrum is obtained and then normalized to 1-sun intensity for the photodiode active area. Then, by multiplying the normalized spectrum to the photodiode spectral sensitivity and integrating over wavelengths, we can estimate the photodiode current output at 1 sun intensity. This can also be represented as:

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$$I_{1-sun} = \int_{400}^{700nm} C * P_{LED}(\lambda) * S_{Si}(\lambda), \qquad C = \int_{400}^{700nm} \frac{1000 \ \frac{W}{m^2}}{P_{LED}} A_{Si}$$

Where $P_{LED}(\lambda)$ is the output power of the LED in W/m²/nm, and $S_{Si}(\lambda)$ is the responsivity of the silicon photodiode in A/W. The output current from the photodiode is dropped across a 10 Ω resistor. This value is chosen to generate a voltage that is less than 10% of the open circuit voltage, to avoid non-linear current generation from the diode's IV curve.

2.2.3 Thermal Testing

When started from ambient, LiTE takes ~10 min to heat to 65 °C, and ~40 minutes to heat to 85 °C, which is the maximum temperature, primarily limited by natural convection of the heat sink. The temporal fluctuations around the 85 °C setpoint are +0.5/-1.0 °C. The cell-to-cell deviation at 1-sun and 65 °C is +/-1 °C, and the maximum deviation in cell-to-cell temperature is +/-3 °C, which occurs at 65 °C and 7.2 suns.

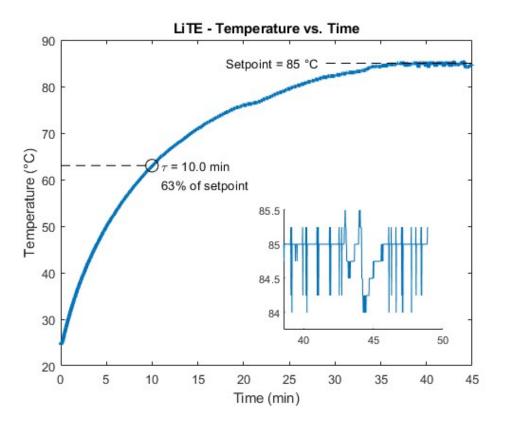


Figure 2.5: LiTE's warm-up time and temporal fluctuations. Heating to 63% of the 85 °C setpoint shows a time constant of 10.0 minutes.

2.2.4 Thermal Design Challenges

A thermal challenge occurs from both electrically and thermally contacting the cells, within a thin and compact package. While a printed circuit board (PCB) allows for electrical contact, its thermal resistance is high and impedes heat transfer – whether it is made from fiberglass, aluminum, or ceramic. Therefore, this work's design increases thermal conductivity by using interdigitated aluminum and PCB layers; aluminum fingers conduct heat away from the cell and PCB fingers make electrical contact at the cell corners. This unique arrangement enables a high cell packing-density, which also requires using a 2-layered PCB for the numerous electrical connections.

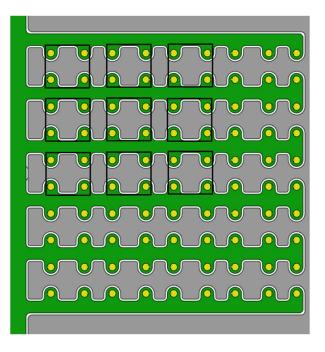


Figure 2.6: Interdigitated aluminum (gray) and PCB (green) layers, with four pogo pin (gold) connections in cell corners. A 3x3 grid of cells is outlined in black for reference. Heat is conducted out of the page, while current is conducted in plane of the PCB.

Additional challenges arose from the use of a thin glass diffuser, as it is prone to shattering at low stresses. The sample tray, containing the glass diffuser, is compressed against the thermal pad, to conduct heat away from the cells. Adequate compression of the thermal pad is specified as ~30%, which corresponds to 10 psi ^[20]. This load is transmitted through the tray assembly structure, which if not supported properly, will shatter the thin piece of diffusing glass. Thus, the aluminum reflectors implemented to increase illumination uniformity also serve to stiffen and support the glass diffuser on which the cells sit. The tray is compressed from six user-tightened thumb screws (shown in red) around the edges and is reacted against by the cells' compression into the thermal pad (shown in orange).

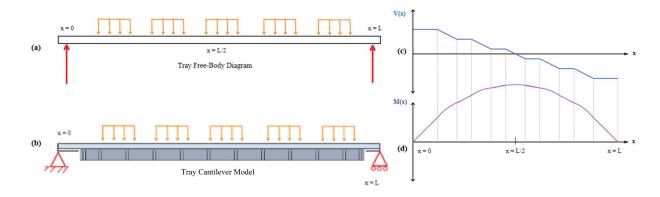


Figure 2.7: (a) Free-body diagram of the simplified tray, with fastener loadings at the end in red, and restoring distributed loads from five cells along the length. (b) Free-body diagram for approximating the tray as a lumped cantilever beam, with pivot and roller supports to replace the fastener loads. (c) Shear and (d) bending moment diagrams for the tray – bending stress peaks at L/2.

The stress within the tray assembly can be approximated by considering a lumped cantilever beam of the glass and aluminum reflectors. The thumb-screw fasteners are modeled as a pivot and roller support because they are assumed to apply a reaction force but not a moment. Additionally, each cell is assumed to provide an equal, distributed force over its area. Since the pad restoring force is proportional to compression, and since beam deflection is roughly half the pad compression ($\delta \propto L^3/EI_{beam} \approx 0.5 * (\delta \propto L/EA_{pad})$), the thermal pad reaction force is assumed constant. The remaining error in this assumption is absorbed into a safety factor of 2. Thus, from a desired pad compression of 0.1mm, and from the vertical forces and moments from the integration of shear, we can approximate the total maximum bending stress as 20 MPa.

$$\Sigma F_y = 0 \rightarrow 2F_{bolt} = 5q_{cell}L_{cell}, \qquad M(x) = \int_0^L V(x)dx, \qquad \sigma = \frac{My}{I} = \frac{M}{6bh^2}$$

Since the effective stiffness of the glass is $\sim 6x$ less than the aluminum reflectors, and because the beams resist deflection in parallel, the stress in the glass can be estimated from the parallel stiffnesses as 2.6 MPa.

$$K = \frac{48EI}{L^3}$$
, $\sigma_{glass} = \frac{K_{glass}}{K_{glass} + K_{alum}}$

The utilized 1.6mm diffusing glass from Edmund Optics^[27] has a fracture strength of 7 MPa, which results in a 2.7 factor of safety.

2.3 Sealing

Perovskites are sensitive to moisture (H_2O) and oxygen (O_2), and experience accelerated degradation when exposed to these stressors. Therefore, most perovskite devices are sealed, and thus to decouple the degradation from these stressors, the enclosure must also be sealed. A reusable, robust seal with a leak rate comparable to that of a glovebox is desired. Thus, an off-the-shelf sealed aluminum enclosure is selected that meets an IP68 rating.

In practice, the enclosure pressurized slightly above atmospheric pressure and is continually pumped with argon (or another inert gas). Both techniques aim to decrease the amount of moisture and oxygen entering the enclosure. Pressurizing the box should cause gas to leak out, instead of seeping in. The pressure is specified as 0.5 psi, which is a safety factor of 4 above the enclosure's maximum pressure. Additionally, the flow rate "cleans" the enclosure continuously, and is specified at a rate ten times greater than the leak rate – a choice to minimize contamination while reducing gas consumption.

The gasket's volumetric leak rate dV/dt can be estimated from differentiating the ideal gas law and measuring the depressurization rate. This assumes that the volume change from pressurizing the enclosure is negligible.

$$PV = nRT \quad \rightarrow \quad \frac{dP}{dt}V = \frac{dn}{dt}RT$$

From this equation, the rate of change of pressure relates to the rate of change of moles.

Additionally, by relating change in moles to change in volume, assuming the small change holds the pressure constant, and dividing by a differential time step, we obtain a second equation.

$$P\Delta V = \Delta n(RT) \rightarrow \frac{P\Delta V}{\Delta t} = \frac{\Delta n(RT)}{\Delta t}$$

We can now equate the two equations and rearrange to find the percentage volumetric leak rate (1/V*dV/dt).

$$P \frac{dV}{dt} = \frac{dP}{dt}V \quad \rightarrow \quad \frac{dV}{dt}\left(\frac{1}{V}\right) = \frac{dP}{dt}\left(\frac{1}{P}\right)$$

Thus, the rate of change of pressure is proportional to the volumetric leak rate. LiTE's leak rate is calculated as 0.3% volume per hour. For reference, a common ISO industry standard for gloveboxes is 0.05%/hr ^[21], and the larger leak rate is balanced by the much smaller volume.

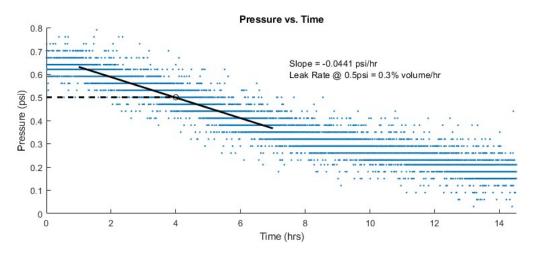
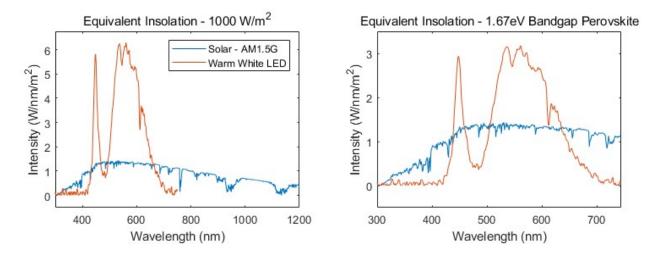


Figure 2.8: Decrease in pressure over time, where the extrapolated slope at 0.5 psi is proportional to the volumetric leak rate.

To maintain the seal, only fasteners and electrical connectors with O-rings or gaskets were used. Design attention was paid to the consolidation of connectors, fasteners, and valves, given the strict space constraints, as well as surface roughness and planarity. These, with the enclosure gasket, were applied with vacuum grease – an essential component for dramatically decreasing leak rate. The diameter of fasteners, and thus diffusion area for their O-rings, was minimized by performing stress calculations for axial (pressurization) and shear (thermal expansion) loading of fasteners and comparing the Von Mises stress to the bolt's yield strength.

2.4 Light Source

The ISOS protocols recognize that light sources vary widely in laboratories, and allow the use of many different types, so long as the irradiance is between 800-1000 W/m² and the spectrum is reported. There are several commonly used options in laboratories, including sulfur plasma, xenon arc, metal halide, and white LEDs ^[18]. In selecting the light source for this enclosure, a low-cost option is desired. Since the tests to be conducted are of extended duration, the light spectrum should also change minimally over time. Lastly, since the total area of the sample tray is quite large, the light source should be simple to tune for uniformity. As such, high power LEDs are selected because they are inexpensive and are easy to implement. In addition, LEDs are relatively simple to make uniform over a custom area, as their unit footprint is small. Also, crucial to extended duration tests is LEDs' lack of spectral drift, a common problem that hinders other light sources. For these reasons, LEDs are a popular choice for extended duration tests over large areas in laboratories ^[18]. An important factor to consider when selecting LEDs is the spectral match between their spectrum and that of the solar spectrum incident to terrestrial solar cells – on average, AM1.5G. Thus, warm white LEDs were chosen over cool or neutral



LEDs. Notably, the spectrum measured through the diffuser sheet is largely unchanged.

Figure 2.9: Comparison of LED and AM1.5G spectra. Tunability of LED intensity allows for equivalent irradiances for perovskites of varying bandgaps.

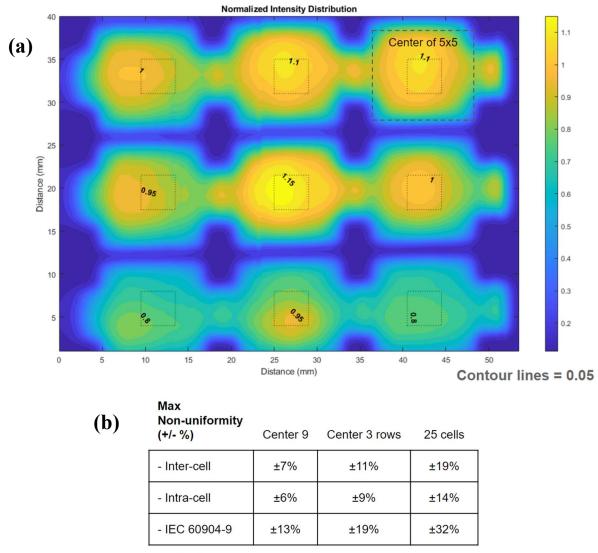
The above graph shows how the LED spectrum compares to the solar spectrum AM1.5G, for equivalent insolations of 1000 W/m² and for an example perovskite of 1.67eV bandgap for a tandem solar cell. These scenarios represent example tests for perovskites of varying bandgaps, while maintaining equivalent usable radiation.

Uniformity of the LEDs presented a significant challenge, both within the solar cell active area and from cell to cell. As such, one LED was chosen per cell – as opposed to a high-density grid of lower-power LEDs – for simplicity, high intensities, uniformity over the cell active area, and for future integration of constant current control. To increase uniformity, a sandblasted glass panel is placed between the LEDs and cells to diffuse the light. Sandblasted glass is chosen as an economic option that can withstand high temperatures (>85 °C). Additionally, a gridded array of aluminum strips acts as reflectors, columnizing the light. This increases uniformity both within each cell and between neighboring cells by reflecting light at the edges towards the center. The light uniformity is increased significantly from the glass

diffusing sheet and the reflector array – the reflectors increase spatial uniformity by 45%, and the diffuser increases uniformity by 25%.

The intensity of the LEDs is quantified by mounting the enclosure on an x-y stage and measuring the voltage output from a Thorlabs amplified silicon photodiode ^[22]. A step size of 0.5mm is chosen, and as such the aperture of the photodiode must be reduced to a 0.5mm diameter hole. This is quite simply accomplished by placing black aluminum foil with a 0.5mm hole over the photodiode. Data is taken over a corner subset of 9 cells of the total 25, due to the 4 lines of symmetry in the 5x5 array.

The illumination uniformity over the 25 cells is found to have an average of $\pm 9.6\%$ cellto-cell peak intensity, with a maximum of $\pm 19\%$. The intra-cell spatial non-uniformity, calculated as the maximum range of intensities, is on average $\pm 9.0\%$, maximum of $\pm 14.1\%$. Notably, the center-most cells are more uniform. The lower intensities in the edge column are likely due to leakage of light between the aluminum gridded columns – center cells will be brighter; edge cells will become rapidly less bright. Considering the center 3 columns (shown as the two right columns), average cell-to-cell non-uniformity drops to $\pm 7.5\%$ with a maximum of $\pm 11\%$, and average spatial non-uniformity drops to $\pm 5.9\%$ with a maximum of $\pm 9.0\%$. Cell-tocell variation is also amplified by the manufacturing variations in each LEDs, specified as a $\pm 6.0\%$ flux variation. For reference, the ASTM E927-10 and IEC 60904-9 standards for Class C uniformity of a solar simulator is $\pm 10.0\%$, and is calculated as $(I_{max} - I_{min}) / (I_{max} + I_{min})$.



IEC 60904-9 Class C: ±10%, Class B: ±5%, Class A: ±2%

Figure 2.10: (a) Contour plot with heat map of normalized intensity, measured with a rasterscanning photodiode at cell height. The top right cell corresponds to the center of the 25 cells. Contour lines represent normalized increments of 0.05, and the dotted boxes represent the perovskites' active areas. (b) Max non-uniformity, calculated from maximum & minimum values as well as ASTM E927-10/IEC 60904-9 standards, for increasing sections of cells. Additional data is provided in Appendix B.

2.5 Electronics

2.5.1 LED Driver

The 25 LEDs for this system are driven in parallel on a constant voltage power supply, with a 1 Ω current limiting resistor in series, calculated to have the optimal voltage drop for a given current draw and power supply. As LED current draw increases with temperature, the series resistor maintains constant current by decreasing LED voltage for higher currents and increasing voltage for lower. This configuration of 25 parallel LEDs is inexpensive and simple to implement – it requires only two voltage connections to the LEDs. However, it can shorten LED lifetime. By driving all LEDs at the same voltage, small manufacturing variations will cause some LEDs to draw more current than others. Over time, the increased current will heat the LED, which further decreases the forward voltage, and draws more current from the constant voltage supply. This feedback loop will cause some LEDs to become brighter than the rest, which might lead to burnout. Future iterations may consider individually current-controlled LEDs with series resistors. This will maximize LED lifetime and accurately maintain current draw, however with added expense and complexity.

2.5.2 MPP Circuit

A specification of the ISOS tests, and a commonly used test for solar cells, is the maximum power point (MPP) test. MPP tests find the solar cell's voltage which they produce the greatest output power, and then hold at this voltage. Installed solar modules use MPP trackers to maximize power output, since the optimal voltage changes with irradiance, temperature, and device age. Thus, MPP tests more accurately replicate the conditions of solar cells in the field.

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Commercially available controllers for MPP ^[23-24] are expensive, which is exacerbated by the large number of prototype perovskite cells to test. As such, this work presents the design of a 45-channel MPP tracker and tester, with Arduino's 10-bit, 4.9 mV resolution and up to 9 mA per channel. This circuit is an adaptation from the circuit designed by the Buonassisi Lab at MIT ^[25].

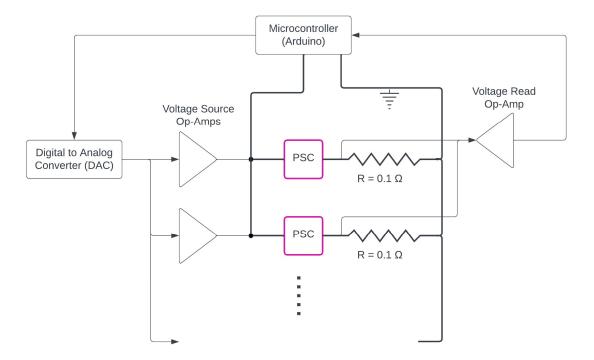


Figure 2.11: Simplified MPP circuit diagram, with perovskite solar cells (PSCs) outlined in pink. Current system has capacity for 45 cells, abbreviated by the vertical dotted line. Circuit for PSC current flow is bolded.

The most common method of finding the MPP is by using the "perturb-and-observe" (P&O) method, where the voltage (and thus power) is incrementally increased until the power output decreases. The P&O method is chosen due to simplicity and flexibility across devices. As such, each channel must source voltage (V) to the cell and measure the current (I) – thus, a source-meter unit (SMU). Voltage values for the cell are swept from 0V to V_{oc} to compute the full I-V curve. The voltage is applied by using an op-amp wired for unity gain, to prevent current draw from the solar cell circuit. The voltage is sourced from a digital to analog converter (DAC) that receives signal from a microcontroller – for this work, an Arduino. LiTE's electronics –

temperature control, sensor reading datalogging, and JV-scanning – are also controlled through Arduinos, chosen for their low-cost, simplicity, and widespread use.

To measure current, the solar cell is routed in series with a low $0.1\Omega + 1\%$ resistor, to minimize interference with current output. The voltage drop is amplified by a non-inverting summing amplifier circuit, with the maximum expected output calibrated to the Arduino's maximum input voltage. To reduce cost, a series of transistors toggles the measured device, so that one measurement circuit is used per 45 cells. At roughly 10s per scan, this is ~10-minute resolution for each cell. For our lab's cell active area of ~16mm² with an expected maximum current of 30 mA/cm², the expected maximum current is 4.8 mA – producing 0.48mV over the 0.1\Omega resistor. Since the Arduino's max voltage is 5V, this implies a necessary gain of 10,000. Thus, the resistor and voltage values are calculated from: $V_{Arduino} = V_{PSC}(\frac{R_1}{R_1+R_2})(1+\frac{R_4}{R_3})$ for a summing amplifier circuit ^[26].

Sourcing a voltage and measuring a current for each cell implies that 4 contact points are needed for accurate measurements. Otherwise, with 2 contact points, a voltage drop would occur due the voltage wires and contact resistances. The cells are contacted at the silver and ITO, the latter of which is reached by scratching excess perovskite to reveal the underlying ITO. This is to further reduce resistance for the current path. The current from each cell is sunk through the Arduino Megas, which limits the current output from each cell to ~9mA. Development is currently underway to integrate MPP tests into LiTE.

Chapter 3

User Experience

3.1 Cost Analysis

As a crucial goal of the project was to design an inexpensive set-up, particular attention was paid in economic decisions, without compromising quality or test specifications. This commonly resulted in consolidated manufacturing; all custom parts were manufactured with waterjet cutting, which is a simple, inexpensive, and scalable method. The quest for cost reduction also frequently resulted in designing custom systems. For example, the custom MPP circuit reduces cost both by nature and by designing specifically for our needs. The retrofitted, off-the-shelf aluminum enclosure is also less expensive than custom CNC-machining. Benefitting from this upfront development, LiTE now boasts an impressive ~\$2.5k price tag considering its capabilities. As such, one of the most exciting features of LiTE is how its low cost allows for scalability. Laboratories can build multiple enclosures to scale their testing capacity rapidly, compactly, and inexpensively. This usually requires an order of magnitude higher cost than is possible with LiTE. In practice, costs may vary depending on available parts or bulk quantities. Additionally, this estimate does not include a cost of labor.

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Table 3.1: Summary of LiTE costs. Hardware components are in subgroups: enclosure (aluminum, fasteners, valves), thermal (fans/heat sinks, TIMs, heaters), LED (power supplies, LEDs, diffuser, connectors).

Component	Cost		
Enclosure Hardware	\$700		
Thermal Hardware	\$200		
LED Hardware	\$500		
MPP Circuit	\$300		
Waterjet Cutting	\$150		
Tax & Shipping	\$300		
Misc.	\$300		
	Total = \$2450		

3.2 Usability

Since perovskites are manufactured in a glovebox or similar sealed environment, LiTE was designed compactly, to be brought into a glovebox for loading cells. This required both a high cell packing density, and a simple user experience within the glovebox's thick rubber arms and plexiglass cover. As a result, switching out cells takes ~10 minutes and requires no external tools. The enclosure halves and tray assembly are fastened with thumb screws. The wires to LiTE disconnect using sealed connectors, which facilitated this loading but presented space challenges.

3.3 Failure Modes

In LiTE development, several failure modes have been observed and designed around – primarily, part failure from excessive heat and assembly. Here we document our engineered solutions as a reference guide for others fixing common issues. Our current most common failure

mode is LED burn-out. Several challenges were overcome to ensure that all parts could handle

the high temperatures. Special attention and care must also be paid during assembly and

disassembly, as several parts are prone to bending, tearing, or shattering.

Table 3.2: Detailed failure modes, along with their causes and solutions – also common sources of error in experimental measurements. Failure modes are color coded for thermal (•), assembly (•), or electrical (•) problems.

Failure Mode	Cause	Solution		
 Warped and melted plastic 	High temperatures and	Use a glass diffuser, attached		
diffuser sheet	cantilever loading	to a stiff, tall, reflector array		
		$(I \propto h^3)$		
 Aluminum sheet buckling 	Constrained thermal	Add clearance in fastener and		
	expansion	aligning holes		
• Aluminum sheet bending and	Loading sheets as a	Load sheets axially – without		
creep	cantilever. High stress and	cantilever overhang		
	temp. causes creep			
 Reflector array bending and 	High stress from fasteners	Reduce fastener loading		
creep	and temp. causes creep			
 Higher than expected 	Aluminum sheet bending	Ensure planar aluminum		
temperatures		sheets, sand all surfaces.		
• Torn O-rings	Burrs from manufacturing	Sand all surfaces & edges		
	at surface edges			
 Tray stencil snapping 	Waterjet cutting of thin	Remove small features,		
	profiles	increase stencil thickness		
 Depressurization 	Loose sealing screws,	Loctite [®] the nuts		
	vibration from regular			
	handling			
• LED intensity off-center	Imprecise assembly,	Use aligning rods for stacked		
	tolerance stack-up	parts on both halves.		
 Wire solder connection 	High separating force over	Attach all cables, use larger		
failure	small area	diameter cables		
 Glass diffuser shattering 	Cutting small piece from	Take care with diamond		
	larger stock	cutting wheel		
 Gas-leaking electrical 	Polymer encapsulant	Use low-temperature solder		
connectors	separating from	and soldering iron		
	connectors when soldering			
• LED current increasing over	As LED temperature	Add a series resistor to voltage		
time	increases, the current for	supply. (or individual constant-		
	constant voltage increases	current LEDs)		
 LED burn-out 	Constant voltage power	Individual current-control		
	supply for all LEDs			

Chapter 4

Conclusion

This work presents the novel and successful design of an accelerated and inexpensive testing enclosure for perovskites photovoltaics. We demonstrate that LiTE can perform ISOS specified tests up to 85 °C and 7.2 suns illumination intensity, with 4-point electrical connection in a sealed environment. By constructing a model of LiTE's thermal resistances and heat transfer, we find close alignment with the observed performance. Additionally, the thermal model can enhance further thermal design efforts, such as increasing illumination intensity, temperature, cell area, or adding thermoelectric cooling. We show that the center nine cells of this prototype are uniform to +/- 10% within the cell area, and just shy of the IEC-60904-9 Class C non-uniformity. To improve uniformity, especially cell-to-cell, the height and reflectivity of the aluminum grid could be increased. As a more complex solution, constant-current control of each LED and a photodiode feedback-loop would virtually guarantee cell-to-cell uniformity. These compound capabilities come with an industry-low price tag of \sim \$2.5k, allowing the testing of prototype perovskites at scale. Upon additional tests, we also soon expect the validation and full integration of MPP testing. Lastly, we detail the challenges, failure modes, and trade-offs of designing a compact, inexpensive, and high-temperature system.

Further LiTE work could involve simplifying the stacked-layer design and assembly into a single CNC-machined aluminum enclosure, however with added expense. Development

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towards individual, current-controlled LEDs will also reduce operational cost from burnt-out chips. As capacity increases to 45-cells or to larger areas, cell-to-cell temperature and illumination uniformity should be monitored; these could be mitigated by improved reflectors and heat spreading. As perovskites emerge to proliferate renewable energy, this work hopes to help LiTE the way.

Appendix A

Electrical Connections

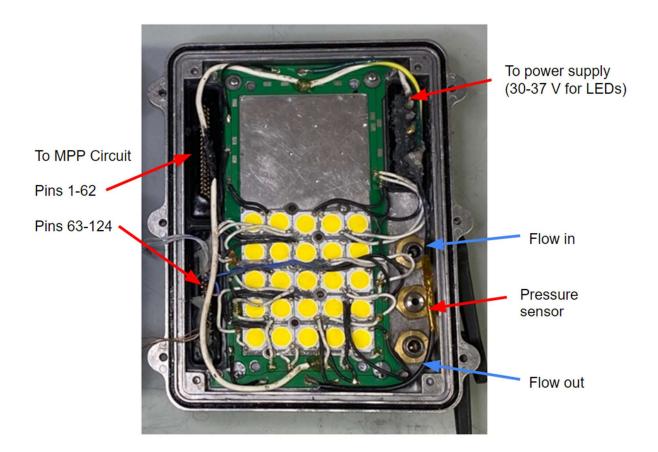
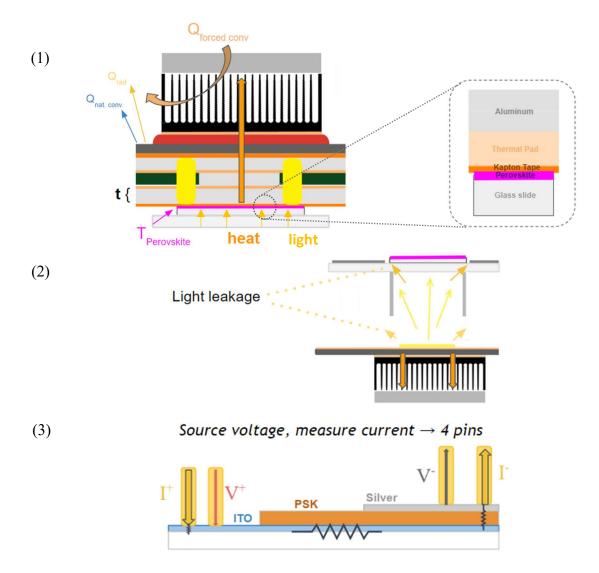


Figure A.1: Illustration of the bottom half's electrical connections, valves, and pressure sensor location. The valves were not pre-installed with O-rings, and thus are retrofitted with Teflon tape over the threads, and two O-rings – one at the nut and one at the value surface. Fasteners hold each part in place.

Appendix B

Additional Schematics



(4)	Cell-to-cell Normalized Intensity				W	ell	
				Ī	Spatial Non-Uniformity (+/- %)		
	0.69	0.93	<u>1</u>	Ī	7.6	5.9	5.6
	0.88	1.07	1.01	Ī	14.1	4.6	4.3
Γ	0.72	0.86	0.90	Ī	10.7	6.4	6.9

Figure B: (1) Diagram of how heat flows through LiTE, with a callout to show detail of thin layers at the cell level. (2) Diagram of locations for light leakage, posing opportunities for improvement. (3) Cross-section of perovskite cell and electrical contacts. Two pins at each contact supply voltage, two more act to source and sink current independently. (4) Additional data characterizing the variation in light uniformity; 3x3 table entries are mapped to 3x3 heat map.

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*** Supplemental files and documentation can be found at: <u>https://github.com/azakoor/LiTE---</u> <u>Solar-Testing-Enclosure</u>. Inquiries are welcome and encouraged through email at <u>azakoor@ucsd.edu</u>. ***