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High-speed avalanche photodiodes for low light level detection

By

CESAR BARTOLO-PEREZ
DISSERTATION

Submitted in partial satisfaction of the requirements for the degree of

DOCTOR OF PHILOSOPHY

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OFFICE OF GRADUATE STUDIES

of the

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DAVIS

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Committee in Charge

2022

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Abstract

Extremely sensitive optical receivers operating at high bandwidth are critical for optical communications technologies and other emerging applications that require the detection of an extremely low number of photons. Light imaging, detection and ranging (LIDAR), quantum communications, biophotonics, medical imaging systems, and other emerging applications will require a new generation of photodetectors that can detect extremely low power levels and be mass manufacturable. Today, Avalanche Photodetectors (APDs) and Single Photon Avalanche Photodetectors (SPADs) are the only detectors that can meet those requirements, but their bandwidth, sensitivity, and noise limitation must be overcome.

This thesis presents the development of new silicon and germanium-on-silicon-based APDs and SPADs with high speed and absorption efficiency at visible and near-infrared wavelengths. Through the modeling, fabrication, and characterization we show that the implementation of photonic nanostructures in photodetectors enhances their responsivity and gain by guiding the light parallel to its surface, greatly enhancing the interaction with the semiconductor material. These nanostructures also allow enhancing their time response by two methods: (i) use of thinner absorption layers to reduce the transit time of the photogenerated carriers, without sacrificing their absorption capabilities and (ii) reduction of junction capacitance by reducing the effective area of the device through the removal of material. This thesis also develops the concept of penetration depth engineering. We show that it is possible to guide photons to a critical depth in semiconductors and maximize the gain-bandwidth performance and absorption efficiency in avalanche-based photodetectors by integrating photon-trapping nanoholes. Our new Si APDs have shown superior amplification gain and speed compared to their conventional counterparts.

The advantages of photon-trapping are exploited in Germanium (Ge) on Si photodetectors. Our Ge-on-Si PDs show enhanced absorption capabilities at the O (original band: 1260-1360 nm) and C (conventional band: 1530 nm to 1565 nm) optical wavelengths of bands and enable their use at longer wavelengths in the L band (long wavelength: 1565 nm to 1625 nm). These PDs with photon-trapping holes have the potential to be monolithically integrated with CMOS/BiCMOS ASICs and offer a promising solution for waveguide PDs required for Photonic Integrated Circuits (PICs).

A new generation of APDS and SPADs are now designed with the implementation of appropriate doping profiles for high amplification, thin semiconductor layers for high speed, and the accurate design of micro/nanoholes for highly sensitive and ultrafast optical receivers.

Acknowledgments

I am thankful to many people and organizations for making this research project possible.

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Special thanks to the outstanding scientists at W&Wsens, Shih-Yuan Wang, Aly F. Elrefaie, Toshishige Yamada, and Ekaterina Ponizovskaya Devine for their support and their suggestions related to optical receivers, their applications, and challenges.

I am forever indebted to my family who always supported me to pursue my passion for research. Especial thanks to mother Lourdes and my sister Rosalia. Finally, I am deeply thankful to my partner in life Alma, and my son Santiago, who are my support and inspiration, this work is dedicated to you.

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Chapter 1

Introduction

In an era of the digital economy, the demand for data has grown exponentially, boosting innovations in its storage, transport, analysis, and use [1]. This insatiable demand has brought challenges concerning bandwidth and power consumption. The network infrastructure is now replacing the copper wire connections with optical interconnections in data centers and high-performance computers [2]. Following the path of the electronic industry, optical components are being developed and looking to be highly integrated to meet the current challenges at the lowest cost. One of the critical optical components is the photodetector, a semiconductor device that generates an amount of electrical current based on the properties of the input light, making it a crucial bridge between optical and electrical systems.

1.1 Motivation

Avalanche photodetectors (APDs) contain an internal gain enabling highly sensitive optical receivers. Silicon in a P-I-N configuration and APDs were used in the first generation of optical communication systems that operated in a wavelength range from 800 to 900 nm. Then, the optical systems were developed at transmission wavelengths of 1300 nm and 1550 nm for the lower dispersion and attenuation of these optical windows. The operation at these longer wavelengths motivated the development of

photodetectors based on III-V materials like InGaAs and, germanium-on-silicon (Ge-on-Si PDs) [3]. The desire to detect the smallest number of photons motivated to use of the avalanche effect in Single Photon Avalanche Photodetectors (SPADs), where a single photon can generate a self-sustained current in the PD that is biased above its breakdown voltage. Their capability to operate without cryogenic temperatures and integrate them with the current semiconductor fabrications processes made them attractive for a high deployment of these sensors [4]. Despite their different mechanism of operation, these devices share similar challenges to the APDs, in terms of sensitivity, speed, and noise. The multiplication of noise has limited the gain-bandwidth product on APDs, while the high dark count rate, low timing resolution, and detection efficiency in SPADs need to be addressed.

Nowadays, Silicon Photonics is motivating the development of waveguide integrated Ge-on-Si photodetectors and Si PDs. Silicon Photonics leverage the knowledge of Complementary Metal-Semiconductor (CMOS) processing techniques to integrate photonic components and systems with lower cost, high yield, and small footprint. Emerging applications enabled by silicon photonics such as Light Detection and Ranging (LIDAR), 3D imaging, biosensing, and quantum computing, are reviving the research efforts to develop a new generation of avalanche photodetectors with high bandwidth, low noise, and high sensitivity that can even reach the single-photon level.

LIDAR has been highly developed due to the interest to implement these systems in autonomous cars. Commonly, a 1550 nm wavelength is used in these systems, but high atmospheric transmission loss, environmental noise, and the restrictions on maximum

laser power that can be used cause only a small number of photons to reach the receiver [5]. Silicon APDs and SPADs have now been integrated into LIDAR systems for mobile devices. However, the low laser power required to meet the eye safety standards and the use of VCSELS at 905 nm and 1040 nm makes it critical to increase the sensitivity of the silicon receiver at those wavelengths. In life sciences applications, silicon APDS and SPADs are mostly used since they need to detect photons in the visible range. Applications such as Fluorescence Lifetime Imaging (FLIM) and Positron Emission Tomography (PET) imaging, from a general point of view, require the application of an external chemical in a biological sample to generate an emission of photons. The limited amount of chemicals that can be used to avoid toxicity makes it necessary to increase the sensitivity of the PDs and the speed for higher resolutions [6]. For Optical Communications, PDs with 265 GHz of bandwidth have been reported [7]. While the speed is enough in most current fiber optical communication systems, their responsivity needs to be improved to reduce the laser output power. In addition, Visible Light Communications have been developed but they suffer from the high losses and sources of noise from the environment[8]. The information age brings its challenges, especially insecure data transmission. Quantum communication is predicted to be the most secure technology for data transmission. Since tapping into the transmission line can destroy the quantum states of entangled photons, immediate detection of a tapped line will be possible in a quantum communication system (QCS) [9]. Single-photon detectors are the main component in the receiver of a QCS and SPADs are the only options available today that can operate without cryogenic temperatures, unlike superconducting detectors.

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As noticed, ultra-fast and sensitive detectors are needed to meet the requirements of emerging applications that require precise measurement of sub-nanosecond lifetimes of very weak optical signals in the visible and near-infrared wavelengths [9, 10]. Moreover, power consumption is a real issue for the development of the next-generation optical systems, making it necessary to reduce the output light power, thus requiring increasing the receiver sensitivity. Therefore, the goal of this thesis is to develop highly sensitive silicon and germanium-on-silicon avalanche-based photodetectors with high gain and bandwidth.

1.2 Contribution

The results of this thesis enable the development of APDs and SPADs based on Silicon and germanium-on-silicon with picosecond time response but at the same time with high detection efficiency at visible and near-infrared wavelengths. This work includes the design, fabrication, and characterization of the responsivity, gain, and time response of photodetectors with the implementation of photon-trapping structures that manipulate the interaction of light with the semiconductor material. We simulated the optical and electrical properties of PDs obtained by different photon-trapping structure designs. We also contributed to their implementation using CMOS compatible processes available in the nanofabrication facilities at UC Davis and UC Berkeley. The results obtained allowed us to develop a series of empirical equations for designing photon-trapping structures optimized for different wavelengths, avoiding the fabrication of a high number of designs.

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We show that the limiting factor of speed in PDs, transit time, and capacitance can be simultaneously addressed by photon-trapping structures. The increase in absorption allows for the design of devices with thinner layers of semiconductor without sacrificing its absorption capabilities and a reduction of the effective area on the surface of the device allows for a decrease in its capacitance.

This work also introduces the concept of penetration depth engineering for improvement in multiplication gain and bandwidth in APDs and SPADs. We developed a series of optical and electrical simulation methods to understand the regions where light is absorbed in a semiconductor for different nanostructure designs. The location of the photogenerated electron-hole pair in a semiconductor is a critical factor that determines the noise multiplication and limits the gain on avalanche PDs, and we showed that nanostructures can be exploited to control the probability of avalanche and carrier transport dynamics. The characterization of the gain on PDs with these novel nanostructures allows demonstrating that different expected penetration depths contribute to different gain values. All of them with better performance than conventional devices.

We used the knowledge acquired and have designed a new generation of photodetectors with appropriate doped layers and integrated photon-trapping structures, to enable increasing their multiplication gain and absorption efficiency for a wide range of wavelengths.

Finally, this work expands the applications of our PDs from optical communications to new areas such as biosciences and imaging. Along with our collaborator Dr. Simon Cherry from the Biomedical Engineering department at UCD, we are exploring the implementation of ultrafast SPADs in Positron Emission Tomography. The group is now also exploring new applications in Fluorescence Lifetime Imaging Microscopy (FLIM) and Spectrometry.

1.3 Dissertation Outline

The thesis is organized as follows: Chapter 1 presents the motivation and contributions of this work. Chapter 2 describes the current technologies and methods explored to achieve high photon sensitivity. Chapter 3 presents the implementation of photon-trapping structures on the surface of the device and the enhanced absorption achieved. Chapter 4 presents the absorption and gain in APDs enhancement by engineering the penetration depth of the incident wavelength. The speed of operation of our novel photodetectors is presented in Chapter 5. Based on the absorption and speed enhancement obtained, Chapter 6 presents the design and recent fabrication of optimized avalanche photodetectors. Extending the wavelength of operation, Chapter 7 presents the results obtained when the photon-trapping approach is implemented in germanium-on-silicon photodetectors. Finally, in Chapter 8 we present future opportunities for these new avalanche photodetectors, further developments, and new applications.

Chapter 2

Avalanche photodetectors

This chapter describes different detectors used to achieve extremely low light level detection, their advantages, and their challenges. Up to date, avalanche photodetectors are the only technology that can be highly integrated, reducing power consumption, cost, and footprint, but some limitations need to be overcome. We explore different methods to achieve higher sensitivity and speed and present the concept of photon-trapping, a nanophotonic approach used in this work to meet the current PD requirements.

2.1 Low light level detectors

Low light level detectors that reach the single-photon level can be sorted into three principal categories of devices: photomultiplier tubes (PMTs), superconducting devices, and semiconductor avalanche (APDs) and single-photon avalanche diodes (SPADs). Apart from these devices, there are also some recent technologies for single-photon detection, such as quantum-dot optically gated field-effect transistors and quantum dot resonant tunneling diodes. A more detailed description of these detectors can be found in [9-11].

2.1.1 Photomultipliers

Photomultiplier tubes are operated in high-vacuum tubes with high voltages between anodes and photocathodes. A primary electron is produced in the photocathode material when it absorbs light due to the photoelectric effect. The electrons generated are subsequently accelerated with a voltage in the order of 100V to an intermediate electrode (dynode) and generating secondary electrons. This multiplication process can be repeated toward further dynodes amplifying the photocurrent. Such mechanism makes photomultipliers highly sensitive photodetectors with gain, fast response, and low noise. However the high voltage required for its operation and high footprint limits the application of these devices to highly specialized areas [12].

2.1.2 Superconducting nanowires

Superconducting SPDs include superconducting nanowire single-photon detectors (SNSPD) and superconducting transition-edge sensors and tunnel junctions [11]. In the SNSPD, a hotspot is created after the absorption of a single photon in superconducting nanowires, and subsequently, the superconducting current density increases due to the size expansion of the hotspot. The high voltages of operation are required, and the big dimensions of PMTs limit their applications to laboratories, while the cryogenic operating conditions required for SNSPDs do not allow them to be practical devices yet.

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2.1.3 Avalanche photodetectors (APDs)

Currently, the mainstream solution for low light level detection in practical applications is the use of APDs and SPADs. APDs are high-sensitivity photodetectors that have an internal gain mechanism created by the impact ionization of their carriers. This mechanism provides higher signal-to-noise ratios and higher receiver sensitivities. The gain depends on the internal electric field and hence on the reverse voltage applied. Generally, their output photocurrent is linearly proportional to the input optical power when operated below their breakdown voltage. These characteristics made them attractive for optical communications, imaging, and, more recently, single-photon avalanche photodetectors (SPADs).

2.1.4 Single photon avalanche photodetectors (SPADs)

The SPAD is designed based on an avalanche photodiode structure. The diode is reverse biased above the breakdown voltage, and this is known as Geiger mode operation [13]. The carriers generated by photon absorption undergo avalanche gain, triggering a macroscopic breakdown of the diode junction (Fig. 2.1a). The avalanche process must be stopped, and the device is reset by a quenching circuit to detect another incoming photon (Fig. 2.1b). During the time it takes to quench the avalanche, the diode is not able to detect another incoming photon, and this is known as dead time. Therefore, the performance of a single-photon detection system depends both on the SPAD device itself and the quenching electronics. These silicon based APDs and SPADs have the advantage of facilitating the fabrication of arrays along with an integrated quenching

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circuit that reads each device in parallel (Fig. 2.1c). These devices are known as Silicon Photomultipliers (SiPMs) and are the only single-photon detectors that have been highly integrated using the current CMOS technologies processes. All these characteristics made these devices the current solutions for low light level photon detection required in many emerging applications.
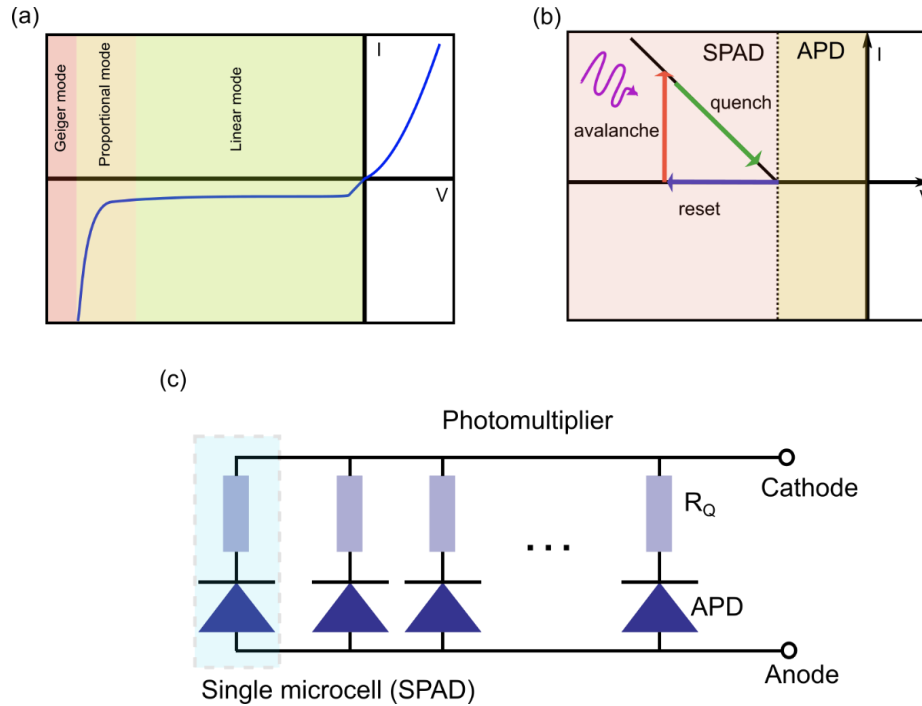
Fig. 2.1. (a) Current-Voltage characteristics of an SPAD. A PN Diode is operated in Geiger mode. (b) Description of the quenching process. (c) An array of SPADs in parallel creates a Silicon Photomultiplier (SiPM).
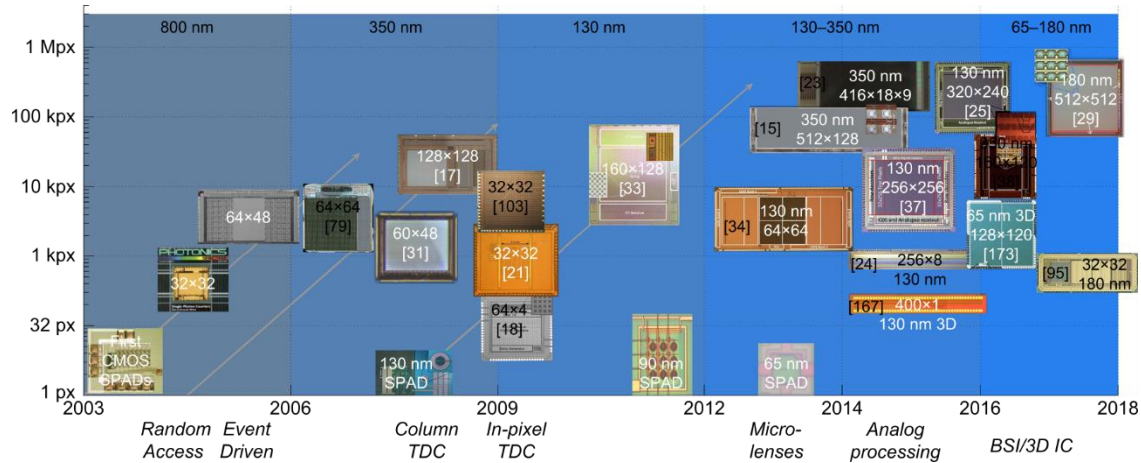
Fig. 2.2. Overview of the evolution of SPAD imagers [6]. These are the only single-photon detectors that have been highly integrated with the required post signal processing. In the recent years, intense efforts have been directed to create Backside Illuminated devices to increase the fill factor of the devices, increasing the amount of light captured and improving its low light performance and 3D IC integration to reduce power consumption, time of response, and footprint.

2.2 Challenges for silicon-based low light level detectors

2.2.1 Absorption efficiency of silicon

The absorption coefficient (α) of a material determines how far light can penetrates a material before it is absorbed (Fig. 2.3). Low values mean that light is poorly absorbed. This coefficient is dependable on the incident wavelength of light. For the case of silicon, the α values above the 800nm of wavelength (<1.54eV) decrease sharply since the energy at these wavelengths is close to the energy bandgap of the material (1.1eV). For example, for short wavelengths, such as 450nm, $\alpha_{Si}=25500$ cm^{-1}, which suggest that

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silicon thickness of 392nm is enough to absorb the incident light. For a velocity saturation (V_{sat}) of silicon ~1×10^7 cm/s, it takes 3.92ps for a carrier of silicon to travel across that distance. However, at a telecommunication wavelength of 850nm, α_{Si} = 535 cm^{-1}, making it necessary to have ~18.7 µm of silicon thickness to absorb the light efficiently. Such thickness increases the transit time of the photogenerated carriers to 188ps. Such an increase has limited the application of silicon APDs in NIR wavelengths.
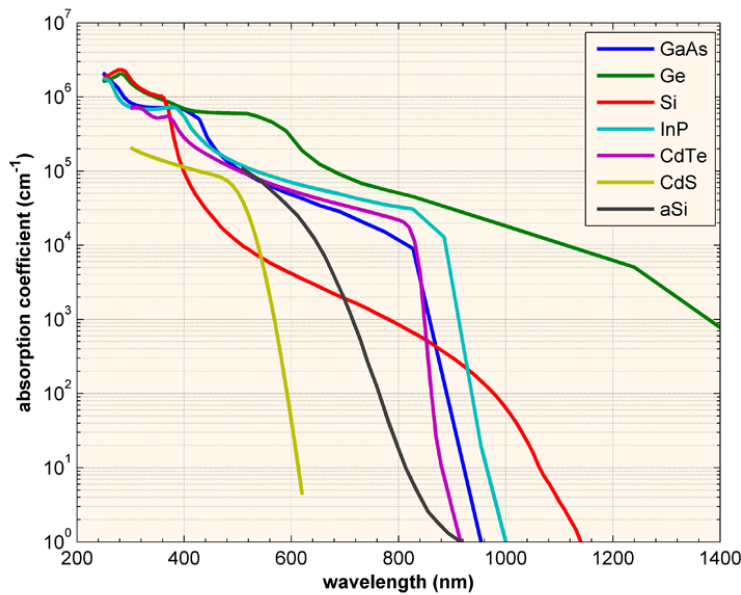
Fig. 2.3. Absorption coefficient (α) of different semiconductor materials. Silicon has a sharp decay in α at wavelengths close to its bandgap of 1.1eV, making it ineffective for NIR wavelength applications [14].

2.2.2 Gain-bandwidth product limitation in APDs

High sensitivity optical receivers can be achieved by using avalanche photodetectors (APDs). This type of photodetector uses internal gain. The APDs need optimization in two phases. First, the APD should maximize the absorption of light and its conversion to an

electrical signal. Then, the electrical signals should be amplified through the avalanche process. However, the avalanche multiplication process that generates the internal gain, limits the speed performance of the APDs due to the avalanche buildup time. Such tradeoff is known as the Gain-Bandwidth Product (GBP) and is related to the ratio of electron and hole coefficients. The development of photodetectors has been divided into those with high responsivity but low bandwidth and vice versa. Since the gain scales linearly with responsivity, this tradeoff is related to the GBP. The current GBP in the upper left and bottom right quadrants of Fig. 2.4a correspond to a GBP of ~106-109 Hz-A/W. The research efforts focus on moving to the top right quadrant of the plot, where high responsivity and bandwidth can be obtained in APDs. Fig. 2.4b shows a Ge on Silicon APD with a GBP of 340GHz, where the maximum bandwidth is 11.5GHz when the gain is 20. Then, the bandwidth dropped, as the gain increased.
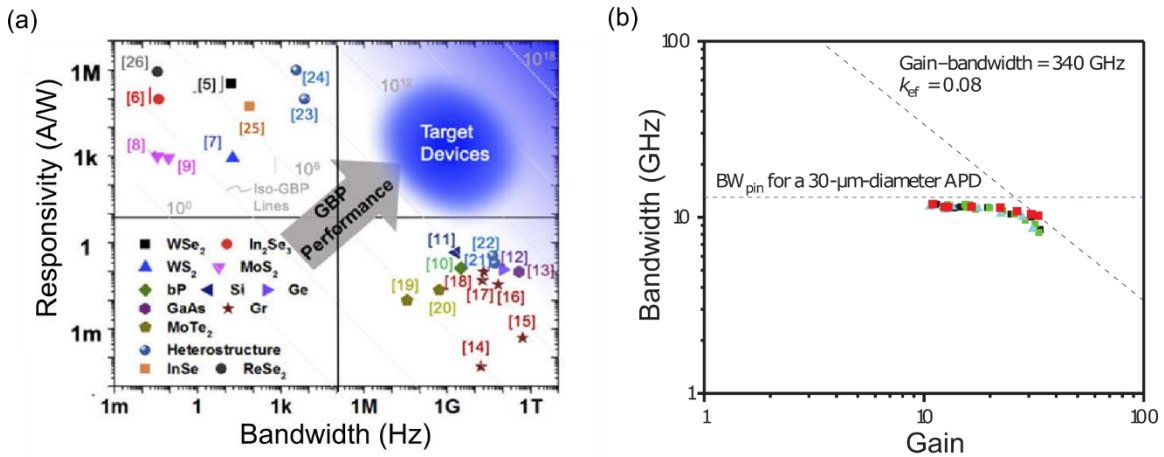
Fig. 2.4. Gain-Bandwidth product in APDs.(a) Current APDs can achieve high gain or high responsivity. New materials and approaches are been explored to achieve higher GBP and meet the target performances [15]. (b) Gain-Bandwidth Product in a Ge on Si APDs. This example shows how the bandwidth decreases as the gain is increased in the device [16].

2.2.3 Photon detection efficiency and photon timing resolution in avalanche-based photodetectors

Currently, the highest efficiency commercial SPADs are based on thick, 180 µm diameter detectors with active quenching circuits and a cooling system. These devices offer single-photon sensitivity in the 400–1000 nm range and achieve a peak efficiency of 65% at ~650 nm wavelength. The high EQE is achieved at the expense of time response which is in the range of 350ps FWHM. The other approach is the implementation of shallow-junction planar devices with a diameter of 50 µm and operating at low voltages. The timing is greatly improved to below 40 ps FWHM, but the peak detection efficiency is reduced to 49% at 550 nm wavelength (Fig. 2.5). At longer wavelengths, the efficiency gets further reduced in a photodiode designed to exhibit a fast response time. Such a trade-off is due to the poor detection efficiency as the input wavelength reaches the cutoff wavelength of silicon at 1100 nm, where the absorption coefficient (α) drops dramatically because of the indirect bandgap of the material.

SPADs can be fabricated using CMOS technologies with thin-planar layers that can provide high resolution in photon timing which is dominated by the transit time of the carriers from the absorption region to the multiplication region. However, high photon timing resolution with thin layers comes at the expense of low photon detection efficiency (PDE), especially for longer wavelengths. Silicon SPADs are an active area of development and efforts are underway to increase the PDE without sacrificing timing resolution and the integration of detector elements directly with quenching circuitry.

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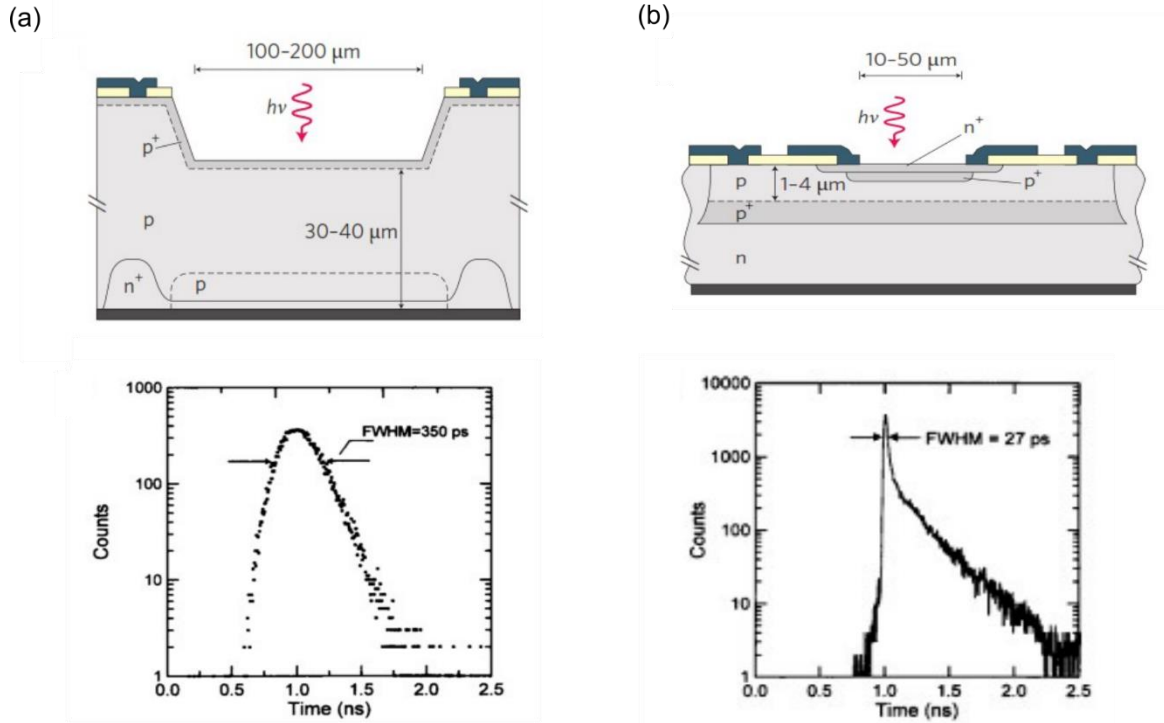
Fig. 2.5.Current SPAD characteristics and limitations in speed and absorption efficiency.(a) A thick silicon SPAD that offer high-efficiency used in low light level detection at the expense of speed. (b) A thin layer-based SPAD used in high speed operations that suffers from low detection efficiency [9].

To extend the performance of SPADs to telecommunications wavelengths of 1310 nm and 1550 nm, it is necessary to use lower bandgap semiconductor materials such as Ge and InGaAs. The best results have been achieved with an InGaAs absorption region and an InP multiplication layer, giving single-photon sensitivities from 1000 nm to 1600 nm wavelength range and peak efficiencies of ~20% at 1550 nm [17], but their lack of compatibility with silicon fabrication processes have motivated the development of Ge-on-Si SPADs. Ge-on-Si SPADs have been demonstrated for single-photon operations at 1310 and 1550 nm with a 4% and 0.15% single-PDE [18]. Despite their 4% lattice

mismatch with respect to silicon and their high amplification noise, these detectors are highly attractive for their potential integration with photonic integrated circuits (PICs). The planar Ge-on-Si PDs have shown 38% of PDE at 1310 nm with a lower after-pulse compared with InGaAs/InP devices [19].

2.3 Photon-trapping theory and opportunities in PDs

Different methods have been explored to increase the interaction of light with the semiconductor material in photodetectors including plasmonic, resonant cavities, and the implementation of nanostructures.

Plasmonics: An incident light propagates through a plasmonic nanostructure such as gold nanoparticles, at a specific wavelength. The free electrons generated oscillates collectively on the surface of the plasmonic antennas enhancing the interaction with metallic nanostructures and therefore resulting in the enhancement of the electric field around the plasmonic nanostructures [20-22].

Resonant Cavities: In a Resonant Cavity Enhanced (RCE) Photodetector a thin absorbing layer is placed inside a Fabry–Perot cavity where the feedback mirrors are usually comprised of quarter wavelength stacks with a periodic modulation of the refractive index. At resonance, construction interference is built up within the cavity to enhance the internal optical field intensity [23]. In addition to their fabrication complexity, their design at a specific wavelength made them challenging for broadband applications.

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Micro/Nanostructures: The implementation of micro/nanostructures to increase the interaction between light and the semiconductor material can address the trade-off between speed (bandwidth) and efficiency [24-29]. The low-dimensional structures can control light for further interaction with the absorbing materials, excite the lateral propagation mode, and reduce surface reflection. Different structures have been explored, such as nanowires, nanorods, and nanoholes. The last approach is attractive given its low modification of the current PD fabrication and its possibility to integrate them into CMOS processes. Such nanoholes are based on the principle of photon-trapping.

The theory of light trapping was initially developed for solar cells [30]. From a ray optics perspective, light trapping exploits the effect of total internal reflection between the semiconductor material and the surrounding medium. Under a ray optics approach, when roughening the semiconductor-air interface, the light propagation direction gets randomized inside the material. The effect of total internal reflection results in a longer propagation distance inside the material and hence a substantial absorption enhancement [30].
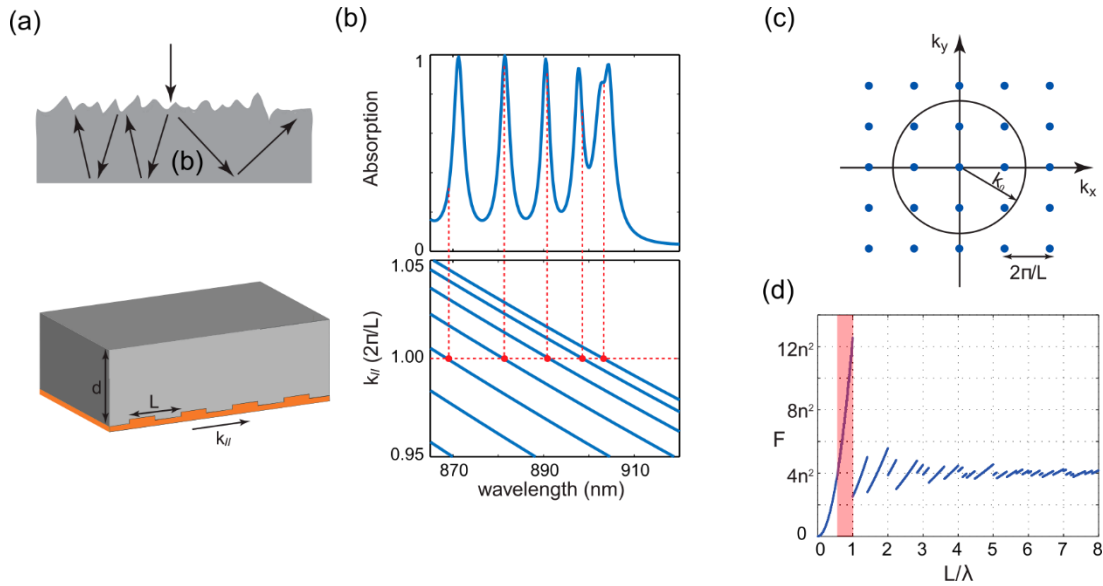
Fig. 2.6. Light trapping through the coupling of light modes.(a) random roughening or a grating structure with L/λ in a structure with a high index material and a high reflective material, (b) resonances presented in structure, (c) resonance coupling to channels equally spaced, and (d) resonance mode coupled onto the guiding mode [14].

Considering a high-index material (in our case, silicon with n_{Si} = 3.5), a high reflectivity mirror at the bottom such as SiO_2 (n_{SiO2} = 1.45), and air (n_{air}~1) at the top, such film supports guided optical modes. In the limit where the absorption of the active layer is weak, these guided modes typically have a propagation distance along with the film that is much longer than the thickness of the film. Light trapping is accomplished by coupling the incident planer waves into these guided modes with a grating structure with periodicity L that is comparable to the free space wavelength of the incident light (Fig. 2.6).

The absorption spectrum consists of multiple peaks, each corresponding to a guided resonance. Each resonance in the frequency range can couple to channels that are equally spaced by 2π/L in the parallel wave vector $|K_{II}|$. To maximize the absorption, one

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should choose the periodicity to be slightly smaller than the wavelength range of interest (L/λ) (red region in Figure 2.1d). This light trapping effect is exploited in thin-film layers of silicon and Ge on Si, to increase their absorption in the near-infrared wavelength range, ensuring high efficiency and speed of operation [30].

2.3.1 Enhancement of light-matter interaction in photodetectors

The idea of photon-trapping theory and its implementation in silicon was first motivated by the increase of efficiency in solar cells. In this work, we use the same principle for photodetectors. Increasing the absorption efficiency of PDs will allow designing devices with thinner absorbing layers, which would improve their speed of operation.

Fig. 2.7a shows the top and cross-sectional view of 850 nm-wavelength light propagation in silicon for 46 picoseconds. It can be observed that modes of light will propagate in the lateral direction, increasing the interaction of light with the semiconductor, instead of simply passing through the silicon layer. In other words, we can obtain the same absorption in a thin layer of silicon as a thick layer will have without any photon-trapping structure (Fig. 2.7b). The advantage will be a shorter transit time for the carriers generated in the detector.

(a)

Normalized electric field (λ=850nm)

Top view

Cross-sectional view

(b)

$$I_{abs} = (1 - R) \times (1 - e^{-\alpha d})$$

$\updownarrow h$

$d > \dfrac{1}{\alpha_{bulk}}$

$\alpha_{effective} \gg \alpha_{bulk}$

$t_{transit} = h/v_{saturation}$

$h \ll d$

Thin device with light bending holes

Thick device
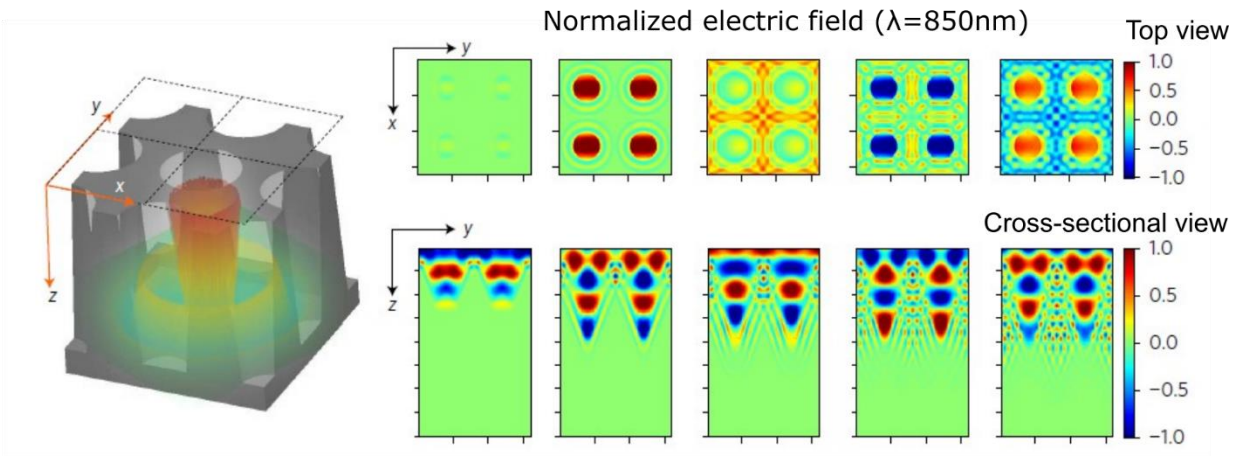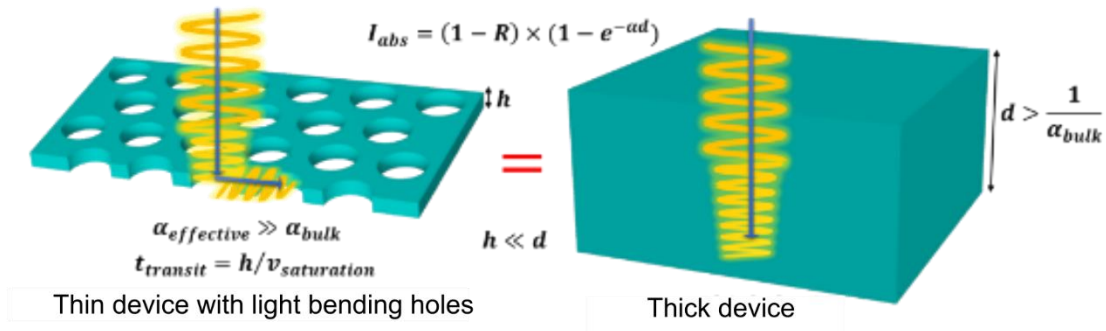
Fig. 2.7. Light bending by photon-trapping structures and benefits.(a) Pointing vector propagation of 850 nm input light in silicon shows the lateral propagation of the optical modes in a direction parallel to the surface, increasing the interaction of light with the semiconductor. (b) Representation of light bending in silicon with photon-trapping structures. The higher interaction of light in a thin material allows obtaining the same absorption efficiency as in a thicker material. Thus, the transit time is reduced without degrading absorption.

2.3.2 Photon-trapping in avalanche-based photodetectors

The gain in APDs originates from impact ionization, a stochastic process that results in excess noise relative to shot noise, and therefore limits the gain-bandwidth [31].

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Different methods have been explored to achieve low noise and gain-bandwidth, such as selecting a semiconductor with favorable impact ionization coefficients, scaling down the multiplication region to exploit the impact ionization of carriers that become less dependent on the local electric field [32, 33], or impact ionization engineering using appropriately designed heterojunctions [31, 34, 35]. In an APD structure with an N-on-P doping profile, with the multiplication region close to the surface, the avalanche multiplication will be mainly triggered by the holes when short wavelengths illuminate the device since most of the photons will be absorbed close to the surface. As the ionization coefficient for holes is smaller than that for electrons, the total current gain will be lower for short-wavelength than that for longer wavelengths. Thus, two variants of APD devices are commonly fabricated, N-on-P for greater gain and sensitivity at longer wavelengths (enhanced red-NIR sensitivity) [36], and P-on-N for shorter wavelengths (enhanced UV/blue sensitivity) [37]. In silicon, longer wavelengths penetrate deeper into the structure and require the use of longer absorbing layers at the expense of a reduction in bandwidth [36]. One of the key material properties that determine the gain-bandwidth product and the excess noise of APDs is the effective k ratio of the ionization coefficient of electrons versus holes. Low k values are desirable for high-performance APDs [16], making silicon an attractive material for APDs due to its low k value (<0.1) that results in a low excess-noise factor, F. Another key parameter impacting the gain is penetration depth. A penetration depth is a measure of how deep the electromagnetic wave penetrates the material. It is defined as the depth at which the intensity of radiation inside the material

falls to 1/e (37%) of its value at the surface. This parameter plays a critical role in APDs by making the gain a function of the incident wavelength [38].

Avalanche photodetectors are complex devices that require a low multiplication of noise while increasing their GBP. We propose a method to engineer the gain and bandwidth of avalanche photodetectors by controlling the penetration depth of light in the semiconductor with the implementation of photon-trapping nanoholes. We hypothesize that it is possible to control the penetration depth of light into silicon APDs and promote the initialization of impact ionization by electrons leading to a lower multiplication noise, and a higher gain-bandwidth desired in avalanche-based photodetectors (Fig. 2.8a-b).
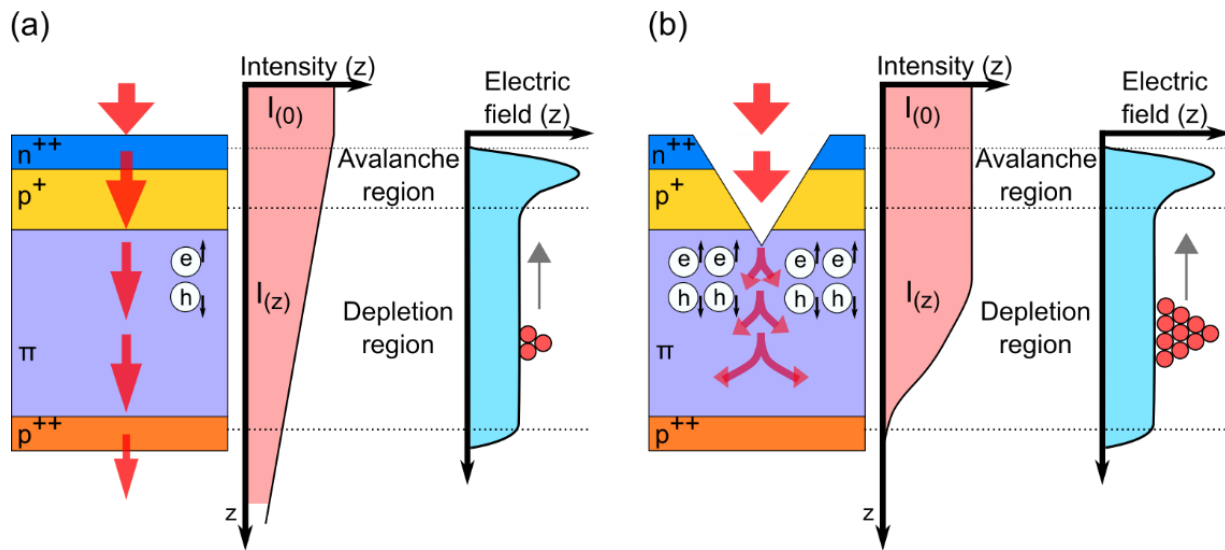
Fig. 2.8. Representation of the absorption and electric field profiles of two APD configurations. (a) Conventional APD (Control), and (b) Photon-trapping APD (PT APD). The light can be delivered to the absorbing region of the APD for efficient carrier separation and multiplication.

2.4 Summary

This chapter has presented different technologies and devices used to detect extremely low optical power. APDs and SPAD and the only devices that can be highly integrated using the current CMOS technologies and processes, but the gain-bandwidth of these devices should be improved. We explored different methods to achieve higher interaction between the semiconductor and the light. The concept of photon-trapping, which was first used to increase the efficiency in solar cells, is now applied in photodetectors to increase their sensitivity, speed, and reduction of noise. We hypothesize that these photon-trapping structures can promote the guiding of light in specific regions of the semiconductor, impacting the gain and the dynamics of the electrical carriers.

Chapter 3

Photon-trapping structures for absorption enhancement in photodetectors

Conventional silicon photodetectors (PDs) have weak absorption capabilities at near IR (NIR) wavelengths, forcing them to be designed with thick absorbing layers to obtain high efficiency at the expense of a limited speed of operation. Hence, the tradeoff between speed and efficiency limits the use of Si-based PDs. In this chapter, it is shown that by introducing PT structures on the surface of Silicon, the reflection of light is reduced, and the optical path length is increased, enhancing the photon absorption.

3.1 Device design

The silicon detectors consist of N-doped/Intrinsic/P-doped (NIP) or (PIN) doping layers, epitaxially grown on top of a silicon-on-insulator (SOI) wafer or bulk wafer and with a mesa-type structure. The profile design of the photodiodes consists of highly doped n^{++} and p^{++} layers with 0.25 μm thickness that serves as contact layers and a 2 μm-thick i-layer is used as the absorber region. This thin layer minimizes the transit time for the generated electron and holes. An introduction of a nanohole array on the surface of the PD serves to provide the photon-trapping effect (Fig. 3.1a) while a device with no holes serves as our control or conventional device for comparison (Fig. 3.1b).
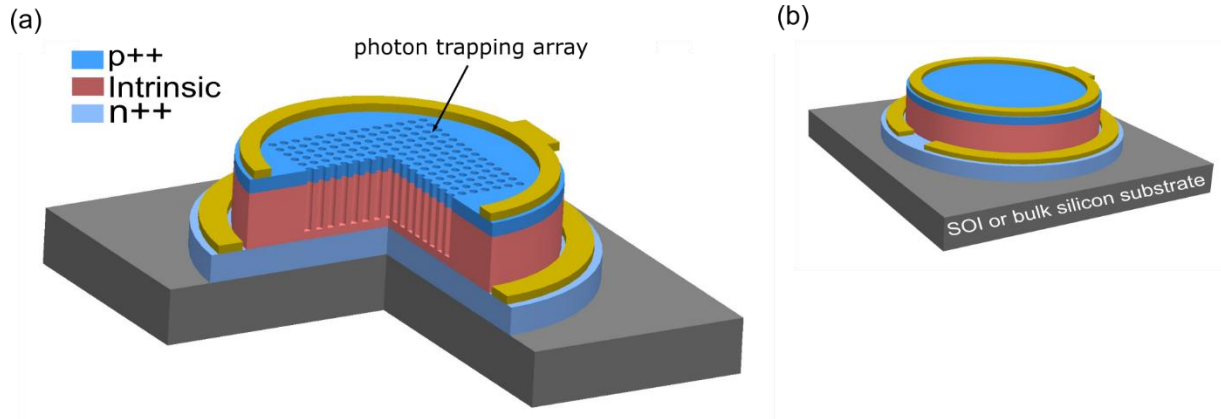
Fig. 3.1. Silicon PD design with implementation of photon-trapping structures. (a) Silicon PD with nanohole array patterned on the surface of the device (Photon-trapping PD). (b) A device with no nanohole patterning for comparison (Conventional/Control PD)

3.2 Device Optical-electrical simulation

Finite Difference Time Domain (FDTD) simulations are used to study the interaction of light with a photon-trapping PD. This method computes the electric and magnetic fields by solving the Maxwell time-dependent equations. For this simulation, a plane wave source is injected normally to the surface. A Perfect Matching Layer (PML) is used as a boundary condition in the direction normal to the surface (z-direction) and is set far enough to avoid any undesired reflections. Periodic Boundary Conditions (PBC) are used in the x-y direction once the unit cell is defined (Fig. 3.2a)

Fig. 3.2b shows the absorption enhancement on silicon achieved with photon-trapping structures from 300 nm to 1100 nm wavelength when photon-trapping structures with a cylindrical profile is implemented in a silicon PD. For this case, cylindrical shape holes

with 700 nm of diameter and 1000 nm of the period have shown enhancement over all the wavelengths of study, especially between 900 nm to 1100 nm wavelength.

 The blue line shows the absorption for bulk silicon and in the red color can be seen the absorption spectrum for silicon with the hole array.
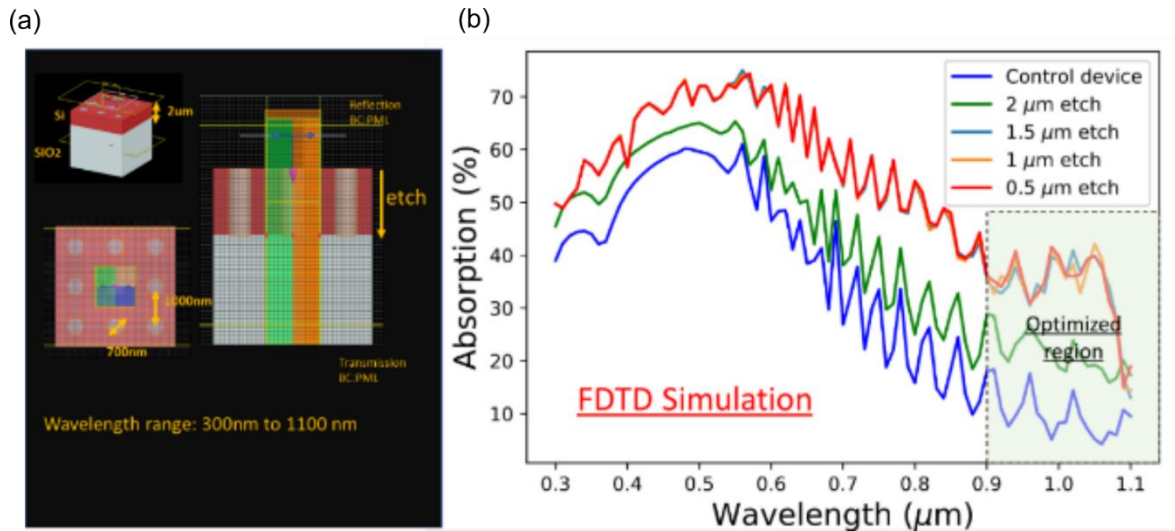
Fig. 3.2. Finite Difference Time Domain Simulation for photon-trapping structure design. (a) FDTD simulation setup. (b) Absorption enhancement on silicon from 0.3 to 1.1 μm wavelength was achieved by the nanohole implementation.

3.2.1 Simulation at near-infrared wavelength

The simulated light absorption of the PD control and PDs with different photon-trapping profiles are depicted in Fig. 3.2 a and b respectively. At 850 nm wavelength, the control PD absorption was estimated to be 8%, as most of the input light was transmitted without interacting with the absorbing layer.

The implementation of photon-trapping structures reduces the reflection from 32% to 17% and exhibits an increased absorption in this 2.5 μm-thickness device to 61% (Fig. 3.3 a-d). A higher number of modes is seen in inverted pyramid nanohole devices (iii) as compared with cylindrical (i) and funnel shape (ii) nanohole devices due to the reflection at the interface of SiO_2 and Si and enhanced lateral propagation of incident light within the devices. Hence, inverted pyramid PDs fabricated on SOI substrates noticeably exhibit higher absorption in comparison with the PDs fabricated on bulk Si and SOI substrates. The simulated inverted pyramid structures exhibit an EQE of 75% and responsivity of 0.53 A/W, while the PDs with etching profiles of the funnel and cylindrical shapes exhibit absorption efficiencies of 70% and 52% and responsivities of 0.49 and 0.36 A/W, respectively (Fig. 3.3e).
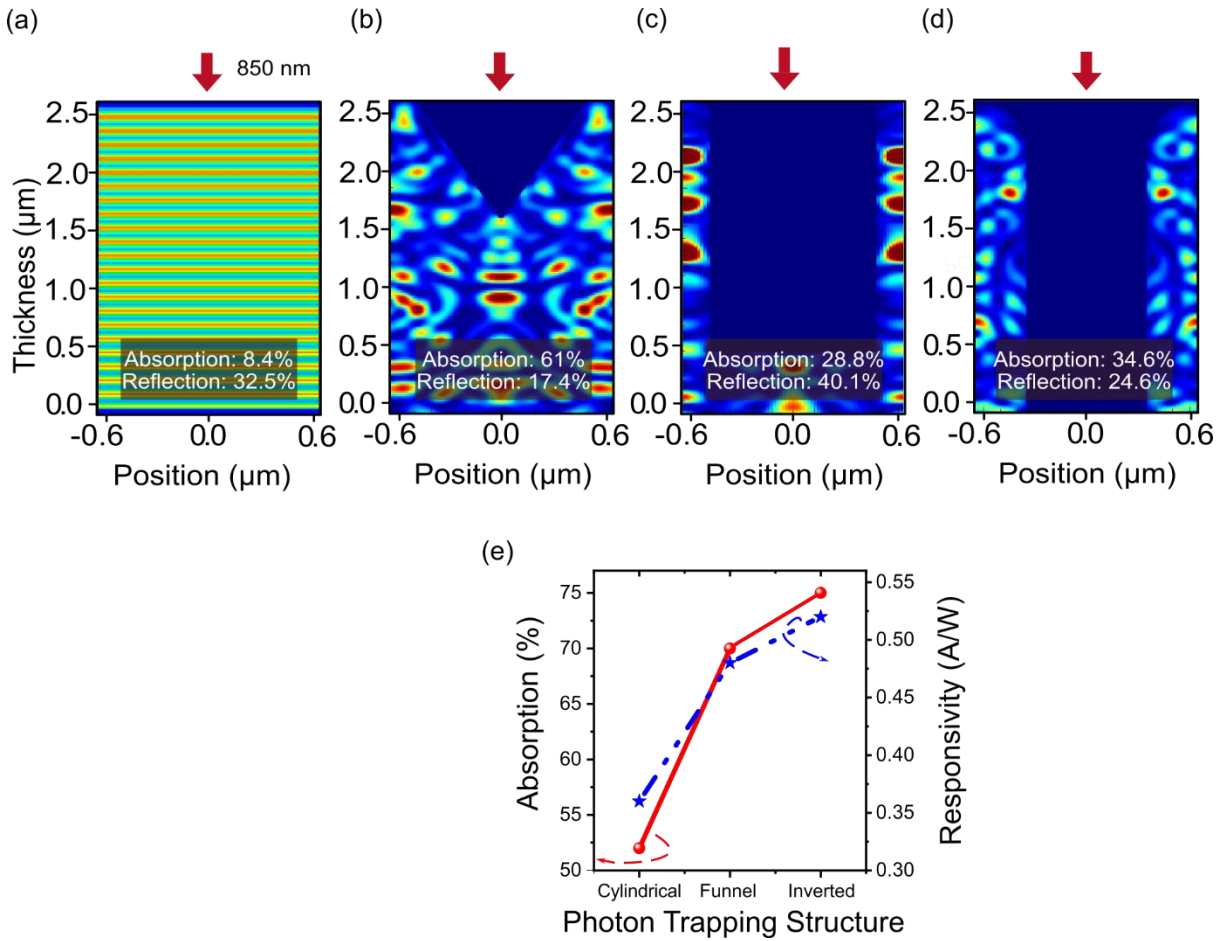
Fig. 3.3. Optical and electrical simulations in Si APD at 850nm wavelength. Power absorption in (a) control Si PD and (b-d) PT-silicon PDs. (e) Calculated maximum photon absorption and responsivity for such PT structures.

3.3 Device fabrication

3.3.1 Doping profile design

A 2.5 μm thick intrinsic silicon layer (*i*-layer) is used as the absorbing material. A boron-doped (5×10^{20} cm^{-3}) SiGeB layer is used as a p-type contact layer, and a phosphorus-doped (10^{19} cm^{-3}) Si layer is used as an n-type contact layer. The high doping decreases

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the minority carrier lifetimes and, at the same time, minimizes the diffusion of photocarriers, as well as reduces the series resistance.

The doping profile was verified using a SIMS measurement (Fig. 3.4). The i-layer is left undoped but turned out to be very slightly n-type doped ($\leq 5 \times 10^{16}$ cm^{-3}) in our devices. Due to the diffusion of the dopant atoms from n+ and p+ layers, transition layers are formed next to the *i*-layer. They are 0.2 and 0.65 µm thick, respectively, and result in reduced thickness of the *i*-layer.
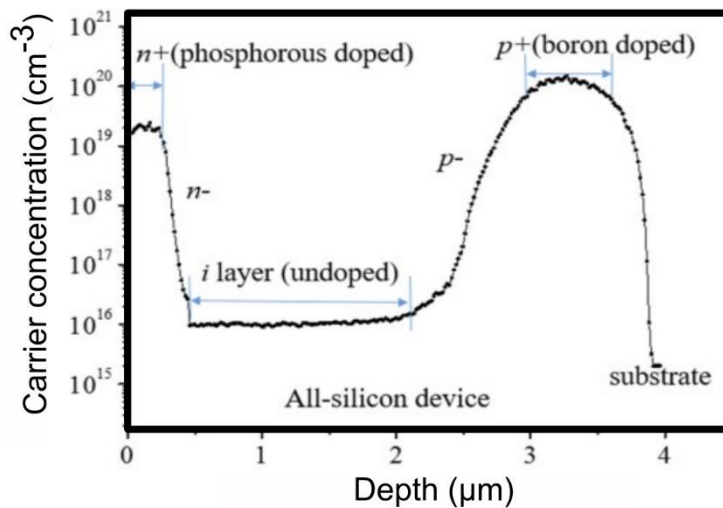
Fig. 3.4. Carrier concentration profile of the fabricated photodiode device. This is measured by the two-point spreading resistance technique. The intrinsic layer thickness is less than the designed 2-µm due to the dopant diffusion from highly doped p$^+$ and n$^+$ layers.

3.3.2 Photodetector fabrication

All the fabrication processes for the photodiodes are CMOS compatible and were done in a class 100 cleanroom. The PIN wafer was precleaned in a piranha solution to remove any organic residue. 100 nm of PECVD silicon nitride film was coated on the wafer at 250 °C for KOH etched holes (DRIE and RIE holes are fabricated without the PECVD nitride film). The next step consisted in patterning the holes on the silicon surface using DUV lithography. The etching method depends on the profile of the hole.

3.3.3 Fabrication of photon-trapping holes

Micro/nano holes with different diameters and periods are used as the grating structures required for photon-trapping. These holes are etched on the surface of the detector at different depths. The etching profiles area cylindrical, funnel shape, and inverted pyramids these structures are arranged in a square or hexagonal lattice. the etching profile and dimensions accuracy are verified by the top and cross-section views of Scanning Electron Microscopy (SEM) [39] (Fig. 3.5).

Photon Trapping Nanoholes

Photon trapping PD

Inverted pyramid Funnel shape Cylindrical
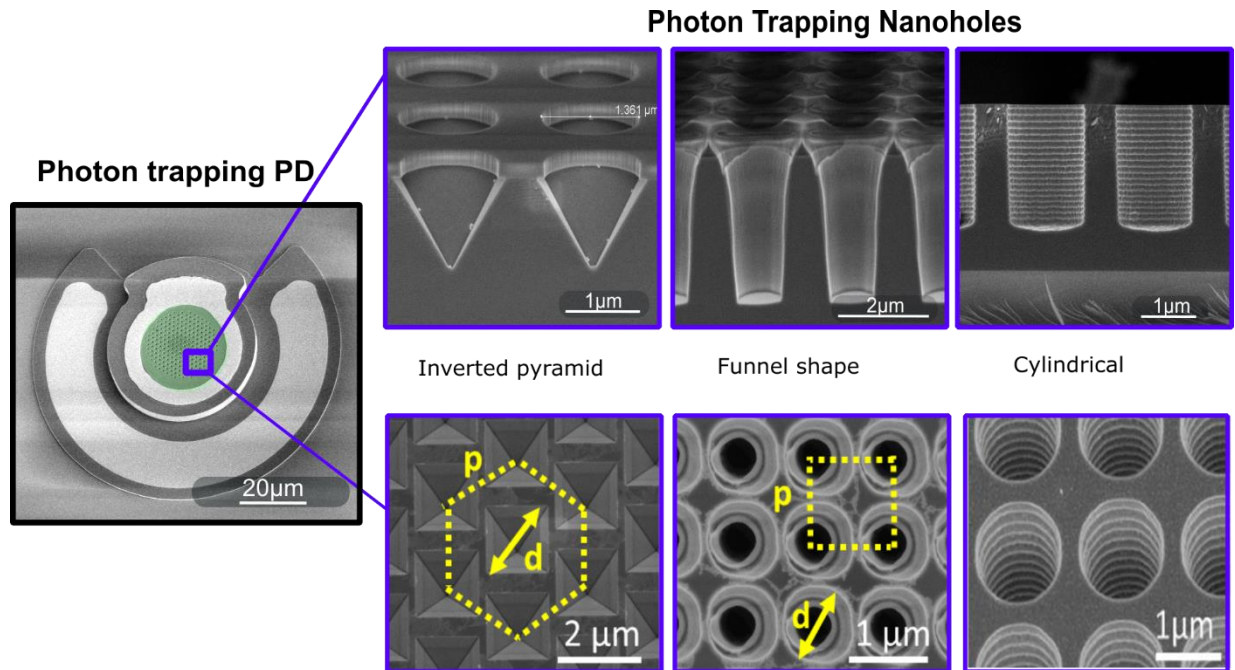
Fig. 3.5. Scanning Electron Microscopy (SEM) top and cross-section view of hole array etched in silicon PD. The images describe a complete PD and the different profiles fabricated as photon-trapping holes including cylindrical, inverted pyramid, and funnel shape profiles. The structures are arranged in a hexagonal or square lattice.

These structures are fabricated as follows:

Cylindrical. Deep Reactive Ion Etching (DRIE) technique was employed to create straight etching. The depth of the holes is controlled by the etching time and etchant concentration.

Inverted Pyramid. A silicon nitride layer is grown by Plasma Enhanced Chemical Vapor Deposition (PECVD) and it is used as a hardmask. Then, it is etched by DRIE to pattern the holes. Then the wafer was immersed in 24% KOH solution for 2 min at 65 °C. Next, DRIE was used to etch the n-mesa to p-Si layer and p-mesa to the SOI substrate.

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KOH anisotropic wet etch can form inverted pyramid-shaped holes with a fixed sidewall angle of 54.7° in the (1 0 0) silicon wafer. The intersection of the (1 1 1) plane causes a self-limiting to etch and thus the depths of the different holes are determined by the diameter of the hole. In addition, due to the etch rate difference in (1 0 0), (1 1 0), and (1 1 1) planes the KOH wet etch makes undercut under the silicon nitride mask and forms square inverted pyramid-shaped holes as Fig. 3.5 shows even if the hard mask pattern is circular.

Funnel shape. The DRIE dry etch follows the remaining circular nitride hard mask pattern and creates circular-shaped holes on the sidewalls of existing KOH etched holes. The combined wet and dry etches create holes with a combination of the square (on top) and circular shapes (at the bottom) as illustrated in Figure 4e. It can also be seen that there is a very abrupt change from 54.7° to 90° at the sidewall. KOH wet etch and the combination of KOH and DRIE etches can create holes with tapered angles of 54.7°.

3.3.4 Electrical contacts

N-ohmic and p-ohmic metal rings that consist of 100 nm of Al and 20 nm of Pt are deposited on n-mesa and p-mesa, respectively, by evaporation followed by a lift-off process. To minimize the leakage current, the wafer was treated in HF or silicon isotropic etchant for 10 s. Finally, the whole device was passivated with an insulating layer consisting of 150/300/150 nm $Si_3N_4/SiO_2/Si_3N_4$ thin layers with contact open. The alternate nitride and oxide layers are used to minimize the effect of possible pinholes and

maximize the insulating effect [40]. Coplanar waveguide contact is designed and implemented to perform measurements at high-speed operation.

3.3.5 Design variations of photon-trapping structures

Several device designs are studied by varying some important device parameters. The devices are optimized by carefully selecting etching profiles, dimensions, distance, and type of substrate (Fig. 3.6).
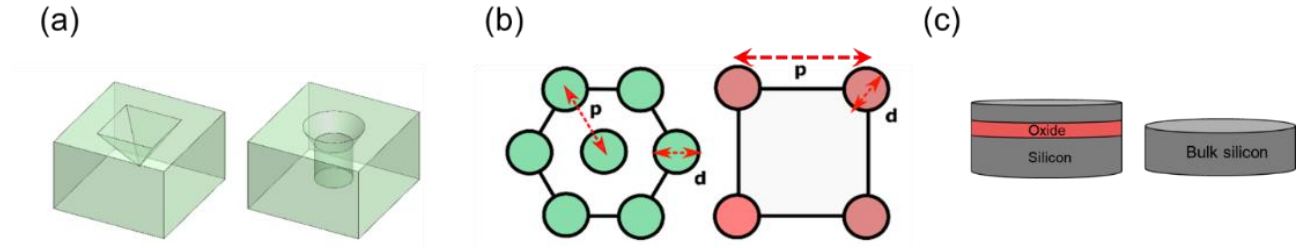
Fig. 3.6. Design parameters of photon-trapping structures. (a) Inverted pyramid and funnel shape etching profile with a tapered hole. (b) Location order of structures: hexagonal (left) and square (right) lattice with lattice parameters of diameter (d) and period (p). (c) Type of substrate: bulk silicon or Silicon-on -Insulator (SOI) wafer.

These nanoholes are distributed in hexagonal or square lattices, designed with different diameters (d) and periods (p) ranging from 630 to 1500 nm and 900 to 3000 nm, respectively. The dimensions of the PT structures are selected to be close to the wavelengths of interest. The periodic distance between structures is reduced in each set of devices by keeping the d fixed, allowing to increase the number of nanoholes that can be accommodated on the surface of PD. The depth of the nanoholes was etched to be

around 2 µm for funnel shape, while it varies between 450 to 1000 nm for inverted pyramids. Also, an unpatterned device is fabricated as a reference which we call a control device to compare with the PT PDs. The devices are fabricated on bulk silicon or silicon-on-insulator (SOI) wafers also for comparison.

Different diameters of photodetectors (D) were fabricated in this work ranging from 30µm to 500µm. Such variation allows us to study the effect of capacitance and EQE as a different number of holes can be accommodated on the surface of the PD (Fig. 3.7).
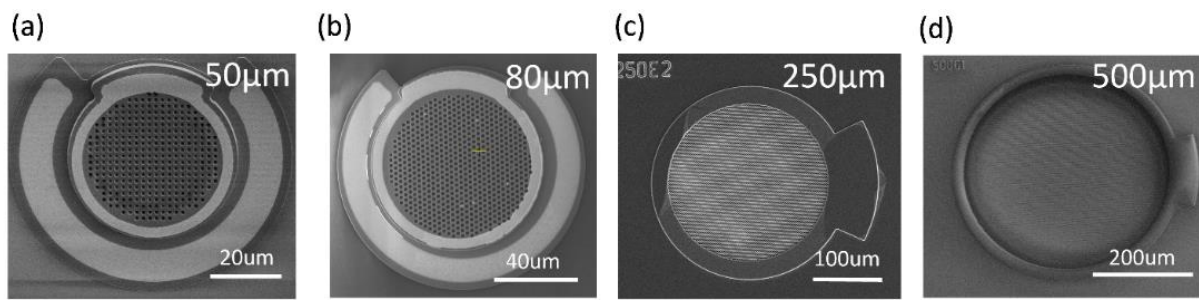
Fig. 3.7. Scanning Electron Microscopy (SEM) images of the fabricated photodetector. (a) 50 µm, (b) 80 µm, (c) 250 µm, and (d) 500 µm diameter.

The different designs are summarized in Table 3.1.

Table 3.1. Device design variations with different parameters. It includes the substrate, diameter of photon-trapping structure and period, etching profile, and device diameter. Both square and hexagonal lattice structures are investigated for all devices.

Parameter	Variation
Substrate	Silicon-On-Insulator (SOI), Bulk silicon
Photon-trapping diameter (d)	630 nm-1500 nm
Period between photon-trapping structures (p)	900 nm-3000 nm
Etching profile	Funnel shape, inverted pyramid, cylindrical
Lattice	Square, hexagonal
Device diameter	30, 40, 50, 80, 100, 500 μm

3.3.6 Optical and electrical characterization

Current-Voltage (I-V) measurements were performed on different fabricated devices under dark conditions and under optical illumination at 450 nm and 850 nm wavelengths with a total power of 1 μW for each. This light was delivered to the PD through an optical fiber with an incident angle normal to the surface. A fiber splitter was used to tap 10% of the light for continuous monitoring of the incident light power. This measurement allows calculating the External Quantum Efficiency (EQE), the dark current of the photodetector, and the reflectance.

External Quantum Efficiency (EQE) is defined as the ratio of photo-generated carriers collected to the number of incident photons at a given wavelength and is used to evaluate the absorption in a detector and is one of the key parameters that describe the sensitivity of PDs.

Reflectance: The cladding material in the silicon PDs is air and the reflection from the top surface of the PDs depends on the index of refraction difference between the silicon and air interface. Thus, 32% of light is reflected from the top surface for a flat silicon PD at 450 nm. However, for a photon-trapping PD, the drop in reflection observed in the simulation can be attributed to the gradual change in the index of refraction from the surface to the bottom of the silicon [41]. This reduces the index of refraction offset between engineered PD surface and air, thus reducing the reflection. The reflectance in the PDs is measured with a custom setup.

Dark Current: While attractive for light manipulation, these high surface-to-volume-ratio nanostructures, which are created by top-down dry etching processes, can also bring other challenges, such as creating silicon surface damage and crystalline defects. Dry etch can cause damage to the silicon surfaces due to the physical ion bombardment and these damaged surfaces can serve as the defect sites that lead to undesirable surface states, traps, and recombination sites [42, 43]. Such defects can degrade the detection sensitivity and increase the noise of photodetectors. Four types of passivation schemes

for our PDs were studied: (1) alternate PECVD layers of SiO_2 and Si_3N_4, (2) thermal oxidation, (3) LIEE using the minimum amount of plasma energy, and (4) hydrogenation by HF treatment.

3.4 Results and discussion

3.4.1 External quantum efficiency at a single wavelength

For an input wavelength, 850 nm series of EQE measurements were performed to study the effect of etching profile, d, p, and substrates (SOI and Si bulk substrate) and maximize the absorption efficiency of the PDs. The results are presented in Fig. 3.8 and discussed based on their different parameters varied in the design.
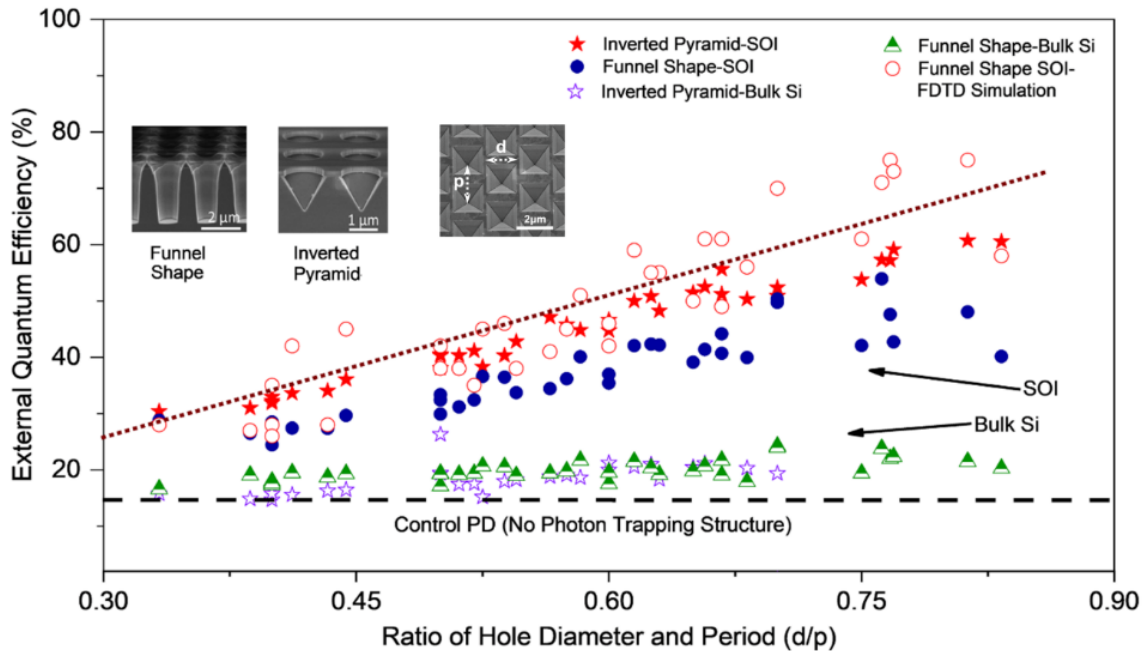
Fig. 3.8. Measured EQE of fabricated Si PDs versus nanohole diameter/period for PT structures at 850 nm wavelength. The PT structures (funnel shape and inverted pyramid) and substrate (bulk Si and SOI) were systematically varied. The FDTD simulated EQE of a PD with funnel shape structure is also included (hollow red circle). The devices exhibit an EQE from 15% to more than 60%.

Substrate. The maximum EQE exhibited by the control device is about 15%, which is in good agreement with the FDTD simulated control device. The PT PDs fabricated on a bulk Si wafer exhibit EQEs between 15% and 25%. However, compared to the control and PT devices fabricated on bulk Si, the EQEs of PT PDs on SOI substrate distinctly increased, resulting in a higher EQE ranging between 30% and 56%.

Subsequently, the influences of the etching profile of PT structures on the EQE are studied.

Nanohole profile. The PT PDs fabricated on SOI substrate are arranged in hexagonal or square lattices with an inverted pyramid or funnel shape etching profiles. PDs with an inverted pyramid exhibit relatively higher EQE than the devices with a funnel shape. For instance, the inverted pyramid PDs with a diameter/period (d/p) of 0.81 exhibit an EQE over 60%, whereas the EQEs exhibited by funnel shape are lower than 50%. This discernible enhancement obtained in the inverted pyramid can be attributed to the effective refractive index gradient in the interface of air and Si, resulting in a superior antireflection effect and efficient coupling of light over a wide wavelength and angular ranges[44]. This is an added advantage of PT structures over traditional quarter-wavelength thin-film antireflection coatings [45].

Diameter/period. The investigated PDs with a 500 μm diameter have a filling fraction as high as ~45%. The EQE of such PDs measured as a function of *d/p* is depicted in Fig. 3.8, where the EQE values increase almost in a linear fashion as *d/p* changes from 0.4 to 0.8 due to the different 2D hole crystalline symmetries. The measured EQE reaches its maxima at *d/p* = ~0.8, which is due to the maximum influence of photon interaction with the 2D hole array, and equivalently the slowest photon velocity or the maximum photon-trapping. The EQE values are in good agreement with the theoretical value simulated from the absorption of 2.5 μm-thick silicon PD.

3.4.2 Rigorous Coupled Wave Analysis (RCWA)

Absorption in photodiodes with photon-trapping holes with different diameters and periods was calculated by applying the Rigorous Coupled Wave Analysis (RCWA) method [46].

RCWA is a rigorous grating diffraction theory that is suited to study the mechanism of the diffraction of light from periodically structured surfaces. In RCWA, the devices and electromagnetic fields are represented by a sum of spatial harmonics, as Maxwell's equations are solved in Fourier space. The eigenmodes of electric and magnetic fields in the grating layer are calculated and analytically propagated. The problem is then solved by matching boundary conditions at each interface using scattering matrices. The hole-integrated i-Si layers in our photodiodes were treated as crossed gratings (or 2D gratings).

Fig. 3.9 shows the RCWA calculated absorption and experimentally measured EQE of photodiodes on the SOI wafer with hole arrays in a hexagonal lattice with diameters of 630 and 700 nm at different periods. The measured EQE of hole-based photodiodes fabricated on the bulk Si substrates is also presented. Generally, the experimentally measured EQE of photodiodes on an SOI wafer matches well with the RCWA calculation for both diameters of 63 and 700 nm.

This analysis shows that hole arrays provide laterally propagating waves due to the deflection of light and they are trapped inside the Si layer with the help of the BOX layer of the SOI substrate due to back-reflection. In the case of bulk Si wafer, holes can generate lateral waves but as there is no back-reflection and thus high transmission to the substrate, these lateral waves are not trapped but are leaking away from the substrate. When the diameter of the holes is a constant, there is a trend that a smaller

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period (higher d/p) generally leads to a better EQE performance of the photodiodes. Based on our analysis, this is attributed to the more significant reduction in both reflection and transmission at a lower period, which allows more light trapped and absorbed in the *i*-Si layer. As higher absorption can be achieved for photodiodes with hole array with higher d/p, we fabricated more photodiodes with d/p between 0.65 and 0.85.
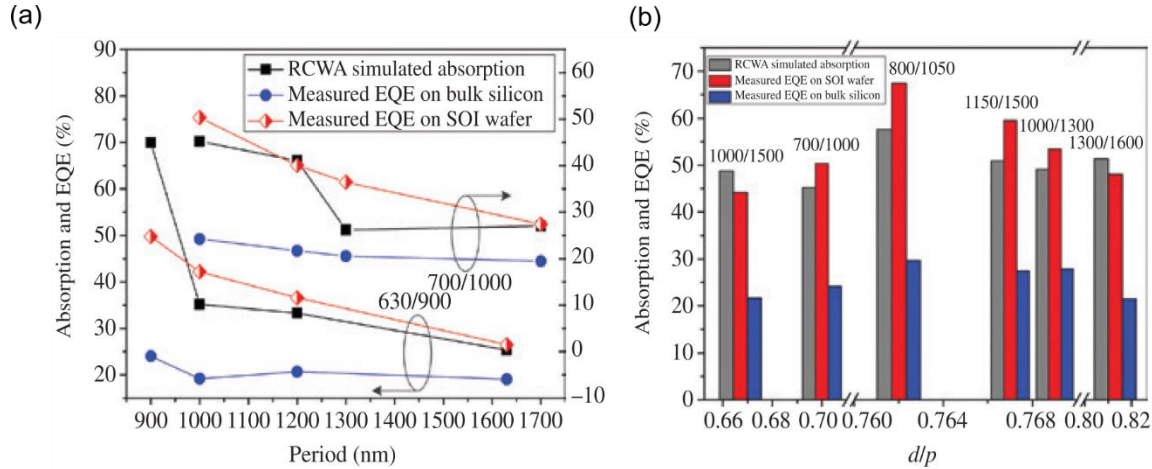
Fig. 3.9. Calculated absorption and measured EQE of photodiodes with integrated photon-trapping holes. (A) RCWA calculated absorption versus period for cylindrical hole arrays on the SOI wafer and experimentally measured EQE versus period for funnel-shaped hole-based photodiodes on bulk Si and SOI wafer. The holes are arranged in a hexagonal lattice with diameters (d) of 630 and 700 nm. (B) RCWA calculated absorption versus d/p for cylindrical hole arrays on the SOI wafer and experimentally measured EQE versus d/p for funnel-shaped hole-based photodiodes on bulk Si and SOI wafer. The holes are arranged in a hexagonal lattice with d/p in 0.65–0.85. Period (p) means the period in the x-direction.

The measurements of EQE confirm that the photos are effectively coupled to the guided mode. The lower measured EQE with respect to the simulated values can be attributed to the effectiveness of carrier collection in the PDs. The nature of the isotropic etch can

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easily cause the adjacent holes to interconnect with each other, especially in the holes with smaller periods. These interconnecting holes contribute to a significant materials loss on the sidewall and lead to exceptionally low EQEs of the device. This is because the spacing between the holes becomes very thin and any electron−hole pair generated experiences higher resistance in constricted structures where surface depletion can impose additional constraints on the transport characteristics [47].

3.4.3 Broadband EQE measurements

Fig. 3.10a illustrates the broadband measurements of 500 µm PDs incorporated with inverted pyramids in a hexagonal lattice formation. The wavelengths range from 800 to 1000 nm, while the nanohole p is varied by fixing the d to 1000 nm. Devices with 1000 nm of d and 1300 nm of p pronounce the highest EQE for all the incident wavelengths. This confirms that a high EQE can be attained for a relatively large d/p. Particularly, the maximum efficiencies at wavelengths of 800, 850, and 900 nm are measured as 58%, 56%, and 45%, respectively for the PT devices with d/p ≈ 0.77. The enhanced absorption coefficients at wavelengths, λ= 800, 850, and 900 nm are calculated to be 4335.5, 4104.9, and 2989.2 cm^{-1} by assuming 2-µm of Si i-layer thickness, whereas the absorption coefficients for bulk Si at those λ points are 850, 535, and 306 cm^{-1}, respectively. Hence, a maximum of about >10 times higher absorption enhancement is attained at some of the incident wavelengths by integrating inverted pyramids or funnel shape nanoholes in the PDs fabricated on SOI substrates (Fig. 3.10b). Herein, the SiO_2 layer of the SOI substrate

acts as a mirror due to the high refractive index difference between Si and SiO_2, resulting in an enhanced reflection and consequently a higher absorption in the *i*-layer of the PDs.
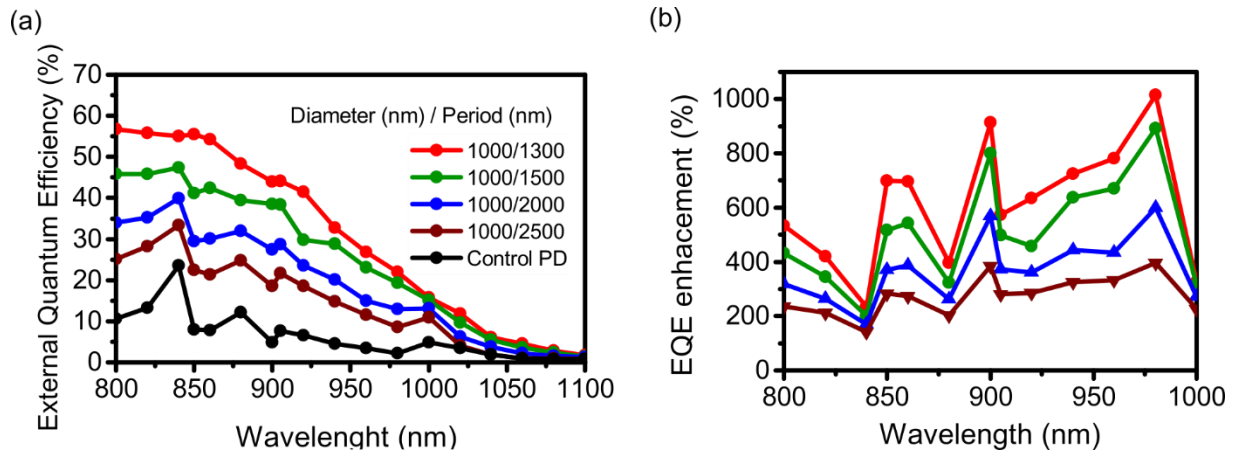
Fig. 3.10. Broadband EQE enhancement in the fabricated PDs. (a)Wavelengths ranging from 800 to 1000 nm with a diameter of 1000 nm and decreasing periodicity. (b)A 10x enhancement in EQE is observed at some wavelengths.

3.4.4 Reflectance

The previous results were also corroborated by reflectance measurements taken on PDs fabricated on SOI wafers and with a custom build setup. Fig. 3.11a shows a reflectance of 35% for the control device without holes. However, such reflectance is reduced to <5% when the diameter of the structures is closer to its period.
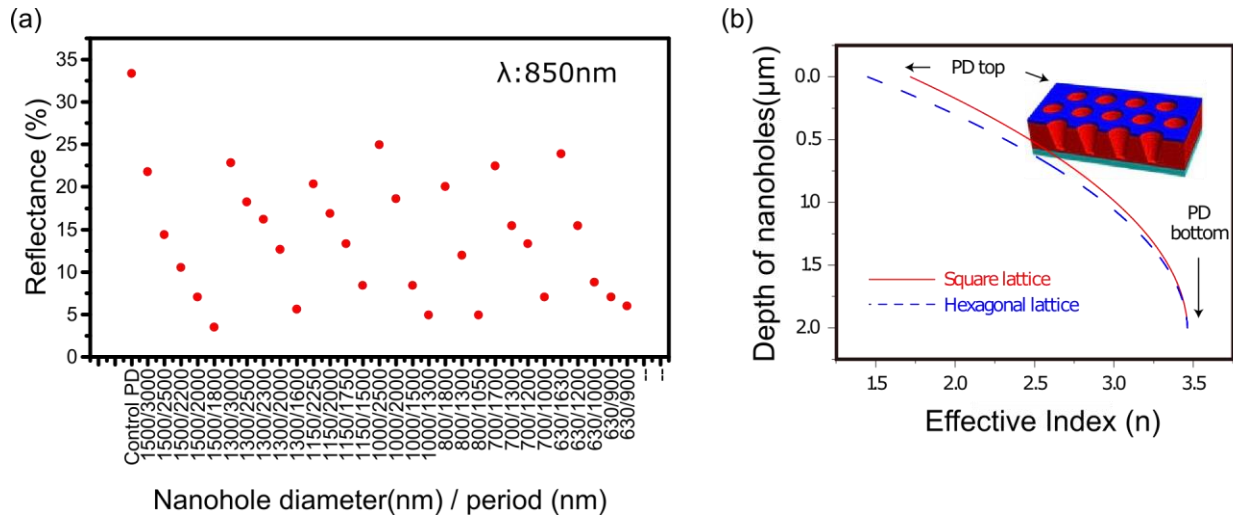
Fig. 3.11. Reflectance reduction in silicon. (a) Reflectance measurements were performed over PDs with different diameters and periods. (b) The effective index of refraction vs depth for a nanostructured silicon surface.

As we move deeper, from the surface, the index of refraction gradually changes from a close-to-the-air value to 3.5 (silicon index of refraction). This gradual change in the index helps in reducing the reflection on the surface. We reached close to 1% reflection in our device for some wavelengths (Fig. 3.11b).

3.4.5 Absorption coefficient

To evaluate the efficiency of the photon-trapping structure the effective absorption coefficient (α_{eff}) is calculated as:

$$\alpha_{eff} = -\ln{(1-A)}/d \qquad (3.1)$$

Fig. 3.12 compares α_{eff} of our photon-trapping-based photodiode with typical bulk silicon ($\alpha_{silicon}$) and GaAs (α_{GaAs}), a material that is currently used in the market due to its direct bandgap and high mobility of its carriers.

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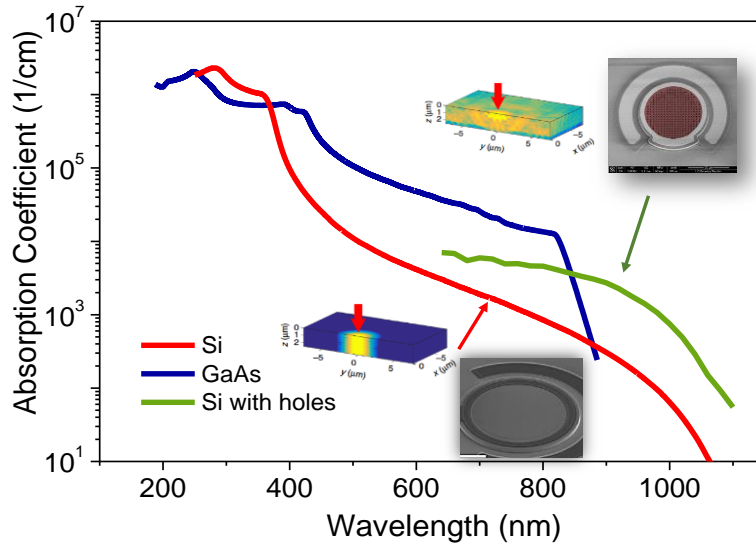
Fig. 3.12. Effective alpha (α_{eff}) for silicon with integrated nanoholes and comparison with bulk silicon and GaAs. The green curve represents the absorption coefficient of Si with light-trapping holes demonstrating superior absorption efficiency at light wavelengths longer than 850 nm.

For bulk silicon at 850 nm wavelength, the α value is 535cm^{-1}, however, when photon-trapping structures are implemented, silicon obtains an α_{eff}=4100cm^{-1}, approximately an 8-fold improvement. The enhancement of absorption overpass GaAs at wavelengths beyond 900 nm, opens the possibility to develop receivers based on silicon instead of using GaAs, the current dominant material.

3.4.6 Dark current

A four-orders of magnitude decrease in leakage current was achieved using HF passivation, reducing the voltage dependency response and eliminating the dependence of EQE with a voltage of 3V and 10V(Fig. 3.13) [48]. Hydrogenation of the damaged Si surface states was done by immersing the Si pin PD wafers in HF solution (HF: H2O

1:10), or silicon isotropic wet etchant (HNO_3/ H_2O/NH_4F mixed solution), for 15 s after the hole and mesa dry etch. The solution removes DRIE and RIE-associated surface damages of Si. HF can provide hydrogen atoms to the dangling bonds at the Si surface and reduces these dangling bonds and metallic paths [49] and, hence, lowers the trapped charges at the surface. On the other hand, the silicon isotropic wet etchant can etch off these damaged silicon surfaces. Both methods are effective to passivate the dry-etched silicon surfaces and minimize the leakage current of the photon-trapping holes-based photodiodes by almost 2 orders of magnitude (Fig. 3.13).
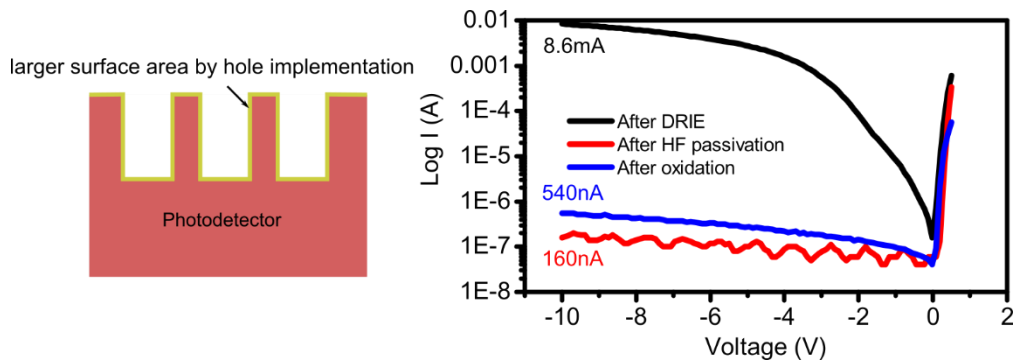
Fig. 3.13. Leakage current and passivation by HF and Oxidation. The etching of holes can damage the surface of the PD and promote crystalline defects. HF and Oxidation methods are effective to passivate the dry-etched silicon surfaces and minimize the leakage current of the photon-trapping holes-based photodiodes

Table 1 shows a summarized comparison of the overall quality of different passivation schemes implemented on the PDs [50]. These schemes can reduce the density of surfaces states on Si surfaces induced by top-down dry etching processes while fabricating the micro/nanoholes. All the passivation schemes can suppress the dark current to an acceptable level (a few hundred nA range); however, some techniques may affect the EQE of the PDs by changing the dimension of the holes or the surface refractive

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index, or by causing unintended dopant diffusion. The method chosen for this work is HF due to the low process of temperature used, at the low changes on EQE. However, other structures such as integrated PDs may be benefited from the oxidation method, due to the SiO_2 used as cladding in Photonic Integrated Circuits. In that case, the change in the index of refraction may need to be considered.

Table 3.2. Comparison of Different Passivation Schemes on the Si pin PD with implemented nanostructures [50].

Passivation schemes	PECVD	Oxidation	LIEE	HF
Dark current suppression	>3 orders	>4 orders	>4 orders	>4 orders
Dimension change of the nanohole	Yes	Yes, small	Yes, small	No
Refractive Index change on the surface	Yes	Yes	No	No
Surface states removal	Partial	Complete	Partial	Complete
PD EQE voltage dependency	Yes	No	Yes	No
Changes in EQE	Yes	Yes	Negligible	Np
Process Temperature	Relatively low	High	Low	Low

3.5 Photon-trapping structures design optimization

Due to the different degrees of freedom for design and fabrication, the implementation of PT structures in PDs remains a challenge. The extensive design variations can be analyzed by numerical methods to optimize the performance of the device. This extensive exercise along with the uncertainties in the fabrication processes contribute to significant challenges in optimizing the device performance.

The extensive simulation and designed vertical silicon photodetectors with more than 150 unique integrated PT structures establis a crucial correlation between these parameters to enhance the device performances. The rigorous simulations and extensive experimental investigations enabled a combination of optimum parameters to help to overcome the trade-off between bandwidth and efficiency in the PDs, where the low absorption coefficient of silicon at NIR, forces the use of a thick layer of semiconductors, degrading the speed of operation. Besides, it allows high sensitivity for low levels of photon detection with 500% higher external quantum efficiency (EQE) as compared with the conventional PDs at 850 nm wavelength, and up to 1000% enhancement at other NIR wavelengths around 1000 nm. Additionally, our fabricated devices exhibit a 35% reduction in junction capacitance due to the introduction of PT structures, with a potential reduction of more than 50%. This, in turn, improves the speed of operation and potentially the device bandwidth.

The extensive design variations make it the most comprehensive study aimed at understanding the PT phenomenon in high-performance PDs. To enable performance projections, it is of interest to develop simple, closed-form expressions for the EQE of a high-speed PT photodetector that intuitively connect the physical parameters of the PT structures, material characteristics, and quality of fabrication. This work elucidates such crucial expressions to enable the implementation of the PT structures for absorption efficiency enhancement, capacitance reduction, and faster time response.

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3.5.1 EQE with respect to the number of photon-trapping structures

Employing the following design guidelines, one can easily fabricate an optimized device by performing simulations beforehand. Firstly, the influence of the number of holes (*N)* on the measured EQE is studied, where a set of devices with a constant device diameter (*D*) of 50 µm is characterized. SEM images of such devices with different N are illustrated in the inset of Fig. 3.14. The measured EQE is presented in Fig. 3.14 for PT PDs with a fixed period and diameter of 1000 and 700 nm, respectively for hexagonal lattice and inverted pyramid profile on SOI, where the N is varied from 0 (control) to 820. Compared to the control device with an EQE of ~12%, the EQE of the PT devices gradually increases with increasing *N*, exhibiting a maximum of >38% for an N value exceeding 820. It is important to note that the test devices above were not among the designs with optimum parameters. This experiment mainly demonstrates a correlation between the EQE of a photodetector and N. Other periods and diameters that were optimized contributed to considerably higher peak efficiencies. The EQE enhancement observed in the device is due to the improved coupling of vertically incident light into laterally propagating modes with increasing *N* within the same area of the devices. Besides, a reduction of planar area in a device leads to decreased surface reflection and improved transmission of the incident light, resulting in relatively higher absorption in the photoactive layer. Consequently, the overall EQE of the PT devices is distinctly increased in comparison to the control device.

Next, EQEs of 500 µm devices with higher *N* values and maximum up to 145000 nanoholes with the same design as 50 µm diameter devices are added to establish a

relationship as shown in Fig. 3.14 (top inset). It shows that, for this design with *d/p*=700/1000, the EQE value can saturate at ~56% for approx. 5000 nanoholes. The maximum *N* presented in Figure 1e is 820 with a filling fraction (*Area_{holes}* / *Area_{device}*) of only 16% for the 50 μm device, while a maximum of about 5000 nanoholes can be accommodated in the same device contributing to a very high filling fraction. Advanced foundry processes can accommodate almost 100% filling fraction by reducing the size of the features (such as contact electrodes, the separation between the region covered by the holes, and interconnect) using tighter fabrication tolerances.
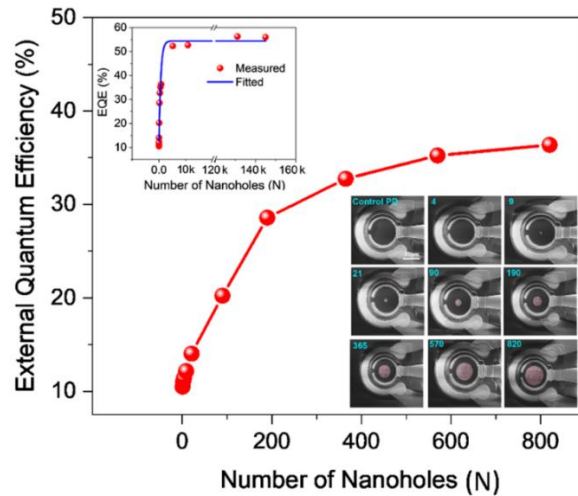
Fig. 3.14. EQE versus number of nanoholes (N) in PDs under 850 nm laser illumination. Insets: (top) fitted curve shows that EQE starts with ~12% efficiency for control PD and saturates at ~56% for PT PD with ~5000 nanoholes. (bottom) SEM images of PDs with an increasing N in devices with 50 μm diameter. Over 40 different PT design variations in diameter, period, and shape are investigated.

3.5.2 Empirical correlations

a) Number of holes

Based on the fitting curve, an empirical equation can correlate the EQE of the devices with the photon-trapping structural and device parameters,

$$\eta_{PT} = \eta_{max} \times \Delta - a\Delta \times \left(\frac{p}{d}\right) [exp\,(-bN)] \quad (3.2)$$

where η_{PT} is the EQE of a PT PD for a specific N, η_{max} is the maximum possible EQE (simulated value) for the device, a and b are design constants that were calculated to be 41 and 0.00147, respectively, for this design, and Δ is the ideality factor of the device. Δ represents the degrees of perfection in the fabrication process and material quality. When the value of Δ is 1, η_{PT} value gets closer to η_{max}. Imperfection in device fabrication and the impurity of materials could lead to Δ smaller than unity, whereas in our devices, it varied between 0.75 to 0.81. Several of the η_{PT} values of fabricated devices were calculated based on Equation 3.2 with varying N, where a good agreement between the calculated values and the performances of the fabricated devices was observed. This equation is valid for any device diameter and can accommodate any number of nanoholes, as shown in the top inset of Fig. 3.14.

b) Diameter/period

The experimental results shown in Figure 3.7 can lead to an empirical equation to capture the correlation between η_{PT} and the d/p in a very generalized fashion,

$$\eta_{PT} = \eta_{flat} + \left(\frac{d}{p}\right)\Delta \times \beta \quad (3.3)$$

where η_{flat} is the EQE of the control devices and β is the PT factor. β can be determined from the slope of a linear curve connecting multiple EQEs as a function of d/p. Equation 3.3 is valid for PD with both hexagonal and square lattices with varying β values, provided that enough PT nanoholes are integrated on the surface of the PDs to reach saturation level in photon absorption. Before fabrication, one can determine β by simulating a set of PDs as a function of d/p. The linear fitting curve shown in Fig. 3.8 was drawn using Equation 3.3 for the simulated funnel shape PDs. With a set of ideal simulations, one can estimate the efficiency of the fabricated devices as a function of d/p by following this design guideline.

3.6 Summary

This chapter demonstrates the design and fabrication of a silicon photodiode with photon-trapping micro/nano holes structures. These photon-trapping holes successfully enhance the absorption of Si to more than 10 times in the NIR wavelengths of operation. At 850 nm, it shows an EQE of more than 56%, which represents a 5-fold increased efficiency compared to Si devices without any photon-trapping holes. It is the first time that Si PDs exhibited such absorption capabilities with a thin absorbing layer of less than 2.5 μm.

Through extensive simulations and experimental implementations of photon-trapping structures in silicon photodetectors, we helped divulge a direct correlation between the enhancement of absorption and physical parameters of the photon-trapping structures integrated in the photodetectors. We employed cylindrical nanoholes, inverted pyramids, and funnel-shaped surface formations and achieved up to 1000% higher quantum efficiency compared to the control devices.

This absorption enhancement was possible by bending the incident beam of light and enabling lateral propagation of modes to prolong the light-matter interactions and suppress back reflection. Analytic equations based on empirical modeling are presented to make it possible to correlate, with high accuracy, the photon-trapping efficiency of the photodetector with the physical properties of the photon-trapping structures, material characteristics, and limitations of the fabrication technologies. Such results open opportunities for the development of complete CMOS integrated receivers operating with high sensitivity and high speed and can be expanded to other semiconductors such as germanium (Ge), gallium arsenide (GaAs), and indium phosphide (InP) based ternary and quaternary materials [51-56].

The higher absorption achieved also allows an increase in the output signal photocurrent of avalanche photodetectors and the photon detection of efficiency of SPADs, a topic that it is discussed in the next chapters.

Chapter 4

Penetration depth control for high gain avalanche photodetectors

Photon-trapping micro and nanostructures in silicon have demonstrated the ability to modify the propagation of light from the incident direction to a perpendicular direction. Such effects reportedly enhanced the absorption in both P-I-N (p-region, intrinsic-region, n-region) [39, 41] and Metal-Semiconductor-Metal (MSM) photodetectors at infrared wavelengths [57]. Thus, the utilization of photon-trapping nanostructures is proposed to overcome the bandwidth-efficiency product limitation that semiconductor detectors pose, by enhancing the absorption and the probability of avalanche by electrons for higher gain and lower noise values [41, 58-61].

This chapter show that photon-trapping nanostructures in silicon photodetectors have the potential to promote the initialization of avalanche by electrons, achieve higher multiplication gain values, and reduce the pulse time response, reducing the absorption in the highly doped regions. This was the first time that photon-trapping structures demonstrate an enhancement in gain, absorption, and time response in silicon PDs at both ends of the visible range, opening the opportunity to develop highly sensitive receivers that could reach the single-photon level.

4.1 Penetration depth engineering for low noise and high gain in APD

The penetration depth is a measure of how the electromagnetic wave penetrates the material. It is defined as the depth at which the intensity of radiation inside the material falls to 1/e (37%) of its value at the surface. This parameter plays a critical role in APDs by making the gain a function of the incident wavelength[38]. For example, in an APD structure with a doping profile as N-on-P, short wavelengths will be absorbed close to the surface. Since the ionization coefficient for holes is smaller than for electrons, the total current gain will be lower than at longer wavelengths (Fig. 4.1a).

We propose and demonstrate the control of the penetration depth of light into silicon APDs, promoting the initialization of impact ionization by electrons, which leads to lower multiplication noise, and higher gain-bandwidth required in avalanche-based photodetectors (Fig. 4.1). We have fabricated Si-photodetectors with photon-trapping nanoholes of different profiles and depths that change the penetration depth of light in silicon at 450nm and 850nm wavelength and how it impacts the gain observed in the devices.
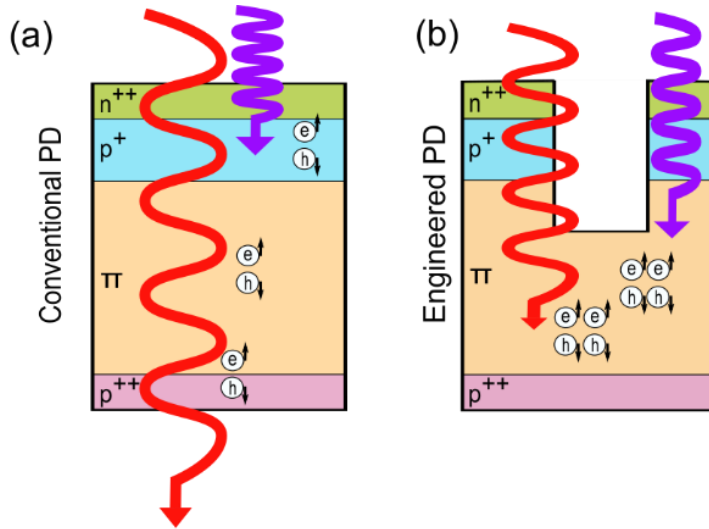
Fig. 4.1. Representation of penetration depth control of different wavelengths in two APD configurations. (a)Conventional penetration depth of short and long wavelengths in an avalanche PD structure with separate absorption and multiplication layers. Short wavelengths (such as blue light from 380 nm to 485 nm) are mostly absorbed close to the surface due to their high absorption coefficient. Longer wavelengths (such as red and near-infrared light from 625 nm to 1100 nm) travel deeper into the device. (b) A potential engineered PD with integrated photon-trapping nanoholes can modify the penetration depth of the incident light. Shorter wavelengths travel deeper while longer wavelengths can be absorbed at a shorter distance.

4.1.1 Optical and electrical simulations

The first set of FDTD simulations is performed to understand the penetration depth and the optical generation of carriers when light with wavelengths of 450 nm and 850 nm are injected into the devices.

Previously, we have performed Finite-Difference Time-Domain (FDTD) simulations to study the interaction of the incident electromagnetic wave in silicon with photon-trapping structures and showed that the presence of photon-trapping structures increases the

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carrier generation by an order of magnitude for 450 nm as well as 850 nm light wavelengths. A Rigorous Coupled-Wave Analysis (RCWA) has also been performed to study the diffraction of light inside the different layers of a PD with a nanohole array [62]. We now use the FDTD analysis to determine the power absorption more precisely in different regions of the semiconductor and calculate the penetration depth of the incident light in the engineered device. Lastly, the impact of this new absorption profile on the overall dynamics of the avalanche photodetector was studied by complementing the optical simulations with electrical simulations using an electrical solver software (Silvaco Inc, Santa Clara, CA, US).

The use of the FDTD method allows for to calculation of the total power of the light absorbed throughout the semiconductors and an integration is performed for every 50 nm of depth to calculate the power decay against the distance from the surface. Such a process allows comparing the penetration depth (δ) of the incident light for PDs with different photon-trapping nanoholes ($\delta_{engineered}$) and conventional PDs ($\delta_{conventional}$).

The absorption profile shown in Fig. 4.2a suggests that it is feasible to control the injection of carriers in the avalanche photodetector to achieve higher signal-to-noise (SNR) ratios by increasing the gain and suppressing the excess noise. Fig. 4.2c shows the calculated power absorption accumulated over the absorbing layer of the control and the photon-trapping PD. The electric field profile corresponding to the doping of the PD demonstrated that the absorbing region was completely depleted (superimposed in Fig.

4.2b. A uniform high electric field over the depleted region ensures an improvement of the amplification factor by raising the impact ionization within the absorbing region.

The FDTD simulations showed that the penetration depth (δ) of the 850nm wavelength-light in the inverted pyramid design was reduced from $\delta_{conventional}$=18.7 µm to $\delta_{engineered}$=2.3 µm (Fig. 4.2c). This nanohole design exhibited higher absorption, shorter penetration depth, and maximum gain. The control of the penetration depth, the reduction of reflection, and the increase of absorption in silicon PDs, collectively increase the gain in the engineered PDs and allows for the fabrication of Si PDs with thinner absorbing layers for high bandwidth operation.

(a)

(b)

(c)
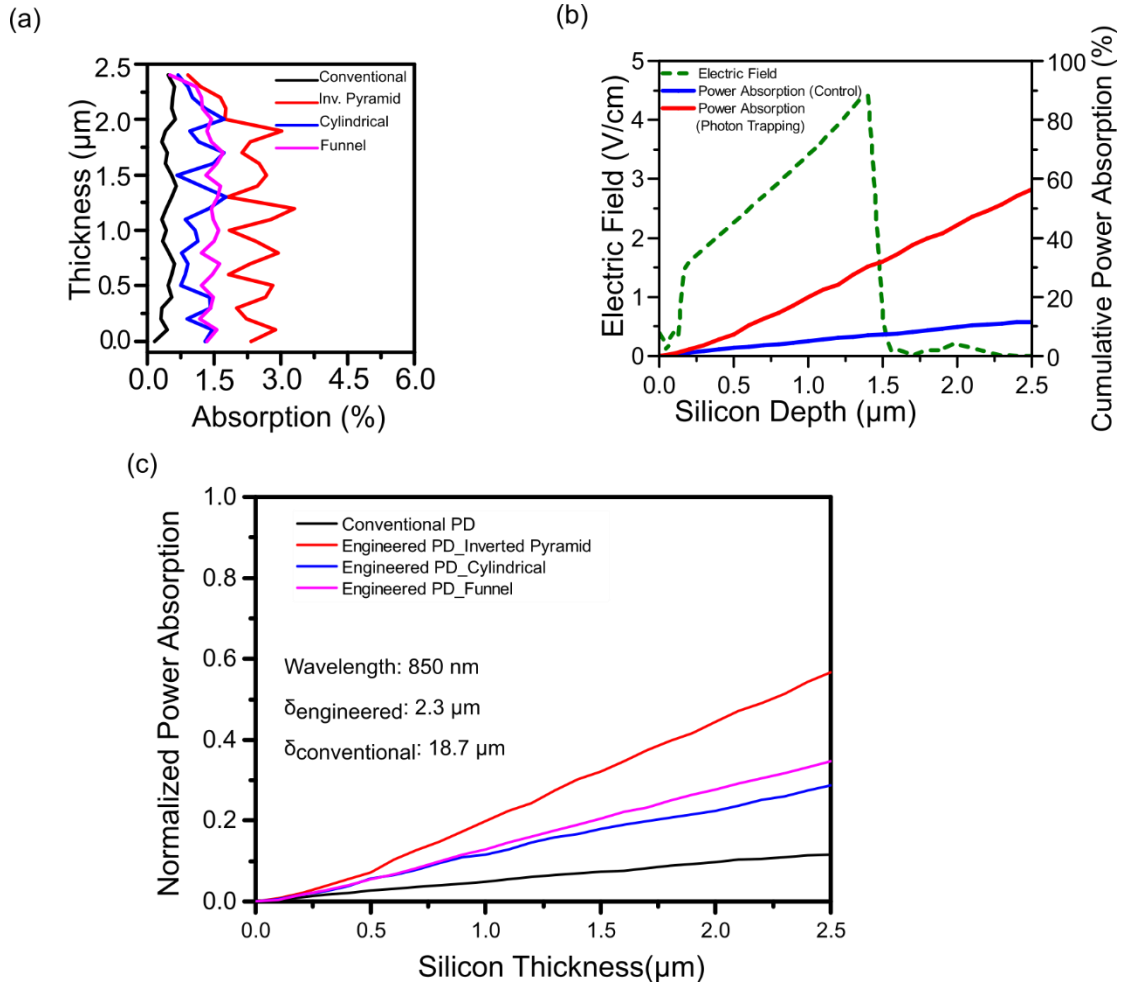
Fig. 4.2. Power absorption of light at 850 nm wavelength. Diverse nanohole profiles are simulated by FDTD. (a) Percentage of absorbed light with respect to the depth. (b) Schematic of the doping profile of the fabricated PD. (c) Comparison of the penetration depth between conventional ($\delta_{conventional}$) and engineered ($\delta_{engineered}$) APDs for 850 nm wavelength. δ is reduced from 18.7 µm to 2.3 µm.

4.2 Simulation at short visible wavelength

For an incident light with 450nm wavelength, the FDTD simulations show in Fig. 4.3 that in conventional silicon with a thickness of 2.5 µm, 60% of the light is absorbed, mostly

close to the surface, while the remaining 40% is reflected. The implementation of the photon-trapping structures reduces the reflection to 14% and the remaining 86% is absorbed (Fig. 6b). Based on these simulations, it is expected to increase the absorption in silicon from 60% to 83.5% with the implementation of nanoholes.
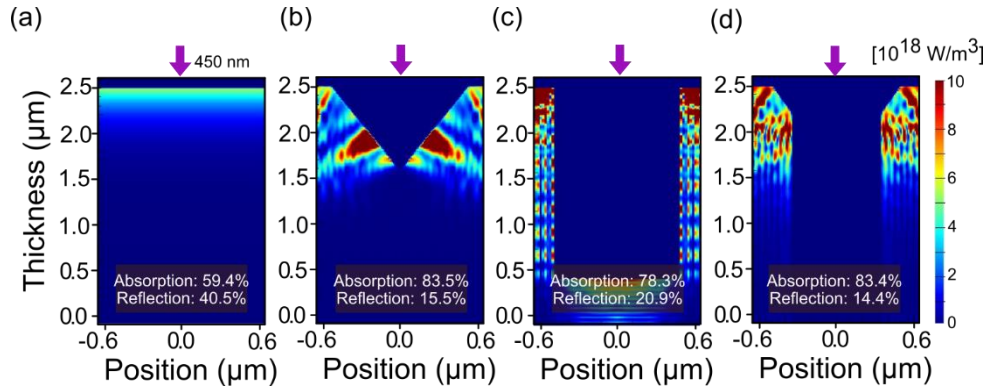
Fig. 4.3. Absorption at 450 nm wavelength in PDs with different photon-trapping structures. (a-d) FDTD simulations of the PD with cylindrical holes show that the 450 nm-wavelength light penetrates deeper in the semiconductor than with other profile designs.

FDTD simulations of the PD with cylindrical holes show that the 450 nm-wavelength light penetrates deeper in the semiconductor (Fig. 4.4), moving from a penetration depth of 0.25 μm in the conventional PD to a maximum of 0.75 μm in the engineered PD with cylindrical nanohole (Fig. 4.4 b). Contrary to the 850 nm wavelength case, at 450 nm the gain increases in devices with nanohole designs that allow a deeper penetration depth.
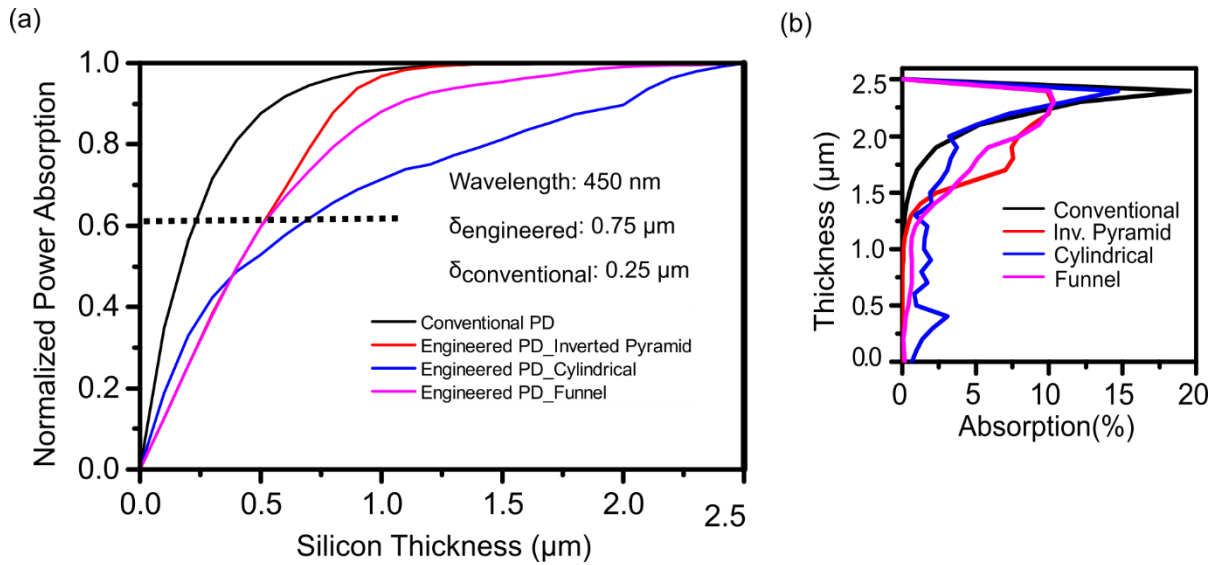
Fig. 4.4. The power absorption and penetration depth at 450nm wavelength. (a)The penetration depth increases from 0.25 to 0.75 µm with the implementation of the cylindrical holes. (b)Absorption distribution at different depths of silicon. Funnel and cylindrical holes reduce the absorption close to surface of silicon while inverted pyramid holes promote the absorption at deeper levels.

TCAD simulations performed with Silvaco show that due to the EM wave interference in the presence of photon-trapping structures, the penetration depth of 450 nm wavelength increases and assists the 450 nm photon in reaching the π-region. Such an arrangement is expected to enhance the carrier generation. Similarly, the penetration depth for 850 nm photons is shown to decrease which will further assist the carrier generation in the π-region. Fig. 4.5a, compares generated carrier-concentration between structures, with and without holes and holes, both for 450 nm and 850 nm light exposure. A clear enhancement of one order in magnitude in the generated carrier concentration can be obtained with the introduction of holes. Further, Fig. 4.5b-e, has compared the

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current density profile between w/o holes and w/ holes structures both for 450 nm and 850 nm wavelengths.
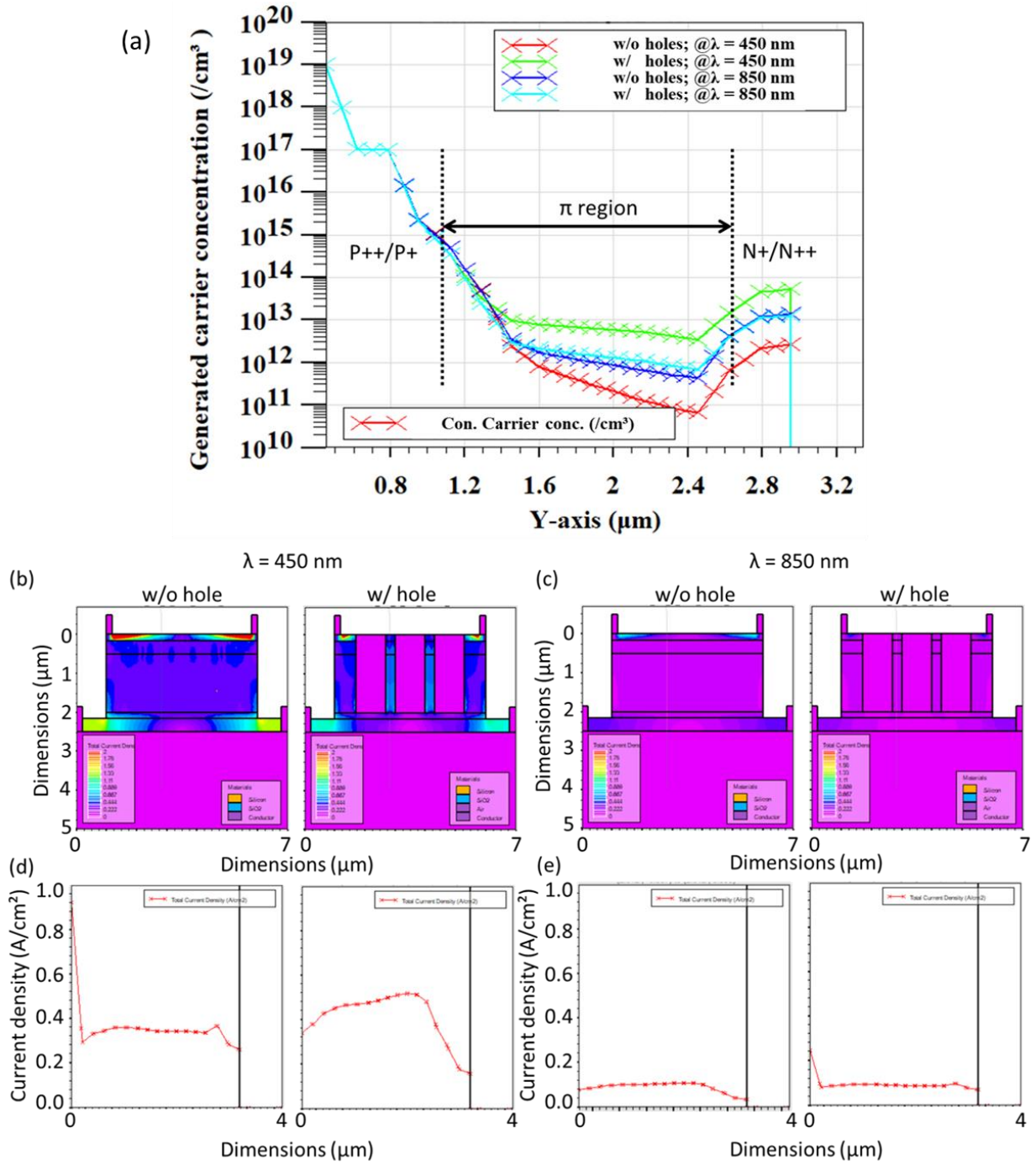
Fig. 4.5. Generated carrier concentration and current density in photon-trapping PDs. (a) Generated carrier concentration comparison between w/o holes and w/ holes PD structure both for 450 nm and 850 nm wavelengths. Total current density comparison via (b-c) 2D contour plots, and (d-e) 1D cutline.

4.3 Device design studied

First, two PDs with an inverted pyramid profile and different period (p) and diameter (d) were studied (configuration 1: p/d = 630/900 nm and configuration 2: p/d = 1200/1500 nm). A PD with the same design and without any etched structures was also fabricated as a reference which is named the control PD.

Secondly, we compare the three different etching profiles of nanoholes with the same d and p values and study the gain obtained. The nanoholes studied have a diameter (d) of 1000 nm and a periodicity (p) of 1300 nm. The depths of the cylindrical and funnel-shaped holes were measured to be 2 µm and 2.5µm, respectively, by Scanning Electron Microscopy (SEM). For the inverted pyramid hole, the depth was measured to be 0.8 µm, which is calculated by considering the etching angle in silicon when KOH is used to etch silicon. The P-I-N structure studied here will favor the enhancement of shorter wavelengths, but a similar approach can be implemented on an N-I-P structure for longer wavelengths.
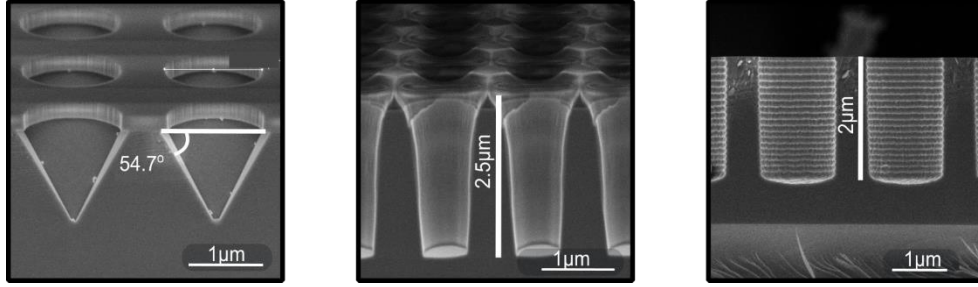
Fig. 4.6. Different photon-trapping nanohole profiles to study the penetration depth and gain.

4.4 Experimental gain measurements

4.4.1 Multiplication gain at 850nm wavelength

Input light with a power of 10 µW at 850 nm wavelength was delivered to the surface of a photodetector with a diameter of 30 µm.

The Multiplication Gain (M) was calculated as

$$M = \frac{\left[I_{photo(V)} - I_{dark(v)}\right]}{\left[I_{photo(ref)} - I_{dark(ref)}\right]} \tag{4.1}$$

Where V_{ref} was taken at 10V.

The I-V curves shown in Fig. 4(a) describe a higher current in the photon-trapping avalanche detector which was attributed to the enhanced absorption. The breakdown voltage in the control PD was measured as 34 V, whereas the photon-trapping device showed a breakdown voltage of around 30 V.

Multiple measurements were taken on the different devices on the same wafer to consider the stochastic process of the avalanche process, obtaining a mean value <M> of 14.5 for the control PD and <M> of 554.6 for the photon-trapping device [Fig. 4.7(b)] with a

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standard deviation of ±0.6 and ±9.6, respectively. From the gain measurements, we can identify the three regimes of operation of these PDs. Up to 10V, the PDs present unity gain and hence are considered PIN regimes. Above 10V and below the breakdown voltage, where the gain values increase by the factor M, is considered the APD regime. Above their breakdown voltage, the devices operated in the Geiger mode regime and hence considered Single Photon Avalanche Detector (SPAD) mode.
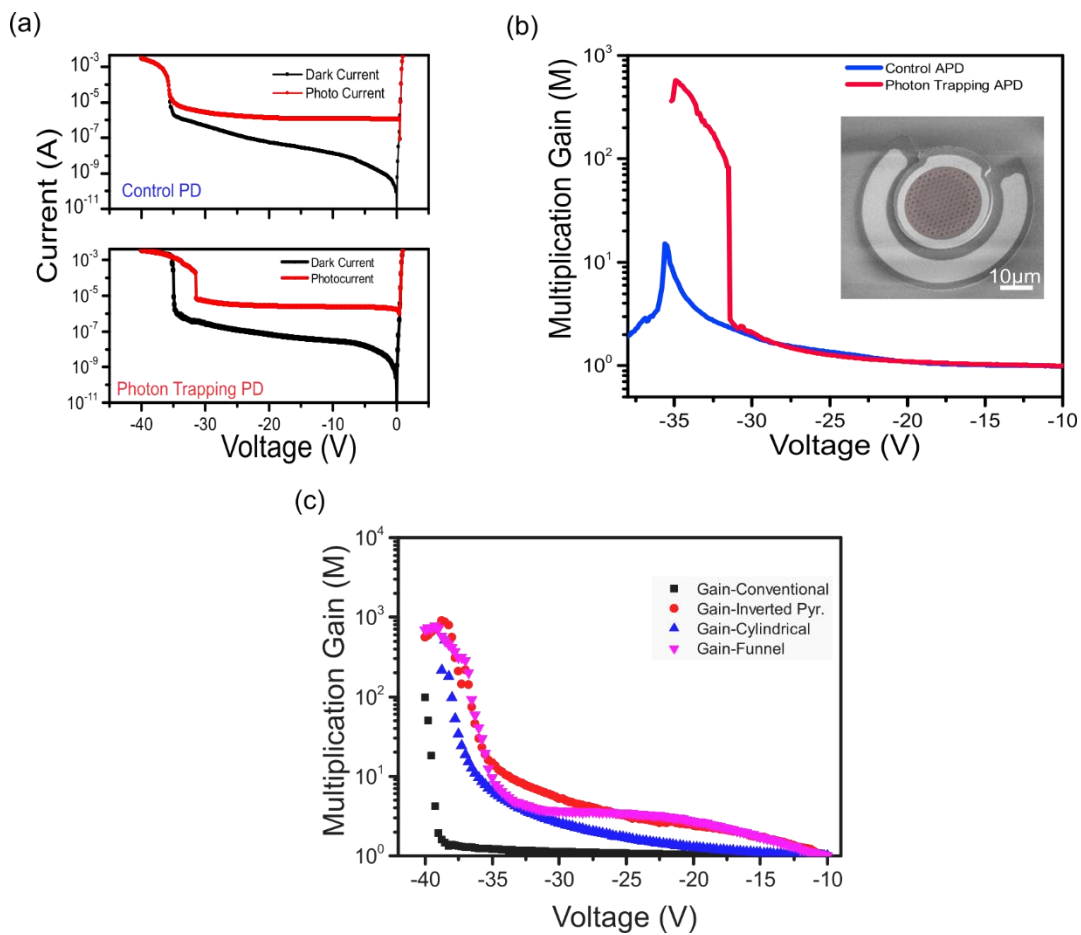
Fig. 4.7.Current-Voltage, gain, and impulse response for Si APD. (a) I-V characteristics of control and photon-trapping (PT) devices. (b) Multiplication gain comparison of PT and control

device. (c) Experimental multiplication gain measurements comparing different nanohole profiles.

When comparing the 3 different etching profiles of nanoholes, it is observed that photon-trapping devices exhibit a gain factor increase from M=97.9, in the conventional PD, to a maximum of M= 893 for the engineered PD with the inverted pyramid hole profile, followed by the funnel (M=770.3) and the cylindrical hole profile (M=515.2) (Fig. 4.7c).

4.4.2 Multiplication gain at 450 nm wavelength

The EQE and gain of the fabricated photon-trapping avalanche PD were also measured with a laser diode emitting at 450 nm wavelength and a power of 30 µW. The bias voltage was swept from 1 to -34 V, in steps of 100 mV, for the devices with a 30 µm diameter, to obtain the dark current and the photocurrent and calculate its gain.

First, two PT APDs devices with different diameters and depths of structures were characterized in addition to the control PD. The diameter of the two PT structures (holes) were 630 and 1300 nm, with a calculated depth of 445 and 919 nm, respectively.

The EQE obtained for the photon-trapping device with a diameter of 630 nm and a periodic distance of 900 nm was 82%, and the PT PD with a hole diameter of 1300 nm gave an EQE of 80%. On the other hand, the control device had an EQE of 54%. The EQE values obtained are corroborated by FDTD analysis. In addition to the higher absorption capabilities of photon-trapping silicon PDs, the multiplication gain was

measured in the APDs. The control PD exhibited a gain of 24, while the PT PDs exhibited a gain factor of 157 and 524, for the 630 nm and 1300 nm diameter structures, respectively (Fig. 4.8a).
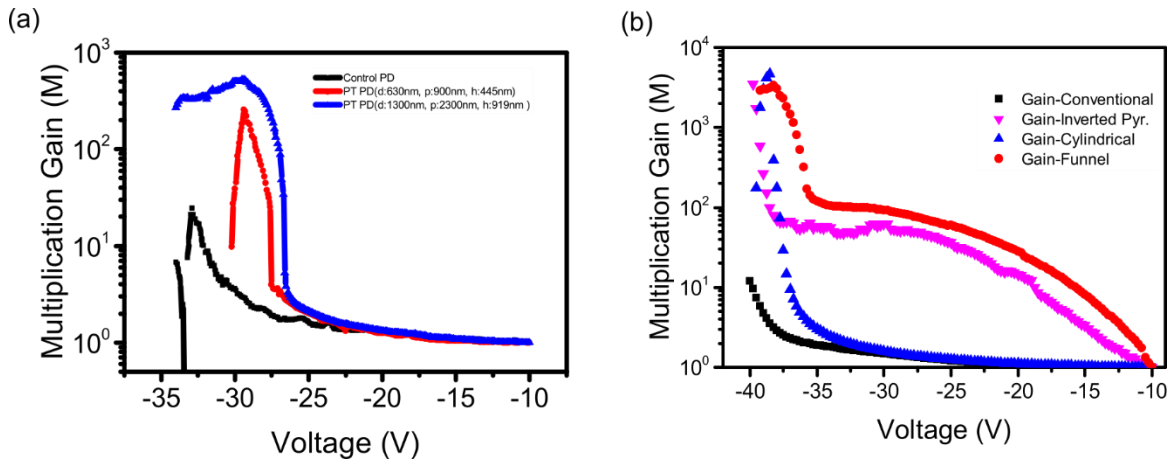
Fig. 4.8. Experimental gain measurements of fabricated devices at 450 nm wavelength (a) Comparison between inverted pyramid profiles with different periods, diameter, and thickness. (b) Comparison between different profile designs. The gain increases by nearly a factor of four hundred, from 11.9 to more than 4000. Cylindrical holes allow deeper penetration of light and obtain higher gain.

Comparing the gain in PDs with different hole designs, our engineered PDs exhibit a gain of M=4707.9 for the cylindrical hole, followed by the funnel-shaped nanohole (M=3925) and the inverted pyramid (M=3508.3) (Fig. 4.8b)

The difference in gain observed can be attributed to the different light penetration depths in the PDs. While in the control PD the 450 nm-wavelength light is absorbed close

to the surface, the deeper PT structure increased the penetration length, affecting the probability of electrons and holes generating an avalanche. The breakdown voltage also varies in the three devices. The PT PDs exhibit a breakdown voltage of 26-27 V, while the control PD required a voltage of 28 V. The variation in the breakdown voltage can be explained by the smaller net volume of the PT PD.

The results of the photon-trapping avalanche photodetectors studied at 450 nm wavelength are summarized in Table 4.1. For this wavelength, devices with deeper holes exhibit a higher gain, similar to EQE and breakdown voltage. Our subsequent study of penetration depth suggests that the deeper absorption of light allows obtaining a higher gain.

Table 4.1. Geometric details, and experimental measurements for EQE, gain, and breakdown voltage of control and photon-trapping APDs for 450 nm wavelength photons.

	Control	Configuration 1 (p/d=630/900 nm)	Configuration 2 (p/d=1200/1500 nm)
Shape	-	Inverted pyramid	Inverted pyramid
Diameter (nm)	-	630	1300
Depth (nm)	-	445	919
Periodicity (nm)	-	900	2300
EQE$_{450nm}$ (%)	54	82	80
Gain$_{450nm}$ 8M)	24	157	524
Breakdown voltage$_{450nm}$ (V$_{BD}$)	28	26	27

Table 4.2 summarizes the obtained results with respect to the penetration depth, gain and External Quantum Efficiency (EQE) obtained in our fabricated devices with different etching profiles at 450 nm and 850 nm wavelength light. It is seen that the longer penetration depth at 450 nm reduces the absorption close to the surface of the device, where, due to high impurity concentrations, carriers can be lost by recombination or slowly transported by diffusion. On the other hand, the penetration depth at 850 nm is reduced from 18.3 μm to only 2.3 μm. Such reduction in penetration depth allows for decreasing the device transit time with a direct impact on the bandwidth of the devices. These results

allow increasing the gain in APDs by 400 times at 450nm and by more than 9 times at 850 nm in our first demonstration.

Table 4.2. Penetration depth, multiplication gain, and EQE in silicon photodetectors with different nanohole profiles. The gain in APDs with photon-trapping holes is measured to be almost 400-fold higher at 450 nm and almost 9-fold higher at 850 nm.

	Wavelength (nm)	Conventional	Inverted Pyramid	Cylindrical	Funnel
Penetration depth (µm)	450	0.25	0.55	0.75	0.61
	850	18.7	2.3	>2.5	>2.5
Multiplication Gain (M)	450	11.9	3508.3	4707.9	3925.8
	850	97.9	893.8	515.8	770.3
External Quantum Efficiency (%) for M=1	450	54	82	74	79
	850	14	56	39	42

The enhancement in the generated carrier concentration and gain could be attributed to penetration depth modulation for both wavelengths. Due to the diffraction, the penetration depth for lower wavelengths such as 450 nm, increases, and due to the very same diffraction, the penetration depth for higher wavelengths such as 850 nm, decreases resulting in enhanced absorption in the π-region causing enhanced carrier generation.

Our results are compared again to different silicon avalanche PDs reported in the literature (Table 4.3) Demonstrating a superior absorption at short-visible and near-infrared wavelengths. In addition, our PT device exhibit a responsivity of 297 mA/W at 450 nm and 425 mA/W at 850 nm. Reported responsivities on silicon APDs range from 90 mA/W to 230 mA/W between 400 nm and 480 nm [63-66] and from 4mA/W to 560 mA/W at 850nm[67, 68], as also reported in [69]

Table 4.3. Benchmark of different high-speed silicon avalanche photodiodes.

Author/ Year	Material	EQE	Wavelength	Gain	Reference
Bartolo-Perez, 2021	Si pin APD	EQE 82% (R=0.297A/W) EQE 62% (R=0.425A/W)	450 nm 850nm	$M_{450nm}=524$ (27V) $M_{850nm}=554$ (29V)	[70]
Pancheri, 2007	Si CMOS (0.35 μm)	EQE 23% (R=0.09 A/W)	480 nm	13 (10.3V)	[63]
Rochas, 2002	Si APD 0.8μm	EQE 50% (R=0.16A/R)	400 nm	20 (19V)	[64]
Biber, 2000	BiCMOS 2μm	EQE 25% (R=0.128A/W)	635 nm	7 (19.1V)	[65]
Pauchard, 2000	custom	EQE 70% (R=0.237A/W)	420 nm	16 (14.1V)	[66]
Youn, 2014	Si APD	1.4 A/W with gain	850 nm	(12.4V)	[67]
Stenindl, 2014	High Voltage CMOS 0.35(um)	0.41 A/W (75.8%)	670nm	$6.6e10^4$ $M_{optimum}=50$	[68]

4.5 Summary

We have demonstrated that it is possible to guide photons to a critical depth in a semiconductor and maximize the gain-bandwidth performance and absorption efficiency in avalanche-based photodetectors by integrating photon-trapping nanoholes with

different profiles and depths on the device surface. Such nanoholes allow for the engineering of the penetration depth for different wavelengths on silicon. A longer penetration depth for short wavelengths such as 450 nm can reduce the absorption close to the surface of the device, where carriers can be lost by recombination or slowly transported by diffusion. On the other hand, the penetration depth for the long wavelengths such as 850 nm is reduced from 18.3 µm to only 2.3 µm. Such reduction in penetration depth allows for decreasing the device transit time with a direct impact on the bandwidth of the devices. To the best of our knowledge, this study is the first comprehensive evaluation of the gain, and detection efficiency of avalanche photodiodes (APD) with photon-trapping nanostructures for photons of 450 nm and 850nm wavelengths [71].

These results allow increasing the gain in APDs by 400 times at 450 nm and by more than 9 times at 850 nm. The engineering of the penetration depth in APDs and SPADs allows for designing devices with higher gain-bandwidth required in a myriad of emerging applications including biomedical imaging systems such as Fluoresce Lifetime Imaging Microscopy (FLIM) and Time-of-Flight Positron Emission Tomography (TOF-PET), quantum communications systems, and 3D imaging systems.

First, we have fabricated photon-trapping photodetectors and evaluated their performance at 850 nm. Our detectors exhibited 30 times higher gain, and enhanced absorption efficiency – from 16% to >60%. At an input wavelength of 450 nm, the EQE

increased from 54% to 82% and the gain was 22 times greater in a device with photon-trapping structures. Therefore, Si-based APDs with photon-trapping structures showed a significant increase in absorption when compared to their flat counterparts. With an optimized doping profile and thinner layers, the gain can be further enhanced. Such effort will be described in chapter 6.

Chapter 5

Time response of photon-trapping PDs

Here we analyze the time response of our photon-trapping APDs at unity gain. We demonstrate that the devices have superior time responses over the conventional devices. This is due to the lower transit times and the reduction in capacitance achieved when implementing the nanoholes. Then, an analysis of the time response of the devices when they are biased in APD mode is presented, demonstrating that the effective absorption of light in the intrinsic layer further improves their response time.

5.1 Time response in unity gain mode

For high-speed characterization, a mode-locked pulsed fiber laser at 850nm with an average power of 100 µW is used as the light source. The laser output pulses are focused on the active region of the silicon PDs with the use of a single-mode fiber tip. The photoresponse is measured using a 20GHz sampling module.

Fig. 5.1 shows a pulse response for devices with different diameters. The smallest device has a diameter of 30µm and exhibited a pulse response of 30ps Full-Width-Half-Maximum (FWHM). When considering the 20ps FWHM of the sampling and the optical pulse width

<1ns, the actual FWHM of the device is 23 ps. Such a response suggests that a data transmission rate of 20Gbps can be achieved with these photodetectors [41, 72].

The FWHM of the impulse response has been reduced up to 25% in the PD with an 80 µm diameter. This is due to the reduced effective capacitance and consequently reduced RC time in PT PDs compared to the control devices. Previous modeling of the impulse time response obtained in the 30 µm device diameter shows a calculated bandwidth of 3.5GHz when considering the tail. Achieving more abrupt junctions in the p-i and i-n interfaces can allow a 3dB bandwidth of 13GHz, due to the smaller tail [41, 73]. Higher FWHM and RC time reduction can be achieved in optimally designed PT PDs by fabricating them with tightly packed nanoholes and narrower ohmic contacts in advanced semiconductor foundries.
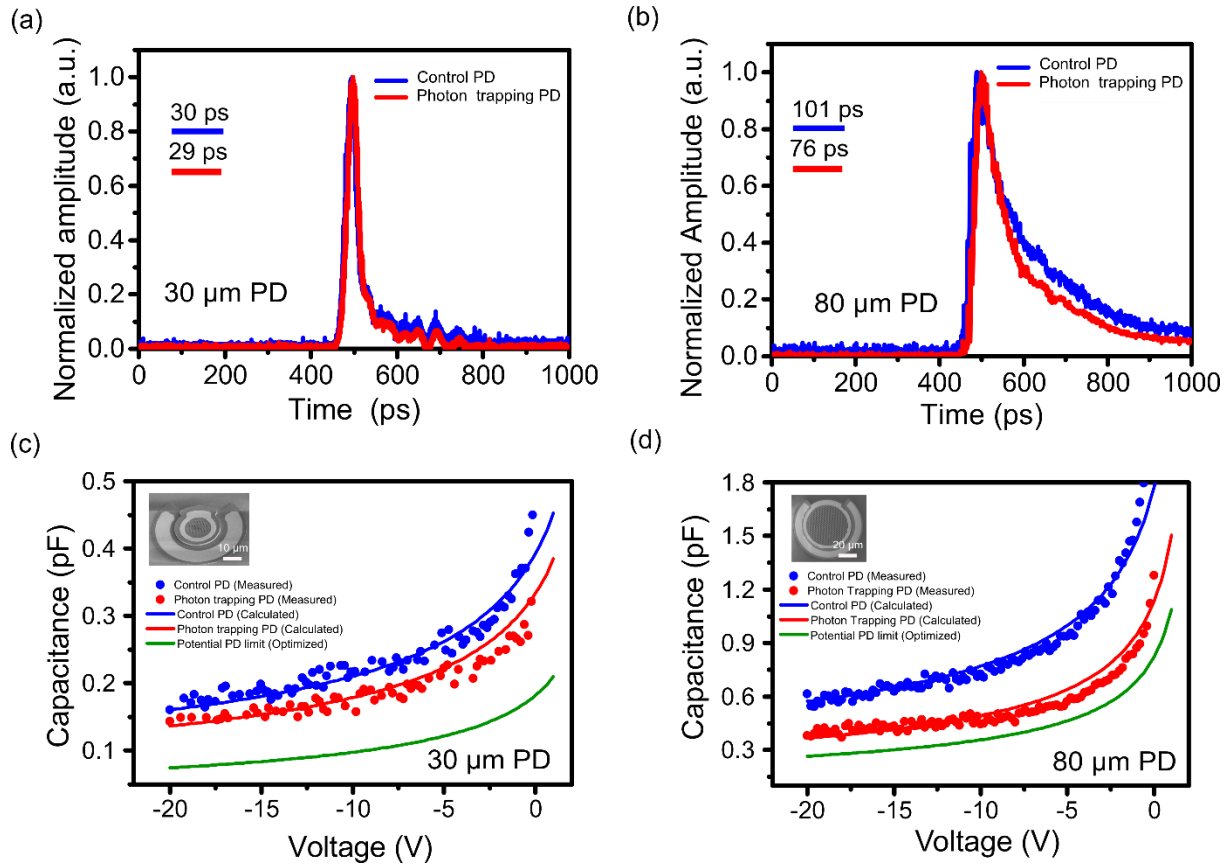
Fig. 5.1. Speed and Capacitance characteristics in PDs. (a) Pule time response in a device with 30 µm of diameter shows an FWHM of 29-30ps.(b) for an 80 µm diameter device, the FWHM difference is more prominent since more holes are added to the device. Capacitance-voltage characteristics of PDs comparing PT and control device. (c) 30 and (d) 80 µm diameters, confirming a 15% and 35% capacitance reduction, respectively. Over 50% capacitance reduction can be realized by increasing the number of PT nanoholes.

5.1.1 Capacitance reduction in photon-trapping PD for high-speed operation

The 3dB frequency of pin PD is highly dependent on two factors: (i) RC time, dominated by the junction capacitance, and (ii) transit time. Both terms are dependent on the

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thickness of the PD, while a thin device layer (1-5 µm) decreases the transit time, it will introduce a higher junction capacitance.

A reduction in the junction capacitance due to the presence of the nanoholes can be taken into consideration to write the following modified expression of f_{3dB} [74].

$$f_{3dB} = \frac{1}{\sqrt{[2\pi R \times C(1 - ff)\,]^2 + [t_r/0.44]^2}} \quad (5.1)$$

Where t_r is the transit time required for the carriers to reach the electrode at saturation velocity, R is assumed as 50 Ω, and ff is the filling fraction of the nanohole array. By considering the PIN PD as a parallel plate, the capacitance can be written as $C=\varepsilon_o\varepsilon_r A/w$, where ε_o and ε_r are the permittivity of vacuum and silicon, respectively; w is the depletion layer width, typically the i-layer, and A is the junction area. The integration of an array of PT holes leads to the reduction of effective cross-section area and active materials in the PDs. Consequently, the overall junction capacitance of a PD is reduced proportionally to the ff of the nanohole array. The use of a thin i-layer in conventional PDs reduces the transit time but increases the junction capacitance. Such a trade-off is effectively addressed with integrated PT nanoholes.

The improvement shown in the pulse time response can be explained by the reduction of the capacitance created by the incorporation of holes on the surface of the PD.

Fig. 5.1b and c present the results of capacitance-voltage (C-V) measurements performed on the PDs with a diameter of 30 and 80 µm, respectively. The top left insets represent the top view of SEM images of PDs. The experimental C-V measurements

between the control and the PT PD show a 15% and 35% of capacitance reduction for PDs with 30 and 80 µm of diameter, respectively. Such reduction is corroborated by applying analytical modeling of the capacitance based on the doping profile and built-in potential as described in the next sections[75]. Furthermore, the same investigation is also conducted for devices with 40 and 50 µm diameter and included.

Higher capacitance reduction is observed as the diameter of the PDs increases since, in our current design, a larger diameter of PD allows to accommodate a higher number of nanoholes. Both devices can reach >50% of capacitance reduction by decreasing the area occupied by the ohmic contacts on the surface of the PDs using CMOS foundries where the width of metal contacts can be less than 150 nm[76].

5.1.2 Capacitance modeling

In Fig. 5.1, the capacitance was measured in the control PD and modeled based on the doping profile using Equation 5.2 (blue solid line). Using the same model, the capacitance is calculated for 15% and 35% of area reduction for the device with 30 µm and 50 µm of diameter, respectively. The resulting capacitance (solid red line) agrees with the experimental capacitance measured in PT PDs. The previous results allow us to extrapolate the model to 53% of area reduction, obtaining the green solid line that describes the potential capacitance reduction. The analytical model used to calculate the junction capacitance with consideration of the filling fraction is as follow:

$$C_j = \frac{\varepsilon_s}{w} \times A_{reduced} = \sqrt{\frac{q \times \varepsilon_s}{2 \times \emptyset_i}} \; x \; \frac{N_a \times N_d}{N_a + N_d} \times A \times (1 - FF) \qquad (5.2)$$

Due to the larger ratio between the active region over the total device area in PDs, with a bigger diameter in our current design, it is expected to observe a bigger capacitance difference in such devices. We have calculated the percentage of capacitance reduction for all the periods and holes fabricated and compared them with respect to the control device.

PDs with a large diameter, such as 500 µm are expected to have more than 50% of capacitance reduction with our current designs. Devices with a smaller diameter, such as 100µm are estimated to have a capacitance reduction of around 30% (close to the capacitance reduction obtained in devices with 80µm of diameter and reported). Smaller devices present lower capacitance reduction due to the number of holes that can be placed on their surface. However, state-of-the-art semiconductor foundries can fabricate narrower ohmic rings, allowing to increase the number of holes, and the distance between them, allowing to increase the filling fraction of the nanohole array and decrease its capacitance further. In such a case, it is expected to obtain a capacitance reduction of more than 50%, when nanoholes have d/p ratios higher than 0.8 and are arranged in a hexagonal lattice (Fig. 5.2, green line)
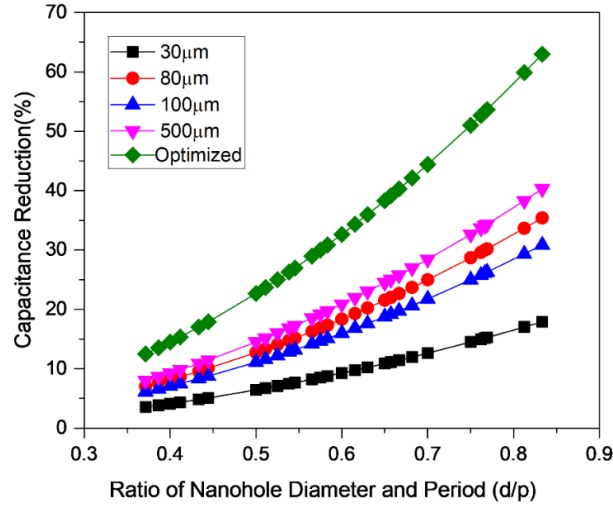
Fig. 5.2. Estimated capacitance reduction of photon-trapping PDs with respect to the ratio of nanohole diameter and period (d/p) for devices with different diameters of device.

5.1.3 Ultimate bandwidth-efficiency

The 3dB frequency bandwidth of a PD can be further optimized by the reduction of capacitance observed in our devices, and by using a proper intrinsic layer thickness. Fig. 5.3 shows the estimated 3dB bandwidth of PDs for the intrinsic layer thickness in a conventional PD and a novel photon-trapping PD (assuming a 60% of capacitance reduction) for a 12 µm diameter device. Such a PD is expected to have its highest 3dB frequency of operation to over 100 GHz with only 0.4-0.7 µm of thickness. This is >30% of enhanced bandwidth compared with a conventional PD. With the photon-trapping approach, such speed enhancement can be achieved since the capacitance is reduced, and the efficiency is enhanced despite such thin absorption layers.

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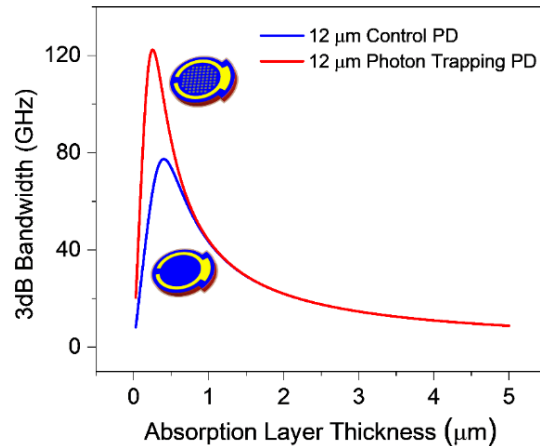
Fig. 5.3. Estimated 3dB bandwidth of operation for silicon PDs with different absorption layer thicknesses. Here a 12 µm diameter device is considered. A photon-trapping PD is estimated to achieve over 100 GHz 3dB bandwidth of operation which would require a thickness of 0.4-0.7 µm.

The reduction of capacitance can also benefit sensors that require photodetectors with a large area, such as single-pixel imagers. These sensors are generally limited in speed of operation due to their large junction capacitance related to the area of the device. However, photon-trapping structures implemented in such devices can decrease their capacitance, and enhance their speed of operation, enabling imaging systems with higher resolution [9].

The collective absorption enhancement of >75 %, capacitance reduction of >50%, and FWHM reduction of > 35% allow any designer to optimize the PDs with integrated photon-trapping structures (Fig. 5.4a). A drastic reduction in the capacitance can dramatically enhance the ultrafast operation of a PD. For example, the impulse response of a control

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device with 30 µm of diameter is measured to be 30 ps and with optimum PT nanoholes, it can exhibit ~19 ps FWHM (Fig. 5.4d, inset).
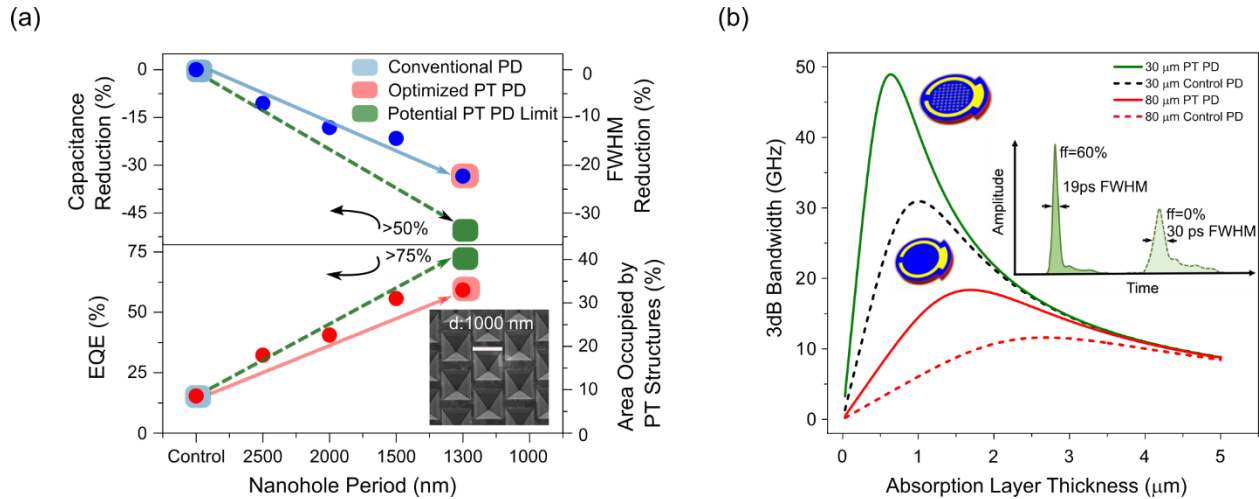
Fig. 5.4. Absorption efficiency and bandwidth optimization. (a) A study of >150 different devices are used to optimize PT PDs with simultaneous improvement in EQE, reduction in capacitance, and enhancement in time response. A set of devices with fixed d of 1000 nm and different periods are used to show that >50% of capacitance reduction and >75% of EQE can be achieved at 850 nm. (b) Modeling of 3dB bandwidth versus absorption layer thickness considering 60% of capacitance reduction in PT PDs. Illustrations in the inset show a stronger signal amplitude and narrower impulse response of 19 ps is possible in a 30 µm PT PD.

5.2 Time response in APD mode

We have demonstrated that our photon-trapping structures can reduce the capacitance by more than 50% due to the reduction of the surface area of the device [77]. Transient time can be improved by employing thin highly doped contact layers (n^{++} and p^{++} layers)

that facilitate the generated fast carriers' transition to the outer circuit elements and reduce the slow carries effect on device response.

The time response of the control and PT PDs was measured with a pico-second pulsed laser with 850 nm wavelength at the 3 regimens of operation: PIN (pink), APD (green), and SPAD (red) (Fig. 5.5 a-b). At 35 V, the SPAD regime, the photon-trapping PDs exhibited a decrease in the FWHM from 99 ps to 40 ps, as well as a faster decay (fall time) from 293 ps to 105 ps of the pulse response. This can be attributed to the efficient delivery of the input light to the high electric field regions and a decrease in absorption in the highly doped regions, where diffusion is the dominant carrier transport method.

Most of the photons absorbed in the doped n and p regions of the photodiodes do not contribute to the photocurrents or EQE due to a lack of electric field in the highly doped p–n contact regions. A small fraction of photogenerated carriers in the photodiode contact regions are collected by the external circuit via the carrier diffusion process and contribute to the overall EQE. For an illumination wavelength of 850 nm, ~1% of the light is absorbed in the top p region. However, when the top contact layer is thinned down from 200 nm to 100 nm, the percentage of absorbed light in the device's intrinsic region would increase by around 10% at shorter wavelengths such as 450 nm. Farther thinning the top contact would augment the sheet resistance, contributing negatively to the bandwidth. We emphasize that the photon-trapping devices can inhibit surface reflection, absorb most photons, and exhibit reduced capacitance, contributing to higher absorption efficiency and high bandwidth. These devices also allow penetration of light to a much deeper level to

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maximize the gain, which is especially important for illumination with short wavelengths such as 450 nm.
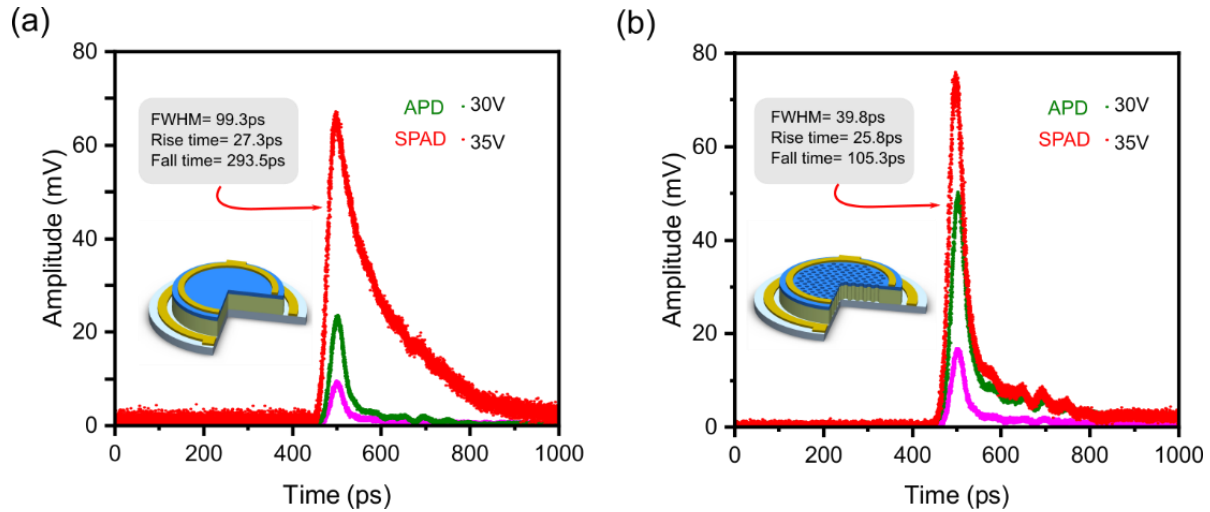
Fig. 5.5. Pulse time response for Si PD. Three regimes of operation: PIN (pink) APD (green) and SPAD (red), for the (a) control and (b) Photon-trapping PD. In the SPAD regime, the photon-trapping PDs exhibited a decrease in the FWHM from 99 ps to 40 ps, as well as a faster decay (fall time) from 293 ps to 105 ps of the pulse response. This can be attributed to the efficient delivery of the input light to the high electric field regions and a decrease of absorption in the highly doped regions.

5.3 Analysis of carrier transport in nanohole based PD

In the previous analysis of transient time response in APD mode, the continuous 850 nm illumination is suddenly turned off and the device output was shown as a function of time for various applied device voltages. The nanohole devices present a higher amplitude of the impulse response and they turn off with smaller tails than flat devices. This behavior can be understood by (1) nanohole devices have a significantly enhanced quantum efficiency and (2) they have much fewer photogenerated minority carriers

(electrons) in the bottom p-layer, which must obey the slow diffusion process and move from the p-layer, through the i-layer, and to the n-layer. Most photons have already been absorbed in the i-layer in nanohole PDs, resulting in much less diffusion minority carriers at the bottom highly doped layer.

To explain the transient behavior in the PD, we use a model like the one shown in Fig. 5.6. The figures on the left show the devices with holes (top) and flat (bottom), while the figure on the right shows the logarithm of normalized incoming photon density $P(x)$ (top) and the absorption probability $A(x)$ as a function of device depth x from the surface. In the flat device, the incoming photon density $P(x)$ decreases slowly; on the other hand, for the photon-trapping device, $P(x)$ quickly decreases up to $-L_{nh}$, and then it slows due to the photon-trapping effect. Consequently, the absorbed photons $A(x)$ decrease slowly in the flat device with an exponential decay α_{nh}, and it decreases quickly in the nanohole region ($\alpha_{nh} >> \alpha_0$) followed by the slow absorption region.

In this model, the top n-layer L_n is very thin ($L_n << 1$ μm), the middle i-layer has a thickness of $L_i \sim 1$ μm, and the bottom p-layer $L_p < 1$ μm.

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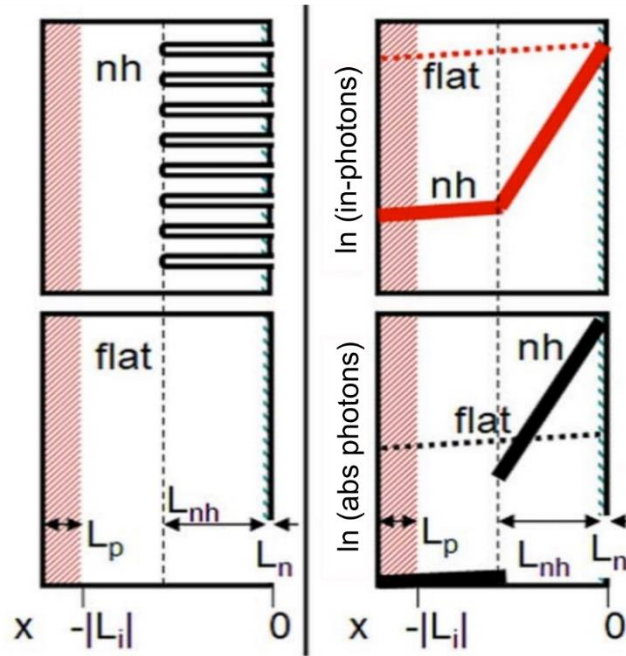
Fig. 5.6. Photon absorption probability in device with no holes and photon-trapping PD.

It can be proved that the nanohole-device carrier density at the bottom of the p-layer is lower than in the flat device, given by the following expression:

$$\frac{A_{nh}(-L_i)L_p}{A_0(-L_i)L_p} = \exp[-(\alpha_{nh} - \alpha_0)L_{nh}] \quad (5.3)$$

Where:

- A_{nh} and A_0 are the absorption probability as a function of device depth.

- L_i and L_p are the layer thickness for the i and p++ region, respectively.

- L_{hn} is the depth of the holes.

- α_{nh} and α_0 are the absorption exponential decay for the photon-trapping and flat device.

The mathematical expression shows that the ratio between carrier densities in the highly doped p region is simply the depth of the nanohole region times the difference in the absorption coefficient between nanohole and flat devices.

The expression shows that the difference in amplitude of the pulse response tail between the nanohole device and the flat device increases, as the difference in the photon absorption in nanohole and flat devices is larger [78].

It is now possible to numerically estimate the amplitude of the tail using our experimental data. We have measured an i-layer thickness L = 1.3 μm and, for the photon wavelength of 850 nm, we have calculated the absorption coefficients as follows: α_{nh}=0.0538/μm α_{n0}=0.4615/μm. Thus, α_{nh}L = 0.07 and α_0L = 0.60.

Then, the tail amplitudes are calculated as follows:

- Nanohole PD long time tail amplitude:

$$exp(\alpha_n(i)L) = exp(-0.60) = 0.54$$

- Flat PD long time tail amplitude:

$$exp(\alpha_F(i)L) = exp(-0.07) = 0.93$$

These calculations suggest that the nanohole devices typically have a factor of ~0.54/ 0.93 = 0.58 smaller long time tail amplitude compared to flat devices. This is consistent with the experimental results.

For APD mode, the higher bias increases the amplitude of the signal at higher rates than in the flat devices. It means that the difference between α_{nh} and α_0 increases, resulting in an even higher ratio between amplitudes of the tail. In other words, the benefits of the holes on the transit time behavior of the PD, increase as we increase the bias voltage to the level of the APD mode.

5.4 Summary

This chapter has demonstrated the temporal impulse response for Si PDs of 30ps FWHM, when operating at unity gain. This was the first time that a Si PD with a high EQE of more than 56% shows such high speed. The enhanced absorption allows designing PDs with thinner absorbing layers, reducing the transit time of the photogenerated carriers without compromising their absorption efficiency.

Photon-trapping structures offer a solution to reduce the junction capacitance that depends on the device area and the depletion layer thickness. This approach reduces the capacitance of a thin PD device by the inherent removal of material from the surface of the device when etching the photon-trapping holes, resulting in the overall reduction of the effective area (A) of the device. The enhancement in absorption also comes with a considerable reduction in device capacitance by more than 35% and thereby an improvement in the time response. The combined effect can collectively help to overcome the trade-off between the efficiency and speed of operation of the PDs. State-of-the-art CMOS fabrication processes could enable near-perfect EQE and above the 50% of

capacitance reduction, by increasing the number of photo-trapping nanoholes integrated into the devices, especially in photodiodes with small surface area, required to operate at high bandwidths.

In APD and SPAD regimes, the photon-trapping PDs exhibited a decrease in the FWHM from 99 ps to 40 ps, as well as a faster decay (fall time) from 293 ps to 105 ps of the pulse response. This can be attributed to the efficient delivery of the input light to the high electric field regions and a decrease in absorption in the highly doped regions, where diffusion is the dominant carrier transport method. The carrier density model presented helped to explain such improvement in the time response. The shorter tail observed in the pulse time responses in APD and SPAD mode suggests that is possible to design APDs with faster recovery times, critical for faster optical communication links and photon timing resolutions in the case of imaging technologies.

Chapter 6

Single photon avalanche photodetectors

A single-photon Avalanche Photodetector is an APD biased above the breakdown voltage, also called Geiger mode, where a high gain should be obtained (10^6). Key figures of Merit in SPADs as Photon Detection Efficiency (PDE), Dark Count Rate (DCR), and time response are dependable on the excess bias applied ($V_{excess}=V_{applied}$ - $V_{Breakdown}$). A higher PDE is expected as the EQE is enhanced, without increasing the DCR considerably [79], Achieving a high PDE with lower excess bias, can potentially reduce the Dark Count Rate and will minimize the FWHM. As our previous APD measurements show, our PDs will have a breakdown voltage of 34V. With the enhancement in absorption, no high excess voltage will be required to achieve a high PDE, minimizing the impact on DCR and time jitter.

High-performance photon-trapping SPADs need three elements:

i.   Increase the PDE and multiplication gain.

ii. Increase the speed of operation with a thinner silicon layer for faster carrier collection

iii. Implement a quenching circuit

We developed a simulation package that allowed us to optimize the design of photon-trapping structures to achieve up to 90% of absorption at 450 nm wavelength for a thin silicon layer of 1.2 µm. The combination of these absorption results with the fast speed of operation obtained by reducing the thickness of the device, and an optimized doping profile can contribute to the development of ultra-fast photodetectors with higher gain and photon detection efficiency.

This chapter will describe the steps followed to maximize the absorption efficiency of silicon with a thin layer of 1.2µm for short wavelengths. Then we will study penetration depth at a different wavelength and describe the doping profile required to achieve a gain in the PDs. We finalize the chapter describing the new structure designed and fabricated for ultrafast SPAD, where our findings for maximizing absorption efficiency and speed are applied.

6.1 Simulation study for SPADs for ultrafast operation and high PDE

PDE is defined as the probability that a photon incident in the active area of the detector generates enough avalanche to be registered. The PDE is proportional to the EQE, and its enhancement is a clear signal of the improvements achieved for SPADs.

A series of optical and electrical simulations were performed to further optimize the design of photon-trapping structures, with the aim to design Single Photon Avalanche Photodetectors (PT SPADs) that could enable ultrafast operation in the shorter wavelength of the visible range without compromising their sensitivity. In our proposed device, a silicon thickness of 1.2 µm was chosen to achieve low jitter time. A conventional

device (control) with such a thin layer would be able to absorb only 51% of optical power at 450 nm wavelength, with most of the light being absorbed in the first 300 nm of depth, as FDTD simulations show in Fig. 6.1(a). However, our results suggest that more than 90% of photon absorption can be achieved in such a thin layer with optimized photon-trapping structures when a proper diameter and period are implemented in the photodetectors. Fig. 6.1(b) shows the side and top view of a simulated PT SPAD, suggesting a shift in the absorption with an enhancement peak at 400 nm depth just below the depth of the nanoholes.

Herein, we have studied the impact of design variations in period, diameter, and depth of cylindrical holes through FDTD simulation. Such simulations allowed us to construct Fig. 6.1 (c), where the expected absorption for different diameters and periods, with a depth of 400 nm is presented. As observed in Fig. 6.1(c), the absorption efficiency shows a higher enhancement when the diameter of photon-trapping structures approaches the period length between them, with a maximum of 90% absorption.
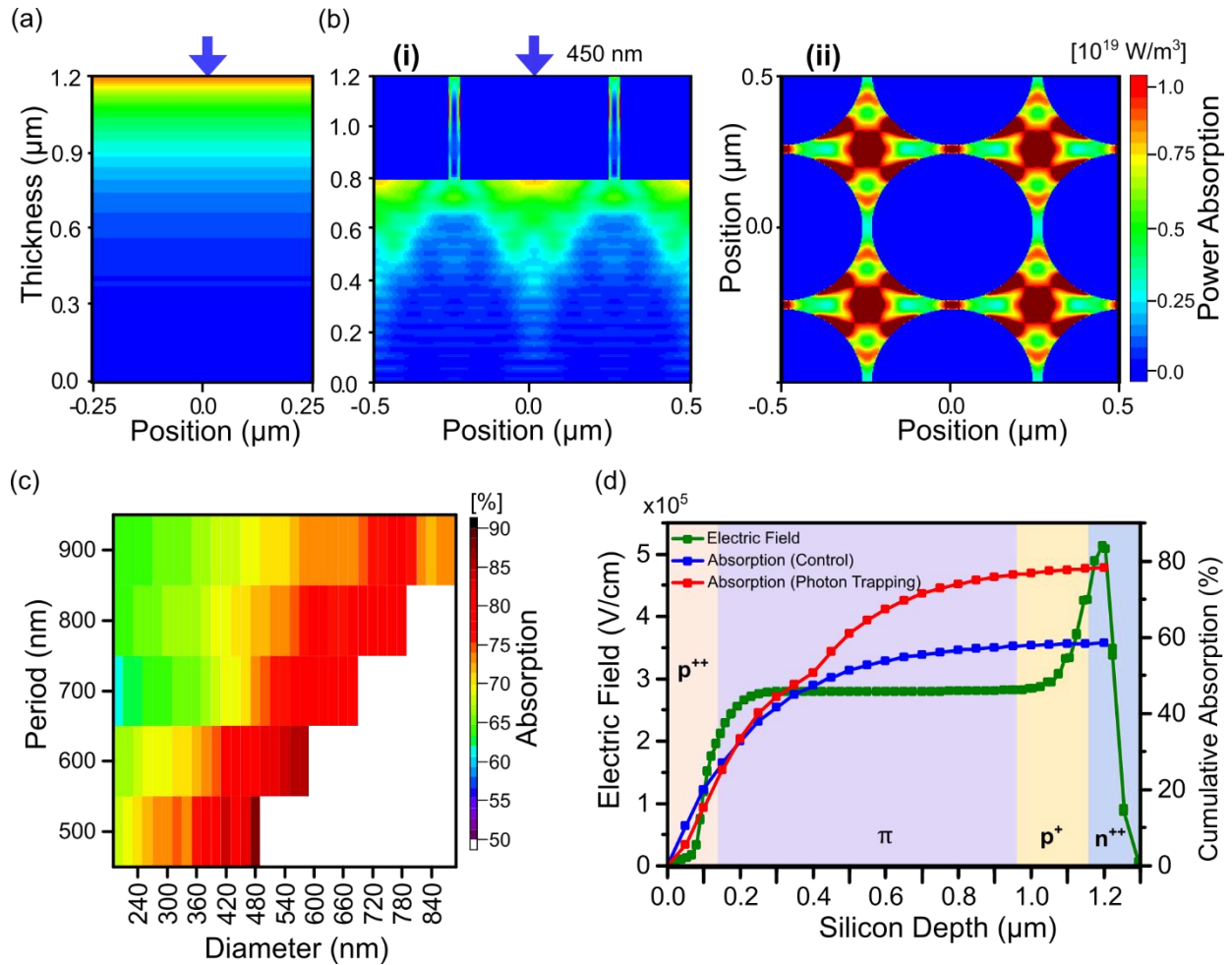
Fig. 6.1. Absorption control in ultra-thin photon-trapping PD at 450 nm wavelength. Comparison of absorption profile in (a) control device and (b) PT device. (c) Optimization of nanohole period and diameter at 450 nm wavelength. (d) Absorption at different depths in the semiconductor and electric field profile in APD.

Fig. 6.1. Absorption control in photon-trapping PD at 450 nm wavelength. Simulated power absorption profile of (a) control and (b) photon-trapping PD with 1.2 µm thick silicon. Our photon-trapping PDs with such a thin absorber layer exhibit more than 90% absorption. (c) Influence of period and diameter of the photon-trapping nanostructures in power absorption at 450 nm wavelength. (d) Cumulative absorption in control (blue) and PT (red) silicon SPAD. Overlap of

electric field profile of a PD with a *pπpn* structure with the absorption of light for optical generation, for higher gain and lower noise avalanche-based PD.

Fig. 6.1d shows the cumulative absorption obtained for the control (blue) and the PT SPAD device (red), in steps of 50 nm. In the first 100 nm depth, the high absorption observed in the control PD is reduced to almost 50%. Then, between the 400 nm and 500 nm depth, the absorption of power in a PT SPAD is increased by 3 times, compared with the control SPAD. This illustrates a reduction in optical power absorption close to the surface with the enhancement of absorption deeper in the device. With a proper electric field profile (green) that allows separating the absorption and the multiplication regions, more electrons can be injected into the multiplication region, promoting higher gain and lower amplification noise.

The higher absorption efficiency achieved in the silicon-photon-trapping APDs at visible and near-infrared wavelengths allows for designing devices with thinner absorption layers. Such a reduction in thickness comes with a reduction in the breakdown voltage [80]. The breakdown voltage of our fabricated device with 2.5 μm of thickness is around 30V and electrical simulations performed on the device proposed with 1.2 μm of thickness, suggest a breakdown voltage of less than 20V. We envision a reduced voltage below 10V as a possibility in our devices with a thinner active layer.

An advantage of our photon-trapping structures with respect to other absorption enhancement methods is its effect across a broad range of wavelengths, critical for

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biomedical imaging technologies. Fig. 6.2a shows the higher absorption obtained in photodetectors with photon-trapping structures from 400 to 800 nm. At 450 nm wavelength, the absorption increases as the hole diameter of the structure reach close to the period within the structures. Different photon-trapping structures can also be implemented, such as inverted pyramids or cylindrical holes. The simulated absorption of these structures reveals a higher absorption in the inverted pyramid profile from 400 to 600 nm wavelength (Fig. 6.2b). In addition, in this range of wavelengths, a more constant absorption value is observed in the inverted pyramid structure. Engineering photon-trapping structures in semiconductor-based photodetectors can benefit many biomedical applications that rely on the detection of optical photons with a broad distribution of wavelengths.
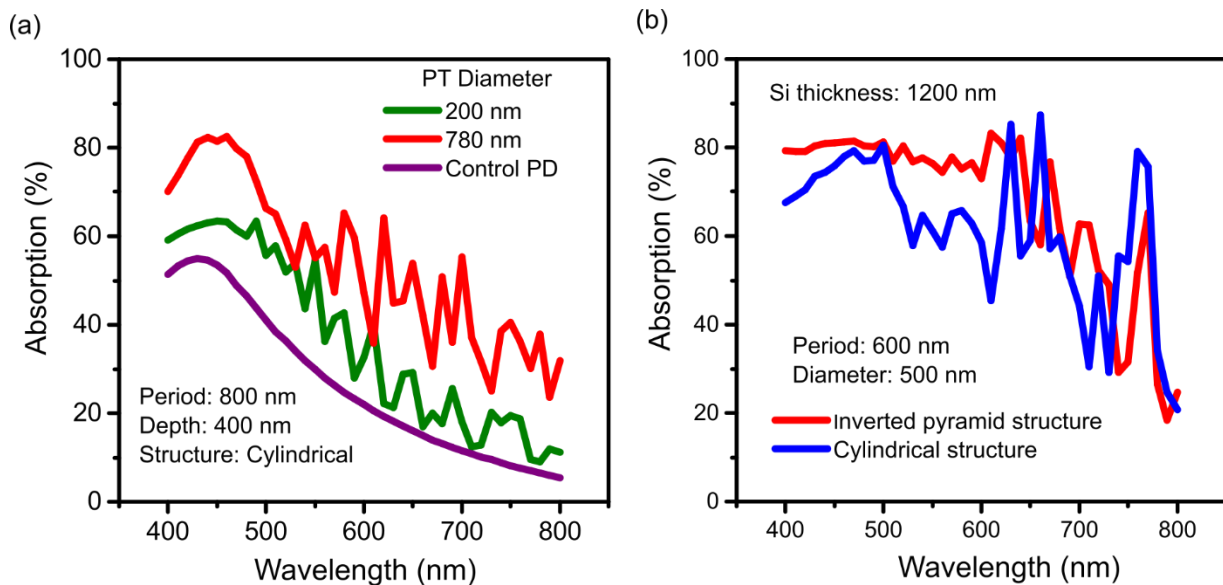
Fig. 6.2. Broadband absorption in ultra-thin PT PD. (a)Influence of diameter in cylindrical photon-trapping structure at a broadband range of wavelengths. (b) Comparison of absorption at a broadband range of wavelengths between cylindrical and inverted pyramid structures.

6.2 Engineering of penetration depth for high gain-bandwidth SPADs

In Chapter 5 we showed how the penetration depth influenced the multiplication gain at short and near-infrared wavelengths, by engineering the penetration depth and modifying the gain obtained in an APD. Furthermore, the bandwidth of photodetectors was enhanced by reducing the transit time of the photogenerated carriers.

A series of simulations have been performed in Si PDs with absorbing layers of only 1.2 μm-thickness, to understand the influence of the nanohole depth and the change of incident wavelengths in the penetration depth. The impact of nanohole depth on the penetration depth was studied by varying its depth between 0 nm (conventional PD) to up to 1200 nm. For this study, an incident wavelength of 450 nm illuminated the PD, with an incident angle normal to the surface of the device. Cylindrical holes, with 480 nm diameter (d) and 500 nm period (p) are used in this study. The power absorption with respect to depth is calculated for each 50nm segment along with the depth. Fig. 6.3a shows that the penetration depth increases from 0.25 μm in the conventional PD to a maximum of 0.63 μm when cylindrical holes are etched with 1200 nm depth. However, etching the nanoholes can also reduce the absorption and increase the transmission of the light, making it necessary to optimize the etching depth. Fig. 6.3b shows that the maximum absorption and penetration depth for this design is obtained with a nanohole depth of 800 nm where 84% of the light is absorbed, and the penetration depth is 0.54 μm.

At 450nm wavelength, silicon exhibits a high absorption coefficient, but it also reflects 40% of the incident light. With the integrated nanohole approach, the reflection is reduced to around 10% at this short wavelength. Fig. 6.3c shows the power distribution of the 450nm wavelength light in the engineered PDs with different nanohole depths.
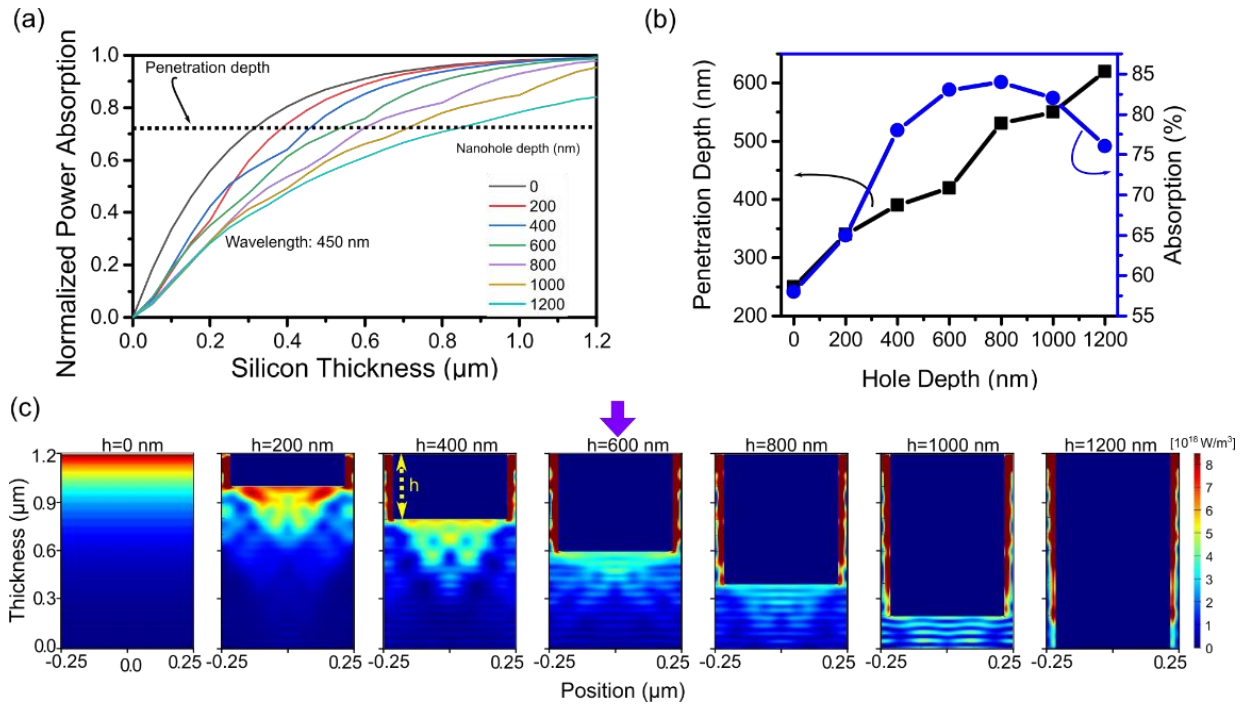
Fig. 6.3. Penetration depth analysis at 450nm wavelength. (a) Penetration depth of 450 nm wavelength varying photon-trapping nanohole depths. The penetration depth increases with the depth of the hole from 250 nm to 620 nm. (b) Absorption and penetration depth for different hole depths at 450 nm wavelength. A maximum of 84% of absorption can be obtained at 800 nm nanohole depth. (c) Optical absorption profile obtained by FDTD for an incident light of 450 nm.

A broad range of applications works at visible wavelengths, making it important to study the change in penetration depth inside of silicon for different input wavelengths from 300nm to 850nm when implementing the nanoholes in silicon. We fixed the depth of the

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nanohole at 400 nm and kept the diameter and the period unchanged (480nm diameter and 500 nm period).

Fig. 6.4a shows the normalized power absorption for different wavelengths in the engineered PD with respect to its thickness. These curves are used to calculate their respective penetration depth. Fig. 6.4(b) compares the penetration depth of conventional devices and the engineered PDs. For wavelengths below 450 nm, our simulations show that a greater penetration depth is achieved (Fig. 6.4b, inset). On the other hand, from 500nm to 850 nm wavelength, the increase in absorption achieved with nanoholes allows decreasing the penetration depth to a range between 0.55 µm to 2.3 µm. Clearly, shorter wavelengths (such as 400 nm) are observed to penetrate deeper into silicon. On the other hand, photons with longer wavelengths (such as 850 nm) are forced to propagate to shallower depths. Fig. 6.4c represents the different distribution of light absorbed in the conventional silicon PD and the engineered PD, for 450nm wavelengths.
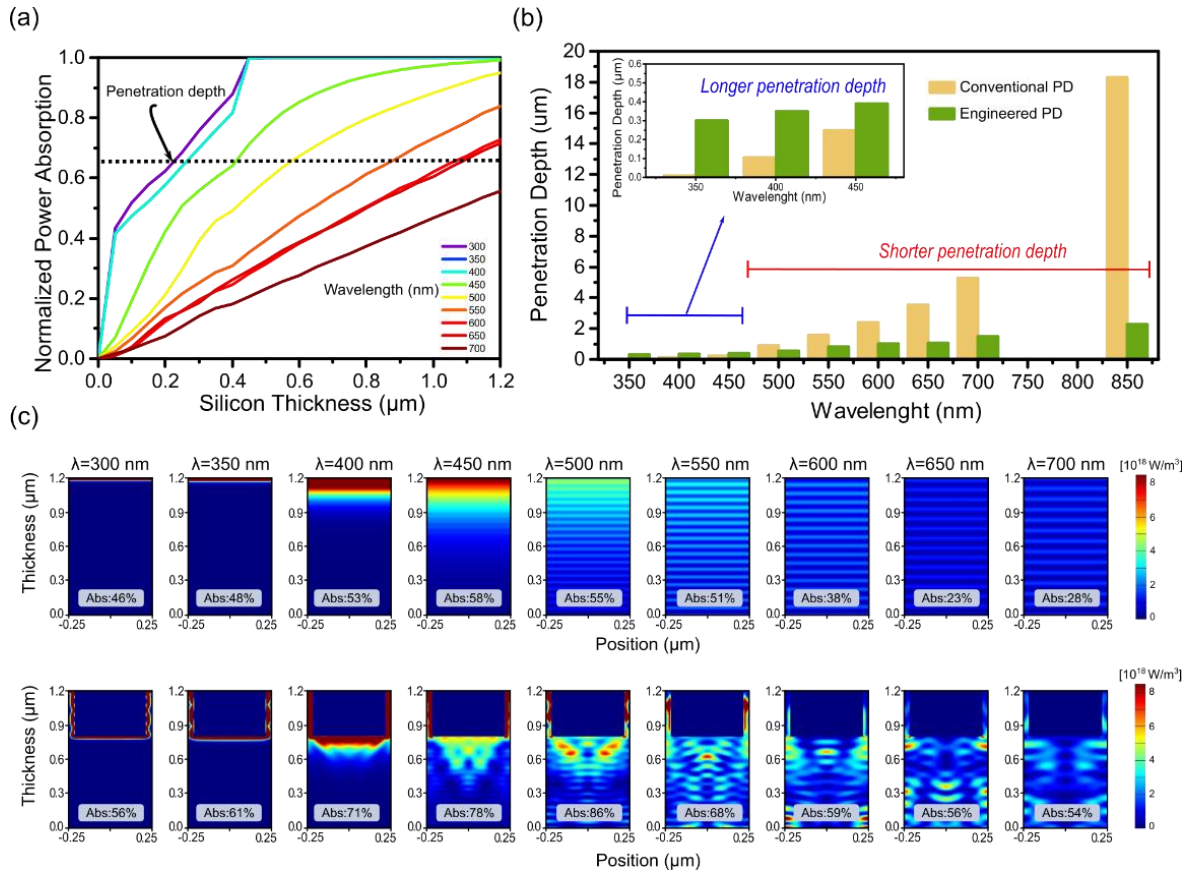
Fig. 6.4. Broadband penetration depth control. (a) Penetration depth engineered on silicon for incident light wavelengths between 300 nm to 700 nm. (b) Comparison of penetration depth between conventional and engineered PDs. At wavelengths below 450nm, the penetration depth is dramatically increased, reducing the loss of carriers by recombination, slow diffusion transport, and high excess noise multiplication. Above 500nm wavelength, the penetration depth is reduced by more than 50%. At 850 nm the penetration depth is reduced from 18.3 μm to only 2.3 μm, an 87% reduction in the depth. (c) The power distribution of incident light at different wavelengths on conventional and photon-trapping photodiodes for nanoholes depth of 400 nm, a diameter of 480 nm, and a period of 500 nm.

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6.3 Coupled optical and electrical simulations for new SPADs

To increase the multiplication, gain a doping structure with a Separate Absorption and Multiplication of Carriers (SAMC) is designed to separate the electron-hole pairs and allow that only electrons to be injected into the multiplication region, where a high electric field promotes the impact ionization and generate a higher multiplication gain without increasing the excess noise factor considerably. For a SPAD optimized for NIR wavelengths, an NpπP structure is preferred, since its higher penetration depth of this wavelength range matches the absorbing layer at the bottom of the device, allowing efficient separation of carriers (Fig. 6.5a). However, the same design process can be used for devices operating at short and visible wavelengths.

Our device is designed with a maximum thickness of 1.2 µm to reduce the transit time of the carriers and achieve higher bandwidth. The IV curves for dark current and photocurrent are described in Fig. 6.5b. For this simulation, an input light of 850 nm and with an optical power of 10 µW is considered. The dark current is in the order of pA but a simplified model was used to avoid a complex simulation. The Photocurrent is in the order of µA but it is expected to obtain a higher current with the implementation of the photon-trapping structures. The IV curves also show a breakdown voltage (V_{Br}) of ~22V. The electric field profile is described in Fig. 6.5c and d. The doping profile selected allows obtaining an electric field below the 3×10^5 V*cm (dotted line) to avoid multiplication in this region. The high electric field is located in the first 500 nm of depth with an electric field strong enough to create the multiplication of carriers. This structure has a high probability

of avalanche by electron, which is desired due to its high probability of avalanche (high

k-value). Finally, Fig. 6.5e shows an estimated a PDE of 80% at an excess bias of 8V

(above the breakdown voltage V_{br})
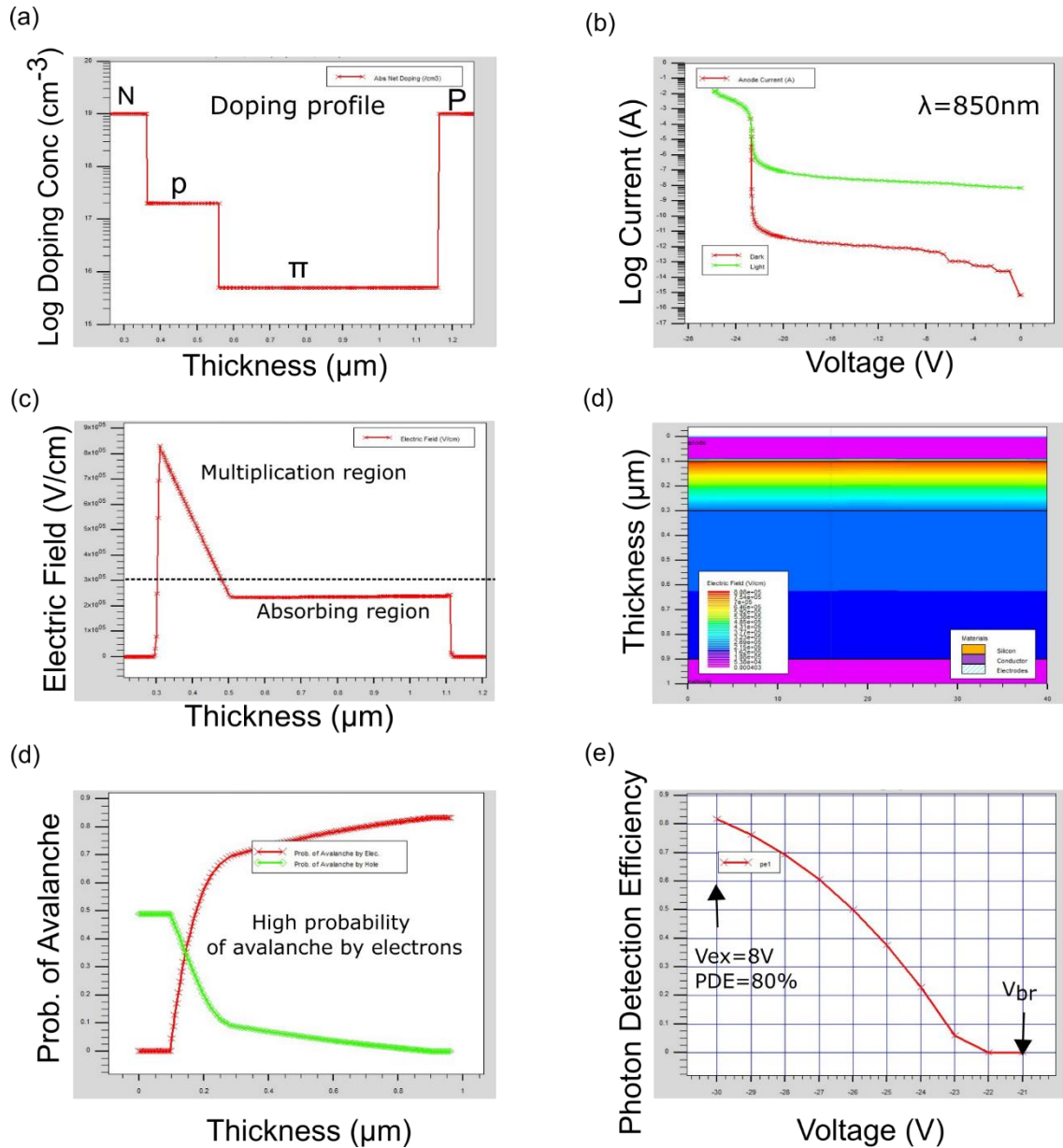
Fig. 6.5. Coupled Electrical and Optical Simulations for New SPADs. (a) Doping profile for a
NpπP structure. (b) Dark current and photocurrent for an input light of 850 nm wavelength. (c)

Electric field profile with SAML structure. (d) Electric field distribution. (e) Probability of avalanche by electrons and holes. (e) Estimated PDE of 80% at an excess bias of 8V.

6.4 Fabrication of new SPADs high multiplication gain and time response.

Based on the optical and electrical simulations presented we proceed with the growth of silicon wafers on SOI with the doping profile required for short and long wavelengths.

Two different epitaxial layers configuration have been fabricated denominated as PT-NIR and PT-VIS:

PT-NIR: Consist of an NpπP stack (Fig. 6.6a). The P and N layers (1e19cm^{-3}) are highly doped to reduce their resistivity and promote the creation of ohmic contacts. The p-layer (2e17cm^{-3}) is used to create the electric high electric field at the top of the PD, while the π-layer (1e15cm^{-3}) with a thickness of 800 nm is used as the absorbing layer.

In this structure, the multiplication region is at top of the PD. This is the typical structure of layers in CMOS processes, where the N layer is added at the end of the doping by diffusion of dopants (Fig. 6.6a).

PT-VIS. Consists of a PπpN stack (Fig. 6.7a). Here, the high electric field, multiplication region is expected to be at the bottom of the PD (Fig. 6.7b). The lower electric field at the top of the surface allows an efficient separation of the electron-hole pairs before the carriers reach the multiplication region. Such structure is expected the have less multiplication noise than the PT-NIR for short and visible wavelengths (Fig. 6.7). This is a custom design with a doping layer different from the generally used for this range of wavelengths. The advantage of this structure is that despite being optimized by short and

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visible wavelengths, NIR wavelengths can also be benefited by compressing the propagation depth to less than 1.2 μm. In addition, the high multiplication region does not interact with the nanoholes, which can potentially distort the carrier multiplication.

PT-NIR SPAD
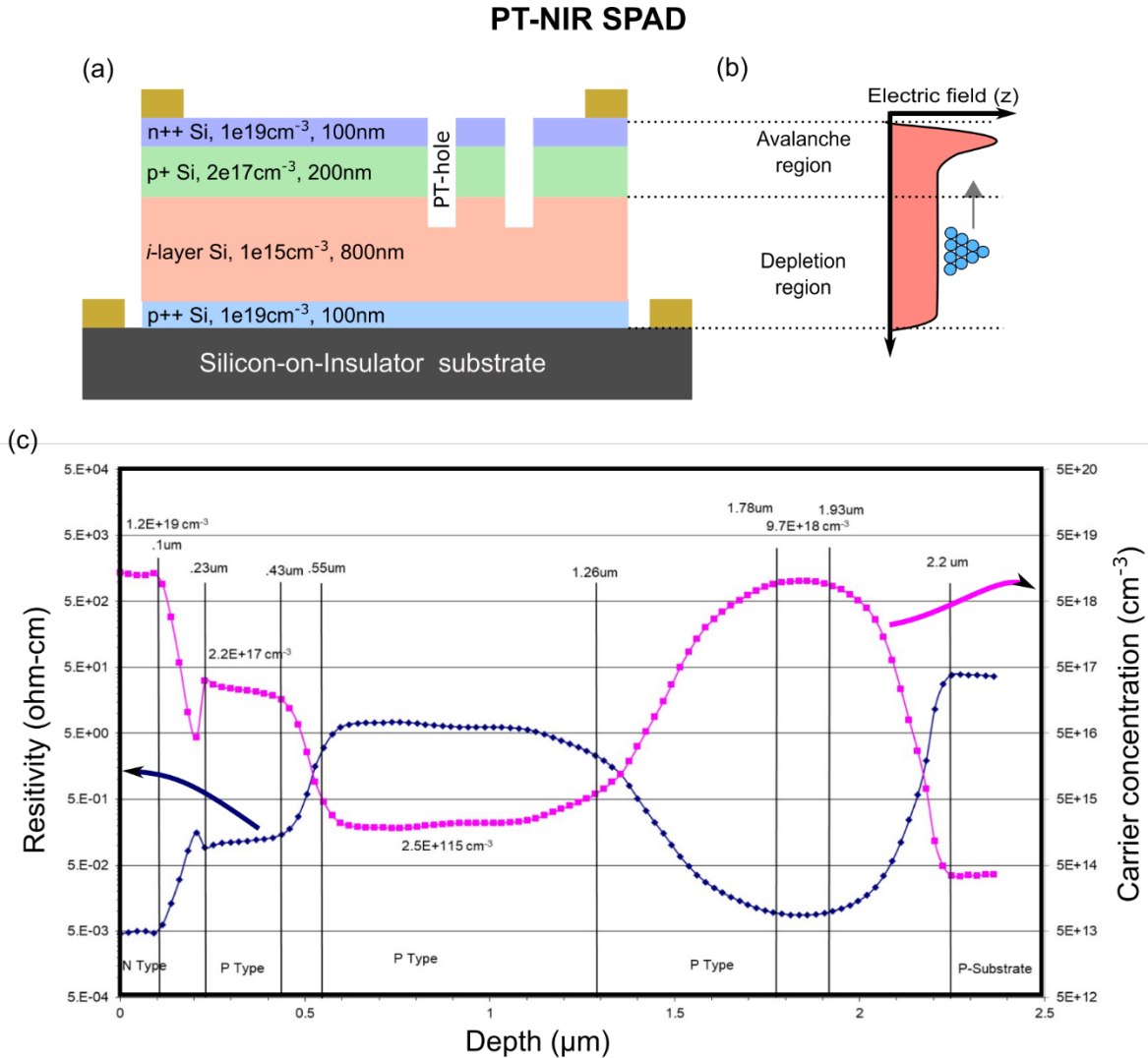
Fig. 6.6. New red enhanced APD design. (a)Doping profile design for SPADs with 1.2 μm absorbing layer. (b)Electric field profile. (c)SIMS measurement of fabricated epitaxial layers.

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The designed devices were epitaxially grown on p-type SOI wafers with a diameter of 150mm, orientation <100> and with a thickness of 600 µm. Using Spreading Resistance Profilometry (SRP) it was possible to determine the active carrier concentration and resistivity of the poly film while Fourier-Transform Infrared Spectroscopy (FTIR) was used to determine the growth rate and cross-wafer thickness uniformity of the epi growth (Fig. 6.6c and Fig. 6.7c). Considering the transition made to reach the desired doping layer, the total thickness of the PD is 2 µm for the PT-NIR and ~2.5 µm for the PT-VIS structure.
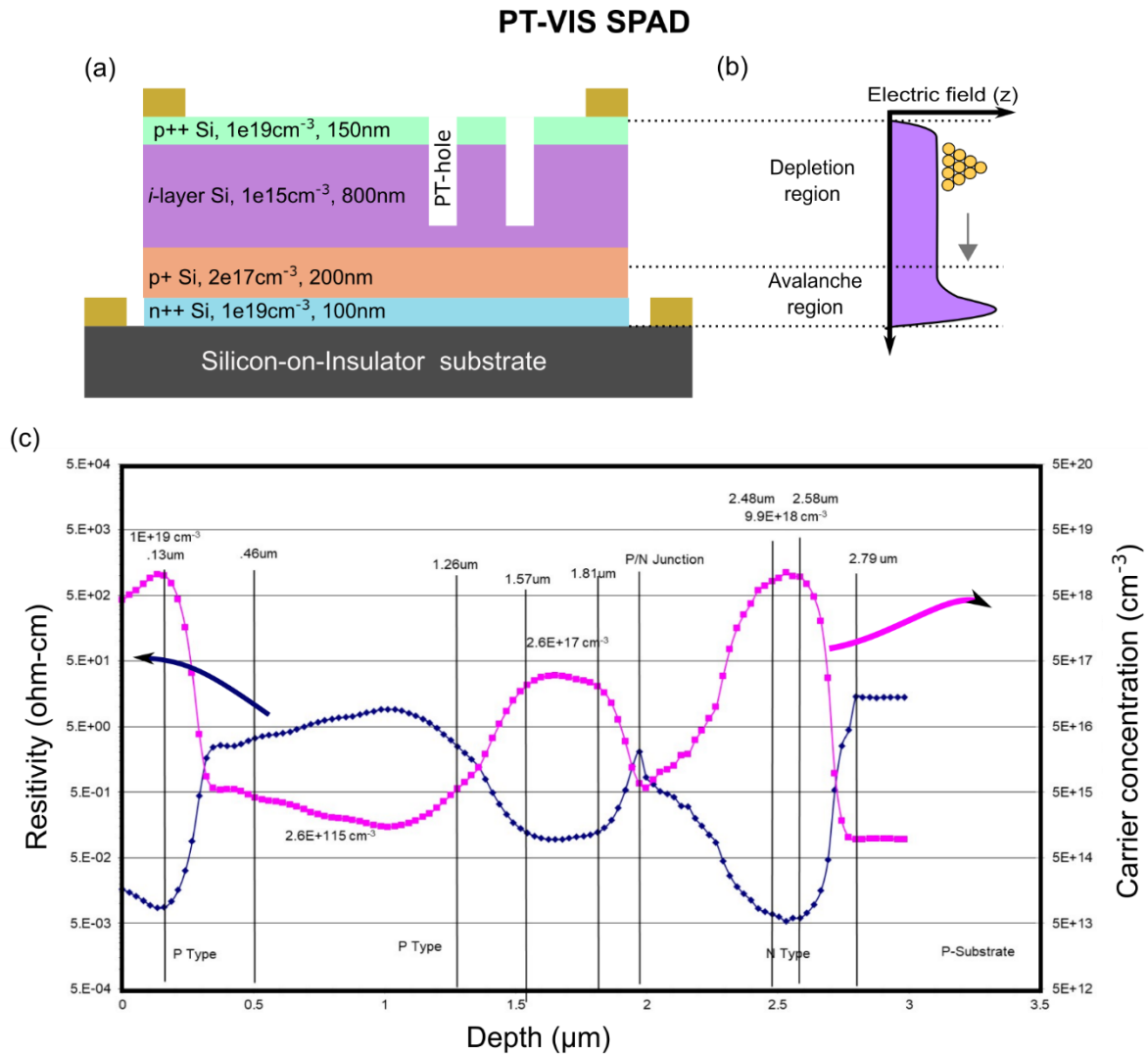
Fig. 6.7. New visible enhanced APD design. (a)Doping profile design for SPADs with 1.2 µm absorbing layer. (b)Electric field profile. (c)SIMS measurement of fabricated epitaxial layers.

6.5 Implementation of quenching circuits

The circuit that quenches the avalanche, resetting the bias voltage a level below the breakdown, plays a key role in the SPAD performance. These quenching circuits can be divided into two types: passive and active quenching circuits.

Passive Quenching Circuits (PQC) were first implemented in single SPAD devices and are highly used for SPAD arrays. The bias voltage is applied through a high-value resistor R_L while a small resistor R_s is connected to the other terminal to observe the current pulse. Photon-counting measurements can be accurately performed only if the total count rate is low enough to make count losses negligible and correction unnecessary. Despite the drawbacks, this quenching resistor is highly employed for arrays of SPADs. As Fig. 6.8 shows a polysilicon-based resistor on top of the active area of the SPAD produces the quenching behavior in each SPAD. The monolithic integration of this resistor reduced the capacitance and the rest transition time get below 1µs.

Active quenching circuits (AQC) solve many of the drawbacks of PQC. These quenching circuits sense the rise of the avalanche and react back, forcing short quench and reset transitions with a controlled bias source. For the present project, an integrated quenching resistor with a value of 500kΩ will be fabricated on top of the SPAD.
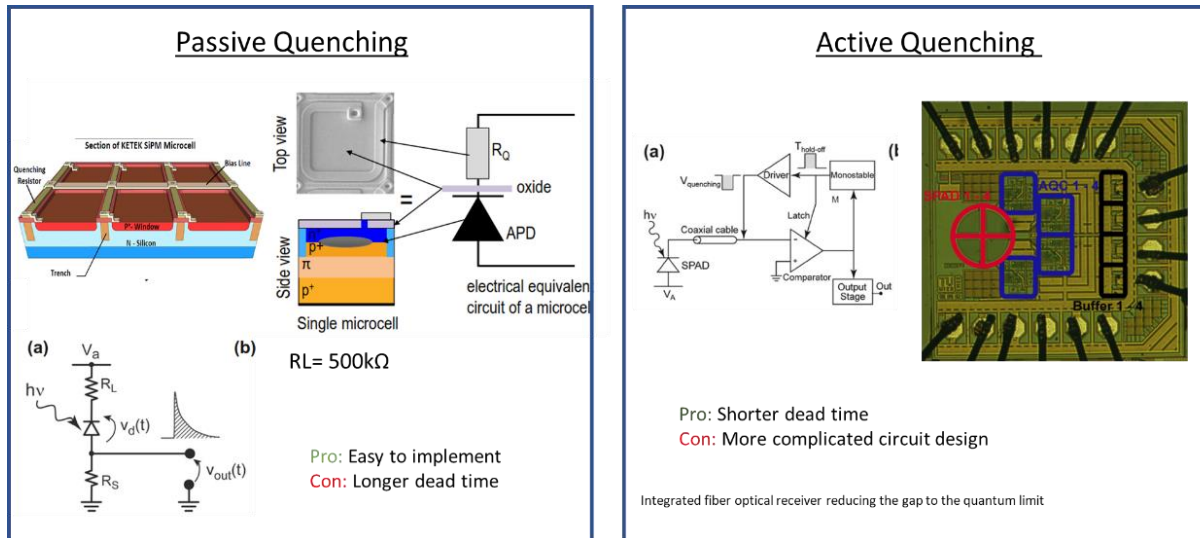
Fig. 6.8. Passive and active quenching circuit.

6.6 Summary

In this chapter, we have used of knowledge acquired in previous chapters to design and fabricate a new generation of Si APDs with ultra-thin absorbing layers of only 1.2um. One optimized for Visible wavelengths (PT-VIS) and another one for Near-Infrared Wavelengths (PT-NIR). With the implementation of our optimization tools, it is shown that at 450 nm, 90% of optical absorption can be obtained with the implementation of the proper photon-trapping structures. With the addition of absorption improvement at NIR wavelengths. These new devices can obtain an enhancement in Photon Detection Efficiency. To maximize their gain, two methods are implemented: (i) design a doping profile using the Separate Absorption and Multiplication layers, allowing for separating the carriers before multiplication, reducing the noise, and increasing the multiplication; (ii) Control the penetration depth for the incident electromagnetic waves. This allows

generating carriers in critical regions of the semiconductor that minimize their time transit time to the multiplication region and contacts.

These PDs are being fabricated and their characterization will determine their performance.

Chapter 7

Germanium-on-silicon photodiodes with photon-trapping structures for NIR wavelengths applications

Applications such as quantum communications[81], eye-safe lidar systems [82], and photonic biosensors [83], require detectors operated in the near-infrared, particularly at 1310 or 1550 nm, taking advantage of the low-loss windows of optical fibers and low scattering of light at those wavelengths in the atmosphere and tissue, respectively. Commercially available optical receivers often contain photodiodes (PDs) based on III–V materials such as InGaAs/InP. However, these materials are not compatible with CMOS technology and would incur additional costs for wafer bonding, packaging, yield, thermal management, etc. Germanium-on-silicon Photodetectors has the advantage to be compatible with CMOS fabrication technologies and Silicon Photonics Platforms, allowing to create monolithic receivers [19, 84-86]. Despite the 4% lattice mismatch between silicon and Ge, the development of PDs with this material are highly attractive, especially for their integration in Photonic Integrated Circuits (PICs)

Here we focus on the absorption and bandwidth enhancement of Germanium-on-silicon Photodetectors; this work is the first step toward the development of Ge-on-Si Single-

Photon Avalanche Photodetectors where Ge can be used as the absorbing layer and Silicon can be used as the multiplication layer.

7.1 Design and simulation

The *pin* layers of Ge photodiodes were epitaxially grown on a Si substrate. A 2 μm thick intrinsic Ge layer is sandwiched between a high phosphorus-doped (10^{19} cm^{-3}) Si n-type contact layer and a high boron-doped (10^{20} cm^{-3}) Ge p-type layer (both contact layers are designed to be 0.2 μm thick), as shown in Fig. 7.1a The contact layers are highly doped to reduce the minority carriers' lifetime outside the space charge region and minimize their diffusion. The intrinsic Ge layer is kept relatively thin to be able to minimize the transit time of photogenerated electrons and holes, thus making the PD operate at a high speed. These doping profiles are corroborated by Secondary ion mass spectrometry (SIMS) measurements (Fig. 7.1b).
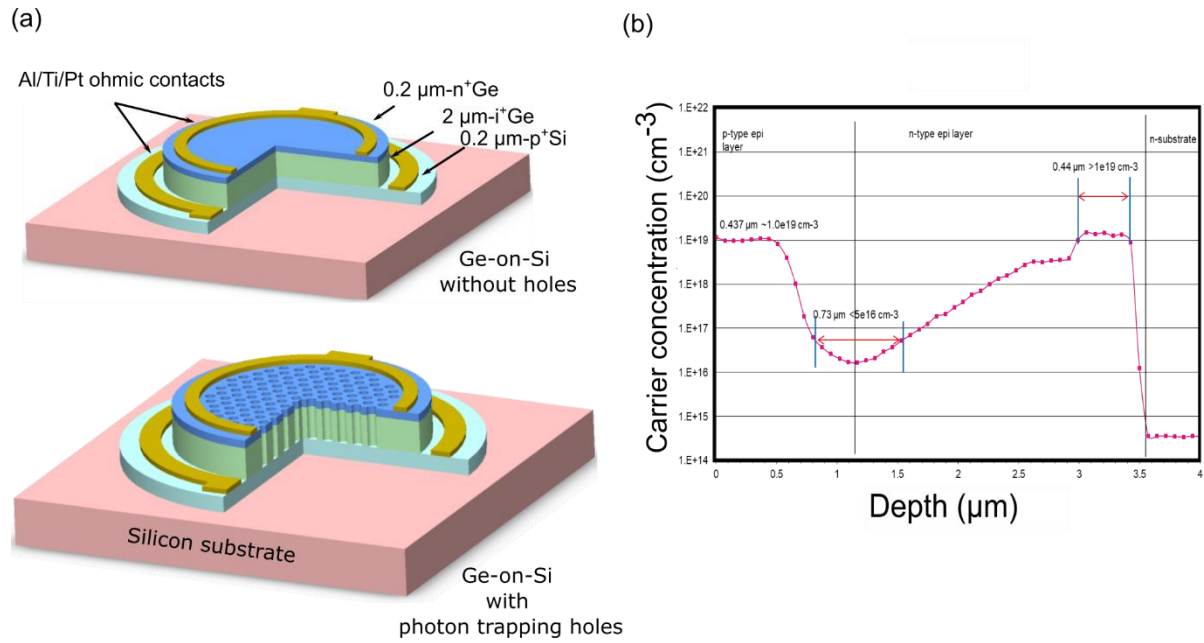
Fig. 7.1. Schematics of Ge/Si PD active layers. Ge-on-Si with (a)No holes and (b) with photon-trapping holes. The Ge-on-Si PD is composed of 0.2 μm p⁺Ge, 2 μm i-Ge, and 0.2 μm n⁺Si layers. The yellow rings are the Al/Ti/Pt ohmic contacts.

FDTD simulations confirm that the light trapping effect is also present in this Ge-on-Si device. A conventional device with no hole is also shown to illustrate the difference in light propagation (Fig. 7.2).
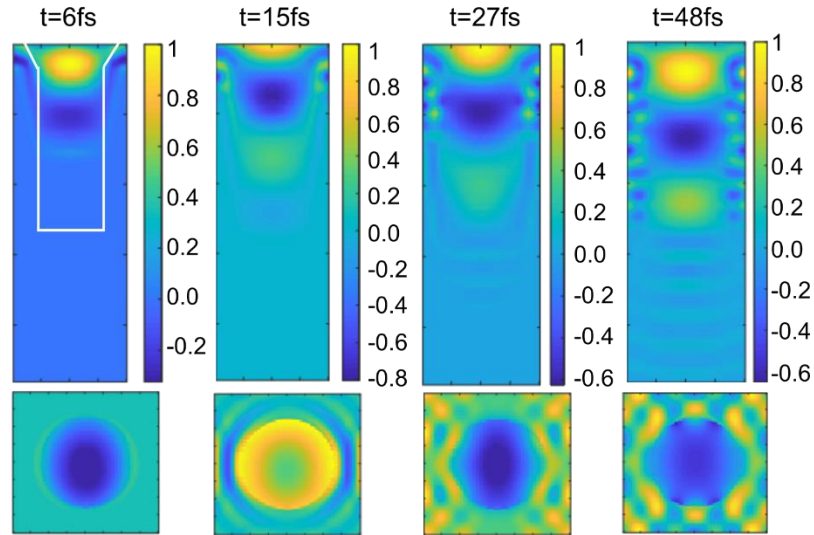
Fig. 7.2. FDTD simulation of light propagation on Ge-on-Si film with and without photon-trapping structures.

7.2 Epitaxial growth and strain measurements of germanium-on-silicon

In this design, the n-type Si epi layer was first grown on the Si substrate at 950°C using epitaxial Chemical Vapor Deposition (CVD). The heteroepitaxy of Ge on Si was initialized by a low-temperature deposited Ge seed layer at 400°C with the aim to minimize the dislocation densities at the Ge/Si interfaces [87, 88]. Then, the temperature was raised to 700°C to grow the intrinsic and p-type Ge epi layers. Because of the different Coefficient of Thermal Expansions (CTEs) between Ge and the Si substrate, a tensile strain can be formed in the Ge film upon cooling from the growth temperature to room temperature [89-91]

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The strain in the Ge layers was characterized by high-resolution XRD (HRXRD), a technique used for the characterization of epitaxial layers in compound semiconductors. Fig. 7.3 depicts the HRXRD (004) θ - 2θ scan of the P-I-N Ge epi layers on Si substrate as compared to the bulk Ge as a reference. The XRD peak for Ge shifts from 65.994° to 66.12°. Using the relationship and calculation of the lateral and vertical lattice constant described in Ref. [92], the strain in the Ge film is estimated to be 0.23%, which is close to the values reported in previous studies [93-95] using similar growth conditions.
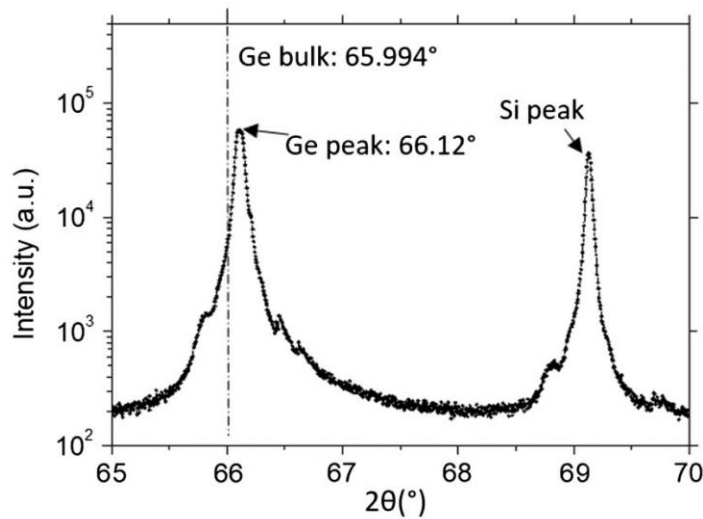
Fig. 7.3. HRXRD (004) θ - 2θ scan of Ge epi layers on Si substrate. The dashed line represents the peak of bulk Ge as a reference.

7.3 Device fabrication

Holes were etched using the Reactive Ion Etching (RIE) technique to create holes with a funnel shape profile. As previously shown for silicon PDs, the tapering angle can help to reduce reflection and improve the quantum efficiency of the PDs. Metal layer stacks

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composed of 100 nm Al, 10 nm Ti, and 30 nm Pt were deposited sequentially on p-mesa and n-mesa by sputtering, followed by a lift-off process. Ohmic contacts between the metal and semiconductors were formed by rapid thermal processing (RTP) at 465°C for 30s in a forming gas (H_2 / N_2) environment. Next, an additional layer of polyimide (3 μm thick) was used for planarization as well as for reducing the parasitic capacitance of coplanar waveguides (CPWs). Last, CPWs composed of 10 nm Ti and 300 nm Al were sputtered followed by a lift-off process (Fig. 7.4).

(a)   (b)
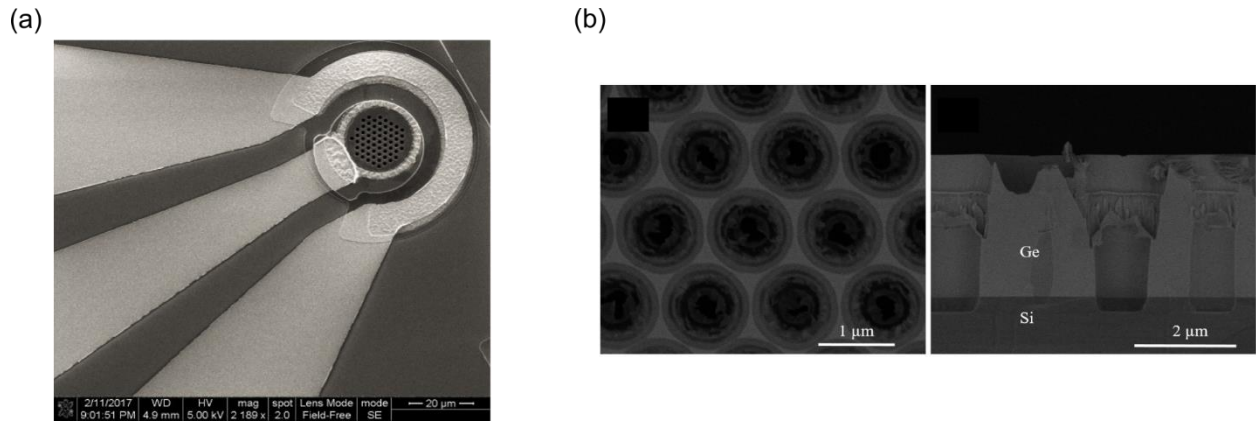
Fig. 7.4. Ge on Si PD with photon-trapping structures. SEM of top and cross-section views clearly showing the interface between the silicon substrate and Ge.

7.4 Optical and DC electrical characterization

7.4.1 External quantum efficiency

The EQEs of Ge-on-Si PDs with funnel-shaped photon-trapping holes (diameter, 1150 nm; period, 1750 nm; hexagonal lattice) was measured between the wavelengths of 1200 and 1800 nm. In addition, PDs without holes were also characterized for comparison. Since for Germanium, the target wavelength is larger than for silicon, the diameter of holes that has given us better results has increased to 1150 nm with a period of 1750 nm, these hole arrays have been used as the optimum design for our Germanium PDs.

Fig. 7.5a shows the measured EQE and absorption in the i-layer calculated by FDTD simulations in a wavelength range of 1200 to 1800 nm. The enhancement in the EQE of the Ge on SI PDS with photon-trapping holes is noticeable in both data communications wavelengths (1300 nm and 1550 nm). An 80% EQE is achieved at 1300 nm wavelength, whereas a PD without holes provides 65% EQE. A similar trend is observed at a wavelength of 1550 nm, where the EQE is improved from 43% to 73% by photon-trapping holes. This enhancement is present over the entire broadband of wavelengths studied (Fig. 7.5b). Analyzing the responsivity of our Ge on SI PDs, at 1550 nm input wavelength,

the responsivity is improved from 0.6 A/W to 0.91 A/W, representing a 50% improvement.
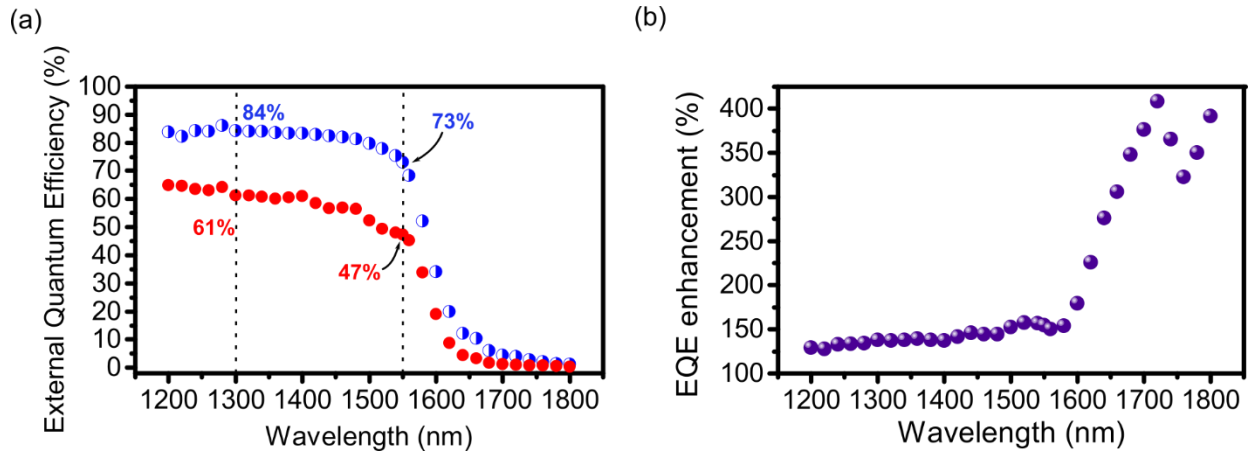
Fig. 7.5. EQE of Ge on Si photodetectors. a) Quantum efficiency from 1200 nm to 1800 nm of Ge on Si photodetectors with and without photon-trapping structures. b) EQE enhancement.

Fig. 7.6 represents the measured EQEs at 1550 nm wavelength from various hole designs. PDs with larger holes seem to have better EQEs at the wavelength of 1550 nm, which is different from our Si PDs at visible wavelengths, where smaller holes perform better.
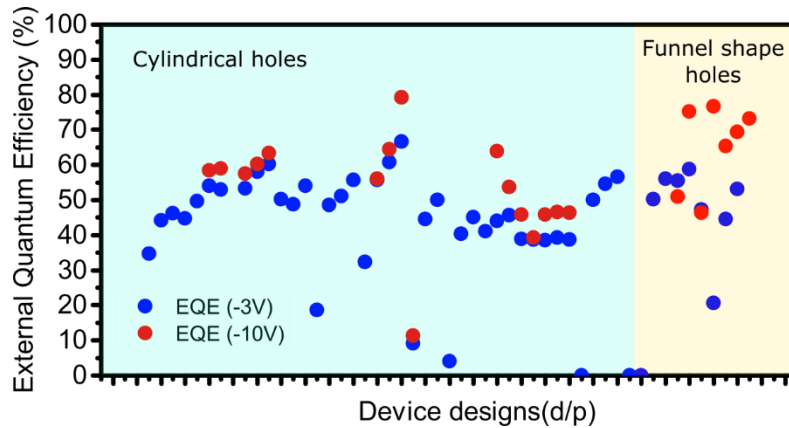
Fig. 7.6. EQE of Ge-on-Si PDs with different photon-trapping holes.

7.4.2 Dark count rate

Since the photon-trapping holes are created by dry etching with the physical bombardment of high-energy plasma ions, crystalline defects, and dangling bonds can be formed at the Ge surface and create surface states that can contribute to the increased dark current level, and thus need to be efficiently passivated. For no hole devices at -1V, the Dark Current Density (DCD) is 10-20mA/cm^2, while our devices with hole array present from 50-70mA/cm2 (Fig. 7.7a and b). Passivation of the surface with 10 nm SiO$_2$ was uniformly deposited on the wafer via ALD after the hole and mesa etches, reducing the leakage current in the photon-trapping devices. More passivation methods need to be investigated to effectively reduce the leakage current that can cause future Dark Count Rates in SPADs.

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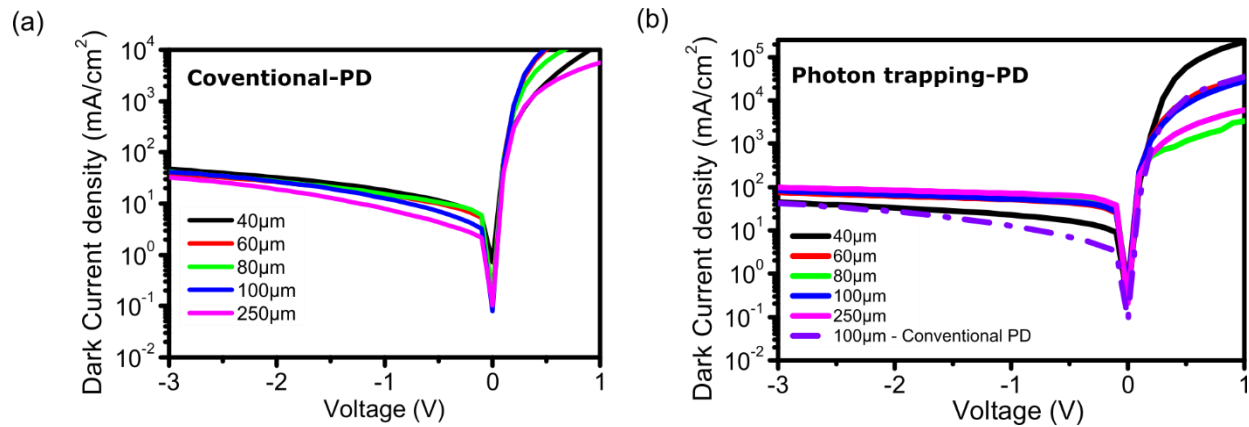
Fig. 7.7. Dark current density of Ge-on-Si photodetectors.

a) Conventional PD shows a DCD of 10-20mA/cm^2 while b) photon trapping PD present 50-70mA/cm^2.

7.5 Pulse time response measurements

Fig. 7.8a shows the pulse response in a photon-trapping PD with a mesa diameter of 30 μm. An improvement in the FWHM from 80ps to 75ps can be observed in our devices compared with the control device. A diffusion tail was observed after the pulse fall-time due to the slow carriers generated in the transition regions (p-i and i-n boundary regions). The dopant diffusion during epitaxial growth made the transition regions longer and softer where the applied field is not strong enough to drift the photogenerated carriers.

A computer simulation is used to evaluate the performance of Ge PDs with and without hole arrays for transmission speed. A pattern consisting of 2000 random bits was convolved with the PD impulse responses. The effect of a trans-impedance amplifier (TIA)

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was included in the simulations by applying the PD output to a third-order Butterworth filter with a 3-dB bandwidth equal to 0.75× bit rate[96]. The insets in Fig. 7.8 show the simulated eye diagrams at the filter output for a 10 Gb/s data transmission rate, indicating possible operation at such a rate. Compared to the eye diagrams generated with the measured impulse response of Ge PDs without hole arrays, there is an apparent improvement in transmission speed by Ge PDs with hole arrays, securing an operation of 10 Gb/s.

A pattern generator measurement has been done and as the eye diagrams show, this photon-trapping Ge-on-Si overcomes the bulky devices and can operate at such a high rate (Fig. 7.8b). The input wavelength was set to 1300 nm.
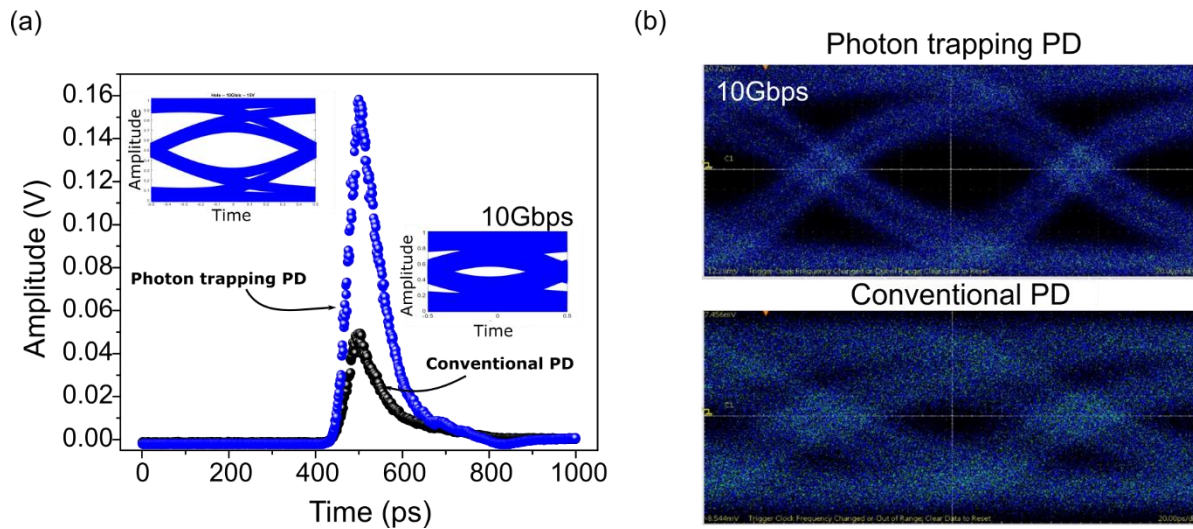
Fig. 7.8. Time response of Ge-on-Si photodetectors. a) Pulse response of Ge-on-Si photodetectors, b) eye diagrams at 10Gbps operation.

7.6 Summary

This chapter focused on demonstrating a surface-illuminated Ge-on-Si photodiode with photon-trapping holes. The photon-trapping holes have enabled lateral propagation modes in the thin Ge layers and, thus, successfully improved the external quantum efficiencies of the PDs at wavelengths between 1200 and 1800 nm. EQEs of 80% and 73% have been demonstrated at two data communication wavelengths (1300 and 1550 nm), respectively, both showing enhancement compared to Ge-on-Si PDs without holes.

In addition, the EQE has been improved beyond the L band (1620 nm) by more than 3.5-fold, which makes these PDs attractive for a new data transmission window. The photon-trapping holes also reduce the temporal response of the PDs by reducing the junction capacitance. The Ge-on-Si PD with photon-trapping holes has an FWHM temporal response of 70 ps, which is suitable for 10 Gb/s data transmission operation.

The Ge-on-Si PDs with an array of high-density photon-trapping holes have the potential to be monolithically integrated with CMOS/ BiCMOS ASICs. Such monolithic integration offers low-cost packaging solutions and allows low parasitics, resulting in high performance. Ge-on-Si PDs with photon-trapping holes can have applications for short- and long-reach communication at intra- and inter-datacenters, passive optical networks [3], lidar [47,48], and quantum communication systems [49], as well as enhancing the capacity of long-haul DWDM systems beyond the L band.

Chapter 8

Applications opportunities for new APDs

This chapter explores the benefits of our new photodetectors in a set of critical applications such as optical communications, LIDAR, and PET imaging.

8.1 Optical communications

Silicon APDs were first implemented in fiber optics communications. However, their limitation in gain-bandwidth, development of optical amplifiers, and the use of low loss wavelengths at 1300 nm and 1500 nm reduced the use of these APDs. New free-space and underwater optical communication are now proposed [97-99]. These applications operate at 600 nm to 700 nm, where silicon can still be used on the receiver end. A recent study compares the performance of APD and SPADs in free-space communications, showing that SPADs receiver requires approximately 45 times fewer detected photons per bit than a state-of-the-art APD [8]. So far, 1Gbps has been demonstrated in SPAD-based receivers for this type of communication, and efforts are being made to increase this data rate [99].

A signal-to-noise ratio calculation is done to illustrate the advantage of using the photon-trapping APD compared with a conventional device using Eq. 8.1.

$$\frac{S}{N} = \frac{I_p^2 * M^2}{2 * q * (I_P + I_D) * M^2 * F(M) * B_e + 2 * q * I_L * B_e * \frac{4 * k_B * T}{R_L} * B_e} \quad (8.1)$$

Fig. 8.1 compares the minimum optical power than can be detected with our silicon PIN and APD device with and without photon-trapping structures at 10 GHz. An APD allows detecting one order of magnitude less power than a PIN device due to the internal amplification gain. Even more, the enhanced EQE in the APD device enables the detection of a few 100s of nW less than a conventional device. At higher input power, the internal noise is also amplified, and the sensitivity of an APD is similar to a PIN device (Table 8.1). An optimal amplification of 14 was calculated for our photon-trapping device, while a conventional device obtains an optimum amplification of 12 according to [100].
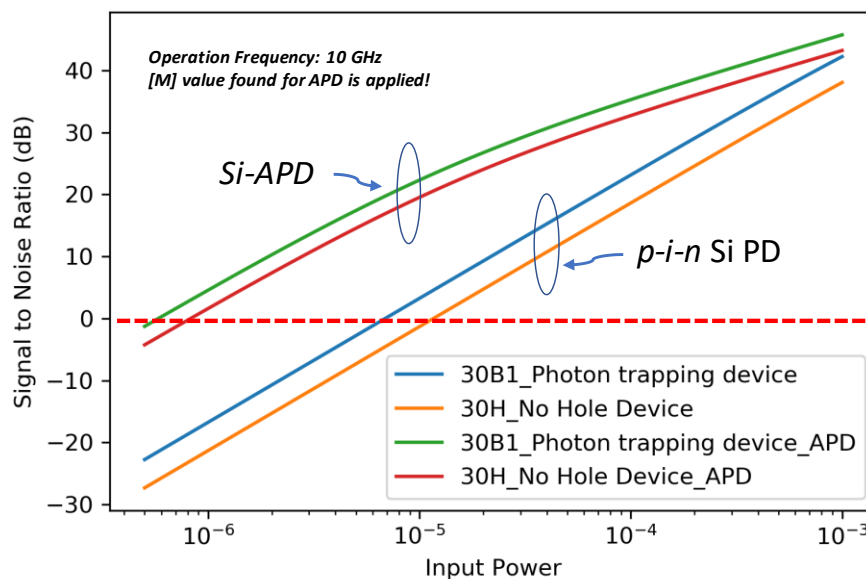
Fig. 8.1. Comparison in minimum power required to obtain an SNR=1 at 10GHz operation with and without photon-trapping hole array in APD and PIN mode.

Table 8.1. Comparison of Noise Equivalent Power of PIN and APD photodetector with and without photon-trapping hole array.

	PIN_Photon Trapping	PIN_No hole	APD_Photon Trapping	APD_No hole
Responsivity at 850 nm (A/W)	0.257	0.152	3.11	2.205
Dark Current (A)	7.3e-10	6.73e-10	7.3e-10	6.73e-10
Gain (M)	1		12.1	14.5
Voltage Operation (V)	10	10	29	34
NEP (W/sqrt(Hz))	6.866e-11	1.161e-10	5.67e-12	8.011e-12

8.2 Light Detection and Ranging (LIDAR) systems

Light detection and ranging (LIDAR) systems have been developed to provide autonomous cars with the capabilities to navigate safely. More than US$5 billion is expected to be invested in this technology by 2023 and US$28 billion by 2032 [101]. Long-range detection (>200m) is required to be measured by LIDAR and only APDs and SPADs can achieve that range. Receivers based on Silicon operating at 905 nm and Ge-on-Si operating at 1550 nm, are the two current technologies, each with different advantages in terms of laser power requirements, maturity of fabrication, and atmospheric transmission. The number of photons that reach the receiver surface decrease as $1/R^2$ where R is the range of measurement, limiting to a small number of photons than can be

sensed. As Fig. 8.2 illustrates, only 100's of photons return to the receiver when a maximum laser output power of 1 µJ is used and a few hundred meters are measured [102].
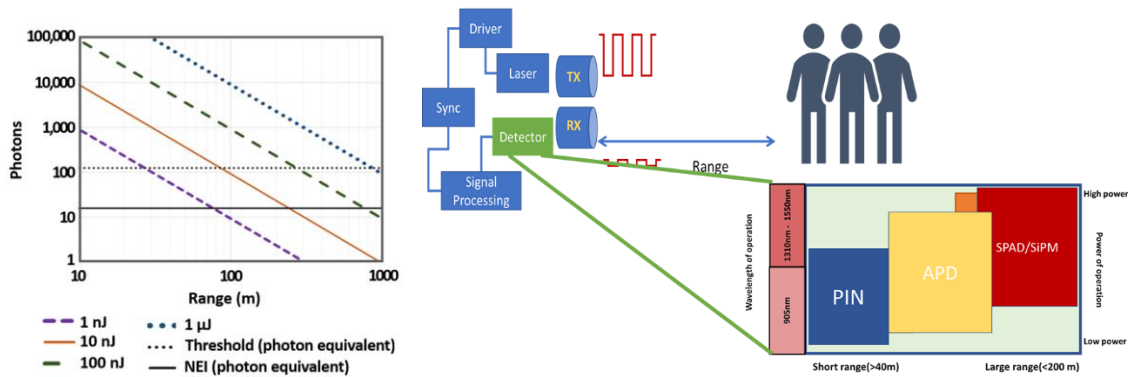
Fig. 8.2. Number of photons received by a LIDAR system and photodetector options.The number of photons that reach a receiver decreases a few 10's of photons as the distance of detection increases [102]. APD and most import SPADS are the only detectors available nowadays to sense more than 100m.

The enhancement in quantum efficiency from 7.6% to 44.1% at an input wavelength of 905 nm, while reducing the time response due to a reduction of the junction capacitance, allows for expanding the range of detection of LIDAR systems with higher timing resolution compared with a conventional photodetector. Using the range equation for LIDAR [103], it is possible to estimate the distance range that these new photodetectors can potentially measure. In addition to the enhancement of quantum efficiency, this calculation also considers different noise sources, beam propagation, and reflectivity of

the surface. Fig. 8.3 serves to illustrate the increment of distance measurement that a LIDAR can achieve with these new photodetectors [104, 105].
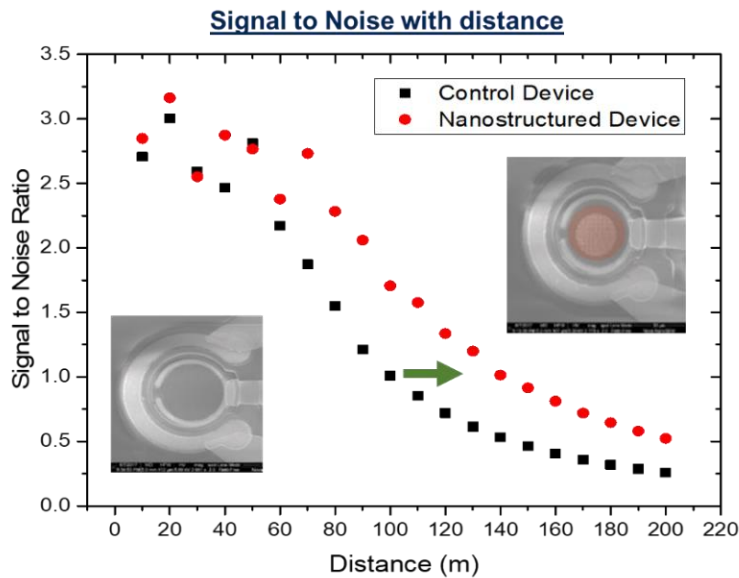
Fig. 8.3. Calculation of Signal to Noise Ratio with respect to the distance of a LIDAR system, considering the enhancement of EQE.

8.3 Time-of-flight positron emission tomography

PET uses lesser amounts of radioactive materials called radiotracers, a special camera, and image processing tools to help evaluate human organ and tissue functions. By identifying body changes at the cellular level, PET may detect the early onset of disease in cancer and a variety of neurological, cardiovascular, and musculoskeletal disorders before it is evident on other imaging tests. PET imaging can pinpoint molecular activity

within the body and offer the potential to identify disease in its earliest stages as well as a patient's immediate response to therapeutic interventions [106, 107].

State-of-the-art time-of-flight PET (TOF-PET) scanners currently employ scintillation crystal detectors coupled to photomultiplier tubes (PMTs) or silicon photomultipliers (SiPMs) to achieve coincidence time resolutions below 300-700 ps at FWHM. Based on TOF-PET's better signal-to-noise ratio (SNR) and artifact reduction capabilities compared to conventional PET systems, these scanners provide much more precise localization of metabolic activity, improved quantitative accuracy, and more confidence in diagnostic classification of small lesions (Fig. 8.4a and b) [108, 109].

(a) Without TOF   (b) With TOF
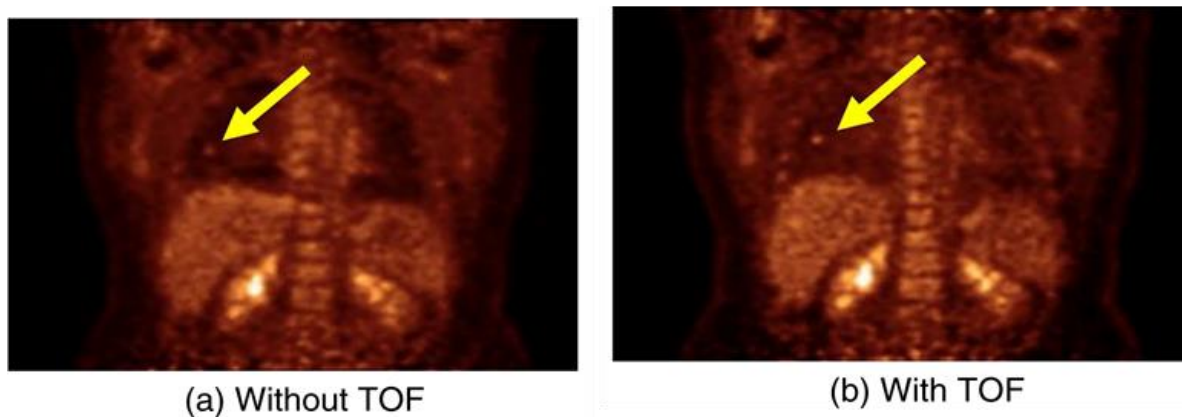
Fig. 8.4. Improvement in image quality due to the incorporation of TOF in the reconstruction. (a) no TOF information and (b) with TOF information with a timing resolution of 375 ps [28].

For early diagnosis of lung cancer, brain diseases, or in the assessment of coronary diseases, TOF-PET is exceptionally useful [110]. The impact and benefits of advancing toward reconstruction-less TOF-PET in oncology, cardiology, or neurology, among others will be dramatic. However, timing resolutions of PET detectors need to

improve more than an order of magnitude since the current time resolution in commercially available TOF-PET systems is 300-700 ps FWHM [111]. Laboratory systems have achieved values around 100 ps. TOF-PET will reach its maximum impact when the timing resolutions are 10 ps, allowing precise localization of each positron-electron annihilation in a 3-D point with <1 mm spatial accuracy and enabling reconstruction-less TOF-PET [112, 113]. For this project, Islam's Lab and Cherry's Lab, from the Department of Biomedical Engineering, have a collaboration with the aim to develop arrays of SPADs for high-resolution Positron emission tomography (PET).

8.4 Summary

This chapter has presented the advantages of highly sensitive APDs and SPADs in different emerging applications. For optical communications, we analyzed the Signal to Noise Ratio (SNR) obtained by different input powers. As we know, APDs tend to have higher SNR than PIN devices and our new APDs have the potential to increase this value. In LIDAR, the length of distance that can be measured can increase with a higher sensitivity device when the power does not exceed the eye safety limitations. From another point of view, the laser output power can be decreased when having such a sensitive device, contributing to reducing the overall power consumption of the system. PET imaging is an application where in addition to sensitivity at visible wavelengths, high-speed SPADs are required to obtain the origin of the emitted positron. Ultra-fast devices are critical to getting higher-resolution medical imaging.

Chapter 9

Conclusions and future work

In this chapter, we discuss the conclusions of this dissertation and future research opportunities.

9.1 Summary

We have developed new silicon and germanium-on-silicon-based PDs with high speed and absorption efficiency at visible and near-infrared wavelengths.

In chapter 3, we showed the design and fabrication of an all-silicon photodiode with photon-trapping micro/nanoholes structures. These photon-trapping holes successfully enhance the absorption of silicon by more than 10 times in the NIR wavelengths of operation and by more than 50% in short visible wavelengths. Through extensive simulations and experimental implementations of photon-trapping structures in silicon photodetectors, we helped divulge a direct correlation between the enhancement of absorption and physical parameters of the photon-trapping structures integrated into the photodetectors. The higher absorption achieved allows an increase in the output signal photocurrent of avalanche photodetectors and the photon detection efficiency of SPADs.

In chapter 4, we have shown that it is possible to guide photons to a critical depth in a semiconductor and maximize the gain-bandwidth performance and absorption efficiency

in avalanche-based photodetectors by integrating photon-trapping nanoholes with different profiles and depths on the device surface. Such nanoholes allow engineering the penetration depth for different wavelengths in silicon. A more extended penetration depth for short wavelengths such as 450 nm can reduce the absorption close to the surface of the device, where carriers can be lost by recombination or be slowly transported by diffusion. On the other hand, the penetration depth for the long wavelengths such as 850 nm is reduced from 18.3 μm to only 2.3 μm. Such reduction in penetration depth allows to reduce the device transit time with a direct impact on the bandwidth of the devices. This study is the first comprehensive evaluation of the gain and detection efficiency of avalanche photodiodes (APD) with photon-trapping nanostructures for photons of 450 nm and 850 nm wavelengths.

Chapter 5 has demonstrated the temporal impulse response for Si PDs of 29ps FWHM when operating at unity gain with potential operation at 20Gbps. For the first time, a silicon PD exhibited such a high speed and high EQE. The enhanced absorption demonstrated enables designing PDs with thinner absorbing layers, reducing the transit time of the photogenerated carriers without compromising their absorption efficiency. Photon-trapping structures offer a solution to reduce the junction capacitance by >50%, which depends on the device area and the depletion layer thickness. The combined effect collectively can help overcome the trade-off between the efficiency and speed of operation of the PDs. In APD and SPAD regimes, the photon-trapping PDs exhibited a decrease in the FWHM from 99 ps to 40 ps. A conspicuous faster fall time from 293 ps to

105 ps of the impulse response is attributed to the efficient delivery of the input light to the high electric field regions and a decrease of absorption in the highly doped regions, where diffusion is the dominant carrier transport method. The carrier density model presented helped explain such improvement in the time response.

In Chapter 6, We have designed and fabricated Si APDs with ultra-thin absorbing layers of only 1.2 μm and with a doping layer profile optimized to maximize its gain. With the implementation of our optimization tools, it is shown that at 450 nm, 90% of optical absorption can be obtained with the implementation of photon-trapping structures. Additionally, there is a notable improvement in absorption at NIR wavelengths.

Chapter 7 focused on demonstrating a surface-illuminated Ge-on-Si photodiode with photon-trapping holes. The photon-trapping holes have enabled lateral propagation modes in the thin Ge layers and, thus, successfully improved the external quantum efficiencies of the PDs at wavelengths between 1200 and 1800 nm. EQEs of 80% and 73% have been demonstrated at two data communication wavelengths (1300 and 1550 nm), respectively, both showing enhancement compared to Ge-on-Si PDs without holes.

In addition, the EQE has been improved beyond the L band (1620 nm) by more than 3.5 times, which makes these PDs attractive for new data transmission windows. The photon-trapping holes also reduce the response time of the PDs by reducing the junction capacitance. The Ge-on-Si PDs with photon-trapping holes have an FWHM temporal response of 70ps, which is suitable for 10 Gb/s data transmission operation.

The Ge-on-Si PDs with an array of high-density photon-trapping holes have the potential to be monolithically integrated with CMOS/ BiCMOS ASICs or implemented in waveguide PDs for their integration on photonic integrated circuits (PIC).

9.2 Future opportunities

a. **Photon-trapping structures in PDs based on other semiconductor materials.** These nanostructures can be implemented in other semiconductor materials required in NIR wavelengths such as GaAs, InGaAs, or in Infrared wavelengths such as lead selenide (PbSe) and mercury cadmium telluride (HgCdTe) [53-55].

b. **Integration of structures on CMOS foundries PDKs.** A Process Design Kit (PDK) is a fabrication process defined by a semiconductor foundry that is then passed to its customer to follow it. To make the photon-trapping approach commercially viable, it is necessary to accommodate the fabrication of these nanostructures in their current PDKs [114, 115].

c. **Unique responsivity in PDs for spectral applications.** Our group is exploring the capabilities of the nanostructures to create a unique responsivity for each individual photodetector in an array. Such an approach would enable the creation of highly compact spectrometers based on deep learning and computational

imaging [116, 117]. An array of unique PDs is capable of real-time in-situ tissue diagnosis during surgery, cell labeling, and locating molecular activity in living organisms under low light illumination, detecting diseases and early disorders before they are diagnosed with conventional methods.

d. **Use of nanostructure as biosensing platforms.** Nanoholes are used for DNA analysis and sequencing [118, 119]. The current dimensions of the nanostructures on the order of micrometers made them suitable for the detection of bacteria and cells. The change in the optical and electrical properties of the device can be exploited as biosensors.

The end of the 19th century and the beginning of the 20th century set the theoretical base and experiments that lead to the development of Quantum Mechanics. One hundred years later, we can now manipulate the matter at the atomic level, inviting us to 'look at the bottom' and find solutions to fundamental problems in biology and chemistry for the good of our society.

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