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***Abstract*—Flying capacitor multilevel (FCML) converters typically rely on natural balancing to achieve a balanced distribution of flying capacitor voltages. The mechanisms by which the flying capacitor voltages are able to balance have been extensively studied and theoretically there are certain combinations of level count and duty cycle at which the flying capacitor voltages do not balance. Although the flying capacitor voltages should diverge from the balanced distribution, in practice this behavior is rarely observed. To resolve this discrepancy between FCML converter theory and experiment, this article analyzes the impact of switch output capacitance on the flying capacitor voltage balancing dynamics, and illustrates that this capacitance has a naturally balancing effect. The additional mechanism of switch output capacitance induced balancing is analytically described and compared against experimental results on several FCML converter prototypes.**

I. Introduction

POWER converters in applications such as traction and propulsion drives and data center power delivery require high power density and efficiency [1]–[3]. In pursuit of maximizing these objectives, the flying capacitor multilevel (FCML) converter has emerged as a promising topology for these cutting edge applications [4]–[8]. Although the topology was initially developed to remedy the lack of high voltage switches rated for the input voltage in high voltage power conversion applications [9], the FCML converter is able to outperform conventional topologies in lower voltage applications. A simplified schematic of a five-level FCML converter is presented in Fig. 1. A key practical challenge in the utilization of high-performance FCML converters is the voltage balancing of the flying capacitors, the focus of this work. Specifically, we demonstrate the effect of transistor output capacitance on natural balancing, and derive key equations along with experimental validation.

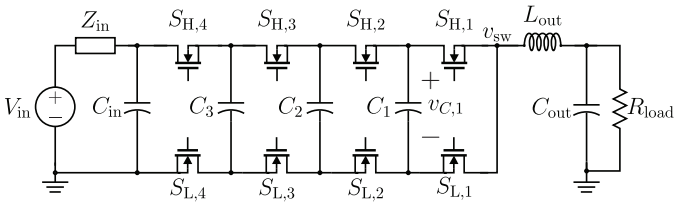

Fig. 1: Simplified five-level FCML converter circuit schematic with input impedance explicitly drawn. The ground-referenced switch-node voltage v_{sw} is explicitly labeled.

Several works [10]–[13] have discovered "unbalanced" conversion ratios, at which the flying capacitor voltages theoretically do not passively balance to their desired steady-state values and instead diverge. These "unbalanced" conversion ratios are defined as conversion ratios where $D \cdot (N-1)$ and $(N-1)$ are not co-prime, where D is the duty cycle of the high-side switches $S_{\text{H},k}$ in the FCML converter operated with symmetric phase-shifted PWM (PS-PWM), and where $D \cdot (N-1)$ is an integer. Of note, however, is that these theoretically unbalanced operating points and divergent flying capacitor voltages are not typically observed in experimental hardware [11], pointing to a gap in the understanding of all pertinent balancing mechanisms within the converter. Of particular interest in this work is the combination of a five-level FCML converter operated at a duty cycle of $D = 50\%$ as it is the simplest FCML converter which exhibits this theoretical behavior.

This work analyzes the natural balancing of the capacitor voltages in an FCML converter, and extends past work to also include the impact of switch output capacitance. Crucially, it is discovered that the transient charge flow between flying capacitors and parasitic switch output capacitance C_{oss} during switch transitions has a naturally balancing effect, which has previously not been documented. A detailed state-space model is developed to include this balancing mechanism, and through hardware validation, it is shown that the proposed model accurately captures the experimental behavior, which was not achieved by previous models.

This work has two key contributions: 1) Identification of the role of the switch output capacitance in the natural balancing of the flying capacitor voltages, along with an analytical expression of the strength of the balancing mechanism. 2)

Part of this manuscript was presented at the 2022 IEEE Workshop on Control and Modeling for Power Electronics (COMPEL) as the paper "On the Role of Switch Output Capacitance on Passive Balancing within the Flying Capacitor Multilevel Converter". This manuscript extends the previous work by including the impact of source impedance on flying capacitor voltage balancing and comparing this impact to that of C_{oss}-induced charge flow. Additionally, we extend our previous model to include the nonlinear capacitances which are typically found in high performance power converters.
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Development of an analytical model incorporating said balancing mechanism, which shows excellent agreement with experimental results. Together, these two contributions yield — for the first time — a model of FCML converter natural balancing that matches experimental observations during practical operating conditions (e.g., start-up transients). In [14], the authors utilized C_{oss}-induced charge flow to actively balance the flying capacitor voltages at zero output current. This manuscript, however, analyzes how C_{oss}-induced charge flow participates in the natural balancing process, particularly as it relates to "unbalanced" conversion ratios. Several other works focused on FCML converter design and optimization [15], [16] have considered the power loss penalty of C_{oss}, but not this parasitic's impact on the flying capacitor voltages.

This manuscript is based on our previously published conference publication [17]. In this work, we incorporate the impact of source input impedance and compare its tendency to generate imbalanced flying capacitor voltages to the balancing effect of C_{oss}-induced charge flow. Additionally, we include discussion on the incorporation of nonlinear capacitances in an analytical model of the FCML converter. The remainder of this manuscript is organized as follows: Section II introduces the FCML converter and provides a brief overview of natural balancing theory. In Section III, analysis of the charge flow induced by C_{oss} and this charge flow's impact on the flying capacitor voltages is presented. This phenomenon is then incorporated into a state space model for the FCML converter to investigate the transient response of the converter. Section IV shows the experimental setup and data which validate the proposed flying capacitor voltage balancing model. Several FCML converter prototypes are excited with a high slew rate input voltage step and the flying capacitor voltage transient response is analyzed and compared. Finally, Section V concludes this manuscript.

II. Flying Capacitor Multilevel Converter Balancing Mechanisms and Unbalanced Conversion Ratios

The promise of the FCML topology to enable the incorporation of high-performance low-voltage switches [16] with an even voltage stress distribution requires that the voltages of the flying capacitors not deviate too far from their ideal distribution. If this constraint is violated, the system efficiency will decrease and in the worst case, the switches will be exposed to a voltage higher than their ratings, yielding converter failure.

Previous works [10], [11], [13], [18]–[21] have analyzed the mechanisms by which the flying capacitors within an FCML converter converge to the balanced steady-state voltage distribution $v_{C,k} = (kV_{\text{in}})/(N-1)$ where N is the number of discrete levels in the switch node waveform, and k ranges from 1 to $N-2$, with capacitor voltages as annotated in Fig. 1. Work in [9] demonstrated that with symmetric Phase-Shifted PWM (PS-PWM) modulation, the flying capacitor voltages will dynamically balance to the aforementioned voltage distribution. Furthermore, if the high-side switches $S_{\text{H},k}$ are operated with a duty cycle D, and the low-side $S_{\text{L},k}$ switches in a complementary fashion, the output voltage will

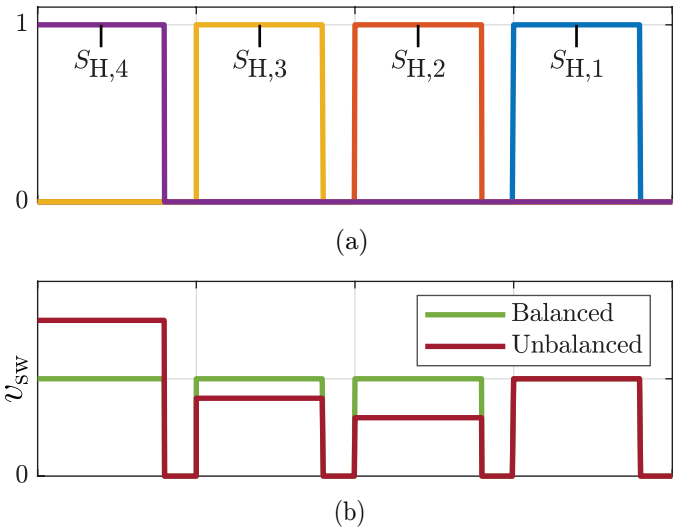

Fig. 2: (a) Example symmetric phase-shifted PWM (PS-PWM) switching signals for a five-level FCML converter operated at a duty cycle $D = 0.2$. (b) Switch-node voltage voltage v_{sw} resulting from both a balanced and an example unbalanced flying capacitor voltage distribution. When the flying capacitor voltages are balanced, the voltage stress applied to the switches and the volt-seconds applied to the output filter inductor are minimized. The unbalanced case shown has flying capacitor voltages of $v_{C,1} = 0.25V_{\text{in}}$, $v_{C,2} = 0.4V_{\text{in}}$, and $v_{C,3} = 0.6V_{\text{in}}$.

be $V_{\text{out}} = D\,V_{\text{in}}$. Example switching signals and switch node voltages for balanced and unbalanced flying capacitor voltages are shown in Fig. 2.

When the flying capacitor voltages are balanced, the lowest frequencies present in the switch node waveform are dc and $(N-1)f_{\text{sw}}$. According to previous analyses [11], [22], natural balancing occurs because unbalanced flying capacitor voltages create a switch node voltage which has harmonic content between f_{sw} and $(N-2)f_{\text{sw}}$, as can be seen in Fig. 2. When these "lower-order" voltage harmonics are present, they induce current and losses in the RLC circuit of the output filter. These losses work to drive the flying capacitor voltages to their balanced distribution. However, at certain combinations of level count and duty cycle, the flying capacitor voltages are unable to be independently impacted by the RLC circuit dynamics of the output filter [12], [13] and thus natural balancing fails. Fig. 3 shows the equivalent circuits for a five-level FCML converter operated with symmetric PS-PWM at a duty cycle of 50%. At this operating point, it can be seen that capacitors C_1 and C_3 are always connected in series when connected to the output filter. Since these flying capacitor voltages cannot be independently changed, the flying capacitor voltages theoretically will not balance.

III. Switch Output Capacitance (C_{oss}) Impact on Flying Capacitor Natural Balancing

To resolve the discrepancy between previous literature and experimental evidence regarding natural balancing at the "unbalanced" conversion ratios [11], [13], there must exist some mechanism not included in the aforementioned works' simplified model of the FCML converter which acts to drive the flying capacitor voltages to the balanced state, even at

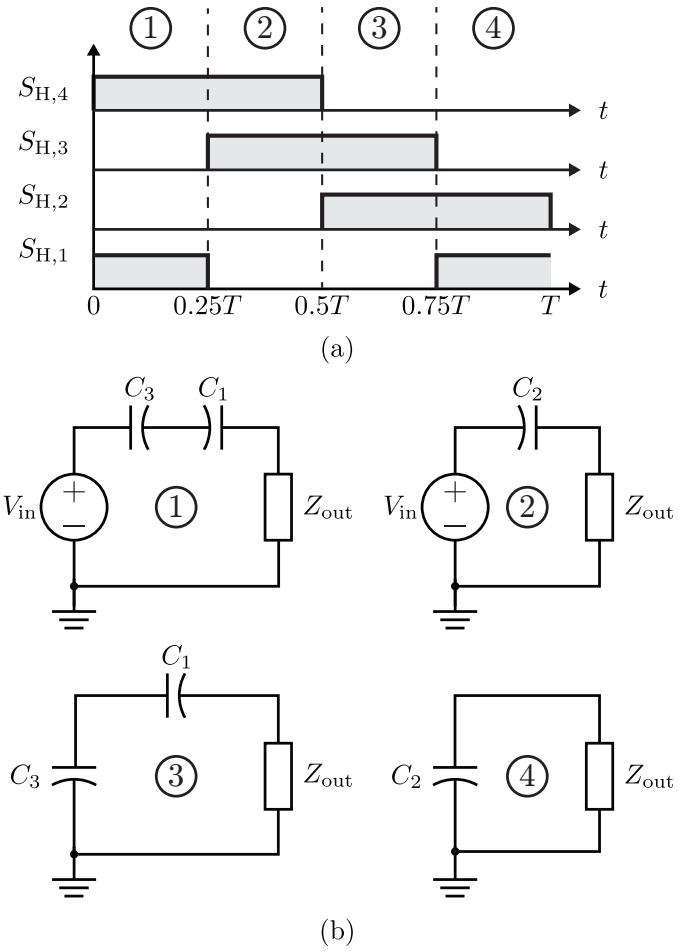

Fig. 3: (a) Gate signals for a five-level FCML converter operated with PS-PWM at a duty cycle of 50%. (b) Equivalent circuits of the FCML converter. Z_{out} represents the impedance of the output filter inductor and capacitor and load resistance as connected in Fig. 1.

"unbalanced" conversion ratios. One such mechanism not previously modeled is charge redistribution induced by the switch parasitic output capacitance. During each switching event, the output capacitance C_{oss} of a switch which was previously on is charged from ≈ 0 V to a linear combination of the flying capacitor voltages and the input voltage. For example, when $S_{\text{H},2}$ switches from ON to OFF and $S_{\text{L},2}$ switches from OFF to ON, the C_{oss} of $S_{\text{H},2}$ is charged from $\approx 0\,\text{V}$ to $v_{C,2} - v_{C,1}$. Similarly, the C_{oss} of $S_{\text{H},1}$ will be charged from $\approx 0\,\text{V}$ to $v_{C,1}$ when $S_{\text{H},1}$ switches from ON to OFF. As will be shown in the subsequent analysis, these previously unmodeled charge flows due to C_{oss} are functions of the flying capacitor voltages and provide an inherent balancing mechanism in the FCML converter.

A. Charge Flow Analysis

To provide a tractable, analytical description of this charge flow mechanism, we make the following simplifying assumptions: 1) all switches are commuted with zero dead-time and in perfect complementary fashion, and 2) the flying capacitors and C_{oss} parasitic capacitances are linear. These simplifying assumptions will be examined and re-evaluated in Section III-C. Examining the switching event illustrated in Fig. 4, at $t = 0$, $S_{\text{H},2}$ opens and $S_{\text{L},2}$ closes. The charge quantity circulating during this commutation event can be expressed in terms of the flying capacitor voltages at $t = 0$ and $t = t_{\text{f}}$, where t_{f} is the time at which the system voltages have approximately settled. Expressing the charge flowing in the highlighted commutation loop of Fig. 4 as Q_{flow}:

$$Q_{\text{flow}} = C_{\text{oss,H}} \Delta v_{\text{H}} = C_{\text{oss,H}} \cdot \big(v_{\text{H}}(t_{\text{f}}) - v_{\text{H}}(0)\big) \quad (1)$$

$$v_{\text{H}}(t_{\text{f}}) = v_{C,2}(t_{\text{f}}) - v_{C,1}(t_{\text{f}}),\ v_{\text{H}}(0) \approx 0$$

$$Q_{\text{flow}} \approx C_{\text{oss,H}} \cdot \big(v_{C,2}(t_{\text{f}}) - v_{C,1}(t_{\text{f}})\big) \quad (2)$$

In this process, charge Q_{flow} leaves C_2 and is deposited on C_1. The flying capacitor voltages, $v_{C,1}$ and $v_{C,2}$, after a commutation event are thus functions of this Q_{flow}:

$$\begin{aligned} v_{C,2}(t_{\text{f}}) &= v_{C,2}(0) - \frac{Q_{\text{flow}}}{C_2} \\ &= v_{C,2}(0) - \frac{C_{\text{oss,H}}}{C_2} \cdot \big(v_{C,2}(t_{\text{f}}) - v_{C,1}(t_{\text{f}})\big) \\ &= \frac{C_2}{C_2 + C_{\text{oss,H}}} v_{C,2}(0) + \frac{C_{\text{oss,H}}}{C_2 + C_{\text{oss,H}}} v_{C,1}(t_{\text{f}}) \quad (3) \end{aligned}$$

$$\begin{aligned} v_{C,1}(t_{\text{f}}) &= v_{C,1}(0) + \frac{C_{\text{oss,H}}}{C_1} \cdot \big(v_{C,2}(t_{\text{f}}) - v_{C,1}(t_{\text{f}})\big) \\ &= \frac{C_1}{C_1 + C_{\text{oss,H}}} v_{C,1}(0) + \frac{C_{\text{oss,H}}}{C_1 + C_{\text{oss,H}}} v_{C,2}(t_{\text{f}}) \quad (4) \end{aligned}$$

Substituting (3) into (4) yields:

$$v_{C,1}(t_{\text{f}}) \left[1 - \frac{C_{\text{oss,H}}^2}{(C_1 + C_{\text{oss,H}})(C_2 + C_{\text{oss,H}})}\right] = \frac{C_1}{C_1 + C_{\text{oss,H}}} v_{C,1}(0) + \frac{C_{\text{oss,H}} C_2}{(C_1 + C_2)(C_2 + C_{\text{oss,H}})} v_{C,2}(0). \quad (5)$$

Finally, by rearranging we obtain an equation for $v_{C,1}$ at the end of a commutation event:

$$v_{C,1}(t_{\text{f}}) = \frac{v_{C,1}(0) \cdot (C_1 C_2 + C_1 C_{\text{oss,H}}) + C_2 C_{\text{oss,H}} v_{C,2}(0)}{C_1 C_2 + C_{\text{oss,H}}\,(C_1 + C_2)}. \quad (6)$$

As expressed in (6), the flying capacitor voltages rapidly change after a commutation event due to C_{oss}-induced charge redistribution.

Under the assumption of zero dead-time, both high-to-low switch transitions and low-to-high switch transitions experience the same charge flow. Table I summarizes each flying capacitor voltage after a commutation event (obtained by the same process that yielded (6)). These approximations assume that the commutation events are "local", that is, only the flying capacitors connected to a commutating switching cell participate in C_{oss} charge redistribution[1]. Additionally, if two cells commutate at the same time, the voltage at the end of the event can be approximated by a cascade of two separate switching events. Note that the entries in Table I are

[1]In reality, flying capacitors that are not directly connected to a switching cell are weakly connected to the cell through the C_{oss} of a turned OFF switch. For example, C_2 is in parallel with the series combination of C_3 and C_{oss} when the S_2 switching cell commutes. However, due to the relative sizing of C_{fly} and C_{oss} (i.e., $C_{\text{fly}} >> C_{\text{oss}}$) in practical implementations of the topology, the modeling error introduced is negligible.

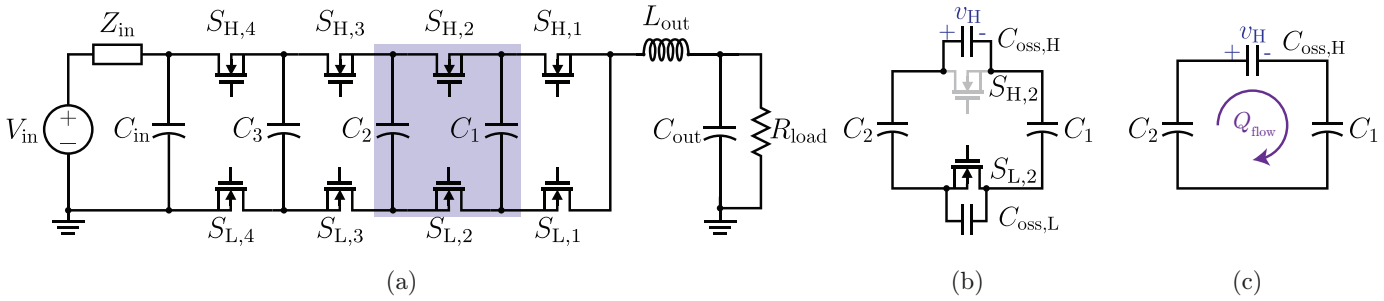

Fig. 4: (a) Simplified five-level FCML converter circuit schematic with source input impedance explicitly drawn and switching cell 2 highlighted. (b) Switching cell 2 with switch output capacitances C_{oss} explicitly drawn. At $t = 0$ a commutation of the S_2 switching cell occurs, with $S_{\text{H},2}$ turning OFF and $S_{\text{L},2}$ turning ON. (c) Equivalent circuit after $t = 0$ for analyzing commutation charge flow. Charge Q_{flow} circulates around the commutation loop, discharging C_2 and charging C_1 and $C_{\text{oss,H}}$. Parasitic resistances are omitted for clarity.

TABLE I

TABULATED ANALYTICAL SOLUTIONS TO THE FLYING CAPACITOR VOLTAGES AFTER A COMMUTATION EVENT OCCURS FOR N=5.

Switching Cell Event (ON or OFF)	**Flying Capacitor Voltage After Commutation**
S_1	$v_{C,1}(t_{\text{f}}) = v_{C,1}(0) - \frac{C_{\text{oss}}}{C_1+C_{\text{oss}}} v_{C,1}(0)$
S_2	$v_{C,1}(t_{\text{f}}) = v_{C,1}(0) + \frac{C_2 C_{\text{oss}}}{C_1 C_2 + C_{\text{oss}}\,(C_1+C_2)}(v_{C,2}(0) - v_{C,1}(0))$ $v_{C,2}(t_{\text{f}}) = v_{C,2}(0) + \frac{C_1 C_{\text{oss}}}{C_1 C_2 + C_{\text{oss}}\,(C_1+C_2)}(v_{C,1}(0) - v_{C,2}(0))$
S_3	$v_{C,2}(t_{\text{f}}) = v_{C,2}(0) + \frac{C_3 C_{\text{oss}}}{C_2 C_3 + C_{\text{oss}}\,(C_2+C_3)}(v_{C,3}(0) - v_{C,2}(0))$ $v_{C,3}(t_{\text{f}}) = v_{C,3}(0) + \frac{C_2 C_{\text{oss}}}{C_2 C_3 + C_{\text{oss}}\,(C_2+C_3)}(v_{C,2}(0) - v_{C,3}(0))$
S_4	$v_{C,3}(t_{\text{f}}) = v_{C,3}(0) + \frac{C_{\text{oss}}}{C_3+C_{\text{oss}}}(V_{\text{in}} - v_{C,3}(0))$

generalizable to FCML converters with arbitrary level counts as can be seen by the symmetry in the equations for the S_2 and S_3 switching cell. That is, the form of the equations for switching cell S_2 apply to all switching cells with two flying capacitors.

In reality, commutations are not perfectly instantaneous and practical converters will introduce a deadtime period where $S_{\text{H},k}$ and $S_{\text{L},k}$ are OFF simultaneously. These non-zero deadtimes will impact the previously described charge flows in the following ways. For the sake of simplicity, we assume the inductor current i_L is positive (i.e., flowing to the output in Fig. 4(a)). After $S_{\text{L},k}$ turns OFF and before $S_{\text{H},k}$ turns ON, the inductor current i_L will discharge the $C_{\text{oss,L}}$ of $S_{\text{L},k}$. If this capacitance is fully discharged, the body diode (or effective body diode) of this switch will turn ON. If this occurs before $S_{\text{H},k}$ switch turns on, the low side capacitance will then be charged from $-V_{\text{d}}$, the "diode voltage", up to a combination of the flying capacitor voltages rather than from $\approx$ 0 V as the equations in Table I assume. In practice, this slight approximation error was found to be negligible. Conversely, after $S_{\text{H},k}$ turns OFF and before $S_{\text{L},k}$ turns ON, $C_{\text{oss,H}}$ will be partially charged and $C_{\text{oss,L}}$ partially discharged by the inductor current. This will reduce the charge flow when $S_{\text{L},k}$ turns ON. Similar to neglecting the body diode voltage drop, this approximation error was found to have negligible impact.

B. Analytical FCML Converter Model Incorporating C_{oss} Induced Charge Flow

Given that the C_{oss}-induced voltage changes per commutation event are very small compared to the average values of the flying capacitor voltages[2], it is difficult to ascertain a priori whether the flying capacitor voltages will settle to a balanced state and if they do, how quickly transients settle. To investigate the circuit response, an analytical model was developed in MATLAB to solve for the state variables within the circuit as a function of time. To analytically simulate the circuit, each switching configuration is associated with a set of state-space matrices. As an example, consider the symmetric PS-PWM switch configuration to generate an approximate switch node voltage of $V_{\text{in}}/2$ with switches $S_{\text{H},1}$, $S_{\text{L},2}$, $S_{\text{L},3}$, and $S_{\text{H},4}$ ON while complementary switches are OFF. The circuit associated with this switching configuration is illustrated in Fig. 5. The state-space description of this circuit is:

$$\dot{x}(t) = \frac{\text{d}}{\text{d}t}\begin{bmatrix} v_{C,1} \\ v_{C,2} \\ v_{C,3} \\ i_L \\ v_{\text{out}} \\ v_{C_{\text{in}}} \\ i_{Z_{\text{in}}} \end{bmatrix} = \mathbf{A}\begin{bmatrix} v_{C,1} \\ v_{C,2} \\ v_{C,3} \\ i_L \\ v_{\text{out}} \\ v_{C_{\text{in}}} \\ i_{Z_{\text{in}}} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 1 \end{bmatrix} V_{\text{in}} \tag{7}$$

[2]For example, in the converter shown in Section III, the flying capacitor voltages may change by less than a tenth of a percent in a commutation event.

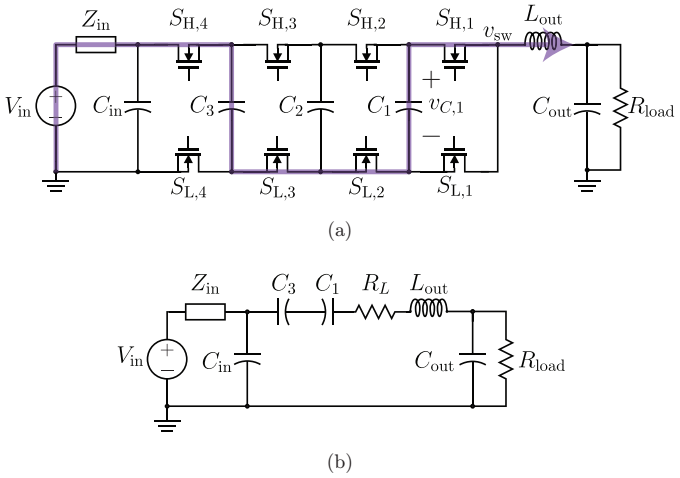

Fig. 5: (a) Circuit schematic of a five-level FCML converter to generate a switch-node voltage of $V_{\text{in}}/2$ with current path highlighted and input network explicitly drawn. (b) Equivalent circuit used to obtain the state space description of Eq. 7. R_L models the sum of series resistances in the power path (e.g., inductor and FET resistance, etc.).

$$\mathbf{A} = \begin{bmatrix} 0 & 0 & 0 & -C_1^{-1} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & C_3^{-1} & 0 & 0 & 0 \\ L_{\text{out}}^{-1} & 0 & -L_{\text{out}}^{-1} & -R_L L_{\text{out}}^{-1} & -L_{\text{out}}^{-1} & L_{\text{out}}^{-1} & 0 \\ 0 & 0 & 0 & C_{\text{out}}^{-1} & -C_{\text{out}} R_{\text{load}}^{-1} & 0 & 0 \\ 0 & 0 & 0 & -C_{\text{in}}^{-1} & 0 & 0 & C_{\text{in}}^{-1} \\ 0 & 0 & 0 & 0 & 0 & -L_{\text{in}}^{-1} & 0 \end{bmatrix} \tag{8}$$

Where R_L is the sum of series resistances within the sub-circuit comprising inductor resistance, switch on-state resistance, flying capacitor ESR, and any other parasitic resistances.

The state variables at the end of a switching state $x(t_f)$ are then found by solving the state evolution equation:

$$\dot{x}(t) = \mathbf{A}\, x(t) + \mathbf{B}\, V_{\text{in}}(t) \tag{9}$$

as a function of the state variables at the beginning of a switching state $x(t_0)$. This solution is [23]:

$$x(t_{\text{f}}) = \exp(\mathbf{A}(t_{\text{f}} - t_0))x(t_0) + \int_{t_0}^{t_{\text{f}}} \exp(\mathbf{A}(t_{\text{f}} - \tau))\mathbf{B}V_{\text{in}}(\tau)\text{d}\tau \tag{10}$$

where $x(t_0)$ is the initial condition for the state variables and $x(t_{\text{f}})$ the final state value. To save memory and computational load, the state variables are only solved at each switching instance, thus the time steps of the solver are the same as those of the switching instances of the converter. By "stitching" together these final and initial states and continually solving the state evolution equation we can obtain time-series data of the converter's state variables.

To incorporate the charge flows and voltage changes induced by the switch output capacitance, the flying capacitor voltages at the end of a switching state are changed according to Table I. These modified flying capacitor voltages are then used as the initial value for the next state evolution equation solver.

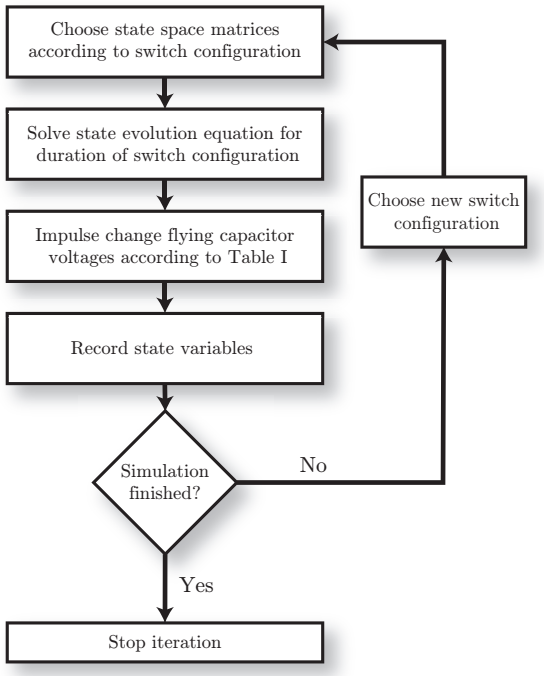

Fig. 6: Flowchart illustrating the MATLAB algorithm developed to obtain the FCML converter state variables as a function of time.

The developed algorithm is shown in the flowchart of Fig. 6.

C. Extension to Nonlinear Capacitances

In many practical implementations of the FCML topology, nonlinear flying capacitors and nonlinear device C_{oss} will be employed, requiring an increase in simulation complexity for model fidelity. Class 2 ceramic capacitors (e.g., X6S) are often used for the flying capacitors due to their superior energy density compared to Class 1 capacitors [24]. This benefit in density comes at the penalty of a strongly nonlinear small-signal capacitance versus bias voltage characteristic. To incorporate this impact in an analytical simulation, the state space matrices can be modified by updating the flying capacitance values with a look up table using the flying capacitor voltage at the start of a switching phase. This process implicitly assumes the flying capacitor voltage will not change drastically over a switching phase, an assumption which is generally true in practical implementations.

A more severe nonlinearity is encountered in the transistor output capacitance, C_{oss}. Fig. 7 depicts the C_{oss} vs. V_{ds} curve for the EPC2302 [25], a high performance 100 V eGaN FET. In many implementations, the output capacitance will swing from $\approx$ 0 V to a significant fraction of $V_{\text{ds,max}}$ during a commutation event. Accurate models attempting to capture the impact of C_{oss} in this operating regime will thus need to include this nonlinearity. At the end of a commutation event, the output capacitance of a switch which was previously ON is charged from ≈ 0 V to a combination of the flying capacitor and input voltages. During this process an amount of charge Q is transferred within the converter. For linear capacitances, this charge is $Q = CV_{\text{final}}$ where V_{final} is the voltage across

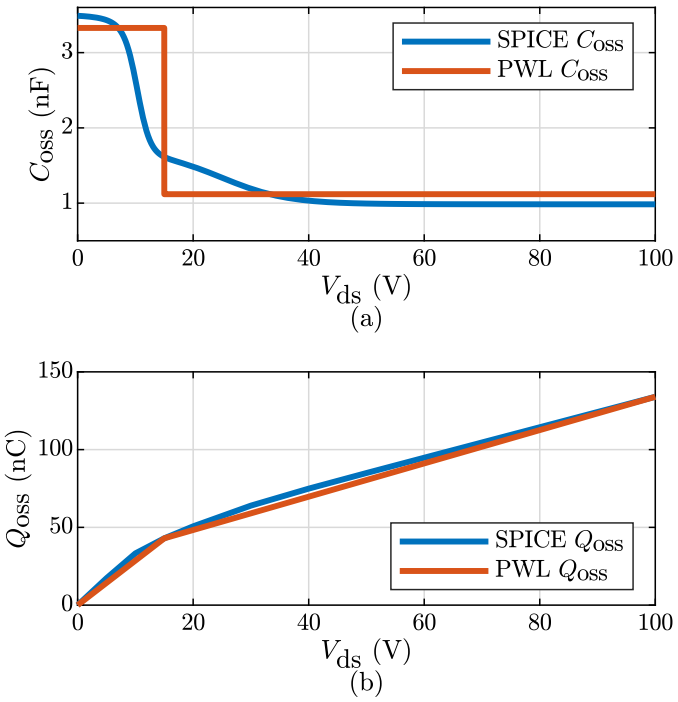

Fig. 7: (a) C_{oss} characteristics for an example EPC2302 device [25]. Data are obtained by differentiating the manufacturer provided LTSPICE Q-v curve. (b) Q_{oss} vs. V_{ds} for the EPC2302. This curve is well approximated by a two-part piecewise linear (PWL) function.

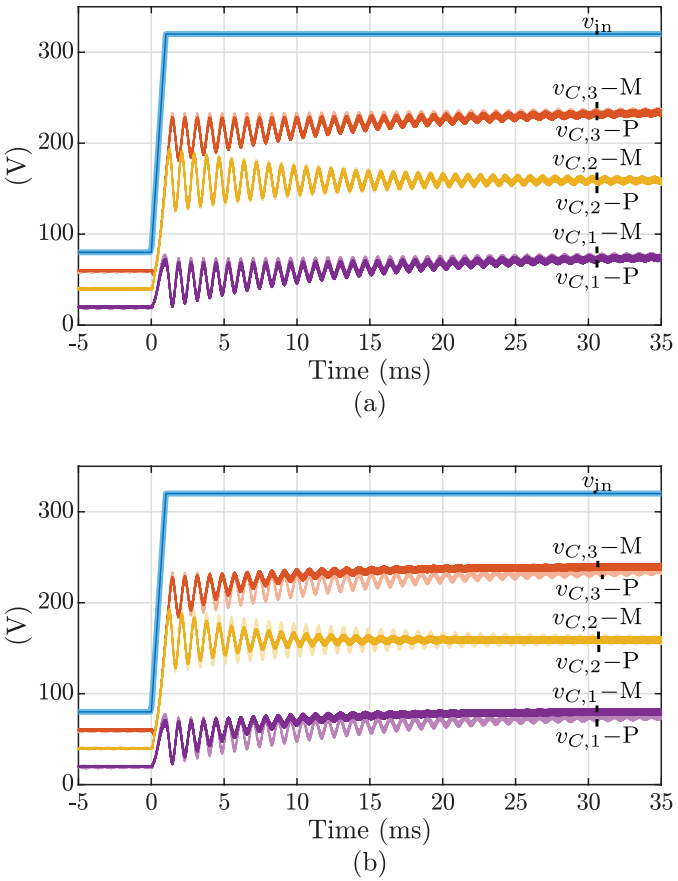

Fig. 8: Transient simulation of a five-level FCML converter including nonlinear C_{oss}. (a) Analytical model incorporating PWL C_{oss}. (b) Analytical model assuming a constant $C_{\text{oss}} = C_{\text{oss}}(v_{\text{ds}} = 0)$. Traces labeled $v_{C,i}-$P are from obtained from PLECS while $v_{C,i}-$M, are obtained from an analytical MATLAB simulation. The nonlinear C_{oss} are implemented in PLECS via variable capacitors and a look up table derived from the EPC2302 [25] datasheet.

the C_{oss} at the end of a commutation event. For nonlinear capacitances however, this charge Q is a nonlinear function of the final voltage. It is therefore necessary to know the charge flow induced by this voltage change across C_{oss} to determine the flying capacitor voltages after a commutation event.

Fig. 7(b) shows the Q_{oss} vs. V_{ds} curve for the EPC2302 obtained from the manufacturer provided LTSPICE model. Above a certain v_{ds} voltage (in this case $\approx 15\,\text{V}$), the slope of the curve decreases drastically. A faithful approximation is thus obtained through a two-part piecewise linear fit of the curve. This linear fit can be used to approximate the charge flow induced by the charging of the device's C_{oss} when solving for the flying capacitor voltages after a commutation event. This charge flow is described by

$$Q_{\text{oss}}(v) = \begin{cases} C_{\text{high}} v & v < V_{\text{b}} \\ C_{\text{high}} V_{\text{b}} + C_{\text{low}}(v - V_{\text{b}}) & v > V_{\text{b}} \end{cases}. \tag{11}$$

To illustrate this technique, we use the commutation event of the S_2 switching cell in a five-level FCML converter (illustrated in Fig. 4) and assume that $v_{\text{C},2}(t_{\text{f}}) - v_{\text{C},1}(t_{\text{f}}) > V_{\text{b}}$ as an example.

$$v_{C,2}(t_{\text{f}}) = v_{C,2}(0) - \frac{Q_{\text{flow}}}{C_2} \tag{12}$$

$$Q_{\text{flow}} = C_{\text{high}} V_{\text{b}} + C_{\text{low}}(v_{C,2}(t_{\text{f}}) - v_{C,1}(t_{\text{f}})) \tag{13}$$

Similar to (2), (13) expresses the charge flow as a function of the flying capacitor voltages at the end of a commutation event. The flying capacitor voltages can be solved in a similar manner to that presented in Section III-A.

Fig. 8 shows simulations of a five-level FCML converter which demonstrates the inclusion of the nonlinear C_{oss} and a piecewise linear approximation as a comparison. This simulation operates at a significantly higher v_{in}, up to 320 V. At this input voltage, the v_{ds} of the switches is up to 80 V, a large enough voltage to encounter the nonlinearity in the $C_{\text{oss}}(v_{\text{ds}})$ curve. A PLECS simulation using variable capacitors and look up tables implements the nonlinear C_{oss} curve from the EPC2302 [25] datasheet. Fig. 8(a) implements the piecewise linear C_{oss} model described above while Fig. 8(b) assumes that the C_{oss} is constant at the value of $C_{\text{oss}}(v_{\text{ds}} = 0\,\text{V})$. Since $C_{\text{oss}}(v_{\text{ds}})$ drops significantly above $v_{\text{ds}} = V_{\text{b}}$, assuming a constant C_{oss} predicts a circuit that exhibits a more damped response than the PLECS simulation.

D. Comparison to Insufficient Input Capacitance

The balancing mechanism produced by C_{oss}-induced charge flow serves to work in tandem with natural balancing and combat other imbalance mechanisms. One such imbalance mechanism found to have a significant impact in [18], [26] is that of input voltage ripple due to insufficient input capacitance. The authors in [18], [26] found that this imbalance mechanism had a much stronger impact than other mechanisms (e.g., gate driver delay mismatch).

TABLE II

SIMULATION PARAMETERS FOR STUDY IN SECTION III-D

Parameter	Value	Parameter	Value
V_{in}	50 V	R_{load}	2 Ω
L_{in}	1 μH	C_{out}	44 μF
R_{in}	0.1 Ω	L_{out}	10 μH
f_{sw}	120 kHz	D	0.251
C_{fly}	5 μF	C_{oss}	3.5 nF

TABLE III

CIRCUIT PARAMETERS USED IN EXPERIMENT IN FIG. 12

Component	Description	Part Name
Power Semicond.	200 V, 10 mΩ, 450 pF*	EPC2034
C_{fly}	4.4 μF	C5750X6S2W225K250KA
L_{out}	7.5 μH	XAL1510-153
C_{out}	0.6 μF	C5750C0G2J104J280KC

*This is the C_{oss} for $v_{\text{ds}} = V_{\text{rated}}/2$.

To compare the impacts of the C_{oss}-induced balancing mechanism and the insufficient input capacitance unbalancing mechanism, a simulation study was performed. In one simulation the influence of C_{oss}-induced charge flow is included while in the other, a traditional simulation (i.e., one without C_{oss}) is performed. The results of this study for a five-level FCML converter are shown in Fig. 9 with simulation parameters reported in Table II. A model excluding C_{oss} significantly overpredicts the steady-state error of the flying capacitor voltages. Although a model including C_{oss} accurately predicts a slight steady-state error, C_{oss}-induced charge flows drive the converter closer to the ideal balanced voltage distribution. Thus, including the impact of the C_{oss} charge flows in a converter model will predict a more realistic flying capacitor voltage distribution. Note, the steady-state values reported are the midrange of the capacitor voltage waveform (i.e., $[\max(v_{C,k}) - \min(v_{C,k})]/2$).

This example illustrates a key aspect of C_{oss}-induced balancing: The C_{oss}-induced charge flows by no means guarantee that the flying capacitor voltages will be perfectly balanced. Known imbalance mechanisms such as gate driver delay mismatch, switch on-resistance mismatch, and insufficient input capacitance work in opposition to C_{oss} charge flows and may result in a flying capacitor voltage distribution that deviates from the ideal. Additionally, the "strength" of the C_{oss}-induced balancing mechanism depends on both C_{oss} and the capacitance of the flying capacitors C_{fly}. Larger C_{oss} and smaller C_{fly} result in a more pronounced C_{oss}-induced balancing impact.

IV. Experimental Validation

To validate the theory of C_{oss}-induced natural balancing of the flying capacitor voltages, we imposed input voltage transients on several five-level FCML converter hardware prototypes and observed the oscillatory response of the flying capacitor voltages and the time-domain response of the circuit. To experimentally observe all pertinent frequencies, the step input voltage excitation must have a rise time sufficiently

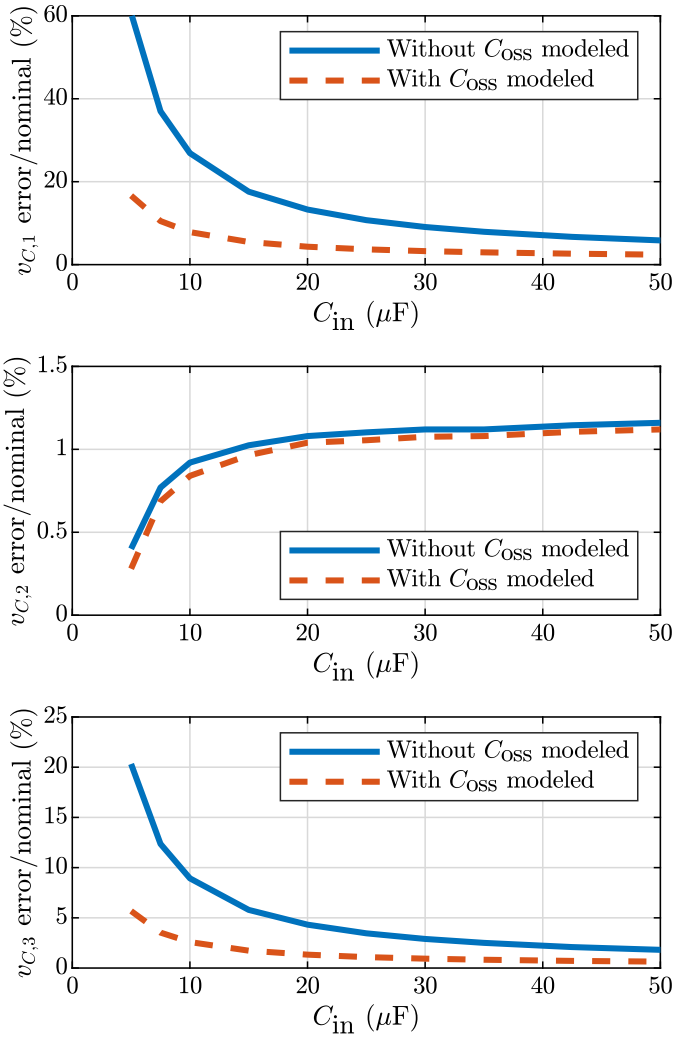

Fig. 9: Simulation study results investigating the steady-state error distribution of flying capacitor voltages. Including the impact of C_{oss}-induced charge flow predicts a more balanced distribution of flying capacitor voltages than a model without. Reported voltages are the midrange of the flying capacitor voltage waveform.

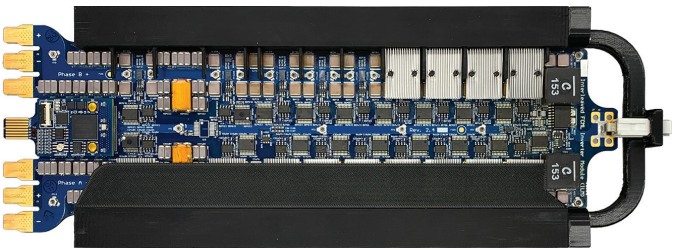

Fig. 10: A top-down view of the ten-level FCML converter prototype [5] used to obtain the experimental data shown in Fig. 12. Each PCB contains two, interleaved ten-level FCML converters switching at a frequency of 115 kHz with LC filters on board. Circuit parameters are given in Table III. The converter is configured for five-level operation by turning ON switches $S_{\text{H},5-9}$ and $S_{\text{L},5-9}$. One of the two FCML converters is left disconnected for the experiments performed in this work.

fast to excite higher frequency oscillations. To accomplish this, the circuit highlighted in the top left of Fig. 11 was devised. Before the step occurs, the gate of the MOSFET S_{tr} is held low (where $S(t)$ is the switching signal applied to S_{tr}) and $V_{\text{in,FCML}} = V_{\text{in}} - V_Z$, where V_Z is the Zener

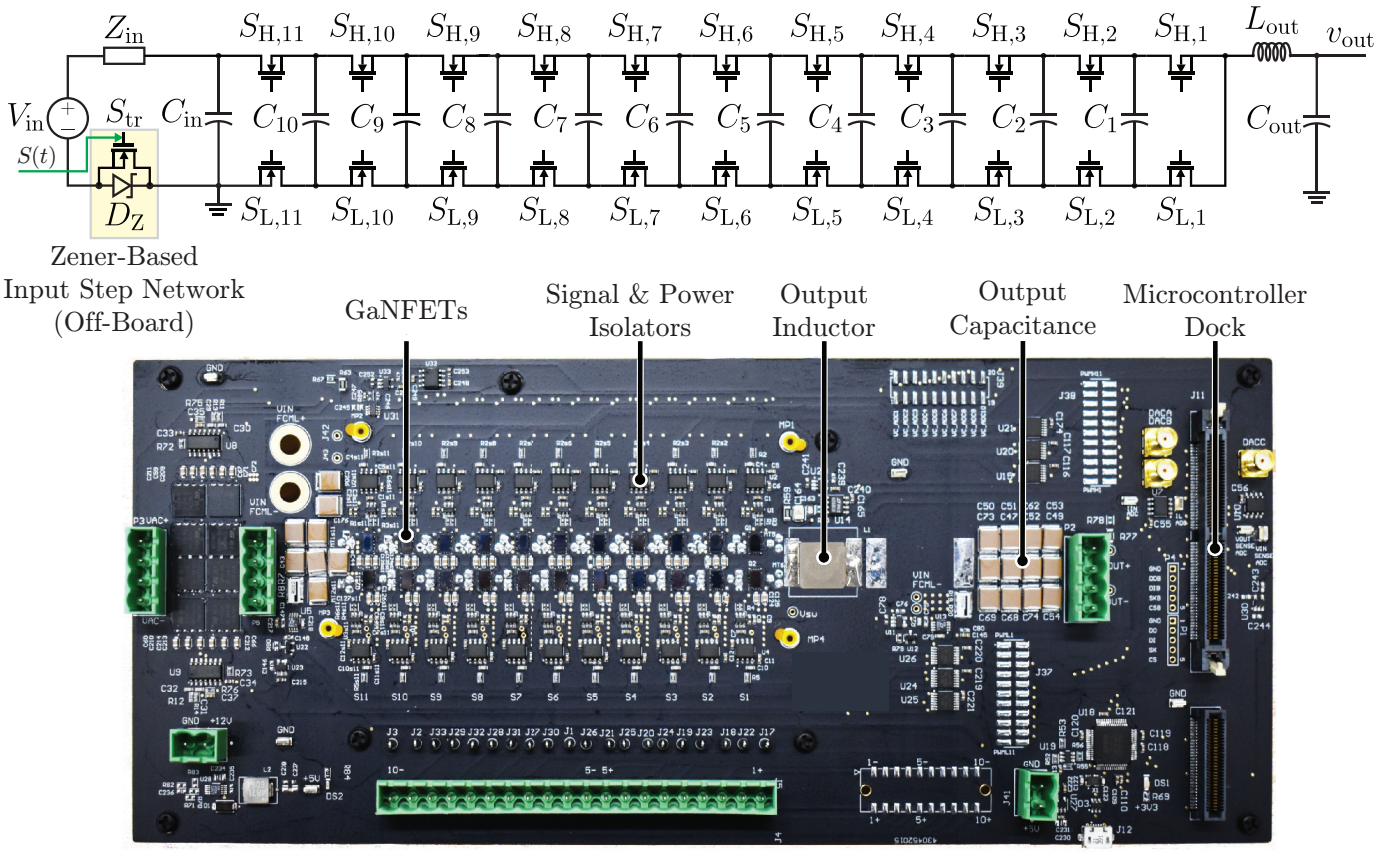

Fig. 11: Hardware photograph of prototype 2, a twelve-level FCML converter configured for five-level operation for the experiments performed in Fig. 13. Highlighted in the top left corner of the figure is the input step network. By adjusting the switching signal $S(t)$ from OFF to ON, the input voltage to the FCML is raised from $V_{in} - V_Z$ to V_{in} where V_Z is the Zener voltage of the external Zener diode D_Z in series with the input port of the FCML converter. The converter is configured for five-level operation by turning ON switches $S_{H,5-11}$ and $S_{L,5-11}$. Pertinent component parameters are given in Table IV.

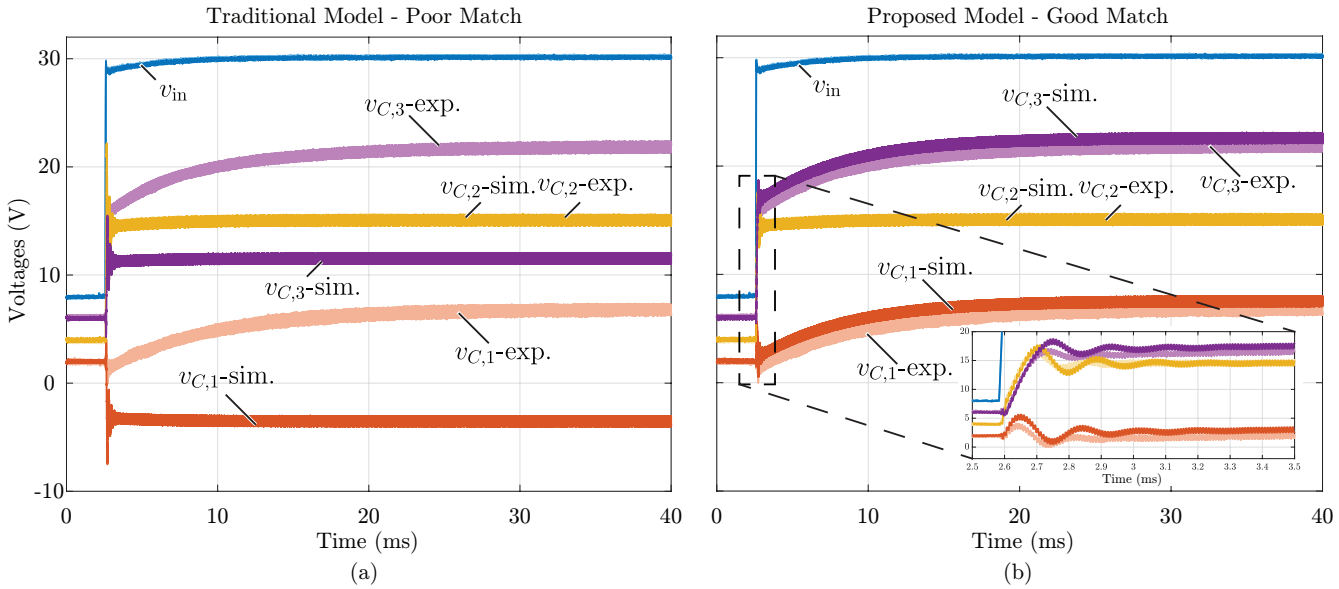

Fig. 12: Measured data from prototype 1, a five-level FCML [5] shown in Fig. 10. The FCML converter was excited with an ≈ 22.5 V input voltage step by the input step network highlighted in the top left of of Fig. 11 while operating at a duty cycle of 50%. Waveforms labeled "-sim." are simulation data while those labeled "-exp." are experimental data. (a) A simulation of a traditional model (i.e., one that does not include the impact of C_{oss}) compared with experiment. This model is clearly deficient in modeling the flying capacitor voltages' transient response. (b) Transient response of model including the impact of C_{oss} which predicts the flying capacitors natural convergence to their balanced values as experiment does. The inset in (b) shows a zoomed in view of the initial transient response of the flying capacitor voltages, which exhibits an oscillatory behavior. Both simulations employed the algorithm shown in Fig. 6.

TABLE IV

CIRCUIT PARAMETERS USED IN EXPERIMENTS IN FIG. 13

Component	Description	Part Name
Power Semicond.	100 V, 1.8 mΩ, 1 nF*	EPC2302
C_{fly}	8.8 μF	C5750X6S2W225K250KA
L_{out}	10 μH	IHLP5050CEER100M01
C_{out}	44 μF	C5750C0G2J104J280KC

*This is the C_{oss} for $v_{\text{ds}} = V_{\text{rated}}/2$.

TABLE V

PROTOTYPE PARAMETER COMPARISON

Parameter	Ratio
$R_{\text{ds},1}/R_{\text{ds},2}$	5.5
$C_{\text{fly},1}/C_{\text{fly},2}$	2
$C_{\text{out},1}/C_{\text{out},2}$	73
$C_{\text{oss},1}/C_{\text{oss},2}$	0.5

voltage, is applied to the FCML converter's input port. To activate the step, the gate of S_{tr} is pulled high, increasing the input voltage to the converter to V_{in} at a high slew rate. The outputs of both converters were connected to a constant 9.8 Ω load. To add further experimental evidence of the proposed C_{oss}-induced balancing theory, two FCML converter prototypes were developed. The prototypes differ significantly in converter parameters found to influence natural balancing dynamics. A summary of the differences in the two prototypes is provided in Table V.

A. Prototype 1 Validation

Presented in Fig. 12 are the results from this input voltage step study applied to the FCML converter shown in Fig. 10. As can be seen, both the analytical simulation and measured results agree very well when including the impact of C_{oss}-induced charge flow on the FCML converter as derived in Section III. If the impact of C_{oss} is not included and the FCML converter is modeled in the traditional way, the flying capacitor voltages will not converge to a balanced state as experiment does. These results are significant as they indicate that previous models of the FCML converter were inadequate as they neglected a key parasitic element in the circuit rather than a flaw in the analysis of the simplified circuit. The converter was operated with symmetric PS-PWM at a constant switching frequency of 115 kHz.

B. Prototype 2 Validation

Fig. 13(a) shows the transient response of prototype 2, shown in Fig. 13(b), while operating at a "balanced" conversion ratio of 25%. Since the RLC circuit dynamics investigated in previous works [22], [27] are now able to participate in driving the flying capacitors to their balanced voltages at this conversion ratio, the flying capacitor voltages converge much faster to their balanced values compared to the case of a conversion ratio of 50%, shown in Fig 13(b). The component parameters are given in Table IV and the converter was operated at a switching frequency of 75 kHz. The six highest

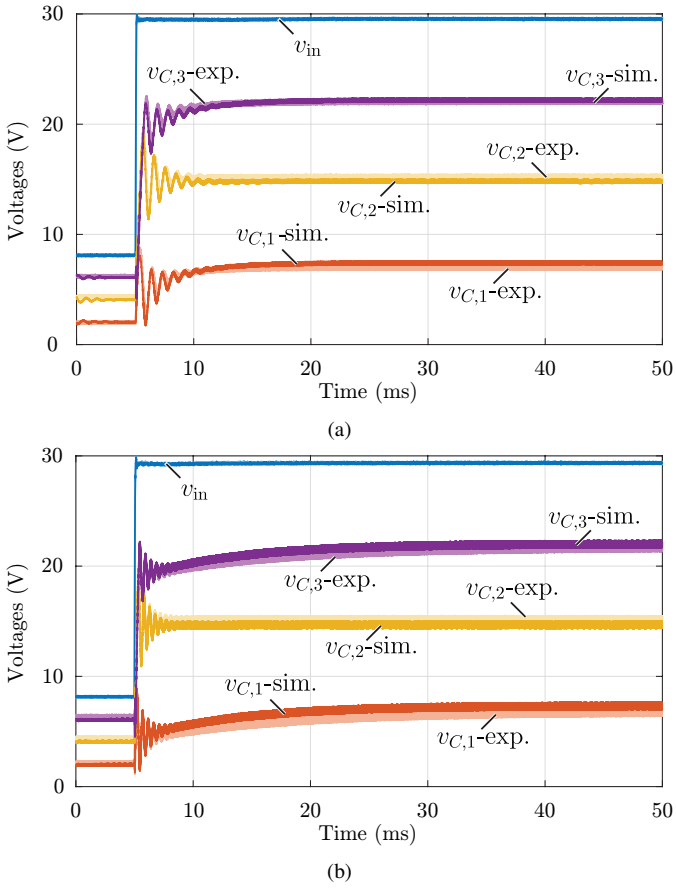

Fig. 13: Measured data from prototype 2, a five-level FCML shown in Fig. 11. (a) operated at a "balanced" conversion ratio of 25% and (b) an "unbalanced" conversion rate 50%. The input port of the FCML converter was excited with the same input voltage excitation as the experiment presented in Fig. 12. Compared to the experiment presented in Fig. 12, prototype 2 operates at a slower switching frequency (65%) and utilizes a larger output capacitor (73×). Despite these differences the presented model and experiment agree quite well. Waveforms labeled "-sim." are simulation data while those labeled "-exp." are experimental data.

voltage switch pairs were held constantly ON to generate the five-level converter.

V. Conclusion

This work has analyzed a key parasitic element, the switch output capacitance C_{oss}, and its impact on the ability of the flying capacitors within a FCML converter to balance to their desired voltages. Without the inclusion of this previously neglected balancing mechanism, simulation and analytical models of the FCML converter are unable to track experimental data. Ensuring model fidelity of the FCML converter is critical for both flying capacitor voltage estimation (e.g., for converter health monitoring) and active balancing control of the flying capacitor voltages. Although C_{oss}-induced balancing reduces switch voltage stress and inductor current harmonics, the flying capacitor voltages are balanced through a lossy mechanism. That is, FCML implementations which do not exhibit soft-switching will incur increased switching and/or overlap losses due to increased C_{oss}. Thus, attempts to force balanced flying capacitor voltages through increased C_{oss} will be met with increased switching losses. Using the modeling

techniques presented in this paper, the designer can assess the impact of parasitic device C_{oss} and whether additional external capacitance is beneficial.

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