UNIVERSITY OF CALIFORNIA SAN DIEGO

A Time Amplifier Assisted FDC and DTC Linearization for Digital Fractional-*N* PLLs

A dissertation submitted in partial satisfaction of the requirements for the degree

Doctor of Philosophy

in

Electrical Engineering (Electronic Circuits and Systems)

by

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The dissertation of Eslam Mohamed Sayed Ali Helal is approved, and it is acceptable in quality and form for publication on microfilm and electronically.

University of California San Diego

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DEDICATION

To my family

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ABSTRACT OF THE DISSERTATION

A Time Amplifier Assisted FDC and DTC Linearization for Digital Fractional-*N* PLLs

by

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Phase-locked loops (PLLs) are critical components in modern electronics communication systems, where they are used to synthesize local oscillator signals for modulation and demodulation in wireless transceivers. They are also used to clock digital-to-analog converters (DACs), analog-to-digital converters (ADCs), and digital processors.

Most PLLs incorporate either analog filters and voltage-controlled oscillators (VCOs) or digital filters and digitally-controlled oscillators (DCOs). The former are called analog PLLs

and the latter are called digital PLLs. To date, analog PLLs have the best phase error performance, but digital PLLs have the lowest circuit area and are more compatible with highly-scaled CMOS integrated circuit (IC) technology. Thus, improving the performance of digital PLLs has been the subject of intensive research for many years.

The first chapter of this dissertation presents time-difference amplifier (TA) and its application to a digital fractional-*N* phase-locked loop (PLL). The TA includes a delay-averaging linearity enhancement technique and the PLL is based on an improved dual-mode ring oscillator (DMRO) delta-sigma (ΔΣ) frequency-to-digital converter (FDC). The TA mitigates contributions to the PLL's phase noise from DMRO noise. The paper also presents a delay-free asynchronous DMRO phase sampling scheme, and the first experimental demonstration of a recently-proposed ΔΣ FDC digital gain calibration technique.

The second chapter of this dissertation presents an entirely digital background calibration technique that adaptively measures and cancels error resulting from DTC component mismatches that would otherwise degrade the phase noise of digital PLLs with DTC-based quantization noise cancellation. This technique indirectly addresses the well-known DTC nonlinearity problem because it facilitates the use of inherently-linear DTCs comprised of cascades of 1-bit DTC stages. Such DTCs tend to introduce excessive error from component mismatches, which has heretofore hindered their application to low-jitter PLLs. Published digital predistortion techniques provide an alternate means of mitigating DTC nonlinearity, but their convergence rates are at least an order of magnitude slower than that of the presented technique. It also presents a rigorous mathematical analysis that precisely quantifies the

calibration technique's settling performance and provides conditions under which it is unconditionally stable.

CHAPTER 1

A TIME AMPLIFIER ASSISTED FREQUENCY-TO-DIGITAL CONVERTER BASED DIGITAL FRACTIONAL-N PLL

Abstract— This paper presents a wide input-range delay chain based time amplifier (TA) and its application to a 6.5 GHz digital fractional-N phase-locked loop (PLL). The TA includes a delay-averaging linearity enhancement technique and the PLL is based on an improved dual-mode ring oscillator (DMRO) delta-sigma (ΔΣ) frequency-to-digital converter (FDC). The TA mitigates contributions to the PLL's phase noise from DMRO flicker noise, which would otherwise degrade the PLL's in-band phase noise, and from ΔΣ FDC quantization error, which would otherwise degrade the PLL's phase noise at high bandwidth settings. The paper also presents a delay-free asynchronous DMRO phase sampling scheme, and the first experimental demonstration of a recently-proposed ΔΣ FDC digital gain calibration technique. The TA assisted PLL achieves a random jitter of 145 fs_{rms}, a total jitter that ranges from 151 to 270 fs_{rms} as a result of fractional spurs, and a worst-case fractional spur of –49 dBc without requiring nonlinearity calibration.

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I. INTRODUCTION

Many types of phase-locked loops (PLLs) use a phase-frequency detector (PFD) with subsequent circuitry to measure the time differences between corresponding edges of the reference signal and a divided-down version of the PLL output signal. In such PLLs, using a time amplifier (TA) to amplify the edge time differences prior to the PFD and subsequently dividing the measured time differences by the gain of the TA attenuates the noise introduced by the measurement process without otherwise changing the loop dynamics.

Several TAs have been proposed over the last two decades [1]–[6], yet most suffer from significant drawbacks such as narrow input range [1]–[4], gain and input range dependency on technology parameters [1]–[4], high nonlinearity [1]–[5], a tradeoff between gain and input range [1]–[3], and a tradeoff between linear input range and noise [4]. The TA presented in [6] avoids most of these issues, but its relatively complicated implementation limits its noise performance which reduces its suitability for high-performance PLLs.

A low-noise inverter based delay chain TA with an analog delay-averaging nonlinearity mitigation technique is presented in this paper. The gain of the TA is nearly constant across a wide input range and is relatively insensitive to process, voltage and temperature (PVT) variations, as it depends on a ratio of inverter delays. The TA's principle of operation is similar to that of the TA presented in [6], but its implementation is simpler and it achieves better noise performance.

The proposed TA is demonstrated in the context of a 6.5 GHz digital fractional-N PLL based on a dual-mode ring oscillator (DMRO) delta-sigma ($\Delta\Sigma$) frequency-to-digital converter (FDC) [7]–[9]. As demonstrated in [7], this type of PLL can achieve good fractional spur

performance, but the DMRO's $1/f^3$ phase noise component degrades the PLL's in-band phase noise, and ΔΣ FDC quantization error limits the PLL's performance at high bandwidth settings. The PLL presented in this paper applies the proposed TA to overcome these issues by attenuating both noise sources by approximately 16 dB. Additionally, it incorporates and is the first experimental demonstration of several ΔΣ FDC improvements proposed in [9]. These improvements include an all-digital background gain calibration technique that simplifies the DMRO design, and various architecture changes that relax the ΔΣ FDC's timing constraints. A modified delay-free asynchronous DMRO phase sampling scheme is also incorporated in the PLL to further relax the ΔΣ FDC's timing constraints.

II. PLL HIGH-LEVEL ARCHITECTURE

A. PLL Overview

A high-level block diagram of the PLL is shown in Fig. 1(a), where $v_{\text{ref}}(t)$ and $v_{\text{PLL}}(t)$ are the output waveforms of the reference oscillator and the PLL, respectively. Ideally, $v_{\text{PLL}}(t)$ is periodic with frequency $f_{\text{PLL}} = 2(N+\alpha)f_{\text{ref}}$, where f_{ref} is the reference frequency, N is a positive integer, and α is a fractional frequency offset that ranges from –½ to ½.

The PLL consists of a TA-assisted DMRO ΔΣ FDC, a digital loop controller (DLC) with quantization noise cancellation (QNC), a digitally-controlled oscillator (DCO), and a divide-by-2 block with output $v_{\text{div2}}(t)$. The ΔΣ FDC generates two f_{ref}-rate digital sequences, $y[n]$ and $-\hat{e}_q[n]$. Ideally,

$$y[n] = -\alpha - e_{\text{PLL}}[n] + e_q[n] - 2e_q[n-1] + e_q[n-2], \tag{1}$$

where $e_{PLL}[n]$ is a measure of the PLL's average frequency error over the nth reference period and $e_q[n]$ is ΔΣ FDC quantization error [8], [9]. The sequence $\hat{e}_q[n]$ is an estimate of $e_q[n]$, and it is used to cancel most of the contribution of $e_q[n]$ prior to the digital loop filter (DLF) [7]–[12].

Fig. 1(a) and (1) imply that the DLF input, $p[n]$, is a measure of the PLL average phase error over the nth reference period plus a first-order highpass shaped version of the residual ΔΣ FDC quantization error, $e_q[n] - \hat{e}_q[n]$. The $p[n]$ sequence is lowpass filtered by the DLF, the output of which controls the DCO.

Fig. 1(b) shows a simplified block diagram of the TA-assisted DMRO ΔΣ FDC. It consists of a PFD, a DMRO, a digital ring phase calculator (RPC), a multi-modulus divider (MMD), and a TA. The signal $v_{samp}(t)$, which is an inverted version of $v_{ref}(t)$, is used within the RPC to sample the DMRO phase each reference period. The signal processing details of the RPC including the gain calibration technique are shown in Fig. 1(c) [9].

B. TA-Assisted DMRO ΔΣ FDC Behavior

An analysis similar to that presented in [8] but modified to include the TA and the improvements presented in [9] yields the ΔΣ FDC behavioral model shown in Fig. 2. In this model, $J_{TA}[n]$ is the TA's output jitter during the nth reference period, $\theta_{PLL}(t)$, $\theta_{ref}(t)$, and $\theta_{DMRO}(t)$ are the respective phase errors in cycles of $v_{PLL}(t)$, $v_{ref}(t)$, and the DMRO, τ_n, t_n, ρ_n and γ_n, for $n = 0, 1, 2, \ldots$, are the respective times of the nth rising edges of $v_{div}(t)$, $v_{ref}(t)$, $v_{TA}(t)$ and $v_{samp}(t)$, $T_{ref} = 1/f_{ref}$, and $T_{PLL} = 1/f_{PLL}$.[2] The behavioral model in Fig. 2 does not include error

[2] By definition, $\theta_{ref}(t)$ is the phase error at time t of $v_{ref}(t)$ in units of cycles of $v_{ref}(t)$. Accordingly, $T_{ref}\theta_{ref}(t)$ has units of seconds and it represents the reference oscillator's absolute jitter. Similarly, $\theta_{PLL}(t)$ represents the phase error at

sources corresponding to the PFD, the MMD, or the divide-by-2 block. Simulations performed by the authors indicate that these blocks do not significantly affect the PLL's phase noise, so they are omitted in the figure for simplicity.

The MMD is identical to those in analog PLLs, so, as illustrated in Fig. 2, τ_n is an accumulated version of $2T_{\mathrm{PLL}}(N - \nu[n-1])$ plus noise, where $2T_{\mathrm{PLL}}$ is the divide-by-2 block's output period and $N - \nu[n-1]$ is the MMD modulus.

As explained in Section III-B, the TA is implemented as a chain of N_{TA} nominally identical delay cells. The propagation delay of each delay cell is τ_{fast} when $v_{\mathrm{ref}}(t)$ is low and τ_{slow} otherwise, where $\tau_{\mathrm{fast}} < \tau_{\mathrm{slow}}$. As also explained in Section III-B, the TA delays the rising edges of $v_{\mathrm{div}}(t)$ such that the pulse-width of the PFD output, $u(t)$, during the nth reference period, i.e., $u_n = \rho_n - t_n$, is given by

$$u_n = -A_{\mathrm{TA}}\left(t_n - \tau_n\right) + N_{\mathrm{TA}}\tau_{\mathrm{slow}} + J_{\mathrm{TA}}[n], \tag{2}$$

where

$$A_{\mathrm{TA}} = \tau_{\mathrm{slow}} / \tau_{\mathrm{fast}} \tag{3}$$

is the TA gain and $N_{\mathrm{TA}}\tau_{\mathrm{slow}}$ is a constant offset term introduced as a byproduct of the TA's operation. Thus, the combined behavior of the TA and the PFD is equivalent to that of an inverting amplifier with input $t_n - \tau_n$ and additive noise and offset terms.

The DMRO is a ring of N_R nominally identical delay cells. Ideally, its frequency is f_{high} when $u(t)$ is high and f_{low} otherwise, where $f_{\mathrm{high}} > f_{\mathrm{low}}$. As explained in [8] and illustrated in Fig. 2, the behavior of the DMRO is that of an accumulator with gain

time t of $v_{\mathrm{PLL}}(t)$ in units of cycles of $v_{\mathrm{PLL}}(t)$, so $T_{\mathrm{PLL}}\theta_{\mathrm{PLL}}(t)$ has units of seconds and it represents the PLL output signal's absolute jitter.

$$A_{\mathrm{DMRO}} = f_{\mathrm{high}} - f_{\mathrm{low}} \tag{4}$$

followed by an additive noise source, an additive $nf_{\mathrm{low}}T_{\mathrm{ref}}$ term, and a quantizer, Q_r, with quantization step-size $\Delta_r = (2N_R)^{-1}$.

As explained in [9], the RPC extracts the information encoded in the sampled and quantized DMRO phase and computes a fixed-point measure of $-\alpha - e_{\mathrm{PLL}}[n]$ each reference period. This measure is quantized to the nearest integer to compute $y[n]$, and the resulting quantization error, $\hat{e}_q[n]$, is used within the DLC to perform QNC. This *coarse* quantization operation is represented by a unity step-size quantizer, Q_c, in Fig. 2.

An analysis similar to that presented in [9] shows that the DMRO locks to an average frequency of Mf_{ref}, and the average $u(t)$ pulse width, $T_{\bar{u}}$, is

$$T_{\bar{u}} = A_{\mathrm{DMRO}}^{-1}\left(M - T_{\mathrm{ref}}\, f_{\mathrm{low}}\right). \tag{5}$$

The parameter M is chosen so that the falling edges of $u(t)$ occur between rising edges of $v_{\mathrm{ref}}(t)$ and $v_{\mathrm{samp}}(t)$, i.e., $t_n < \rho_n < \gamma_n$ for all n. This with the TA operation described in Section III-B causes the rising edges of $v_{\mathrm{div}}(t)$ to precede the rising edges of $v_{\mathrm{ref}}(t)$, i.e., $\tau_n < t_n$ for all n, so that

$$\gamma_{n-1} < \tau_n < t_n < \rho_n < \gamma_n \tag{6}$$

when the PLL is locked.

A simplified version of the TA-assisted ΔΣ FDC behavioral model that is valid for constant g_n is shown within the dashed contour in Fig. 2, wherein all noise components are input-referred and lumped into $e_{\mathrm{PLL}}[n]$, the offset components are omitted, and the quantizers Q_r and Q_c are replaced by their respective additive error sequences, $e_{qr}[n]$ and $\hat{e}_q[n]$. The model implies that the behavior of the ΔΣ FDC when

$$g_n = \frac{1}{2T_{\mathrm{PLL}} A_{\mathrm{TA}} A_{\mathrm{DMRO}}} \tag{7}$$

is identical to that of a second-order ΔΣ modulator, the output of which is given by (1) with

$$e_q[n] = g_n e_{qr}[n] + \hat{e}_q[n]. \tag{8}$$

As explained in [9], when (7) is not satisfied, $\hat{e}_q[n]$ is imperfectly canceled by QNC so it leaks into the DLF input, thereby degrading the PLL's phase noise. The gain calibration technique shown in Fig. 1(c) causes g_n to converge to the right side of (7), which effectively circumvents this problem [9].

It follows from Fig. 2 and (7) that the power contribution of the DMRO's phase noise to $y[n]$, and, hence, to the PLL's phase noise, is proportional to both A_{TA}^{-2} and A_{DMRO}^{-2}. The original DMRO ΔΣ FDC PLL presented in [7] does not incorporate a TA, so it corresponds to the case of $A_{\mathrm{TA}} = 1$ in (7), and its in-band phase noise is dominated by the DMRO's $1/f^3$ phase noise component. In the absence of a TA, modifying the DMRO to increase A_{DMRO} and/or reduce the DMRO's $1/f^3$ phase noise component are the only options that would have mitigated this problem.

Unfortunately, these options are not attractive. In principle, increasing the widths of the transistors that make up the DMRO's delay cells increases A_{DMRO} via **Error! Reference source not found.** and decreases the DMRO's $1/f^3$ phase noise component by reducing transistor flicker noise, but in practice A_{DMRO} increases only up to a point beyond which parasitic capacitances and supply resistance cause A_{DMRO} to decrease with further transistor width increases. After this point, A_{DMRO} can only be increased further by reducing the number of DMRO delay cells, N_R. Given that $e_{qr}[n]$ is proportional to $\Delta_r = (2N_R)^{-1}$, this would

reduce the effectiveness of QNC, which would require the PLL bandwidth to be reduced to compensate for the increase in quantization noise power. Interestingly, increasing the number of DMRO delay cells does provide a modest net benefit. For example, doubling N_R reduces $A_{\mathrm{DMRO}}{}^2$ by 6 dB, but as shown in [13] it decreases the power of the DMRO's $1/f^3$ phase noise component by 9 dB. Hence, each doubling of N_R reduces the power contribution of the DMRO's $1/f^3$ phase noise component to the PLL's phase by 3 dB. Unfortunately, achieving large phase noise reductions in this manner typically requires impractically large numbers of DMRO delay cells.

These tradeoffs are avoided in this work because the TA provides amplification prior to the DMRO. As described above, the DMRO's contribution to the PLL's phase noise is proportional to $A_{\mathrm{TA}}{}^{-2}$, so each doubling of A_{TA} reduces the power of the DMRO's contribution to the PLL's phase noise by 6 dB.

Both the TA and the DMRO are made up of dual-delay inverter based delay cells, but the TA is an open-loop chain and the DMRO is a ring, so transistor flicker noise gives rise to $1/f$ noise in $J_{\mathrm{TA}}[n]$ and $1/f^3$ noise in $\theta_{\mathrm{DMRO}}(\gamma_n)$. Nevertheless, as implied by Fig. 2, the contributions of $J_{\mathrm{TA}}[n]$ and $\theta_{\mathrm{DMRO}}(\gamma_n)$ to $y[n]$ are first-order and second-order highpass shaped, respectively, so flicker noise injected by each TA transistor has a similar contribution to the PLL's phase noise as that injected by each DMRO transistor.

Yet it is not the case that using the TA simply transfers the problem of reducing the effect of flicker noise from the DMRO to the TA. As implied by (3), A_{TA} depends on a ratio of inverter delays, so the TA's flicker noise can be reduced by increasing transistor widths without significantly decreasing A_{TA} or incurring other side effects similar to those mentioned above

that come with reducing the DMRO's $1/f^3$ phase noise component. Furthermore, the TA is only active for a fraction of each reference period, whereas the DMRO operates continuously. As the power of the noise introduced by a chain of inverters grows at least proportionally to the number of inverters that transition as explained in [13], it follows that the TA noise contribution can be made small compared to that of the DMRO.

For instance, in the implemented PLL, 100 TA delay cells transition each reference period, whereas 660 DMRO delay cells transition each reference period on average. Moreover, in contrast to the TA, each delay cell within the DMRO transitions four to six times each reference period. Given that flicker noise changes slowly relative to T_{ref}, having four to six transitions per reference period effectively increases each delay cell's power contribution to the DMRO's $1/f^3$ phase noise component by approximately 6 to 9 dB compared to what the delay cell would have contributed had it only transitioned once per reference period. These features made it possible for the TA to suppress the DMRO's contribution to the PLL's phase noise without the TA's noise being a limitation.

III. IMPLEMENTATION DETAILS

The implemented PLL is shown in Fig. 3. It has four power supply domains, which correspond to the dashed boxes in Fig. 3. The place-and-route (PNR) digital block is clocked at a rate of $f_{\text{PLL}}/8$ by $v_{\text{clk}}(t)$ and contains the DLC, the DCO control logic, the $\Delta\Sigma$ FDC's z^{-1} register, and all RPC components except the cycle counter and phase-sampling flip-flops.

As shown in Fig. 4, the PNR digital block comprises three sub-blocks, FDC digital, DLC, and DCO digital, that are clocked sequentially by gated versions of $v_{\text{clk}}(t)$. The signal

$v_{rdy}(t)$ is timed such that it goes high once each reference period when the DMRO phase information is ready to be processed by the PNR digital block. The clk_{FDC}, clk_{DLC} and clk_{DCO} clock signals are generated by the flip-flop chain driven by $v_{rdy}(t)$, and the numbers of flip-flops between adjacent clock signals are such that enough time is allocated for each digital sub-block to meet digital timing constraints across PVT corners for an input clock frequency of 1 GHz.

The details of the sub-blocks within the PNR digital block are similar to those presented in [7]. Most of the differences are in the ΔΣ FDC's digital sub-block to incorporate the improvements proposed in [9] which include the gain calibration technique shown in Fig. 1(c). As explained in [9], the f_{ref}-rate multiplier prior to the RPC's accumulator in Fig. 1(c) represents most of the gain calibration technique's added complexity. Its inputs have respective bit-widths of 12 and 14 bits, and its output has a bit-width of 25 bits. The RPC's accumulator would have required 24 bits in the absence of the multiplier, so the inclusion of the gain calibration technique negligibly increases the power consumption and circuit area of the RPC accumulator and subsequent digital sub-blocks. Furthermore, the relaxed timing of the implemented ΔΣ FDC architecture relative to that presented in [7] causes the power consumption and circuit area of the multiplier to be negligible relative to those of the overall digital block.

A. Timing

As shown in the timing diagram of Fig. 5, the MMD loads its inputs, $mod_4[n]$ and $mod_5[n]$, $30T_{PLL}$ after the rising edge of $v_{div}(t)$. Fig. 5 implies that for the earliest possible $v_{div}(t)$ rising edge, the ΔΣ FDC portion of the PNR digital block has a time budget of about $51T_{PLL} \cong \frac{3}{4}T_{ref}$ to generate its outputs after $v_{rdy}(t)$ goes high. This constraint is easy to satisfy in practice as the ΔΣ FDC logic does not require more than two periods of $v_{clk}(t)$ (i.e., $16T_{PLL}$) to compute

the MMD inputs. Accordingly, the implemented PLL has no significant timing bottle-necks, which makes its implementation much simpler than that of prior ΔΣ FDCs [7], [8], [12], [14], [15].

B. TA

Fig. 6(a) shows a conceptual block diagram of the proposed TA. It consists of N_{TA} nominally identical inverter based delay cells, where N_{TA} is an even number. The delay of each delay cell, τ_{delay}, takes on one of two values: τ_{fast} when $v_{\mathrm{ref}}(t)$ is low and τ_{slow} when $v_{\mathrm{ref}}(t)$ is high.

It follows from (6) that during the nth reference period, the time, t_n, of the rising edge of $v_{\mathrm{ref}}(t)$ occurs after the time, τ_n, of the corresponding rising edge of $v_{\mathrm{div}}(t)$, but before the time, ρ_n, at which the rising edge of $v_{\mathrm{div}}(t)$ finishes propagating through the TA. Therefore, at time τ_n, when the rising edge of $v_{\mathrm{div}}(t)$ starts propagating through the TA, the delay cells have a delay of τ_{fast}. When $v_{\mathrm{ref}}(t)$ goes high at time t_n, the rising edge of $v_{\mathrm{div}}(t)$ has already propagated through $\lfloor (t_n-\tau_n)/\tau_{\mathrm{fast}} \rfloor$ delay cells and a fraction, given by $(t_n-\tau_n)/\tau_{\mathrm{fast}} - \lfloor (t_n-\tau_n)/\tau_{\mathrm{fast}} \rfloor$, of a delay cell. Thus, at time t_n, the rising edge of $v_{\mathrm{div}}(t)$ has propagated through an equivalent of $(t_n-\tau_n)/\tau_{\mathrm{fast}}$ delay cells, including both integer and fractional parts. At this time, the TA's delay cells are switched to have a delay of τ_{slow}, so the remaining TA delay cells through which the edge must propagate contribute a combined delay of $(N_{\mathrm{TA}}-(t_n-\tau_n)/\tau_{\mathrm{fast}})\tau_{\mathrm{slow}}$. Consequently, the time, ρ_n, at which $v_{\mathrm{TA}}(t)$ goes high is given by

$$\rho_n = \tau_n + \left(\frac{t_n-\tau_n}{\tau_{\mathrm{fast}}}\right)\tau_{\mathrm{fast}} + \left(N_{\mathrm{TA}} - \frac{t_n-\tau_n}{\tau_{\mathrm{fast}}}\right)\tau_{\mathrm{slow}}. \tag{9}$$

This implies that the pulse-width of $u(t)$ during the nth reference period, $u_n = \rho_n - t_n$, is given by **Error! Reference source not found.** with A_{TA} given by (3), where the jitter term, $J_{TA}[n]$, represents the combined effect of all transistor noise sources within the TA.

It follows from the explanation above that for the TA to provide time-difference amplification it is necessary to ensure

$$0 < t_n - \tau_n < N_{TA}\tau_{fast}. \tag{10}$$

Otherwise, the TA would only introduce a fixed delay between $v_{div}(t)$ and $v_{TA}(t)$. Fig. 5 implies that the time at which the MMD loads its inputs also imposes a constraint on the maximum value of $t_n - \tau_n$. Specifically, the MMD must load its inputs at the time of the rising edge of clk_{FDC} at the earliest, which can occur up to $37T_{PLL}$ after the falling edge of $v_{ref}(t)$. Therefore, $t_n - \tau_n$ must satisfy

$$t_n - \tau_n < \tfrac{1}{2}T_{ref} - 7T_{PLL} \tag{11}$$

in addition to (10). Moreover, for the ΔΣ FDC to work properly, $u(t)$ must go low before the DMRO phase is sampled at time γ_n, which requires

$$0 < u_n < \tfrac{1}{2}T_{ref} + 10T_{PLL}. \tag{12}$$

Equations (10)-(12) impose design constraints on the TA parameters N_{TA}, τ_{slow}, τ_{fast} and A_{TA}.

As shown in Fig. 6(b), each of the TA's dual-delay inverters consists of a standard inverter in parallel with a larger tri-state inverter. When $v_{ref}(t)$ goes high, the tri-state inverter is

disabled by disconnecting its ground and power supply terminals from the supply rails, thereby increasing τ_{delay} from τ_{fast} to τ_{slow}.

Ideally, τ_{delay} changes instantaneously from τ_{fast} to τ_{slow} when $v_{ref}(t)$ goes high, in which case the TA performs linear amplification. Unfortunately, the τ_{fast}-to-τ_{slow} transitions are non-instantaneous in practice, which causes TA nonlinearity. Moreover, as illustrated in Fig. 6(c), this transition also depends on whether the cell's input, $d_{n-1}(t)$, goes from low to high or vice versa.

The TA topology shown in Fig. 7(a) is proposed to reduce such nonlinearity. It consists of two nominally identical delay chains in parallel, where the input of one delay chain is an inverted version of that of the other delay chain, both delay chains are controlled by $v_{ref}(t)$, and each pair of parallel delay cells are cross-connected with averaging resistors. As shown in Fig. 7(a) for the top and bottom delay chains in isolation, the odd-indexed and even-indexed delay cells have inputs that transition in opposite directions, so they have different τ_{fast}-to-τ_{slow} transitions. This causes a quasi-periodic artifact in the input-output characteristics of the delay chains. Driving the bottom delay chain by an inverted version of $v_{div}(t)$ causes its input-output characteristic to be shifted with respect to that of the top delay chain such that, when averaged via the cross-coupled resistor network, the non-linearity of the cross-coupled delay chains is considerably smaller than that of either delay chain in isolation. Behavioral simulations of the PLL in which the TA's nonlinear behavior is considered and all other spur-generation mechanisms are neglected suggest that the power of the PLL's worst-case fractional spur decreases by 7 dB when the proposed nonlinearity mitigation technique is used.

In addition to having improved linearity, the proposed TA topology's pseudo-differential nature can be exploited to implement a TA power-saving (PS) mode. Without the PS mode, the falling edge of $v_{div}(t)$ propagates through the TA each reference period. This resets the delay cells' states for the next rising edge of $v_{div}(t)$, but the power consumed by the resulting delay cell transitions represents a significant portion of the TA's total power consumption. The idea behind the PS mode is to swap the differential inputs and swap the differential outputs of the TA each reference period to obviate the need to reset the delay cells, so the falling edge of $v_{div}(t)$ can be prevented from propagating through the TA to save power.

The implemented TA, which includes the non-linearity mitigation technique and PS mode option as described above, is shown in Fig. 7(b). It comprises the TA core shown in Fig. 7(a) as well as input and output swapping circuitry used when the PS mode is enabled. The transistor-level details of the TA's delay cells are shown in Fig 7(c). The TA core was designed to maximize the value of A_{TA} while satisfying the constraints in (10)-(12). Specifically, N_{TA} = 100, τ_{fast} = 10 ps, τ_{slow} = 70 ps and A_{TA} = 7. Simulation results predict that the TA's gain varies by ±7% across process corners, ±10% across process corners and temperature variations (0 °C to 85 °C), and ±14% across process corners, temperature variations, and voltage variations (±10%).

The PS mode is enabled and disabled via the PS_{en} signal. When enabled, the $\phi_1(t)$ and $\phi_2(t)$ signals are used to implement the input and output swapping operations. The signal $\phi_1(t)$, which is derived from $v_{div}(t)$, is used to swap the inputs and the outputs of the TA core each reference period, whereas $\phi_2(t)$ is used to control the input and output latches. As illustrated in the timing diagram shown in Fig. 7(b), these latches prevent the falling edges of $v_{div}(t)$ from

propagating through the TA core, and also prevent the output swapping circuitry from disturbing $v_{TA}(t)$ while the swapping occurs.

The TA was laid out such that systematic mismatch among its unit cells is negligible, and the unit cells are sized such that the power of the PLL's worst-case fractional spur caused by random mismatches among the TA's delay cells is approximately –50 dBc. This was determined by performing a Monte Carlo simulation in Cadence to obtain 90 different TA input-output characteristics, and the results were imported into a bit-exact, event-driven, custom behavioral PLL simulator. Fig. 7(d) shows a histogram of the simulated PLL's worst-case fractional spur power. As shown in the figure, the worst-case fractional spur power's expected value is –51.7 dBc, and its standard deviation is 2.5 dBc.

As mentioned in Section I, the proposed TA achieves better noise performance than a comparably configured TA of the type presented in [6]. One reason for this difference is that the TA in [6] incorporates two ring oscillators that both contribute noise to the output whereas the proposed TA incorporates a single delay-chain that contributes noise to the output. Another reason is that TA presented in [6] requires NAND gate-based delay cells instead of inverter-based delay cells which each introduce more phase noise than comparable inverter-based delay elements.

C. DMRO and Phase Sampling Scheme

The DMRO, which is shown in Fig. 8, consists of $N_R = 127$ inverter delay cells and has $A_{DMRO} = 670$ MHz ($f_{high} = 730$ MHz and $f_{low} = 60$ MHz). Each DMRO delay cell contains a dual-delay inverter that is similar to that used in the TA. It includes a standard ×1 inverter in parallel with a ×16 tri-state inverter, and the tri-state inverter's power and ground lines are connected

to or disconnected from the supply rails when $u(t)$ is high or low, respectively. This modulates each delay cell's propagation delay such that the DMRO frequency is f_{high} when $u(t)$ is high and f_{low} when $u(t)$ is low. In both cases, the DMRO outputs swing from rail-to-rail, which allows the DMRO outputs to drive standard digital logic without the need for level-shifting. The ×2 inverter shown within the dashed box in Fig. 8 is used to buffer the delay cell's input to reduce the disturbance to the DMRO when its phase is sampled.

As explained in Section II-B, the TA causes the PLL phase noise contributed by the DMRO to be attenuated in power by a factor of A_{TA}^2. Additionally, the DMRO's $1/f^3$ phase noise component is further mitigated by using a large number of stages [13]. This comes at the expense of higher digital complexity and higher power consumption, primarily due to the charging and discharging of the gates controlled by $u(t)$.

To prevent the DMRO from running with multiple stages transitioning simultaneously, even for a brief period of time, the first delay cell includes a switch between the ground terminal of the ×1 inverter and the ground rail. At startup, both $u(t)$ and the enable signal are set low. This opens the ring so that any transition propagating through it eventually reaches the first stage and stops propagating. The switch is subsequently closed after which the DMRO operates normally.

The DMRO phase sampling scheme is shown in Fig. 8. As explained below, it addresses the issue that the sampling clock, $v_{samp}(t)$, and the DMRO are asynchronous yet avoids the delay incurred by the DMRO sampling scheme in [7]. It consists of a cycle counter followed by sampling flip-flops and a phase decoder. The principle behind the sampling of the cycle

counter's outputs is based on that of the asynchronous sampling schemes presented in [16], [17]. To the knowledge of the authors, the proposed phase decoder implementation described below is introduced for the first time in this work.

The cycle counter consists of two 4-bit counters that are clocked, respectively, by the rising and falling edges of the DMRO delay cell with output $d_1(t)$. On each rising edge of the f_{ref}-rate signal $v_{\text{samp}}(t)$, the counter outputs $c_{\text{pos}}(t)$ and $c_{\text{neg}}(t)$ are sampled to generate $c_{\text{pos}}[n]$ and $c_{\text{neg}}[n]$, and the DMRO outputs $d_1(t)$, $d_2(t)$, …, $d_{127}(t)$ are sampled to generate $d_1[n]$, $d_2[n]$, …, $d_{127}[n]$. The phase decoder consists of a lookup table (LUT) that quantizes the sampled DMRO outputs to a 10-bit sequence, $t_R[n]$, which represents the fractional part of the sampled DMRO phase, and logic that computes $c_R[n]$, which represents the integer part of the sampled DMRO phase. The number of bits of $t_R[n]$ was chosen to ensure that the contribution to the PLL's phase noise from the error introduced by the LUT's quantization operation is negligible compared to those of the other error sources.

The top and bottom counters in the cycle counter are clocked when $t_R[n] \cong 0$ and $t_R[n] \cong 126\Delta_r$, respectively, where $\Delta_r = 1/254$. Hence, $t_R[n]$ can be used to determine which counter output was not changing when the sampling event occurred. As shown in Fig. 8, whenever $t_R[n]$ is between $63\Delta_r$ and $189\Delta_r$, $c_R[n]$ is set to $c_{\text{pos}}[n]$. Ideally, $c_R[n]$ should be set to $c_{\text{neg}}[n]$ when $t_R[n]$ is between $190\Delta_r$ and $253\Delta_r$, and to $c_{\text{neg}}[n] + 1$ when $t_R[n]$ is between 0 and $62\Delta_r$ so as to account for the bottom counter being clocked half a DMRO cycle after the top counter is clocked. Yet to work correctly this would require $c_{\text{pos}}(0) = c_{\text{neg}}(0)$ and the initial DMRO fractional phase to be such that the top counter is clocked before the bottom counter after startup, which are hard to ensure in practice.

These requirements are avoided via the $c_{\text{corr}}[n]$ correction logic shown in Fig. 8. As both sampled counter outputs are reliable when $t_R[n]$ is around $63\Delta_r$ and $190\Delta_r$, the $c_{\text{corr}}[n]$ logic block in Fig. 8 computes

$$c_{\text{corr}}[n]=\begin{cases} c_{\text{pos}}[n]-c_{\text{neg}}[n]-1, & \text{if } t_R[n]\in[53\Delta_r, 73\Delta_r], \\ c_{\text{pos}}[n]-c_{\text{neg}}[n], & \text{if } t_R[n]\in[180\Delta_r, 200\Delta_r], \\ c_{\text{corr}}[n-1] & \text{otherwise,} \end{cases} \tag{13}$$

and $c_R[n]$ is set to $c_{\text{neg}}[n] + c_{\text{corr}}[n]$ when $t_R[n]$ is between $190\Delta_r$ and $253\Delta_r$, to $c_{\text{neg}}[n] + c_{\text{corr}}[n] + 1$ when $t_R[n]$ is between 0 and $62\Delta_r$, and to $c_{\text{pos}}[n]$ otherwise.

D. MMD

As shown in Fig. 9, the MMD consists of a finite-state machine (FSM), a 4/5 prescaler, an edge-select flip-flop and a resynchronization flip-flop. As explained below, the MMD causes the rising edges of $v_{\text{div}}(t)$ during the nth and (n+1)th reference periods to be separated by $N - v[n]$ periods of $v_{\text{div2}}(t)$.

When the FSM's $p_{\text{sel}}(t)$ output bit is low, the prescaler divides by 4. Otherwise, it divides by 5. At the beginning of each MMD cycle, the FSM sets $p_{\text{sel}}(t)$ low for five periods of $v_{\text{pres}}(t)$, so the first five periods of $v_{\text{pres}}(t)$ each have a duration of four $v_{\text{div2}}(t)$ periods. Then, the FSM sets $p_{\text{sel}}(t)$ so that $\text{mod}_4[n]$ counts to 4 followed by $\text{mod}_5[n]$ counts to 5 occur, where

$$\begin{aligned} \text{mod}_5[n] &= N - v[n] - 20 - 4\left\lfloor \left(N - v[n] - 20\right)/4 \right\rfloor \text{ and} \\ \text{mod}_4[n] &= \left\lfloor \left(N - v[n] - 20\right)/4 \right\rfloor - \text{mod}_5[n], \end{aligned} \tag{14}$$

after which $N - v[n]$ periods of $v_{\text{div2}}(t)$ will have occurred.

As illustrated in the timing diagram shown in Fig. 9 for the example case of $\mathrm{mod}_5[n] = 1$, the FSM's $p_{\mathrm{pass}}(t)$ output goes high at the start of the last full $v_{\mathrm{pres}}(t)$ period prior to the next rising edge of $v_{\mathrm{div}}(t)$, which causes the edge-select flip-flop's output to go high on the next rising edge of $v_{\mathrm{pres}}(t)$. The resynchronization flip-flop samples the edge-select flip-flop output on the next rising edge of $v_{\mathrm{div2}}(t)$ to prevent the MMD output edge from being corrupted by noise and modulus-dependent delay error that originated in the prior MMD components.

All MMD blocks were built using standard cells, with the exception of the resynchronization flip-flop which was custom-designed to minimize its contribution to the PLL's phase noise.

E. DCO

The DCO is similar to that presented in [7]. It consists of a single-turn center-tapped inductor, a cross-coupled pair of nMOS transistors, a tail resonant tank of the type proposed in [18], a triode MOS transistor tail source, an integer frequency control element (FCE) bank driven by $c_I[p]$, and a fractional FCE bank driven by $c_F[p]$. The implemented FCEs are of the type presented in [15], and the minimum-size FCE has an equivalent frequency step of $\Delta_{\mathrm{min}} =$ 160 kHz at 6.5 GHz. The DCO's 16-bit input sequence, $d[n]$, is split into integer and fractional parts. The integer part is encoded to drive the integer FCE bank, which comprises eight $32\Delta_{\mathrm{min}}$ FCEs and five pairs of $16\Delta_{\mathrm{min}}$, $8\Delta_{\mathrm{min}}$, $4\Delta_{\mathrm{min}}$, $2\Delta_{\mathrm{min}}$ and Δ_{min} FCEs. The fractional part is up-sampled and re-quantized by a second-order $\Delta\Sigma$ modulator that generates a 5-level output sequence. This output sequence is scrambled by a dynamic element matching (DEM) encoder,

the outputs of which drive four Δ_{min} FCEs within the fractional FCE bank. The PLL controls the DCO over a range of 41 MHz with a minimum step size of 625 Hz.

The DCO also contains a binary-weighted capacitor array controlled via a serial peripheral interface (SPI), which is in parallel with the integer and fractional FCE banks. The capacitor array has 7 bits of tuning over a frequency range of 5.6–6.6 GHz.

IV. MEASURMENT RESULTS

The prototype IC contains the PLL in Fig. 3 as well as an SPI port and test circuitry to measure internal signals during testing. It was fabricated in the GlobalFoundries 22 nm CMOS 22FDX technology. A die photograph is shown in Fig. 10, and area and power breakdowns are presented in Table I. The IC is packaged in a QFN28 package with ground paddle and was tested with an Ironwood SG-MLF-7003 compression elastomer socket. Except where noted otherwise, all of the measurements presented below were taken with a common set of PLL parameters set via the SPI.

Unfortunately, the DCO tank's quality factor is severely degraded by a layout issue to the point that the DCO as-fabricated does not even oscillate, and the problem was not flagged by simulations prior to fabrication because of a post-layout extraction tool flaw. Removing metal near the DCO's main inductor via FIB surgery made the DCO functional, but even with its maximum current setting and its supply set to 0.9 V, its oscillation amplitude is extremely low. Consequently, the DCO's power consumption is that of a high-performance DCO, yet it achieves relatively poor phase noise performance (e.g., 10 dB worse at a 1 MHz offset than

expected[3]) and its low oscillation amplitude makes it highly sensitive to interference from other circuit blocks. While the PLL's overall measured performance is nevertheless in line with the current state of the art, these issues limited its performance as quantified later in the section. The IC's measured output power is around –34 dBm, so an amplifier module was used to boost the output power to around –2 dBm.

Fig. 11 shows the measured phase noise of the PLL at $f_{\mathrm{PLL}} = 6.5$ GHz with and without the TA enabled for PLL bandwidths of 1 MHz and 4.5 MHz. The integrated random jitter (i.e., the jitter omitting spurious tones), σ_{RJ}, is also reported in Fig. 11, where the integration band extends from 10 kHz to 80 MHz. To estimate the expected noise reduction when the TA is enabled, A_{TA} was calculated indirectly from (7) using measured values of g_n read through the SPI. It was found that g_n converged to about 0.758 and 4.832 with and without the TA enabled, respectively, with which two equations based on (7) were solved to find $A_{\mathrm{TA}} = 6.37$. This suggests that the TA reduces the power of the portions of the PLL's phase noise contributed by both the DMRO's circuit noise and its quantization noise by 16 dB.

In the case of Fig. 11(a), the in-band spot phase noise at a 100 kHz offset frequency decreases from –99 to –107 dBc/Hz when the TA is enabled, whereas in the case of Fig. 11(b), the in-band spot phase noise at a 1 MHz offset frequency decreases from –100 to –112 dBc/Hz when the TA is enabled. In the former case, the PLL's in-band phase noise has comparable contributions from the DMRO, reference signal, and DCO, whereas in the latter case, the in-band phase noise is mostly dominated by the DMRO phase noise. Accordingly, as the TA

[3] The spot phase noises of the DCO after the FIB surgery when tuned to 6.5 GHz are –59, –117 and –148 dBc/Hz at offset frequencies of 10 kHz, 1 MHz and 100 MHz, respectively.

suppresses the DMRO's contribution to the PLL's phase noise, the PLL's in-band spot phase noise reduction is more significant in Fig. 11(b). Nonetheless, as shown in Fig. 11(a), the spot phase noise at a 1 MHz offset frequency decreases from –100 to –112 dBc/Hz when the TA is enabled, which occurs because the PLL's phase noise is dominated by DMRO quantization error around that offset frequency.

Fig. 12 shows the PLL's measured phase noise with αf_{ref} set to 18 MHz, the PLL bandwidth set to 1 MHz, and the TA enabled. In this case, the integrated total jitter (i.e., the jitter including spurious tones), σ_{TJ}, was 151 fs_{rms}. This represents the best-case total jitter because it corresponds to a case where the spurious tones are well outside the PLL bandwidth.

The largest measured fractional spur and σ_{TJ} versus αf_{ref} are shown in Fig. 13(a) and Fig. 13(b), respectively, for a PLL bandwidth of 1 MHz. The fractional frequency offset, α, was swept such that αf_{ref} ranges from 1 kHz to 40 MHz with 20 equally-spaced values per decade on a log scale. The integration band of the jitter extends from 10 kHz to 80 MHz to include all significant spurs. The spur powers were measured with the spectrum analyzer's averaging option disabled, and for each value of α, the instrument was configured to ensure that five negative and positive fractional spur harmonics were always visible. In each case, the largest fractional spur was one of the first three harmonics of αf_{ref}, and was no higher than –49 dBc. The measured worst-case spurious tone powers are in line with those predicted by simulation results that include random mismatches among the TA delay cells.

For some values of $\alpha f_{ref} > 5$ MHz, spurs with power lower than –60 dBc and frequencies that are not multiples of αf_{ref} were measured. The authors have not definitively determined the origin of these spurs, but suspect they are from external interference that is parasitically coupled

into the DCO and their effect is exacerbated by the DCO's abnormally low amplitude. These interference spurs are not reported in Fig. 13(a), although their contribution to σ_{TJ} is taken into account in Fig. 13(b), which is why σ_{TJ} increases somewhat for $\alpha f_{ref} > 5$ MHz.

As shown in Fig. 14, the measured reference spur power is lower than –80 dBc. As mentioned above, the authors believe that the DCO's low oscillation amplitude makes it extremely sensitive to external interference. This theory is supported by the observation that increasing the DCO supply, which increases its oscillation amplitude somewhat, tends to reduce the measured spurs. For example, measurements taken with the DCO supply set to 1.1 V yields a reference spur of –85 dBc. Accordingly, the reported reference spur power in Fig. 14 is a worst-case bound on the reference spur performance of the PLL, as the power of this spur is expected to decrease when the DCO problem mentioned above is fixed in a future version of the PLL.

Fig. 15 shows the measured phase noise of the PLL with and without the gain calibration technique enabled for a PLL bandwidth of 4.5 MHz. The results demonstrate the effect of non-ideal ΔΣ FDC forward path gain, i.e., the effect of g_n not satisfying (7), on the PLL's performance at high bandwidth settings. As indicated in the figure, the spot phase noise at a 20 MHz offset frequency decreases by 32 dB when enabling the gain calibration technique, which causes σ_{TJ} to decrease from 2.7 ps_{rms} to 248 fs_{rms}.

Measurements indicate that enabling the TA PS mode has several effects: 1) it decreases the PLL's power consumption by 1.45 mW, which corresponds to 37% of the TA power consumption when the PS mode is disabled, 2) it increases the best-case σ_{TJ} by 20 fs because the swapping circuitry shown in Fig. 7(b) introduces noise into the reference path, 3) it

decreases the worst-case σ_{TJ} by 30 fs due to the slightly better fractional spur performance, and 4) it increases the reference spur power by 14 dB. The authors believe that the reference spur power increase is related to coupling from the analog domain to the DCO, again because of the DCO's low oscillation amplitude.

Table II summarizes the performance of the PLL with and without the TA PS mode enabled, along with that of the best digital PLLs published to date [7], [19]–[27]. As shown in the table, the PLL achieves one of the best in-band spot phase noises, and its spurious tone performance is comparable to that of other state-of-the-art digital PLLs, even though no dedicated spur mitigation technique is used. In contrast, automatic time-to-digital converter (TDC) gain tracking is used to reduce the fractional spur from –35 dBc to –55 dBc in [22], a TDC calibration technique is used to reduce the fractional spur power from –43 dBc to below –74 dBc in [21], and a phase interpolation nonlinearity calibration technique is used to reduce the fractional spur from –24.58 to –53.1 dBc in [20]. Similarly, digital-to-time converter (DTC) range reduction techniques are used in [19], [24] and [25] to improve fractional spur performance.

The PLL's best-case σ_{TJ} is lower than most of the other PLLs in Table II, but its power consumption is higher than those of the other PLLs. As previously mentioned, the implemented DCO consumes the power of a DCO with much better phase noise. Simulations run by the authors suggest that for a properly designed DCO with similar phase noise to that of the implemented DCO, the power consumption should be around 4 mW instead of 8.75 mW. Alternatively, if the DCO had performed as expected, the PLL's best-case σ_{TJ} would have been 115 fs_{rms} instead of 151 fs_{rms}. Furthermore, as mentioned in Section III, the PNR digital was

overdesigned to be clocked at 1 GHz, which is supported by measurement given that the digital domain power supply can be reduced from 0.8 V to 0.55 V without affecting the PLL's performance. In this case, the power consumption of the PNR digital goes down from 4.76 mW to 2.66 mW. Therefore, the implemented PLL's power consumption is higher than necessary, and it could potentially be lowered by approximately 6.85 mW.

Nonetheless, as shown in Table II, even with the higher-than-necessary digital power consumption and worst-than-expected DCO performance, the PLL achieves a Gao figure of merit (FoM) comparable to or better than prior-art digital PLLs [28]. Had the DCO performed as expected, i.e., with performance comparable to that of the DCO presented in [7], the PLL's best-case FoM would have been –245.1 dB and –245.4 dB with and without the TA PS mode disabled, respectively. Alternatively, had the PLL's power consumption be 6.85 mW lower as explained above, the PLL's best-case FoM would have been –244.3 dB and –243.7 dB with and without the TA PS mode disabled, respectively.

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FIGURES

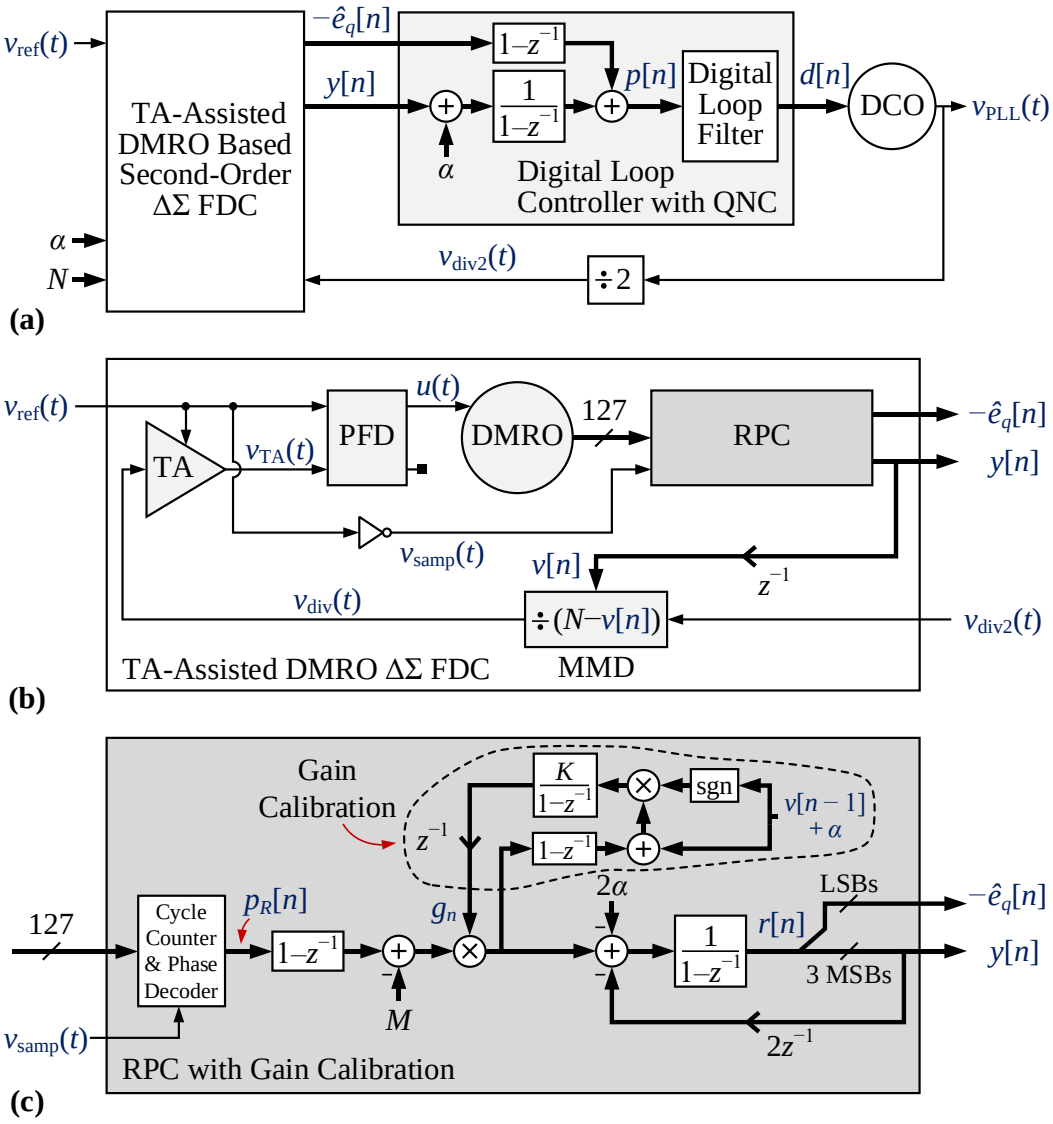

Figure 1: (a) High-level block diagram of the PLL, (b) simplified block diagram of the TA-assisted DMRO ΔΣ FDC, and (c) details of the RPC with gain calibration.

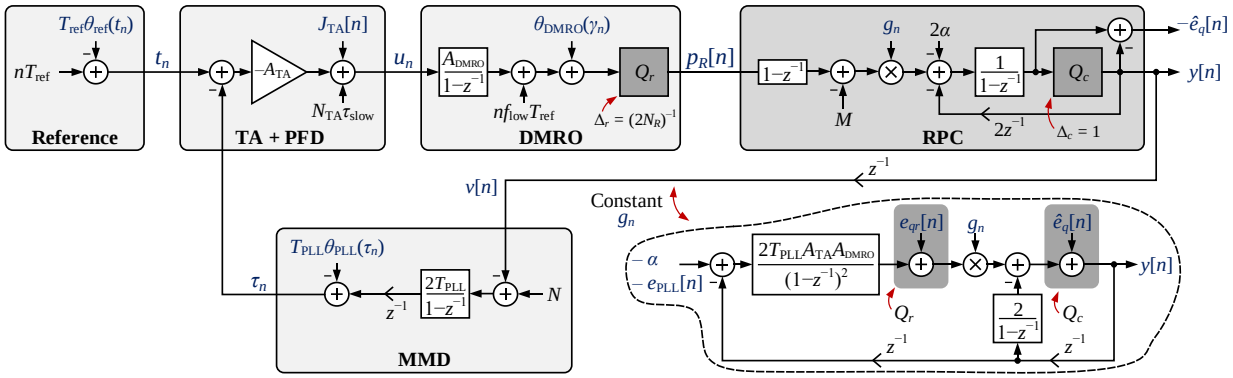

Figure 2: Behavioral model of the TA-assisted DMRO ΔΣ FDC with the gain calibration technique details omitted.

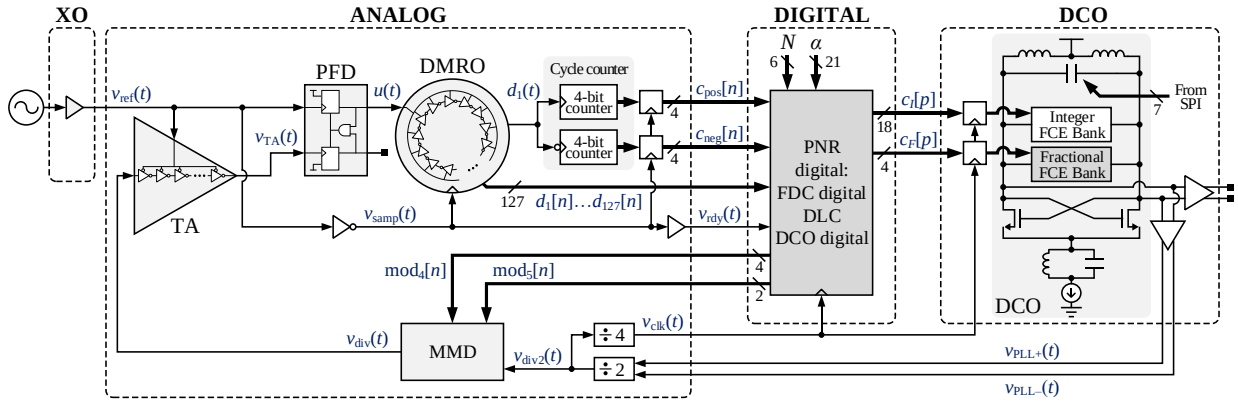

Figure 3: Block diagram of the PLL showing implementation details and the four different power domains in dashed boxes.

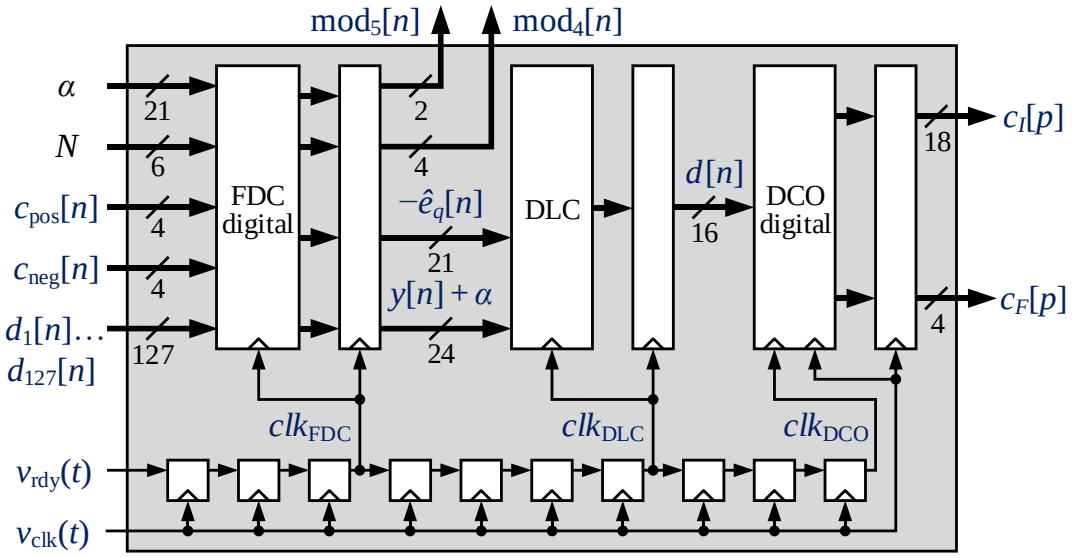

Figure 4: High-level block diagram of the PNR digital block and clocking scheme.

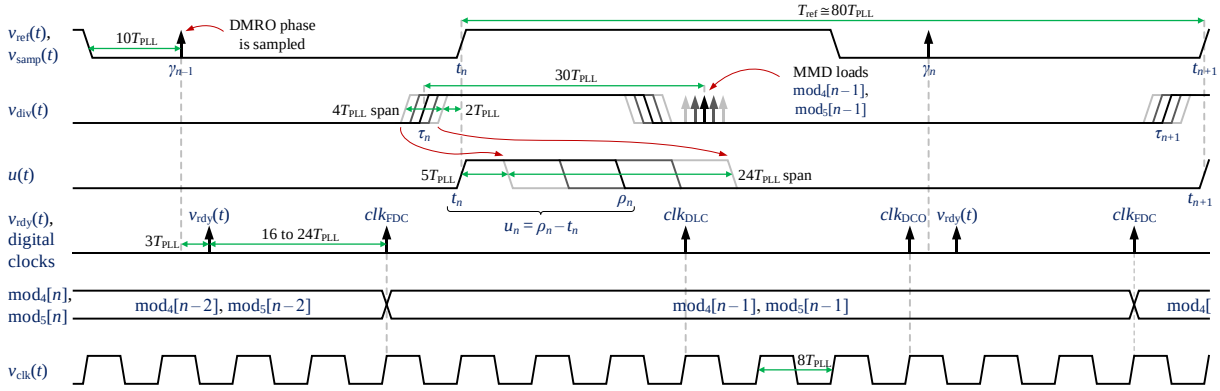

Figure 5: PLL timing diagram.

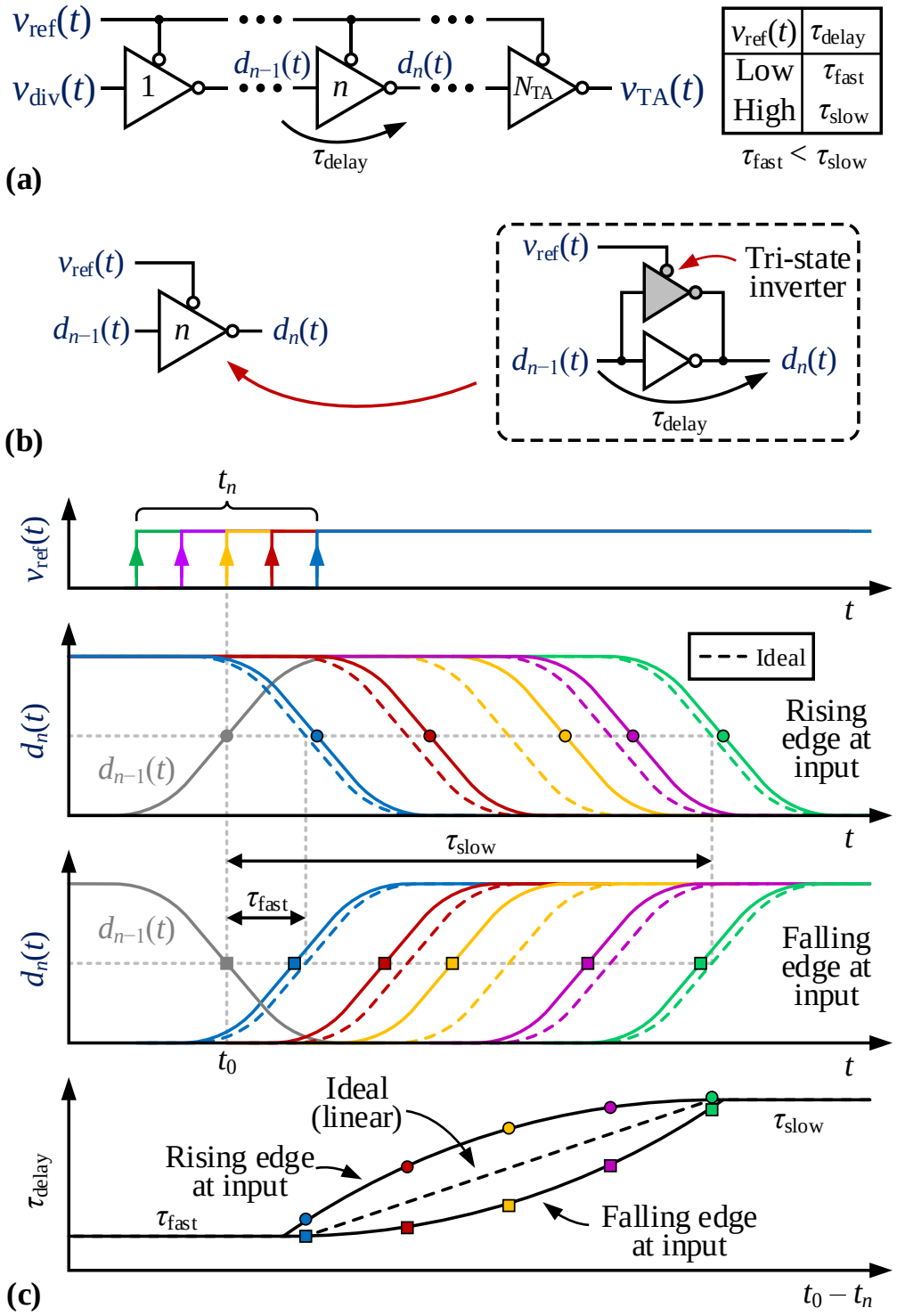

Figure 6: (a) Dual-delay inverter chain based TA concept, (b) details of TA unit delay cell, and (c) illustration of τ_{delay} versus t_n for low-to-high and high-to low input transition (not to scale for illustration purposes).

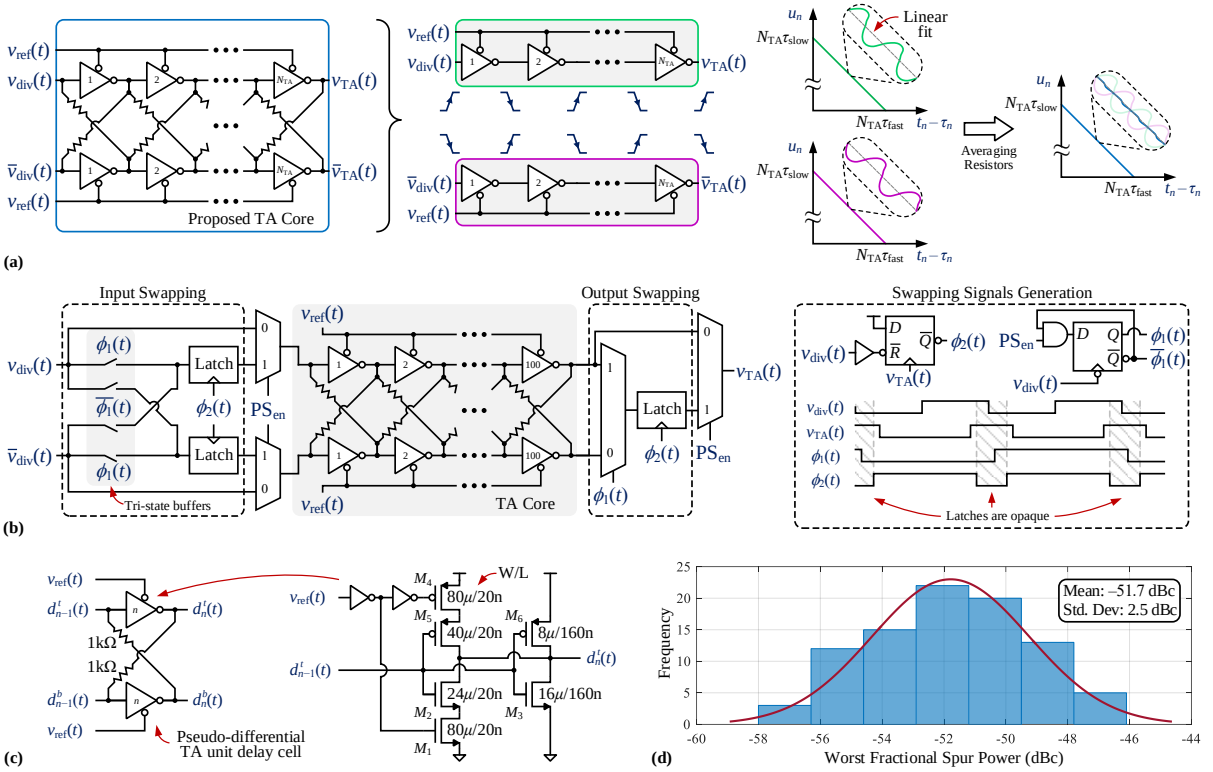

Figure 7: (a) Proposed TA core including the non-linearity mitigation technique, (b) implemented TA architecture with PS mode, (c) TA unit delay cell circuit details, and (d) histogram of the highest fractional spur power that results from the (simulated) TA's unit delay cells' random mismatches.

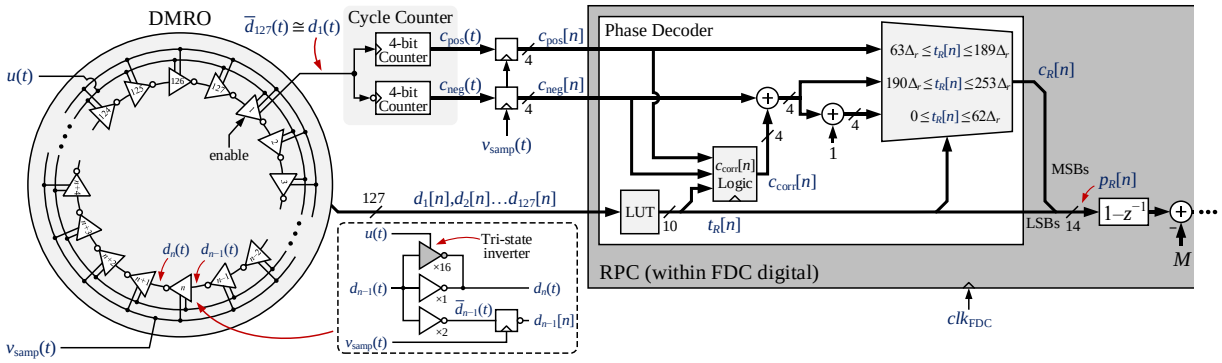

Figure 8: DMRO and delay-free asynchronous phase sampling scheme details.

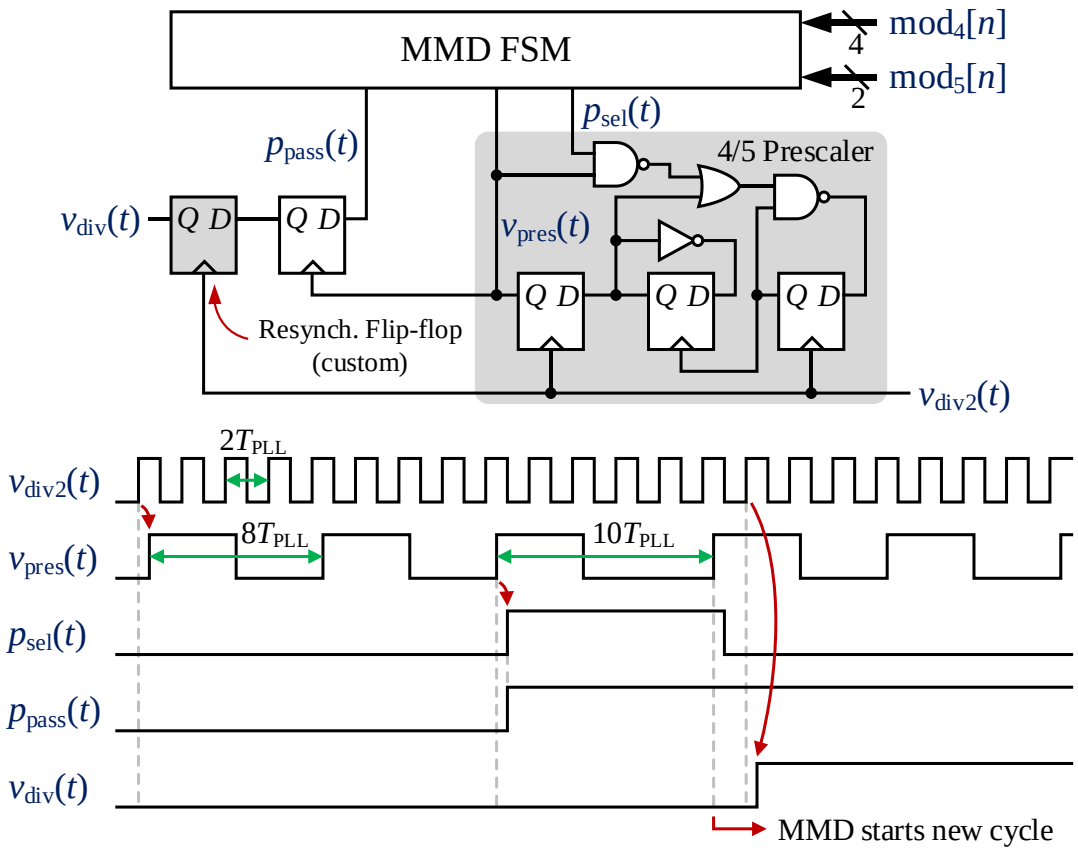

Figure 9: MMD block diagram with example timing diagram.

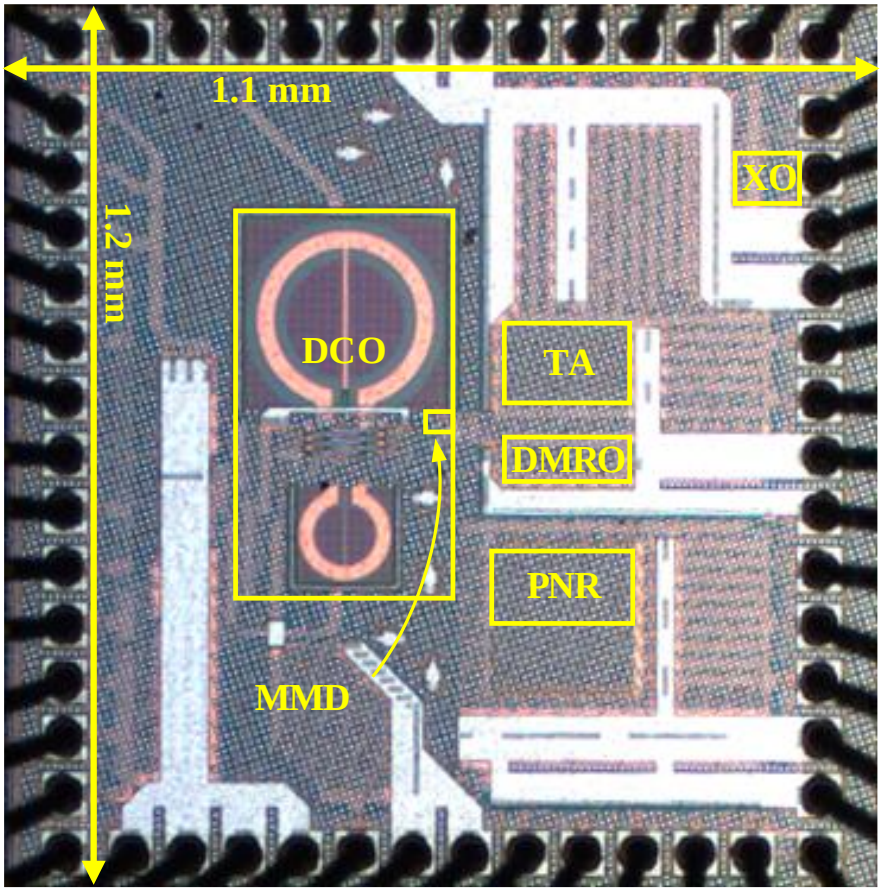

Figure 10: Die photograph.

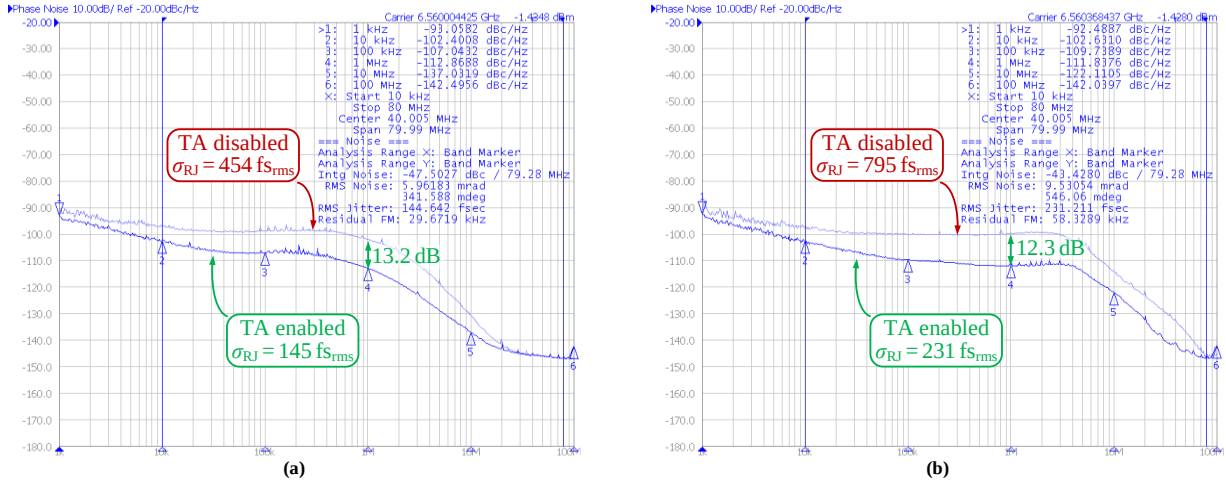

Figure 11: Measured PLL phase noise at f_{PLL} = 6.56 GHz with and without the TA enabled for (a) 1 MHz bandwidth and (b) 4.5 MHz bandwidth.

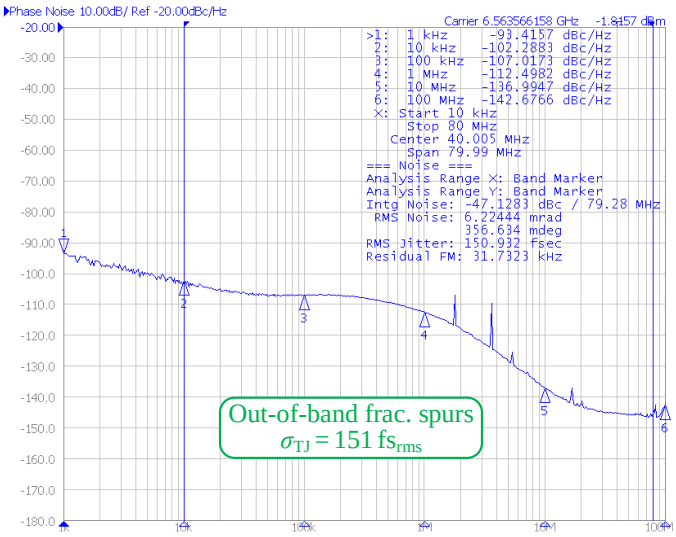

Figure 12: Measured PLL phase noise at f_{PLL} = 6.56 GHz with the TA enabled for out-of-band fractional spurs at 18 MHz offset frequency.

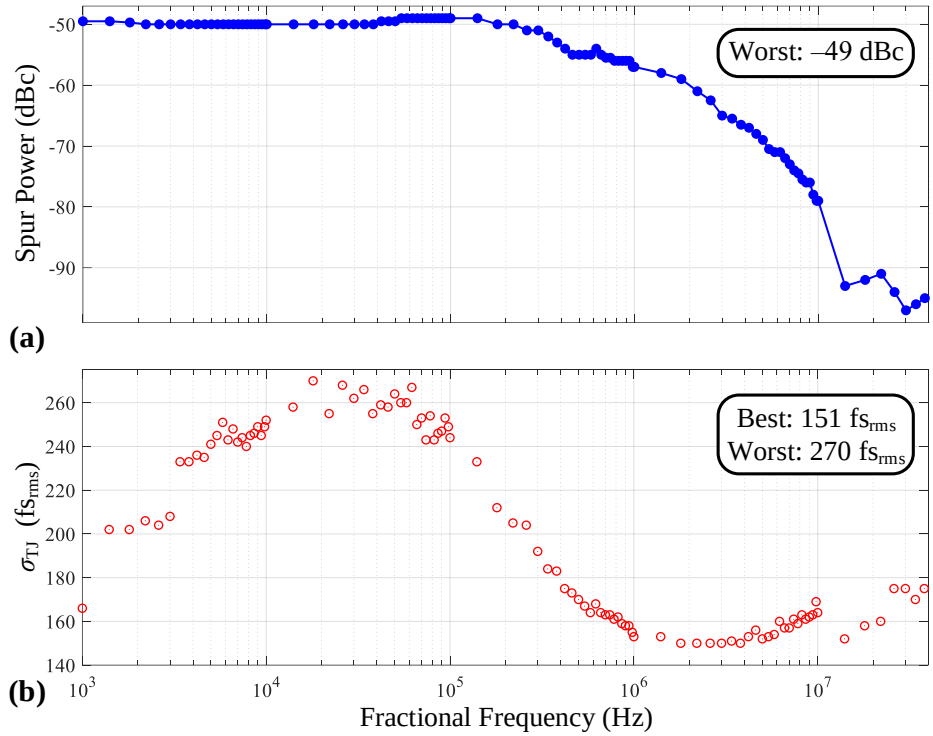

Figure 13: (a) Largest measured fractional spurious tone and (b) total integrated jitter (σ_{TJ}) as a function of the fractional frequency.

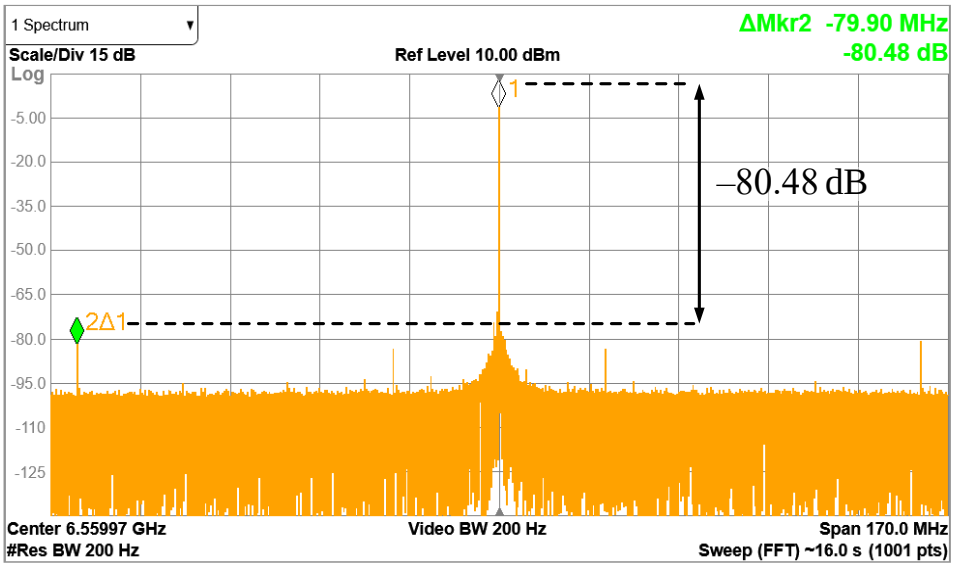

Figure 14: Representative PLL output spectrum.

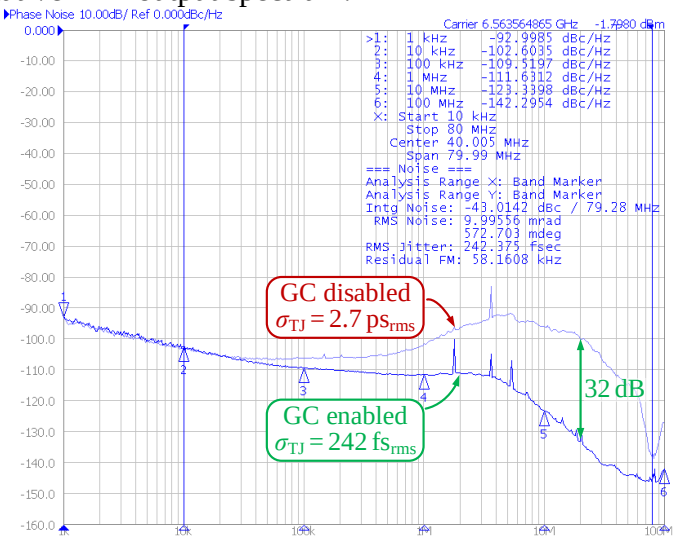

Figure 15: PLL phase noise with and without gain calibration (GC) enabled for a 4.5 MHz bandwidth.

TABLES

Table 1: Area and power breakdown of the IC.

Block	Area (mm^2)	Power (mW)
PNR Digital	0.0242	4.76
Reference Buffers	0.00158	0.165
ΔΣ FDC	0.00713	9.44 / 8 [1]
DCO	0.137	8.75
Total Area	0.6321	23.15 / 21.7 [1]
Active Area [2]	0.1683	

[1] Without and with TA PS mode enabled, respectively.
[2] Without decoupling capacitors.

Table 2: Performance summary and comparison table.

	This work		C. Weltin-Wu JSSC'15 [7]	A. Elkholy JSSC'15 [19]	M. Heo ESSCIRC'17 [20]	C. Yao JSSC'17 [21]	D. Liao JSSC'17 [22]	Z. Xu JSSC'16 [23]	Y. Wu JSSC'17 [24]	L. Bertulessi ISSCC'18 [25]	X. Gao ISSCC'16 [26]	Z. Chen ISSCC'15 [27]
	TA PS dis.	TA PS ena.										
Architecture	ΔΣ FDC+TA		ΔΣ FDC	DTC+TDC +TA	PI+TA	TDC+SA R-ADC	2D Vernier TDC	SAR-ADC TDC	DTC+ TDC	Bang-Bang	Digital Sampling	Digital Sampling
Technology	22 nm		65 nm	65 nm	40 nm	14 nm	55 nm	65 nm	40 nm	65 nm	28 nm	65 nm
Supply (V)	0.8 [1]		1.0	1.0	1.1	-	-	1.0	0.65/0.8/ 1.1	-	1.05/1.5	1
Area (mm^2)	0.63/0.17 [2]		0.35	0.22	0.14	0.257	0.56	0.38	0.5	0.61	0.3	0.23
f_{ref} (MHz)	80		26	50	32	26	80	50	50	52	40	49.15
f_{PLL}(GHz)	6.5		3.5	4.5	3.6	2.7	2.08	3.63	2	3.8	5.83	2.68
BW (kHz)	1000		140	750	1100	500 [4]	1000	1000	800	150	-	700
In-band PN (dBc/Hz) [3]	–107 @100kHz	–106 @100kHz	–87.6 @100kHz	–98.8 @100kHz	–96.9 @300kHz	–106 @100kHz	–97.1 @100kHz	–102.2 @500kHz	–98.7 @100kHz	–102 @100kHz	–104.6 @100kHz	-102.9 @100kHz
Frac. Spur (dBc)	–49	–50	–60	–51.5	–50	–74.5 [4]	–55	–41	–42	–50	–54	–62.3
Ref. Spur (dBc)	–80	–66 [5]	–81	–69	–60	–87.6	-	–39.6	-	-	–78	–60
Tot. Jitter (fs_{rms}) [6]	151/270 10k-80MHz	170/240 10k-80MHz	665 [7] 12k-20MHz	440/490 10k-20MHz	534 [7] 10k-30MHz	137 [7] 10k-10MHz	549/- 10k-10MHz	390/622 [8] 10k-10MHz	330/490 1k-30MHz	183 [7] 1k-30MHz	159 [7] 10k-40MHz	226/240 1k-100MHz
Power (mW)	23.15	21.7	15.6	3.7	5	13.4	9.9	9.7	10.7	5.28	8.2	11.5
FoM_{jitter} [9]	–242.8/ –237.7	–242/ –239	–231.6	–241.5/ –240.5	–238.5	–246	–235.3/ -	–238.3/ –234.3	–239.3/ –235.9	–247.5	–246.8	–242.3/ –241.8

[1] DCO power supply is set to 0.9 V instead of 0.8 V.
[2] With and without decoupling capacitors, respectively.
[3] Phase noise (PN) normalized to 6.5 GHz.
[4] BW estimated from Fig. 15 and spur value taken from Fig. 17 in [21].
[5] Decreases to –70 dBc by raising the DCO supply to 1.1 V.
[6] Best and worst reported total integrated jitters (including spurs), σ_{TJ}.
[7] Not specified if it is random jitter (σ_{RJ}), or best/worst total jitter (σ_{TJ}).
[8] Worst jitter taken from Fig 18(b) in [23].
[9] $FoM_{jitter} = 10\log(jitter^2 \times power/1mW)$ [28].

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CHAPTER 2

DTC LINEARIZATION AND MISMATCH-NOISE CANCELLATION FOR DIGITAL FRACTIONAL-*N* PLLS

Abstract— Digital-to-time converter (DTC) based quantization noise cancellation (QNC) has recently been shown to enable excellent fractional-*N* PLL performance, but it requires a highly-linear DTC. Known DTC linearization strategies include analog-domain techniques which involve performance tradeoffs and digital predistortion techniques which converge slowly relative to typical required PLL settling times. Alternatively, a DTC implemented as a cascade of 1-bit DTC stages can be made highly linear without special techniques, but such DTCs typically introduce excessive error from component mismatches which has so far hindered their use in low-jitter PLLs. This paper presents a background calibration technique that addresses this issue by adaptively canceling error from DTC component mismatches. The technique is entirely digital, is compatible with a large class of digital fractional-*N* PLLs, and has at least an order of magnitude lower convergence time than the above-mentioned predistortion techniques. The paper presents a rigorous theoretical analysis closely supported by simulation results which quantifies the calibration technique's convergence time and noise performance.

I. INTRODUCTION

The signal processing performed within any fractional-*N* phase-locked loop (PLL) for frequency synthesis inevitably involves quantization. The resulting quantization error degrades the PLL's phase noise unless it is actively canceled prior to frequency modulation, a process known as quantization noise cancellation (QNC). An increasingly popular QNC method uses a digital-to-time converter (DTC) to cancel most of the quantization error prior to phase error measurement within the PLL. This prevents the quantization noise from being subjected to the inadvertent but inevitable nonlinearity of the phase error measurement circuitry, thereby avoiding fractional spurs which would otherwise be caused by nonlinearly distorting the quantization error [1]-[5].

However, for such DTC-based QNC to be effective, the DTC must be highly linear. Otherwise, it nonlinearly distorts the quantization error directly, so it becomes a cause of fractional spurs in its own right. Several analog and digital techniques have been proposed to linearize DTC circuits to address this issue. The published analog techniques generally increase power consumption or circuit area considerably [6]-[10]. The published digital techniques perform predistortion via look-up tables (LUTs) to mitigate DTC nonlinearity, but the data with which the LUTs are populated must be measured in background via correlation algorithms which take considerably longer to converge than typical target PLL settling times [11]-[13]. As examples, the cold-start convergence times of the techniques presented in [11] and [12] are over 30,000 and 600,000 reference cycles, respectively.

Alternatively, a DTC implemented as a cascade of 1-bit DTC stages can be made highly linear without any special linearization techniques provided the stages are sufficiently buffered

so that the state of each stage does not significantly affect the delays through the other stages. However, such DTCs typically introduce far more error from component mismatches than the more commonly used single-stage DTCs, which has so far stymied their application to DTC-based QNC in low-jitter PLLs. While dynamic element matching (DEM) can be applied to cause the DTC error arising from component mismatches, i.e., the DTC *mismatch noise*, to be free of nonlinear distortion and have a highpass spectral shape, the power of the mismatch noise nevertheless tends to be high enough that it significantly degrades the PLL's jitter.

This paper proposes an entirely digital DTC mismatch noise cancellation (MNC) technique that is applicable to a large class of digital fractional-*N* PLLs. The DTC-MNC technique adaptively measures and cancels DTC mismatch noise in background within the PLL prior to the PLL's digital loop filter, thereby making highly-linear DTCs comprised of 1-bit DTC stages practical for low-jitter digital fractional-*N* PLLs (although the technique is also applicable to single-stage DTCs). The DTC-MNC technique's convergence time is an order of magnitude faster than that of the fastest of the published predistortion techniques and results in significantly lower simulated jitter and spurious tones than the corresponding reported simulation and measurement results for the previously published predistortion techniques. The paper presents a rigorous analysis closely supported by simulation results which quantifies the DTC-MNC technique's convergence time, and proves that the DTC-MNC technique has no convergence bias and is unconditionally stable.

II. DTC-BASED QUANTIZATION NOISE CANCELLATION

A. General Form of a Digital PLL with DTC-Based QNC

The general form of a digital fractional-N PLL driven by a reference oscillator of frequency f_{ref} is shown in Fig. 16a [14]-[26]. The PLL is comprised of a phase-error-to-digital converter (PEDC), a lowpass digital loop filter, and a digitally controlled oscillator (DCO). Its objective is to generate a low-noise oscillatory output signal, $v_{PLL}(t)$, with instantaneous frequency $f_{PLL} = (N+\alpha)f_{ref}$, where N is a positive integer and α is a fractional value bounded in magnitude by 1.

In many digital fractional-N PLLs, the PEDC incorporates a multi-modulus divider as shown in Fig. 16b. The multi-modulus divider is controlled such that its nth and $(n+1)$th rising output edges are separated by $N-v[n]$ DCO cycles, where $v[n]$ is an integer-valued digital sequence generated within the PEDC. The rest of the PEDC digitizes the phase difference between $v_{ref}(t)$ and $v_{div}(t)$ to generate $p[n]$, and the PLL's feedback loop controls the DCO such that $p[n]$ stays bounded, thereby ensuring that the divider's average output frequency is f_{ref}. In some PLLs, $v[n]$ is generated by a digital delta-sigma ($\Delta\Sigma$) modulator such that its average value is $-\alpha$, and in other PLLs, $v[n]$ is generated within the PLL's feedback loop such that its average converges to $-\alpha$. In either case, the $N-v[n]$ division in conjunction with the feedback causing the divider's average output frequency to converge to f_{ref} causes the DCO's average output frequency to converge to $(N+\alpha)f_{ref}$.

The reason that $v[n]$ is restricted to integer values is that dividers are only capable of counting integer numbers of DCO cycles. Hence, in all such PLLs, $v[n]$ contains zero-mean

quantization error which ultimately contributes to the PLL's overall phase error unless it is canceled prior to the DCO via QNC.

The quantization process with which the PEDC generates $v[n]$ happens in the digital domain so the quantization error is known to the system. One option is to perform QNC in the digital domain after the PEDC digitizes the phase difference between $v_{ref}(t)$ and $v_{div}(t)$. However, in most PLLs with divider-based PEDCs, quantization error is the dominant component in $v[n]$ and when the quantization error is subjected to the inevitable nonlinearity of the PEDC's phase error measurement and digitization circuitry, fractional spurs are induced which digital-domain QNC is unable to cancel. Therefore, it is desirable to perform QNC prior to phase error measurement and digitization if possible.

In principle, this can be done by inserting a DTC between the divider output and the rest of the PEDC. Ideally, the DTC would introduce a time delay of $T_D + \varepsilon[n]$ to the nth output edge of the divider, where $\varepsilon[n]$ represents the effect of the quantization error on the time of the nth rising output edge of the divider, and T_D is a constant that is large enough to ensure that $T_D + \varepsilon[n] > 0$ for DTC causality. Hence, the time of the nth rising edge of the DTC output is the ideal time of the nth rising edge of the divider output, i.e., the time that would have resulted had $v[n]$ not been quantized, aside from an additional fixed delay of T_D. The rest of the PEDC digitizes the phase difference between $v_{ref}(t)$ and $v_{DTC}(t)$, so the PLL's feedback controls the DCO such that the average value of this difference converges to zero, thereby causing the average DCO frequency to converge to $(N+\alpha)f_{ref}$. The primary difference between this case and that of Fig. 16 is that QNC occurs prior to phase error measurement and digitization, which has the potential to significantly reduce spurious tones.

A commonly used DTC circuit is shown in Fig. 17 [7], [8], [27]. It consists of inverters I_1, I_2, I_3, and I_4, and a bank of capacitors. The ith capacitor's top plate is connected to the output of inverter I_2, and its bottom plate is connected to or disconnected from ground when the ith bit of the input codeword $c[n]$ is high or low, respectively. Hence, $c[n]$ controls the RC time constant at the output of inverter I_2, and, consequently, the delay through the DTC.

Inverter I_2 differs from the other inverters, which are standard two-transistor inverters, in that it contains resistor R in series with the drain of the inverter's pMOS transistor. The pMOS transistor is chosen to be wide enough that its on-resistance is small compared to R. This makes the time constant at the output node of inverter I_2 relatively independent of the transistor's on-resistance when the inverter's output voltage transitions from low-to-high, thereby improving the DTC's linearity, i.e., the linearity of the delay between each rising edge of $v_{div}(t)$ and the corresponding rising edge of $v_{DTC}(t)$ as a function of $c[n]$. Another advantage of this design choice is that the large pMOS transistor size results in a relatively low flicker noise contribution from the transistor. As the PLL's timing information is only carried by the times of the rising edges of the divider and DTC outputs, it is not necessary for the nMOS transistor in inverter I_2 to be large or to include a resistor in series with its drain.

B. Nonideal DTC Behavior

A DTC's resolution specifies the number of different delays that the DTC is able to introduce. For example, if the capacitors in the DTC of Fig. 17 have values of 2^iC for $i = 0, 1, 2, \ldots, b-1$, and the ith bit of $c[n]$ controls the transistor connected to the 2^iC capacitor, then the DTC is said to have b bits of resolution because it can introduce 2^b different delays.

In many applications, the minimum step-size of α is so small that it is not practical to implement a DTC with sufficient resolution to achieve delays of exactly $T_D + \varepsilon[n]$, so it is often necessary to have the DTC input be a quantized version of $\varepsilon[n]$. As described above, the purpose of the DTC is to cancel the effect of the quantization error in $v[n]$ prior to the PEDC's phase error measurement and digitization process, so quantizing $\varepsilon[n]$ prior to the DTC appears, at first glance, to defeat the purpose of the DTC. However, the error from quantizing $\varepsilon[n]$ prior to the DTC usually can be made much smaller than the quantization error in $v[n]$, so the quantization-noise-induced spurious tones it causes are much smaller than the those which would have occurred in the absence of the DTC. Furthermore, the quantization of $\varepsilon[n]$ is done in the digital domain, so the quantization error is available within the PEDC as digital sequence. Hence, if necessary, the small amount of quantization error introduced by the quantization of $\varepsilon[n]$ can be canceled within the rest of the PEDC following the phase error measurement and digitization operation.

Another practical DTC limitation relates to component mismatches. In the DTC example described above, the 2^iC capacitor would typically be implemented as a parallel combination of 2^i unit capacitors of size C for each $i = 1, \ldots, b-1$. Mismatches among the different unit capacitors from fabrication errors and systematic layout asymmetries cause the b capacitors to deviate from their ideal values, which results in DTC nonlinearity.

If necessary, DEM can be applied to at least partially address this problem [28], [29]. Provided the number of DTC capacitors and their nominal values satisfy certain constraints, a digital DEM encoder can be used prior to the DTC to control which capacitors are connected and disconnected within the DTC during each reference period such that the error introduced

by component mismatches is either white or highpass spectrally shaped noise instead of nonlinear distortion [30].

As described above, the DTC ideally introduces a delay to the nth rising edge of $v_{div}(t)$ that well-approximates $T_D + \varepsilon[n]$. However, DTC gain error, which is inevitable in practice because of various types of nonideal circuit behavior, causes this delay to instead approximate $A_{DTC}(T_D + \varepsilon[n])$ where A_{DTC} is a constant that deviates from its ideal value of unity. Fortunately, background calibration techniques that adaptively measure A_{DTC} and compensate for it are well-known [4], [22].

Fig. 18 shows a DTC-enabled version of the PEDC of Fig. 16b in which DTC gain calibration, quantization, and DEM are applied to address the DTC's gain error, resolution limitation, and component mismatches, respectively. The details of the DEM encoder and the DTC gain calibration are not described in detail in this paper because they are well-known, established techniques that are described in detail in the cited references.

The remaining types of nonideal DTC behavior are circuit noise, and nonlinearity from sources other than component mismatches. Usually, for a given DTC topology, circuit noise can only be reduced at the expense of increased power consumption and/or area. Nevertheless, fractional-N PLLs with DTC-based QNC have been demonstrated with excellent phase noise performance and power efficiency, so the circuit noise issue has proven to be manageable [7], [8]. Unfortunately, DTC nonlinearity from sources other than component mismatches remains a significant issue, especially for DTCs with high dynamic range [6].

C. DTC Linearity Versus Component Mismatch Tradeoff

While careful sizing of the pMOS transistor and resistor in Inverter I_2 can reduce the nonlinearity of the type of DTC shown in Fig. 17 as described above, it is often not possible to reduce it sufficiently to prevent it from causing significant spurious tones. Consequently, low-jitter fractional-*N* PLLs with DTC-based QNC typically incorporate DTC linearization techniques as mentioned in the introduction.

Alternatively, the DTC can be implemented as a cascade of 1-bit DTC stages as shown in Fig. 19. Ideally, the *i*th DTC stage introduces a delay of $\delta_i[n] = T_i + c_i[n]\Delta_i$, where T_i is a constant delay, $c_i[n]$ is the *i*th output bit of the DEM encoder preceding the DTC, and Δ_i is a constant which represents the DTC stage's delay *step-size*. For example, each 1-bit DTC stage in Fig. 19 can be implemented by the DTC shown in Fig. 17 except with a single capacitor and nMOS transistor in place of the full DTC capacitor bank. To the extent that the inverters at the input and output of each stage provide sufficient isolation that the *i*th stage's delay, $\delta_i[n]$, does not depend on $c_j[n]$ for any $j \neq i$, each DTC stage introduces one of only two possible delays to its input at any given time so each 1-bit stage is inherently linear (two points always lie on a straight line). However, component mismatches cause the two possible delays from each DTC stage to have static deviations from their ideal values, which, in the absence of DEM, would introduce overall DTC nonlinearity. Fortunately, by scrambling the usage pattern of the DTC stages, the DEM encoder causes error from component mismatches to introduce noise-like error instead of nonlinear distortion [30].

However, unlike the single-stage DTC of Fig. 17 wherein mismatch noise is dominated mainly by unit capacitor mismatches, every component within each stage of the multi-stage

DTC contributes to the DTC's mismatch noise. As mentioned in the introduction, this typically causes the mismatch noise from the multi-stage DTC of Fig. 19 to be so high that its application to QNC in low-jitter PLLs has been problematic to date. The DTC-MNC technique presented in the next section addresses this problem.

III. ADAPTIVE DTC MISMATCH NOISE CANCELLATION

The PEDC of Fig. 18 generates an output sequence which can be written as

$$p[n] = r_{ideal}[n] + r_e[n], \tag{15}$$

where $r_{ideal}[n]$ is what $p[n]$ would have been had the DTC not introduced mismatch noise, and $r_e[n]$ is the component of $p[n]$ resulting from DTC mismatch noise. The purpose of the DTC-MNC technique is to adaptively measure and cancel $r_e[n]$. As explained shortly, this is accomplished by the block labeled DTC-MNC logic in the digital PLL shown in Fig. 20

In general, DEM causes the DTC's mismatch noise, $e_{DTC}[n]$, to have the form

$$e_{DTC}[n] = \sum_{k=1}^{L} B_k S_k[n], \tag{16}$$

where L is a constant that depends on the details of the DEM encoder, each $S_k[n]$ is a white or spectrally shaped pseudo-random sequence that is known because it is generated within the DEM encoder, and each B_k is a constant that is unknown because it depends on the DTC's component mismatches [30], [32].

The PEDCs in high-performance PLLs must be quite linear to avoid inducing large spurious tones, so by far the largest term in $p[n]$ resulting from $e_{DTC}[n]$ is a scaled and delayed

version of $e_{DTC}[n]$. While PEDC nonlinearity causes $p[n]$ to also contain a nonlinearly distorted version of $e_{DTC}[n]$ which the DTC-MNC technique does not completely cancel, the power ratio of the linear to nonlinear terms is typically several tens of dB. Provided this ratio is larger than the desired level of cancellation of $e_{DTC}[n]$, which is usually only about 30 dB, then the nonlinearity of the PEDC can be neglected. Hence, (16) implies that $r_e[n]$ can be approximated as

$$r_e[n] = \sum_{k=1}^{L} b_k s_k[n], \tag{17}$$

where b_k is proportional to B_k, $s_k[n] = S_k[n - Q]$, and Q is a positive integer delay.

A. DTC Mismatch-Noise Cancellation Implementation

The details of the DTC-MNC logic block in Fig. 20 are shown in Fig. 21. The structure consists of L feedback loops, each of which contains the residue estimator block shown in Fig. 21b. The kth residue estimator accumulates $Kr[n]s_k[n]$ and multiplies the result by $s_k[n]$, where K is a constant called the DTC-MNC loop gain. For most types of DEM including those considered in this paper, each $s_k[n]$ sequence is limited to values of −1, 0, and 1, so the multiplications are not hardware-intensive. As proven shortly, the kth feedback loop estimates and cancels the kth term of (17) in background, i.e., during normal operation of the PLL.

Although the DTC-MNC technique is applicable to any type of DEM, the analysis presented in this paper assumes that the DEM encoder has the general form of that presented in [31], [32] and causes the DTC's mismatch noise to have either a white or first-order highpass

shaped power spectral density (PSD). In all such cases, $s_k[n]$ for each k is a known, zero-mean pseudo-random sequence called a *switching sequence*, which takes on values of −1, 0, and 1.

It is necessary in the analysis below to keep track of the values of n for which each switching sequence is non-zero, so the mth non-negative integer n for which $s_k[n] \neq 0$ is denoted as $J_{m,k}$. Therefore, $0 \leq J_{1,k} < J_{2,k} < J_{3,k} < \ldots$, and $s_k[n] = 0$ if $n \neq J_{m,k}$ for any value of m.

The two most common options for the switching sequences in (17) are analyzed in this paper: *white switching sequences* and *first-order highpass shaped switching sequences*. The non-zero values of these sequences are given by

$$s_k[J_{r,k}] = w_k[r], \quad \text{and} \quad s_k[J_{r,k}] = (-1)^{r-1} w_k\left[\left\lfloor \frac{r-1}{2} \right\rfloor\right], \tag{18}$$

respectively, where $r = 1, 2, 3, \ldots$, the sequences $w_k[p]$, for all k and p, are independent zero-mean random variables, each of which is restricted to values of −1 and 1, and $\lfloor x \rfloor$ for any real number x denotes the largest integer less than or equal to x.

The two switching sequence options correspond to the switching sequences generated by mismatch scrambling and first-order highpass mismatch shaping DEM encoders, respectively. For the latter case, (18) implies that each successive pair of non-zero $s_k[n]$ values is either 1,−1, or −1, 1, where the choice between these two possibilities is made randomly with equal probability and independently from all other variables in the system.

B. DTC Mismatch-Noise Cancellation Analysis

The DTC-MNC logic is a special case of the multi-loop least-mean-square (LMS) like noise canceler analyzed in [33] for the case of white switching sequences, but not for the case

of spectrally-shaped switching sequences. Furthermore, the DTC-MNC logic for both types of switching sequences differs in two ways from the noise canceler presented in [33], and these differences enable the significantly different and much more precise analysis presented in this paper. One difference is that the input to the DEM encoder that drives the DTC is not arbitrary; it is the sum of the quantization noise component of $v[n]$ and quantization noise from the Q_f quantizer in Fig. 18, each of which is the result of either dithered digital quantization or digital $\Delta\Sigma$ modulation in typical PLLs. The analysis presented in this paper relies on the properties of such DTC input sequences to accurately quantify the convergence speed of the DTC-MNC technique. The other difference is that the DTC-MNC logic is simpler than the noise canceler presented [33], which allows for much tighter error bounds than were derived in [33].

It follows from Fig. 21 and (17) that

$$a_k[n] = a_k[n-1] + Ku_k[n-1] \tag{19}$$

for each $k = 1, 2, \ldots, L$, where

$$u_k[n] = s_k[n]\left(r_{ideal}[n] + \sum_{l=1}^{L} s_l[n]\left(b_l - a_l[n]\right)\right). \tag{20}$$

The objective of the DTC-MNC logic is to cause $r_c[n] = r_e[n]$ such that $r[n] = r_{ideal}[n]$. Fig. 21 implies that

$$r_c[n] = \sum_{k=1}^{L} s_k[n]a_k[n], \tag{21}$$

with which (17) implies that this objective would be perfectly achieved if each $a_k[n]$ coefficient were equal to b_k. Therefore, the *convergence error* of each accumulator in Fig. 21b is defined as

$$z_k[n] = a_k[n] - b_k \,. \tag{22}$$

Combining (19), (20), and (22) with n replaced by n+1 gives

$$z_k[n+1] = z_k[n] + Ks_k\left[n\right] r_{ideal}[n] - Ks_k\left[n\right] \sum_{l=1}^{L} s_l\left[n\right] z_l[n] \tag{23}$$

for each k = 1, 2, …, L. Therefore, $z_k[n]$ for each k = 1, 2, …, L is specified for all $n \geq 0$ by difference equations (23) with initial conditions

$$z_j[0] = a_j[0] - b_j \text{ for } j = 1,\ 2,\ ...,\ L \,. \tag{24}$$

The system is considered to be "turned on" at time n = 0, so

$$z_j[n] = 0 \text{ for } n < 0 \text{ and } j = 1,\ 2,\ ...,\ L \,. \tag{25}$$

The theorems presented below and discussed subsequently, which are proven in the appendix, apply to switching sequences given by (18) and system equations (23), (24), and (25) . They quantify the convergence rate and noise performance of the DTC-MNC technique provided the switching sequences, which depend on the DEM encoder's input sequence, and $r_{ideal}[m]$ satisfy the theorem hypotheses. Simulation results that closely support the theorems' results are presented in the next subsection.

Theorem 1: For white switching sequences and $n \geq 0$, if neither $s_j[m]$ nor $r_{ideal}[m]$ depend on whether $s_k[n]$ is zero or nonzero for any j, k, and $n > m$, then

$$\mathrm{E}\left\{ z_k[n+1] \middle| s_k[n] \right\} = \begin{cases} \bar{z}_k[n], & \text{if } s_k[n] = 0, \\ \bar{z}_k[n]\left(1-K\right), & \text{if } s_k[n] \neq 0, \end{cases} \tag{26}$$

where $\bar{z}_k[n] = \mathrm{E}\{z_k[n]\}$. If, in addition, $\mathrm{E}\{s_k^2[n]\}$ does not depend on n, and $a_j[0] = 0$ for j = 1, 2, …, L, then

$$\bar{z}_k[n] = -b_k\left(1 - c_k K\right)^n, \tag{27}$$

where $c_k = \mathrm{E}\{s_k^2[m]\}$.

□

Theorem 2: For white switching sequences and $n \geq 0$, if $0 < K < 2c_{min}/(cL)$ neither $s_j[m]$ nor $r_{ideal}[m]$ depend on whether $s_k[n]$ is zero or nonzero for any j, k, and $n > m$, neither $\mathrm{E}\{s_k^2[n]\}$ nor $\mathrm{E}\{r_{ideal}^2[n]\}$ depend on n, and $\mathrm{E}\{s_k^2[n]\} \neq 0$ for all k, then

$$\limsup_{n\to\infty}\left\{\sigma_z{}^2[n]\right\} \leq \frac{Kc\sigma_{r_{ideal}}^2}{2c_{min} - KcL}, \tag{28}$$

where

$$\sigma_z{}^2[n] = \frac{1}{L}\sum_{k=1}^{L}\overline{z_k{}^2}[n], \tag{29}$$

$\overline{z_k{}^2}[n] = \mathrm{E}\{z_k^2[n]\}$, $\sigma_{r_{ideal}}^2 = \mathrm{E}\{r_{ideal}^2[n]\}$, and c_{min} and c are the minimum and average values of $c_k = \mathrm{E}\{s_k^2[n]\}$ over $k = 1, 2, \ldots, L$, respectively.

□

Theorem 3: For first-order highpass shaped switching sequences and $n \geq 0$, if $0 < K < 1/L$, $\mathrm{E}\{s_k^2[n]\}$ does not depend on n, neither $s_j[m]$ nor $r_{ideal}[m]$ depend on whether $s_k[n]$ is nonzero for any j, k, and $n > m$, and $a_j[0] = 0$ for $j = 1, 2, \ldots, L$, then

$$\left|\bar{z}_k[n]\right| \leq \left|b_k\right|\left(1 - c_k K\left(\frac{1 - LK}{1 - K}\right)\right)^n, \tag{30}$$

where $c_k = \mathrm{E}\{s_k^2[m]\}$.

□

Theorem 4: For first-order highpass shaped switching sequences and $n \geq 0$, if $0 < a < 1$, where

$$a = 1 - 2c_{min}K + K^2L\left(c_{max}\frac{2(1-K)L}{1-2K} + c\left(1 + L\frac{6+8KL+2K^2L^2}{1-2K}\right)\right), \quad (31)$$

$K < \min\{1/L, ½\}$, neither $s_j[m]$ nor $r_{ideal}[m]$ depend on whether $s_k[n]$ is zero or nonzero for any j, k, and $n > m$, and neither $E\{s_k^2[n]\}$ nor $E\{r_{ideal}^2[n]\}$ depend on n, and $E\{s_k^2[n]\} \neq 0$ for all k, then

$$\limsup_{n\to\infty}\left\{\sigma_z^2[n]\right\} < \frac{cK^2}{1-a}\left(\frac{2+3KL+3K^2L^2+K^3L^3}{1-KL}\right)\sigma_{r_{ideal}}^2, \quad (32)$$

where $\sigma_z^2[n]$, $\sigma_{r_{ideal}}^2$, c_k, c_{min}, and c are as defined in the statement of Theorem 2, and c_{max} is the maximum value of $c_k = E\{s_k^2[n]\}$ over $k = 1, 2, \ldots, L$.

□

Theorems 1 and 3 quantify the convergence rates of the DTC-MNC technique for white and first-order highpass switching sequences, respectively, in terms of the statistical means of $z_k[n]$, i.e., $\overline{z}_k[n]$, for all $n \geq 0$. Theorem 1 provides an exact expression for $\overline{z}_k[n]$ whereas Theorem 3 provides a tight upper bound on the magnitude of $\overline{z}_k[n]$. The theorems show that the convergence of the DTC-MNC technique is unbiased, which, with (22), implies that the mean values of $a_k[n]$ converge exactly to their ideal values, b_k, for all k. The theorems also show that each convergence rate is exponential with a convergence speed that increases with DTC-MNC loop gain K.

While Theorems 1 and 3 show that the means of $z_k[n]$ converge to their ideal values, they do not by themselves guarantee that the DTC-MNC logic is unconditionally stable, as they do not rule out the possibility that the variances of $z_k[n]$ could conceivably diverge. Theorems

2 and 4 address this issue by bounding the steady state variances of $z_k[n]$ for white and first-order highpass shaped switching sequences, respectively. They state conditions which ensure that the variances of $z_k[n]$ are bounded, thereby ensuring unconditional stability. The bounds they provide are in terms of K, the variance of $r_{ideal}[n]$, and how frequently the switching sequences are non-zero over time. The theorems imply that the maximum variances of $z_k[n]$ decrease with K and with the variance of $r_{ideal}[m]$. Together with Theorems 1 and 3, they quantify the convergence speed versus accuracy tradeoff associated with the choice of DTC-MNC loop gain K.

The theorems also provide insight into the tradeoffs between white and first-order highpass shaped switching sequences. Typically, K is small, e.g., less than 2^{-7}, so Theorems 1 and 3 imply that while the convergence rate is faster for white switching sequences than for first-order highpass shaped switching sequences, the difference is relatively small and decreases with K. However, Theorems 2 and 4 suggest that the variance of the convergence error is higher for first-order highpass shaped switching sequences than for white switching sequences. Nevertheless, first-order highpass shaped switching sequences suppress mismatch noise at low frequencies, so error from imperfect convergence introduced by DTC-MNC with these switching sequences tends to be suppressed at low frequencies. Consequently, the results suggest that white switching sequences become increasingly advantageous as the PLL's bandwidth is increased whereas the opposite is true as the PLL's bandwidth is decreased.

C. DTC Mismatch-Noise Cancellation Simulation Results

This subsection presents simulation results of a digital PLL enabled by the DTC-MNC technique, and compares them to the theoretical results presented above. The simulated PLL is based on that presented in [34] but with the modified PEDC shown in Fig. 22. The combination of the fixed divide-by-two and the multi-modulus divider can be viewed as a single multi-modulus divider that divides by $2(N+\alpha)$, so the PEDC has the general form shown in Fig. 16b. The time amplifier (TA), PFD, cycle counter, phase decoder, and dividers are exactly as described in [34]. The dual-mode ring oscillator (DMRO), which has the same topology as that described in [34], has 31 delay elements and its output frequencies are approximately 3 GHz and 250 MHz when the u output of the PFD is high or low, respectively. Quantizers Q_f and Q_c are each implemented as 2nd-order $\Delta\Sigma$ modulators with LSB dither [35].

Like the original PLL presented in [34], the modified PLL has a reference frequency of f_{ref} = 80 MHz and its output frequency is tunable from 6 GHz to 7 GHz. All the PLL simulation results described in this section correspond to $f_{PLL} \cong$ 6.4 GHz with $\alpha f_{ref} \cong$ 104 kHz which is about a tenth of the PLL's 1 MHz bandwidth.

The DTC has 9 bits of resolution and has the form shown in Fig. 19 with M = 20 1-bit DTC stages. It is driven by a segmented DEM encoder of the type presented in [32] with the option of either white or first-order highpass mismatch shaping, and the relative 1-bit DTC stage weights were chosen based on the tradeoffs presented in [31]. The ith 1-bit DTC stage has a nominal delay step-size of $\Delta_i = K_i\Delta$, where Δ = 1.4 ps is the DTC's minimum delay step-size, $K_1, K_2, \ldots, K_{12}$ equal 1, 1, 2, 2, 4, 4, …, 32, 32, respectively, and $K_{13} = K_{14} = \cdots = K_{20} = 64$. The delay between the DEM encoder and $p[n]$ is 2 reference periods, so the results presented in [32]

imply that $r_e[n]$ is given by (17) with $L = 19$ and $s_k[n] = S_k[n-2]$ where $S_k[n]$ is the DEM encoder's kth switching sequence. The DTC gain calibration technique is as presented in [22].

The authors designed a transistor-level version of the DTC for the Global Foundries 22FDX process, wherein each of the 20 1-bit DTC stages has the form shown in Fig. 17 except with a single capacitor and transistor in place of the DTC capacitor bank. Circuit simulations predict that the DTC's mid-code phase noise floor relative to the 80 MHz reference frequency is −161 dBc/Hz and its power consumption is 1.8 mW, which is in line with state-of-the-art designs [6], [7]. Circuit simulations also predict that the PLL's worst-case fractional spur resulting from imperfect isolation among the 1-bit DTC stages is lower than −70 dBc.

The results presented in [31] ensure that the switching sequences satisfy (18), which is a requirement of the theorems presented above. By definition, $r_{ideal}[m]$ does not depend on $s_k[n]$, and it represents measured PLL phase error so it is reasonable to expect that $\mathrm{E}\{r_{ideal}^2[n]\}$ does not depend on n once the PLL is locked. As quantified in [31], whether or not $s_k[n]$ is nonzero at time n is a complicated function of the DEM encoder's input code value at time n and some or all the values of $s_1[n]$, $s_2[n]$, …, $s_{k-1}[n]$ at time n. The DEM encoder's input sequence consists of quantization noise and accumulated quantization noise from the Q_f and Q_c ΔΣ modulators, respectively, and the LSB dither causes both quantization noise sequences to be asymptotically white and uniformly distributed prior to second-order noise shaping [35]. Consequently, it is reasonable to expect that $s_k[n]$ does not depend on whether future values of $s_j[n]$ are nonzero for any j and k, and that $\mathrm{E}\{s_k^2[n]\}$ is nonzero and does not depend on n. These observations, which are further supported by simulation results performed by the authors, are consistent with the hypotheses of the four theorems presented above.

The authors used Cadence Spectre PNOISE circuit simulations to predict the phase noise of each PLL circuit block and Monte-Carlo simulations to determine component mismatches within the DTC. The results were back-annotated into a behavioral, event-driven C-language PLL simulator (along the lines of those presented in [36]-[37]) which generated all of the simulation results presented below.

Fig. 23 shows simulated PLL phase noise spectra which demonstrate the individual and combined effects of DTC mismatches, DEM, and DTC-MNC relative to the PLL's ideal phase noise spectrum. Without DEM or DTC-MNC (Fig. 23a), the DTC mismatches result in large spurious tones which degrade the PLL's RMS total jitter, σ_{TJ}, (integrated from 10 kHz to 80 MHz) to 550 fs from its ideal value of 90 fs which would have occurred in the absence of DTC mismatches. Enabling DEM without DTC-MNC causes the DTC mismatches to introduce noise rather than spurious tones, but with either white (Fig. 23b) or first-order highpass shaped (Fig. 23c) switching sequences, the noise significantly degrades the PLL's jitter. In both cases, enabling DTC-MNC cancels the noise as expected such that the simulated jitter differs insignificantly from its ideal value of 90 fs.

The results shown in Fig. 23 with DTC-MNC enabled correspond to a DTC-MNC loop gain of $K = 2^{-8}$. The theoretical results presented in Section III-B as well as the simulation results presented in Figures 24 and 25 imply that the corresponding DTC-MNC cold-start settling time — the time from when DTC-MNC technique is first enabled with uninitialized registers to the time at which the PLL's phase noise profile becomes visually indistinguishable from that which would have occurred in the absence of DTC mismatches — is less than 2000

reference periods, i.e., less than 25 μs. As mentioned in the introduction, this is at least an order of magnitude faster than reported for the published DTC predistortion techniques [11], [12].

Fig. 24a shows simulated cold-start trajectories (solid curves) of the 19 $\overline{z}_k[n]$ sequences for DTC-MNC with $K = 2^{-12}$ and white switching sequences along with the corresponding theoretical trajectories (dashed curves) predicted by Theorem 1.

The simulated $\overline{z}_k[n]$ trajectories were obtained by averaging the $z_k[n]$ trajectories from ten separate simulation runs starting from the same initial state. As indicated in the figure, the simulated and calculated trajectories are extremely close, and the authors have verified that the simulated and corresponding theoretical trajectories become visually indistinguishable as the number of averages is increased. In principle, the averaging option is necessary because $\overline{z}_k[n]$ in Theorem 1 is the statistical mean of $z_k[n]$. Nevertheless, as shown in Fig. 24b, even without averaging, i.e., for only one simulation run, the simulated trajectories of $z_k[n]$ are very close to the trajectories of $\overline{z}_k[n]$ predicted by Theorem 1. Other values of K yield results similar to those shown in Fig. 24 aside from convergence-rate and noise variances differences.

Fig. 25 shows the simulated cold-start trajectories of $\sigma_z^2[n]$ for DTC-MNC with white switching sequences and various loop gains relative to the steady-state bounds predicted by Theorem 2. As expected, the simulated trajectories remain below the bounds predicted by Theorem 2 after the initial settling transient. As can be seen in the figure, the bounds become tighter as K is decreased.

Fig. 26 shows results that correspond to those shown in Figures 24a, but for the case of first-order highpass shaped switching sequences. Given that Theorem 3 bounds the magnitude of $\overline{z}_k[n]$, Fig. 26 shows trajectories of the magnitudes of $\overline{z}_k[n]$, but otherwise the results

including the convergence rates are very similar those shown in Fig. 24. Furthermore, as can be seen from Fig. 26, the bound provided by Theorem 3 is extremely tight.

Fig. 27 shows results that correspond to those shown in Fig 25, but for the case of first-order highpass shaped sequences. As with the Fig. 25 results, Fig. 27 shows results for three values of DTC-MNC loop gain, K. The hypothesis of Theorem 4 for the parameters of this particular design example restricts K to be less than or equal to about 2^{-11}, so even though the simulation results suggest that $\sigma_z^2[n]$ has a steady-state bound and Theorem 3 ensures that $\overline{z}_k[n]$ converges to zero for all three cases, Theorem 4 only provides a bound for one of the three K values.

IV. CONCLUSION

An entirely digital background calibration technique has been presented that adaptively measures and cancels error resulting from DTC component mismatches that would otherwise degrade the phase noise of digital PLLs with DTC-based quantization noise cancellation. Aside from virtually eliminating DTC component mismatches as a source of phase noise in general, the technique indirectly addresses the well-known DTC nonlinearity problem because it facilitates the use of inherently-linear DTCs comprised of cascades of 1-bit DTC stages. Such DTCs tend to introduce excessive error from component mismatches, which has heretofore hindered their application to low-jitter PLLs. Published digital predistortion techniques provide an alternate means of mitigating DTC nonlinearity, but their convergence rates are at least an order of magnitude slower than that of the presented technique.

A rigorous mathematical analysis has been presented that precisely quantifies the calibration technique's settling performance and provides conditions under which it is unconditionally stable. Closed-loop PLL simulations are notoriously time-consuming, so it is generally not practical to perform simulations over all possible PLL operating conditions. Hence, the results of the analysis are essential to ensure that the calibration technique is robust and works properly over all possible PLL operating conditions.

V. APPENDIX: PROOFS OF THEOREMS 1-4

Proof of Theorem 1: Replacing n with $n - 1$ in (23) gives

$$\begin{aligned} z_k[n] = z_k[n-1] + Ks_k[n-1]r_{ideal}[n-1] \\ -Ks_k[n-1]\sum_{l=1}^{L} s_l[n-1]z_l[n-1] \end{aligned} \tag{33}$$

for all n. Recursively substituting (33) into itself shows that $z_k[n]$ is a function, $f_{k,n}$, of only the variables $r_{ideal}[m]$ and $s_j[m]$ for $j = 1, 2, \ldots, L$ and $m \leq n-1$, i.e.,

$$z_k[n] = f_{k,n}\left(r_{ideal}[m],\ s_j[m];\ j = 1,\ 2,\ ...,\ L,\ m \leq n-1\right). \tag{34}$$

Given that $s_k[m]$ for all m is restricted to values of -1, 0, and 1, it follows that $s_k^2[m] = 1$ when $s_k[m] \neq 0$. Hence, (23) can be written as

$$\begin{aligned} z_k[n+1] = z_k[n]\left(1-K\right) + Ks_k\left[n\right]r_{ideal}[n] \\ -Ks_k\left[n\right]\sum_{\substack{l=1 \\ l\neq k}}^{L} s_l\left[n\right]z_l[n] \end{aligned} \tag{35}$$

whenever $s_k[n] \neq 0$.

The theorem hypothesis states that neither $s_j[m]$ nor $r_{ideal}[m]$ depend on whether $s_k[n]$ is zero or nonzero for any j, k, and $n > m$, so (34) implies that

$$\mathrm{E}\left\{z_k[n]\middle| s_k[n]\neq 0\right\} = \mathrm{E}\left\{z_k[n]\right\} = \bar{z}_k[n], \tag{36}$$

and

$$\mathrm{E}\left\{z_k[n]\middle| s_k[n]= 0\right\} = \mathrm{E}\left\{z_k[n]\right\} = \bar{z}_k[n]. \tag{37}$$

For white switching sequences, when $s_k[n] \neq 0$ it is independent of all other random variables in the system, and (34) implies that $z_k[n]$ is not a function of $s_k[n]$, so (35) and (36) imply

$$\mathrm{E}\left\{z_k[n+1]\middle| s_k[n]\neq 0\right\} = \bar{z}_k[n]\left(1-K\right). \tag{38}$$

It follows from (23) that $z_k[n+1] = z_k[n]$ whenever $s_k[n] = 0$. This with (37) implies

$$\mathrm{E}\left\{z_k[n+1]\middle| s_k[n]= 0\right\} = \bar{z}_k[n]. \tag{39}$$

Combining (38) and (39) yields (26).

By definition, $s_k^2[n]$ is restricted to values of 1 and 0, so the condition that $c_k = \mathrm{E}\{s_k^2[n]\}$ is independent of n for $n \geq 0$ implies that

$$\Pr\left\{s_k[n]\neq 0\right\} = c_k \quad \text{and} \quad \Pr\left\{s_k[n]= 0\right\} = 1-c_k, \tag{40}$$

where $\Pr\{A\}$ denotes the probability of event A. The properties of conditional expectations imply

$$\begin{aligned}\mathrm{E}\left\{z_k[n+1]\right\} = \mathrm{E}\left\{z_k[n+1]\middle| s_k[n]=0\right\}\Pr\left\{s_k[n]=0\right\} \\ + \mathrm{E}\left\{z_k[n+1]\middle| s_k[n]\neq 0\right\}\Pr\left\{s_k[n]\neq 0\right\},\end{aligned} \tag{41}$$

so it follows from (26) and (40), that

$$\bar{z}_k[n+1] = \bar{z}_k[n]\left(1-c_k K\right). \tag{42}$$

If (27) holds for any particular value of n, it follows from substituting (27) into (42) that it must hold for n+1. It follows from (22) that if $a_k[0] = 0$, then $\overline{z}_k[0] = -b_k$ so (27) holds for n = 0. Therefore, (27) must hold for all n = 0, 1, 2, … by mathematical induction.

□

Proof of Theorem 2: The same reasoning that led to (36) and (37) implies

$$\mathrm{E}\left\{z_k{}^2[n]\middle| s_k[n]\neq 0\right\} = \mathrm{E}\left\{z_k{}^2[n]\middle| s_k[n]=0\right\} = \overline{z_k{}^2}[n] \tag{43}$$

for all k and n. Given that that $z_k[n+1] = z_k[n]$ whenever $s_k[n] = 0$, it follows from (43) that

$$\mathrm{E}\left\{z_k{}^2[n+1]\middle| s_k[n]=0\right\} = \overline{z_k{}^2}[n]. \tag{44}$$

This with (40) implies

$$\overline{z_k{}^2}[n+1] = \overline{z_k{}^2}[n]\left(1-c_k\right) + \mathrm{E}\left\{z_k{}^2[n+1]\middle| s_k[n]\neq 0\right\}c_k. \tag{45}$$

Squaring both sides of (23) yields

$$
\begin{aligned}
z_k{}^2[n+1] = z_k{}^2[n] + K^2 s_k{}^2[n] r_{ideal}{}^2[n] + 2K s_k[n] r_{ideal}[n] z_k[n] \\
+ K^2 s_k{}^2[n] \sum_{l=1}^{L} \sum_{j=1}^{L} s_j[n] z_j[n] s_l[n] z_l[n] \\
- 2\left(z_k[n] + K s_k[n] r_{ideal}[n] \right) K s_k[n] \sum_{l=1}^{L} s_l[n] z_l[n].
\end{aligned}
\tag{46}
$$

As indicated by (34), $z_i[n]$ does not depend on $s_j[n]$ for any i, j, and n, and by the definition of white switching sequences, for each integer, i, $s_i[n]$ either equals zero or it has zero mean and is independent of all other random variables in the system. Therefore, taking the expectation of (46) conditioned on $s_k[n] \neq 0$ and applying (43) yields

$$
\begin{aligned}
\mathrm{E}\left\{ z_k{}^2[n+1] \middle| s_k[n] \neq 0 \right\} = \overline{z_k{}^2}[n]\left(1-2K\right) + K^2 \sigma_{r_{ideal}}^2 \\
+ K^2 \sum_{l=1}^{L} \overline{z_l{}^2}[n] \mathrm{E}\left\{ s_l{}^2[n] \middle| s_k[n] \neq 0 \right\}.
\end{aligned}
\tag{47}
$$

Given that $0 \leq s_l{}^2[n] \leq 1$, this implies

$$
\begin{aligned}
\mathrm{E}\left\{ z_k{}^2[n+1] \middle| s_k[n] \neq 0 \right\} \leq \overline{z_k{}^2}[n]\left(1-2K\right) + K^2 \sigma_{r_{ideal}}^2 \\
+ K^2 \sum_{l=1}^{L} \overline{z_l{}^2}[n].
\end{aligned}
\tag{48}
$$

It follows from (29), (40), (45), and (48) that

$$
\overline{z_k{}^2}[n+1] \leq \overline{z_k{}^2}[n]\left(1-2c_k K\right) + c_k K^2 \sigma_{r_{ideal}}^2 + c_k K^2 L \sigma_z{}^2[n]. \tag{49}
$$

This with (29) implies

$$
\sigma_z{}^2[n+1] \leq \sigma_z{}^2[n]\left(1-2Kc_{min} + cLK^2\right) + K^2 c \sigma_{r_{ideal}}^2 . \tag{50}
$$

Hence, $\sigma_z{}^2[n] \leq y[n]$, where $y[n]$ satisfies the constant-coefficient linear difference equation

$$y[n+1] = y[n]\left(1 - 2Kc_{min} + cLK^2\right) + x[n], \tag{51}$$

with

$$x[n] = cK^2\sigma^2_{r_{ideal}} u[n], \tag{52}$$

and $u[n]$ is the unit step function. This implies that $y[n]$ can be viewed as the output of a linear time-invariant (LTI) system with input sequence $x[n]$, where $x[n]$ is a step function.

Solving the z-transform of (51) for the transfer function from $x[n]$ to $y[n]$ yields

$$B(z) = \frac{z^{-1}}{1 - z^{-1}\left(1 - 2Kc_{min} + cLK^2\right)}, \tag{53}$$

where $B(z) = Y(z)/X(z)$, and $Y(z)$ and $X(z)$ are the z-transforms of $y[n]$ and $x[n]$, respectively. The condition $0 < K < 2c_{min}/(cL)$ implies that $|1 - 2Kc_{min} + cLK^2| < 1$, so the LTI system is stable. As $x[n]$ is a step function, the properties of stable LTI systems imply that the limit of $y[n]$ as $n \to \infty$ is the zero-frequency gain of $B(z)$ times the amplitude of $x[n]$, i.e.,

$$\lim_{n\to\infty}\left\{y[n]\right\} = cK^2\sigma^2_{r_{ideal}} B(z^0) = \frac{Kc\sigma^2_{r_{ideal}}}{2c_{min} - KcL}. \tag{54}$$

Given that $\sigma_z^2[n] \le y[n]$ for all n, it follows that the upper bound of $\sigma_z^2[n]$ in the limit as $n \to \infty$, i.e., the limit supremum of $\sigma_z^2[n]$, is bounded by the right side of (54).

□

Lemma 1: For first-order highpass shaped switching sequences, if $l \neq k$, m is an even integer, and $0 < K < 1/L$, then

$$\left|E\{s_k[J_{m,k}]s_l[J_{m,k}]z_l[J_{m,k}]\}\right| \le K\left|E\{z_k[J_{m-1,k}]\}\right|. \tag{55}$$

Proof: Equation (55) holds by inspection if $s_l[J_{m,k}] = 0$. Therefore, it remains to show that (55) holds when $J_{m,k} = J_{p,l}$ for some integer p. By definition, $s_l[J_{p,l}]$ has zero mean and, if p is odd, is independent of all other contemporaneous and prior random variables in the system. It follows that (55) holds if p is odd. It remains to show that (55) holds when $J_{m,k} = J_{p,l}$ and p is even, so for the remainder of the proof suppose that $J_{m,k} = J_{p,l}$ and p is even.

As $z_l[n] = z_l[n-1]$ whenever $s_l[n-1] = 0$, it follows from (33) and the definition of $J_{p,l}$ that

$$\begin{aligned} z_l[J_{p,l}] = (1-K)z_l[J_{p-1,l}] + Ks_l[J_{p-1,l}]r_{ideal}[J_{p-1,l}] \\ -Ks_l[J_{p-1,l}]\sum_{\substack{j=1 \\ j\neq l}}^{L} s_j[J_{p-1,l}]z_j[J_{p-1,l}]. \end{aligned} \tag{56}$$

By definition, $s_k[n]$ has zero mean for all n and k, the nonzero values of $s_k[n]$ are independent of $r_{ideal}[n']$ for all k and n', and $s_l[J_{p,l}]s_l[J_{p-1,l}] = -1$. Hence, (56) implies

$$\begin{aligned} &\mathrm{E}\{s_k[J_{m,k}]s_l[J_{p,l}]z_l[J_{p,l}]\} \\ &\quad = (1-K)\,\mathrm{E}\{s_k[J_{m,k}]s_l[J_{p,l}]z_l[J_{p-1,l}]\} \\ &\quad +K\,\mathrm{E}\{s_k[J_{m,k}]s_k[J_{p-1,l}]z_k[J_{p-1,l}]\} \\ &\quad +K\sum_{\substack{j=1 \\ j\neq l,k}}^{L}\mathrm{E}\{s_k[J_{m,k}]s_j[J_{p-1,l}]z_j[J_{p-1,l}]\}. \end{aligned} \tag{57}$$

Equation (34) implies that $z_i[J_{p-1,l}]$ does not depend on $s_l[J_{p,l}]$ or $s_l[J_{p-1,l}]$ for any i, and, by definition, $s_l[J_{p,l}]$ has zero mean and is independent of all other contemporaneous and prior random variables in the system except $s_l[J_{p-1,l}]$. Hence, the first term on the right side of (57) is

zero. Nearly identical reasoning implies that if $J_{m-1,k} > J_{p-1,l}$ then all the remaining terms on the right side of (57) are also zero, and if $J_{m-1,k} = J_{p-1,l}$ then all the remaining terms except the second term on the right side of (57) are zero. Furthermore, given that $J_{m,k} = J_{p,l}$ and $s_k[J_{p,l}] = -s_k[J_{p-1,l}]$, if $J_{m-1,k} = J_{p-1,l}$ then the second term on the right side of (57) is $-K\mathrm{E}\{z_k[J_{m-1,k}]\}$ if $J_{m-1,k} = J_{p-1,l}$. Hence, the lemma holds when $J_{m-1,k} \geq J_{p-1,l}$.

For the remainder of the proof. suppose that $J_{m-1,k} < J_{p-1,l}$. As explained above, the first term on the right side of (57) is zero. The second term on the right side of (57) is also zero because $J_{m-1,k} \neq J_{p-1,l}$ implies that $s_k[J_{p-1,l}] = 0$. By the same reasoning followed in the first paragraph of the proof, the jth term in the summation on the right side of (57), i.e., is zero unless $J_{p-1,l} = J_{q,j}$ for some even integer q. If $J_{p-1,l} = J_{q,j}$ for some even integer q, then

$$\begin{aligned}\mathrm{E}\{s_k[J_{m,k}]s_j[J_{p-1,l}]z_j[J_{p-1,l}]\} \\ = \mathrm{E}\{s_k[J_{m,k}]s_j[J_{q,j}]z_j[J_{q,j}]\}.\end{aligned} \tag{58}$$

The right side of (58) has the same form as the left side of (55) but with different indices. Therefore, the results of the proof so far imply that the right side of (58) is either zero, $K|\mathrm{E}\{z_k[J_{m-1,k}]\}|$, or

$$K \sum_{\substack{u=1 \\ u \neq j,k}}^{L} \mathrm{E}\{s_k[J_{m,k}]s_u[J_{q-1,j}]z_u[J_{q-1,j}]\}. \tag{59}$$

As $0 < K < 1/L$, it follows that $K(L-2) < 1$. Therefore, (55) holds if the right side of (58) is either 0 or $-K\mathrm{E}\{z_k[J_{m-1,k}]\}$ for each j not equal to l or k. The above reasoning can be applied recursively in each case where the right side of (58) is neither 0 nor $-K\mathrm{E}\{z_k[J_{m-1,k}]\}$ for any j not equal to l or k. At each recursion step, each potentially non-zero term in the sum

corresponding to (59) has the form of the right side of (58), but with a reduced value of $J_{q,j}$. After a finite number of conversion steps, $J_{q,j}$ for each term in the sum becomes small enough that $J_{m-1,k} \geq J_{q-1,j}$, in which case the term is either 0 or $-K\mathrm{E}\{z_k[J_{m-1,k}]\}$.

□

Proof of Theorem 3: By definition, $s_k[n]$ has zero mean for all n and k, and the nonzero values of $s_k[n]$ are independent of $r_{ideal}[n']$ for all k and n'. Consequently, (35) implies

$$\begin{aligned}\mathrm{E}\left\{z_k[n+1]\middle| s_k[n]\neq 0\right\} &= \left(1-K\right)\mathrm{E}\left\{z_k[n]\middle| s_k[n]\neq 0\right\} \\ &\quad -K\sum_{\substack{l=1\\ l\neq k}}^{L}\mathrm{E}\left\{s_k[n]s_l[n]z_l[n]\middle| s_k[n]\neq 0\right\}.\end{aligned} \tag{60}$$

By definition, $s_k[n] \neq 0$ for $n \geq 0$ if and only $n = J_{m,k}$ for some integer m. Hence, (60) can be written as

$$\begin{aligned}E\{z_k[J_{m,k}+1]\} &= \left(1-K\right)E\{z_k[J_{m,k}]\} \\ &\quad -K\sum_{\substack{l=1\\ l\neq k}}^{L}E\{s_k[J_{m,k}]s_l[J_{m,k}]z_l[J_{m,k}]\}.\end{aligned} \tag{61}$$

The right-most equation in (18) implies that for each odd value of m, $s_k[J_{m,k}]$ is independent of all other contemporaneous and prior random variables in the system, so (61) implies

$$\mathrm{E}\left\{z_k[J_{m,k}+1]\right\} = \left(1-K\right)\mathrm{E}\left\{z_k[J_{m,k}]\right\} \tag{62}$$

for odd values of m. For even values of m, (62) does not hold as $z_l[J_{m,k}]$ depends on $s_k[J_{m-1,k}]$ and $s_k[J_{m,k}] = -s_k[J_{m-1,k}]$ if m is even.

Applying Lemma 1 and the triangle inequality to (61) gives

$$\begin{aligned}\left|\mathrm{E}\left\{z_k[J_{m,k}+1]\right\}\right| \le{}& \left|\mathrm{E}\left\{z_k[J_{m,k}]\right\}\right|(1-K) \\ &+(L-1)K^2\left|\mathrm{E}\left\{z_k[J_{m-1,k}]\right\}\right|.\end{aligned} \tag{63}$$

Given that $m-1$ is odd when m is even, it follows from (62) that when m is even $|\mathrm{E}\{z_j[J_{m-1,k}]\}| \le |\mathrm{E}\{z_j[J_{m,k}]\}|/(1-K)$. Therefore, (63) can be written as

$$\left|\mathrm{E}\left\{z_k[J_{m,k}+1]\right\}\right| \le \left|\mathrm{E}\left\{z_k[J_{m,k}]\right\}\right|\left(1-K\left(\frac{1-LK}{1-K}\right)\right). \tag{64}$$

This inequality holds for even values of m, but given that $0 < K < 1/L$ and, by definition, $L \ge 1$, it is a less restrictive inequality than (62), so it must also hold for odd values of m.

As mentioned above, $s_k[n] \ne 0$ for $n \ge 0$ if and only if $n = J_{m,k}$ for some value of $m \ge 1$. Hence, (64) implies

$$\begin{aligned}&\left|\mathrm{E}\left\{z_k[n+1]\middle|s_k[n]\ne 0\right\}\right| \\ &\qquad\le \left|\mathrm{E}\left\{z_k[n]\middle|s_k[n]\ne 0\right\}\right|\left(1-K\left(\frac{1-LK}{1-K}\right)\right).\end{aligned} \tag{65}$$

This with (36), (37), (39) and (40) implies

$$\begin{aligned}&\left|\mathrm{E}\left\{z_k[n+1]\middle|s_k[n]\ne 0\right\}\right|c_k + \left|\mathrm{E}\left\{z_k[n+1]\middle|s_k[n]=0\right\}\right|(1-c_k) \\ &\qquad\le \left|\bar{z}_k[n]\right|\left(1-c_k K\left(\frac{1-LK}{1-K}\right)\right).\end{aligned} \tag{66}$$

Given that c_k and $1-c_k$ are both non-negative, it follows from the definition of $\overline{z}_k[n]$, (41), the triangle inequality, and (66) that

$$\left|\overline{z}_k[n+1]\right| \le \left|\overline{z}_k[n]\right|\left(1-c_k K\left(\frac{1-LK}{1-K}\right)\right). \tag{67}$$

If (30) holds for any particular value of n, it follows from substituting (30) into (67) that it must hold for n+1. It follows from (22) that if $a_k[0] = 0$, then $\overline{z}_k[0] = -b_k$ so (30) holds for n = 0. Therefore, (30) must hold for all n = 0, 1, 2, … by mathematical induction.

□

Lemma 2: For first-order highpass shaped switching sequences, if $K < 1/L$ and $\mathrm{E}\{r_{ideal}^2[n]\}$ does not depend on n, then for any n'

$$\left|\mathrm{E}\left\{r_{ideal}[n']s_i[n]z_i[n]\right\}\right| < \frac{K\sigma_{r_{ideal}}^2}{1-KL}, \tag{68}$$

when $n = J_{m,i}$ and m is a non-negative even integer, and

$$\mathrm{E}\left\{r_{ideal}[n']s_i[n]z_i[n]\right\} = 0, \tag{69}$$

otherwise.

Proof: If $s_i[n] = 0$, then (69) holds by inspection. Otherwise, $n = J_{m,i}$ for some non-negative integer m. If m is odd, then by the definition of the first order highpass shaped switching sequences, $s_i[J_{m,i}]$ is independent of all other contemporaneous and prior random variables in the system and it has zero mean, so (69) holds in case too. Therefore, (69) holds unless $n = J_{m,i}$

and m is a non-negative even integer, so to show that (68) holds, it is sufficient to evaluate $\mathrm{E}\{r_{ideal}[n']s_i[J_{m,i}]z_i[J_{m,i}]\}$ for the case where m is even.

For the remainder of the proof, suppose that m is even. Equation (56) holds with p replaced by m and l replaced by i, and the definition of the first-order highpass shaped switching sequences implies that $s_i[J_{m,i}]s_i[J_{m-1,i}] = -1$ when m is even, so

$$\begin{aligned} s_i[J_{m,i}]z_i[J_{m,i}] = s_i[J_{m,i}]z_i[J_{m-1,i}]\left(1-K\right) - Kr_{ideal}[J_{m-1,i}] \\ +K\sum_{\substack{l=1 \\ l\neq i}}^{L} s_l[J_{m-1,i}]z_l[J_{m-1,i}]. \end{aligned} \tag{70}$$

By definition, $s_i[J_{m,i}]$ has zero mean and is independent of all other contemporaneous and prior random variables in the system except $s_i[J_{m-1,i}]$, and (34) implies that $z_i[J_{m-1,i}]$ does not depend on either $s_i[J_{m,i}]$ or $s_i[J_{m-1,i}]$, so it follows from (70) that

$$\begin{aligned} \mathrm{E}\left\{r_{ideal}[n']s_i[J_{m,i}]z_i[J_{m,i}]\right\} = -K\,\mathrm{E}\left\{r_{ideal}[n']r_{ideal}[J_{m-1,i}]\right\} \\ +K\sum_{\substack{l=1 \\ l\neq i}}^{L}\mathrm{E}\left\{r_{ideal}[n']s_l[J_{m-1,i}]z_l[J_{m-1,i}]\right\}. \end{aligned} \tag{71}$$

The Cauchy-Schwarz inequality for random variables implies that

$$\left|\mathrm{E}\left\{r_{ideal}[p]r_{ideal}[q]\right\}\right| \le \sigma^2_{r_{ideal}} \tag{72}$$

for any integers p and q [38]. This with (71) and the triangle inequality implies that

$$\begin{aligned} &\left|\mathrm{E}\left\{r_{ideal}[n']s_i[J_{m,i}]z_i[J_{m,i}]\right\}\right| \\ &\qquad \le K\sigma^2_{r_{ideal}} + K\sum_{\substack{l=1 \\ l\neq i}}^{L}\left|\mathrm{E}\left\{r_{ideal}[n']s_l[J_{m-1,i}]z_l[J_{m-1,i}]\right\}\right|. \end{aligned} \tag{73}$$

Hence,

$$\left|\mathrm{E}\left\{r_{ideal}[n']s_i[J_{m,i}]z_i[J_{m,i}]\right\}\right| \quad \le K\sigma_{r_{ideal}}^2 + K\left(L-1\right)A_1. \tag{74}$$

where

$$A_1 = \max_{l,l\neq i}\left\{\left|\mathrm{E}\left\{r_{ideal}[n']s_l[J_{m-1,i}]z_l[J_{m-1,i}]\right\}\right|\right\}. \tag{75}$$

As A_1 has the same form as the expectation in the lemma statement, the results of the proof so far apply to it. Substituting (73) with a change of variables into (75) and substituting the result into (74) yields

$$\begin{aligned}\left|\mathrm{E}\left\{r_{ideal}[n']s_i[J_{m,i}]z_i[J_{m,i}]\right\}\right| \le K\sigma_{r_{ideal}}^2 + K^2\left(L-1\right)\sigma_{r_{ideal}}^2 \\ +K^2\left(L-1\right)^2 A_2,\end{aligned} \tag{76}$$

where A_2, like A_1, has the same form as the expectation in the lemma statement. Recursively repeating this process $N-2$ more times yields

$$\begin{aligned}\left|\mathrm{E}\left\{r_{ideal}[n']s_i[J_{m,i}]z_i[J_{m,i}]\right\}\right| \le \sigma_{r_{ideal}}^2 K\sum_{r=0}^{N-1}\left(K\left(L-1\right)\right)^r \\ +K^N\left(L-1\right)^N A_N,\end{aligned} \tag{77}$$

where A_N has the same form as the expectation in the lemma statement. For a sufficiently large value of N, $A_N = |\mathrm{E}\{r_{ideal}[n']s_u[n'']z_u[n'']\}|$ where $n'' < 0$ in which case it follows from (25) that $A_N = 0$. Therefore,

$$\left|\mathrm{E}\left\{r_{ideal}[n']s_i[J_{m,i}]z_i[J_{m,i}]\right\}\right| < \sigma_{r_{ideal}}^2 K\sum_{r=0}^{\infty}\left(K\left(L-1\right)\right)^r, \tag{78}$$

which implies (68) (in which L has been used in place of $L-1$ to simplify the expression at the expense of a slightly looser bound).

□

Lemma 3: For first-order highpass shaped switching sequences, if p is even and $K < ½$ then

$$\mathrm{E}\left\{z_i^2[J_{p-1,i}]\right\} \le \frac{1}{1-2K}\mathrm{E}\left\{z_i^2[J_{p,i}]\right\}. \tag{79}$$

Proof: Equation (56) can be rewritten as

$$z_i[J_{p,i}] = z_i[J_{p-1,i}] + A, \tag{80}$$

where

$$A = Ks_i[J_{p-1,i}]\left(r_{ideal}[J_{p-1,i}] - \sum_{j=1}^{L} s_j[J_{p-1,i}]z_j[J_{p-1,i}]\right). \tag{81}$$

Therefore,

$$z_i^2[J_{p,i}] = z_i^2[J_{p-1,i}] + A^2 + 2Az_i[J_{p-1,i}], \tag{82}$$

so

$$\mathrm{E}\left\{z_i^2[J_{p,i}]\right\} \ge \mathrm{E}\left\{z_i^2[J_{p-1,i}]\right\} + 2\mathrm{E}\left\{Az_i[J_{p-1,i}]\right\}. \tag{83}$$

Given that p is even, $p-1$ is odd, so $s_i[J_{p-1,i}]$, which has zero mean, is independent of all other contemporaneous and prior random variables in the system. Consequently,

$$2\mathrm{E}\left\{Az_i[J_{p-1,i}]\right\} = -2K\,\mathrm{E}\left\{z_i^2[J_{p-1,i}]\right\}. \tag{84}$$

This with (83) and $K < ½$ implies (79).

□

Lemma 4: For first-order highpass shaped switching sequences and any integers $j \neq l$ and $m \geq 1$, if $K < \min\{1/L, ½\}$ and $\mathrm{E}\{r_{ideal}^2[n]\}$ does not depend on n, then

$$\begin{aligned}\left|\mathrm{E}\left\{s_j[J_{m,k}]z_j[J_{m,k}]s_l[J_{m,k}]z_l[J_{m,k}]\right\}\right| &< K^2\left(\frac{1+KL}{1-KL}\right)\sigma_{r_{ideal}}^2 \\ &+\frac{K(1-K)L}{1-2K}\left(\mathrm{E}\left\{z_j{}^2[J_{m,k}]\right\}+\mathrm{E}\left\{z_l{}^2[J_{m,k}]\right\}\right) \\ &+\frac{2K(1+KL)}{1-2K}\sum_{r=1}^{L}\mathrm{E}\left\{z_r{}^2[J_{m,k}]\right\}.\end{aligned} \tag{85}$$

Proof: By definition, $s_i[J_{r,i}]$ for each nonnegative odd value of r has zero mean and is independent of all other contemporaneous and prior random variables in the system, and (34) implies that $z_{l'}[J_{r,i}]$ does not depend on $s_i[J_{r,i}]$ for any i and l'. Therefore,

$$\mathrm{E}\left\{s_j[J_{m,k}]z_j[J_{m,k}]s_l[J_{m,k}]z_l[J_{m,k}]\right\}=0 \tag{86}$$

unless $J_{m,k} = J_{p,j}$ and $J_{m,k} = J_{q,l}$, where p and q are even integers. For the remainder of the proof, suppose $J_{m,k} = J_{p,j}$ and $J_{m,k} = J_{q,l}$, where p and q are even integers, so

$$\begin{aligned}&\mathrm{E}\left\{s_j[J_{m,k}]z_j[J_{m,k}]s_l[J_{m,k}]z_l[J_{m,k}]\right\} \\ &\qquad=\mathrm{E}\left\{s_j[J_{p,j}]z_j[J_{p,j}]s_l[J_{q,l}]z_l[J_{q,l}]\right\},\end{aligned} \tag{87}$$

and (70) with a change of indices implies

$$\begin{aligned}s_j[J_{p,j}]z_j[J_{p,j}] &= s_j[J_{p,j}]z_j[J_{p-1,j}](1-K) \\ &-K\left(r_{ideal}[J_{p-1,j}]-\sum_{\substack{r'=1\\ r'\neq j}}^{L}s_{r'}[J_{p-1,j}]z_{r'}[J_{p-1,j}]\right)\end{aligned} \tag{88}$$

and

$$s_l[J_{q,l}]z_l[J_{q,l}] = s_l[J_{q,l}]z_l[J_{q-1,l}]\left(1-K\right) \\ -K\left(r_{ideal}[J_{q-1,l}] - \sum_{\substack{r=1 \\ r\neq l}}^{L} s_r[J_{q-1,l}]z_r[J_{q-1,l}]\right). \tag{89}$$

The remainder of the proof bounds the expectation of the product of (88) and (89) by bounding the magnitudes of the expectations of the various product terms individually and applying the triangle inequality.

The expectations of several of the product terms contain r_{ideal}. Given that $J_{p,j} = J_{q,l}$ and $J_{q,l} > J_{q-1,l}$, the definition of the switching sequences and (34) imply that $s_j[J_{p,j}]$ is independent of $z_j[J_{p-1,j}]r_{ideal}[J_{q-1,l}]$, so

$$\mathrm{E}\left\{K\left(1-K\right)s_j[J_{p,j}]z_l[J_{p-1,j}]r_{ideal}[J_{q-1,l}]\right\} = 0\,. \tag{90}$$

The same reasoning further implies that

$$\mathrm{E}\left\{K\left(1-K\right)s_l[J_{q,l}]z_l[J_{q-1,l}]r_{ideal}[J_{p-1,j}]\right\} = 0\,. \tag{91}$$

Lemma 2, inequality (72), and the triangle inequality imply that

$$\left|R\right| \le K^2\left(1+\frac{2K\left(L-1\right)}{1-KL}\right)\sigma^2_{r_{ideal}} < K^2\left(\frac{1+KL}{1-KL}\right)\sigma^2_{r_{ideal}}\,, \tag{92}$$

where R is the expectation of the remaining product terms that contain r_{ideal}.

Equation (34) implies that $z_i[n]$ is not a function of $s_k[n']$ for any i, k, and $n' > n-1$. Given that $j \neq l$, if $J_{p-1,j} > J_{q-1,l}$ then $s_j[J_{p,j}]$ is independent of $z_j[J_{p-1,j}]s_l[J_{q,l}]z_l[J_{q-1,l}]$. Otherwise, $s_l[J_{q,l}]$ is independent of $z_l[J_{q-1,l}]s_j[J_{p,j}]z_j[J_{p-1,j}]$. Hence,

$$\mathrm{E}\left\{s_j[J_{p,j}]z_j[J_{p-1,j}]s_l[J_{q,l}]z_l[J_{q-1,l}]\right\} = 0\,. \tag{93}$$

Given that the switching sequences are bounded in magnitude by 1, each of the terms of the product of (88) and (89) that have yet to be considered satisfy

$$\begin{aligned} K(1-K)\left|\mathrm{E}\left\{s_j[J_{p,j}]z_j[J_{p-1,j}]s_r[J_{q-1,l}]z_r[J_{q-1,l}]\right\}\right| \\ \leq K(1-K)\mathrm{E}\left\{\left|z_j[J_{p-1,j}]z_r[J_{q-1,l}]\right|\right\}, \end{aligned} \tag{94}$$

$$\begin{aligned} K(1-K)\left|\mathrm{E}\left\{s_l[J_{q,l}]z_l[J_{q-1,l}]s_{r'}[J_{p-1,j}]z_{r'}[J_{p-1,j}]\right\}\right| \\ \leq K(1-K)\mathrm{E}\left\{\left|z_l[J_{q-1,j}]z_{r'}[J_{p-1,j}]\right|\right\}, \end{aligned} \tag{95}$$

or

$$\begin{aligned} K^2\left|\mathrm{E}\left\{s_{r'}[J_{p-1,j}]z_{r'}[J_{p-1,j}]s_r[J_{q-1,l}]z_r[J_{q-1,l}]\right\}\right| \\ \leq K^2\,\mathrm{E}\left\{\left|z_{r'}[J_{p-1,j}]z_r[J_{q-1,l}]\right|\right\}. \end{aligned} \tag{96}$$

The Cauchy-Schwarz inequality implies that

$$\mathrm{E}\left\{\left|z_u[J_{p-1,j}]z_w[J_{q-1,l}]\right|\right\} \leq \sqrt{\mathrm{E}\left\{z_u{}^2[J_{p-1,j}]\right\}}\sqrt{\mathrm{E}\left\{z_w{}^2[J_{q-1,l}]\right\}}\,, \tag{97}$$

for any u and w. This with Lemma 3 implies

$$\begin{aligned}&\mathrm{E}\left\{\left|z_u[J_{p-1,j}]z_w[J_{q-1,l}]\right|\right\}\\&\qquad\le\frac{1}{1-2K}\sqrt{\mathrm{E}\left\{z_u{}^2[J_{p,j}]\right\}}\sqrt{\mathrm{E}\left\{z_w{}^2[J_{q,l}]\right\}}.\end{aligned}\tag{98}$$

For any non-negative real numbers *a* and *b*,

$$\sqrt{a}\sqrt{b}\le\left(\max\left\{\sqrt{a},\sqrt{b}\right\}\right)^2=\max\left\{a,b\right\}\le a+b\,,\tag{99}$$

so (98) implies

$$\begin{aligned}&\mathrm{E}\left\{\left|z_u[J_{p-1,j}]z_w[J_{q-1,l}]\right|\right\}\\&\qquad\le\frac{1}{1-2K}\left(\mathrm{E}\left\{z_u{}^2[J_{p,j}]\right\}+\mathrm{E}\left\{z_w{}^2[J_{q,l}]\right\}\right).\end{aligned}\tag{100}$$

Given that $J_{m,k} = J_{p,j}$ and $J_{m,k} = J_{q,l}$, it follows from (88)-(96), (100), and the triangle inequality that

$$\begin{aligned}\left|\mathrm{E}\left\{s_j[J_{m,k}]z_j[J_{m,k}]s_l[J_{m,k}]z_l[J_{m,k}]\right\}\right|&<K^2\left(\frac{1+KL}{1-KL}\right)\sigma_{r_{ideal}}^2\\&+\frac{K(1-K)}{1-2K}\sum_{\substack{r=1\\r\ne l}}^{L}\left(\mathrm{E}\left\{z_j{}^2[J_{m,k}]\right\}+\mathrm{E}\left\{z_r{}^2[J_{m,k}]\right\}\right)\\&+\frac{K(1-K)}{1-2K}\sum_{\substack{r'=1\\r\ne j}}^{L}\left(\mathrm{E}\left\{z_l{}^2[J_{m,k}]\right\}+\mathrm{E}\left\{z_{r'}{}^2[J_{m,k}]\right\}\right)\\&+\frac{K^2}{1-2K}\sum_{\substack{r=1\\r\ne l}}^{L}\sum_{\substack{r'=1\\r'\ne j}}^{L}\left(\mathrm{E}\left\{z_{r'}{}^2[J_{m,k}]\right\}+\mathrm{E}\left\{z_r{}^2[J_{m,k}]\right\}\right),\end{aligned}\tag{101}$$

which implies (85) (wherein L has been used in place of $L-1$ for simplicity at the expense of a slightly looser bound).

□

Proof of Theorem 4: Equations (40) hold by the same argument made in the proof of Theorem 1, and (43), (44), (45), and (46) hold by the same arguments made in the proof of Theorem 2.

By definition, $n = J_{m,k}$ for some integer m if and only if $s_k[n] \neq 0$, so

$$\Pr\left\{s_k[n] \neq 0\right\} = d_{n,k} + \Pr\left\{n = J_{m,k} \text{ for some odd } m\right\}, \tag{102}$$

where

$$d_{n,k} = \Pr\left\{n = J_{m,k} \text{ for some even } m\right\}. \tag{103}$$

This and (40) imply that

$$0 \le d_{n,k} \le c_k, \tag{104}$$

and

$$\Pr\left\{n = J_{m,k} \text{ for some odd } m\right\} = c_k - d_{n,k}. \tag{105}$$

Therefore, it follows from (45) that

$$\begin{aligned}
&\overline{z_k^{\,2}}[n+1] \\
&\quad = \mathrm{E}\left\{z_k^{\,2}[n+1] \middle| n = J_{m,k} \text{ for some even } m\right\} d_{n,k} \\
&\quad + \mathrm{E}\left\{z_k^{\,2}[n+1] \middle| n = J_{m,k} \text{ for some odd } m\right\}\left(c_k - d_{n,k}\right) \\
&\quad + \overline{z_k^{\,2}}[n]\left(1 - c_k\right).
\end{aligned} \tag{106}$$

Equation (46) implies that $z_k^2[n+1] = z_k^2[n]$ whenever $s_k[n] = 0$, so it follows from (46) and the definition of $J_{m,k}$ that

$$
\begin{aligned}
&z_k{}^2[J_{m,k}+1] = \\
&\quad z_k{}^2[J_{m,k}] + K^2 r_{ideal}{}^2[J_{m,k}] + 2K r_{ideal}[J_{m,k}] s_k[J_{m,k}] z_k[J_{m,k}] \\
&\quad + K^2 \sum_{l=1}^{L} \sum_{j=1}^{L} s_j[J_{m,k}] z_j[J_{m,k}] s_l[J_{m,k}] z_l[J_{m,k}] \\
&\quad - 2\left(z_k[J_{m,k}] s_k[J_{m,k}] + K r_{ideal}[J_{m,k}] \right) K \sum_{l=1}^{L} s_l[J_{m,k}] z_l[J_{m,k}],
\end{aligned}
\tag{107}
$$

which can be rearranged as

$$
\begin{aligned}
&z_k{}^2[J_{m,k}+1] = z_k{}^2[J_{m,k}](1-2K) \\
&\quad + K^2 r_{ideal}{}^2[J_{m,k}] + 2K(1-K) s_k[J_{m,k}] r_{ideal}[J_{m,k}] z_k[J_{m,k}] \\
&\quad + K^2 \sum_{l=1}^{L} z_l{}^2[J_{m,k}] \\
&\quad + K^2 \sum_{l=1}^{L} \sum_{\substack{j=1 \\ j \neq l}}^{L} s_j[J_{m,k}] z_j[J_{m,k}] s_l[J_{m,k}] z_l[J_{m,k}] \\
&\quad - 2K\left(z_k[J_{m,k}] s_k[J_{m,k}] + K r_{ideal}[J_{m,k}] \right) \sum_{\substack{l=1 \\ l \neq k}}^{L} s_l[J_{m,k}] z_l[J_{m,k}].
\end{aligned}
\tag{108}
$$

The next steps in the proof apply the triangle inequality to bound $\mathrm{E}\{z_k{}^2[J_{m,k}+1]\}$ by summing bounds on the magnitudes of the expectations of the individual terms in (108).

Lemmas 2 and 4 (using L in place of $L-1$ for simplicity at the expense of slightly looser bounds) can be applied to bound magnitudes of the expectations of several of these terms. Lemma 2 implies that

$$
\begin{aligned}
&2K(1-K) \left| \mathrm{E}\left\{ s_k[J_{m,k}] r_{ideal}[J_{m,k}] z_k[J_{m,k}] \right\} \right| \\
&\qquad \leq \begin{cases} \dfrac{2K^2(1-K)}{1-KL} \sigma^2_{r_{ideal}}, & \text{if } m \text{ is even,} \\ 0, & \text{if } m \text{ is odd,} \end{cases}
\end{aligned}
\tag{109}
$$

and

$$2K^2\sum_{\substack{l=1\\l\neq k}}^{L}\left|\mathrm{E}\left\{r_{ideal}[J_{m,k}]s_l[J_{m,k}]z_l[J_{m,k}]\right\}\right|<\frac{2K^3L\sigma_{r_{ideal}}^2}{1-KL}. \tag{110}$$

Lemma 4 with (29) and (43) imply

$$\begin{aligned}&K^2\sum_{l=1}^{L}\sum_{\substack{j=1\\j\neq l}}^{L}\left|\mathrm{E}\left\{s_j[J_{m,k}]z_j[J_{m,k}]s_l[J_{m,k}]z_l[J_{m,k}]\right\}\right|\\&\quad<2K^3L^3\left(\frac{2+KL}{1-2K}\right)\sigma_z{}^2[J_{m,k}]+K^4L^2\left(\frac{1+KL}{1-KL}\right)\sigma_{r_{ideal}}^2,\end{aligned} \tag{111}$$

and

$$\begin{aligned}&2K\sum_{\substack{l=1\\l\neq k}}^{L}\left|\mathrm{E}\left\{z_k[J_{m,k}]s_k[J_{m,k}]s_l[J_{m,k}]z_l[J_{m,k}]\right\}\right|\\&<\frac{2K^2\left(1-K\right)L^2}{1-2K}\overline{z_k{}^2}[J_{m,k}]+2K^2L^2\left(\frac{3+2KL}{1-2K}\right)\sigma_z{}^2[J_{m,k}]\\&+2K^3L\left(\frac{1+KL}{1-KL}\right)\sigma_{r_{ideal}}^2.\end{aligned} \tag{112}$$

It follows from (29), (43), (44), (106), (108), (109), (110), (111), (112), the triangle inequality, and again using L in place of $L-1$ that

$$\begin{aligned}\overline{z_k{}^2}[n+1]<&\,\overline{z_k{}^2}[n]\left(1-2c_kK\right)+c_k\frac{2K^2\left(1-K\right)L^2}{1-2K}\overline{z_k{}^2}[n]\\&+c_kK^2L\left(1+L\frac{6+8KL+2K^2L^2}{1-2K}\right)\sigma_z{}^2[n]\\&+c_kK^2\left(1+KL\frac{4+3KL+K^2L^2}{1-KL}\right)\sigma_{r_{ideal}}^2\\&+d_{n,k}\frac{2K^2\left(1-K\right)}{1-KL}\sigma_{r_{ideal}}^2.\end{aligned} \tag{113}$$

Summing both sides of (113) over k, dividing the result by L, and applying (29) yields

$$\sigma_z{}^2[n+1] < a\sigma_z{}^2[n] + x[n] \tag{114}$$

where a is given by (31),

$$\begin{aligned} x[n] = u[n]K^2 \Bigg[& c\left(1 + KL\,\frac{4+3KL+K^2L^2}{1-KL}\right) \\ & + d_n\,\frac{2(1-K)}{1-KL}\Bigg]\sigma_{r_{ideal}}^2, \end{aligned} \tag{115}$$

$$d_n = \frac{1}{L}\sum_{k=1}^{L} d_{n,k}\,, \tag{116}$$

and $u[n]$ is the unit step function (because the system is "turned on" at time $n = 0$). Hence, $\sigma_z{}^2[n] < y[n]$, where $y[n]$ satisfies the constant coefficient, linear difference equation

$$y[n+1] = ay[n] + x[n]. \tag{117}$$

The definitions of the first-order switching sequences, $J_{m,k}$, and c_k imply

$$\mathbf{p}_{n+1,k} = \mathbf{M}_k\mathbf{p}_{n,k}, \quad \text{where} \quad \mathbf{M}_k = \begin{bmatrix} 1-c_k & c_k \\ c_k & 1-c_k \end{bmatrix}, \tag{118}$$

and

$$\mathbf{p}_{n,k} = \begin{bmatrix} \Pr\{\text{largest } J_{m,k} \le n \text{ has odd } m\} \\ \Pr\{\text{largest } J_{m,k} \le n \text{ has even } m\} \end{bmatrix}. \tag{119}$$

The matrix $\mathbf{M}_k$ is a Markov matrix and $\boldsymbol{\pi} = [\tfrac{1}{2}\ \tfrac{1}{2}]$ is a probability vector that satisfies $\boldsymbol{\pi}\mathbf{M}_k = \boldsymbol{\pi}$, so it follows that all elements of $\mathbf{M}_k{}^n$, and, hence, of $\mathbf{p}_{n,k}$ converge to ½ as $n \to \infty$ [38]. Given that $d_{n,k} = c\Pr\{\text{largest } J_{m,k} \le n \text{ has odd } m\}$, it follows from (116) that

$$\lim_{n\to\infty} d_n = \frac{c}{2} \tag{120}$$

Solving the z-transform of (117) for the transfer function from $x[n]$ to $y[n]$, yields

$$B(z) = \frac{z^{-1}}{1 - az^{-1}}, \tag{121}$$

where $B(z) = Y(z)/X(z)$, and $Y(z)$ and $X(z)$ are the z-transforms of $y[n]$ and $x[n]$, respectively. The properties of stable LTI systems imply that

$$\lim_{n\to\infty} \left\{ y[n] \right\} = B\left(z^0\right) \lim_{n\to\infty} x[n]. \tag{122}$$

The limit supremum of $\sigma_z^2[n]$ as $n \to \infty$ is less than or equal to (122) because $\sigma_z^2[n] < y[n]$, so (32) follows from (31), (115), (120), (121) and (122).

□

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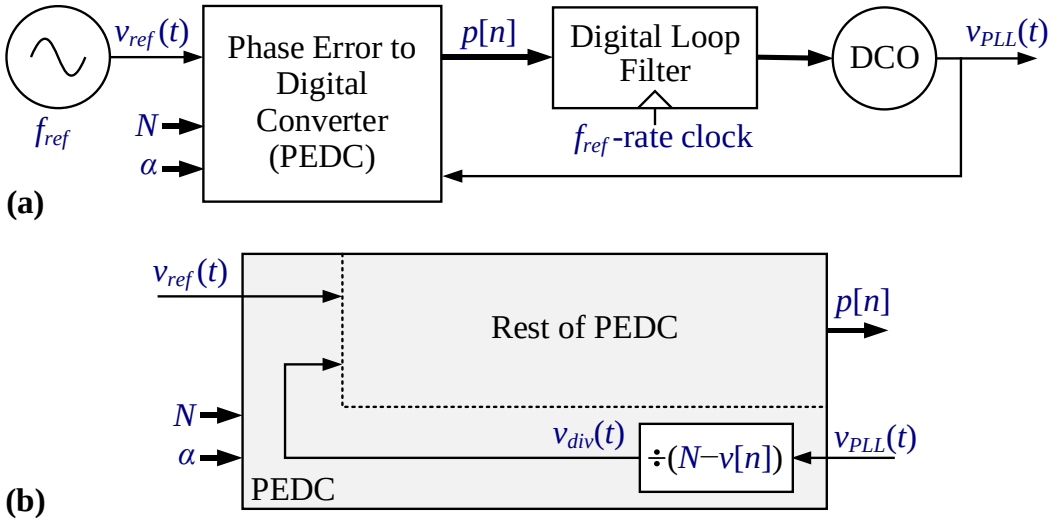

Figure 16: a) General form of a digital fractional-N PLL driven by an f_{ref}-frequency reference oscillator, b) general form of a multi-modulus divider-based PEDC.

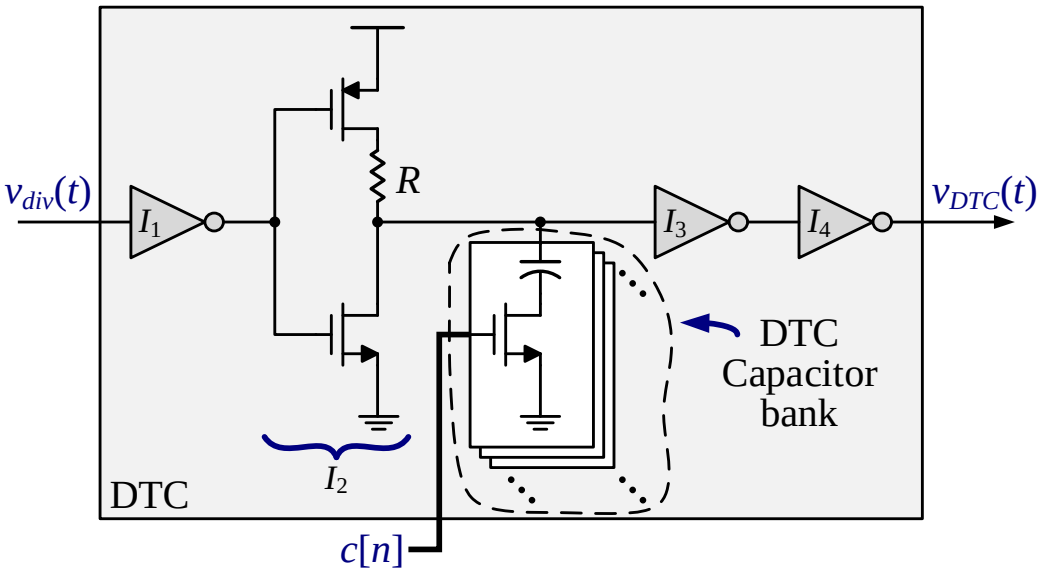

Figure 17: A commonly-used DTC circuit.

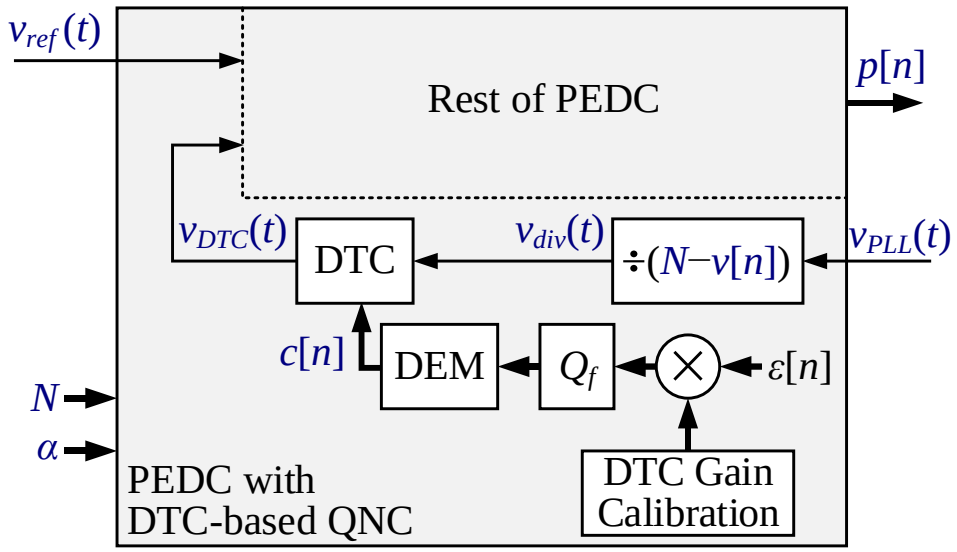

Figure 18: The PEDC of Fig. 1b with a DEM encoder, quantizer Q_f, and DTC gain calibration.

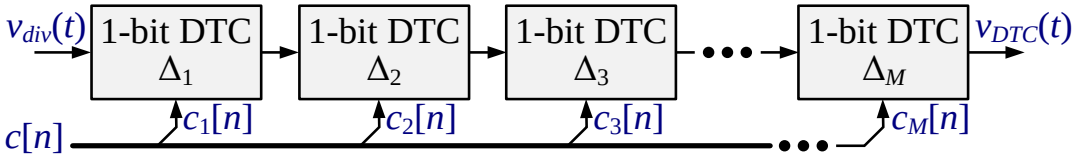

Figure 19: A DTC implemented as a cascade of M 1-bit DTCs.

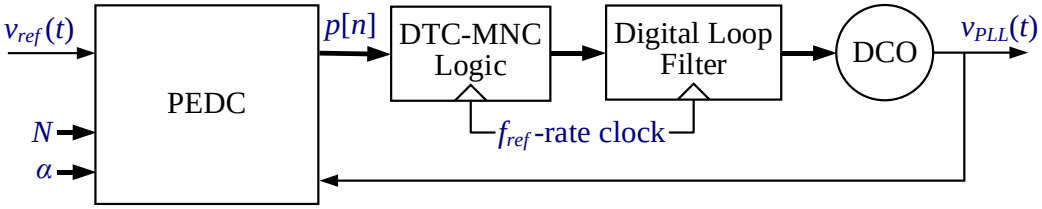

Figure 20: General form of a digital fractional-N PLL with the MNC technique.

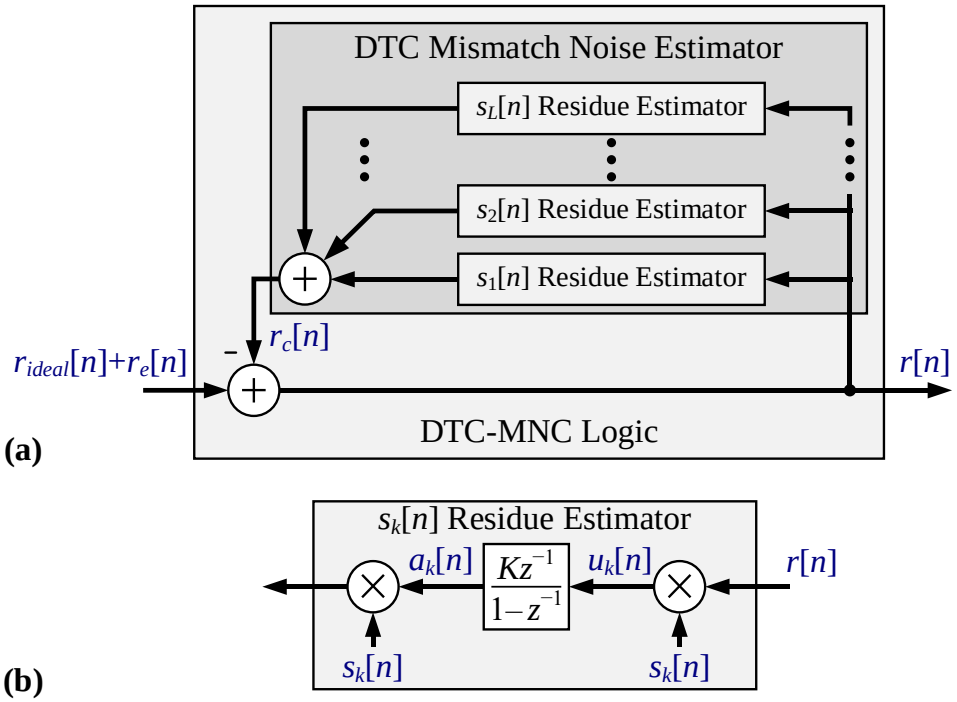

Figure 21: DTC-MNC logic details; a) high-level view, b) details of the *k*th feedback loop's $s_k[n]$ residue amplifier.

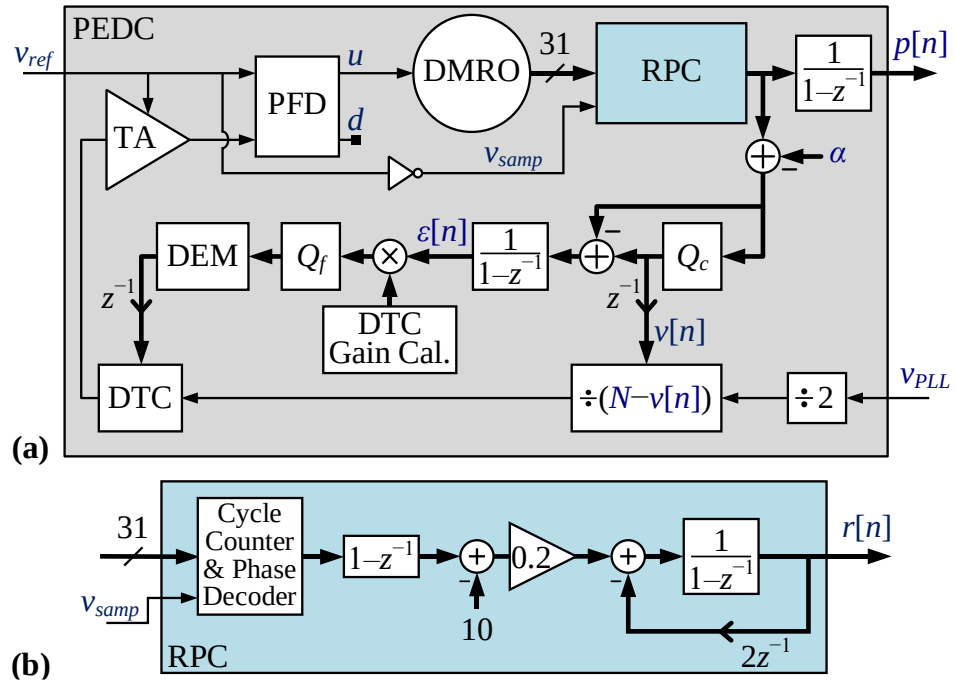

Figure 22: Details of the simulated PLL a) high-level view of the PEDC b) digital ring phase calculator (RPC).

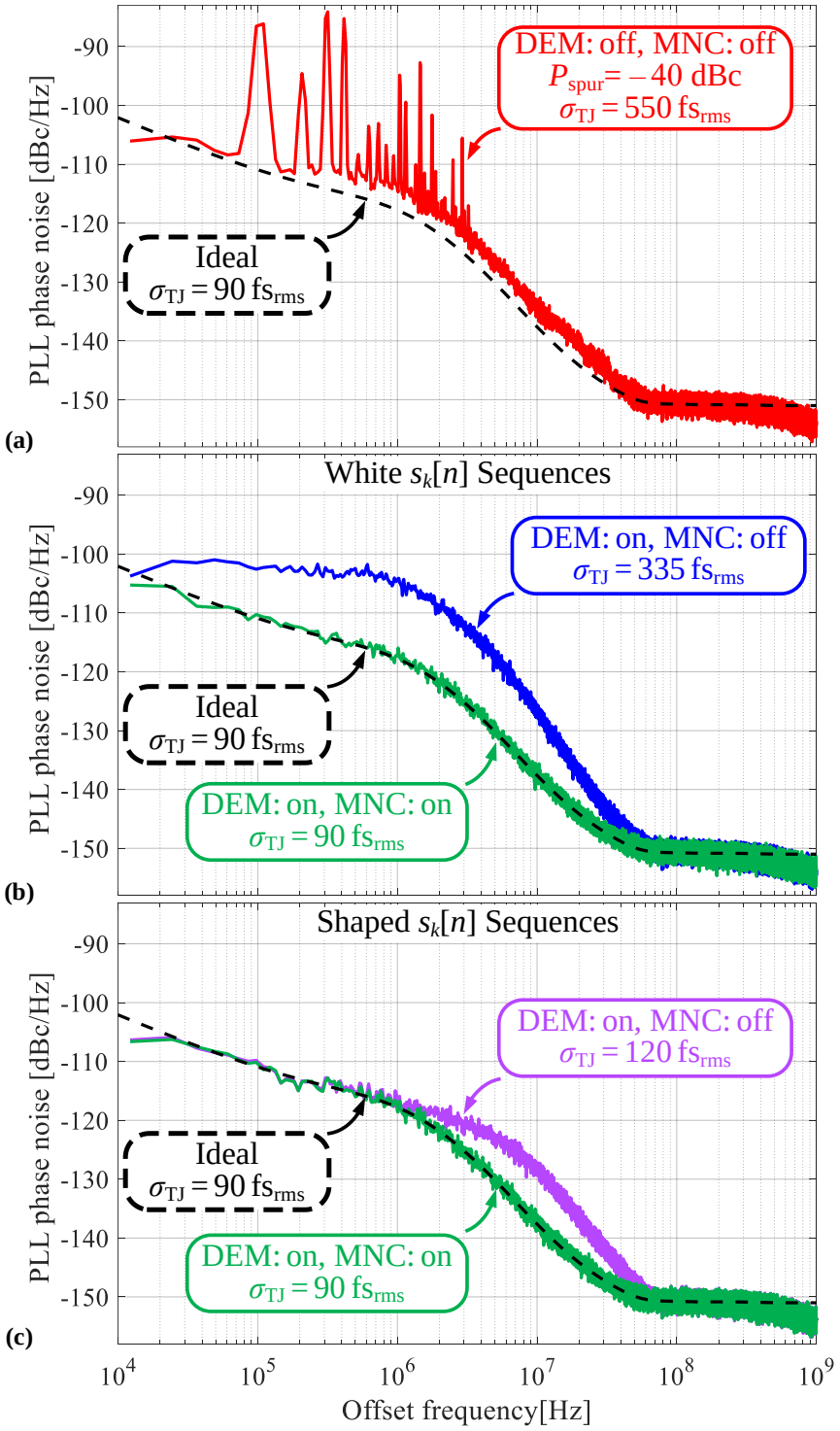

Figure 23: PLL phase noise spectra from simulation (solid curves) and theoretical analysis (dashed curves).

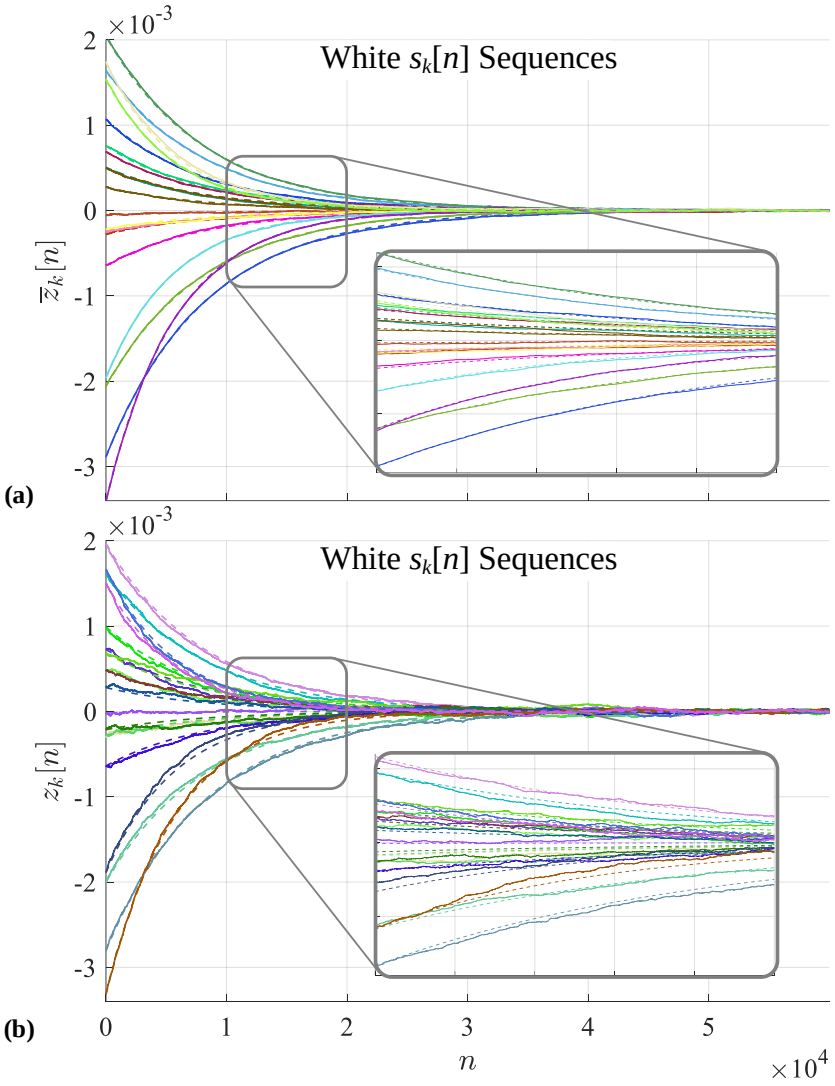

Figure 24: Cold start trajectories of $\overline{z}_k[n]$ for white switching sequences predicted by Theorem 1(dashed curves) with simulated trajectories (solid curves) of a) $\overline{z}_k[n]$ and b) $z_k[n]$.

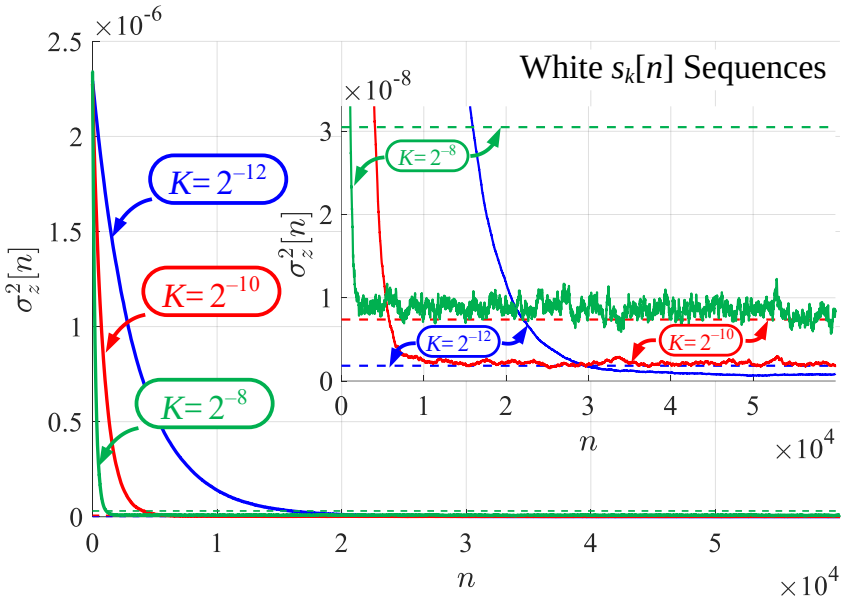

Figure 25: Simulated cold start trajectories (solid curves) of $\sigma_z^2[n]$ for white switching sequences with the bounds predicted by Theorem 2 (dashed curves).

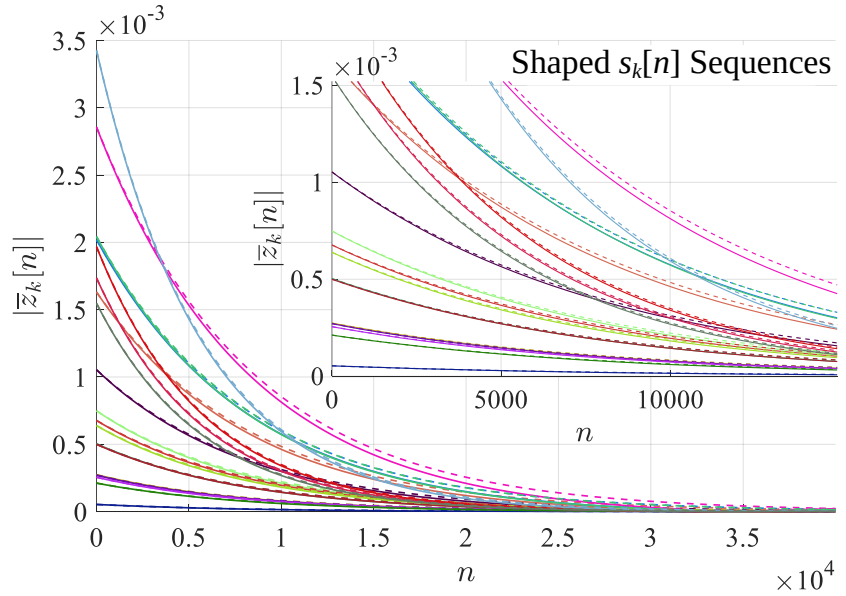

Figure 26: Simulated cold start trajectories (solid curves) of the magnitudes of $\overline{z}_k[n]$ for first-order highpass shaped switching sequences with the bounds predicted by Theorem 3 (dashed curves).

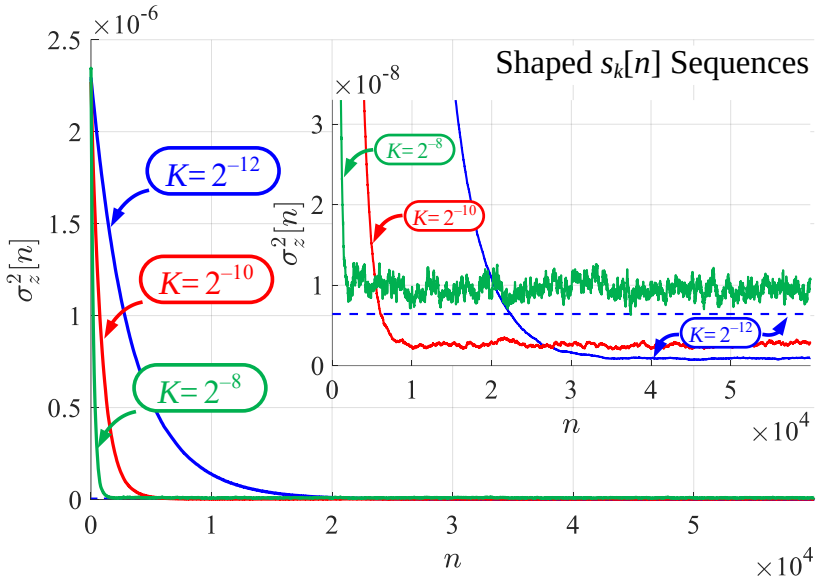

Figure 27: Simulated cold start trajectories (solid curves) of $\sigma_z^2[n]$ for first-order highpass shaped switching sequences with the bound predicted by Theorem 4 (dashed curve)

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