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Electrical Spin Injection and Detection in Ge Nanowires and Topological Insulators

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Electrical Spin Injection and Detection in Ge Nanowires and Topological Insulators

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by

Jianshi Tang

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ABSTRACT OF THE DISSERTATION

Electrical Spin Injection and Detection in Ge Nanowires and Topological Insulators

by

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Professor Kang L. Wang, Chair

The continuous scaling of Si transistor feature size has driven the advancement of semiconductor technology in the past decades; however, such aggressive scaling is approaching the ultimate physical limit soon. Novel materials and devices are in urgent need to resolve a number of critical challenges. In particular, spintronic devices have been proposed and extensively studied by using the spin of electrons as another degree of freedom in devices for information processing, which enables advanced electronic devices that could potentially outperform Si devices with lower power dissipation and faster switching.

In this work, the carrier and spin transport in Ge nanowires will be presented. Atomic-scale thermal annealing was established as a convenient approach to make high-quality nanoscale source/drain contacts in high-performance Ge nanowire transistors. Electrical spin injection and detection in both *p*- and *n*-type Ge nanowires were demonstrated using ferromagnetic Mn_5Ge_3 Schottky contacts and Fe/MgO tunnel junctions, respectively. The measured spin lifetime and spin diffusion length in Ge nanowires were much larger than those reported for bulk Ge, suggesting that the spin relaxation was significantly suppressed in nanowires.

Furthermore, we studied the spin transport in topological insulators, in which the spin-momentum locking of helical surface states was preserved by the strong spin-orbit interaction and time-reversal symmetry. We demonstrated the electrical detection of the spin-polarized surface states conduction in topological insulator $(Bi_{0.53}Sb_{0.47})_2Te_3$ using a Co/Al_2O_3 ferromagnetic tunnel contact. Voltage (resistance) hysteresis was observed when sweeping the magnetic field, and the two resistance states were reversible by changing the electric current direction. Our results showed a direct evidence of the charge current-induced spin polarization in the topological surface states. With the understanding of spin injection and detection, it might open up great opportunities to explore novel spintronic devices based on topological insulators and Ge nanowires.

The dissertation of Jianshi Tang is approved.

Oscar M. Stafsudd

Benjamin S. Williams

Yu Huang

Kang L. Wang, Committee Chair

University of California, Los Angeles

2014

This dissertation is dedicated to my family,

for their unconditional love, encouragement and support

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SYMBOLS AND ACRONYMS

1D/2D/3D	One-/Two-/Three-Dimensional
2DEG	Two-Dimensional Electron Gas
3-T/4-T	Three-/Four-Terminal
AB	Aharonov-Bohm
AFM	Atomic Force Microscopy
AHE	Anomalous Hall Effect
ALD	Atomic Layer Deposition
AMR	Anisotropy Magnetoresistance
ARPES	Angle-Resolved Photoemission Spectrum
BCB	Bulk Conduction Band
BDR	Brinkman-Dynes-Rowell
BVB	Bulk Valence Band
CMOS	Complementary Metal-Oxide-Semiconductor
DMS	Diluted Magnetic Semiconductor
EBL	E-Beam Lithography
EDS	Energy-Dispersive Spectrum/Spectrometer
EELS	Electron Energy-Loss Spectroscopy
FCC	Face-Centered Cubic
FET	Field-Effect Transistor
FFT	Fast Fourier Transform

FIB	Focused-Ion Beam
FM	Ferromagnet/Ferromagnetic Metal
HF	Hydrofluoric Acid
HLN	Hikami-Larkin-Nagaoka
HRTEM	High-Resolution Transmission Electron Microscope
HSQ	Hydrogen Silsesquioxane
HRS	High Resistance State
IPA	Isopropyl Alcohol
LPCVD	Low-Pressure Chemical Vapor Deposition
LRS	Low Resistance State
MBE	Molecular Beam Epitaxy
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MR	Magnetoresistance
MTJ	Magnetic Tunnel Junction
PMMA	Polymethyl Methacrylate
PPMS	Physical Property Measurement System
RA	Resistance-Area
RHEED	Reflection High-Energy Electron Diffraction
RTA	Rapid Thermal Annealing
SC	Semiconductor
SdH	Shubnikov-de Haas
SEM	Scanning Electron Microscope

SFLS	Supercritical Fluid-Liquid-Solid
SOI/SOC	Spin-Orbit Interaction/Coupling
SpinFET	Spin Field-Effect Transistor
SpinLED	Spin Light-Emitting Diode
SQUID	Superconducting Quantum Interference Device
SS	Surface States
TAMR	Tunneling Anisotropy Magnetoresistance
TEM	Transmission Electron Microscope
TMR	Tunneling Magnetoresistance
TI	Topological Insulator
VCMA	Voltage-Controlled Magnetic Anisotropy
VLS	Vapor-Liquid-Solid
ZBR	Zero-Bias Resistance

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Chapter 1

Introduction

1.1 Introduction of Spintronics

The continuous scaling of Si transistor feature size has driven the advancement of semiconductor technology in the past decades. According to the Moore's law, however, such aggressive scaling is approaching the ultimate physical limit soon. Several critical challenges are highlighted in the *International Technology Roadmap of Semiconductors*,[1] including the need to decrease power dissipation and manufacturing variability, as well as the increase in functionality. First of all, there is troublesome energy dissipation from static leakage due to the fact that the CMOS state is volatile and power supply must be on all the time. Besides, the voltage cannot be scaled down further due to the finite threshold voltage V_{th}. Novel physics, materials and devices are in urgent need to resolve those critical challenges. Spintronics (or spin-based electronics) has emerged as a promising solution by utilizing the spin of electrons as another degree of freedom in devices for information processing. It could enable advanced electronic devices with nonvolatility and low threshold voltage to achieve low power dissipation along with increased functionalities.[2-3] In particular, as an appealing substitute for Si complementary metal-oxide-semiconductor (CMOS) devices, several prototypes of spin field-effect transistors (spinFETs) have been proposed and extensively studied because of their nonvolatility nature and additional control of current from the ferromagnetic state other than the gate electrode.[4-8] A typical spinFET is composed of two ferromagnetic contacts on a semiconductor channel, in which the transistor's current drivability is controlled by the magnetization orientation of the two ferromagnetic contacts. The operation of spinFETs typically involves the injection, manipulation and detection of electron spins in the spin/charge transport process.

In 1985, Johnson and Silsbee were the first to successfully demonstrate electrical spin injection and detection from a ferromagnetic metal (permalloy) into a nonmagnetic metal (Al).[9] Johnson then extended the spin injection structure to develop an all-metal three-terminal bipolar spin switch,[4] in which the spin state of the injected carriers was controlled by an external magnetic field. This type of all-metal spintronic devices can take advantage of the nonvolatility of magnetism to reduce the static power dissipation; and at the same time to improve variability.[10] However, the device operation yielded only a small change of the output voltage with no signal gain due to its all-metal construction.

Other than the all-metal construction, several proposals of spinFETs have been attempted in semiconductor structures to exploit the spin-dependent transport of charge carriers with a high spin-current gain. The manipulation of single spins suffers from having both charge and spin currents and thus power dissipation. For example, Nikonov and Bourianoff devised a spin gain transistor based on ferromagnetic semiconductor, whose spontaneous magnetization was initiated by a small spin-polarized current, generating a spin gain of more than 1000 at the output.[11]

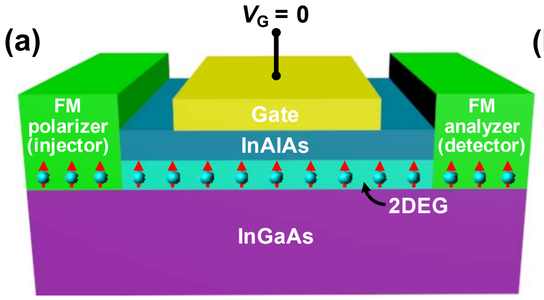

Figure 1-1. Redraw of Datta-Das type spin-polarized FET from Ref. [5].[5] A prototype of spin-polarized FET can be built on a high-mobility InAlAs/InGaAs heterostructure transistor with two-dimensional electron gas (2DEG) channel and ferromagnetic source/drain contacts. (a) ON state under zero gate voltage; (b) OFF state under a positive gate voltage that induces the electron spin precession through the Rashba effect, causing the electron spin is rotated by 180 degree. This device uses both charge and spin currents and the threshold voltage V_{th} is similar to those of CMOS and other 2DEG devices.

In 1990, Datta and Das proposed a spin-polarized FET, an electronic analog to the electro-optic modulator,[5] as shown in Figure 1-1. In this Datta-Das type spinFET, spin-polarized electrons are injected into a semiconductor channel from one ferromagnetic contact (spin injector or polarizer), then the electron spin precession is modulated by the gate voltage through the Rashba effect,[12] and is finally probed by the other ferromagnetic contact (spin detector or analyzer). Here the electron transmission coefficient through the spin detector is determined by the relative orientation between the electron spin after precession and the magnetization of the spin detector. The gate controlled electron spin precession has been observed in an InAs high-electron mobility transistor;[13] however, the full functionality of spin-polarized FET has not been experimentally verified.[14] It should be noted that, while semiconductors with strong spin-orbit interaction (SOI) are usually favored for spin-polarized FET to have an enhanced Rashba effect, the strong SOI could also lead to dramatic degradation in the spin lifetime and spin diffusion length. Therefore, in practice, the semiconductor channel material should be carefully selected for a trade-off between the two.

Another variant of using single spins plus metallic ferromagnets, proposed by Sugahara and Tanaka,[6] is a spin-MOSFET comprised of an ordinary MOSFET with half-metallic source/drain contacts, in which the gate electrode modulates the Schottky barrier shape at the source/drain junctions and hence the current, as shown in Figure 1-2. In the parallel magnetic configuration, the spin-MOSFET operates like an ordinary Schottky barrier MOSFET; while in the anti-parallel magnetic configuration, the half-metal contacts present another barrier for the carrier transport from the source to drain. The barrier filters carriers with an opposite spin direction to the ferromagnetic drain contact, and it can be overcome by a large drain bias. The resulting output characteristic in the anti-parallel magnetic configuration shows a threshold voltage in the drain bias V_{DS}, compared with that in the parallel configuration. Despite of progressive simulation work based on the spin-MOSFET, the full functionality of spin-MOSFET has not been demonstrated so far.[15-18] Also, the growth of stable half metals with high Curie temperatures and the fabrication of a high-quality half metal/semiconductor interface to achieve effective spin injection remains a big technological challenge. The power dissipation issues of this device are similar to those of scaled CMOS with V_{th}, and thus limited by V_{dd}. Likewise, the variability is the same as CMOS.

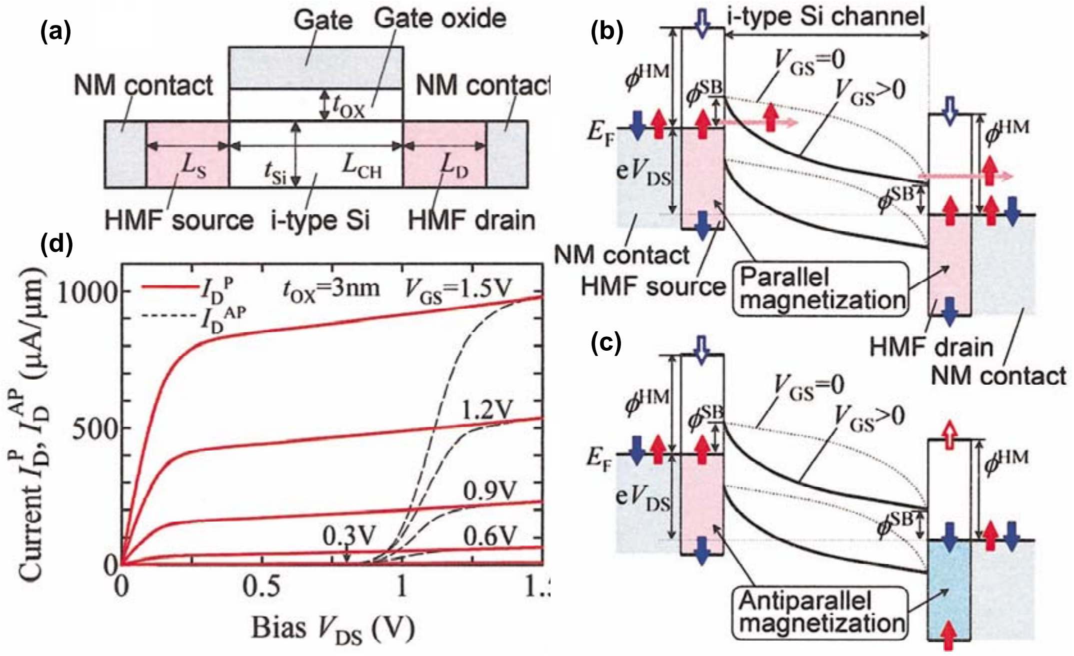

Figure 1-2. Sugahara-Tanaka type spin-MOSFET. (a) Schematic device structure of the spin-MOSFET, composed of an ordinary MOSFET with half-metal source/drain contacts. (b-c) Energy band diagrams of the spin-MOSFET in the parallel and anti-parallel magnetic configurations, respectively. (d) Simulated output characteristics of the spin-MOSFET in the parallel and anti-parallel magnetic configurations. Adopted from Ref. [6].[6]

As we can see, both the spin-polarized FET and the spin-MOSFET modulate single spin of individual electron, hence they have the similar V_{th} limitation and are not energy efficient. Also, the electron spin is mainly used as another handle to modulate the current drivability in the above proposed devices, which are expected to be governed by the same scaling limit of CMOS.[1] All these spinFETs still use electronic charge current along with spin transport that inevitably consumes power through both transport mechanisms. As a result, the potential advantage in reducing the active power dissipation is very limited compared with conventional CMOS devices.[19] In order to make a spinFET that can truly outperform Si CMOS device and meanwhile operate at room temperature, one practical approach is to reduce or eliminate the charge current flow. Besides, another important issue is to operate spin at room temperature, by which magnetic devices (or collective behavior of spins) are preferred. This is one of the motivations of this research, and our unique approach using diluted magnetic semiconductor (DMS) will be described in details in Chapter 3.5.

1.2 Introduction of Spin Injection and Detection

As we can see from the above discussion, electrical spin injection and detection is the one of the key steps to explore practical spintronic devices. In experiments, spin injection and transport are usually electrically characterized by nonlocal spin valve and Hanle precession measurements, from which the spin lifetime and spin diffusion length can be extracted.[20-23] Likewise, optical detection of the spin injection has also been reported in a Si *n*-*i*-*p* spin light-emitting diode (spinLED) structure with Fe/Al_2O_3 tunneling contact by detecting the emitted polarized light.[24] Here we mainly focus on the electrical spin detection in this dissertation. In the nonlocal spin valve measurement, an in-plane magnetic field is applied along the easy axis of the ferromagnetic spin injector and detector in order to change the relative magnetization direction of the two, as shown in Figure 1-3(a). A spin-polarized current is injected from a ferromagnetic contact (spin injector) to create a spin accumulation in the semiconductor channel. As the spin-polarized carriers diffuse away from the spin injector, another ferromagnetic contact (spin detector), placed outside the charge current loop, probes the spin-dependent electrochemical potential of one spin channel (spin up or spin down) related to the reference contact. Therefore, as the relative magnetization direction of the spin injector and the detector switches from parallel state to anti-parallel state, a bipolar nonlocal voltage V_{NL} should be sensed, namely $V_{\mathrm{p}}>0$ and $V_{\mathrm{ap}}<0$ in the ideal case. As the spin potential sense loop is separated from the current loop to avoid any suspicious artifacts, the nonlocal spin valve signal is usually considered as a clear and conclusive evidence for successful spin injection.

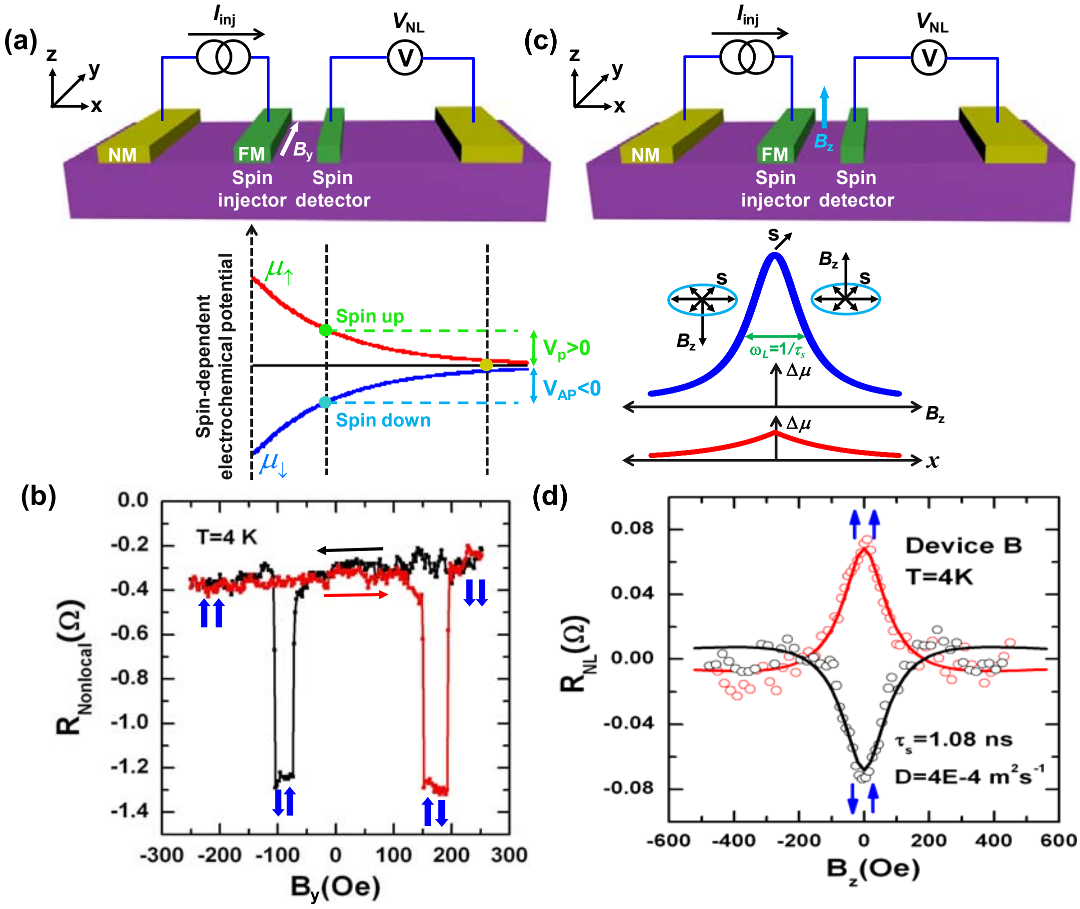

Figure 1-3. Nonlocal spin valve and Hanle measurements. (a) Schematic illustration of nonlocal spin valve measurement in which the in-plane magnetic field is applied along the easy axis of the ferromagnetic spin injector and detector. (b) Nonlocal spin valve signal measured in Ge at the temperature of 4 K. The black and red arrows indicate the sweeping direction of the magnetic field. The blue arrows indicate the relative magnetization directions of the spin injector and the detector. (c) Schematic illustration of Hanle measurement in which the out-of-plane magnetic field is applied

perpendicular to the FM/SC interface. (d) Nonlocal Hanle precession signal measured in Ge at the temperature of 4 K. The blue arrows indicate the relative magnetization directions of the spin injector and the detector. Experimental data (b) and (d) are adopted from Ref. [21].[21]

Theoretically, in the tunneling spin injection case where the tunnel barrier resistance is typically much larger than the channel resistance over a spin diffusion length ($R_N = l_{sf}/\sigma_s A$), the nonlocal spin valve signal can be derived the one-dimensional spin drift-diffusion model as:[20]

$$\frac{V_{NL}}{I_{inj}} = \pm\frac{1}{2}{P_J}^2\frac{\lambda_{sf}}{\sigma_s A}\exp\left(-\frac{L}{l_{sf}}\right) \qquad (1-1)$$

where P_J is the spin polarization of the current I_{inj} injected from the spin injector into the semiconductor channel and is defined as $P_J = (J_\uparrow - J_\downarrow)/(J_\uparrow + J_\downarrow)$ with $J_\uparrow$ ($J_\downarrow$) being the majority (minority) spin current density, l_{sf} is the spin diffusion length, σ_s is the semiconductor conductivity, A is the semiconductor channel cross-sectional area, and L is the spatial distance between the spin injector and the detector. The + (−) sign denotes the parallel (anti-parallel) magnetization state for the spin injector and the detector. In practice, there is typically a nonzero background voltage on the measured V_{NL};[25] however, the bi-state nonlocal voltage should be observed when changing the relative magnetization direction of the spin injector and the detector. Therefore, the amplitude of the nonlocal spin valve signal is usually measured for further physical interpretation (such as the extraction of the spin diffusion length), and it is obtained from Equation (1-1) as:

$$\Delta R_{NL} = \frac{|V_p - V_{ap}|}{I_{inj}} = {P_J}^2 \frac{l_{sf}}{\sigma_s A} \exp\left(-\frac{L}{l_{sf}}\right) \qquad (1-2),$$

which is a simple exponential decay function of the spatial distance L with respect to the spin diffusion length l_{sf} (typically hundreds of nanometers. See Table 1-1 below for literature-reported values). It also suggests that, in order to observe an appreciable nonlocal spin valve signal, the designed distance between the spin injector and the detector in practical devices is required to be at most comparable with the spin diffusion length, and hence high-resolution e-beam lithography (EBL) is usually adopted in the device fabrication. Figure 1-3(b) shows an example of typical nonlocal spin valve signals measured from Ge,[21] in which the nonlocal voltage changed between V_p and V_{ap} as the magnetic field was swept back and forth.

On the other hand, in the Hanle measurement, a out-of-plane magnetic field is applied to induce the spin precession along the magnetic field direction as the injected spin-polarized carriers diffuse away from the ferromagnet/semiconductor (FM/SC) interface, as shown in Figure 1-3(c).[23] Hanle measurements can be performed in both three-terminal (3-T, usually referred as “local”) device structure and four-terminal (4-T, referred as “nonlocal” or “NL”) device structure. However, the 4-T nonlocal measurement technique is usually adopted to detect the intrinsic spin injection signal in order to avoid any spurious signals.[26] In this device configuration, the spin injector and the spin detector are spatially separated so that the spin signal sense loop is separated from the charge current loop, compared with the 3-T device configuration in which the spin injector and detector uses the same ferromagnetic contact. Similar to the nonlocal spin valve device, the distance between the spin injector and the detector in the 4-T Hanle device needs to be at most comparable with the carrier spin diffusion length; hence high-resolution electron-beam lithography is usually adopted in the device fabrication. Theoretically, the precession and dephasing of the injected spins as a function of the magnetic field can be described using the one-dimensional spin drift-diffusion model.[20] The applied out-of-plane magnetic field B_z changes the electron spin direction by an angle of $\varphi = \omega_L t$ through spin precession in a certain period of time t, where $\omega_L = g\mu_B B_z/\hbar$ is the Larmor frequency (g is the Landé g-factor of the electron, μ_B is the Bohr magneton, $\hbar$ is the reduced Planck constant). The spin detector detects the projection of the electron spin direction on its own magnetization; therefore, the contribution of an electron to the output voltage V_{NL} is proportional to $\pm\cos(\varphi)$, where the + (–) sign denotes the parallel (anti-parallel) magnetization state for the spin injector and the detector. In a diffusive channel, the probability for the injected electrons from the spin injector to arrive at the spin detector (with a spatial distance of L from the injector) after a diffusion time t follows a Gaussian distribution, and it is given by:[20]

$$P(t) = \frac{1}{\sqrt{4\pi D t}} \exp\left(-\frac{L^2}{4Dt}\right) \qquad (1-3),$$

where D is the diffusion constant. During this time t, the spin polarization is also reduced by a factor of $\exp(-\,t/\tau_s)$ through spin relaxation in the channel, where τ_s is the spin lifetime. Then, the output voltage V_{NL} at the spin detector as a function of B_z

can be calculated by summing the contributions of the electron spins over all diffusion times *t*:[20]

$$\frac{V_{NL}}{I_{inj}} = \pm {P_J}^2 \frac{D}{\sigma_s A} \int_0^{\infty} \frac{1}{\sqrt{4\pi D t}} \exp\left(-\frac{L^2}{4Dt}\right) \cos(\omega_L t) \exp\left(-\frac{t}{\tau_s}\right) \mathrm{d}t \qquad (1-4)$$

It should be noted that for the case where $\omega_L = 0$ (or equivalently $B_z = 0$), Equation (1-4) reduces to Equation (1-1) for the nonlocal spin valve signal amplitude. From the Hanle curve, D and τ_s can be obtained by numerical fitting, and then the spin diffusion length can be calculated as $l_{sf} = \sqrt{D\tau_s}$. Under certain circumstance (especially for 3-T device geometry where the dimension of the ferromagnetic contact is typically much larger than the spin diffusion length), the Hanle curve can be approximately represented with a Lorentzian function:[23]

$$V_{NL} = \frac{V_0}{1 + (\omega_L \tau_s)^2} \qquad (1-5)$$

where the spin lifetime can be easily found as the reciprocal of the full width at half maximum of the Lorentzian curve. Figure 1-3(d) shows an example of typical nonlocal Hanle curves measured from Ge, in which the polarity of the Hanle voltage depends on the relative magnetization direction of the spin injector and detector. Besides, it is noting that inverted Hanle measurements are also reported as an important evidence for successful spin injection,[27] especially for 3-T device configuration. Different from the normal Hanle measurement, the magnetic field in the inverted Hanle measurement is applied in-plane along the easy axis of the ferromagnetic spin injector and detector, which effectively suppresses the spin precession and hence increases the spin accumulation. Therefore, the measured inverted Hanle signal looks like a upside-down (so-called “inverted”) Lorentzian function.[27]

1.3 Spin Lifetime and Diffusion Length in Bulk Semiconductors

In literature, there have been extensive studies on the spin lifetime and spin diffusion length in both *n*-type and *p*-type Ge/Si under a wide range of conditions, including doping concentrations from intrinsic to degenerate level, temperatures from liquid helium temperature to room temperature and up to 500 K, different ferromagnetic metals and barriers (tunneling oxides and Schottky barrier). Most experiments are carried out in 3-T device geometry rather than 4-T geometry, mainly because that the former one benefits from its simple device fabrication process in which convenient photolithography rather than sophisticated electron-beam lithography is sufficient. For bulk Si/Ge with crystal inversion symmetry, the spin relaxation is dominated by the Elliott-Yafet mechanism, in which the spin relaxation is accompanied by momentum scatterings (by phonons and impurities) through the SOI.[2] Table 1-1 lists selected literature results of carrier spin lifetime and diffusion length for Ge/Si bulk and thin films. (A broader literature survey of spin lifetimes specifically in *n*-type Si can be found in Ref. [25].[25])

Table 1-1. Typical spin lifetime and diffusion length in Ge/Si bulk and thin film.

SC	***n* or *p*** **(cm^{-3})**	**FM**	**Barrier**	**Method**	**T (K)**	**τ_{sf} (ns)**	**l_{sf} (μm)**
***i*-Si**	undoped	$Co_{84}Fe_{16}$	Schottky	Hot e^-	85	1	N/A[28]
***n*-Si**	5×10^{19}	Fe	Al_2O_3	NL	10	0.9	0.95[29]
	5×10^{19}	Fe	MgO	NL/3-T	8	8.95/8.50	1.72/1.68[30]
	3×10^{18}	$Ni_{80}Fe_{20}$	SiO_2	3-T	10	0.32	0.19[31]
	1×10^{19}	$Ni_{80}Fe_{20}$	Graphene	3-T	4	0.14	0.12[32]
	1.8×10^{19}	$Ni_{80}Fe_{20}$	Al_2O_3	3-T	300	0.14	0.23[23]
	6×10^{17}	CoFe	Schottky	3-T	300/40	1.36/3.02	N/A[33]
***p*-Si**	4.8×10^{18}	$Ni_{80}Fe_{20}$	Al_2O_3	3-T	300	0.27	0.31[23]
***p*-Ge**	8.2×10^{18}	Fe	MgO	3-T	300	0.013	0.08[34]
***n*-Ge**	2×10^{19}	Fe	MgO	NL	4	1.08	0.58[21]
	2.5×10^{18}	CoFe	MgO	3-T	300	0.12	0.683[35]
	10^{18}-10^{19}	$Ni_{80}Fe_{20}$	Al_2O_3	3-T	10	0.035	N/A[36]
	10^{18}	Fe	Schottky	3-T	50	0.14	0.63[37]

It is noted that there is a large discrepancy among the values obtained by different research groups. This is because that the spin injection process is very sensitive to the FM/SC interface, which is closely related to how the FM/SC junction is prepared. Interface defects, such as the surface roughness and interface states, may trap electron spins or jeopardize the spin transport through the FM/SC interface.[27] Also, different measurement methods (3-T *versus* 4-T nonlocal technique) could also give very different results, arising from the surface roughness-induced magnetostatic fields and the bias effect on the spin transport process.[26-27] In general, Si is found to have a relatively longer spin lifetime compared with Ge, which is because that Si (E_{SO} = 44 meV) has a much weaker SOI than Ge (E_{SO} = 290 meV).

To get a better understanding of the spin lifetime dependence on the SOI, we plot the measured spin lifetime of Ge/Si as a function of the SOI strength represented by the spin-orbit splitting energy (E_{SO}), as shown in Figure 1-4. We also included selected literature results from weak SOI material (graphene,[38-39] and GaN[40]) and strong SOI materials (GaAs,[41-42] InAs,[43] and InSb[44]). Although in compound materials lacking crystal inversion symmetry, the D'yakonov-Perel' spin relaxation mechanism (mediated by intrinsic internal magnetic fields induced by inversion asymmetry) becomes important and even dominated,[2] they generally follow the trend that stronger SOI renders smaller spin lifetime. Elliot has shown that the electron spin relaxation time (spin lifetime) τ_{sf} is related to the elastic scattering time (momentum relaxation time) τ_{e} through the SOI in the case of Elliot-Yafet spin relaxation mechanism:[45-47]

$$\frac{\tau_{\mathrm{e}}}{\tau_{\mathrm{sf}}} = \mathrm{const} \propto \left(\frac{\lambda}{\Delta E}\right)^2 \qquad (1-6)$$

where λ is the atomic SOI constant for a specific energy band, ΔE is the energy gap between the considered energy band to the nearest one that is coupled through the atomic SOI, and the ratio of $\tau_{\mathrm{e}}/\tau_{\mathrm{sf}}$ is shown to be temperature independent. Here the square comes from the calculation of scattering probability between two opposite spin states.[47] Qualitatively, the general trend in Figure 1-4 agrees with Equation (1-5): the stronger SOI strength, the stronger spin relaxation, and hence the smaller spin lifetime.

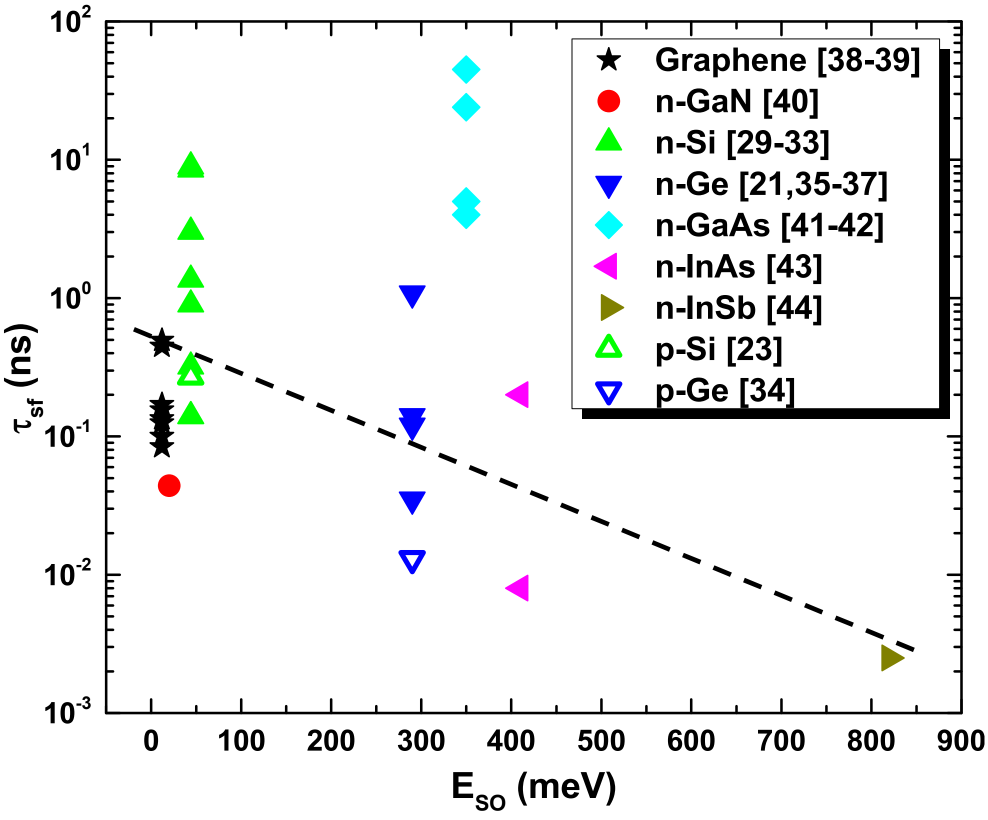

Figure 1-4. Literature reported spin lifetimes in various semiconductors as a function of the SOI strength represented by the spin-orbit splitting energy. The references of

experimental data are given in the legend. The dash line is a guide to the eye. In general, they follow the trend that stronger SOI leads to stronger spin relaxation and hence smaller spin lifetime.

1.4 Motivation for Spin Transport in Ge Nanowire

In the fabrication of most spintronic devices, it is essential to achieve an efficient spin injection in semiconductors and further to effectively manipulate the spin transport in them. Following this rationale, the spin injection and transport in a broad range of semiconductors (such as Si,[23-24] Ge,[21,35] GaAs,[42,48] *etc*) have been extensively studied to seek for long carrier spin lifetime and diffusion length. Most pioneer work has been conducted on bulk and thin film semiconductors, because they are easy to tune the doping profile and fabricate into devices. As shown in Table 1-1 and Figure 1-4 above, the measured spin lifetime ranges from tens of picoseconds to several nanoseconds, and the diffusion length is typically hundreds of nanometers.

To further explore new materials with long spin lifetime and diffusion length, low-dimensional semiconductor quantum structures have attracted numerous interests because of their unique physical properties for electron electrical and spin transport. Again, Si/Ge-based nanostructures are of particular interest among all the candidates because of their ready integration into the current Si technology. For example, Ge/Si quantum well structures produce a high-mobility 2D electron/hole gas channel, which may promise for a long spin diffusion length. Ge/Si nanowires on the other hand provide a one-dimensional channel with substantial quantum confinements. In those low-dimensional Ge/Si nanostructures, the crystal inversion symmetry is not preserved (for example, the inversion symmetry in Ge/Si heterostructures is broken by the presence of asymmetric confining potentials). Therefore, the absent

D'yakonov-Perel' spin relaxation mechanism in bulk crystals become appreciable in Ge/Si nanostructures. The breaking of inversion asymmetry in quantum wells increases the SOI, which could improve the gate modulation of the spin transport through the Rashba effect but meanwhile decrease the carrier spin lifetime. It has been demonstrated that the electrical spin injection into InAs quantum wells with a spin lifetime of only several picoseconds.[43] To date, however, little progress has been made on the electrical spin injection into Ge/Si quantum wells. Very recently, the optical spin injection in Ge/SiGe quantum wells was evidenced by the photoluminescence, showing a very short spin lifetime for holes of 0.5 ps.[49]

Despite of the short spin lifetime in quantum well structures, semiconductor nanowires on the other hand could have very long spin lifetimes, even longer than those in bulk materials. This is because that the phonon scattering is significantly suppressed in nanowires because of a reduced density of states,[50] so that the momentum relaxation and hence the spin relaxation is effectively reduced in the Elliott-Yafet mechanism. Also, the one-dimensional channel confines the momentum along the wire axis, and all the spin rotations are limited to a single axis; therefore, the spin dephasing induced by the randomizing momentum-dependent magnetic field in the D'yakonov-Perel' spin relaxation mechanism is minimized.[51] It has been experimentally observed that the spin relaxation rate in submicron InGaAs wires was significantly suppressed for widths that are up to one order of magnitude larger than the electron mean free path.[52] Although on the other hand the surface roughness scattering, considering the large surface-to-volume ratio of nanowires, may contribute to additional spin relaxation,[53] the suppressed Elliott-Yafet and D'yakonov-Perel' mechanisms, along with surface passivation and engineering, could effectively reduce the overall spin relaxation in nanowires compared with bulk materials. In fact, it has been experimentally demonstrated that spin relaxation can be suppressed by quantum confinements in both $Ga_xIn_{1-x}As$/InP quantum wires and InAs nanowires, as evidenced by the crossover from weak anti-localization to weak localization as the wire width (diameter) is reduced.[54-55] Recently there have been increasing research efforts in realizing electrical spin injection into semiconductor nanowires, and several pioneer work has indeed revealed a longer spin lifetime and diffusion length in nanowires compared with their bulk counterparts.[7-8,56-60] The results from literature (including this dissertation) are summarized in Table 1-2. This motivates us to study the spin transport in Ge nanowires and to further build Ge-based spintronic devices, which is of both physical and technological significance.

Table 1-2. Comparison of spin lifetime and diffusion length in semiconductor nanowires (NW) and bulk.

SC		n or p (cm^{-3})	FM	Barrier	Method	T (K)	τ_{sf} (ns)	l_{sf} (μm)
n-Si	**NW**[58]	3×10^{19}	Co	Al_2O_3	2-T/NL	5	90	6
	bulk[29]	5×10^{19}	Fe	Al_2O_3	NL	10	0.9	0.95
n-Ge	**NW**[8]	9×10^{18}	Fe	MgO	NL	40	7.2	2.57
	bulk[21]	2×10^{19}	Fe	MgO	NL	4	1.08	0.58
p-Ge	**NW**[7]	8×10^{18}	Mn_5Ge_3	Schottky	2-T	10	0.244	0.48
	bulk[34]	8.2×10^{18}	Fe	MgO	3-T	5-300	0.013	0.08
n-GaN	**NW**[59]	1×10^{17}	CoFe	MgO	NL	300	0.1	0.26
	bulk[40]	4.2×10^{17}	MnAs	AlAs	3-T	300	0.044	0.175
n-InN	**NW**[60]	1.1×10^{20}	Co	Al_2O_3	NL	4	0.27	0.31

1.5 Dissertation Outline

This dissertation will be organized into three closely-related projects. In Chapter 2, we will first discuss the contact engineering in Ge nanowire transistors, in which an atomic-scale thermal annealing process was established to make high-quality nanoscale source/drain contacts in high-performance Ge nanowire transistors, including Ni_2Ge, NiGe, Ni_3Ge and Mn_5Ge_3. Then in Chapter 3, we will first describe the magneto-transport studies in single-crystalline Mn_5Ge_3 nanowire. Then we will present the studies of spin transport in Ge nanowires, where the electrical spin injection and detection in both *p*- and *n*-type Ge nanowires were demonstrated using ferromagnetic Mn_5Ge_3 Schottky contacts and Fe/MgO tunnel junctions, respectively. The proposal of a novel DMS nanowire-based transpinor device will also be described in this chapter. In Chapter 4, we will present the spin transport in topological insulator (TI), focusing on the electrical detection of the spin-polarized surface states conduction. Besides, the molecular beam epitaxy (MBE) growth of topological insulator will also be concisely introduced in this chapter. Finally, a brief discussion and conclusion will be given in Chapter 5, followed by an outlook of future work.

Chapter 2

Contact Engineering in Ge Nanowire Transistors

2.1 Overview

As an important one-dimensional material, semiconductor nanowires have attracted enormous research interest for their unique electrical properties. As summarized in Figure 2-1, they have shown promising applications as building blocks for nanoelectronics, such as FETs, logic units, memory devices and sensors.[61-67]

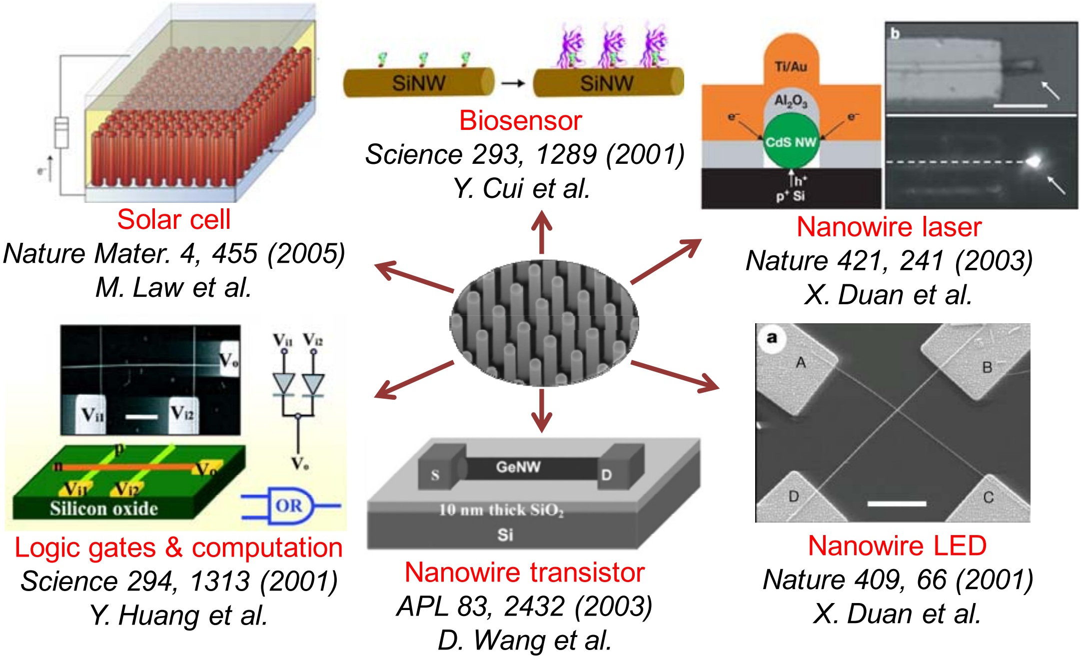

Figure 2-1. Broad applications of semiconductor nanowires, including FET, logic unit, solar cell, biosensor, laser and LED.

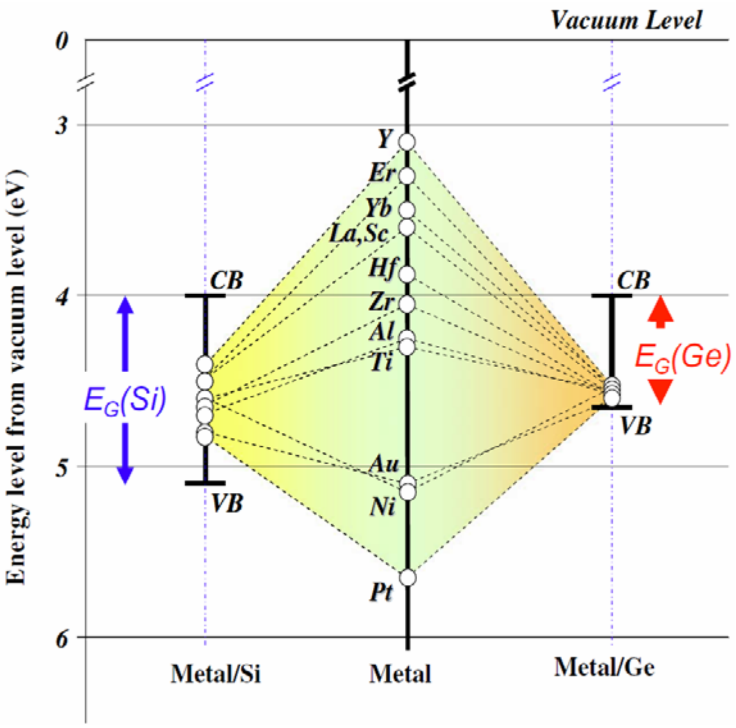

Figure 2-2. Schottky barrier heights for various metal/Si and metal/Ge contacts with different metal work functions. In the case of Ge, the Fermi level is strongly pinned close to the Ge valence band edge. Adopted from Ref. [68].[68]

Group IV materials (Si/Ge) are of particular interest because of their high compatibility to the existing Si CMOS technology. In the fabrication of nanoscale devices, it is a great challenge to make high-quality electrical contacts to nanowires, considering the large surface-to-volume ratio in nanostructures along with the high-density interface states. It is worth noting that the interface states would induce severe Fermi level pinning in metal/semiconductor contacts.[68] For example, the Fermi level in conventional metal/bulk Ge contacts is strongly pinned close to the Ge valence band edge, as shown in Figure 2-2. Even for Si with a lower density of interface states, the ideal Schottky-Mott limit with an interface index $S = 1$ is hardly observed. Such Fermi level pinning effect is expected to be even severer in Si/Ge nanowire devices, which have a larger surface-to-volume ratio and hence higher density interface states, and hence significantly degrades the nanoscale device performance.

To address this Fermi-level pinning issue in semiconductor nanowire devices with direct metal contacts, there have been extensive efforts since 2004 studying the thermal diffusion of metal into a single-crystalline Si nanowire, in which a silicide/silicon/silicide nanowire heterostructure is formed by solid-state reactions between the Si nanowire and metal contacts. Many metals (contact pads or nanowires) have been studied as the diffusion source, such as Ni,[69-71] Co,[72] Pt,[73] and Mn.[74] One of the salient features in this nanowire heterostructure is the atomically sharp interface between the Si nanowire and the formed silicide nanowire. Such clean interface may help to avoid Fermi-level pinning effect. Also, the nanowire heterostructure can be easily used to fabricate nanowire FETs using the formed silicide regions as the source/drain contacts to the Si nanowire channel.[69-70,73] The channel length can be well controlled by the annealing time and growth length of silicide, therefore, can be aggressively scaled down to sub-20 nm.[75] Clearly this process offers great advantages over modern high-cost and complex photolithography technology to fabricate short-channel transistors, and may further facilitate the advance of scaled nanodevices.

Compared with Si nanowire, metal-Ge nanowire is a new system of interest, because Ge is an important complement to Si with the highest hole mobility for further device miniaturization that is compatible to the existing CMOS technology.[76] The atomically sharp interface is of particular interest for Ge to alleviate the significant Fermi-level pinning effect in the metal-Ge contact. Particularly, nickel silicides and germanides were evaluated to be the most favored contact materials in CMOS technology due to their low resistivity and good thermo-kinetic quality.[77-78] Moreover, many germanides, such as Mn_5Ge_3 and Ni_3Ge, exhibit ferromagnetism above room temperature,[79-80] and thus offer great advantages over silicides for future applications in spintronics, such as realizing spin injection into semiconductor from a ferromagnetic contact. In this chapter, we will present the contact engineering in Ge nanowire transistors through rapid thermal annealing (RTA) and demonstrate high-quality Ge nanowire source/drain contacts, including Ni_2Ge (Chapter 2.2), NiGe (Chapter 2.3), and Mn_5Ge_3 (Chapter 2.4). In the end, we will briefly discuss on the interface lattice mismatch in Ge/Si nanowire heterostructures and the effect of the atomically clean interfaces on the Fermi level pinning effect (Chapter 2.5).

2.2 Single-Crystalline $Ni_2Ge/Ge/Ni_2Ge$ Nanowire Heterostructure Transistor

To fabricate the Ni-Ge nanowire device, single-crystalline Ge nanowires with <111> growth direction were firstly synthesized by the supercritical fluid-liquid-solid (SFLS) process developed by Tuan et al,[81] in which the Ge nanowire reaction was carried out in a 10 mL titanium-grade 2 reactor. In short, the reactant solution composed of 0.1 M concentration in Ge moles and dodecanethiol-capped Au nanocrystals (Au/Ge molar ratio of 1:1000) in anhydrous toluene was prepared in a nitrogen-filled glovebox. After the titanium cell was heated to 420 °C and pressurized to 700 psi, the prepared reactant was removed from the glove box, injected into a 0.5 mL injection loop, and then injected into the reactor by a HPLC pump at a flow rate of 0.5 mL/min until reaching a final pressure of 1300 psi. After reaction (~ 5 min), the reactor was cooled by submerging the reactor in a water bath for 2 min. The Ge nanowires collected from the reaction were then used for further device fabrication. Compared with the vapor-liquid-solid (VLS) method, the SFLS method provides better nanowire size control and higher product yields,[82-83] although the reported mobility of SFLS-synthesized Ge nanowires is lower. The typical diameter of as-synthesized Ge nanowires is around 40~50 nm and the length could be more than 10 μm. As-synthesized Ge nanowires are undoped, however, unintentionally *p*-type doping usually exists.[84-85]

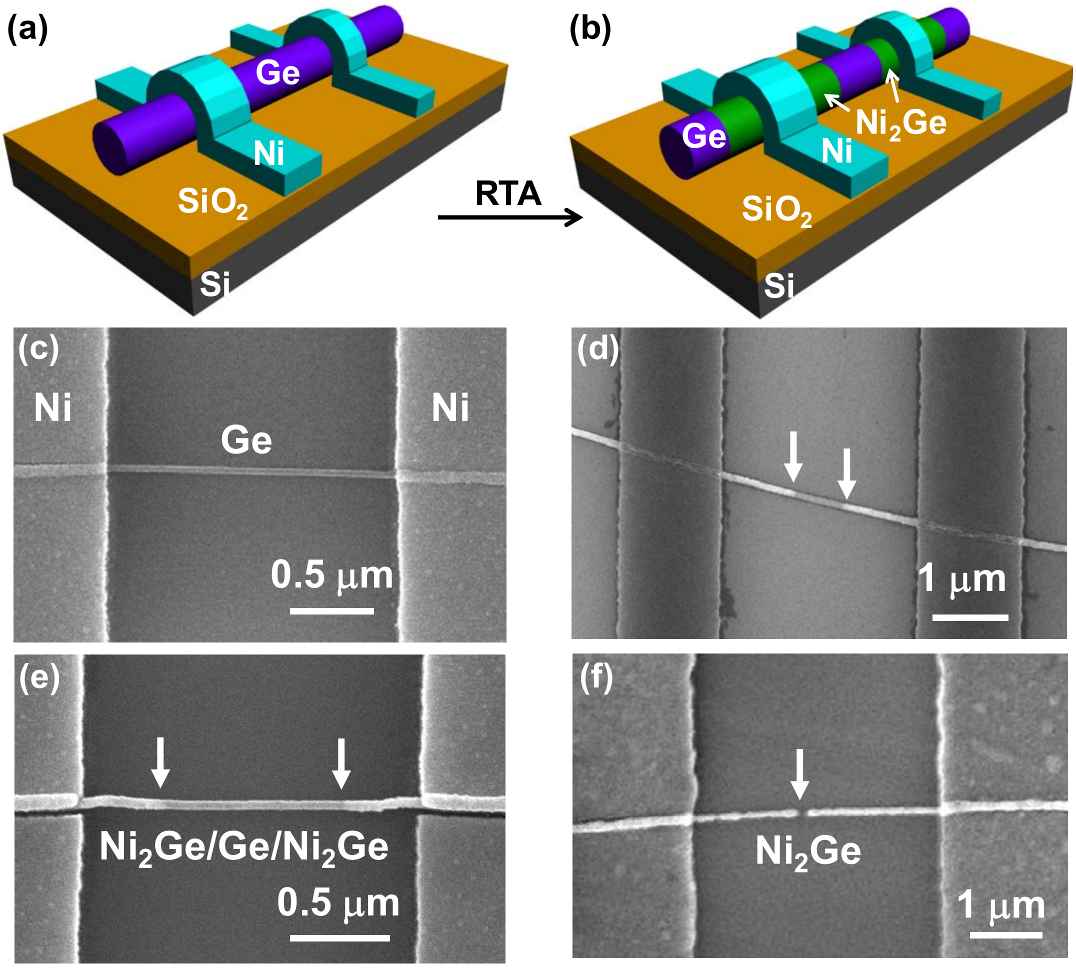

Figure 2-3. Formation of $Ni_2Ge/Ge/Ni_2Ge$ nanowire heterostructure. Schematic illustration showing before (a) and after (b) the thermal diffusion process of Ni into the Ge nanowire forming a $Ni_2Ge/Ge/Ni_2Ge$ heterostructure. (c) SEM image of the Ge nanowire device with EBL-defined Ni electrodes. (d) SEM image of the $Ni_2Ge/Ge/Ni_2Ge$ heterostructure after RTA at 500 °C for 60 s in which the length of the Ge region was easily controlled to sub-micron range. The arrows indicate the growth tips of the Ni_2Ge nanowire. (e) SEM image of the $Ni_2Ge/Ge/Ni_2Ge$ heterostructure after RTA at 400 °C for 40 s. The arrows indicate the growth tips of

the Ni_2Ge nanowire. (f) SEM image of a broken nanowire after further annealing. The arrow highlights the broken region due to volume expansion. (The data also appeared in my publication Ref. [86].[86])

To form Ni_xGe/Ge nanowire heterostructures, SFLS-synthesized Ge nanowires diluted in isopropyl alcohol (IPA) were dispersed onto a SiO_2/Si substrate. The top thermal SiO_2 was about 330 nm thick. The Si substrate was degenerately doped with a resistivity of 1-5 $\times 10^{-3}$ Ω-cm, which served as a back-gate for further device characterization. EBL was used to define Ni contacts to Ge nanowires. Before e-beam evaporation of about 120 nm-thick Ni (with the purity of 99.995 % and in vacuum at a pressure lower than 10^{-6} Torr), the sample was dipped into diluted hydrofluoric acid (HF) solution for 15 s to completely remove native oxide in the contact region. A field-emission scanning electron microscope (JEOL JSM-6700 FESEM) was used to examine the sample morphology before and after the annealing process. Figure 2-3(a) and (b) show the device schematics before and after the thermal diffusion of Ni into the Ge nanowire. Figure 2-3(c) shows the SEM image of the as-fabricated Ge nanowire device showing a uniform contrast. Then the sample was annealed with RTA in the ambient of N_2 to allow Ni thermal intrusion into Ge nanowire and subsequently form Ni_xGe/Ge heterostructures along the nanowire. In the previous study on the interfacial reactions of Ni thin film on Ge(111) substrate, the germanide phase formation sequence was found to be Ni_2Ge and NiGe at increasing temperatures in the range of 160 ^{o}C to 600 ^{o}C.[87] Various annealing temperatures ranging from 400 to 700 °C were used in this study to optimize the formation of nanowire heterostructures. It is found out that Ge nanowires were easily broken at a high annealing temperature (>550 °C) due to the significant reduction of the melting point for Ge nanowires compared with that of bulk Ge.[88] When the temperature decreased to 400-500 °C, clear diffusion of Ni into the Ge nanowire was also observed and the formed germanide was identified to be Ni_2Ge (refer to the TEM analysis later). Figure 2-3(d) shows the SEM image of the Ge nanowire device upon RTA at 500 °C for 60 s, in which clear contrast was observed between the Ge nanowire and the formed nickel germanide nanowire due to the conductivity difference. The remained Ge region was easily controlled down to 650 nm, and it can be further reduced to sub-20 nm.[75] Similar contrast was also observed after RTA at 400 °C for 40 s, as shown in Figure 2-3(e). Volume expansion and segregation of nickel germanide were noticed at the same time (see Figure 2-6). It is noted that the nanowire could be broken after further annealing due to excessive Ni diffusion (Figure 2-3(f)).

In order to identify the phase of the formed germanide and the epitaxial relationship of germanide-germanium interface, *in-situ* transmission electron microscope (TEM) was used to study the formation process and reaction kinetics. To prepare the TEM sample, the single-crystalline Ge nanowires were dispersed on the TEM grid with a square opening of a Si_3N_4 thin film. The low-stress Si_3N_4 film was deposited by low-pressure chemical vapor deposition (LPCVD). The Si_3N_4 film was about 50 nm thick which provided a reliable mechanical support for Ge nanowire devices during the fabrication process; meanwhile, to assure it is transparent to the electron beam without interference with images of the nanowires. EBL-defined Ni pads were employed as the Ni diffusion source. A JEOL-2010 TEM (operated at 200 kV with a point-to-point resolution of 0.25 nm) attached with an energy-dispersive spectrometer (EDS) was used to investigate the microstructures and to determine the compositions of the samples. To *in-situ* observe the reactions of the Ni electrodes with Ge nanowires, the samples were heated inside TEM with a heating holder (Gatan 652 double tilt heating holder connected with a power supply to heat up the samples to the desired temperature) under a RTA mode with a pressure below 10^{-6} Torr. Figures 2-4(a-c) show the high-resolution TEM (HRTEM) images of the formed Ni_xGe/Ge interface upon 500 ^{o}C annealing. According to the lattice-resolved HRTEM analysis, the formed germanide was identified to be single-crystalline Ni_2Ge with an orthorhombic lattice structure and lattice constants a = 0.511 nm, b = 0.383 nm, and c = 0.726 nm (space group 62). It was observed that a large lattice mismatch of 56.3% at the Ni_2Ge/Ge epitaxial interface could result in the segregation of nanoparticles (see Figure 2-6). In Figure 2-4(b), a clean and sharp interface between Ni_2Ge/Ge was observed with an approximately 1 nm GeO_x shell surrounding both the Ge and Ni_2Ge regions. The insets in Figures 2-4(a) and (c) illustrate the fast Fourier transform (FFT) patterns of the Ni_2Ge and Ge HRTEM images, respectively. The crystallographic epitaxial relationships between Ge and Ni_2Ge were shown to be: Ge$[01\bar{1}]$//$Ni_2Ge[0\bar{1}1]$ and Ge$(1\bar{1}\bar{1})$//$Ni_2Ge(100)$. Figures 2-4(d) and (e) show the low-magnification TEM images of Ge NWs before and after RTA at 500 °C, respectively. Figure 2(f) shows the EDS of the formed germanide nanowire region, showing that the ratio of Ni to Ge concentration was about 2:1, which further support the fact that the formed germanide phase is Ni_2Ge. The signals of Si and N peaks originated from the Si_3N_4 window.

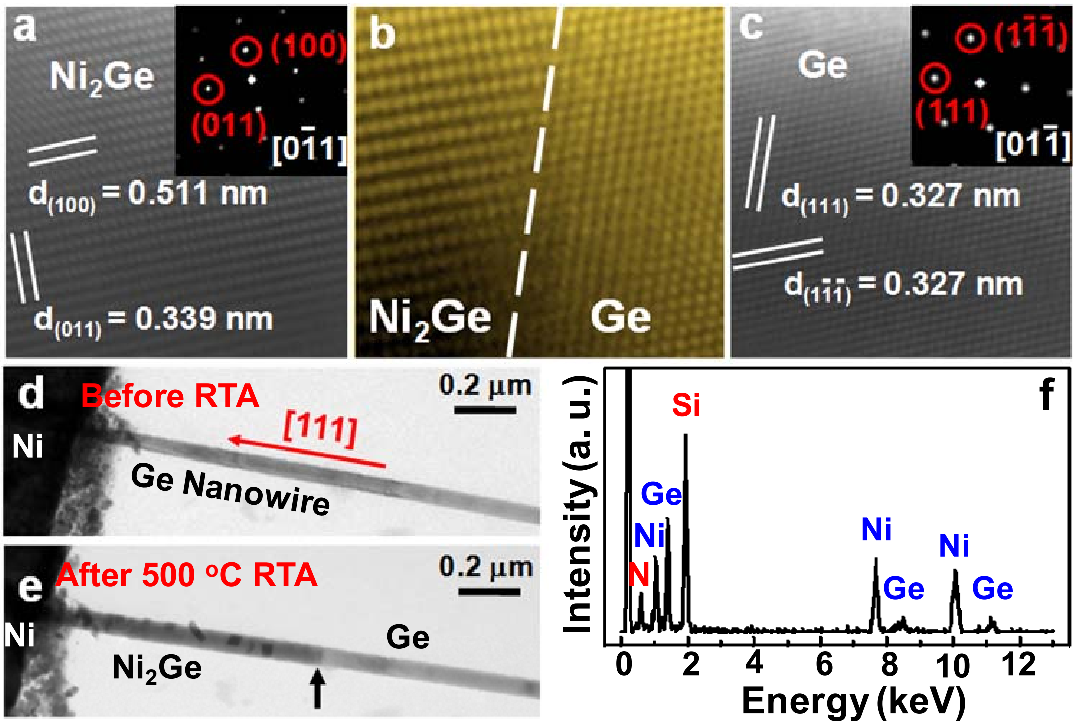

Figure 2-4. Epitaxial relationship at the Ni_2Ge/Ge interface. (a) Lattice-resolved TEM image of the formed Ni_2Ge nanowire. The inset shows the corresponding FFT pattern, confirming that the formed germanide phase is Ni_2Ge. (b) TEM image of Ni_2Ge/Ge heterostructure showing an atomically sharp interface. (c) Lattice-resolved TEM image of the unreacted Ge nanowire. The inset shows the corresponding FFT pattern. (d) Low-magnification TEM image of the as-fabricated device with the Ni pad and the Ge nanowire. (e) Low-magnification TEM image after annealing at 500

^{o}C. The arrow indicates the interface of the Ni_2Ge/Ge nanowire. (f) EDS spectrum of Ni_2Ge, showing a relative 2:1 concentration ratio of Ni and Ge atoms. (The data also appeared in my publication Ref. [86].[86])

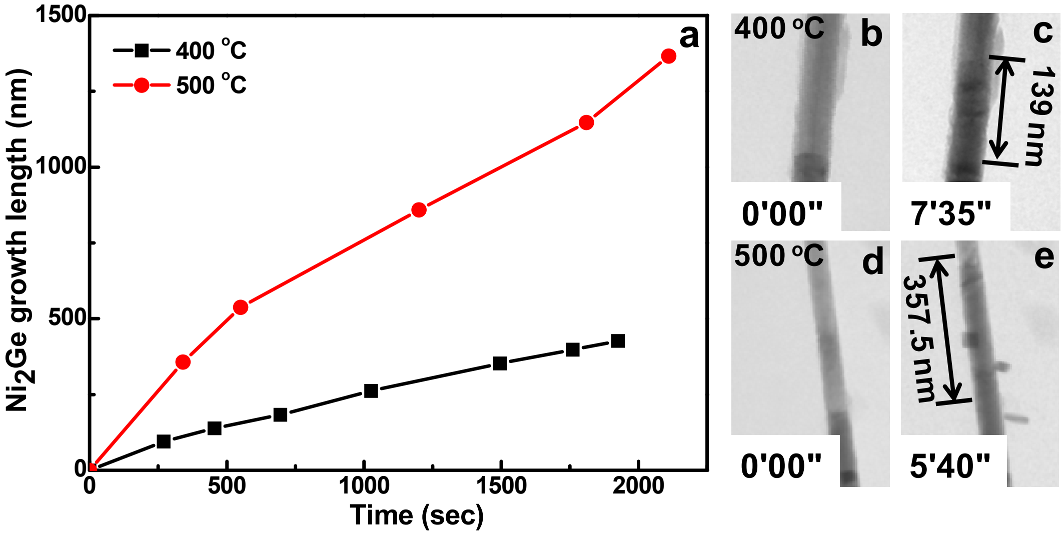

Figure 2-5. Kinetic analysis of the Ni_2Ge epitaxial growth within Ge nanowires. (a) Real-time record of the Ni_2Ge nanowire growth length versus the reaction time at 400 and 500 ^{o}C, illustrating a potentially linear growth rate. (b-c) *In-situ* TEM images of the Ni_2Ge growth within a Ge nanowire at 400 ^{o}C annealing. The arrow indicates a corresponding length of 138.9 nm growth in 7 min 35 sec. (d-e) *In-situ* TEM images of the Ni_2Ge growth within a Ge nanowire at 500 ^{o}C annealing. The arrow indicates a corresponding length of 357.5 nm growth in 5 min 40 sec. (The data also appeared in my publication Ref. [86].[86])

Real-time observation on the Ni_2Ge growth in a Ge nanowire was performed using *in-situ* TEM video, which allows us to obtain lattice-resolved TEM images of the epitaxial interface in progression and thus to estimate the growth velocity. Figure 2-5(a) shows the relation of Ni_2Ge nanowire length versus the reaction time at 400 and 500 ^oC, illustrating a potentially linear growth behavior of Ni_2Ge in the Ge nanowires, while the detailed growth mechanism requires further study. Figures 2-5(b-c) and Figures 2-5(d-e) show the *in-situ* TEM images of the Ni_2Ge nanowire growth at 400 and 500 ^oC, respectively. The growth length of the Ni_2Ge nanowire is 138.9 nm for 455 s at 400 ^oC and 357.5 nm for 340 s at 500 ^oC, respectively. Based on the data collected on more than three nanowires, the extracted growth velocities are about 0.31 nm/s at 400 ^oC and 1.05 nm/s and 500 ^oC, respectively. Using the Arrhenius plot,[71] the activation energy of the Ni_2Ge growth in the Ge nanowire is estimated to be 0.55 ± 0.05 eV/atom.

As mentioned above, due to a large lattice mismatch on the Ni_2Ge/Ge epitaxial interface, the resulting huge strain in the Ni_2Ge/Ge/Ni_2Ge nanowire heterostructure could lead to the segregation of Ni_2Ge nanoparticles on the Ni_2Ge nanowire after a long-time annealing. Figure 2-6(a) shows the TEM image of an as-fabricated Ge nanowire device with EBL-defined Ni pads at room temperature. Figures 2-6(b-d) are a series of *in-situ* TEM images of the Ge nanowire device upon 400 ^oC, 450 ^oC and 500 ^oC sequential annealing, respectively. The time clocks shown at the lower-right corner in each TEM image were captured in the form of hour : minute : second. Volume expansion and segregation to form nanoparticles were clearly observed. Figure 2-6(e) shows a TEM image of another Ge nanowire device annealed at 400 ^oC

for 30 min. The results in Figures 2-6(c-e) clearly demonstrate that, as a result of strain release, Ni_2Ge nanoparticles were formed and segregated on the Ni_2Ge nanowire as Ni diffused along the formed Ni_2Ge nanowire. The suppression of the nanoparticle segregation using oxide confinement will be discussed in Chapter 2.3.

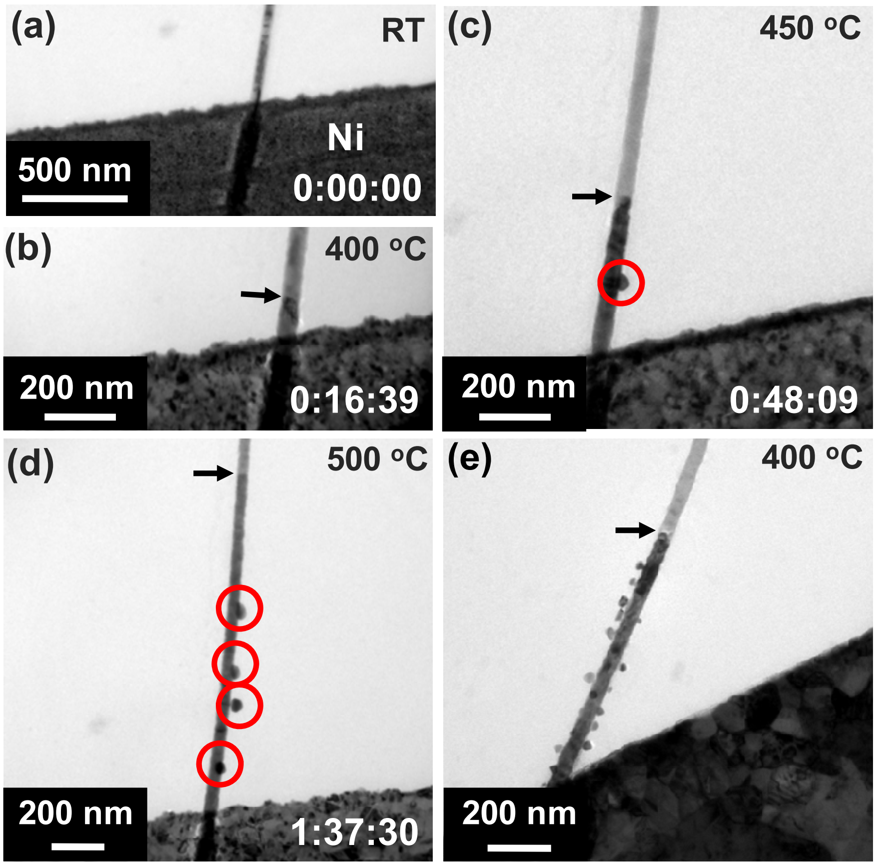

Figure 2-6. Segregation of Ni_2Ge nanoparticles. A series of *in-situ* TEM images at various annealing temperatures: (a) room temperature; (b) 400 °C; (c) 450 °C; (d) 500 °C. The arrows indicate the interface between the formed Ni_2Ge and the Ge nanowire. The red circles indicate Ni_2Ge nanoparticles segregated from the Ni_2Ge nanowire. (e) TEM image of the Ni electrode reacted with a Ge nanowire upon 400 °C annealing

for 30 min. (The data also appeared in my publication Ref. [86].[86])

The formed atomically sharp interface in the Ni_2Ge/Ge/Ni_2Ge nanowire heterostructure can be used to explore the promising applications in nanoscale device, including nanowire FETs. To study the electrical transport property of the Ni_2Ge/Ge/Ni_2Ge nanowire heterostructure, back-gate Ge nanowire FETs were readily fabricated on the SiO_2/Si substrate, in which the high-quality Ni_2Ge segments were used as the source/drain contacts, and the n^+-Si/SiO_2 served as the back-gate stack. The device structure is schematically shown in Figure 2-7(a), and electrical measurements were performed using a home-made probe station connected with a Keithley 4200 semiconductor parameter analyzer. For comparison, Figure 2-7(b) shows the logarithm plot of typical I_{ds}-V_{gs} curves for the Ge nanowire FET at various drain voltages before and after RTA. They both show a *p*-type transistor behavior, although we intended to grow undoped Ge nanowires. This is mainly because of the hole accumulation at the Ge nanowire surface resulted from surface band bending.[84-85] The maximum current measured before RTA at V_{ds} = 0.5 V is about 30 nA, corresponding to a current density of 2.4×10^3 A/cm^2. The current density is relatively small due to a relatively large Schottky barrier at the source/drain contacts before annealing.

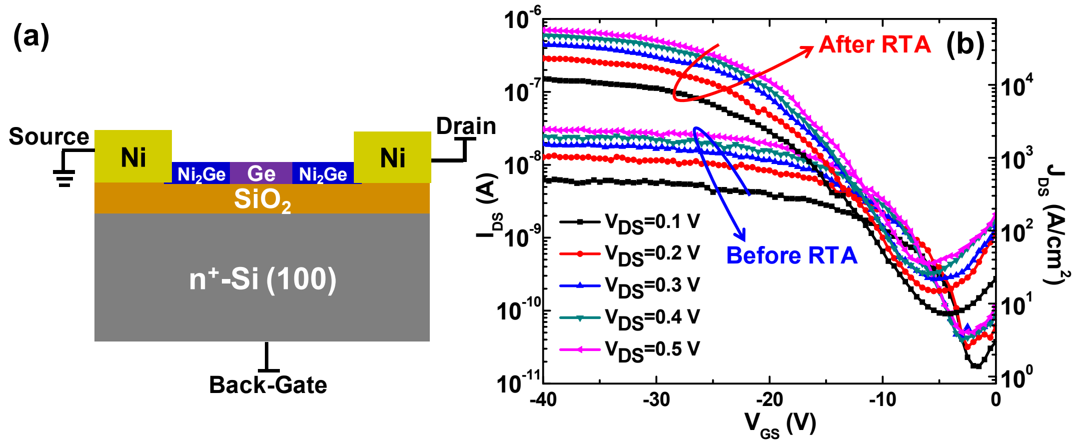

Figure 2-7. Electrical characterization of the Ni_2Ge/Ge/Ni_2Ge nanowire back-gate FETs at 300 K. (a) Schematic of a Ge nanowire back-gate FET. (b) I_{ds}-V_{gs} curves of the back-gate Ge nanowire transistor before and after RTA, both showing a *p*-type FET behavior. The transistor performance was significantly improved after RTA, in which the Ni_2Ge source/drain contacts were formed. (The data also appeared in my publication Ref. [89].[89])

To extract the carrier mobility, we first used the cylinder-on-plate model to estimate the gate capacitance coupling between the Ge nanowire and the back-gate oxide as:[90]

$$C_{ox} = \frac{2\pi\varepsilon_{ox}\varepsilon_0 L}{\cosh^{-1}\left(\dfrac{r+t_{ox}}{r}\right)} \qquad (2\text{-}1),$$

where $\varepsilon_0 = 8.85\times10^{-14}\,F/cm$ is the vacuum dielectric constant, $\varepsilon_{ox} = 3.9$ is the relative dielectric constant for SiO_2, and $r = 20\,nm$ is the radius of the Ge nanowire. The Ge nanowire channel is $L = 3\,\mu m$, and the thickness of the back-gate dielectric is $t_{ox} = 330\,nm$. Given the above parameters, the estimated gate capacitance is $C_{ox} = 1.83 \times 10^{-16}\,F$. The field effect hole mobility can be extracted from the I_{ds}-V_{gs} curves using the transconductance (g_m) at a fixed drain bias V_{ds}:

$$\mu = \frac{g_m L^2}{V_{ds} C_{ox}} \qquad \text{(2-2).}$$

Using the maximum transconductance extracted from the I_{ds}-V_{gs} curves, the hole mobility obtained falls in the range of 3-8 cm^2/Vs. This is consistent with previous reported values (less than 10 cm^2/Vs) for SFLS-synthesized Ge nanowires.[83]

After RTA at 400 ^{o}C for 15 s, however, electrical transport measurements on the Ge nanowire device show much improved transistor characteristics, as shown in Figure 2-7(b). The gate bias was scanned from 0 V to -40 V, the latter of which corresponds to a maximum vertical gate electrical field of 1.21 x10^6 V/cm. The I_{ds}-V_{gs} curves show a *p*-type behavior with an ON/OFF ratio larger than 10^3. The maximum current measured at V_{ds} = 0.5 V is about 0.7 μA corresponding to a current density of 5.6x10^4 A/cm^2, which was more than 20 times larger after annealing, in which the Ni_2Ge contact to the Ge nanowire channel was developed. The maximum transconductance extracted from I_{ds}-V_{gs} curves at drain bias V_{ds} = 0.1 V is 13.3 nS, giving rise to a field-effect hole mobility of 65.2 cm^2/Vs. It should be pointed out that the gate capacitance here was estimated using the cylinder-on-plate model, in which the nanowire was assumed to be completely embedded in the gate dielectric materials. However, in our back-gate transistor, the Ge nanowires are attached onto the SiO_2 surface instead of embedded in the SiO_2. So the calculated gate capacitance using this model is the upper limit. This factor could be taken into account by using an effective dielectric constant of 2.2 for SiO_2 within an analytical model,[91] and then an effective hole mobility is estimated to be 116 cm^2/Vs. Although this mobility is still relatively lower than the reported value from VLS-grown Ge nanowires,[92-93] it still shows about one order of magnitude improvement among SFLS-synthesized Ge nanowires,[83] and this increase may be attributed to the atomically sharp contact of Ni_2Ge to the Ge nanowire.

In summary, a $Ni_2Ge/Ge/Ni_2Ge$ nanowire heterostructure with atomically sharp interface has been formed by thermal intrusion of Ni into a Ge nanowire at a wide temperature range of 400~500 ^oC. Both SEM and TEM studies show a well-controlled diffusion process with a diffusion velocity of 0.31 nm/s at 400 ^oC and 1.05 nm/s at 500 ^oC. Back-gate field effect transistors were fabricated using the formed Ni_2Ge region as source/drain contacts to the Ge nanowire channel. The electrical measurement shows an ON/OFF ratio over 10^3 and a field effect hole mobility of about 65.4 cm^2/Vs, which are superior to the reported values from SFLS-synthesized Ge nanowires.

2.3 Oxide-Confined Formation of Ge Nanowire Heterostructures for High-Performance Transistors

In the previous Chapter 2.2, it is shown that the large lattice mismatch on the Ni_2Ge/Ge epitaxial interface led to a huge strain in the Ni_2Ge/Ge/Ni_2Ge nanowire heterostructure, which resulted in the segregation of Ni_2Ge nanoparticles on the Ni_2Ge nanowire after a long-time annealing. Similarly, the segregation of nanoparticles during annealing was also observed in the Ni-Si nanowire system as reported by Weber, *et al.*[70] For Si, a thin layer of high-quality native oxide is usually formed on the Si nanowire surface, while Ge does not have a stable native oxide. It is observed that the SiO_2 shell has a substantial confinement effect on the nickel silicide growth along with phase transformation in a Si nanowire.[94] For Ge that does not have a stable native oxide, we studied the effect of oxide confinement on the germanide growth in a Ge nanowire using Al_2O_3, which was deposited to cap the Ge nanowire device before the annealing process, as schematically shown in Figures 2-8(a-c). Here VLS-grown Ge nanowires with higher carrier mobility than SFLS-synthesized ones were used in this study in order to further enhance the transistor performance.

Figure 2-8(d) shows the SEM image of an as-fabricated Ge nanowire device showing uniform contrast. Prior to RTA, 20 nm thick Al_2O_3 was deposited on top by atomic layer deposition (ALD) at 250 ^{o}C, as shown in Figure 2-8 (e). It was noticed that the diameter of the Ge nanowire was increased after the Al_2O_3 deposition since ALD provided a conformal coverage. Through extensive experiments, this Al_2O_3

layer was found to efficiently prevent the Ge nanowire from breaking up during the annealing process, and in the meanwhile, to effectively passivate the Ge nanowire surface to minimize dangling bonds,[95-96] and finally to serve as an excellent gate dielectric for top-gate nanowire transistors.

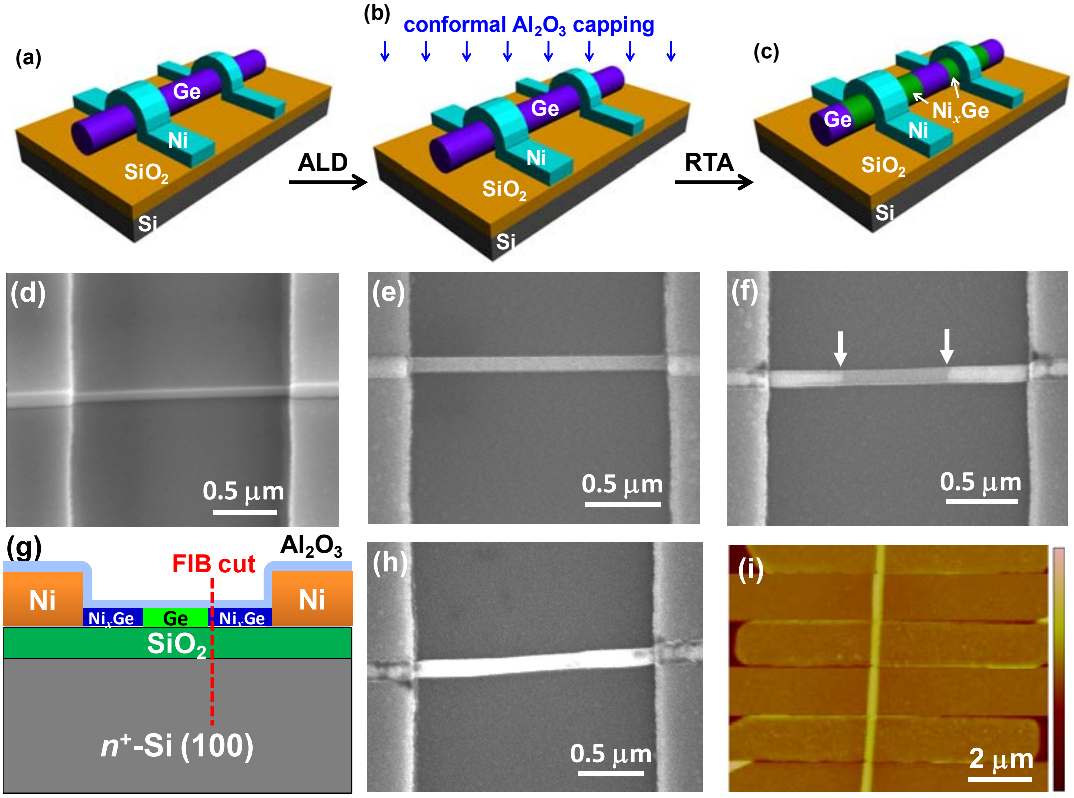

Figure 2-8. Formation of Ni$_x$Ge/Ge/Ni$_x$Ge heterostructure with the Al$_2$O$_3$ confinement. (a-c) Schematic illustration of the ALD-Al$_2$O$_3$ conformal capping on the Ge nanowire device followed by the RTA. (d) SEM image of the as-fabricated Ge nanowire device with EBL-defined Ni electrodes. (e) SEM image of the Ge nanowire device after a conformal capping of 20 nm thick Al$_2$O$_3$. (f) SEM image of the Ni$_x$Ge/Ge/Ni$_x$Ge heterostructure after RTA at 450 ^{o}C for 20 s in which the length of

the Ge region was easily controlled to be several hundred nanometers. The arrows indicate the growth tip of the Ni_xGe nanowire. (g) Schematic illustration showing the formation of $Ni_xGe/Ge/Ni_xGe$ nanowire heterostructure with the Al_2O_3 confinement. The red line indicates the position chosen for FIB to study the cross-sectional structure in Figure 2-9. (h) SEM image of a fully germanided Ge nanowire. (i) AFM image of a Ge nanowire device after annealing, showing no apparent segregated nanoparticles on the surface along the nanowire. (The data also appeared in my publication Ref. [93].[93])

After the Al_2O_3 deposition, the sample was then annealed with RTA in N_2 ambient to allow for the thermal intrusion of Ni into the Ge nanowire and subsequently form the Ni_xGe/Ge heterostructures along the nanowire. Clear diffusion of Ni into the Ge nanowire was observed in both SEM and TEM, and the formed germanide was analyzed in HRTEM, as to be explained further later. Figure 2-8(f) shows the SEM image of the $Ni_xGe/Ge/Ni_xGe$ heterostructures after RTA at 450 ^{o}C for 20 s. Clear contrast was observed between the Ge nanowire and the formed nickel germanide nanowire, which is attributed to the conductivity difference of the two. The remaining Ge nanowire region was easily controlled down to several hundred nanometers and it can be further reduced to sub-50 nm.[74,86] Figure 2-8(g) schematically illustrates the formation of $Ni_xGe/Ge/Ni_xGe$ nanowire heterostructure with the Al_2O_3 confinement. The red line indicates the position where the device was cut with focused-ion beam (FIB) to study the cross-sectional structure, as to be explained in Figure 2-9. Proper control of annealing time can convert the whole Ge nanowire to a fully germanide nanowire, as shown in Figure 2-8(h). Furthermore, atomic force microscopy (AFM) scanning showed uniform contrast without segregation of nanoparticles on the surface along the Ni_xGe/Ge heterostructure nanowire after annealing (see Figure 2-8(i)), as further supported by TEM later.

Figure 2-9(a) shows the low-magnification cross-sectional TEM image of the Ni_xGe/Ge nanowire heterostructure that was cut with FIB from the nanowire FET device, as shown in Figure 2-8(g). The $Ni_xGe/Ge/Ni_xGe$ nanowire device capped with 20 nm Al_2O_3 was fabricated on a SiO_2/Si wafer. When preparing the cross-section of Ni_xGe for TEM analysis using FIB, we chose the position as close as to the Ni_xGe/Ge interface. It is noted that in the cross-sectional view, there were some nanoparticles segregated on the SiO_2 surface from the bottom of the formed nickel germanide, which was not confined by the Al_2O_3 capping layer. This result also explains the fact that we did not observe nanoparticles on the Al_2O_3 capped surface from the AFM scanning. Figure 2-9(b) shows the lattice-resolved HRTEM image of interface between the formed Ni_xGe nanowire and the segregated Ni_xGe nanoparticle, which were both identified to be NiGe from the FFT pattern shown in the inset of Figure 2-9 (b). NiGe has an orthorhombic lattice structure with lattice constants $a = 0.538$ nm, $b = 0.342$ nm, and $c = 0.581$ nm (space group 62). The EDS line-scan results in Figures 2-9(c-e) also proved that the Ni/Ge concentration ratio is about 1:1 in the formed nickel germanide as well as in the segregated nanoparticles (the EDS line profile is not shown). In addition, the EDS-line scan profiles of elements Al and O from the

Al_2O_3 capping layer are shown in Figures 2-9(f) and 2-9(g), respectively.

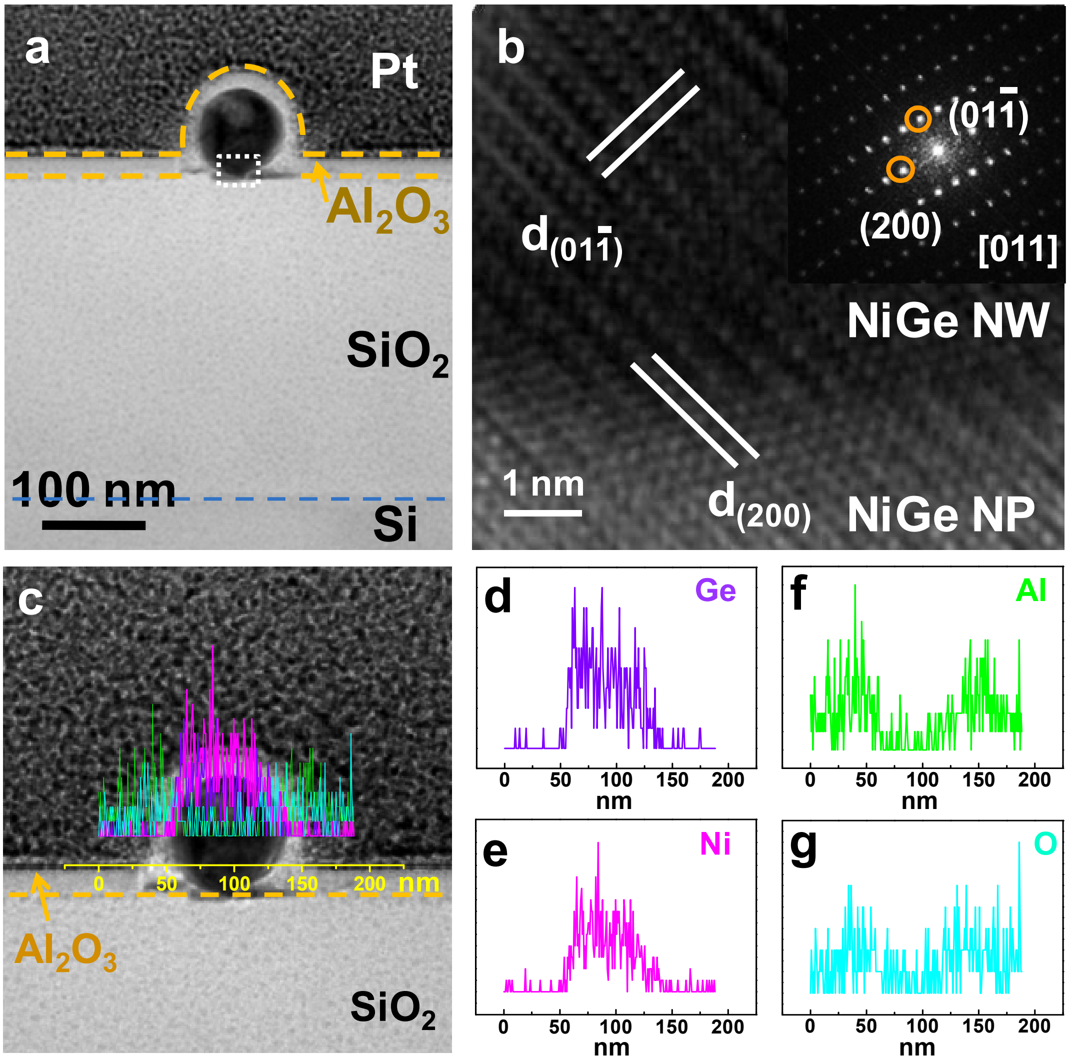

Figure 2-9. Cross-sectional TEM study of a Ni-Ge nanowire device on a SiO_2/Si substrate cut with FIB. (a) Low-magnification cross-sectional TEM image of the NiGe region. The 20 nm thick Al_2O_3 film provides a conformal capping on the device surface and germanide nanoparticles are clearly observed as they segregated underneath the nanowire, the region that is not covered by Al_2O_3. (b) Lattice-resolved

HRTEM image of the interface between the formed NiGe nanowire (NW) and the segregated NiGe nanoparticle (NP), as indicated by the white rectangle in Figure 2-9(a). The inset shows the corresponding FFT pattern. The labeled lattice spacings for NiGe are: $d_{(01\text{-}1)} = 0.295$ nm and $d_{(200)} = 0.269$ nm. (c) Cross-sectional TEM image with the line-scan profiles of Ge, Ni, Al and O atoms. (d-g) The individual line-scan profile of Ge, Ni, Al and O atoms, respectively, The Ni/Ge ratio is about 1:1. (The data also appeared in my publication Ref. [93].[93])

To study the epitaxial relationships between Ni_xGe and Ge, the Al_2O_3-coated Ni-Ge nanowire devices were prepared on the TEM grids were then annealed both *in-situ* and *ex-situ* (in RTA). Figure 2-10(a) shows the low-magnification TEM image of the Ni-Ge nanowire device capped with 10 nm Al_2O_3 after annealing at 450 ^oC for 30 s. The enlarged TEM image in Figure 2-10(b) shows that there are two interfaces in the Ni_xGe/Ge nanowire heterostructure. Figure 2-10(c) shows the EDS line-scan profile from the nanowire heterostructure. The line profile indicates two germanide phases in the formed Ni_xGe region, which corresponds to the two interfaces observed in the Ni_xGe/Ge heterostructure. The Ni/Ge ratio is about 1:1 in the small germanide region close to the Ni_xGe/Ge interface, suggesting the formation of NiGe. This result is consistent with the line-scan profile in Figures 2-9(d) and 2-9(e). The length of the NiGe region can range from tens of nanometers to hundreds of nanometers in our experiments. On the other hand, the Ni/Ge ratio is about 2:1 in the other germanide region close to the Ni pad on the left, implying that the phase is Ni_2Ge. It is also worth noting that the almost constant concentration of Ge along the heterostructure suggests Ni is the dominant diffusion species in this system.[87]

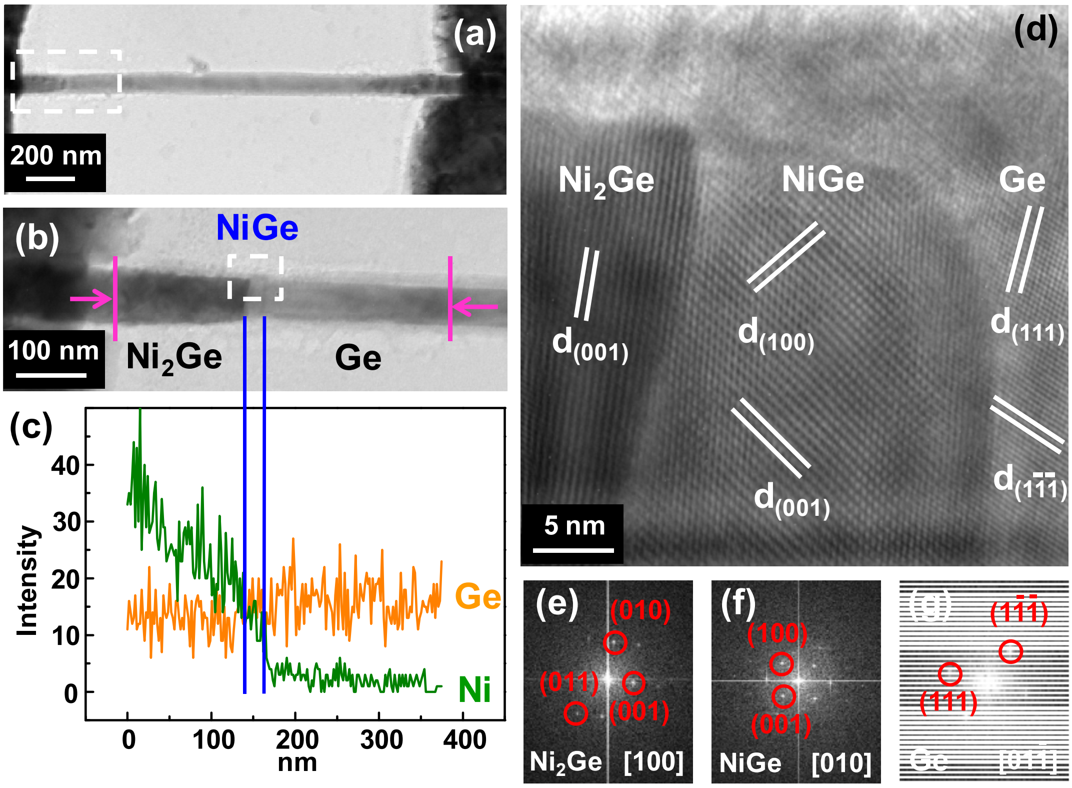

Figure 2-10. Plane-view TEM images of Ni-Ge nanowire devices on a TEM grid with a 50 nm thick Si_3N_4 window. (a) Low-magnification TEM image of a Ge nanowire reacted with 120 nm thick Ni pads upon 450 ^{o}C RTA for 30 s. (b) Enlarged TEM image from the white rectangle in (a). These regions with different contrasts and compositions are labeled. (c) Corresponding EDS line-scan profiles of Ge and Ni across the region between two red lines in (b). (d) Lattice-resolved TEM image of the formed Ni_xGe/Ge nanowire heterostructure from the white rectangle in (b). The labeled lattice spacings are: $d_{(001)} = 0.5036$ nm and $d_{(010)} = 0.3948$ nm for Ni_2Ge; $d_{(100)}$

= 0.538 nm and $d_{(001)}$ = 0.5811 nm for NiGe; $d_{(111)}$ = 0.3265 nm and $d_{(1\text{-}1\text{-}1)}$ = 0.3265 nm for Ge. (e)-(g) are the FFT patterns taken from the Ni_2Ge, NiGe and Ge regions in (d), respectively. (The data also appeared in my publication Ref. [93].[93])

Figure 2-10(d) shows the lattice-resolved HRTEM image of the Ni_xGe/Ge heterostructure, clearly exhibiting two interfaces. The FFT patterns at the Ni_2Ge, NiGe and Ge regions are shown in Figures 2-10(e-g), which help further confirm the germanide phases. The crystallographic epitaxial relationships between the Ge/NiGe interface were determined to be: Ge$[01\bar{1}]$//NiGe[010] and Ge$(1\bar{1}\bar{1})$//NiGe(001); while those for the Ni_2Ge/NiGe interface were: Ni_2Ge [100]//NiGe[010] and Ni_2Ge(011)//NiGe(001). In contrast, the epitaxial relationships in our previously reported Ni_2Ge/Ge/Ni_2Ge nanowire heterostructure formed without oxide confinement during annealing were found to be: Ge$[01\bar{1}]$//$Ni_2Ge$$[0\bar{1}1]$ and Ge$(1\bar{1}\bar{1})$//Ni_2Ge(100).[86] Therefore, the Al_2O_3 capping layer in the present study plays an important role in confining the growth of germanides and also promoting the formation of NiGe to maintain the epitaxial relationships between Ni_2Ge and Ge.

For comparison, Figure 2-11 schematically illustrates the epitaxial relationships of the Ni_2Ge/Ge interface in the previous Ni_2Ge/Ge/Ni_2Ge nanowire heterostructure (see Chapter 2.2), and the NiGe/Ge interface in the Ni_2Ge/NiGe/Ge/NiGe/Ni_2Ge nanowire heterostructure. According to the epitaxial relationships in both cases, the nanowire growth direction (along the Ge [111] direction) is not perpendicular to the epitaxial planes (parallel to the Ge $(1\bar{1}\bar{1})$ plane). This "twisted" growth mode of nanowires is substantially different from that in the typical epitaxial growth of thin films, in which the growth direction is usually perpendicular to the epitaxial planes.[86] The presence of the oxide capping may alter the energy of the growth and thus change the twisted angle. Furthermore, it suggests that the twisting in nanowires may be used to accommodate substantially large lattice mismatches. One possible explanation would be that the epitaxial growth in the Si(Ge) nanowire happens on a very small area, *i.e.*, the cross-section of the Si(Ge) nanowire, so that the energy required to form dislocations could be large. This unique growth mode may be attributed to the fact in minimizing the total system energy in the presence of a large lattice mismatch in the interface. For comparison, in the thin film epitaxy case, the epitaxial area is very large, *i.e.*, typically over the entire substrate. Therefore, the accumulated strain is easily relaxed, which leads to the formation of noticeable defects such as threading dislocations. Further microscopic studies in simulation and experiment as well as growth dynamic analysis are required to understand the growth kinetics for this unique growth mode in one-dimensional systems.

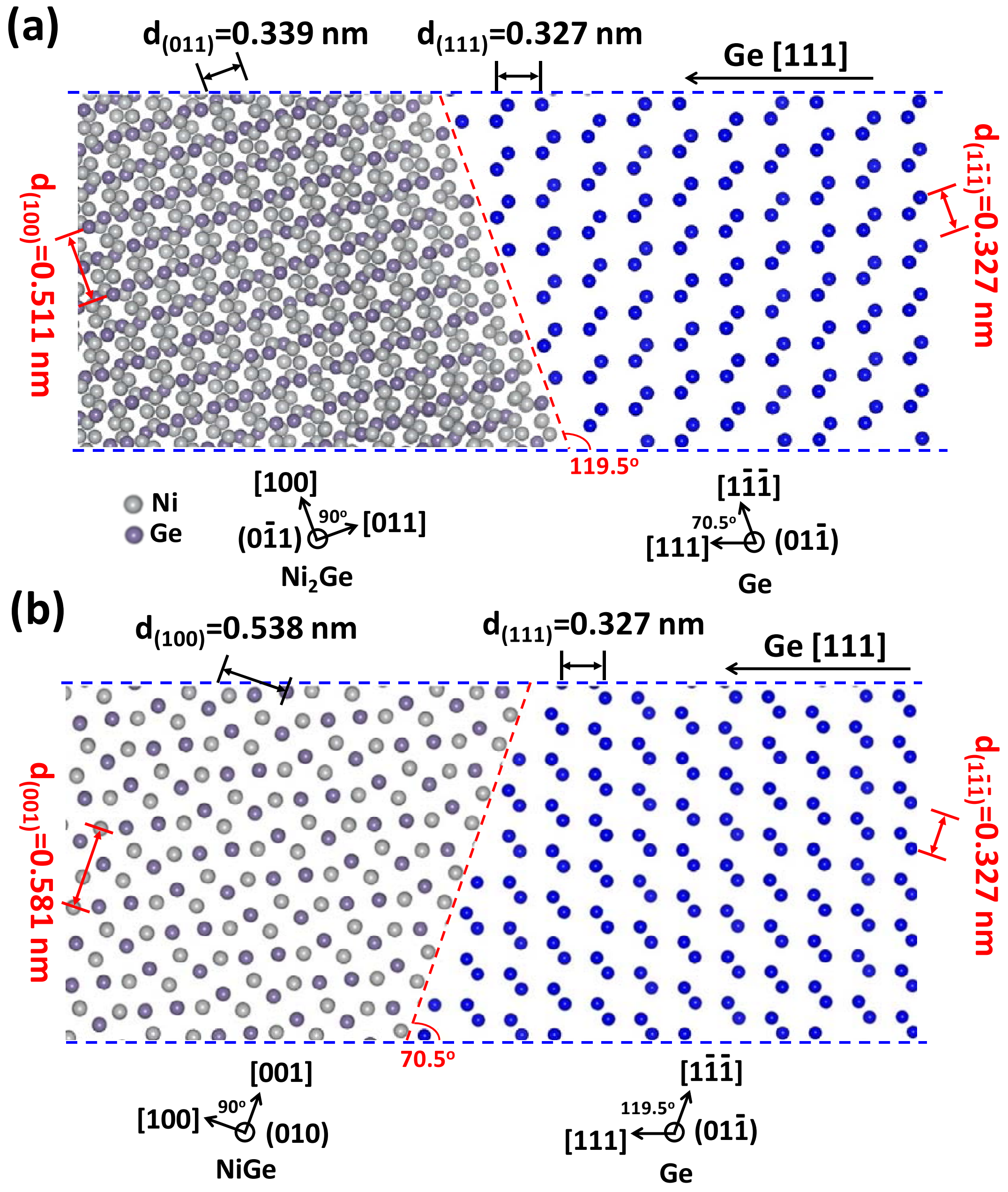

Figure 2-11. Schematic illustration of the epitaxial relationships of (a) the Ni$_2$Ge/Ge interface in the Ni$_2$Ge/Ge/Ni$_2$Ge nanowire heterostructure, and (b) the NiGe/Ge interface in the Ni$_2$Ge/NiGe/Ge/NiGe/Ni$_2$Ge nanowire heterostructure, respectively. Both of them show "twisted" but different growth modes. The grey and purple balls

represent the Ni and Ge atoms in the Ni_xGe lattice, respectively, while the blue one represents the Ge atom in the Ge lattice. Both Ni_2Ge and NiGe have orthorhombic crystal structure, while Ge has diamond cubic crystal structure. (The data also appeared in my publication Ref. [89].[89])

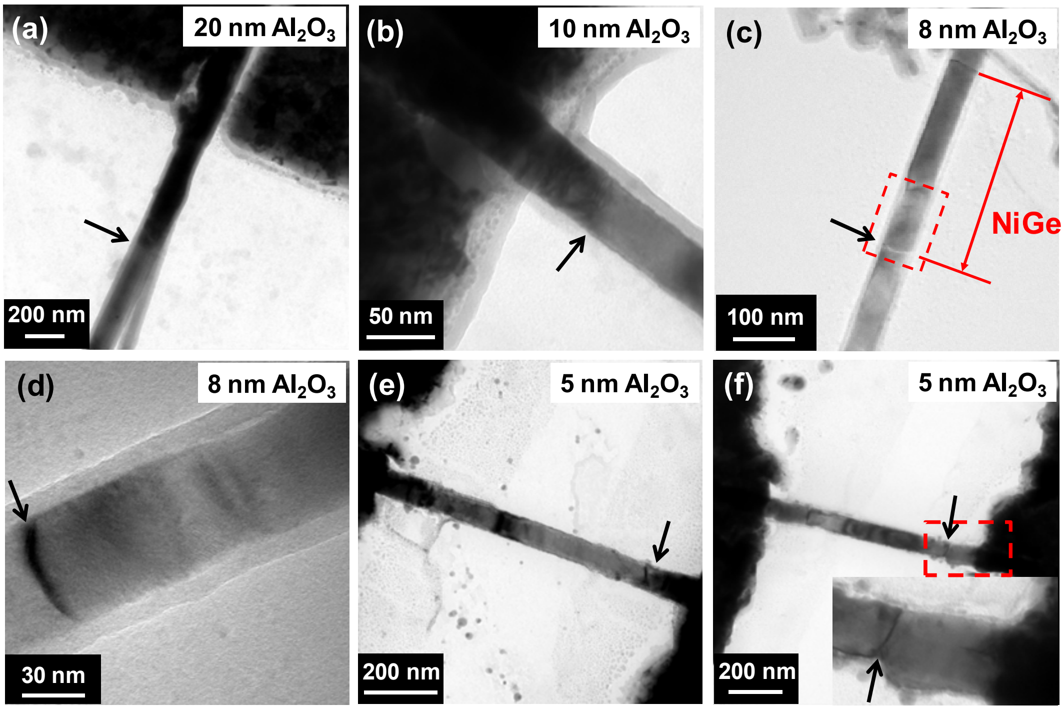

Figure 2-12. TEM images of Ni-Ge nanowire devices with various confining oxide thicknesses: (a) 20 nm; (b) 10 nm; (c) 8 nm; (d) 8 nm (enlarged TEM image of the region indicated by the red rectangle in (c)); (e) 5 nm (a Ni-Ge nanowire device with 5 nm confining oxide showing no apparent volume expansion upon annealing); (f) 5 nm (another Ni-Ge nanowire device with 5 nm confining oxide showing clear volume expansion upon annealing. The inset shows the enlarged TEM image of the region indicated by the red rectangle). The arrows indicated the Ni_xGe/Ge interfaces. (The

data also appeared in my publication Ref. [93].[93])

In addition, various Al_2O_3 thicknesses ranging from 5 to 20 nm were also studied to investigate the lower limit of the confining oxide thickness. Figure 2-12 shows the TEM images with 20 nm, 10 nm, 8 nm and 5 nm Al_2O_3 upon 450 ^oC annealing. The NiGe phase was still preserved when the confining oxide was scaled down to about 8 nm, where no segregation of NiGe nanoparticles was observed upon annealing, as shown in Figures 2-12(a-d). When the confining oxide was continuously scaled down to about 5 nm, there was clear volume expansion during the formation of germanide in some devices (see the inset of Figure 2-12(f)), although no apparent segregation of nanoparticles was observed. Therefore, it is believed that the lower limit of the confining oxide is about 5 nm.

Similar to the previous work in the $Ni_2Ge/Ge/Ni_2Ge$ nanowire heterostructure discussed in Chapter 2.2,[86] the $Ni_2Ge/NiGe/Ge/NiGe/Ni_2Ge$ nanowire heterostructure with atomically sharp interfaces can be also used to explore the promising applications in nanoscale devices, such as nanowire FETs.[69-70,73,86,92] To study the electrical transport property of the $Ni_2Ge/NiGe/Ge/NiGe/Ni_2Ge$ nanowire heterostucture, back-gated FETs were fabricated on the SiO_2/Si substrate using the degenerately doped Si as the back-gate, which provided an efficient and convenient approach to evaluate the device performance, such as the ON/OFF ratio and carrier mobilities. In order to study the effect of Al_2O_3 capping and RTA, I_{ds}-V_{gs} curves were recorded before Al_2O_3 deposition, after Al_2O_3 deposition at 250 ^oC, and after RTA at

450 °C, as shown in Figure 2-13(a). Typically as-fabricated devices show a *p*-type transistor behavior with an ON/OFF ratio in the range of 10-10^2 before Al_2O_3 deposition. The typical on current is about 10-100 nA at a drain bias of $V_{ds} = 0.1$ V. The Ni contact to Ge nanowire is improved after Al_2O_3 deposition and the ON/OFF ratio is enhanced to above 10^3. Further RTA at 450 °C for 20 s can significantly raise the ON/OFF ratio up to > 10^5 owing to the formation of single-crystalline NiGe in which a perfect contact to the Ge channel is developed with reduced contact resistance. Also, the subthreshold swing (SS) is calculated to decrease from 4.49 V/dec to 1.74 V/dec after RTA at 450 °C for our back-gate Ge nanowire FETs. To extract the field-effect hole mobilities before and after RTA, we first used Equation (2-1) to estimate the gate capacitance is $C_{ox} = 1.36 \times 10^{-16} F$ and $C_{ox} = 4.79 \times 10^{-17} F$, before and after RTA, respectively, given that $r = 35\, nm$ is the radius of the Ge nanowire and $t_{ox} = 330\, nm$ is the thickness of the back-gate dielectric. Here the Ge nanowire channel before and after RTA has a length of $L = 1.9\ \mu m$ and $L = 0.67\ \mu m$, respectively. The field-effect hole mobility can be extracted using Equation (2-2). Using the maximum transconductance extracted from I_{ds}-V_g curves, the hole mobility is calculated to be 210 cm^2/V s and 94.2 cm^2/V s, before and after RTA, respectively. The improvement on the hole mobility is also attributed to the improvement of source/drain contact after annealing. In addition, compared with the $Ni_2Ge/Ge/Ni_2Ge$ nanowire transistor built on SFLS-synthesized Ge nanowires in Chapter 2.2,[86] the $Ni_2Ge/NiGe/Ge/NiGe/Ni_2Ge$ nanowire transistor in the present study shows a better performance, because VLS-grown Ge nanowires with higher carrier mobility and

quality are used here in this study.

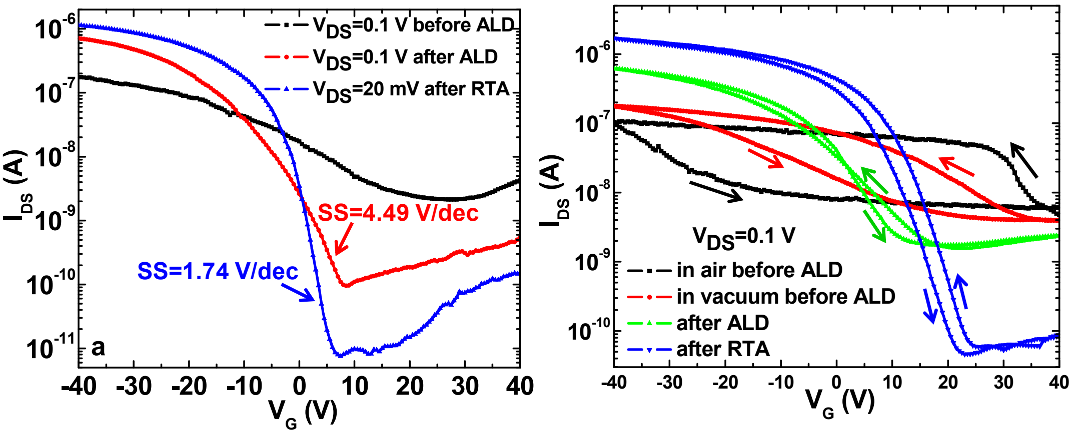

Figure 2-13. Electrical characterization on the effects of ALD-Al_2O_3 deposition and RTA. (a) I_{ds}-V_{gs} curves of a back-gate Ge nanowire transistor recorded before ALD, after ALD at 250 °C, and after RTA at 450 °C, all showing a *p*-type transistor behavior. The back-gate transistor after RTA at 450 °C for 20 s shows an ON/OFF ratio over 10^5 and an extracted field-effect hole mobility of 210 cm^2/Vs. (b) Dual sweepings of the gate bias V_g between +40 V to -40 V showing different sizes of hysteresis under various conditions. The arrows indicate the sweeping directions, and the hysteresis indicates electron trapping at the interface. The hysteresis was significantly reduced after the Al_2O_3 passivation. Small hysteresis was still observed after RTA, which may be attributed to the charge trapping on the Ge surface between the Ge nanowire channel and the back-gate dielectric, the region that is not covered by the Al_2O_3 capping layer. (The data also appeared in my publication Ref. [93].[93])

Dual sweepings of gate bias in I_{ds}-V_g curves were performed to study the impact of the Al_2O_3 capping layer on passivating the Ge nanowire surface. Figure 2-13(b) shows the I_{ds}-V_{gs} curves recorded under various conditions: before Al_2O_3 deposition (both in air and in vacuum), after Al_2O_3 deposition at 250 °C, and after RTA at 450 °C. The gate bias was swept from +40 V to -40 V then back to +40 V in steps of 0.5 V at a fixed drain bias of V_{ds} = 0.1 V. The I_{ds}-V_{gs} curve measured in air before annealing shows the biggest hysteresis from electron trapping, which is mainly due to the absorption of molecules from the ambient and the charge trapping on the Ge surface.[84,97] The measured reduced hysteresis in a vacuum (less than 10^{-5} Torr), however, rules out the contribution from the ambient. Furthermore, the hysteresis was significantly reduced after the Al_2O_3 deposition, which unambiguously demonstrates the passivation effect of the Al_2O_3 layer on the Ge nanowire surface.[98] The small hysteresis present after Al_2O_3 passivation and after RTA, however, may arise from the charge trapping on the Ge surface between the Ge nanowire channel and the back-gate dielectric, the region that is not covered by the Al_2O_3 capping layer.

Although we intended to grow undoped Ge nanowires, their performance of nanowire transistors usually shows a *p*-type behavior in nature, which is mainly due to the surface state-induced Fermi level pinning that results in hole accumulation.[84-85] Temperature-dependent *I-V* measurements were performed to extract the Schottky barrier height of the formed NiGe contact to the Ge nanowire. Figure 2-14(a) shows the two-terminal *I-V* measurements at various temperatures after RTA at 450 °C for 20 s, illustrating a back-to-back Schottky diode behavior. Figure 2-14(b) shows the Arrhenius plot for the Ni_2Ge/NiGe/Ge/NiGe/Ni_2Ge nanowire heterostructure at various biases between 235 and 305 K.[74,92] The linear fitting of ln(I/T^2) versus $1/T$ gave to a Schottky barrier height of 0.11 eV. The consistent behaviors under positive and negative biases demonstrate symmetric source/drain contacts. Measurements over several batches gave a barrier height in the range of 0.11-0.13 eV. Figure 2-14(c) shows the corresponding band diagram with *p*-type Ge nanowire. The effect of the atomically clean interface on the Fermi-level pinning in germanide/Ge nanowire contacts will be discussed in Chapter 2.5.

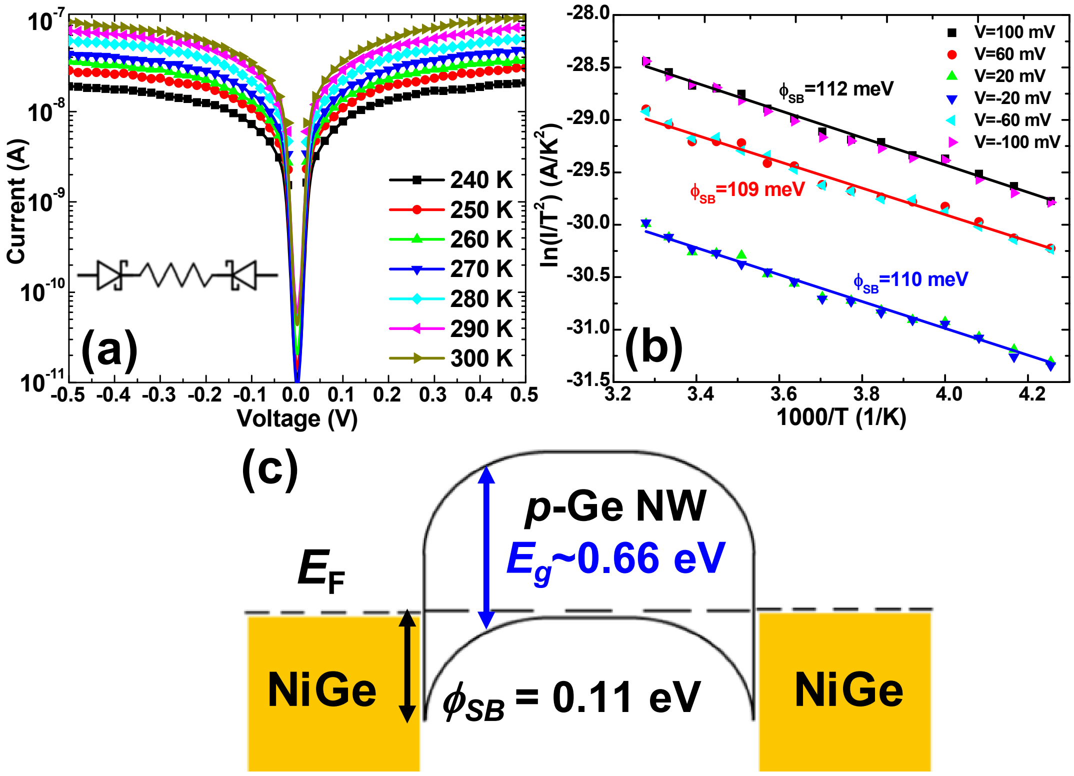

Figure 2-14. Temperature-dependent *I-V* measurements of the $Ni_2Ge/NiGe/Ge/NiGe/Ni_2Ge$ nanowire heterostructure. (a) *I-V* measurements of the $Ni_2Ge/NiGe/Ge/NiGe/Ni_2Ge$ nanowire heterostructure at temperatures ranging from

240 K to 300 K. The inset shows the corresponding circuit symbol. (b) Arrhenius plot for the Ni_2Ge/NiGe/Ge/NiGe/Ni_2Ge nanowire heterostructure at various biases between 235 and 305 K. The extracted Schottky barrier height of NiGe to Ge is about 0.11 eV. (c) The corresponding band structure diagram of the NiGe/Ge contact. (The data also appeared in my publication Ref. [93].[93])

The characteristics of the back-gate Ge nanowire FETs were shown in Figure 2-15. Figure 2-15(a) shows the SEM image of a back-gate FET with multiple Ni probes fabricated on a SiO_2/Si substrate. Clear diffusion of Ni into the Ge nanowire was observed for each Ni electrode, and the process has a high yield after RTA with an Al_2O_3 capping. Figure 2-15(b) shows the typical I_{ds}-V_g curves of a back-gate Ge nanowire FET, and the inset gives a logarithmic plot of drain current I_{ds} versus gate voltage V_g relations at various drain voltages. The maximum transconductance is obtained to be about 0.168 μS at V_{ds} = 0.1 V, which gives rise to a normalized transconductance of 2.4 μS/μm, assuming the effective channel length is equal to the nanowire diameter (70 nm).[73] The extracted hole mobility in our experiments is typically in the range of 150-210 cm^2/Vs. Apparent transition from electron-conduction (V_{gs} >10 V) to hole-conduction (V_{gs} <10 V) was observed. The subthreshold swing is extracted to be 19.1 V/dec and 2.33 V/dec for electron-conduction and hole-conduction, respectively. The smaller conduction current and the larger subthreshold swing for electron-conduction region is due to a larger Schottky barrier for electrons (~0.55 eV) compared with that for holes (~0.11 eV). Figures 2-

15(c) and 2-15(d) show the I_{ds}-V_{ds} curves for the hole-conduction and electron-conduction, respectively. The different characteristics further support NiGe as an Ohmic contact to *p*-type Ge (linear I_{ds}-V_{ds} characteristics at small V_{ds}) and a Schottky contact to *n*-type Ge (highly nonlinear I_{ds}-V_{ds} characteristics). Saturation behavior in the I_{ds}-V_{ds} characteristics for the hole-conduction can be observed at large V_{ds}.

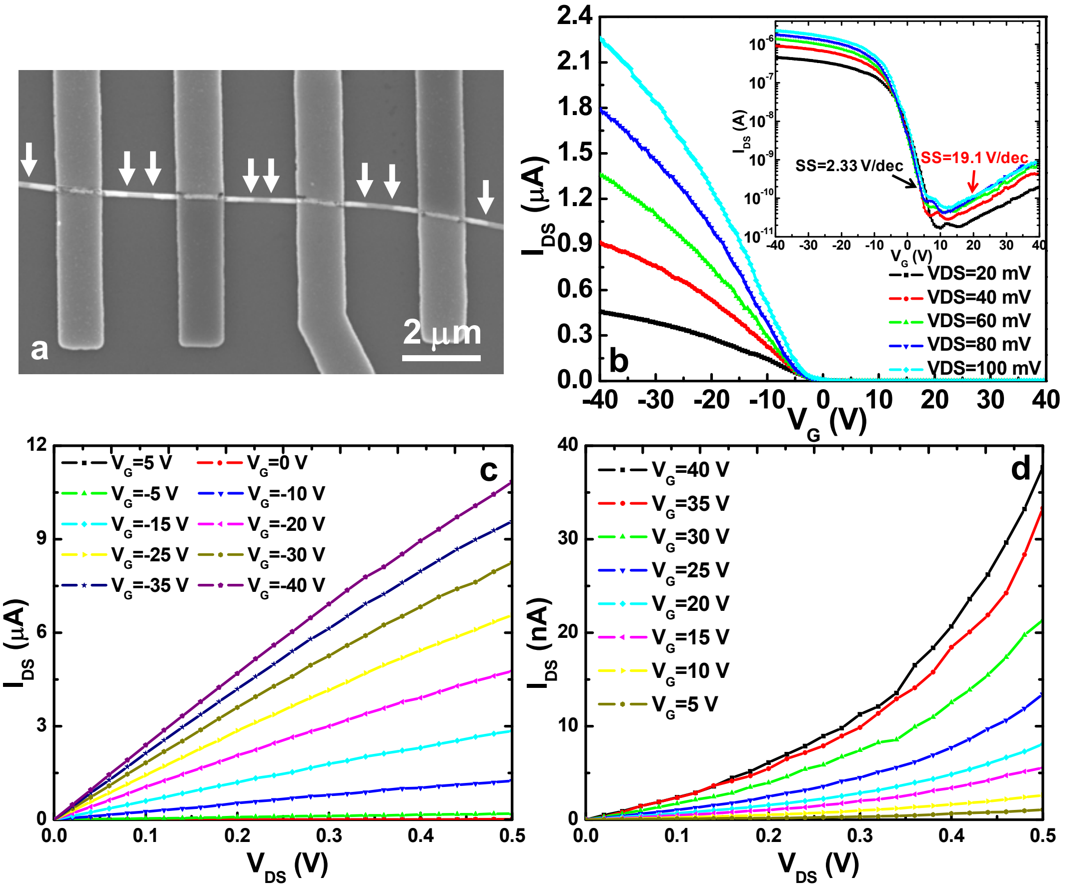

Figure 2-15. Back-gate Ge nanowire FETs characterization. (a) SEM image of a back-gate FET with multiple Ni probes. The arrows highlight the growth tip of the Ni_2Ge/NiGe nanowire. (b) I_{ds}-V_{gs} curves of the back-gate Ge nanowire transistor after

RTA at 450 °C for 20 s, showing an electron-conduction part ($V_{gs} > 10$ V) and a hole-conduction part ($V_{gs} < 10$ V) at different gate biases. (c) I_{ds}-V_{ds} curves of the hole-conduction part, showing good ohmic contacts of the source and drain. (d) I_{ds}-V_{ds} curves of the electron-conduction part, showing a Schottky behavior. (The data also appeared in my publication Ref. [93].[93])

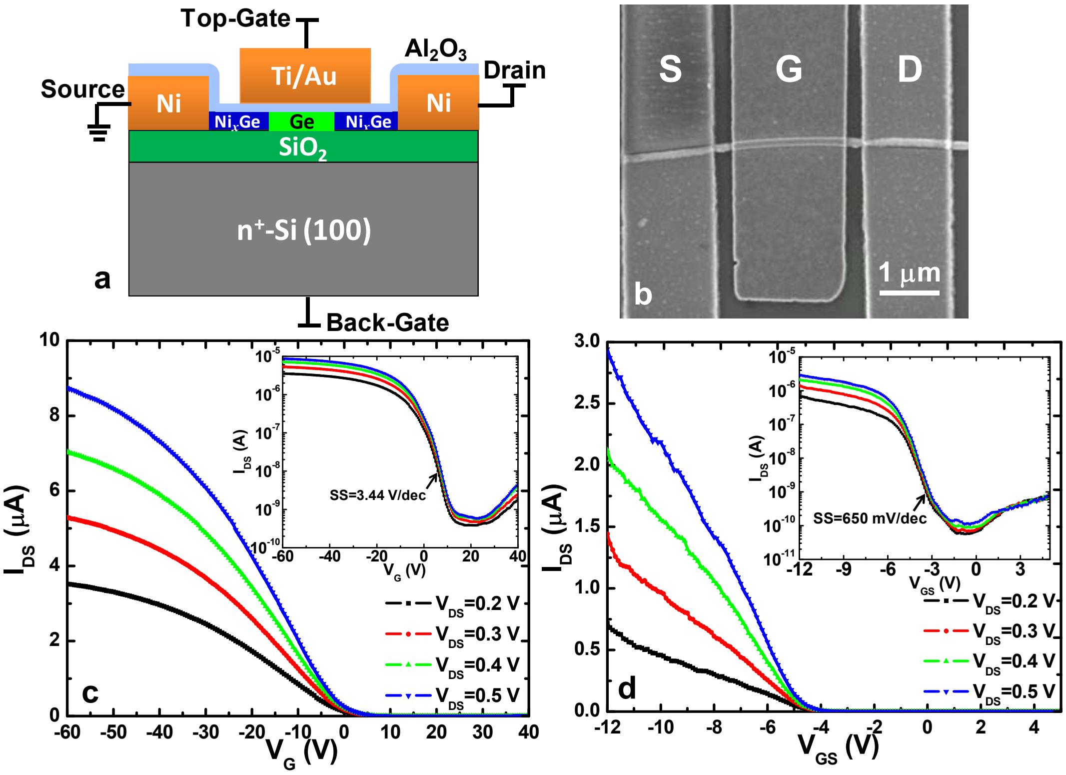

Figure 2-16. Comparison of back-gate and top-gate Ge nanowire FETs. (a) Schematic illustration of a Ge nanowire FET with both back-gate contact and top-gate contacts. (b) SEM image of a top-gate FET device. (c) I_{ds}-V_g curves of the back-gate Ge nanowire transistor with a poor subthreshold swing of 3.44 V/dec because of the thick back-gate dielectric. The inset shows the logarithm plot of I_{ds}-V_{gs} curves. (d) I_{ds}-

V_{gs} curves of the top-gate Ge nanowire transistor, showing an improved subthreshold swing of 650 mV/dec. The inset shows the logarithm plot of I_{ds}-V_g curves. (The data also appeared in my publication Ref. [93].[93])

As mentioned before, the Al_2O_3 capping layer can also be used as a gate dielectric to build top-gate transistors on the formed Ni_2Ge/NiGe/Ge/NiGe/Ni_2Ge nanowire heterostructure. Figure 2-16(a) schematically illustrates the device structure of a Ge nanowire FET with both back-gate and top-gate contacts. Figure 2-16(b) shows the SEM image of a top-gate transistor, in which the Ti/Au gate metal was deposited by e-beam evaporation. In order to reduce the gate leakage current through the overlap between the gate and the formed Ni_xGe region, another layer of Al_2O_3 was deposited with ALD on top of the Al_2O_3-capped Ge nanowire device before the gate metal deposition. The total thickness of Al_2O_3 layer is 23 nm, and its relative dielectric constant is extracted to be 7.5 from the calibrating capacitance-voltage (C-V) measurements. Figure 2-16(c) shows the I_{ds}-V_g curves of a back-gate Ge nanowire transistor, giving a subthreshold swing of 3.44 V/dec and a maximum normalized transconductance of 1.39 μS/μm at V_{ds} = 0.2 V. In comparison, Figure 2-16(d) shows the I_{ds}-V_g curves of the top-gate Ge nanowire transistor fabricated after passivation, showing a subthreshold swing of 650 mV/dec and a maximum transconductance of 3.27 μS/μm at V_{ds} = 0.2 V. Also, the typical field-effect hole mobility in the top-gated transistors falls in the range of 100-150 cm^2/Vs. The improvement in the subthreshold swing and transconductance can be attributed to the increase in the gate capacitance and hence the enhancement of gate control over the nanowire channel in the top-gated device, while the degradation of hole mobility is due to additional scatterings from the top-gate dielectric/Ge nanowire channel interface.[99-100]

In summary, a $Ni_2Ge/NiGe/Ge/NiGe/Ni_2Ge$ nanowire heterostructure with atomically sharp interfaces has been formed by the thermal intrusion of Ni into a Ge nanowire at 450 °C. A segment of NiGe was formed between Ni_2Ge and Ge with an Al_2O_3 capping during annealing. The Al_2O_3 capping provided appreciable confinement during the growth of germanide and changes its composition to maintain the epitaxial relationships. In addition, the Al_2O_3 layer also helped to prevent nanowire breaking and passivate the Ge nanowire surface. SEM and TEM studies showed a well-controlled diffusion process, in which the remaining Ge region was easily controlled down to hundreds of nanometers by RTA. Back-gate FETs were fabricated using the formed $Ni_2Ge/NiGe$ heterostructure as source/drain contacts to the Ge nanowire channel. The electrical measurement showed a high-performance *p*-type behavior with an ON/OFF ratio over 10^5, a maximum transconductance of 2.4 μS/μm and a field-effect hole mobility of 210 cm^2/Vs. The Schottky barrier height extracted from temperature-dependent *I-V* measurements was about 0.11 eV, which affirmed that NiGe was a good Ohmic contact to *p*-type Ge nanowire. Moreover, our top-gate Ge nanowire transistors using the Al_2O_3 layer as the gate dielectric further improved the subthreshold swing and transconductance.

2.4 Ferromagnetic Germanide in Ge Nanowire Transistors for Spintronics Application

As introduced in Chapter 1, efficient spin injection into semiconductors and effective manipulation of spin in semiconductors are considered to be the two major challenges in realizing most practical spintronic devices.[2,5-6] For the spin manipulation, DMS provides an interesting material system with effective control of the magnetic phase transition using an external electric field.[101] Among all the DMS candidates, the Mn-Ge system has attracted extensive research because of its potential to reach a high Curie temperature above 400 K.[102] Epitaxially-grown Mn-doped Ge thin films, however, usually suffered from clusters or amorphous ferromagnetic precipitates.[103-104] Inspiringly, single-crystalline Mn-doped Ge quantum dots have been reported to exhibit electric-field controlled ferromagnetism up to 300 K.[105-106] Meanwhile, electrical spin injection into bulk Ge using the epitaxial Fe/MgO/Ge tunnel junction has been demonstrated up to 225 K in non-local spin-valve measurements (although a relatively low spin injection efficiency of 0.23% at $T = 4$ K was reported),[21] and further at room temperature with three-terminal Hanle measurements (different from the nonlocal ones as discussed in Chapter 1.2).[35,107] Moreover, lateral spin injection into Ge nanowires was also reported to manifest a spin diffusion length of more than 100 μm at low temperature,[56] and the significant enhancement in the spin diffusion length could be attributed to the effective suppression of both Elliot-Yafet and D'yakonov-Perel' spin relaxation mechanisms due to the strong quantum confinements in the one-dimensional (1D) Ge nanowire channel.[108]

It is necessary to point out that the interface between the ferromagnetic metal and the semiconductor channel could play a critical role in the spin injection and detection.[27,36] This is of particular importance for Ge due to its high density of interface states, which could result in strong Fermi-level pinning close to the Ge valence band in conventional metal-Ge contacts.[109] It is also worth noting that the conductivity mismatch is another fundamental obstacle to realize efficient spin injection into semiconductor due to the large conductivity difference between metal and semiconductor.[110] In solving this issue, high-quality epitaxial Fe/MgO/Ge tunnel junction grown by MBE has been widely used in the successful demonstration of spin injection into Ge.[21,35,111] Besides the tunneling contact, Schottky contact has been theoretically shown[112] and later experimentally demonstrated in bulk Si, GaAs and Ge[37,48,113-115] as another effective solution to overcome the conductivity mismatch problem. Again, it is crucial to maintain a high-quality interface between Ge and the ferromagnetic metal for Ge spin injection through the Schottky contact. Recently, the atomically clean interface reported in many MSi_x/Si/MSi_x and MGe_x/Ge/MGe_x (M = various metals including Ni, Pt, Co, *etc*) nanowire heterostructures has been brought into attention for such application.[69-74,86,89,92-93,116] Indeed, the detection of spin-polarized carriers injected from MnSi into Si at low temperature has been reported in the MnSi/Si/MnSi nanowire heterostructure.[74] In order to build spintronic devices for room-temperature applications, however, ferromagnetic silicide or germanide with higher Curie temperature in such nanowire heterostructures has to be developed.

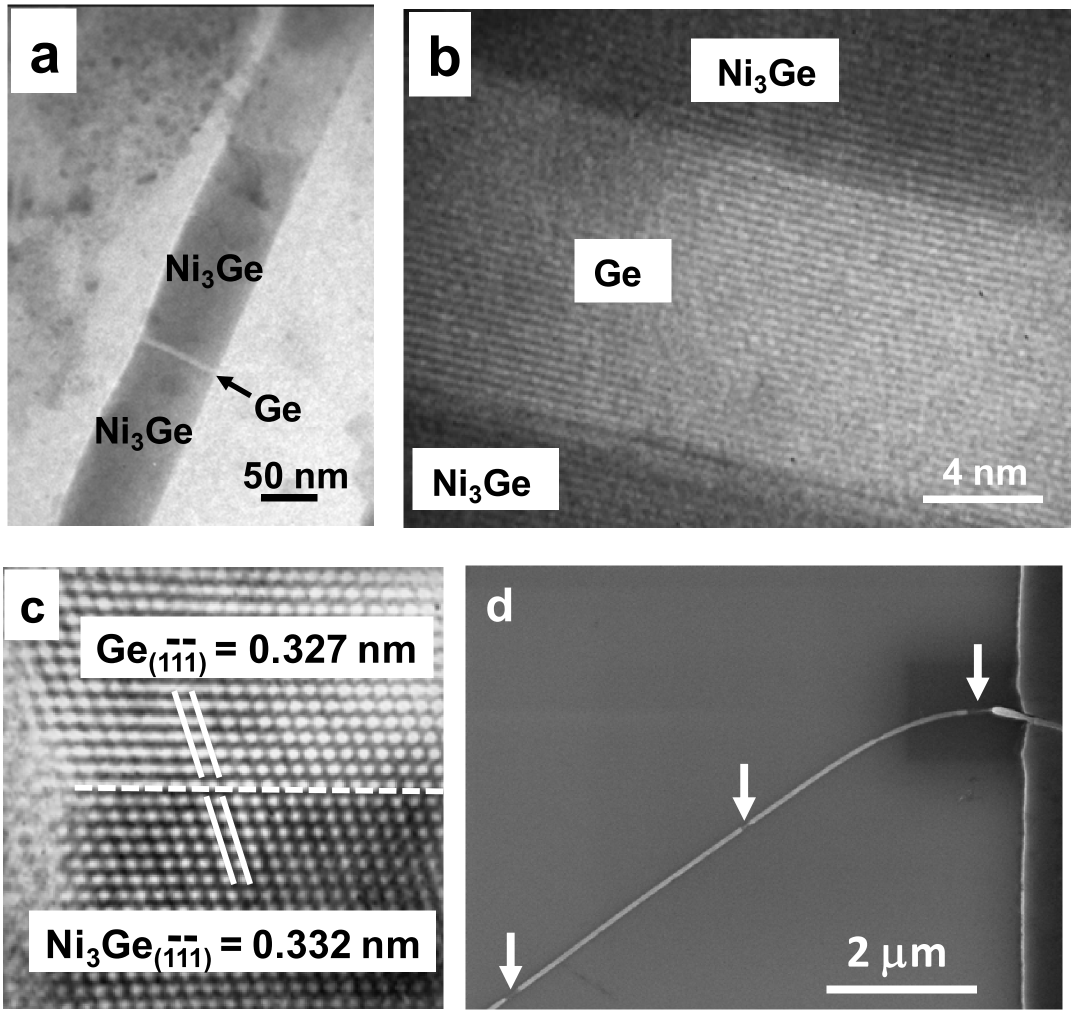

Figure 2-17. Formation of the Ni_3Ge/Ge/Ni_3Ge nanowire heterostructure. (a) TEM image of a fragmented Ni_3Ge nanowire on the TEM grid upon 650 °C annealing. (b) HRTEM image of the Ni_3Ge/Ge/Ni_3Ge nanowire heterostructure showing a clean and sharp interface. (c) Lattice-resolved HRTEM image of the Ni_3Ge/Ge interface. The measured lattice mismatch was only 1.5 % at the $Ni_3Ge(1\bar{1}\bar{1})$/$Ge(1\bar{1}\bar{1})$ interface. As a

result, the twisted growth mode, which was observed in both $Ni_2Ge/Ge/Ni_2Ge$ and $Ni_2Ge/NiGe/Ge/NiGe/Ni_2Ge$ nanowire heterostructures to accommodate the large lattice mismatch, did not occur in this $Ni_3Ge/Ge/Ni_3Ge$ nanowire heterostructure. (d) SEM image showing a broken Ge nanowire upon 650 °C RTA due to a low melting pointing of the Ge nanowire. (The data also appeared in my publication Ref. [89].[89])

In the Ni-Ge nanowire system, a room-temperature ferromagnetic germanide phase Ni_3Ge, in contrast with Ni_2Ge and NiGe discussed in Chapters 2.2 and 2.3,[79] was developed at a high annealing temperature of 650 °C, in which a high-concentration Ni vapor from a large-area Ni contact pattern surrounded the Ge nanowires to form a fragmented Ni_3Ge nanowire. This ferromagnetic phase is favorable for spintronics application, such as spin injection into Ge nanowire. Figure 2-17(a) shows the TEM image of the formed $Ni_3Ge/Ge/Ni_3Ge$ nanowire heterostructure on the TEM grid upon 650 °C annealing. Figure 2-17(b) illustrates the HRTEM image of the Ge nanowire heterostructure with a clean and sharp interface between Ni_3Ge and Ge. The Ge region was controlled down to as small as 12 nm. The strained short Ge region in the $Ni_3Ge/Ge/Ni_3Ge$ nanowire heterostructure is promising for both high-performance FETs and spintronics applications.[74,117] Figure 2-17(c) shows the lattice-resolved TEM image of the Ni_3Ge/Ge interface, and the formed germanide was identified to be single-crystalline Ni_3Ge with a face-centered cubic (FCC) lattice structure (Fd3m, space group 227 and JCPDS No 65-7680) and a lattice constant of $a = 0.574$ nm. Although a slight volume expansion was still observed, the Ni_3Ge lattice was well fit with the Ge lattice, due to their same lattice structure and a very small lattice mismatch of only 1.5% (the lattice constant of Ge is a = 0.568 nm). It is worth mentioning that the twisted growth mode, which was previously observed in both $Ni_2Ge/Ge/Ni_2Ge$ and $Ni_2Ge/NiGe/Ge/NiGe/Ni_2Ge$ nanowire heterostructures to accommodate the large lattice mismatch (see Chapters 2.2 and 2.3), did not occur in this $Ni_3Ge/Ge/Ni_3Ge$ nanowire heterostructure due to such a small lattice mismatch. However, as mentioned above, the melting point of Ge nanowires is significantly reduced from that of bulk Ge.[88] As a result, Ge nanowires were easily broken at high temperature, as shown in Figure 2-17(d). Therefore, a ferromagnetic germanide remains undeveloped at a relatively low annealing temperature in order to study the spin transport in Ge nanowire.

Intriguingly, in the Mn-Ge system, many manganese germanides Mn_xGe_y, such as Mn_3Ge_2, Mn_5Ge_3 and $Mn_{11}Ge_8$, exhibit ferromagnetic ordering close to or above room temperature. In particular, Mn_5Ge_3, with a Curie temperature close to 300 K, has been intensively studied as a high-efficiency spin injection source into Ge toward building Ge SpinFETs,[118-121] although most of the pioneer work has been focused on the epitaxial growth of Mn_5Ge_3 on bulk Ge. Moreover, by introducing carbon doping, the Curie temperature of $Mn_5Ge_3C_x$ can be dramatically increased up to 445 K for building practical spintronic devices that can be operated at room-temperature.[122] In this section, we present the formation and characterization of $Mn_5Ge_3/Ge/Mn_5Ge_3$ nanowire transistors *via* the solid-state reaction between a single-crystalline Ge nanowire and Mn contact pads upon RTA. This work reports the formation of ferromagnetic germanide in Ge nanowire transistors with high-quality interfaces through thermal annealing.

To prepare TEM samples, single-crystalline Ge nanowires with growth direction along [111] axes were synthesized vertically on a Si (100) wafer using a conventional VLS method as described elsewhere.[123] In order to control the nanowire diameter and length, dodecanethiol-coated Au nanoparticles were prepared self-assembly on a Si (100) substrate to serve as the catalyst for the Ge nanowire growth. The precursor diphenylgermane was injected into the reactor to stimulate the nanowire growth at 420 ^{o}C.[124] The VLS-grown Ge nanowires were typically 50-80 nm in diameter with lengths larger than 10 μm. Ge nanowires were not doped on purpose during growth, but unintentional doping usually occurred.[85,125]

Figures 2-18(a) and 2-18(b) schematically illustrate the formation process of the Mn-Ge nanowire heterostructure. TEM studies were performed in order to identify the formed germanide phase and the epitaxial relationship in the Mn-Ge nanowire heterostructure. Mn-Ge nanowire devices for TEM studies were fabricated on Ge nanowires with [111] growth directions, which were dispersed on special TEM grids with 50 nm thick Si_3N_4 windows and patterned by EBL and subsequent e-beam deposition of 150 nm thick Mn. Before the metal deposition, the sample was dipped into diluted HF solution for 15 s to completely remove native oxide in the contact region. To prevent Mn oxidization, a layer of 5 nm Ti followed by 20 nm Au was capped on the Mn electrodes. The diffusion of protection metals (Ti/Au) into Ge nanowires was not observed. Other protection layers, such as Ti/Pt, Ti/Al, and Cr/Pt, were also tested to cap the Mn electrodes, and they all showed the same results. The as-fabricated Mn-Ge nanowire devices were then loaded into the TEM chamber with a heating holder (Gatan 652 double tilt heating holder) for *in situ* annealing under a RTA mode with a pressure below 10^{-6} Torr. The temperature was ramped from room temperature up to 450 ^{o}C at a rate of about 25 ^{o}C/s. A field-emission TEM (JEM-3000F, operated at 300 kV with a point-to-point resolution of 0.17 nm) equipped with an EDS was used to obtain the epitaxial relationships and determine the chemical compositions of the nanowire heterostructure. The formed single-crystalline germanide was identified to be Mn_5Ge_3 based on the following TEM studies. Figure 2-18(c) shows the TEM image of a typical Mn_5Ge_3/Ge nanowire heterostructure upon 450 ^{o}C RTA inside the TEM chamber. The high-resolution TEM image in Figure 2-18(d) demonstrated an atomically clean interface between Mn_5Ge_3 and Ge. Similarly, such high-quality interface has also been observed in many Ge and Si nanowire heterostructures, which is one of the unique properties in the effort of making nanoscale contacts to one-dimensional semiconductor channels through thermal annealing. The diffraction patterns in the inset of Figure 2-18(d) revealed the epitaxial relationship to be [010]Mn_5Ge_3(002)//[110]Ge(002). The formed Mn_5Ge_3 was found to have a hexagonal lattice structure (space group No. 193, $P6_3/mcm$ in the Hermann-Mauguin notation or $D8_8$ structure type in the Strukturbericht designation) with lattice constants: a_{hex} = 0.7184 nm and c_{hex} = 0.5053 nm. From the high-resolution TEM image, the lattice spacings were determined to be d_{002} = 0.253 nm for Mn_5Ge_3(002) planes and d_{002} = 0.283 nm for Ge(002) planes, respectively. The spacing difference gives a relatively small lattice mismatch of 10.6% compared with that reported in Mn-Si nanowire and Ni-Ge nanowire systems.[74,86,93] The EDS in Figure 2-18(e) indicated a Mn/Ge atomic ratio of 62/38, which reaffirms the formed Mn_5Ge_3 phase. The Si peak was originated from the Si_3N_4 window on the TEM grid.

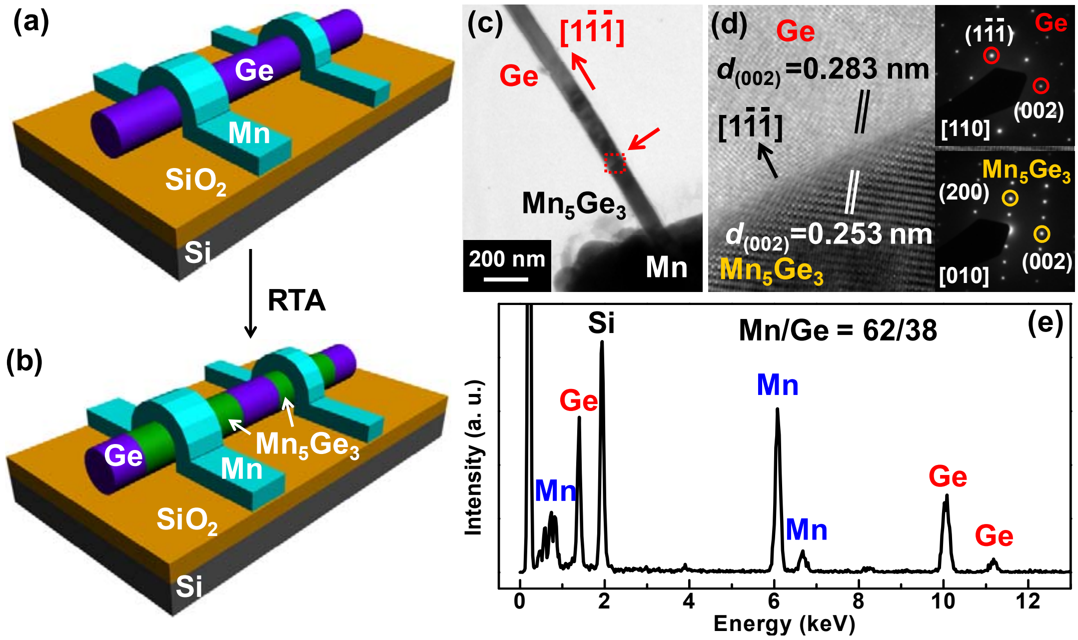

Figure 2-18. Formation of Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire heterostructure. Schematic illustration of (a) as-deposited Mn-Ge nanowire device structure and (b) the formation of Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire heterostructure by the solid-state reaction between a single-crystalline Ge nanowire and Mn contact pads upon RTA. (c) Low-magnification TEM image of a Mn_5Ge_3/Ge nanowire heterostructure. (d) High-resolution TEM image, showing an atomically clean interface between Mn_5Ge_3 and Ge with a relatively small lattice mismatch of 10.6%. The labeled lattice spacings are: d_{002} = 0.253 nm for Mn_5Ge_3 and d_{002} = 0.283 nm for Ge. The inset shows the

diffraction patterns of Ge and Mn_5Ge_3. (e) EDS of the formed germanide region with a Mn/Ge atomic ratio of 62/38, confirming the phase of Mn_5Ge_3. (The data also appeared in my publication Ref. [126].[126])

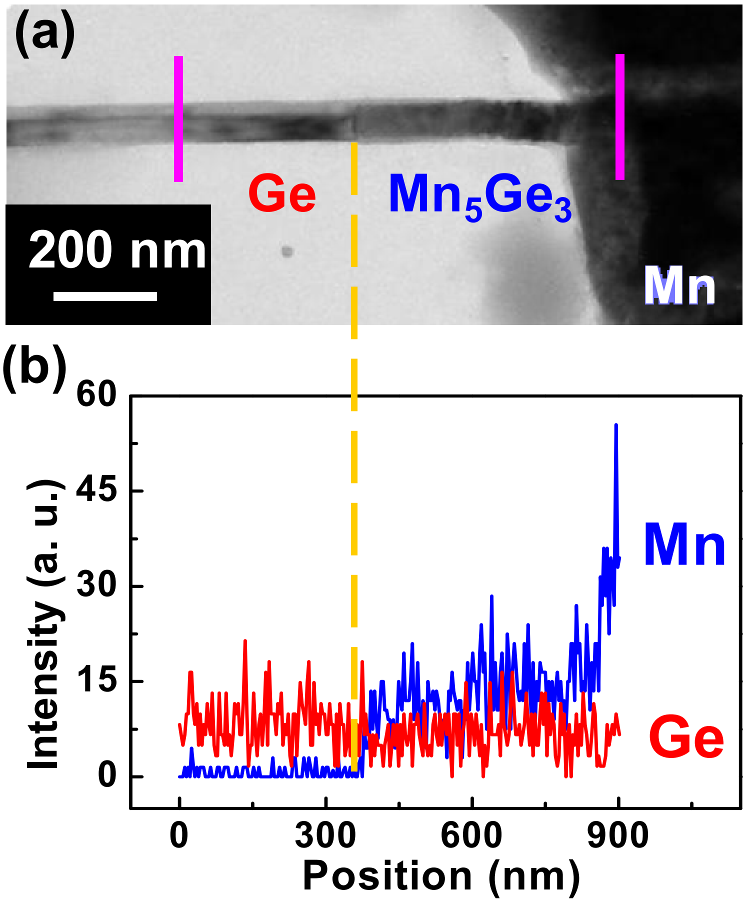

Figure 2-19. Plane-TEM view of the Mn-Ge nanowire device. (a) TEM image of a Mn_5Ge_3/Ge nanowire heterostructure. (b) Line-scan profile across the Mn_5Ge_3/Ge nanowire heterostructure in the region between two red solid lines, showing an almost constant Ge concentration. The yellow dash line indicates the position of the Mn_5Ge_3/Ge interface. (The data also appeared in my publication Ref. [126].[126])

Besides, the line-scan profile of Mn and Ge concentrations in a Mn_5Ge_3/Ge nanowire heterostructure is shown in Figure 2-19. The nearly constant Ge concentration suggests that Mn is the dominant diffusion species in the Mn-Ge nanowire system.

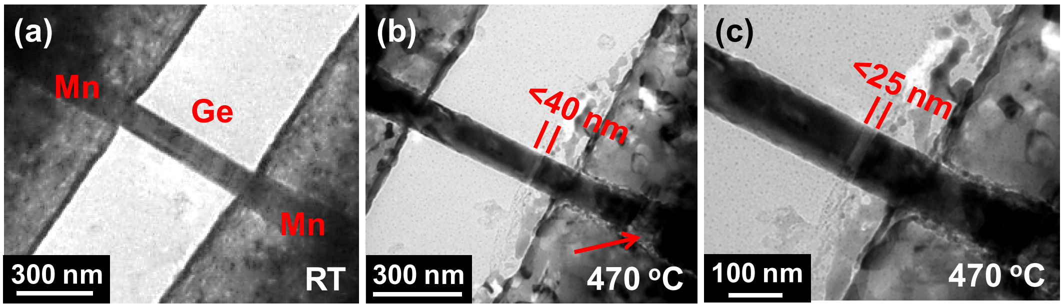

Figure 2-20. Formation of Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire heterostructure with ultra-short Ge nanowire channels. (a) TEM image of an as-fabricated Ge nanowire device with a 560 nm long Ge nanowire channel. (b) TEM image of the formed Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire heterostructure with less than 40 nm long Ge nanowire channel after 470 ^{o}C RTA for about 2 mins. The red arrow indicates a "void" caused by the significant Mn consumption from the Mn electrode during the reaction. (c) TEM image of the formed Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire heterostructure with less than 25 nm long Ge nanowire channel after extended RTA. (The data also appeared in my publication Ref. [126].[126])

It is worth noting that the Ge nanowire channel length can be scaled down to sub-30 nm by carefully controlling the annealing temperature and time. Figure 2-20(a) shows the TEM image of an as-fabricated Ge nanowire device with two Mn electrodes at room temperature. The original Ge nanowire channel was about 560 nm long. Figure 2-20(b) shows the TEM image of the formed Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire heterostructure after the RTA at 470 ^oC for about 2 mins, in which the Ge nanowire channel was reduced down to less than 40 nm. (Note that a small annealing temperature range of 450-470 ^oC was studied and the formed single-crystalline germanide was the same as Mn_5Ge_3) Extended annealing further reduced the Ge nanowire channel down to less than 25 nm, as shown in Figure 2-20(c). It was found that the Mn diffusion velocity in the Ge nanowire not only was a function of the temperature, but also depended on the Mn flux. Significant Mn consumption from the Mn electrodes was observed in the formation of Mn_5Ge_3, as indicated by the red arrow in Figure 2-20(b). The “void” in the lower-side Mn electrode would reduce the Mn diffusion, which causes the seeming “predominant” Mn diffusion from the upper-side contact. It is worth noting that neither significant volume expansion nor apparent nanoparticle segregation was observed in the annealing process, which could be attributed to the relative small lattice mismatch between Mn_5Ge_3 and Ge of about 10.6%.

In addition, exceeding annealing could further convert a Ge nanowire into a single-crystalline Mn_5Ge_3 nanowire, as shown in Figure 2-21. This result clear shows that the Mn_5Ge_3 phase is thermally stable under the annealing condition. Also, significant Mn consumption can be inferred from the voids formed at the edges of Mn electrodes.

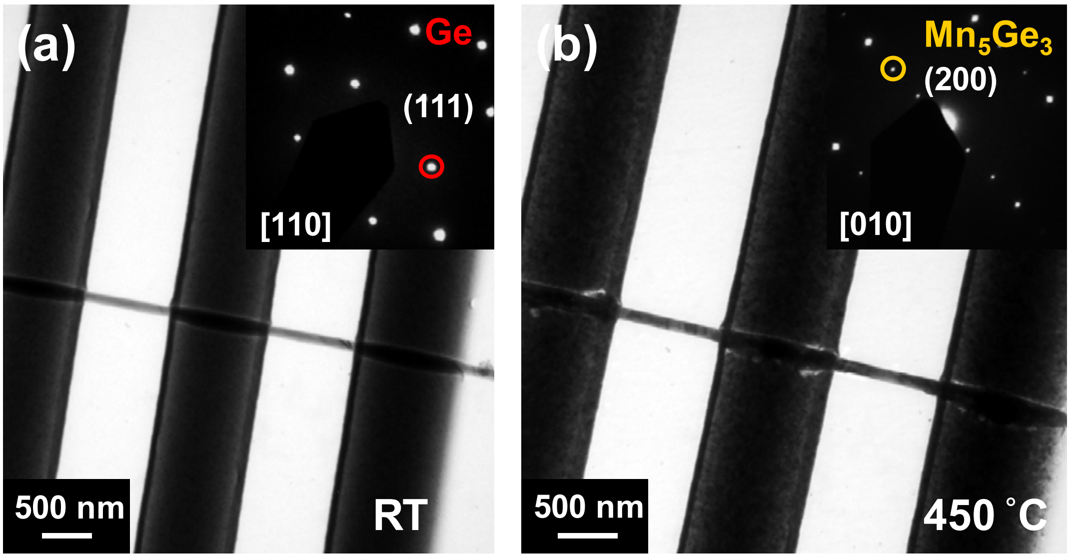

Figure 2-21. Thermal stability of the Mn_5Ge_3 nanowire. TEM images of (a) as-fabricated Ge nanowire device and (b) fully germanided Mn_5Ge_3 nanowire after RTA at 450 °C for more than 30 min. The insets show the diffraction patterns for Ge and Mn_5Ge_3, respectively. The result clear shows that the Mn_5Ge_3 phase is thermally stable under the annealing condition. Also, significant Mn consumption can be inferred from the voids formed at the edges of Mn electrodes. (The data also appeared in my publication Ref. [126].[126])

Similar to the Ni-Ge nanowire system, to further illustrate the epitaxial relationship between Mn_5Ge_3 and Ge in the formed Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire heterostructure, the lattice sketch of a plausible arrangement of the Mn_5Ge_3/Ge interface with an epitaxial relationship of [010]Mn_5Ge_3(002)//[110]Ge(002) is shown in Figure 2-22.

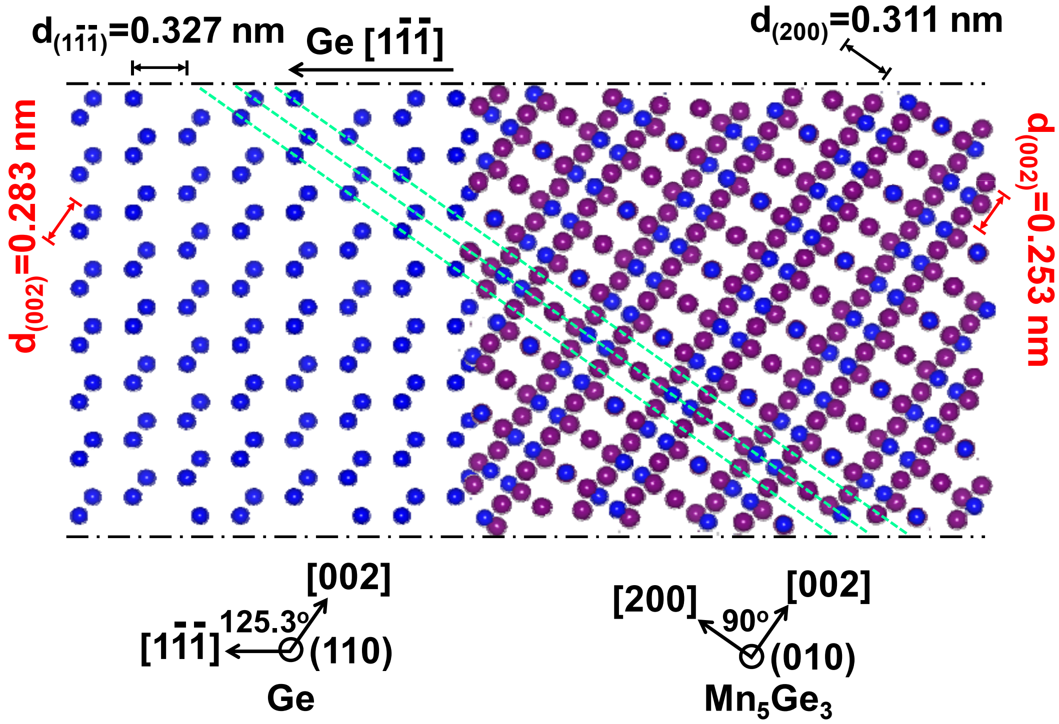

Figure 2-22. Schematic illustration of a plausible arrangement of the Mn_5Ge_3/Ge interface. The blue balls represent Ge atoms, while the purple balls represent Mn atoms. The green dash lines indicate the parallel planes of Ge and Mn_5Ge_3 with a relatively small lattice mismatch of 10.6%. The Mn_5Ge_3 has a hexagonal crystal structure, while Ge has a diamond cubic crystal structure. (The data also appeared in my publication Ref. [126].[126])

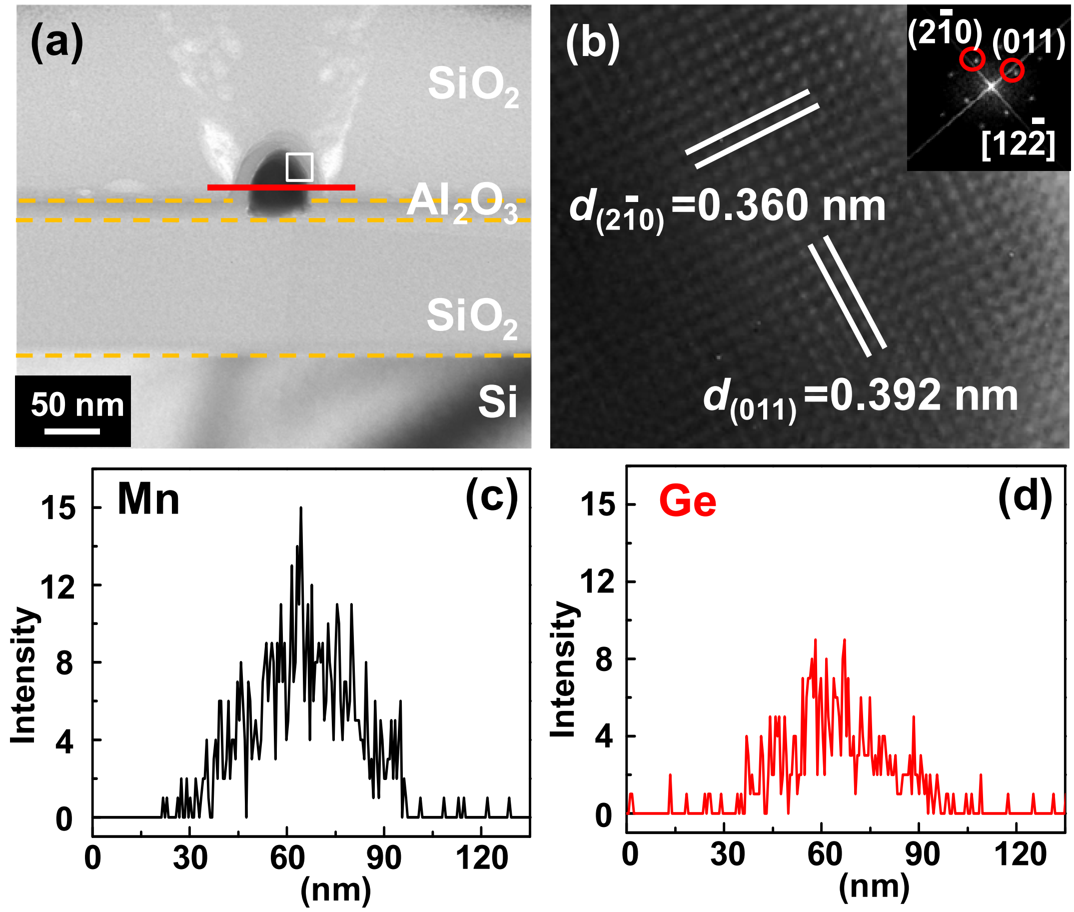

Figure 2-23. Cross-sectional TEM study of a Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire device. (a) TEM cross-sectional view of the formed Mn_5Ge_3 nanowire capped with 20 nm Al_2O_3 on the SiO_2/Si substrate. (b) High-resolution TEM image of the Mn_5Ge_3 region. The inset shows the corresponding diffraction pattern after fast Fourier transform. (c-d) Line-scan profiles of Mn and Ge contents in the formed germanide, respectively, reaffirming the formation of the Mn_5Ge_3 phase. (The data also appeared in my publication Ref. [126].[126])

To further investigate the cross-sectional view of the formed germanide, Mn-Ge nanowire devices were fabricated on the SiO_2/Si substrate as to be described below (see Figure 2-24). FIB was used to cut the germanide region into a 50 nm thick slice as shown in Figure 2(a), which was placed on a carbon-supported TEM Cu grid and then loaded into the TEM chamber for imaging. It is worth noting that, unlike the Ni-Ge nanowire system, no significant segregation of germanide nanoparticles on the germanide region was observed in the Mn-Ge nanowire system, and could be due to the relatively small lattice mismatch (~10.6%) between Mn_5Ge_3 and Ge. Figure 2(b) shows the high-resolution TEM image of the germanide region, and the diffraction pattern in the inset confirmed the single-crystalline Mn_5Ge_3 phase with a hexagonal lattice structure. The EDS line-scan profiles of Mn and Ge across the region indicated by the red line in Figure 2-23(a) are shown in Figures 2-23(c) and 2-23(d), respectively. The Mn/Ge atomic ratio is consistent with the Mn_5Ge_3 phase as well as the EDS result in Figure 2-18(e).

Similar to Ni_2Ge and NiGe in Ni-Ge nanowire heterostructures,[86,93] the formed Mn_5Ge_3 can be used as source/drain contacts to the Ge channel for the fabrication of high-performance Ge nanowire FETs (see Figure 2-24(a)). The Ge nanowire channel length can be scaled down to sub-30 nm by controlling the annealing temperature and time (see Figure 2-20).[89] To fabricate the Mn-Ge nanowire devices for electrical measurements, VLS-grown Ge nanowires were transferred onto a pre-patterned SiO_2/Si substrate. The top thermal SiO_2 was 300 nm thick, and the Si substrate was degenerately doped to have a resistivity of $1\text{-}5\times10^{-3}$ Ω-cm, which served as the back-gate for further device characterization. Mn/Ti/Au contacts to Ge nanowires were defined with EBL followed by e-beam evaporation of the contact layers. Before the metal deposition, the sample was dipped into diluted HF solution for 15 s to completely remove native oxide in the contact region similar to before. Prior to the RTA process in the ambient of N_2, a layer of 20 nm Al_2O_3 was deposited on top with ALD to protect the Mn electrode and the formed germanide from oxidization. TEM studies showed that the Al_2O_3 capping layer did not affect the formed germanide phase and the growth of Mn_5Ge_3 in the Ge nanowire (see Figure 2-23). Figure 2-24(b) shows the SEM image of as-fabricated Mn-Ge nanowire devices with multiple electrodes, and the measurement setup is illustrated in Figure 3(a). The I_{DS}-V_{GS} characteristics of a typical Ge nanowire FET with an effective channel length of 0.5 μm after RTA and a nanowire diameter of 70 nm demonstrated a *p*-type transistor behavior with a current ON/OFF ratio close to 10^5, as shown in Figure 2-24(c). The dual-sweep I_{DS}-V_{GS} curves showed a relatively small hysteresis, which could be attributed to the effective passivation of the Ge nanowire surface by Al_2O_3.[93] The normalized transconductance (g_m) at a drain bias of $V_{DS} = 0.1$ V was extracted to be 3.56 μS/μm, which led to a field-effect hole mobility of 170 cm^2/Vs using Equation (2-1). Mobility measured from more than 20 devices fell into the range of 150-200 cm^2/Vs. The gate capacitance C_{ox} here is estimated using Equation (2-2) from the cylinder-on-plate model, given that r = 35 nm is the radius of the Ge nanowire, t_{ox}=300 nm is the thickness of the back-gate dielectric, L = 0.5 μm is the effective Ge nanowire channel length. In order to provide a more accurate estimation of the gate capacitance, finite element simulation was performed by Wunnicke, which gave rise to an effective dielectric constant of $\varepsilon_{ox,eff} = 2.2$ for SiO_2 in Equation (2-2).[91] Then the calculated gate capacitance and mobility would be $C_{ox} = 2.074\text{x}10^{-17}$ F and $\mu_h = 301$ cm^2/Vs, respectively. Therefore, the value of $\mu_h = 170$ cm^2/Vs using $\varepsilon_{ox} = 3.9$ for SiO_2 is the lower limit for the carrier mobility estimation. The sub-threshold swing was also extracted to be about 3.81 V/dec for a relative thick back-gate dielectric of 300 nm SiO_2. The I_{DS}-V_{DS} characteristics in Figure 2-24(d) reaffirmed that Mn_5Ge_3 are good source/drain contacts.

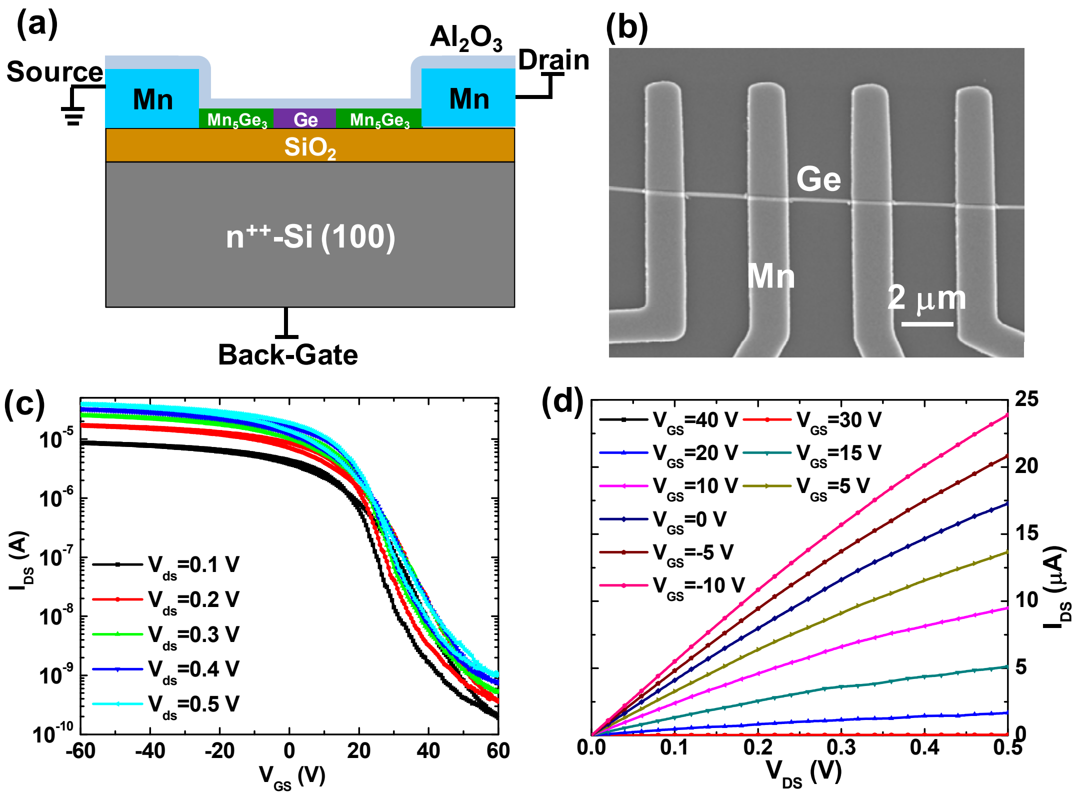

Figure 2-24. Characterization of a back-gate Ge nanowire FET. (a) Schematic illustration of the Ge nanowire FET built on the $Mn_5Ge_3/Ge/Mn_5Ge_3$ nanowire

heterostructure. (b) SEM image of the Ge nanowire FET device. (c) Dual-sweep I_{DS}-V_{GS} characteristics of the back-gate Ge nanowire FET, showing a relatively small hysteresis. (d) The corresponding I_{DS}-V_{DS} characteristics of the Ge nanowire transistor. (The data also appeared in my publication Ref. [126].[126])

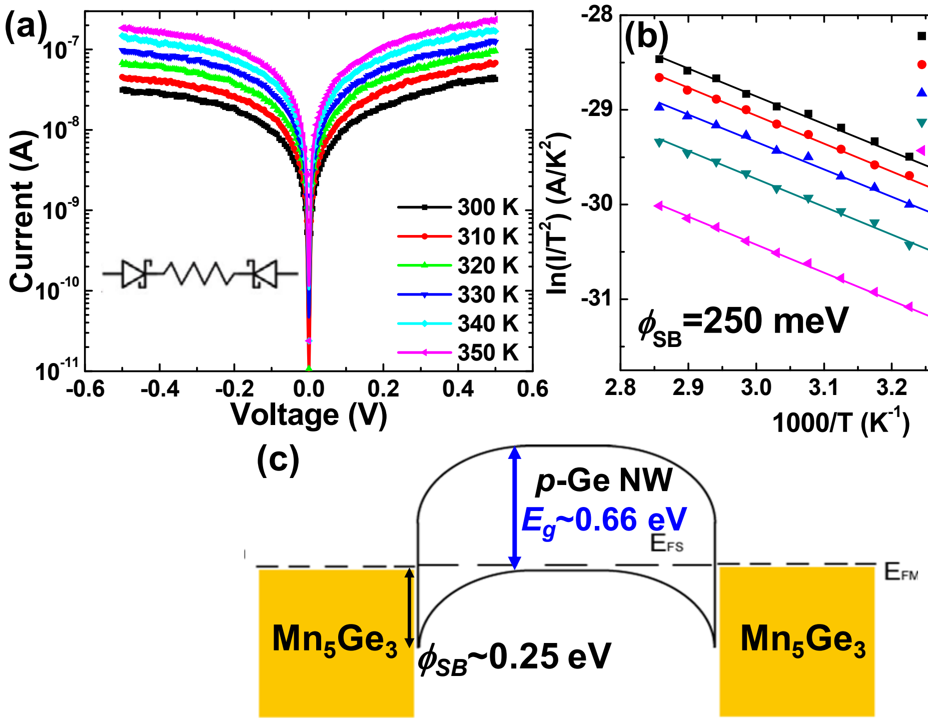

Figure 2-25. Temperature-dependent *I*-*V* measurements on the Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire heterostructure. (a) *I*-*V* measurements on a Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire heterostructure in the temperature range of 300-350 K. (b) Arrhenius plot at various drain biases. The extracted Schottky barrier height from Mn_5Ge_3 to *p*-type Ge is about 0.25 eV. (c) Corresponding energy band diagram of the Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire heterostructure. (The data also appeared in my publication Ref. [126].[126])

To further evaluate the Mn_5Ge_3 contact to Ge, temperature-dependent *I-V* measurements were performed on a Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire heterostructure in the temperature range of 300-350 K, and the results are shown in Figure 2-25(a). Figure 2-25(b) shows the linear fitting of $\ln(I/T^2)$ *versus* $1/T$ in the Arrhenius plot at various drain biases revealing a consistent Schottky barrier height of 0.25 eV. The corresponding band diagram for the Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire heterostructure is drawn in Figure 2-25(c).

In summary, a Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire heterostructure with atomically clean interfaces has been formed by the thermal intrusion of Mn into a single-crystalline Ge nanowire at 450 ^{o}C. TEM studies revealed an epitaxial relationship of [010]Mn_5Ge_3(002)//[110]Ge(002) with a relatively small lattice mismatch of 10.6% between Mn_5Ge_3(002) and Ge(002) planes. Back-gate Ge nanowire FETs have been fabricated on the Mn_5Ge_3/Ge/Mn_5Ge_3 heterostructure by using the formed Mn_5Ge_3 region as the source/drain contacts to the Ge nanowire channel. Electrical measurements have shown a high-performance *p*-type transistor behavior with a current ON/OFF ratio close to 10^5, and a field-effect hole mobility of 150-200 cm^2/Vs. The Schottky barrier height from the Mn_5Ge_3 contact to *p*-type Ge extracted from the temperature-dependent *I-V* measurement was about 0.25 eV; the result suggested that Mn_5Ge_3 may be used as a promising spin injection source into Ge nanowires. It should be pointed out that heavily-doped Ge nanowires are usually required to overcome the fundamental obstacle of the conductivity mismatch between metallic Mn_5Ge_3 and semiconducting Ge.[110] This work represents a promising step toward electrical spin injection into Ge nanowires and thus realization of high-efficiency spintronic devices, which will be discussed in Chapter 3.3 later.

2.5 Atomically Clean Interfaces in Ge Nanowire Heterostructure Transistors

At this point, we have fabricated several Ge nanowire heterostructures with different germanide contacts, including Ni_2Ge, NiGe, Ni_3Ge, and Mn_5Ge_3, using thermal annealing, as discussed in the previous Chapters 2.2-2.4. It can be seen that they all showed atomically clean interfaces to the Ge nanowire, despite of the fact that noticeable lattice mismatch ranging from 1.5 % up to 77.7 % was observed at the germanide/Ge nanowire interfaces. For comparison, Table 2-1 summarizes the measured lattice mismatch in the literature-reported Ge nanowire heterostructures as well as Si nanowire heterostructures. It can be seen that such large lattice mismatch was widely observed in the 1D epitaxial growth of germanide/silicide in the Ge/Si nanowire. As we know, a large lattice mismatch in the 2D epitaxial growth could lead to the formation of noticeable defects such as threading dislocations and quantum dots. It is noted that the epitaxial area in 2D is very large, *i.e.*, typically over the entire substrate; therefore the accumulated strain is easily relaxed, which leads to the defects formation. For the unique 1D growth mode, however, the epitaxial growth in the Ge/Si nanowire occurs on a very small area, *i.e.*, the cross section of the Ge/Si nanowire, so that the energy required to form dislocations could be large (as discussed previously in Chapter 2.3). We have also shown that the oxide confinement could affect the germanide formation and the associated lattice mismatch in the Ni-Ge nanowire system. Further microscopic studies in simulation and experiment as well as growth dynamic analysis are required to understand the growth kinetics for this unique growth mode in one-dimensional systems.

Table 2-1. Lattice mismatch at the interfaces of Ge and Si nanowire heterostructures.

Material system	**RTA condition (^{o}C)**	**Formed silicide/germanide**	**Lattice mismatch**
Ni-Ge[86]	400-500	Ni_2Ge	56.3 %
Ni-Ge[93]	450 (capped with Al_2O_3)	Ni_2Ge/NiGe	77.7 %
Ni-Ge[89]	650	Ni_3Ge	1.5 %
Mn-Ge[126]	450	Mn_5Ge_3	10.6 %
Cu-Ge[92]	310	Cu_3Ge	38.6 %
Ni-Si[71]	500-700	NiSi	5.62 %
Co-Si[72]	800	Co_2Si	1.2 %
Pt-Si[73]	520	PtSi	8.8 %
Mn-Si[57]	650	MnSi	24.5 %

Finally, let’s take a look at the effect of such atomically clean interface on the electrical transport properties. As we discussed in the Overview, there is a strong Fermi level pinning in conventional metal/Ge contacts because of the high-density interface states. The produced atomically clean interfaces in the Ge nanowire heterostructures would be able to alleviate the Fermi level pinning in the germanide contacts to the Ge nanowire. Figure 2-26 shows the Arrhenius plot extracted from the temperature-dependent *I*-*V* measurements on three Ge nanowire heterostructures with different germanide contacts at a drain bias of 0.1 V. The extracted Schottky barrier heights for Mn_5Ge_3, NiGe and Ni_2Ge contacts to *p*-type Ge are 0.25 eV, 0.11 eV and 0.08 eV, respectively. This is in contrast with the scenario in Figure 2.2 in Chapter 2.1, where strong Fermi level pinning occurs in conventional metal/Ge contacts. In our work, the change in the Schottky barrier height for different germanide contacts suggest that the Fermi level pinning is indeed alleviated using the high-quality germanide contacts.

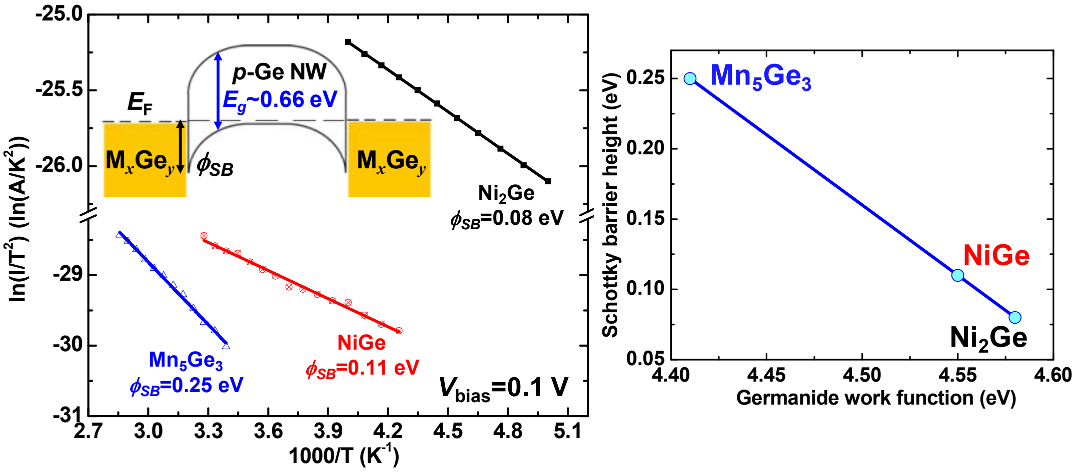

Figure 2-26. Schottky barrier height of three Ge nanowire heterostructures. (a) Arrhenius plot from the temperature-dependent *I*-*V* measurements on three Ge nanowire heterostructures with different germanide contacts at a drain bias of 0.1 V. The inset shows the corresponding energy band diagram. (b) The extracted Schottky barrier heights for Mn_5Ge_3, NiGe and Ni_2Ge contacts to *p*-type Ge versus their work functions. The clear change in the Schottky barrier height for different germanide

contacts suggests that in all the studies discussed previously in Chapters 2.2-2.4, Fermi level pinning did not occur. (The data also appeared in my publication Ref. [127].[127])

Chapter 3

Electrical Spin Injection into Ge Nanowires

3.1 Overview

For the sake of long spin lifetime and diffusion length, there has been increasing research interest in investigating the spin transport in semiconductor nanowires, in which the spin relaxation has been predicted to be significantly suppressed.[51-52,54-55] Recently, both tunneling and Schottky spin injection into several semiconductor nanowires have been reported, including Ge,[7-8,56] Si,[57-58] GaN,[59] and InN,[60] and the observed spin lifetimes and diffusion lengths are indeed much larger than those reported in bulk materials, as shown in Table 1-2. This stimulates the research interest to study the spin transport in semiconductor nanowires and further to build nanowire-based novel spintronic devices.

It should be pointed out that the electrical spin injection is very sensitive to the interface of FM/SC junction, because the localized states and the surface roughness could significantly complicate and jeopardize the spin injection process.[27] Therefore, the fabrication of high-quality ferromagnetic junction on nanowires for spin injection is very challenging, especially considering the cylindrical geometry of nanowires and the high density interface states associated with the high surface-to-volume ratio. Besides, the large difference in the conductivity between FM/SC would make the spin injection efficiency negligibly small, well known as the conductivity mismatch problem.[110] Therefore, a Schottky or tunneling barrier is usually employed at the FM/SC interface to circumvent this problem.[128-129] For the Schottky barrier approach, it is very important to maintain a clean interface for the FM/SC Schottky contact to minimize defects-induced interface states and Fermi level pinning.[130] On the tunneling approach, various oxides have been studied as the tunneling barrier in the spin injection into Si and Ge,[21,23,34-35,131] including native oxide (SiO_2 and GeO_x), Al_2O_3 (usually by oxidizing a thin layer of Al or ALD) and MgO (by sputtering or MBE). In fact, the insertion of such a thin intervening insulator in the FM/SC junction has been demonstrated to be an effective approach to modulate the Schottky barrier height and alleviate the Fermi level pinning,[98,132-133] The thin insulator layer is considered either to passivate the semiconductor surface states and/or reduces the metal-induced gap states by suppressing the wave function tailing of the metal into the band gap of the semiconductor.[134]

In this Chapter, we will take the advantage of the room-temperature ferromagnetic germanide contact with atomically clean FM/SC interfaces in the fabricated Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire transistor to realize the electrical spin injection into Ge nanowires (Chapter 3.3). Before that, the magnetic property of the single-crystalline Mn_5Ge_3 nanowire will be studied through electrical magneto-transport measurements to probe the magnetic phase transition and domain wall motion (Chapter 3.2). Alternatively, tunneling spin injection into Ge nanowires will also be demonstrated using high-quality epitaxial Fe/MgO tunnel junctions (Chapter

3.4). In the end, we will briefly discuss the proposal of a novel DMS-based nonvolatile spin transistor (transpinor), which can be fabricated on the spin injection device demonstrated using the Mn_5Ge_3 Schottky contact and Fe/MgO tunnel junction (Chapter 3.5).

3.2 Electrical Probing of Magnetic Phase Transition and Domain Wall Motion in Single-Crystalline Mn_5Ge_3 Nanowire

In the previous studies of Si(Ge) nanowire heterostructures formed by RTA, most have been focused on the growth dynamics of silicides(germanides) in Si(Ge) nanowires and the electrical property of silicide (germanide) contacts to determine the resistivities and Schottky barrier heights to Si(Ge) nanowires, which are crucial for determining the nanowire transistor performance.[135-137] However, little has been done in studying detailed magnetic properties, magnetization dynamics in particular, of the formed silicide and germanide nanowires,[57] which are critical in order to further explore spintronic applications in those Si(Ge) nanowire heterostructures. For example, recalling the above-discussed high-quality epitaxial interface of Mn_5Ge_3 on Ge and the room-temperature ferromagnetism of Mn_5Ge_3, it is promising to realize spin injection from Mn_5Ge_3 into Ge nanowires through this Schottky barrier.

In the literature, both theoretical calculations and experimental work have been carried out to investigate Mn_5Ge_3 as a high-efficiency spin injection source into Ge.[118-121,138] Most of the pioneer experimental work has been focused on the epitaxial growth of Mn_5Ge_3 on bulk Ge, and the Mn_5Ge_3 epilayer on both Ge (111) and GaAs (111) substrates was reported to have a spin polarization of about 42% at $T=1.2$ K from Andreev reflection measurements.[120] Besides, in the previous study of Chapter 2.4,[126] we have successfully fabricated $Mn_5Ge_3/Ge/Mn_5Ge_3$ nanowire heterostructure for future spin transport studies (as to be discussed in Chapter 3.3). However, there is very limited study, to the best of our knowledge, on the 1D Mn_5Ge_3 nanowire system. In fact, the 1D Mn-Ge system may offer great advantages in spintronics applications since the D'yakonov-Perel' spin relaxation could be significantly suppressed in the 1D regime.[108] Therefore, a long spin diffusion length could be expected in the Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire heterostructures. Furthermore, in order to observe the spin signal at room temperature and above, carbon doping can be incorporated into Mn_5Ge_3 to dramatically boost the Curie temperature: $Mn_5Ge_3C_x$ films with carbon concentration $x \geq 0.5$ showed a Curie temperature up to 445 K while maintaining the hexagonal lattice structure.[122]

As a preparation for studying the spin transport in the Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire transistor in Chapter 3.3, here we present a systematic study on the magnetic phase transition and domain wall motion in the as-fabricated single-crystalline Mn_5Ge_3 nanowire using electrical and magneto-transport measurements. The single-crystalline Mn_5Ge_3 nanowire was fabricated by thermally converting a single-crystalline Ge nanowire into Mn_5Ge_3 through a solid-state reaction between the Ge nanowire and Mn metal contacts, as described in the previous Chapter 2.4 for the formation of Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire transistors (also appeared in my publication Ref. [126]).[126] The fabrication process is schematically illustrated in Figures 3-1(a-b). Briefly, Ge nanowires grown by conventional VLS method with [111] growth directions were dispersed on a SiO_2/Si substrate,[123] and then patterned with EBL followed by the e-beam deposition of 150 nm-thick Mn contacts. A 5 nm/20 nm thick Ti/Au capping layer was also deposited on top of the Mn electrodes to prevent Mn from oxidization. The Mn-Ge nanowire device was then annealed at 450 ^{o}C in the ambient of N_2 with RTA to drive Mn atoms diffuse into the Ge nanowire and then completely convert it into Mn_5Ge_3. Excessive annealing could assure the fully germanidation of the Ge nanowire but did not change the phase of the formed Mn_5Ge_3 nanowire, suggesting that Mn_5Ge_3 is a thermally stable phase under this annealing condition.[126] The diameter of as-fabricated Mn_5Ge_3 nanowires was typically 50-80 nm, and the length could be several micrometers. The nanowire morphology was inspected with TEM and SEM, as shown in Figure 3-1(c) and the inset of Figure 3-1(d), respectively. The HRTEM image and the corresponding diffraction pattern confirmed the single crystallinity of the formed Mn_5Ge_3 nanowire. Mn_5Ge_3 was found to have a hexagonal lattice structure with lattice constants: a_{hex} = 0.7184 nm and c_{hex} = 0.5053 nm, same as the results in Chapter 2.4. From the high-resolution TEM image, the lattice spacings were determined to be d_{002} = 0.253 nm for the (002) planes and d_{100} = 0.622 nm for the (100) planes, respectively. To extract the electrical resistivity and exclude the contribution from the contact, 2-probe and 4-probe I-V measurements were performed on a 650 nm-long single-crystalline Mn_5Ge_3 nanowire, as shown in Figure 3-1(d). The inset of Figure 3-1(d) shows the SEM image of a typical Mn_5Ge_3 nanowire device with multiple electrodes. The 4-probe resistance measurement of the Mn_5Ge_3 nanowire (with a diameter of about 60 nm) gave $R_{4\mathrm{p}}$ = 551 Ω at T = 300 K, which corresponds to a resistivity of ρ = 240 μΩ-cm. The extracted resistivity is on the same order with the reported values from an early work on Mn_5Ge_3 bulk crystals ($\rho \sim$ 500 μΩ-cm) and more recent studies on Mn_5Ge_3

thin films (ρ = 90-120 μΩ-cm).[118,120,139]

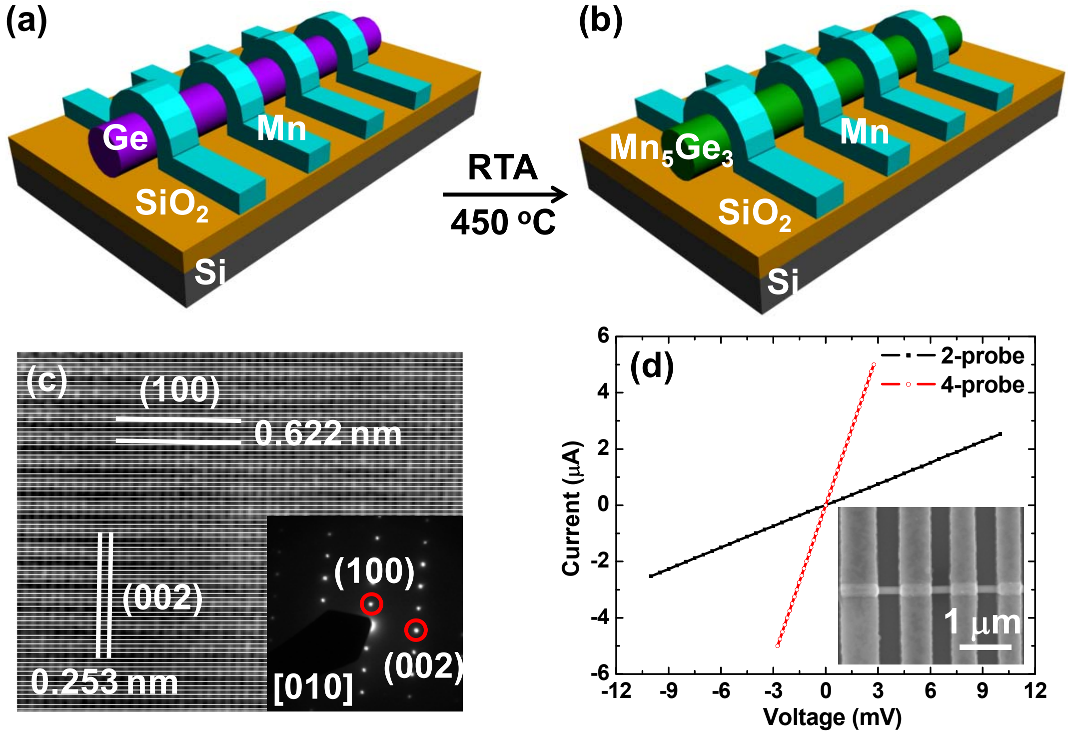

Figure 3-1. Formation of single-crystalline Mn_5Ge_3 nanowire. Schematic illustration of (a) an as-fabricated Ge nanowire device with multiple Mn electrodes on a SiO_2/Si substrate, and (b) thermal conversion of a Ge nanowire into a single-crystalline Mn_5Ge_3 nanowire through RTA at 450 °C. (c) High-resolution TEM image of the formed Mn_5Ge_3 nanowire, confirming its single crystallinity. The inset shows the diffraction pattern along the [010] zone axis. Mn_5Ge_3 was found to have a hexagonal lattice structure (space group No. 193, $P6_3/mcm$ in the Hermann-Mauguin notation) with lattice constants: a_{hex} = 0.7184 nm and c_{hex} = 0.5053 nm. The lattice spacings were determined to be d_{002} = 0.253 nm for the (002) planes and d_{100} = 0.622 nm for

the (100) planes, respectively. (d) 2-probe and 4-probe *I-V* measurements on a single Mn_5Ge_3 nanowire. The inset shows the SEM image of a typical Mn_5Ge_3 nanowire with four electrodes. (The data also appeared in my publication Ref. [140].[140])

In order to study the onset of the magnetic phase transition in nanoscale material systems, it is quite difficult to use conventional methods such as superconducting quantum interference device (SQUID) and Hall or Torque magnetometries,[141-145] because of the extremely weak magnetic signal, for single nanowire in particular. However, the strong correlation between the magnetism and the electrical transport in magnetic systems,[141] namely, a conductivity signature accompanied with a magnetic phase transition enables the latter to be probed electrically. Following this rationale, we carried out temperature-dependent magneto-transport measurements to investigate the nature of magnetic phase transition in the Mn_5Ge_3 nanowire. In particular, temperature-dependent resistance (R-T) measurements were performed on the Mn_5Ge_3 nanowire under various magnetic fields of 0 Oe, 45 kOe, and 90 kOe, as shown in Figure 3-2(a). The axial magnetic field $H_{//}$ was applied parallel to the nanowire growth direction, which is also the magnetic easy axis due to the shape anisotropy (to be discussed below). To exclude the contact resistance, a standard 4-probe measurement setup with lock-in technique was carried out in a Quantum Design physical property measurement system (PPMS). Under zero magnetic field ($H_{//}$ = 0 Oe), the Mn_5Ge_3 nanowire resistivity decreased from about 248 μΩ-cm at T = 375 K down to a residual resistivity of about 46.5 μΩ-cm at T = 2 K. Note that the non-zero residual resistivity here is mainly due to impurity scatterings.[146] The monotonic decrease in the resistance when reducing the temperature confirmed the metallic characteristic of Mn_5Ge_3, which was also reaffirmed by the fact that the nanowire resistance showed no dependence on the gate bias. Significantly, there is a clear transition in the R-T curve near $T = 300$ K as highlighted in the inset of Figure 3-2(a), which corresponds to the reported Curie temperature for Mn_5Ge_3 bulk materials and thin films (in the range of 296-304 K).[118-120,122,138] The slope change in the R-T curve near the Curie temperature may be attributed to the spin order-disorder transition and will be discussed in details later in this Chapter.[146] The resistivity change ratio (under zero magnetic field) below the Curie temperature, $\rho(300\ \mathrm{K})/\rho(2\ \mathrm{K}) \sim 5.2$, is much larger than that for a normal metal due to additional electron-magnon scatterings from the interaction between electron spins and local magnetic moments in the ferromagnetic Mn_5Ge_3 nanowire.[118,120,139] For comparison, the resistivity change ratio above the Curie temperature, $\rho(375\ \mathrm{K})/\rho(300\ \mathrm{K}) \sim 1.03$, is typically small and it is dominated by phonon scatterings and electron-electron scatterings. It is worth noting that the R-T curve measured in warming up (as the temperature increased from 2 K up to 375 K) shows no apparent difference from that measured in cooling down (as the temperature decreased from 375 K down to 2 K). The inset of Figure 3-2(a) magnifies the region of the R-T curves near the Curie temperature, again showing that there is no measurable thermal hysteresis. Such a feature indicates the absence of latent heat during the underlying phase transition near $T = 300$ K and is associated with a second-order magnetic phase transition in the

Mn$_5$Ge$_3$ nanowire.[143]

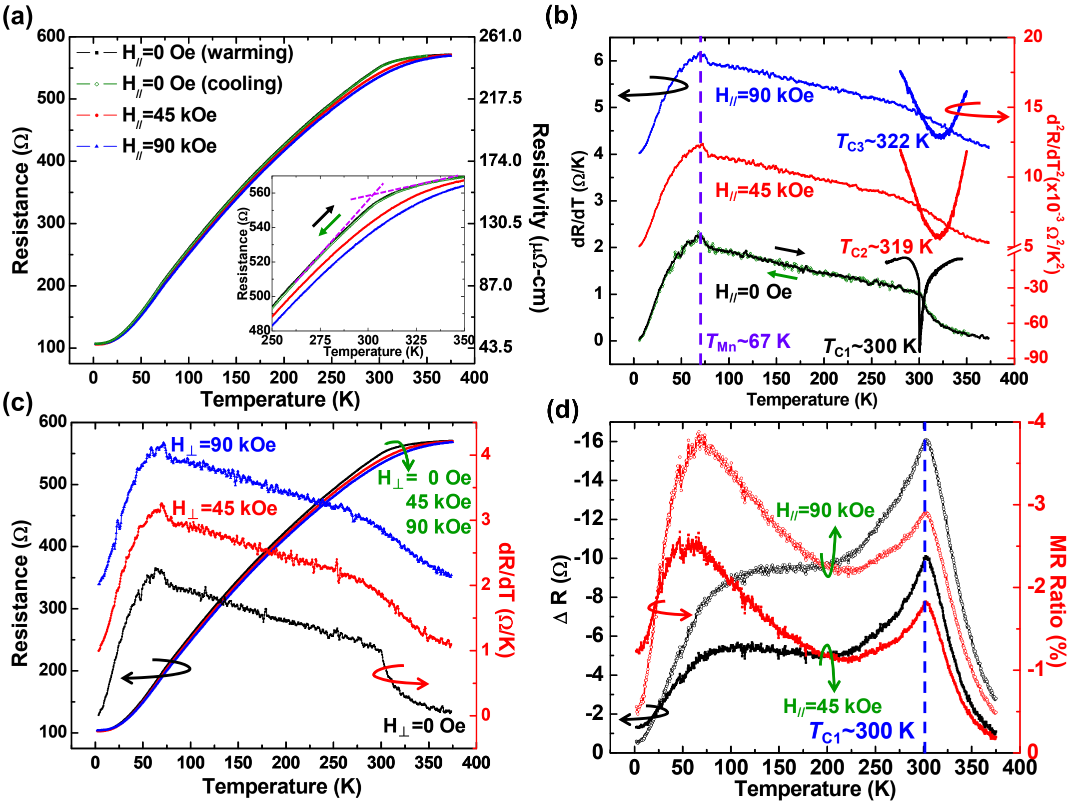

Figure 3-2. Temperature-dependent resistance (R-T) measurements on a single Mn$_5$Ge$_3$ nanowire under different axial and radial magnetic fields. (a) R-T curves under axial magnetic fields of 0 Oe (during both warming up and cooling down), 45 kOe and 90 kOe (during warming up) using a standard 4-probe measurement. The inset shows the enlarged view of the R-T curves near the Curie temperature of about 300 K. The arrows indicate the temperature sweeping directions and the dash lines indicate the slope change in R-T curves near 300 K. The black (warming up) and blue (cooling down) curves overlap each other, indicating a second-order magnetic phase

transition in the absence of latent heat. (b) First-order (left axis) and second-order (right axis) derivatives of the R-T curves. The peak positions in the second-order derivative correspond to the "effective" Curie temperature under the specific magnetic fields, respectively. It can be seen that the Curie temperature increases with increasing magnetic field, showing magnetic field-driven phase transitions. Curves under non-zero magnetic fields are intentionally offset. (c) R-T curves (left axis) and the corresponding first-order derivatives (right axis) under radial magnetic fields of 0 Oe, 45 kOe and 90 kOe. Curves of dR/dT under non-zero magnetic fields are intentionally offset. (d) Temperature-dependent resistance change (ΔR-T, left axis) and magnetoresistance (MR-T, right axis) under axial magnetic fields 45 kOe and 90 kOe extracted from R-T curves in (a) using $\Delta R(T) = R_H(T)-R_0(T)$ and $MR(T) = \Delta R(T)/R_0(T) \times 100\%$. (The data also appeared in my publication Ref. [140].[140])

Interestingly, the transition region near $T = 300$ K became smooth when a large axial magnetic field was applied during the temperature sweeping, as shown in the inset of Figure 3-2(a), which corresponds to the magnetic field-driven phase transition. Similar behaviors were observed in the R-T curves of Mn_4FeGe_3 single crystals,[147] and also in the temperature-dependent magnetization (M-T) curves of $Ge_{1-x}Mn_x$ thin films.[148] In order to reveal the magnetic field-driven phase transition more clearly, the first-order (dR/dT) and second-order derivatives (d^2R/dT^2) of the R-T curves under different magnetic fields were obtained as shown in Figure 3-2(b). The curves were intentionally offset for clarity. As indicated by the arrows, dR/dT curves under zero magnetic field during warming up (black) and cooling down (green) were both plotted to further affirm that there is no thermal hysteresis associated with the magnetic phase transition. The peak position of d^2R/dT^2 could be regarded as the "effective" Curie temperature, and it moved from T_{C1} = 300 K at $H_{//}$ = 0 Oe to T_{C2} = 319 K at $H_{//}$ = 45 kOe, and further to T_{C3} = 322 K at $H_{//}$ = 90 kOe. The magnetic field-driven phase transition can be simply understood as following: at zero magnetic field, magnetizations in the Mn_5Ge_3 nanowire are well aligned below the Curie temperature and the conduction electrons experience additional electron-magnon scatterings (as ρ varies with T^2 to the first-order approximation) besides to phonon (as ρ varies with T^5) and electron-electron scatterings (as ρ varies with T^2).[146] As the temperature is increased to be above the Curie temperature, Mn_5Ge_3 becomes paramagnetic and then phonon scatterings and electron-electron scatterings become the dominant scattering mechanism for conduction electrons. Reflected in the R-T curve is an abrupt slope change near the Curie temperature resulting from the vanishing magnetic orderings and scatterings in the Mn_5Ge_3 nanowire. However, if a magnetic field is applied during this process, as the temperature sweeps across the original Curie temperature, magnetizations are still aligned by the external magnetic field until a certain point at which the magnetizations become randomized again. The higher magnetic field is applied, the higher temperature can be magnetizations in the system maintain aligned.

In addition to the magnetic phase transition near the Curie temperature of Mn_5Ge_3, another interesting feature is that there is a cusp near T_{Mn} = 67 K in the dR/dT curves, and the effect of the axial magnetic field on this cusp, if any, is much smaller than that near the Curie temperature. Similar behavior was also observed in Mn_5Ge_3 thin films epitaxially grown on Ge (111) substrates, and the cusp position is consistent with the cusp in the dM/dT curve by taking the first-order derivative from the temperature-dependent magnetization curve.[118] Polarized neutron diffraction studies on the spatial distribution of the magnetization density in Mn_5Ge_3 revealed two crystallographically nonequivalent Mn sublattices, namely Mn_I and Mn_{II}, with two distinctive magnetic moments of 1.96 μ_B and 3.23 μ_B, respectively.[149] Density function calculations also suggested the coexistence of two energetically degenerate ferromagnetic states, collinear and non-collinear configurations, in the Mn_5Ge_3 lattice,[150] and the observed cusp in the dR/dT curves may be attributed to a possible magnetic transition between these two states. A similar scenario occurs in the anti-ferromagnetic Mn_5Si_3 that has the same crystal structure as Mn_5Ge_3. Indeed, it was reported that a magnetic transition from non-collinear to collinear anti-ferromagnetic spin states in bulk Mn_5Si_3 occurred at almost the same temperature of $T \sim 66$ K as in Mn_5Ge_3,[151-152] which was accompanied by a partial disorder of the magnetic moments carried by two different Mn_I and Mn_{II} sublattices.

The temperature-dependent resistance measurements under different radial (perpendicular to the nanowire axis) magnetic fields of 0 kOe, 45 kOe and 90 kOe were also performed on the Mn_5Ge_3 nanowire, as shown in Figure 3-2(c). The R-T curves here are almost identical to those under axial magnetic fields, showing a similar feature of magnetic field-driven phase transition. However, it is important to point out that the magnetic behavior under a small magnetic field (*i.e.*, near the coercivity field) for axial and radial directions could be different due to the shape anisotropy, as to be discussed in Figure 3. Furthermore, the temperature-dependent magnetoresistance ratio (MR-T) under axial magnetic fields of $H_{//}$ = 45 kOe and 90 kOe was obtained by MR(T) = $\Delta R(T)/R_0(T)$x100%, in which $R_0(T)$ is the temperature-dependent nanowire resistance under zero magnetic field; $\Delta R(T)$, the temperature-dependent resistance change, was obtained by $\Delta R(T) = R_H(T)-R_0(T)$. As shown in Figure 3-2(d), the Mn_5Ge_3 nanowire exhibits a negative MR in the whole temperature range due to the suppression of electron scatterings with an applied magnetic field. Again there are two characteristic features in the MR-T curves: one peak at the Curie temperature T_{C1} = 300 K corresponding to the magnetic phase transition of Mn_5Ge_3 and the other one at T_{Mn} = 67 K attributed to a possible magnetic transition between two collinear and non-collinear ferromagnetic states in Mn_5Ge_3.

In the as-fabricated ferromagnetic nanowires by both top-down lithographic method and bottom-up chemical synthesis, there are unavoidable crystalline defects or artificial structural constraints, which may act as domain wall pinning sites and alter the magnetization dynamics in the nanowire.[153-155] A similar scenario may also occur in our Mn_5Ge_3 nanowires. Also, as Mn atoms diffuse into and react with the Ge nanowire, appreciable strain would be built up in the Mn_5Ge_3 nanowire,[89,126,156] and the accumulated strain could also favor the nucleation of domain walls inside the nanowire. In order to investigate the domain wall dynamics, magneto-transport studies were performed on the Mn_5Ge_3 nanowire by sweeping the magnetic field at different temperatures. The results shown in Figure 3-3 (and the following discussion) indicate that the magnetization, or equivalently the easy axis, lies along the axial direction of the nanowire. The MR here is defined by MR = $(R_H-R_{max})/R_{max} x 100\%$, where R_{max} is the maximum nanowire resistance during magnetic field sweeps. Due to the shape anisotropy, the MR behavior under the axial (along the easy axis) and the radial (perpendicular to the easy axis) magnetic field is very different. For instance, Figure 3-3(a) plots the axial MR (top panel) and radial MR (bottom panel) at T = 20 K. The radial (in-plane) MR shows a regular hysteretic and smooth characteristic as the magnetic field sweeps back and forth between +30 kOe and -30 kOe. The negative MR ratio is about -1.5 % under $H_{\perp}$= 30 kOe, and the coercivity (regarded as the peak position by parabolic fitting near the maximum MR value) is about H_c = 230 Oe at T = 20 K. More interestingly, the axial (out-of-plane) MR shows clear features of abrupt jumps on top of regular hysteretic loops, as indicated by the blue and green arrows in Figure 3-3(a): as the magnetic field is swept from 3 kOe to -3 kOe (backward sweeping, black line), the nanowire resistance drops abruptly at H_1 = -723.0 Oe, followed by another abrupt decrease at H_2 = -871.4 Oe (green arrows); as the magnetic field is swept back to 3 kOe (forward sweeping, red line), the nanowire resistance drops abruptly at H_3 = 719.2 Oe, followed by another abrupt decrease at H_4 = 849.4 Oe (blue arrows), which are almost symmetric to H_1 and H_2. It is noted that the axial switching fields (719.2-871.4 Oe) are larger than the radial coercivity field of H_c = 230 Oe at T = 20 K, and also the axial MR ratio is about -0.6 % under $H_{//}$ = 3 kOe is larger than the value of about -0.3 % under a radial magnetic field $H_{\perp}$= 3 kOe.

These results are consistent with the previous statement that the easy axis is along the nanowire axial direction.

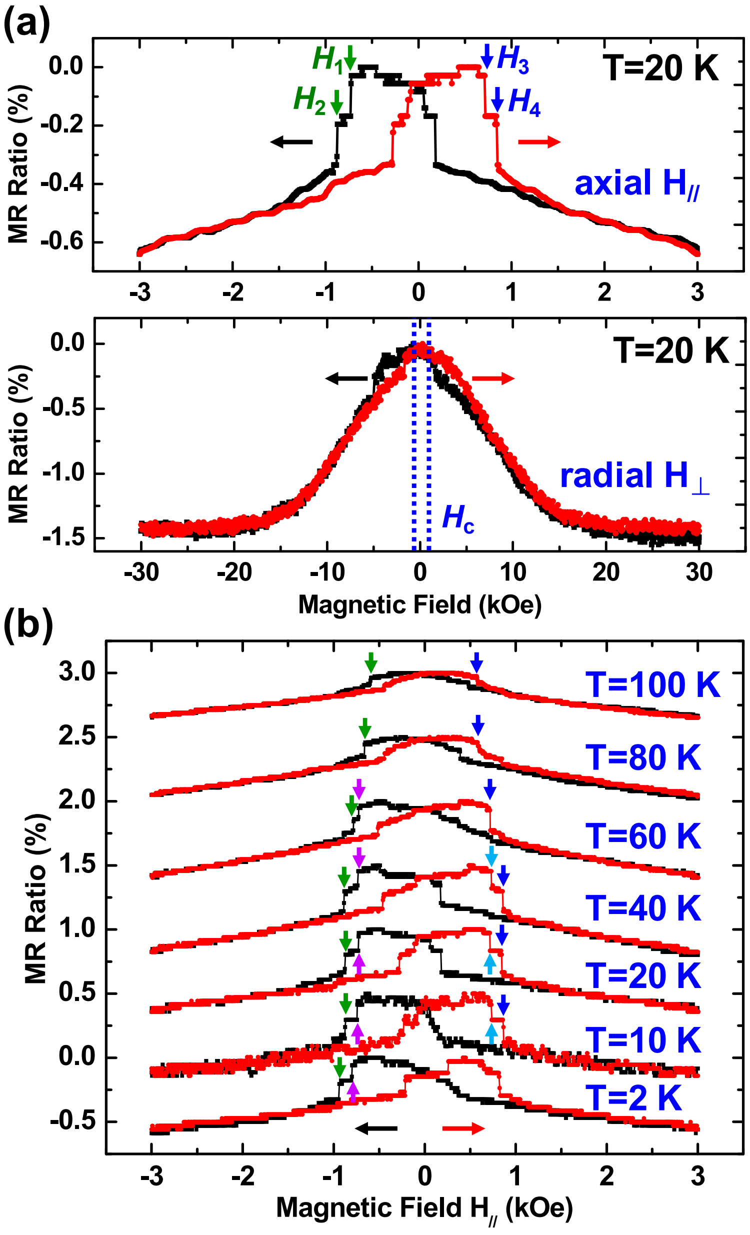

Figure 3-3. Magneto-transport measurements on a single Mn_5Ge_3 nanowire. (a) MR ratio of the Mn_5Ge_3 nanowire as a function of axial magnetic field (top panel) and

radial magnetic field (bottom panel) at T = 20 K. The black and red arrows indicate the sweeping direction of the magnetic field. The MR ratio here is defined as MR = $(R_H\text{-}R_{max})/R_{max}$x100%, similar to that in Figure 3-2. Both two MR data show ferromagnetic hysteresis during the magnetic field sweeping. Noticeably, unlike the relatively smooth change of the radial MR, the axial MR shows stepwise features. The abrupt jumps in the axial MR are indicated by the blue and green arrows as H_1 = -723.0 Oe, H_2 = -871.4 Oe, H_3 = 719.2 Oe, and H_4 = 849.4 Oe. The blue dash line indicates the radial coercivity field of H_c = 230 Oe in the radial MR. (b) MR ratio of the Mn_5Ge_3 nanowire as a function of the axial magnetic field at different temperatures. The blue (trace 1), green (trace 2), cyan (trace 3) and magenta (trace 4) arrows track the abrupt jumps in the MR curves when sweeping the magnetic field, suggesting the presence of multiple domain walls along with magnetic field-driven domain wall motion in the Mn_5Ge_3 nanowire. The MR curves at different temperatures are intentionally offset by multiples of 0.5%. The black and red arrows indicate the magnetic field sweeping directions. (The data also appeared in my publication Ref. [140].[140])

Now let us investigate more on the stepwise features in the axial MR and their temperature dependence. A physical picture of the abrupt jump in the nanowire resistance can be simply described as following: Initially a domain wall is pinned at a certain crystalline defect site inside the nanowire. As the magnetic field increases to a certain value (the so-called depinning field), the domain wall is moved out of the nanowire (or annihilated) as the defect is not able to hold it any more. This would give rise to an abrupt decrease (roughly by the amount of the domain wall resistance) in the measured nanowire resistance. Therefore, the observed multiple abrupt jumps in the axial MR are a strong evidence for the presence of multiple domain walls in the Mn_5Ge_3 nanowire along with magnetic field-driven domain wall motion. In a simplified model,[157-158] the domain wall depinning in a ferromagnetic nanowire can be described as the thermally assisted escape from a single energy barrier. The attempt rate, or inversely the depinning time of the domain wall, is given by the Kurkijärvi model:[153-155,157-159]

$$\tau^{-1} = {\tau_0}^{-1} \exp\left[-\frac{E(H)}{k_B T}\right] \qquad (3-1)$$

Here ${\tau_0}^{-1}$ is the attempt rate at zero temperature, k_B is the Boltzmann constant, and $E(H)$ is the magnetic field-dependent energy barrier. Under the assumption of uniaxial anisotropy, a coherently rotating magnetization, and neglect of interactions, a simple analytical approximation for $E(H)$ is given by:[160]

$$E(H) = E_0 \left(1 - \frac{H}{H_0}\right)^{1.5} \qquad (3-2)$$

in which E_0 is the energy barrier height under zero magnetic field and and H_0 is the domain wall escape field at zero temperature. Inserting Equation 2 into Equation 1 and considering a constant sweeping rate of the magnetic field would yield the temperature dependence of the escape field, or equivalently the depinning field:[157-158]

$$H_d(T) = H_0 \left\{1 - \left[\frac{k_B T}{E_0} ln \frac{{\tau_0}^{-1} k_B T}{1.5 \upsilon E_0 \sqrt{1 - H_d(T)/H_0}}\right]^{2/3}\right\} \qquad (3-3)$$

where υ=5 Oe/s is the magnetic field sweeping rate in this study. In order to extract the energy barrier height E_0 , temperature-dependent MR measurements were performed on the Mn_5Ge_3 nanowire, and the results are given in Figure 3-3(b), whose arrows track the abrupt jumps in the MR curves. The switching field of the last abrupt jump at each temperature is marked by blue and green arrows, regarding as the major depinning field. The temperature-dependent depinning fields are then re-plotted as solid symbols in Figure 3-4 (a) for both forward (trace 1, blue squares) and backward (trace 2, green dots) magnetic field sweepings. The solid lines are fitted curves using the above Kurkijärvi model. In Equation 3-3, only E_0 and H_0 are treated as the fitting parameters. The attempt rate τ_0 is typically in the range of 10^8-10^{12} Hz, and here we assume a constant value of $\tau_0{}^{-1}$ = 10^{10} Hz. The value of $H_d(T)/H_0$ varies roughly between 0.4 and 1.0 in the fitting temperature range of 50-150 K, and here an average value of 0.7 is used. The fitted E_0 (H_0) is 0.167 eV (990 Oe) and 0.165 eV (1062 Oe) for the forward and backward magnetic field sweepings, respectively. The values of the energy barrier height are very close for both magnetic field sweeping directions, consistent with the symmetric switching in the MR curves shown in Figure 3-3. It is worth noting that the fitted values of E_0 and H_0 are not sensitive to the given values for $\tau_0{}^{-1}$ and $H_d(T)/H_0$. The parameter changes in the range of 10^8 Hz $\leq \tau_0{}^{-1} \leq 10^{12}$ Hz and 0.4 $\leq H_d(T)/H_0 < 1$ would only lead to a variation within 15 % for the fitted value of E_0 and less than 1 % for that of H_0 as shown in Tables 3-1 and 3-2. Therefore, our fitting method using constant values for $\tau_0{}^{-1}$ and $H_d(T)/H_0$ are justified.

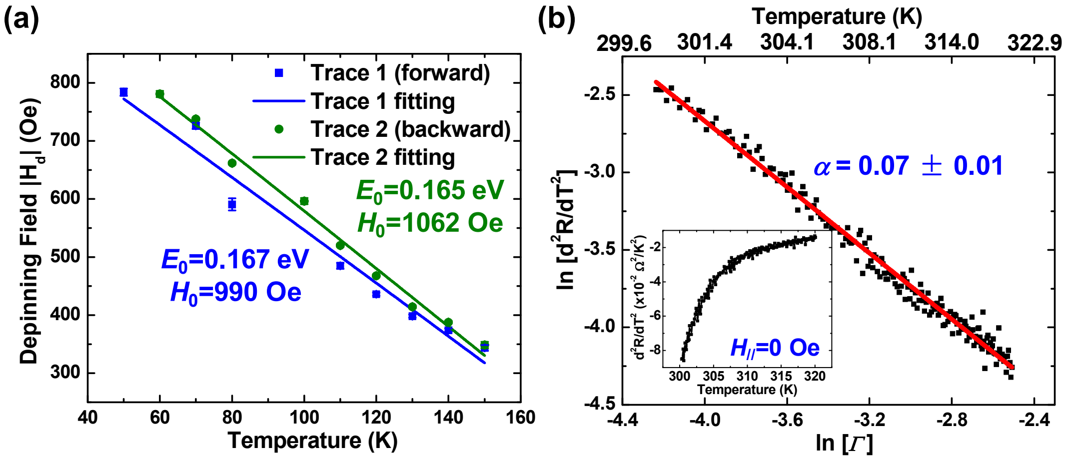

Figure 3-4. Extraction of the depinning energy barrier and critical exponent. (a) Temperature-dependent depinning fields extracted from the MR curves in the temperature range between 50 K and 150 K. Trace 1 (green squares) represents the depinning fields indicated by the green arrows in Figure 3(b), while trace 2 (blue dots) represents the depinning fields indicated by the blue arrows in Figure 3(b). The fittings (green and blue lines) using the Kurkijärvi model reveal a domain wall depinning energy barrier of 0.166±0.001 eV. (b) Linear fitting in the log-log plot of d^2R/dT^2 versus the reduced temperature $\Gamma = (T\text{-}T_C)/T_C$ in the temperature range of 300-320 K, yielding a critical exponent of $\alpha = 0.07\pm0.01$ in the power-law relation of $d^2R/dT^2 \propto \Gamma^{-(1+\alpha)}$. The inset shows the temperature-dependent d^2R/dT^2 curve near the Curie temperature under zero magnetic field. (The data also appeared in my publication Ref. [140].[140])

Table 3-1. Fitting results for forward magnetic field sweeping.

Trace 1	$\boldsymbol{\tau_0^{-1} = 10^8}$ **Hz**	$\boldsymbol{\tau_0^{-1} = 10^{10}}$ **Hz**	$\boldsymbol{\tau_0^{-1} = 10^{12}}$ **Hz**
$\boldsymbol{H_d/H_0=0.4}$	H_0=986 Oe E_0=0.146 eV	H_0=992 Oe E_0=0.165 eV	H_0=993 Oe E_0=0.184 eV
$\boldsymbol{H_d/H_0=0.7}$	H_0=989 Oe E_0=0.147 eV	**H_0=990 Oe** **E_0=0.167 eV**	H_0=994 Oe E_0=0.185 eV
$\boldsymbol{H_d/H_0=0.99}$	H_0=987 Oe E_0=0.155 eV	H_0=991 Oe E_0=0.174 eV	H_0=993 Oe E_0=0.192 eV

Table 3-2. Fitting results for backward magnetic field sweeping.

Trace 2	$\boldsymbol{\tau_0^{-1} = 10^8}$ **Hz**	$\boldsymbol{\tau_0^{-1} = 10^{10}}$ **Hz**	$\boldsymbol{\tau_0^{-1} = 10^{12}}$ **Hz**
$\boldsymbol{H_d/H_0=0.4}$	H_0=1060 Oe E_0=0.144 eV	H_0=1060 Oe E_0=0.164 eV	H_0=1059 Oe E_0=0.183 eV
$\boldsymbol{H_d/H_0=0.7}$	H_0=1057 Oe E_0=0.146 eV	**H_0=1062 Oe** **E_0=0.165 eV**	H_0=1061 Oe E_0=0.184 eV
$\boldsymbol{H_d/H_0=0.99}$	H_0=1060 Oe E_0=0.153 eV	H_0=1062 Oe E_0=0.172 eV	H_0=1064 Oe E_0=0.190 eV

Finally, in order to understand the nature of the second-order magnetic phase transition at the Curie temperature, the d^2R/dT^2 curve of the Mn_5Ge_3 nanowire under

H = 0 Oe was revisited, as shown in the inset of Figure 3-4(b). The critical behavior near the transition temperature can be described with the universal scaling hypothesis, which consists of a set of equations that relate various critical-point exponents.[161] For example, a simple scaling law $\alpha + 2\beta + \gamma = 2$ relates the exponents α, β and γ describing the specific heat $C_p \sim |\Gamma|^{-\alpha}$, the magnetization $M \sim |\Gamma|^{\beta}$ and the isothermal susceptibility $\chi_T \sim |\Gamma|^{-\gamma}$ as T approaches T_C. Here Γ = (T-T_C)/T_C is the reduced temperature. Those exponents offer a systematic characterization of underlying phase transitions, which can be accordingly categorized into different universality classes, such as two-dimensional (2D) Ising, three-dimensional (3D) Heisenberg, as well as mean field theory models, despite of different structures and transition temperatures.[161-162] As discussed previously, the revelation of the critical behavior from the magnetization information is prevented in the present system, resulting from the weak magnetic signal from an individual Mn_5Ge_3 nanowire. In conventional ferromagnetic metals, the specific heat curve is proportional to the dR/dT curve at the critical point,[163-164] since the same electron scattering mechanism in the spin-spin correlation would dominate both dR/dT and the specific heat as T tends to T_C from above.[146] In other words, the critical exponent α in the specific heat is the same as that in dR/dT, which has been experimentally verified in various material systems such as iron and gadolinium.[165-166] Assuming this relation holds, here we discuss an alternative approach to obtain the critical exponent α from the resistance anomaly near the magnetic phase transition,[167] which can be characterized by a power-law relation, as derived from the scaling hypothesis function:[168]

$$\frac{dR}{dT} = \frac{A}{\alpha}(\Gamma^{-\alpha} + 1) + B, \qquad T > T_C \qquad (3-4)$$

or

$$\frac{d^2R}{dT^2} = -\frac{A}{T_C}\Gamma^{-(1+\alpha)}, \qquad T > T_C \qquad (3-5)$$

As shown in Figure 3-4(b), the linear fitting in the log-log plot of d^2R/dT^2 versus Γ in the temperature range of 300-320 K yields a critical exponent of $\alpha = 0.07 \pm 0.01$. Noted that, this value dramatically deviates from both the long-range mean field model ($\alpha = 0$) and the nearest neighbor 3D Heisenberg model ($\alpha = 0.134$).[162] Also, the 1D Ising model, describing an ideal 1D lattice, has no phase transition, hence clearly it does not apply to our system. This deviation may arise from the variation of dimensionality from 3D in bulk systems to 1D in nanowires, which clearly requires further theoretical justification. Noted that similar deviation from theoretical models was also reported in the acquisition of another critical exponent β from temperature-dependent magnetization measurements on 2D Mn_5Ge_3 thin films,[118] and it was attributed to the finite size effect.[169] Nevertheless, our experimental results offer a practical approach to investigate the nature of magnetic phase transitions in 1D systems through electrical transport measurements.

In conclusion, this work presented a systematic study on the electrical transport study of magnetic phase transition and domain wall motion in a ferromagnetic Mn_5Ge_3 nanowire. The single-crystalline Mn_5Ge_3 nanowire was fabricated through the thermal reaction between a Ge nanowire and Mn contacts, which fully converted the Ge nanowire into a Mn_5Ge_3 nanowire upon RTA at 450 ^{o}C. R-T measurements on the Mn_5Ge_3 nanowire were performed to electrically probe the magnetic phase transition at the Curie temperature of about 300 K. The nature of the critical behavior accompanied with this phase transition was characterized using a power-law relation in d^2R/dT^2 with a critical exponent of $\alpha = 0.07 \pm 0.01$. Magnetic field-driven phase transition was also demonstrated with applied axial and radial magnetic fields of 45 kOe and 90 kOe, and the effective Curie temperature was increased to about 319 K and 322 K, respectively. Besides, a possible magnetic transition between non-collinear and collinear ferromagnetic states in the Mn_5Ge_3 lattice resulted in a cusp feature in the dR/dT and MR-T curves. Significantly, the domain wall dynamics in the Mn_5Ge_3 nanowire were investigated by temperature-dependent MR studies. Unlike the relatively smooth change in the radial MR, the axial MR showed symmetric stepwise features, in which the abrupt jumps in the nanowire resistance were attributed to the magnetic field-driven domain wall motion in the Mn_5Ge_3 nanowire. From the temperature-dependent depinning field, the energy barrier was estimated to be about 0.166 eV based on the Kurkijärvi model that describes the field-driven domain wall depinning as thermally assisted escape from a single energy barrier. This magneto-transport study on the Mn_5Ge_3 nanowire advances the fundamental understanding of its ferromagnetic properties, including the magnetic phase transition and domain wall motion. Therefore, this work serves as an important step toward the realization of electrical spin injection from Mn_5Ge_3 into Ge in the Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire transistor and further to build Ge nanowire-based spinFETs, which will be discussed in the following Chapter 3.3.

3.3 Electrical Spin Injection and Detection in $Mn_5Ge_3/Ge/Mn_5Ge_3$ Nanowire Transistors

In the building of semiconductor-based spintronic devices, such as spinFET and spinLED,[2,5-6] one of the key issues is to realize an efficient spin injection from a ferromagnetic metal into a semiconductor. Electrical spin injection into various semiconductors, including Si,[23-24] Ge,[21,56] GaAs,[42,48] and graphene,[38-39] has attracted numerous research efforts in the past two decades. While the electrical spin injection into ordinary metals can be easily demonstrated in metallic spin valve structures,[20,22] the realization of efficient spin injection into semiconductors is much complicated by several factors: 1) the huge difference in the conductivity between ordinary ferromagnetic metals and semiconductors would almost make the spin injection efficiency negligibly small, the well-known conductivity mismatch problem;[110] 2) the increase in the doping concentration in order to reduce such a conductivity difference, however would decrease the carrier spin lifetime due to the aggravated spin relaxation originating from impurity scatterings;[2,31] 3) while the insertion of a tunneling or Schottky barrier helps alleviate the conductivity mismatch,[128-129] the preparation of a high-quality tunneling oxide without pinholes or a defects-free Schottky contact without Fermi-level pinning is not easy.[111,130] Also, the localized states at the FM/SC interface and the surface roughness could significantly complicate and jeopardize the spin injection process.[27] Therefore, the preparation of high-quality FM/SC structures is a key step towards realizing efficient spin injection into semiconductors. In an earlier work as described in the previous Chapter, we were able to fabricate single-crystalline Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire transistors using a simple RTA process,[126] in which the formed Mn_5Ge_3 Schottky contacts maintained atomically clean interfaces with Ge nanowires and the Mn_5Ge_3 nanowire exhibited ferromagnetic orderings up to room temperature.[140] It should be pointed out that the Curie temperature of Mn_5Ge_3 can be further increased up to 445 K with appropriate carbon doping,[122] in order to build practical spintronic devices that can operate at room temperature. Moreover, such one-dimensional high-quality germanide/Ge contacts formed by RTA were found to effectively alleviate the Fermi level pinning as discussed previously in Chapter 2.5,[127] for which conventional metal/Ge contacts were suffered.[133] This should allow us to probe the intrinsic spin property in the Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire transistor. Indeed, with a high spin polarization,[120] Mn_5Ge_3 has been theoretically predicted to be a high-efficient spin injection source into Ge.[121] In this section, we demonstrate the spin injection into Ge nanowires through Mn_5Ge_3 source/drain contacts in Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire transistors. We also study the bias effect and the temperature dependence of the spin transport, revealing a weak temperature dependence for the spin diffusion length of about 480 nm and the spin lifetime exceeding 244 ps in degenerately *p*-doped Ge nanowires. These numbers in Ge nanowires are much larger than those reported in bulk Ge with a similar doping level,[34] which can be attributed to the significant suppression of spin relaxation because of quantum confinements in nanostructures, as previously discussed in Chapter 1.4.

To start, single-crystalline Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire transistors were fabricated on a Ge nanowire with Mn metal contacts using a RTA process, as previously described in a prior work in Chapter 2.4 (also appeared in my publication Ref. [126]).[126] The formed Mn_5Ge_3/Ge heterostructure with an atomically clean interface formed upon 450 °C RTA provides a defects-free FM/SC structure for electrical spin injection. The Schottky barrier for the Mn_5Ge_3 contact to a *p*-type Ge nanowire was determined to be about 0.25 eV from temperature-dependent *I-V* measurements, as discussed earlier in Chapter 2.4.[126] To overcome the fundamental obstacle of conductivity mismatch,[110] heavily-doped Ge nanowires were required in this study in order to achieve appreciable spin injection from the ferromagnetic Mn_5Ge_3 contact into the Ge nanowire. In the previous work (Chapter 2), as-grown Ge nanowires were not intentionally doped during the vapor-liquid-solid growth process.[123] Here in order to introduce a high doping density, as-grown Ge nanowires were exposed in an indium ambient at about 600 °C inside an ultrahigh-vacuum MBE chamber for 2 hours to drive indium atoms diffusing into Ge nanowires as *p*-type dopants, prior to being transferred onto SiO_2/Si substrates for device fabrication. The Ge nanowire morphology was inspected with TEM to ensure that the Ge nanowire maintained the cubic crystal structure after incorporating indium doping, as shown in Figure 3-5. Furthermore, the EDS spectrum (resolution of about 0.1% atomic concentration) of indium-doped Ge nanowires shown in Figure 3-6 revealed a very small peak of indium, affirming the successful incorporation of indium dopants into the Ge lattice.

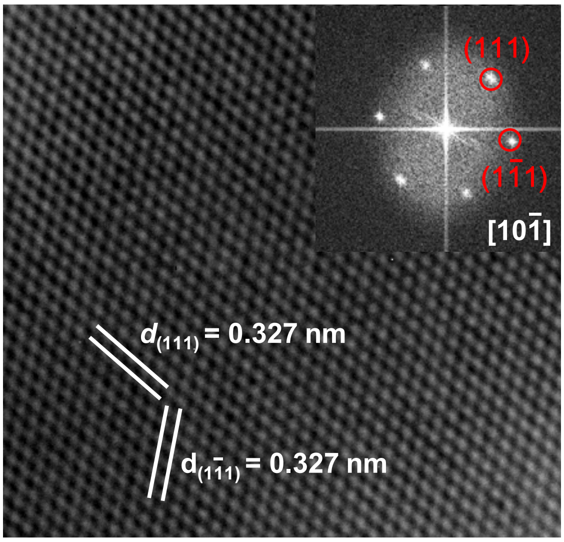

Figure 3-5. High-resolution TEM image and corresponding diffraction pattern of indium-doped Ge nanowires. (The data also appeared in my publication Ref. [7].[7])

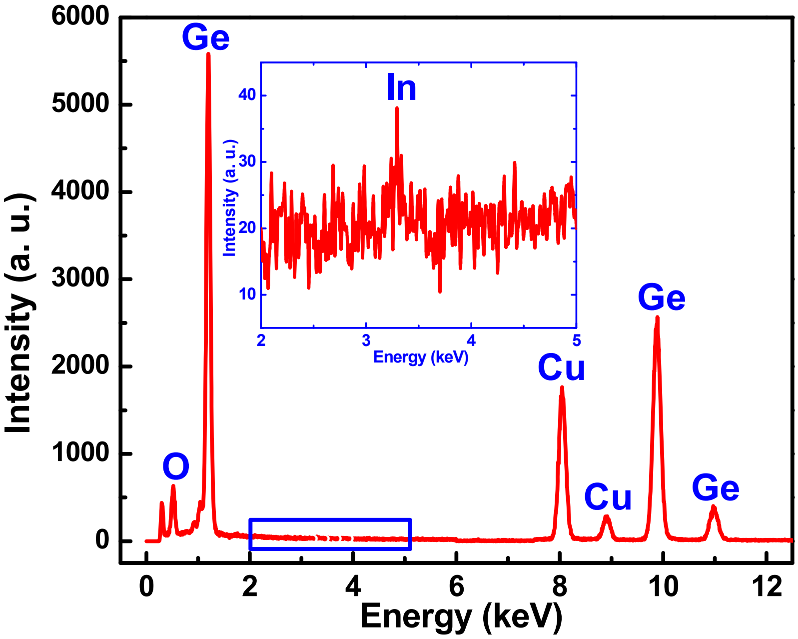

Figure 3-6. EDS spectrum of indium-doped Ge nanowires. The inset shows the

zoom-in spectrum near the indium peak position. The Cu peak originated from the TEM sample holder. (The data also appeared in my publication Ref. [7].[7])

Figure 3-7(a) schematically illustrates the device structure, in which the ferromagnetic Mn_5Ge_3 nanowire contacts were formed upon 450 °C RTA. Figure 3-7(b) shows the optical microscope images of multiple as-fabricated Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire transistors after transferring indium-doped Ge nanowires onto a SiO_2/Si substrate. No scanning electron microscope (SEM) image was taken to avoid undesirable damages on the device by the high-energy electron beam; however it was expected to be similar to the prior work.[126] The Si substrate was degenerately doped and used as a back-gate electrode while the 300 nm-thick SiO_2 layer grown on top by thermal oxidization served as the gate dielectric. Figure 3-7(c) shows the I_{DS}-V_{GS} curves of three Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire transistors with different channel lengths (L_{ch} = 450, 550, and 700 nm) under V_{DS} = 10 mV measured in the room-temperature ambient. They all showed a similar *p*-type transistor behavior with a field-effect hole mobility of about μ_h = 10 cm^2/Vs, which was calculated from the transconductance as discussed in prior works.[86,89,93]

As shown in Figure 3-8, it was noted that the Ge nanowire transistors showed about one order of magnitude improvement in the carrier mobility after RTA at 450 °C, and such an improvement was attributed to the formation of high-quality Mn_5Ge_3 source/drain contacts after annealing.[93] Compared with the reported performance of Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire transistors built on as-grown Ge nanowires,[126] the devices here showed a much lower hole mobility and a smaller current ON/OFF ratio while with a higher nanowire conductance. This result may come from the use of a high concentration of indium doping in the Ge nanowire, due to the fact that it is difficult to deplete a heavily doped semiconductor and the high-concentration dopants drastically degrade the carrier mobility through impurity scatterings.[170] To quantitatively evaluate the Ge nanowire resistivity and the indium doping concentration, temperature-dependent resistance measurements were performed on a Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire transistor with a channel length of L_{ch} = 700 nm and with a diameter of about 60 nm. A standard 4-probe measurement setup with a lock-in technique was used to exclude the contact resistance and improve the signal-to-noise ratio in the measurement. The measurement setup is illustrated in Figure 3-7(a). As shown in Figure 3-7(d), the Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire transistor exhibited a monotonically decreasing resistance with decreasing temperature down to T = 2 K. This behavior reaffirmed the degenerate doping in the Ge nanowire, in which case the dominated impurity scattering was effectively screened by the high-density free carriers.[171] The first-order derivative of the 4-probe resistance with respect to the temperature (dR/dT) was also plotted in the inset of Figure 3-7(d), showing a smooth change from 250 K to 350 K from the Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire transistor. Compared with the clear cusp in the dR/dT curve near T_C =300 K for the Mn_5Ge_3 nanowire in the previous section (also re-plotted in the inset of Figure 3-7(d) for comparison),[140] this result suggested that the part of the resistance from the Mn_5Ge_3 source/drain was small and most of the measured resistance came from the Ge nanowire channel. Quantitatively, using the previously measured resistivity value for the Mn_5Ge_3 nanowire,[140] we calculated that the Mn_5Ge_3 contacts only contributed to less than 3% of the total Mn_5Ge_3/Ge/Mn_5Ge_3 resistance. Therefore, for simplicity, we assumed the measured total resistance equaled to the Ge nanowire channel resistance. Then the resistivity of the Ge channel was calculated to be $\rho_{\mathrm{Ge}} = 2.58\times10^{-3}$ Ω-cm at $T = 300$ K and decreased slightly to $\rho_{\mathrm{Ge}} = 2.22\times10^{-3}$ Ω-cm at $T = 2$ K. On the other hand, the previously reported resistivity values for the Mn_5Ge_3 nanowire were $\rho_{\mathrm{FM}} = 2.4\times10^{-4}$ Ω-cm at $T = 300$ K and decreased to $\rho_{\mathrm{FM}} = 4.65\times10^{-5}$ Ω-cm at $T = 2$ K.[140] The conductivity ratio (inversely the resistivity ratio), $\sigma_{\mathrm{FM}} / \sigma_{\mathrm{Ge}} = \rho_{\mathrm{Ge}} / \rho_{\mathrm{FM}}$, of the Mn_5Ge_3/Ge heterostructure was then evaluated to be between 10 and 50 in the temperature range of 2-300 K. This value is more than 20 times smaller than that of ordinary FM/Ge (eg. Fe/Ge, Co/Ge) spin injection structures, given that the resistivity of commonly used ferromagnetic metals is typically on the order of 10^{-6} to 10^{-5} Ω-cm, or at least 20 times lower than that of Mn_5Ge_3.[172] Therefore, compared with ordinary FM/Ge structures, the conductivity mismatch in the Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire transistor should be significantly reduced to facilitate the spin injection into Ge. It is also worth mentioning that the spin polarization in Mn_5Ge_3 was experimentally reported to be about $P_{\mathrm{FM}} = 42\%$ at $T = 1.2$ K,[120] which is comparable with that of conventional ferromagnetic metals (for instance, $P_{\mathrm{Fe}} = 45\%$, $P_{\mathrm{Co}} = 42\%$ and $P_{\mathrm{Ni}} = 33\%$).[173] The relatively low conductivity and high spin polarization of Mn_5Ge_3, along with the atomically clean interfaces with Ge nanowires, suggests that Mn_5Ge_3 is a promising ferromagnetic material for spin injection into Ge nanowires.

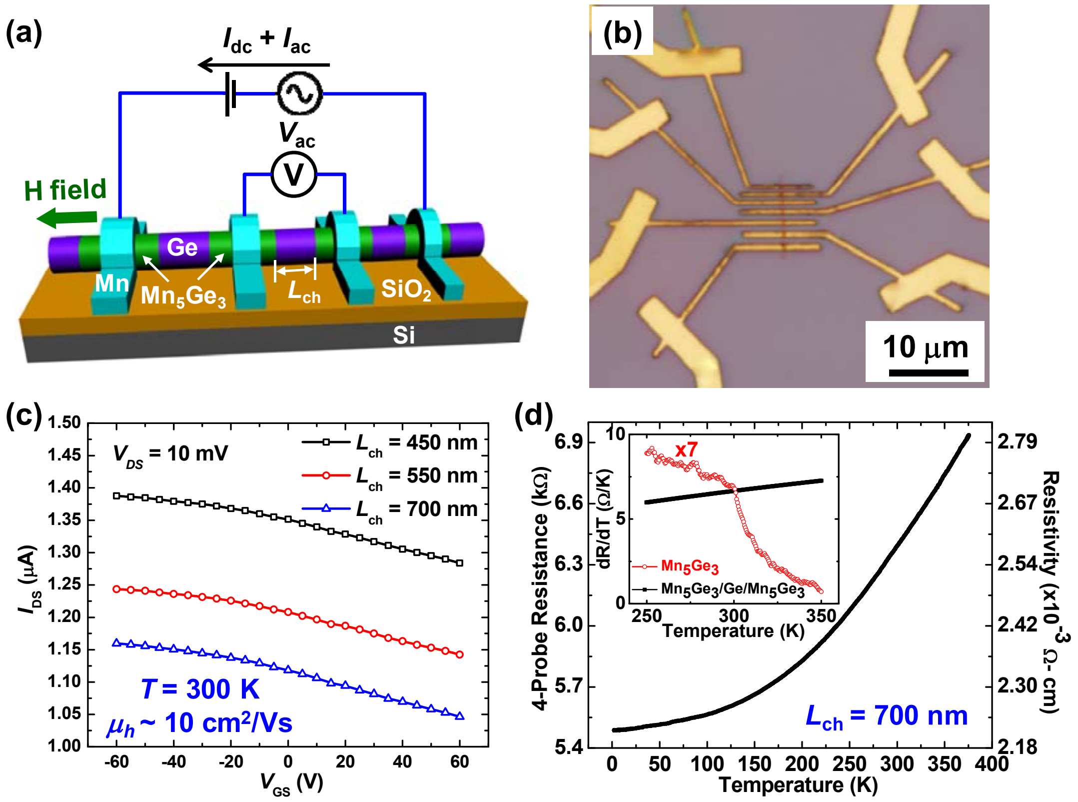

Figure 3-7. Characterization of single-crystalline indium-doped Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire transistors. (a) Schematic illustration of Ge nanowire transistors with thermally formed Mn_5Ge_3 as Schottky source/drain contacts. The setup for a standard 4-probe measurement is also illustrated. The magnetic field for the following measurements in this study was applied along the nanowire axial direction. (b) Optical microscope image of multiple as-fabricated Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire transistors on a SiO_2/Si substrate. (c) I_{DS}-V_{GS} curves of three Ge nanowire transistors with different channel lengths (L_{ch} = 450, 550, and 700 nm) with V_{DS} = 10 mV, showing a p-type transistor behavior with a field-effect hole mobility of about 10 cm^2/Vs. (d) 4-Probe resistance-temperature (R-T) measurement on the

Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire transistor with a channel length of L_{ch} = 700 nm, showing a decreasing resistance with the decreasing temperature. This confirms the degenerate indium doping in the Ge nanowire. The inset shows the first-order derivative of the R-T curve (black curve), showing a smooth transition near T = 300 K. For comparison, the data of a Mn_5Ge_3 nanowire (red curve, multiplied by a factor of 7) is also plotted here. (The data also appeared in my publication Ref. [7].[7])

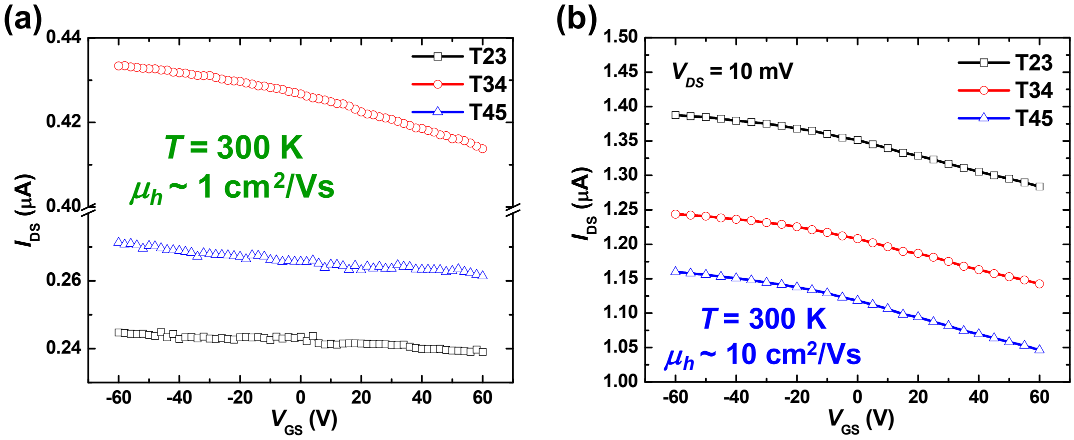

Figure 3-8. I_{DS}-V_{GS} curves of three indium-doped Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire transistors under V_{DS} = 10 mV (a) before and (b) after RTA. (The data also appeared in my publication Ref. [7].[7])

In the characterization of spin injection and transport, Hanle precession measurement is widely used to extract the spin lifetime and spin diffusion length, as previously discussed in Chapter 1.2.[20] Usually nonlocal measurements with a four-terminal geometry are adopted to detect the intrinsic spin injection signal in order to avoid any spurious signals.[26] Unfortunately, this technique could not be used for our

Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire transistor This is because that the Ge nanowire channel is not continuous but isolated into segments by the ferromagnetic Mn_5Ge_3 contacts, hence spin-polarized carriers injected from one ferromagnetic Mn_5Ge_3 contact cannot diffuse away from the current loop because this path is blocked by the Mn_5Ge_3 contact. Alternatively, we may use the Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire transistor as a vertical spin valve with a current perpendicular-to-plane configuration.[174-175] In this case, spin-polarized carriers are injected into the Ge nanowire from one ferromagnetic Mn_5Ge_3 contact (namely the spin injector) and then are scattered as they travel along the Ge nanowire channel before reaching the other ferromagnetic Mn_5Ge_3 contact (namely the spin detector). This process will be discussed in details later (illustrated in Figure 3-9(d)). For non-polar semiconductors like Ge, the dominant spin relaxation mechanism is the Elliot-Yafet spin flip mechanism that occurs when scattered with phonons and impurities.[2] In experiment, a constant dc bias current superimposed with a small ac current of I_{ac} = 1 μA was flowed through the Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire transistor, and the ac voltage signal was sensed with a lock-in technique was used while sweeping the axial magnetic field. The easy-axis of the Mn_5Ge_3 nanowire was found to be along the nanowire axis, and the two ferromagnetic Mn_5Ge_3 contacts were intentionally designed to have different lengths and hence possibly different coercive fields. As the axial magnetic field was swept back and forth between -30 kOe and 30 kOe, the relative magnetization directions of the spin injector and the spin detector were changed between parallel and anti-parallel configurations.

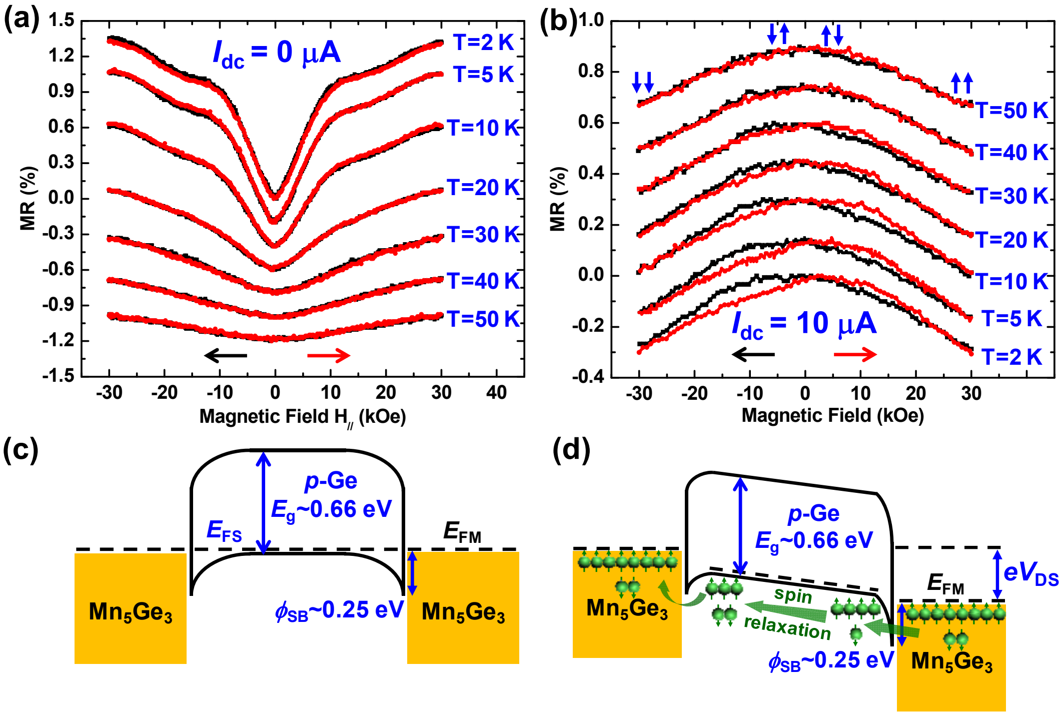

Figure 3-9. MR loops of a Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire transistor with a channel length of L_{ch} = 700 nm at different temperatures from 2 K to 50 K under a dc current bias of (a) I_{dc} = 0 μA and (b) I_{dc} = 10 μA, respectively. The black and red arrows indicate the backward and forward sweeping directions of the axial magnetic field between -30 kOe and 30 kOe, respectively. For clarity, MR curves in (a) and (b) are intentionally offset by multiples of 0.2% and 0.15%, respectively. The Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire transistor showed positive MR curves with no apparent hysteresis under zero dc bias (I_{dc} = 0 μA) while negative and hysteretic MR curves under a large dc bias (I_{dc} = 10 μA), as explained in the text. The blue arrows in (b) indicate the relative magnetization directions of the Mn_5Ge_3 spin injector and the spin

detector. Energy band diagrams of the Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire transistor under zero and large dc bias are shown in (c) and (d), respectively. The transport process of spin-polarized carriers (holes) in the Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire transistor is also illustrated in (d). (The data also appeared in my publication Ref. [7].[7])

Figures 3-9(a-b) show the MR of a Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire transistor with a channel length of L_{ch} = 700 nm under two different dc current biases in the temperature range from 2 K to 50 K. The MR here is defined as $MR = \frac{R(\mathrm{H})-R_{min}}{R_{min}} \times 100\%$ (positive MR) for Figure 2(a), and $MR = \frac{R(\mathrm{H})-R_{max}}{R_{max}} \times 100\%$ (negative MR) for Figure 2(b), similar to that in Figure 3-3 of Chapter 3.2. It is interesting to observe that the MR curves under a zero and a high dc bias current showed distinct characteristics: positive MR with no apparent hysteresis with I_{dc} = 0 μA while there is a negative and hysteretic MR under I_{dc} = 10 μA. It should be pointed out that, while the positive MR under I_{dc} = 0 μA is likely attributed to the anomalous longitudinal MR of Ge,[176] the bias-dependent MR characteristics could not originate from the Ge nanowire, the Mn_5Ge_3 contact and associated anisotropy magnetoresistance (AMR, see Figure 3-10 below for detailed explanation). The bias effect on the MR behavior can be simply explained from the energy band diagram schematically shown in Figures 3-9(c-d): since there is a Schottky barrier height of about 0.25 eV for the ferromagnetic Mn_5Ge_3 contact to the *p*-type Ge nanowire (as previously discussed in Chapter 2.4),[126] a large enough dc bias voltage (current) is required to reduce the

Schottky barrier width in the reverse biased spin injector terminal to allow for sufficient spin-polarized carriers being injected into the Ge nanowire channel, and moving towards the spin detector. The transport process of spin-polarized carriers in the Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire transistor is also schematically illustrated in Figure 3-9(d). As shown in Figure 3-9(b), with a dc current bias of $I_{dc} = 10\ \mu A$, we were able to observe the negative and hysteretic MR from $T = 2$ K up to $T = 50$ K, unambiguously demonstrating the spin injection and detection in Ge nanowires transistors. It is worth noting that similar bias effect on the MR behavior was also observed in the MnSi/Si/MnSi nanowire heterostructure, in which spin-polarized carriers were injected from the Schottky MnSi contact into the *p*-type Si nanowire.[57]

In our analysis, we try to carefully exclude other spurious signals from the Ge nanowire, the Mn_5Ge_3 contact and associated AMR, which cannot explain the bias-dependent MR data shown in Figure 3-9.

(1) The Ge nanowire itself could contribute to the MR signal; however, the longitudinal MR of *p*-Ge is typically positive,[176] so it would not contribute to the negative and hysteretic MR in Figure 3-9(b). Also, the change in the current bias would not result in the change of its MR polarity.

(2) The ferromagnetic Mn_5Ge_3 contact would contribute to a hysteretic MR signal; however, the contribution to the total device resistance from the Mn_5Ge_3 contact is very small. Using the resistivity value measured in our previous work,[140] the Mn_5Ge_3 contacts with lengths of 550-700 nm in the present device would have resistances of 90-170 Ω at low temperatures ($T \leq 50$ K), which contribute to less

than 3% of the total Mn_5Ge_3/Ge/Mn_5Ge_3 resistance. This is consistent with our conclusion drawn from Figure 3-7(d). Considering the MR amplitude of the Mn_5Ge_3 contact is also very small (less than 2% for $H_{//}$ = 30 kOe and T ≤ 50 K), the contribution from the Mn_5Ge_3 contact in the MR signal of the present Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire device is negligible.

(3) AMR describes that the resistance of ferromagnetic materials is dependent on the angle between the current flow direction and the orientation of the magnetization. In general, the resistance reaches the maximum when the current flow is parallel to the magnetization direction, while it reaches the minimum when the two are orthogonal.[177] Typical AMR signals have opposite peaks for magnetic fields parallel and perpendicular to the current direction, and an example from a GaAs/MnAs core/shell nanowire is shown in Figure 3-10(a).[178] To exclude this effect, we have measured the MR of a Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire transistor with both radial (perpendicular to the nanowire axis, $H \perp I$) and axial (parallel to the nanowire axis, H // I) magnetic fields, as shown in Figure 3-10(b). The radial and axial MR curves show similar characteristics, in which the two peaks are in the same direction, and the minimum (maximum) resistance state of the Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire transistor is reached when the two ferromagnetic Mn_5Ge_3 contacts are in parallel (anti-parallel) configuration. This result clearly indicates that the AMR signal is excluded in our measurements.

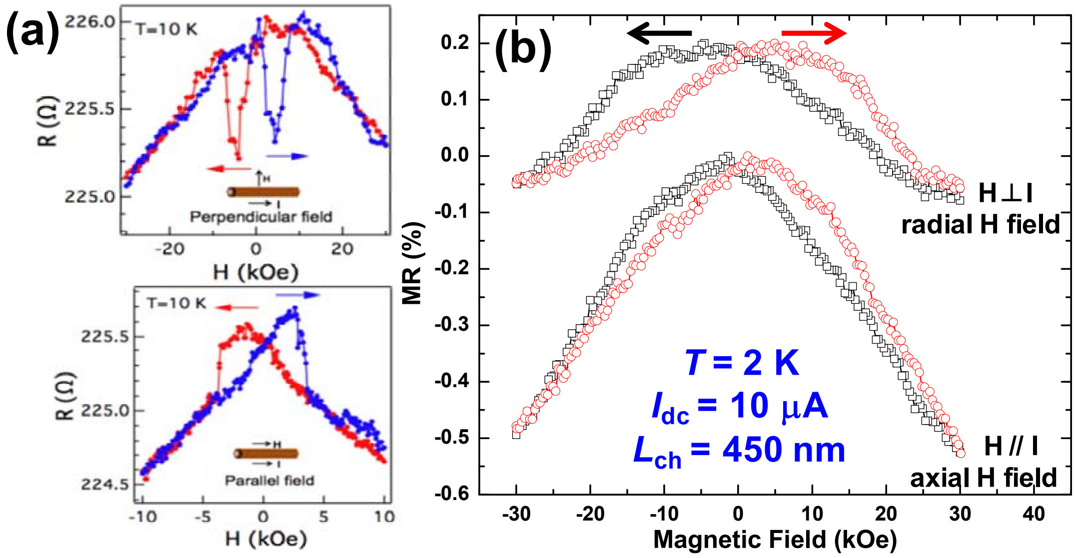

Figure 3-10. MR under in-plane and out-of-plane magnetic fields. (a) Typical AMR curves of a GaAs/MnAs core/shell nanowire, adopted from Liang, *et al.*[178] (b) MR curves of a Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire transistor with a channel length of L_{ch} = 450 nm at T = 2 K under a dc current bias of I_{dc} = 10 μA. Top branch: the magnetic field was applied perpendicular to the nanowire axis (out of plane); Bottom branch: the magnetic field was applied along the nanowire axis. The black and red arrows indicate the backward and forward sweeping directions of the magnetic field, respectively. For clarity, the radial MR curves are intentionally offset by 0.2%. (The data also appeared in my publication Ref. [7].[7])

To quantitatively determine the spin diffusion length, temperature-dependent MR measurements were performed on several Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire transistors with different channel lengths. Figure 3-11(a) shows the MR curves of three Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire transistors with three different channel lengths (L =

450, 550, and 700 nm) at T = 10 K under the same dc current bias of I_{dc} = 10 μA. They showed similar negative and hysteretic characteristics with a systematic decrease in the MR magnitude with the increasing Ge nanowire channel length. Recalling the Julliere's model for a FM/insulator/FM structure,[179] the tunneling magnetoresistance (TMR) is given by:

$$\mathrm{TMR} = \frac{2P_1P_2}{1+P_1P_2} \qquad (3-6),$$

Here P_1 and P_2 are the spin polarizations of the two FM electrodes defined as $P = \frac{N_\uparrow - N_\downarrow}{N_\uparrow + N_\downarrow}$, in which $N_\uparrow$ ($N_\downarrow$) is the density of states at the Fermi level for the majority (minority) spin direction . In our Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire structure with a fairly long Ge channel, the Julliere's model of TMR can be modified as follows to include the spin relaxation in the Ge nanowire:[175]

$$\mathrm{TMR} = \frac{2P_1P_2e^{-\frac{L_{ch}}{l_{sf}}}}{1+P_1P_2e^{-\frac{L_{ch}}{l_{sf}}}} \qquad (3-7),$$

where L_{ch} is the Ge nanowire channel length, and l_{sf} is the spin diffusion length. In the case where $P_1P_2e^{-\frac{L}{l_{sf}}} \ll 1$, or equivalently the TMR magnitude is small (such as in this work), Equation (3-7) can be further simplified as an exponential function:

$$\mathrm{TMR} \approx 2P_1P_2e^{-\frac{L_{ch}}{l_{sf}}} \qquad (3-8).$$

In the MR curves of Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire transistors shown in Figure 3-11(a), it is difficult to accurately determine the TMR magnitude, because typical abrupt resistance steps were not observed as in previous organic spin valves that comprised two different ferromagnetic contacts.[174-175] This could be attributed to a possibly small difference in the coercive field for the Mn_5Ge_3 spin injector and detector (with the same diameter but slightly different lengths). In addition, the presence of multiple domains in the ferromagnetic Mn_5Ge_3 nanowire would also prevent the abrupt switching of its magnetization.[140] Further investigation may be required to understand the detailed mechanism.

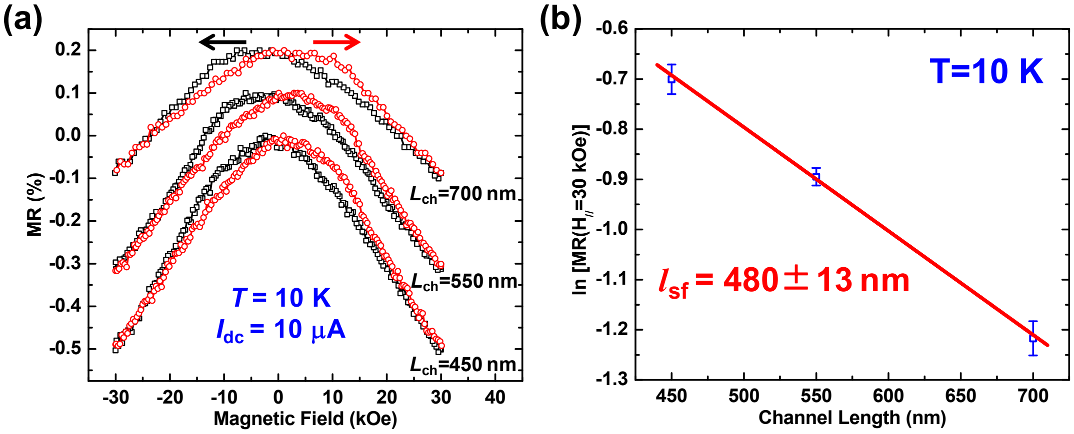

Figure 3-11. Extraction of the spin diffusion length in the Ge nanowire. (a) MR curves of three $Mn_5Ge_3/Ge/Mn_5Ge_3$ nanowire transistor with three different channel lengths (L_{ch} = 450, 550, and 700 nm) at T = 10 K under a dc current bias of I_{dc} = 10 μA. The black and red arrows indicate the backward and forward sweeping directions of the axial magnetic field between -30 kOe and 30 kOe, respectively. All the MR curves are intentionally offset by multiples of 0.1% for clarity. (b) Semi-log plot of the MR magnitude at $H_{//}$ = 30 kOe versus the channel length for the three $Mn_5Ge_3/Ge/Mn_5Ge_3$ nanowire transistors. The linear fitting (red curve) yields a spin diffusion length of l_{sf} = 480±13 nm in the p-type Ge nanowire at T = 10 K. (The data

also appeared in my publication Ref. [7].[7])

Here, in order to extract the spin diffusion length in the Ge nanowire, we obtained the MR amplitude of three Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire transistors with different L_{ch} at the same temperature and magnetic field. Here we picked the largest magnetic field in our measurements to ensure the magnetization of all the Mn_5Ge_3 nanowires in parallel. The rationale is to compare the MR ratio of three Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire transistors with different Ge nanowire channel lengths while keeping all other parameters the same (same temperature and bias condition, *etc*). Therefore, the change in the MR ratio should closely related to the spin relaxation in the Ge nanowire. A semi-log plot of the MR magnitude at $H_{//}$ = 30 kOe versus the channel length is then plotted at T = 10 K in Figure 3-11(b). Using Equation (3-8), one yields a spin diffusion length of $l_{sf} = 480 \pm 13$ nm in the *p*-type Ge nanowire at T = 10 K. To make a meaningful comparison with previous results in Ge, we first estimated the doping concentration in our Ge nanowires. Using the resistivity-doping concentration relation in bulk Ge as an approximation,[180] the resistivity value of $\rho_{Ge} = 2.58 \times 10^{-3}$ Ω-cm at T = 300 K corresponds to a *p*-type doping concentration of about $N_A = 8 \times 10^{18}$ cm^{-3}. Measurements from more than 10 devices yielded a *p*-doping concentration in the range between 6×10^{18} cm^{-3} and 9×10^{18} cm^{-3}. From the literature,[34] *p*-type bulk Ge with a similar doping concentration of $N_A = 8.2 \times 10^{18}$ cm^{-3} was reported to have a spin diffusion length of about l_{sf} = 80 nm (calculated at T = 300 K but it is also valid for temperature down to

T = 5 K as both the spin lifetime τ_{sf} and the diffusion constant D_h have a weak temperature dependence in heavily doped semiconductors[31,34,131]). The significant enhancement in the spin diffusion length in the one-dimensional Ge nanowire channel could be attributed to the effective suppression of electron-phonon scattering and thus spin relaxation by quantum confinements in nanostructures with a reduced density of states.[50] From Equation (3), we can also extract the spin polarization of Mn_5Ge_3 to be about 8 % at T = 10 K, which is much smaller than the reported (42±5)% at T = 1.2 K from point contact Andreev reflection measurements.[120] This large deviation is mainly because that the simplified TMR model here does not include the spin injection efficiency from Mn_5Ge_3 into Ge.

To estimate the spin lifetime, we first calculated the diffusion constant, which can be obtained in degenerately doped semiconductors using the full Fermi-Dirac expression:[170]

$$D_h = \frac{2\mu_h k_B T}{q} \frac{F_{1/2}(\eta_{\mathrm{F}})}{F_{-1/2}(\eta_{\mathrm{F}})} \qquad (3-9),$$

in which μ_h is the hole mobility, k_B is the Boltzmann constant, q is the electron charge, $\eta_{\mathrm{F}} = (E_{\mathrm{V}} - E_{\mathrm{F}})/k_B T$ while $F_{1/2}(\eta_{\mathrm{F}})$ and $F_{-1/2}(\eta_{\mathrm{F}})$ are the Fermi-Dirac integrals. The Fermi-level position in degenerate semiconductors can be determined using the Joyce-Dixon approximation:[181]

$$E_{\mathrm{V}} - E_{\mathrm{F}} \approx k_B T \left(ln \frac{N_{\mathrm{A}}}{N_{\mathrm{V}}} + 2^{-1.5} \times \frac{N_{\mathrm{A}}}{N_{\mathrm{V}}} \right) \qquad (3-10).$$

Using the measured field-effect hole mobility of μ_h = 10 cm^2/Vs at T = 300 K, we can calculate the diffusion constant to be D_h = 0.377 cm^2/s given $N_{\mathrm{A}} = 8 \times 10^{18}$ cm^{-3}

and N_V = 6×10^{18} cm^{-3}.[170] As the diffusion constant is weakly dependent on the temperature,[31,34] we assume the same value for low temperatures so we can further estimate the spin lifetime at T = 10 K using

$$\tau_{sf} = \frac{{l_{sf}}^2}{D_h} = 6.11\, ns \qquad (3-11).$$

It is recognized that the mobility value extracted from the I_{DS}-V_{GS} curves may underestimate the conductivity mobility considering the back-gated device structure and the round shape of Ge nanowires.[126] Therefore, the above-calculated τ_{sf} = 6.11 ns is the upper limit for the spin lifetime. If we adopt the reported hole mobility of μ_h = 250 cm^2/Vs from a p-type Ge thin film with a similar doping concentration,[34] Equation (3-11) would yield the lower limit for the spin lifetime of about τ_{sf} = 244 ps with D_h = 9.43 cm^2/s. Still this value is one order of magnitude larger than that observed in bulk Ge,[34] again implying the advantage of low-dimensional nanostructures in the building of spintronic devices with long spin lifetime and spin diffusion length.[50]

Furthermore, to investigate the temperature dependence of the spin diffusion length, we obtained the temperature-dependent MR magnitudes at $H_{//}$ = 30 kOe for three Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire transistors with different channel lengths (L = 450, 550, and 700 nm) as shown in Figure 3-12(a). Their MR magnitudes showed a similar temperature dependence: the MR magnitude linearly increases with reducing temperature from T = 50 K, and then gradually saturates as the temperature went below T = 10 K. Using Equation (3-8), we obtained the temperature-dependent spin diffusion length as given in Figure 3-12(b), showing a weak temperature dependence of the spin diffusion length in the range of T = 2 K to T = 50 K. The calculated spin lifetime at each temperature using Equation (3-11) is also plotted, assuming a constant diffusion constant of D_h = 9.37 cm^2/s. Such a weak temperature dependence of the spin diffusion length and lifetime was also observed in heavily-doped Si thin films.[31,131] This fact may be explained by the effectively screened ionized impurity scatterings in the heavily doped Ge nanowire,[171] resulting in a weak dependence on the temperature for the momentum relaxation and hence the spin relaxation (as manifested by the spin diffusion length and the spin lifetime). Meanwhile, the additional spin relaxation mechanism from surface roughness scattering is also believed to have weak temperature dependence.[53] For comparison, the data from Ge thin films with a similar p-type doping concentration are also included in Figure 3-12(b),[34] manifesting the significant enhancement of the spin diffusion length and lifetime in Ge nanostructures.[50]

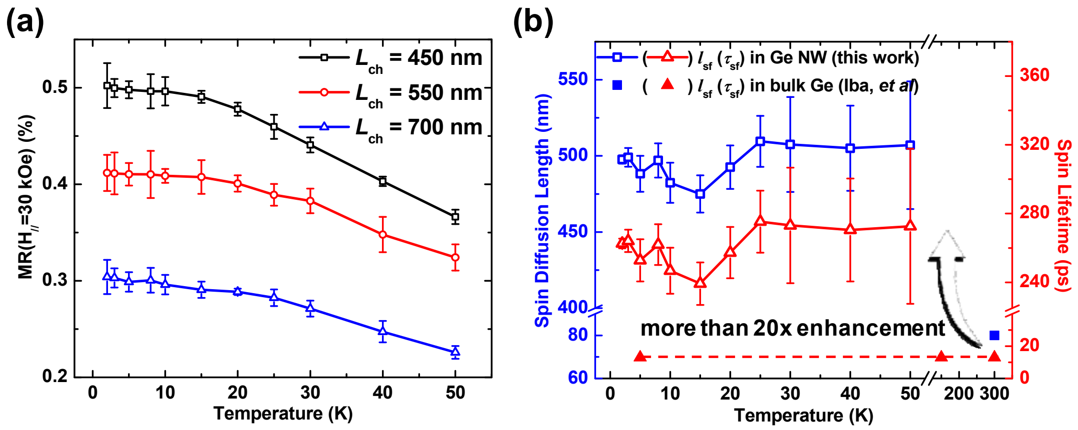

Figure 3-12. Temperature-dependent spin diffusion length and lifetime. (a)

Temperature-dependent MR magnitudes at $H_{//}$ = 30 kOe for three $Mn_5Ge_3/Ge/Mn_5Ge_3$ nanowire transistors with different channel lengths (L = 450, 550, and 700 nm) under a dc current bias of I_{dc} = 10 μA, showing a similar temperature dependence. (b) Fitted temperature-dependent spin diffusion length and calculated spin lifetime, showing a weak dependence on the temperature from 2 K to 50 K. The apparent dip at 10 K is likely due to the fitting error. For comparison, the data from bulk Ge with a similar *p*-type doping concentration in Ref. [34] are also included and represented by solid symbols.[34] Significantly, Ge nanowires showed more than 20 times enhancement in the spin diffusion length and spin lifetime compared with bulk Ge. (The data also appeared in my publication Ref. [7].[7])

To sum up, we have successfully demonstrated electrical spin injection and detection in single-crystalline $Mn_5Ge_3/Ge/Mn_5Ge_3$ nanowire transistors fabricated on degenerately indium-doped Ge nanowires. Under zero current bias, the $Mn_5Ge_3/Ge/Mn_5Ge_3$ nanowire transistor showed positive and symmetric MR characteristics with no apparent hysteresis; on the other hand, negative and hysteretic MR characteristics were observed under a large voltage (current) bias from T = 2 K up to T = 50 K. The hysteretic MR signature clearly indicated spin injection from the ferromagnetic Mn_5Ge_3 contact into the Ge nanowire, and the large bias helped reduce depletion region width of the Mn_5Ge_3/Ge junction to increase the spin injection efficiency. Furthermore, based on the modified Julliere's model, the MR of three $Mn_5Ge_3/Ge/Mn_5Ge_3$ nanowire transistors gave a spin diffusion length of $l_{sf} = 480 \pm 13$

nm and a long spin lifetime of exceeding 244 ps in *p*-type Ge nanowires at $T = 10$ K. The estimated spin diffusion length is significantly larger than the channel length of state-of-the-art MOS transistors,[1] and has a weak temperature dependence. The long spin diffusion length and its weak temperature dependence were explained by the dominant Elliot-Yafet spin-relaxation mechanism as the result of the impurity scatterings in Ge, which was effectively screened in degenerately doped semiconductors. These observed spin diffusion length and spin lifetime in one-dimensional Ge nanowires were much larger than those reported from bulk Ge,[34] which implied that the spin relaxation can be effectively suppressed in the one-dimensional channel because of the quantum confinement effect.[50,56] With a relatively long spin diffusion length and the convenient fabrication process for $Mn_5Ge_3/Ge/Mn_5Ge_3$ nanowire transistors, it is possible to integrate Ge nanowire-based spintronic devices into standard CMOS technology. As an example, the proposal of a transpinor based on this work will be discussed later in Chapter 3.5.

3.4 Tunneling Spin Injection into Ge Nanowires

In the previous Chapter 3.3, we have demonstrated the spin injection from Mn_5Ge_3 into *p*-type Ge nanowire through a Schottky barrier that could help enhance the spin injection efficiency. As we discussed earlier in Chapter 2.4, another approach to circumvent the conductivity mismatch problem is the insertion of a tunneling barrier in the ferromagnetic contact for spin injection.[128-129] In this Chapter, we will present the electrical spin injection into Ge nanowires through epitaxial Fe/MgO tunnel junctions. Also, *n*-type Ge nanowires were used in this study for the longer electron spin lifetime and spin diffusion length because of the weaker spin-orbit interaction in the conduction band (see Table 1-1 and Figure 1-3).

Experimentally, the cylindrical geometry of nanowires has been a major challenge in growing high-quality defects-free tunnel oxides on nanowire surface for spin injection. Firstly, there is no well-defined lattice plane on the round nanowire surface; therefore, the favorable epitaxial growth of tunnel oxide with minimizing lattice matches (*i.e.*, [110]Fe(001)//[100]MgO(001)//[110]Ge(001) in the Fe/MgO/Ge epitaxial tunnel junction) can hardly be realized in nanowire devices. Secondly, the large surface-to-volume ratio in nanowires yields a larger surface area with high-density of interface states, as usually evidenced from the large gate hysteresis in nanowire field-effect transistors.[93] Such high-density interface states would lead to strong Fermi-level pinning in direct ferromagnetic metal contacts to semiconductor nanowires, which could hinder the spin injection process.

In the effort of fabricating high-quality ferromagnetic tunneling contacts to semiconductor nanowires, several approaches have been proposed, as illustrated in Figure 3-13. ALD was used to grow conformal Al_2O_3 tunnel oxide on Si nanowires as shown in Figure 3-13(a);[58] however, the nucleation of ALD is very sensitive to the initial surface condition and the ALD films may be discontinuous with pinholes in the ultrathin film regime.[182] Besides, the metal electrode, which is usually deposited by directional electron beam evaporation, is buckled on top of the nanowire as schematically illustrated in Figure 3-13(b). Such contact morphology would prevent abrupt switchings of the magnetization,[58] especially for nanowires with large diameters (which essentially require thick metal electrodes). To solve this issue, Heedt *et al* proposed a planarization procedure using a hydrogen silsesquioxane (HSQ) lifting layer to reduce the metal electrode thickness and hence make smooth ferromagnetic contacts to cylindrical nanowires,[60] as shown in Figures 3-13(c-d). This process is useful for nanowires with facets and large diameters; however, it is susceptible to the nonuniformity of the nanowire diameters and also process variations (such as the HSQ thickness and etching depth). Alternatively, we used a tilted three-step deposition process to grow Fe/MgO tunnel junctions on Ge nanowires inside a MBE chamber, as illustrated in Figure 3-13(e). The fabrication process is described as follows. To start, single-crystalline Ge nanowires were grown on a Si substrate by the conventional VLS method, and then were exposed in the arsenic (As) ambient at about 600 ^{o}C inside a ultrahigh-vacuum MBE chamber for 2 hours to drive As diffuse into Ge nanowires as *n*-type dopants. Through this process, the introduced As doping concentration was estimated to be about $N_D = 9\times10^{18}$ cm^{-3}, which was calculated from the measured resistivity of 1.68×10^{-3} Ω-cm at $T = 300$ K. As-doped Ge nanowires were then transferred to a SiO_2/Si substrate, and subsequently multiple electrodes were patterned on top with electron-beam lithography using bi-layer polymethyl methacrylate (PMMA) resists (*i.e.*, PMMA 495K and PMMA 950K, where the numbers 495K and 950K here indicate the molecular weight of the resist polymer). After that, the sample was dipped into dilute HF solution for 10 s to remove the native oxide in the contact region, and then quickly loaded into an ultrahigh vacuum MBE chamber for the Fe/MgO tunnel junction growth: 1) firstly $0.5t$-thick MgO was deposited under 5 degree tilting followed by $0.5t$-thick MgO deposition under -5 degree tilting (t is the nominal total thickness of the MgO tunnel oxide); 2) then 120 nm-thick Fe was deposited with normal incidence (0 degree tilting); 3) finally 10 nm-thick Al_2O_3 was capped on top of the Fe electrode to prevent the oxidization. The purpose of this tilted deposition process is to promote a better coverage of MgO on the nanowire surface and hence minimize the undesirable short circuit between the Fe electrode and the nanowire. Indeed, cross-sectional TEM image of the as-grown Fe/MgO/Ge nanowire tunnel junction revealed a uniform coverage of MgO on the Ge nanowire surface as shown in Figure 3-13(f), preventing short circuits directly from Fe to Ge.

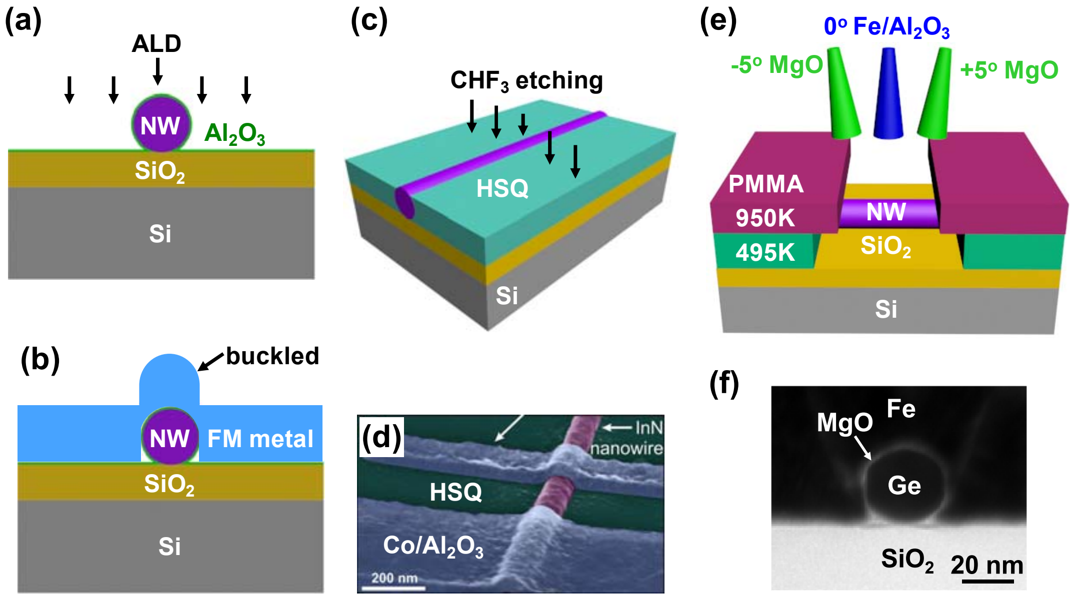

Figure 3-13. Methods of growing tunnel oxides on semiconductor nanowires. (a) Schematic illustration of the Al_2O_3 deposition on semiconductor nanowires by ALD as the tunneling oxide for spin injection. (b) Schematic illustration of the nanowire spin injection device after the ferromagnetic metal deposition, showing a buckled morphology on top of the nanowire. (c) Schematic illustration of the planarization process using a HSQ lifting layer followed by CHF_3 plasma etching. (d) Colored SEM image of the fabricated nanowire spin injection device with smooth ferromagnetic contacts. (e) Schematic illustration of the tilted three-step deposition process to grow Fe/MgO tunnel junctions on semiconductor nanowires. (f) Cross-sectional TEM image of a Fe/MgO/Ge nanowire tunnel junction, showing a uniform coverage of 2 nm MgO on the Ge nanowire surface. (a-b) are reproduced from Ref. [58],[58] (c-d) are reproduced from Ref. [60],[60] and (e-f) also appeared in my publication Ref. [8].[8]

To further investigate the electrical properties of the as-grown Fe/MgO/Ge nanowire tunnel junctions, temperature-dependent *I-V* measurements were performed on a series of Fe/MgO/Ge nanowire devices with different MgO thicknesses ranging from 1 nm to 3 nm.[8] Figure 3-14(a) shows the SEM image of a typical Fe/MgO/Ge nanowire spin injection device fabricated on a SiO_2/Si substrate. As we can see from the temperature-dependent *I-V* measurements shown in Figures 3-14(b-e), for MgO thickness of 1.0 nm and 1.5 nm, the *I-V* curves were linear from 300 K to 10 K, implying the ultrathin MgO films were not continuous and hence the current mainly flowed through pinholes. However, as we further increased the MgO thickness to 2.0 nm and 3.0 nm, the current decreased dramatically, and more importantly the *I-V* curves became nonlinear, suggesting apparent tunneling behaviors for thicker MgO. It should be pointed out that the critical MgO thickness in nanowire device (about 2 nm) to achieve tunneling behaviors is larger than the value in Ge thin film devices (about 0.5-1 nm).[21,133] This is understandable in the sense that Ge thin film has a much flatter surface morphology that allows for a smooth coverage of MgO on the surface during the deposition process. Figure 3-14(f) shows the temperature-dependent resistance-area (RA) product extracted from *I-V* curves in Figure 3-14(e) at a bias voltage of 0.4 V, in which the weak temperature dependence affirmed the tunneling nature for the Fe/MgO/Ge nanowire junction.

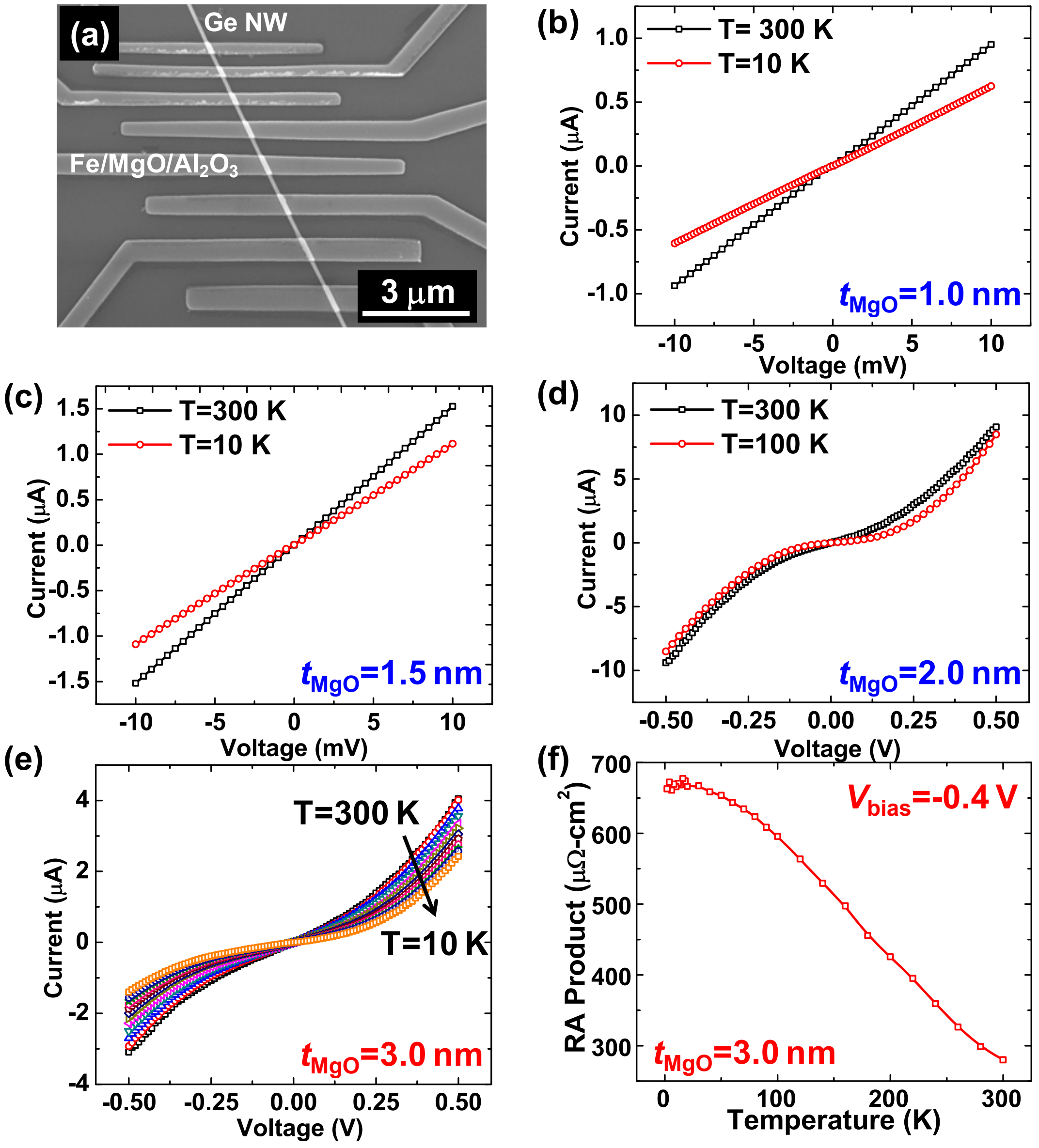

Figure 3-14. Temperature-dependence of the Fe/MgO contacts to Ge nanowires. (a) SEM image of a typical Fe/MgO/Ge nanowire spin injection device. (b-e) Temperature-dependent *I-V* measurements on a series of Fe/MgO/Ge nanowire devices with MgO thickness of 1.0 nm, 1.5 nm, 2.0 nm, and 3.0 nm, respectively. For MgO thickness of 1.0 nm and 1.5 nm, the *I-V* curves were linear, implying a

discontinuous coverage the ultrathin MgO films on the Ge nanowire surface. However, for MgO thickness of 2.0 nm and 3.0 nm, the *I-V* curves became nonlinear, suggesting apparent tunneling behaviors for thicker MgO oxide. (f) RA product extracted from the temperature-dependent *I-V* curves at a bias voltage of 0.4 V for the MgO thickness of 3.0 nm. The weak temperature dependence affirmed the tunneling nature of the Fe/MgO/Ge nanowire junction. (The data also appeared in my publication Ref. [8].[8])

Similar to spin injection into Ge/Si bulk and thin film as discussed in Chapters 1.2-1.3, typically three measurement techniques can be used to study the spin transport in semiconductor nanowires: 3-T Hanle measurement, nonlocal Hanle measurement and nonlocal spin valve measurements. In practice, considering the small diameter of nanowires, the contact area in nanowire spin injection devices is typically much smaller than that of bulk devices, and hence the 3-T Hanle signal would be too small to detect. Also, the spin precession in ideally one-dimensional channel is expected to be significantly suppressed because of quantum confinements, which makes the nonlocal Hanle signal very difficult to be observed. In literature, to the best of our knowledge, the only observation of nonlocal Hanle signals was reported in GaN nanowires with FeCo/MgO tunnel contacts.[59] On the other hand, nonlocal spin valve signals have been observed in several other semiconductor nanowires, including Ge,[8,56] Si,[58] and InN,[60] which are usually considered as a conclusive evidence for successful spin injection. Similar to spin injection in bulk, the nonlocal spin valve measurement setup is shown in Figure 3-15(a) for spin injection into Ge nanowires with MBE-grown Fe/MgO tunnel junctions. Here the 10 nm Al_2O_3 layer is used as a protection layer to prevent Fe from oxidization.

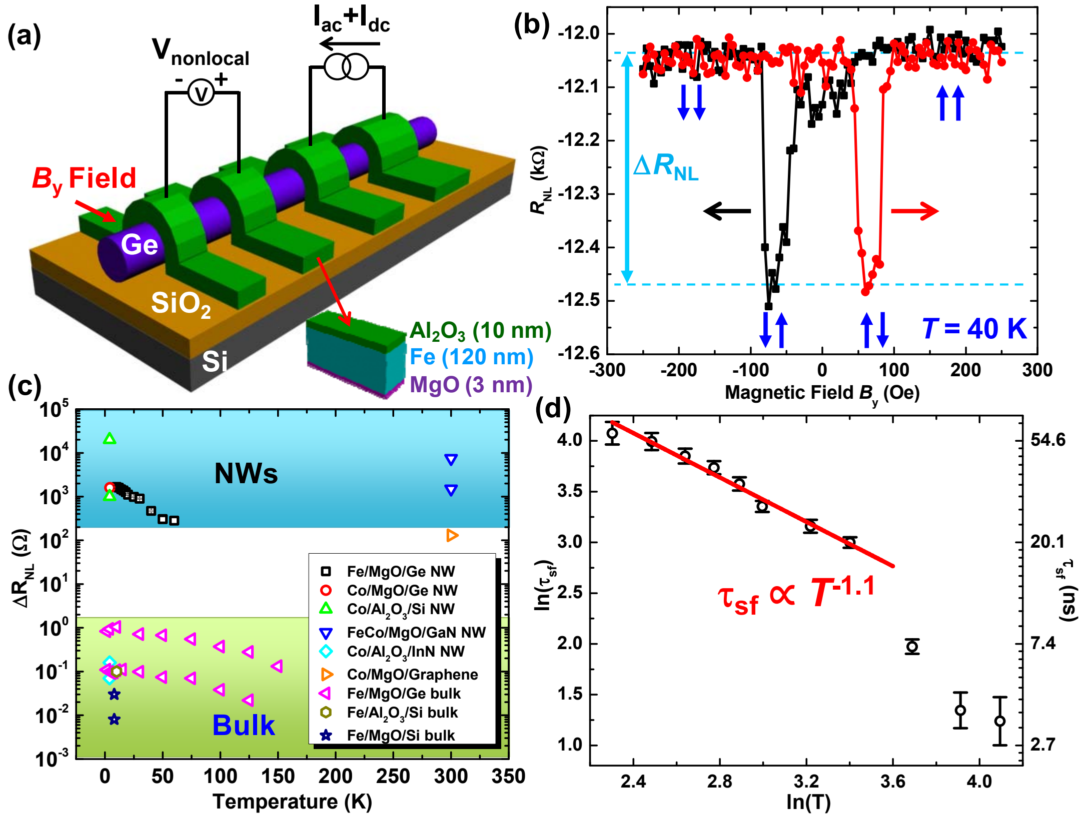

Figure 3-15. Nonlocal spin valve measurement on the Ge nanowire. (a) Schematic illustration of the nonlocal spin valve measurement setup for Ge nanowires with Fe/MgO tunnel junctions, similar to that in Figure 1-3(a) of Chapter 1.2. (b) Nonlocal spin valve signal of Ge nanowires at $T = 40$ K with an injection ac current of 1 μA, showing a nonlocal resistance of $\Delta R_{NL} = 470\ \Omega$. The black and red arrows indicate the sweeping direction of the magnetic field, while the blue arrows denote the relative

magnetization direction of the spin injector and detector. The spin lifetime and spin diffusion length are extracted to be 7.2 ns and 2.57 μm, respectively. (c) Temperature-dependent nonlocal resistance reported in various semiconductor nanowires and bulk as well as graphene.[8,39,56,58,60] In general, the observed nonlocal resistance in nanowire devices is orders of magnitudes larger than that in bulk devices, with one exception for the InN nanowire.[60] (d) A log-log plot of the temperature-dependent spin lifetime in Ge nanowires. The power-law fitting yields a temperature dependence of $\tau_{sf} \propto T^{-1.1}$ for the electron spin lifetime. The deviation from power-law fitting at higher temperature may due to the competing contributions from phonon, impurity, and also surface roughness scatterings. (The data also appeared in my publication Ref. [8].[8])

As an example, Figure 3-15(b) shows the nonlocal spin valve signal in Ge nanowires at $T = 40$ K with an injection ac current of 1 μA. The characteristic of the nonlocal spin valve signal here is similar to that observed in bulk Ge (see Figure 1-3 (b); however, the signal amplitude, namely the nonlocal resistance ΔR_{NL}, is much larger in Ge nanowires. In fact, similar enhancement in the nonlocal resistance in nanowire devices has also been observed in spin injection into other semiconductor nanowires (one exception is the InN nanowire, possibly due to small contact resistance), as shown in Figure 3-15(c). This is mainly because that the channel cross-sectional area in nanowire devices is much smaller, which would give rise to a larger nonlocal spin valve signal according to Equation (1-2) presented in Chapter 1.2 (p.

10). Besides, the longer spin diffusion length in nanowires compared with bulk materials would also enhance the nonlocal spin valve signal as well.

Quantitatively, we can use Equation (1-2) to obtain the electron spin diffusion length of l_{sf} = 2.57±0.09 μm in the Ge nanowire, given L = 850 nm, A = 5.03x10^{-11} cm^2, $\sigma_s = 1/\rho_s$ = 704 S/cm, and assuming P_J = 30%. Using the diffusion constant D = 9.21 cm^2/s for N_D = 9×10^{18} cm^{-3}, we can further calculate the electron spin lifetime to be τ_{sf} = 7.2±0.5 ns. Both values are larger than those reported in bulk Ge with a similar *n*-type doping concentration (l_{sf} = 0.58 μm and τ_{sf} = 1.08 ns).[21] Similar enhancement in the spin lifetime and spin diffusion has also been observed in p-type Ge nanowires in the previous Chapter 3.3, which again affirms that the spin relaxation is effectively suppressed in nanowires. To further understand the spin relaxation mechanism in Ge nanowires, the temperature-dependent spin lifetime is extracted and plotted in Figure 3-15 (d). In the log-log plot, the power-law fitting in the temperature range of 10-30 K yields a temperature dependence of $\tau_{sf} \propto T^{-1.1}$ for the electron spin lifetime. For comparison, the temperature-dependent spin lifetime and momentum relaxation time in bulk n-type Ge were found to be: $\tau_{sf} \propto T^{-1.9}$ and $\tau_m \propto T^{-1.66}$, respectively.[26,183] According to the Elliot-Yafet spin relaxation mechanism, the spin lifetime should have the same temperature dependence as the momentum relaxation time,[45] as shown in Equation (1-5). The small deviation in the temperature dependence of the spin lifetime in *n*-type Ge nanowires from that of momentum relaxation time may suggest there are additional spin scattering mechanisms that have a different temperature dependence as phonon scattering, such as impurity scattering and surface roughness scattering.[53] To further investigate all the possible spin relaxation mechanisms in Ge nanowires, future studies are required to examine the temperature-dependent spin lifetime in Ge nanowires with different diameters and doping concentrations.

To conclude, we have demonstrated the electrical spin injection into *n*-type Ge nanowires using epitaxial Fe/MgO tunnel junctions. In the MBE growth of tunnel junctions, the MgO thickness was carefully engineered to assure tunneling-dominant transport through the MgO junction. Nonlocal spin valve signal were observed up to 60 K, indicating successful spin injection into the Ge nanowire. The spin lifetime and spin diffusion length was extracted to be τ_{sf} = 7.2±0.5 ns and l_{sf} = 2.57±0.09 μm at T = 40 K in *n*-type Ge nanowires, which were much larger than those reported in bulk *n*-type Ge with a similar doping concentration. The significant enhancement in the spin lifetime and spin diffusion length of Ge nanowires again suggests that semiconductor nanostructures have an inherent advantage over bulk materials in fabricating practical spintronic devices that favors long spin lifetime and spin diffusion length.

3.5 DMS Nanowire-based Nonvolatile Transpinor

As discussed in the Introduction section (Chapter 1.1), in order to make a spinFET that can truly meet the challenges and outperform Si scaled CMOS and meanwhile operate at room temperature, one practical approach is to reduce or eliminate the charge current flow. One appealing solution is to use DMS rather than a pure semiconductor or metal as the channel material for spinFET. The unique feature of DMS materials is that their ferromagnetism is mediated by itinerant carriers through exchange interaction with localized spins of magnetic impurities,[102] and hence can be modulated through a gate electrode.[106,184] This is of particular interest for low-power logic and memory applications, because it invokes collective effects to be nonvolatile, low V_{th} due to phase transition, and no charge current, and the use of an electric field rather than an electric charge current to control phase transition. Thus it provides the possibility of building energy-efficient devices.

Recently, we have demonstrated that the MBE growth of singe-crystalline Mn-doped Ge DMS quantum dots with a Curie temperature above 400 K, and more significantly the electric field control of ferromagnetism up to room temperature,[105-106] as shown in Figure 3-16. In that work, the use of Mn-doped Ge nanostructures with substantial quantum confinement helps minimize the defect-induced formation of secondary phases and also enhance the carrier-mediated ferromagnetism. These results imply a unique advantage of using DMS nanostructures over thin films and bulk materials in fabricating practical spintronic devices that can operate at room temperature. For the convenience of device fabrication and integration, we have been working on the MBE growth of Mn-doped Ge DMS nanowires, in which similar electric-field-controlled ferromagnetism with high Curie temperature is expected.

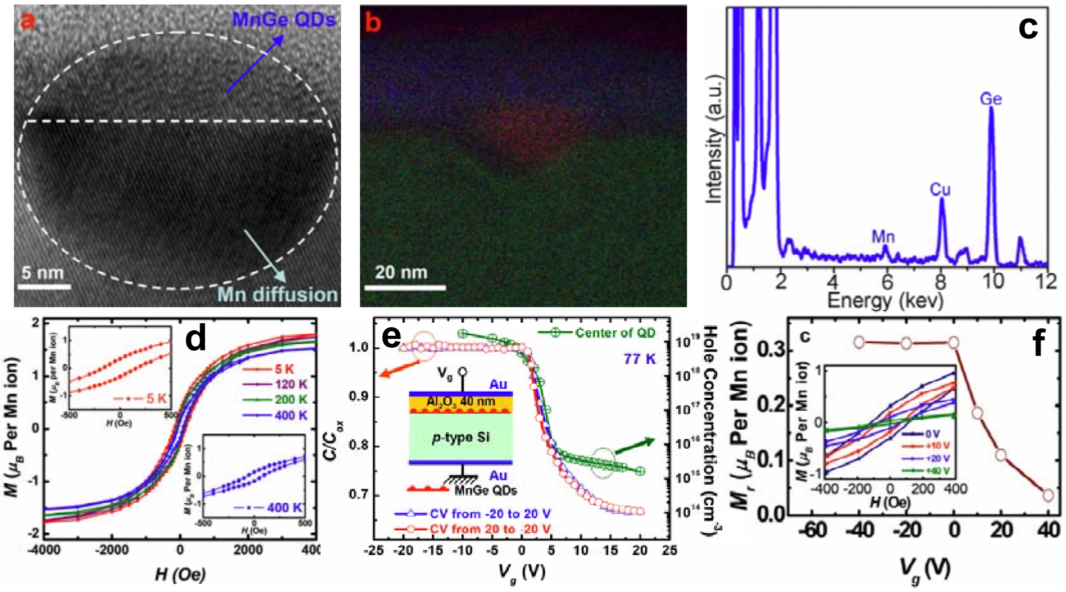

Figure 3-16. Electric field control of ferromagnetism in $Mn_{0.05}Ge_{0.95}$ DMS quantum dots. (a) HRTEM image of a $Mn_{0.05}Ge_{0.95}$ quantum dot showing no apparent lattice defects. (b) Electron energy-loss spectroscopy (EELS) composition mapping of the Mn distribution. Mn is found to distribute uniformly in the $Mn_{0.05}Ge_{0.95}$ quantum dot and the Mn-diffused Si area. (c) EDS composition spectrum showing that both Mn and Ge are present in $Mn_{0.05}Ge_{0.95}$ quantum dot. (d) Magnetic hysteresis loops measured at different temperatures from 5 K to 400 K. (e) C-V curves measured at 77 K with a frequency of 100 kHz along with the simulated hole concentration. It clearly shows a transition between hole accumulation at negative bias and hole depletion at

positive bias. The inset is a schematic drawing of the MOS device. (f) A representation of remnant moments with respect to the gate bias. Inset is an enlarged figure to clearly show the change of remnant moment. (The data also appeared in my publication Ref. [106].[106])

To make a DMS-based spinFET, we have recently proposed a novel nonvolatile transpinor based on a Mn_xGe_{1-x} DMS nanowire.[7-8] This concept is different from those earlier proposals discussed in Chapter 1.1 in that we use DMS as the channel material to allow us to manipulate the magnetic state of the DMS channel through a voltage signal without current flow in the channel. We further integrate the DMS nanowire with high-quality ferromagnetic contacts for spin injection to build the prototype of transpinor. Two possible implementations are schematically illustrated in Figures 3-17(a-b) with Mn_5Ge_3 and Fe/MgO as source/drain contacts,[7-8] respectively. In this transpinor device, the magnetic moments are transferred from the source to the channel, and then to the drain through spin injection and exchange interaction, respectively. As the gate manipulates the ferromagnetism of the DMS channel, it controls the communication between the source and drain.

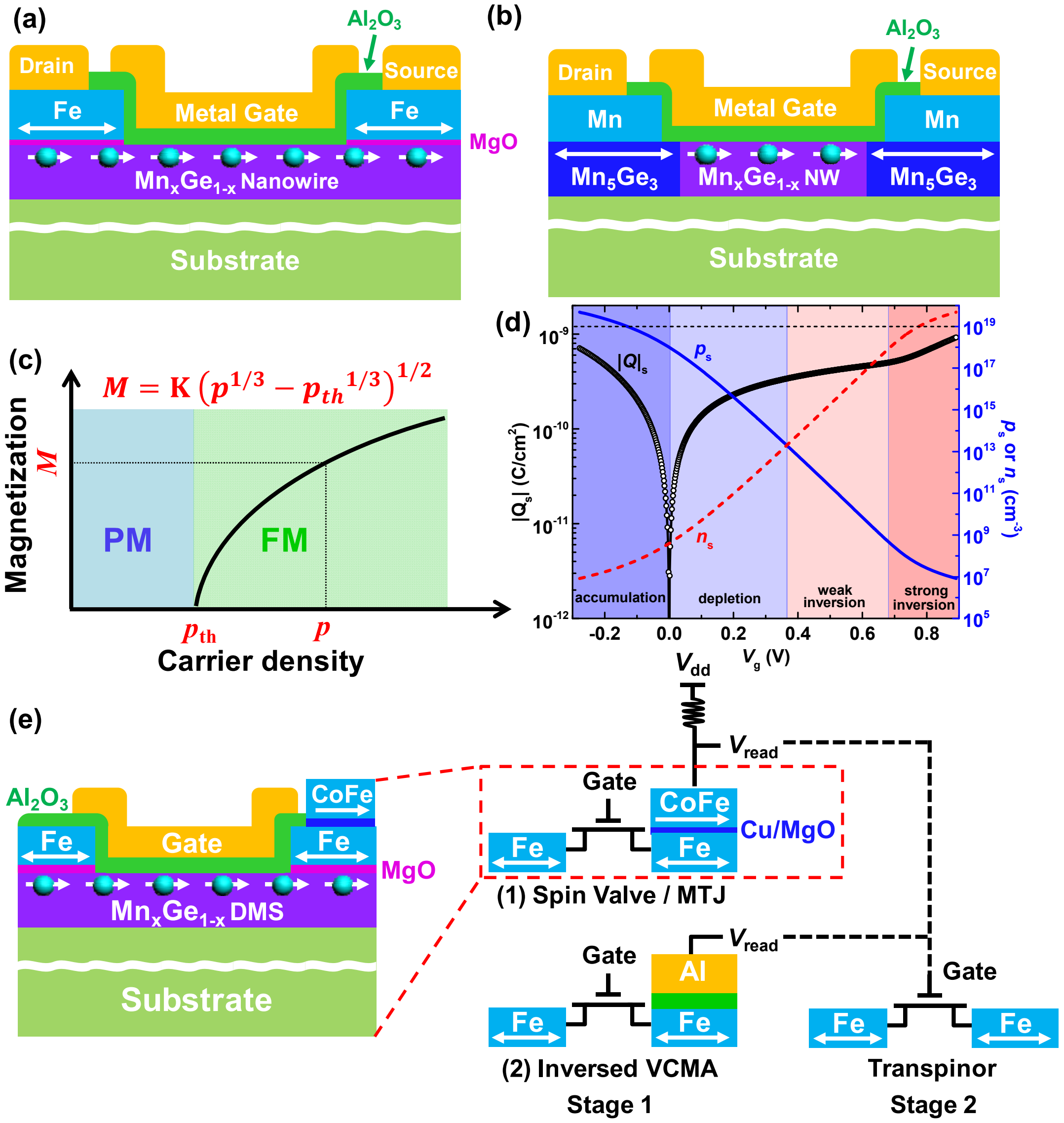

Figure 3-17. DMS nanowire-based nonvolatile transpinor. We named it transpinor because the spin (or magnetic momentum) information is transferred from source to drain through the DMS channel. Two possible implementations of the proposed diluted magnetic Ge nanowire-based nonvolatile transpinor with (a) Fe/MgO tunnel junctions, and (b) ferromagnetic Mn_5Ge_3 Schottky junctions, respectively. The magnetic moments are transferred from the source to the channel, and then to the

drain with a spin gain. The Mn_xGe_{1-x} DMS nanowire channel, whose paramagnetism-to-ferromagnetism phase transition is electrically controlled by the gate voltage, communicates with the input and the output nanomagnets through spin injection/extraction and exchange interaction, respectively. (c) Schematic of the paramagnetism-to-ferromagnetism phase transition. (d) Simulated carrier densities (Q_s is the sheet charge density, p_s is the surface hole density, and n_s is the surface electron density) in a Ge MOS structure with $N_A = 10^{18}$ cm^{-3}, $V_{FB} = 0$ V, and $t_{ox} = 2$ nm. (e) Two possible schemes to convert the magnetization to a voltage signal in read out of a transpinor circuit. The devices can be cascaded to transfer the spin information (hence transpinor), very much like CMOS, but in the magnetic state. The first scheme adopts either a metallic CoFe/Cu/Fe(Mn_5Ge_3) spin valve or a CoFe/MgO/Fe(Mn_5Ge_3) MTJ connected to the power supply V_{dd} through a resistor. The other scheme uses the inverse voltage-controlled magnetic anisotropy (VCMA) effect, in which the switching in the output magnet will induce a voltage pulse in the read out. (The data also appeared in my publication Ref. [8].[8])

Unlike the Datta-Das and Sugahara-Tanaka types of spinFET relying on the control of the spin of individual electron, the proposed transpinor rather manipulates a collection of spins *via* the carrier-mediated paramagnetic-to-ferromagnetic transition as a single identity and thus is more energy-efficient and robust.[11] The use of N collective spins can be treated as a single identity and will enable the ultimate power dissipation of a single switching element (nanomagnet) of $k_BT\ln 2$, instead of $Nk_BT\ln 2$

per switch for conventional equilibrium computing (in a more general case, the energy dissipation should be written as $Nk_BT\ln(r)$, where $1/r$ is the error probability).[185] Moreover, the input and output information can be stored in the ferromagnetic contacts (nanomagnets); therefore, it inherently provides nonvolatility in the transpinor and hence eliminates the standby power dissipation – one major issue of scaled CMOS.

Compared with conventional CMOS devices, the transpinor could provide several important advantages, including a low V_{th} and nonvolatility (the information is stored as the magnetization of nanomagnets), to achieve lower power dissipation (minimize charge current flow), along with added functionalities (spin freedom and gate-controlled ferromagnetism), and faster switching (critical behavior in ferromagnetic phase transition). To see this more clearly, let's first take a quantitative analysis of the gate modulation in the DMS-based transpinor device. For simplicity, according to the Zener model, the Curie temperature of the $\mathrm{Mn}_x\mathrm{Ge}_{1\text{-}x}$ DMS nanowire can be approximately described as:[102]

$$T_c = \mathrm{A}p^{1/3} \qquad (3-12).$$

On the other hand, near the critical temperature T_{c} of the ferromagnetic phase transition, the critical behavior of the magnetization is given by a power-law relation:[186]

$$M(T) = \mathrm{B}(T_c - T)^{1/2} \qquad (3-13),$$

Here A and B are material-related constants. Equation (3-13) can be re-written as:

$$M(p) = \mathrm{B}\left(\mathrm{A}p^{1/3} - T\right)^{1/2} = \mathrm{K}\left(p^{1/3} - {p_{th}}^{1/3}\right)^{1/2} \qquad (3-14),$$

where $p_{th} = (T/\mathrm{A})^3$, and $\mathrm{K} = \mathrm{B}A^{1/2}$, as plotted in Figure 3-17(c). In the fabrication of transpinor, one can design the background doping density in the vicinity of the phase transition point p_{th} (the minimum carrier density to mediate long-range ferromagnetism, $p_{th} \approx 10^{18}$-10^{19} cm^{-3} for $\mathrm{Mn}_x\mathrm{Ge}_{1-x}$ DMS).[106] As the gate voltage is swept to increase p to reach p_{th}, the paramagnetism-to-ferromagnetism phase transition occurs abruptly, and the resulted ferromagnetic DMS channel leads to a simultaneous switch of the output nanomagnet (It should be noted that the required magnetic momentum of the DMS channel to switch the output nanomagnet depends on the switching mechanism and also the dimension of the output nanomagnet). In this process, the change in the gate voltage could be very small (less than 0.15 V as shown below, and there is no theoretical minimum); therefore, the active power dissipation can be minimized and the switching speed can be fast.

In the conventional scaled CMOS, the required gate voltage swing to turn the device on and off is limited by the subthreshold swing of $SS \approx 60$ mV/dec at room temperature. To achieve a current ON/OFF ratio above 10^4, a minimum gate voltage swing is estimated to be about 0.25 V, which limits the voltage scaling in CMOS. On the contrary, the operation of the transpinor relies on the modulation of the magnetic moment rather than the charge current flow in the DMS channel; therefore, the gate voltage swing could be much smaller. To estimate the gate voltage swing for the transpinor, Figure 3-17(d) simulates the gate-dependent carrier densities in a Ge MOS structure with a p-type doping of $N_\mathrm{A} = 10^{18}$ cm^{-3}, flat band voltage of $V_\mathrm{FB} = 0$ V, and 2 nm-thick $\mathrm{Al_2O_3}$ as the gate dielectric. In the accumulation regime, the gate voltage is only changed by less than 0.15 V to increase the carrier density to reach $p_s = 10^{19}$ cm^{-3}, and the swing can be further reduced by using other high-κ gate dielectrics with a higher dielectric constant (such as HfO_2). Thus a much lower V_{th} can be achieved.

It should be pointed out that one of the key challenges to integrate spintronic devices into CMOS circuits is to achieve efficient conversion between a spin signal (magnetization) and a charge signal (current/voltage), and the concatenability (device fan out). Similarly, in order to cascade our transpinor devices for logic computation, several strategies can be adopted to transfer information from one transpinor device to another, as shown in Figure 3-17(e). Possible solutions may involve magnetic tunnel junctions (MTJs), spin valves, or the (inverse) spin Hall effect.[187] For instance, CoFe/MgO/Fe(Mn_5Ge_3) MTJ or CoFe/Cu/Fe(Mn_5Ge_3) metallic spin valve can be integrated on top of the nanomagnets to read out and also manipulate their magnetizations. Alternatively, the recently discovered VCMA effect may be used to read/write the magnetization information in the nanomagnets.[188] In this way, the control and clocking schemes will be carefully designed to enable the switching of the next stage. The read out voltage signal can be used to drive the switching of the next transpinor stage, which ideally requires a very small range of gate voltage in the vicinity of paramagnetic-to-ferromagnetic phase transition.

In the realization of the proposed nonvolatile transpinor, one important step is to synthesize single-crystalline Mn_xGe_{1-x} DMS nanowires with a high Curie temperature electric-field controlled ferromagnetism. As predicted by the Zener model,[101,189] one effective approach to achieve a high Curie temperature in the Mn_xGe_{1-x} DMS system is to increase the Mn doping concentration in the Ge matrix, in which the substitutional Mn dopants provide both the localized magnetic moments and itinerant carriers mediating the ferromagnetic ordering. However, it is important to point out that the major obstacle to synthesize Mn-doped Ge DMS is the low solubility of Mn in the Ge matrix, and hence excessive Mn doping could induce the formation of intermetallic precipitations and secondary phases, such as Mn_5Ge_3 and $Mn_{11}Ge_8$.[104,190] As shown in our early work (see Figure 3-16),[106] the use of nanostructures could help minimize the defects formation and also enhance the carrier-mediated ferromagnetism. Therefore, here we establish the pattern-assisted MBE growth of Mn_xGe_{1-x} DMS nanowires,[191] as illustrated in Figure 3-18.

To fabricate the SiO_2 pattern for the MBE growth, 120 nm thick SiO_2 was deposited on a Ge substrate using PECVD (Figure 3-18(a)), followed by the spin coating of PMMA *e*-beam resist on top. After that, EBL was employed to generate nanotrench patterns on the PMMA layer (Figure 3-18(b)), which were then transferred to the SiO_2 layer by dry etching (Figure 3-18(c)). After removing the PMMA layer (Figure 3-18(d)), the SEM image in Figure 3-18(e) clearly shows that the produced nanotrench has a width of about 100 nm. Finally, the pattern was loaded into the MBE chamber for the Mn_xGe_{1-x} nanowire growth with a Ge growth rate of about 0.2 Å/s and a tunable Mn flux as the dopant source (Figure 3-18(f)). The nominal deposition thickness was about 60 nm. It is noted that the pattern-assisted MBE growth at the low temperature of 180 °C was not selective, and a planarization process was developed to carefully remove the undesired Mn_xGe_{1-x} layer on the SiO_2

mask without damaging the Mn_xGe_{1-x} nanowires inside the trenches.[191]

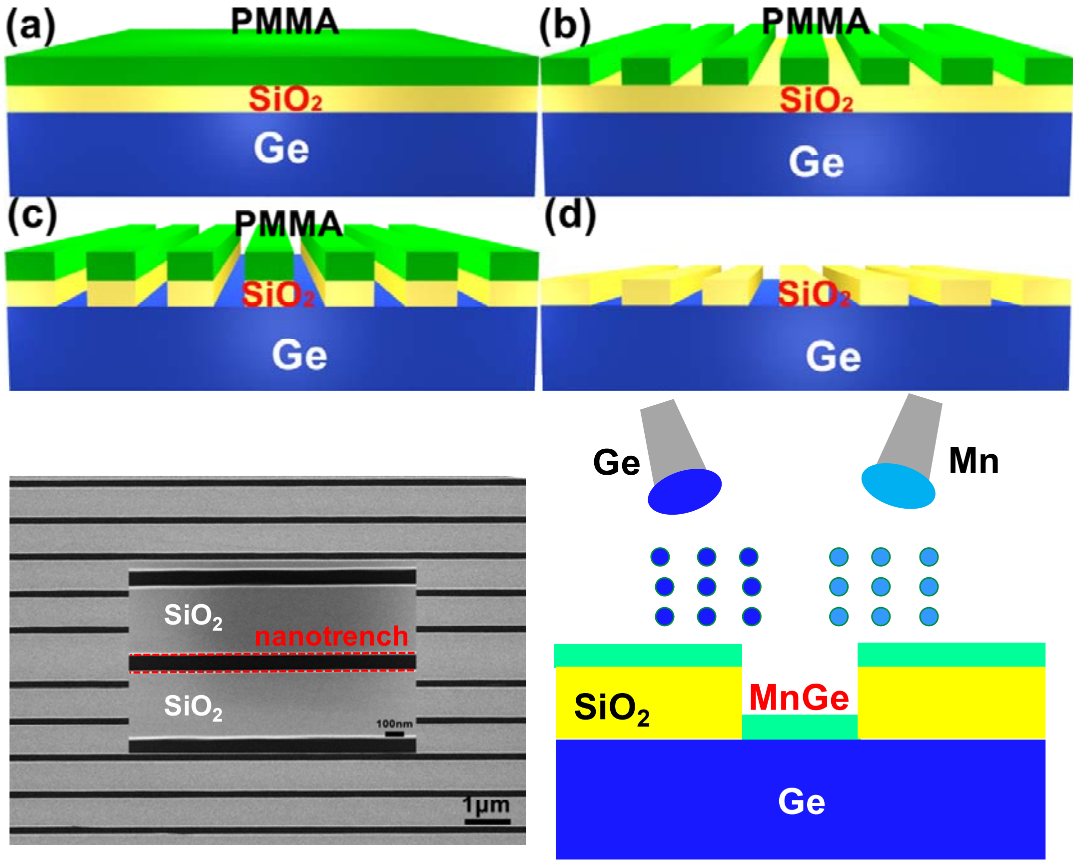

Figure 3-18. Pattern-assisted MBE growth of Mn_xGe_{1-x} DMS nanowires. (a) Deposition of 120 nm thick SiO_2 layer on a Ge substrate by PECVD, followed by spin coating of PMMA *e*-beam resist on top. (b) EBL to generate nanotrench pattern on the PMMA layer. (c) Pattern transfer to the SiO_2 layer by dry etching. (d) Removal of the PMMA layer. (e) SEM image of the produced nanotrench pattern on the SiO_2 layer, showing a width of about 100 nm. (f) MBE growth of the Mn_xGe_{1-x} nanowire. (The data also appeared in my publication Ref. [191].[191])

After the growth, detailed TEM analysis was carried out to understand the microstructure and composition of the grown Mn_xGe_{1-x} nanowires. Figure 3-19(a) shows the cross-sectional TEM image of the Mn_xGe_{1-x} nanowires grown on the Ge substrate with the SiO_2 nanotrench pattern. It is found that the width and height of the Mn_xGe_{1-x} nanowire were about 100 nm and 60 nm, respectively. The high-resolution TEM image and the selected area electron diffraction image affirm that the Mn_xGe_{1-x} nanowire is single crystalline without any precipitates. Besides, the magnetic measurements in SQUID revealed clear magnetic hysteresis curves from 10 K to 400 K, clearly indicating a high Curie temperature far above room temperature (Figure 3-19(b)). These results suggest that single-crystalline Mn_xGe_{1-x} DMS nanowires with room-temperature ferromagnetism have been demonstrated. Toward building the prototype of the nonvolatile transpinor, we have been working on the demonstration of electric-field controlled ferromagnetism in the Mn_xGe_{1-x} DMS nanowire,[191] and further the device integration with the above Fe/MgO and Mn_5Ge_3 ferromagnetic contacts for spin injection. This part of work is still ongoing in my group.

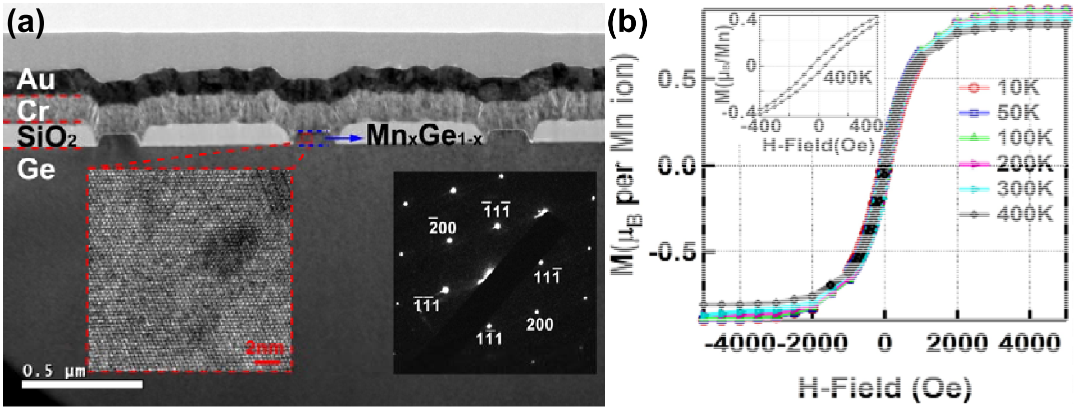

Figure 3-19. Characterization of the grown Mn_xGe_{1-x} nanowires. (a) A typical cross-sectional TEM image of the Mn_xGe_{1-x} nanowires grown on the Ge substrate with the SiO_2 nanotrench pattern. The inset high-resolution TEM image and the selected area electron diffraction image clearly show that the Mn_xGe_{1-x} nanowire is single crystalline without any precipitates. The Cr/Au layer was deposited on top to protect the Mn_xGe_{1-x} nanowires during the sample preparation by FIB. (b) Temperature-dependent magnetic hysteresis loops. The inset is the magnified magnetic hysteresis loop obtained at 400 K, indicating that the Curie temperature is above 400 K. (The data also appeared in my publication Ref. [8].[8])

Chapter 4

Electrical Spin Detection in Topological Insulators

4.1 Overview

This Chapter seeks to study new materials with improved spin polarization for spin injection and detection, *i.e.*, to have close to 100% spin polarization. Thus we look into topological insulators. Topological insulator (TI) is a new state of quantum matter with time-reversal symmetry and non-trivial topological order. Differing from ordinary insulator with fully occupied and empty energy bands that are separated by an energy gap, topological insulator has an extremely strong SOI that the insulating energy gap is inverted, as shown in Figure 4-1(a). The twist in electronic states (band inversion) results in the formation of topological surface states besides to the bulk conduction band and valence band. The unique feature of these topological surface states is that they have helical spin texture, in other words, the spin and the momentum are locked to 90 degree. As a result, these topological surface states are immune to direct back scatterings from nonmagnetic impurities and are protected by the time-reversal symmetry,[192-193] which promise for coherent and dissipationless transport. Since the discovery of 2D (*e.g.*, HgTe quantum well) and 3D TIs (*e.g.*, Bi_2Se_3, Bi_2Te_3, Sb_2Te_3),[194-198] they have attracted extensive research interest for their exotic physical properties that could lead to dissipationless transport in the quantum spin Hall state.[192-193,199-200] The presence of surface states is supported by extensive angle-resolved photoemission spectroscopy (ARPES) measurements and transport studies,[201-207] such as Shubnikov-de Haas (SdH) and Aharonov-Bohm (AB) quantum oscillations. For example, the gapless Dirac surface states with a linear *E*-*k* dispersion in Bi_2Se_3 can be clearly seen in the ARPES data shown in Figure 4-1 (b).

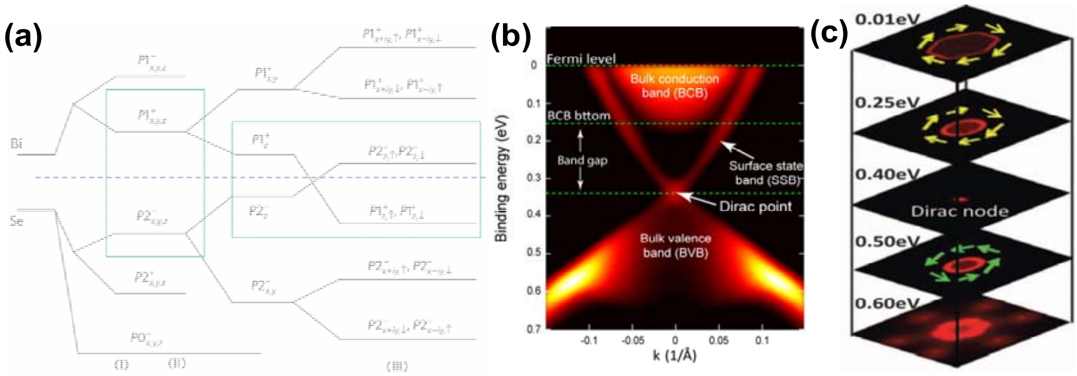

Figure 4-1. Topological insulator with spin-polarized surface states. (a) Schematic diagram of the evolution from the atomic orbitals of Bi and Se into the conduction and valence bands of Bi_2Se_3 at the Γ point. The three stages I, II and III represent the effect of turning on chemical bonding, crystal-field splitting and spin-orbit coupling, respectively. Adopted from Ref. [197].[197] (b) Typical ARPES data of Bi_2Se_3, clearly showing the Dirac gapless surface states besides to the bulk conduction band (BCB) and valence band (BVB). Adopted from Ref. [208].[208] (c) The spin-resolved ARPES data of the topological insulator $BiTlSe_2$ across the Dirac point. The observed spin textures are schematically indicated by arrows, and are opposite above and below the Dirac point. Adopted from Ref. [202].[202]

More importantly, the spin-momentum locking naturally leads to current-induced spin-polarized surface states:[209] the surface states conduction is spin-polarized once an electric current is passing through a TI film, and this spin polarization can be accordingly reversed by simply flipping the electric current direction. This charge-current induced spin polarization is illustrated in Figure 4-2.[210-211] As a result, it has been proposed to use TIs as a promising spin injection source to inject spin-polarized carriers into nonmagnetic materials, such as metal and graphene.[212-214]

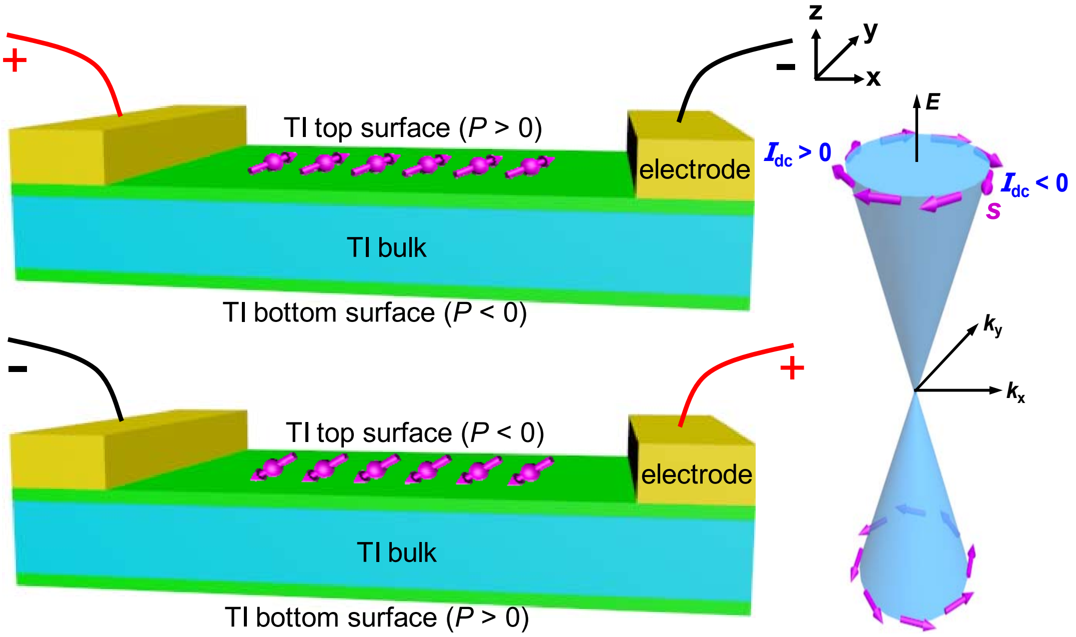

Figure 4-2. Charge current-induced spin polarization in TI. The surface states conduction is spin polarized in TI according to the spin texture and the Fermi level position. More importantly, the surface spin polarization is reversible when flipping

the electric current direction.

The presence of spin-polarized surface states has been mainly examined using optical methods. Spin-resolved ARPES has been widely used to resolve the helical spin texture at different energy levels,[201-203] and the spin texture is found to be opposite for above and below the Dirac point, as shown in Figure 4-1 (c).[202] Another approach is to use circularly polarized light to excite spin-polarized photocurrent in TI surface states.[215-217] Left- and right-circularly polarized light selectively interacts with opposite spin polarizations with components that are either parallel or anti-parallel to the wave vector of the incident light.[215] However, there has been little report of direct electrical injection or detection in TI.

Very recently, the electrical detection of charge-current-induced spin polarization was reported in Bi_2Se_3, and the spin polarization was estimated to be 0.2 per unit current.[218] Although Bi_2Se_3 has a large bulk band gap of about 0.3 eV, it is known that there are excessive Se vacancies in Bi_2Se_3 that can result in a degenerately high n-type doping density ($n_{2D} = 10^{13} \sim 10^{14}$ cm^{-2}), which places the Fermi level within the bulk conduction band.[219] The coexistence of topological surface states and 2DEG with a large tunable Rashba spin splitting on the surface of Bi_2Se_3 would complicate the spin texture.[220] To avoid the 2DEG problem, ternary TI compounds, such as $(Bi_xSb_{1-x})_2Te_3$,[221-222] have been widely investigated for their tunability to achieve low bulk carrier density with Fermi level lying in the bulk band gap and manifest topological surface states conduction. In this Chapter,[223] we describe the use of compound TI $(Bi_{0.53}Sb_{0.47})_2Te_3$ in order to achieve a low bulk carrier density (n_{2D} ~10^{12} cm^{-2}) and clean spin texture;[221] and carry out the electrical detection of the spin-polarized topological surface states conduction, using one ferromagnetic contact as the spin detector to probe the spin polarization.[218] In addition, a tunneling barrier is used to enhance the spin detection efficiency, as previously discussed in Chapter 3.4.[128] It should be pointed out that standard spin injection/detection measurement setup may not be feasible to study the spin transport in TI, due to the fact that the spin diffusion length in TI is expected to be extremely small because of strong spin-orbital interaction.[210] Also, the typical ferromagnetic spin injector is not needed here as the spin polarization in the topological surface states conduction is inherently provided by the spin-momentum locking, as illustrated in Figure 4-2.[192-193]

4.2 Electrical Spin Detection in Topological Insulator

To start, eight quintuple layers of $(Bi_{0.53}Sb_{0.47})_2Te_3$ TI thin film was grown on a high-resistivity GaAs (111)B substrate using an ultra-high vacuum Perkin Elmer MBE,[221,224] through which layer-by-layer growth with well-controlled thickness and doping concentration can be achieved. After chemical cleaning and loading into the MBE chamber, the GaAs substrate was annealed at 580 ^{o}C to remove native oxides. The TI film growth was then performed at a substrate temperature of 200 ^{o}C with high-purity Bi (99.9999%), Sb (99.999%) and Te (99.9999%) evaporated from conventional effusion cells and cracker cells. The Bi and Sb atomic ratio was fine tuned to reach the lowest bulk carrier density. The layer-by-layer growth was *in-situ* monitored by reflection high-energy electron diffraction (RHEED) pattern, as shown in Figure 4-3. Although reducing the film thickness could diminish the bulk conduction and hence enhance the surface states signal,[218] the hybridization between the top and bottom surface states would open a gap at the Dirac point, which transforms massless Dirac Fermions to massive Fermions and might also change the spin texture in TI.[225] Therefore, the thickness of eight quintuple layers in our sample was intentionally chosen to minimize the bulk conductance while avoiding the interaction between the two topological surfaces. The Bi and Sb atomic ratio was fine tuned to reach the lowest bulk carrier density. A 0.8 nm-thick aluminum (Al) layer was *in situ* deposited on top after the growth to cap the $(Bi_{0.53}Sb_{0.47})_2Te_3$ surface and prevent any environment doping and surface oxidation.[226-227] After being taken out from the chamber and exposed to air, the Al capping layer was naturally oxidized into Al_2O_3 with a thickness of about 1.2 nm, which served as the tunneling barrier for the ferromagnetic contact. This method has been widely used to produce the tunneling barrier for electrical spin injection and detection studies in various materials.[38,218,228]

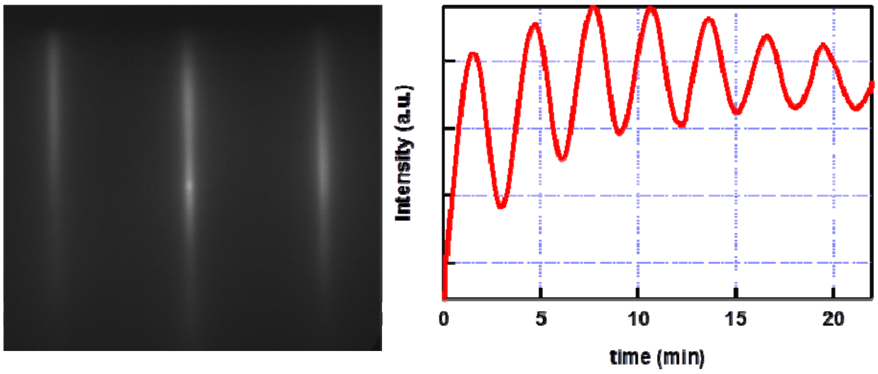

Figure 4-3. RHEED pattern during the growth of the $(Bi_{0.53}Sb_{0.47})_2Te_3$ film on the GaAs substrate. The RHEED oscillation is used to monitor the growth condition and the thin film thickness. The streaky RHEED pattern along the $[11\bar{2}0]$ direction of the as-grown surface suggests a 2D growth mode. The oscillation period indicates a growth rate of about 1 quintuple layer per 3 mins. (The data also appeared in my publication Ref. [223].[223])

HRTEM was used to investigate the TI film quality and crystalline structure. As shown in Figures 4-4(a-b), the HRTEM cross-sectional image demonstrated an abrupt and clean epitaxial interface of $(Bi_{0.53}Sb_{0.47})_2Te_3$ on the GaAs substrate, and each quintuple layer with the van der Waals gap was well resolved. The chemical composition was confirmed by the Bi, Sb and Te peaks in the EDS collected from the $(Bi_{0.53}Sb_{0.47})_2Te_3$ film, as shown in Figure 4-4(c).

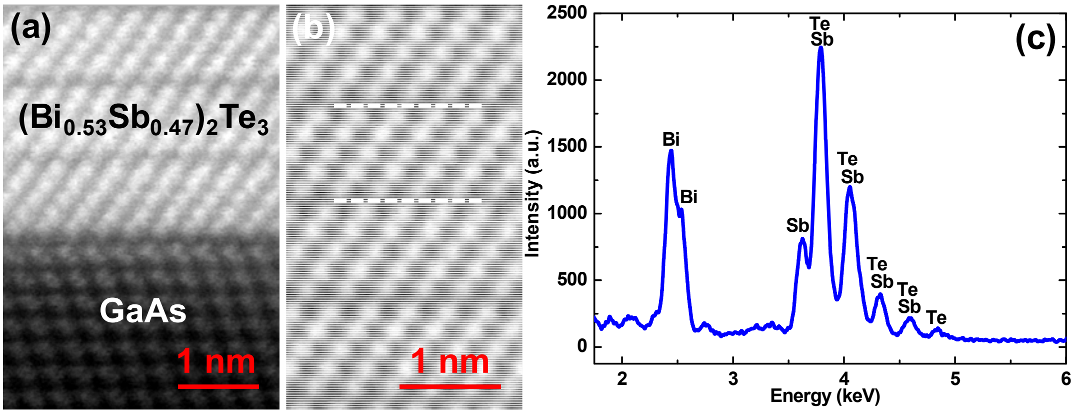

Figure 4-4. TEM analysis of the $(Bi_{0.53}Sb_{0.47})_2Te_3$ thin film. (a) Cross-sectional HRTEM image of $(Bi_{0.53}Sb_{0.47})_2Te_3$ thin film grown on a GaAs substrate with an atomically clean interface. (b) Magnified picture showing the details of the van der Waals gaps. Each quintuple layer with the van der Waals gap is well resolved, as labeled by the white dash lines. (c) EDS of the $(Bi_{0.53}Sb_{0.47})_2Te_3$ film, in which the Bi, Sb and Te peaks are well resolved. (The data also appeared in my publication Ref. [223].[223])

The AFM image was taken on the $(Bi_{0.53}Sb_{0.47})_2Te_3$ film and showed a typical terrace-like surface morphology, as shown in Figure 4-5(a).[219] The root-mean-square (RMS) roughness is calculated to be about 0.57 nm. With an *in situ* 0.8 nm-thick Al layer, it is still possible to produce a reasonably good tunneling barrier later on the $(Bi_{0.53}Sb_{0.47})_2Te_3$ film under the small Co/Al_2O_3 junction (dimension of about 400 nm by 2 μm). The ARPES spectrum was also taken from another $(Bi_{0.53}Sb_{0.47})_2Te_3$ film (without the top Al capping for better signals) to affirm the presence of Dirac surface states with a linear *E*-*k* dispersion, as shown in Figure 4-5(b). Here the photon energy in the ARPES measurement was carefully chosen to clearly show the surface states while suppressing the photoemission from the conduction band.[203,229-230] It should be pointed out that the accurate Fermi level position cannot be determined by *ex-situ* ARPES data because of optical-induced charge accumulation during the ARPES measurement as well as unintentional environmental doping over the time between the sample growth and ARPES measurement.[231-233] Nonetheless, from the ARPES spectrum, we could reconstruct the energy band diagram shown in Figure 4-5(c), and the exact Fermi level position was determined by transport measurements later.

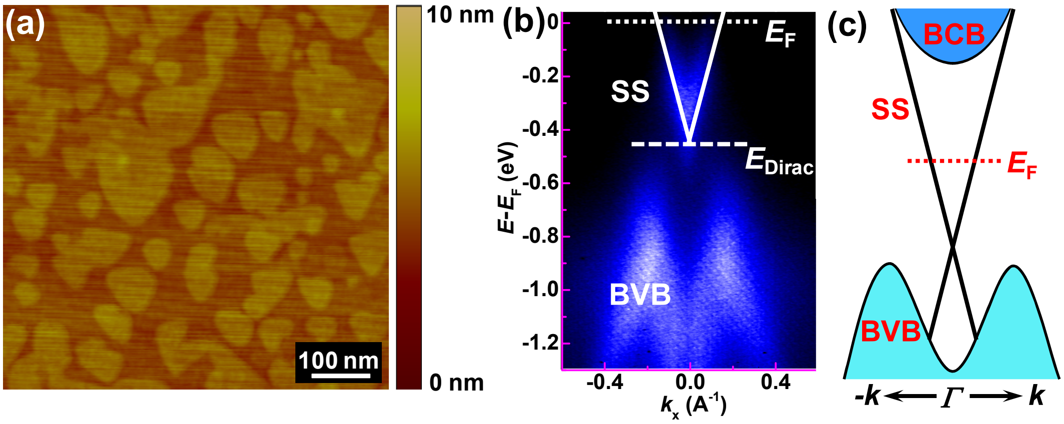

Figure 4-5. AFM and ARPES characterization of the $(Bi_{0.53}Sb_{0.47})_2Te_3$ thin film. (a) AFM image of the Al_2O_3-capped $(Bi_{0.53}Sb_{0.47})_2Te_3$ film grown on the GaAs substrate, showing a terrace-like surface morphology. (b) ARPES spectrum of the $(Bi_{0.53}Sb_{0.47})_2Te_3$ film. The Dirac surface states (SS, indicated by the solid white lines)

and the Fermi level E_{F} are shown above the Dirac point E_{Dirac}. A Fermi velocity of about $v_{\mathrm{F}} = 4.3 \times 10^5\ \mathrm{m/s}$ can be extracted from the linear $E = \hbar k v_{\mathrm{F}}$ relation (indicated by the white lines). (d) Schematic band structure of $(Bi_{0.53}Sb_{0.47})_2Te_3$ illustrating the bulk conduction band (BCB), bulk valence band (BVB), and the Dirac surface states (SS). (The data also appeared in my publication Ref. [223].[223])

After the growth, the $(Bi_{0.53}Sb_{0.47})_2Te_3$ thin film was patterned into Hall bar structures using photolithography and reactive ion etching. Then, another photolithography followed by electron beam evaporation was used to pattern 10 nm/100 nm thick titanium/gold (Ti/Au) metal pads as nonmagnetic contacts to the TI channel. Finally, 40 nm thick cobalt (Co) contacts were defined by electron beam lithography and electron beam evaporation as the ferromagnetic contacts to the channel, and a 5 nm Al_2O_3 layer was also evaporated *in-situ* to prevent subsequent oxidation of the Co electrodes. The microscope image of the final device for spin detection is shown in Figure 4-6(a). To verify the tunneling nature of the Co/Al_2O_3 contact to the $(Bi_{0.53}Sb_{0.47})_2Te_3$ channel, temperature-dependent *I*-*V* measurements were performed from 2 K to 250 K, as shown in Figure 4-6(b). The nonlinear *I*-*V* characteristics suggest tunneling dominant transport through the 1.2 nm Al_2O_3 barrier. Figure 4-6(c) shows the extracted temperature-dependent zero-bias resistance (ZBR) of the Co/Al_2O_3 contact to the $(Bi_{0.53}Sb_{0.47})_2Te_3$ channel in the temperature range from 2 K to 250 K. It is noted that there is some noticeable temperature dependence in the ZBR,[234] which could be attributed to the presence of non-tunneling (*e.g.*, thermionic emission) conduction channels resulting from the surface roughness in our device. However, the ZBR only was increased by about 7 times in the temperature range of 2-250 K and slowly varied at low temperatures (T < 50 K, where the thermionic emission was suppressed), indicating that the tunneling characteristic still dominated the transport through the Co/Al_2O_3 contact.[31,234] To further confirm this, we applied the Brinkman-Dynes-Rowell (BDR) tunneling model to fit the temperature-dependent conductance-voltage (G-V) curves,[235] as shown in Figure 4-6(d). Here the parabolic characteristics of G-V curves also affirm the tunneling transport,[235-237] which is essential to enhance the spin detection efficiency.[20,128]

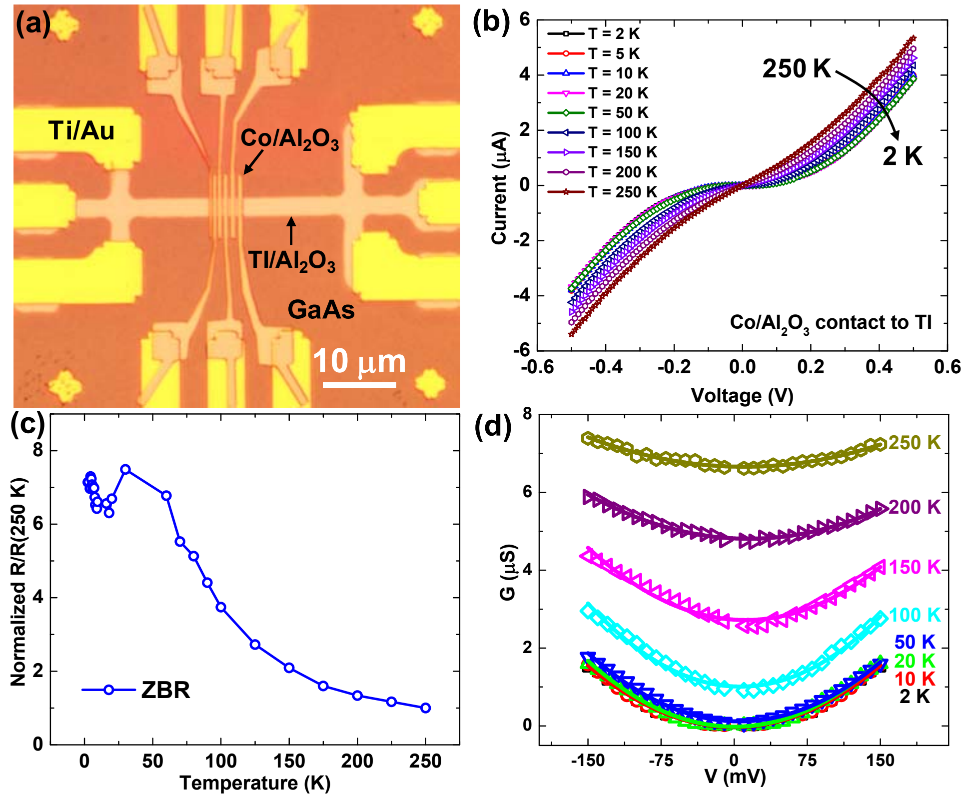

Figure 4-6. Characterization of the Co/Al_2O_3 ferromagnetic tunneling contact. (a)

The microscope image of the as-fabricated TI Hall-bar device with Co/Al_2O_3 ferromagnetic tunneling contacts on the channel. (b) Temperature-dependent *I-V* curves measured from the Co/Al_2O_3 contact on the TI channel. The nonlinear *I-V* characteristics suggest tunneling transport through the 1.2 nm Al_2O_3. (c) ZBR of the Co/Al_2O_3 contact to the $(Bi_{0.53}Sb_{0.47})_2Te_3$ channel in the temperature range from 2 K to 250 K. (d) Parabolic G-V curves of the Co/Al_2O_3 contact to the $(Bi_{0.53}Sb_{0.47})_2Te_3$ channel, which are well fitted by the BDR tunneling model. (The data also appeared in my publication Ref. [223].[223])

Figure 4-7(a) shows the schematic device structure and measurement setup for the electrical detection of spin-polarized surface states conduction in $(Bi_{0.53}Sb_{0.47})_2Te_3$. Here two outer nonmagnetic contacts (Ti/Au) were used to pass electric current (along the *x*-axis) through the TI channel, while one ferromagnetic tunneling contact (Co/Al_2O_3) was used to detect the spin polarization of surface states conduction. A lock-in technique was employed to increase the signal-to-noise ratio, and a 4-probe configuration was also adopted to exclude the contact resistance and any spurious signals from the contact. An in-plane magnetic field was applied along the easy axis (*y*-axis) of the Co electrode to control its magnetization direction. Meanwhile, the spin polarization direction of the surface states conduction was determined by the electric current direction and the spin-momentum locking. It should be pointed out that the electron spin $\boldsymbol{s}$ is anti-parallel to its magnetic moment $\boldsymbol{m}_s$ because of the negative charge of electron.[238] In our $(Bi_{0.53}Sb_{0.47})_2Te_3$ film, the Fermi level is above the Dirac point, so the spin texture of surface states is expected to be clockwise[201-203] from spin-resolved ARPES measurements as illustrated in Figure 4-7(b), that is, the spin polarization ***s*** is pointing along -*y* direction for momentum ($k_x > 0$, $k_y = 0$), while along +*y* direction for momentum ($k_x < 0$, $k_y = 0$).

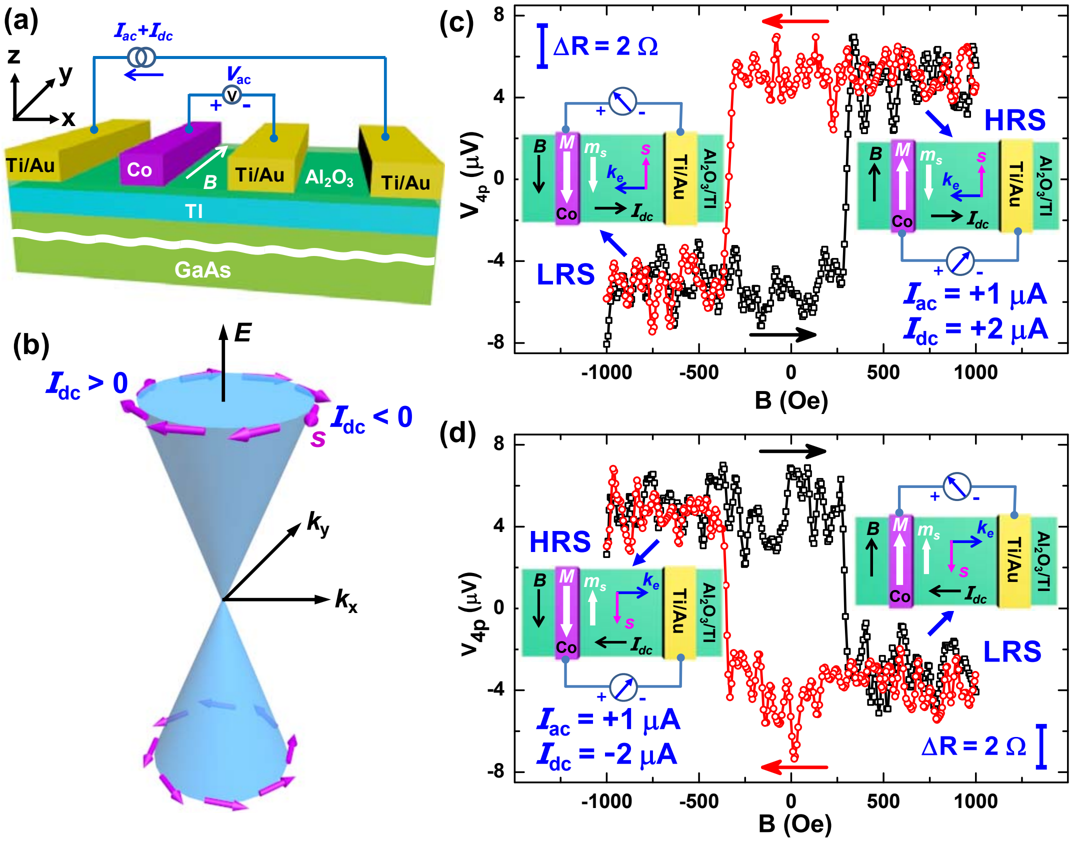

Figure 4-7. Electrical detection of the spin-polarized surface states conduction in $(Bi_{0.53}Sb_{0.47})_2Te_3$. (a) Schematic illustration of the device structure with one ferromagnetic tunneling Co/Al_2O_3 contact for spin detection. The measurement setup with a 4-probe configuration and a lock-in technique is also illustrated. (b) Schematic illustration of the helical spin texture of the surface states in TI: clockwise spin

texture above the Dirac point while counter-clockwise spin texture below the Dirac point. (c-d) The measured voltage (resistance) at $T = 1.9$ K as the in-plane magnetic field is swept back and forth under dc bias of $I_{\mathrm{dc}} = +2$ μA and $I_{\mathrm{dc}} = -2$ μA, respectively. The parabolic background MR was subtracted. The scale bar represents a corresponding resistance change of 2 Ω. The red and black arrows indicate the magnetic field sweeping direction. The insets show the high-resistance state (HRS) and low-resistance state (LRS), determined by the relative orientation between the Co electrode magnetization M and the spin polarization s of surface states. The electron spin s is anti-parallel to its magnetic moment m_{s} because of the negative charge of electron. (The data also appeared in my publication Ref. [223].[223])

Figure 4-7(c) shows the measured hysteresis of the measured voltage at $T = 1.9$ K as the in-plane magnetic field was swept back and forth under a constant ac current of $I_{\mathrm{ac}} = 1$ μA plus a dc bias of $I_{\mathrm{dc}} = +2$ μA. For clarity, the trivial parabolic MR background, originating from the $(\mathrm{Bi}_{0.53}\mathrm{Sb}_{0.47})_2\mathrm{Te}_3$ channel between the two voltage probes, was subtracted. The measured voltage (resistance) depends on the relative orientation between the surface states spin polarization and the Co electrode magnetization: a low resistance state (LRS) when the electron magnetic moment $\boldsymbol{m}_{\mathbf{s}}$ was parallel to the Co magnetization $\boldsymbol{M}$ (hence $\boldsymbol{s}$ was anti-parallel to $\boldsymbol{M}$), and a high resistance state (HRS) when $\boldsymbol{m}_{\mathbf{s}}$ was anti-parallel to $\boldsymbol{M}$ (hence $\boldsymbol{s}$ was parallel to $\boldsymbol{M}$). Such configuration is analogous to that in a typical MTJ, in which the junction resistance is determined by the relative magnetization orientation between the two ferromagnetic layers. The abrupt change in the voltage (resistance) corresponded to the magnetization switching of the Co electrode (with a width of about 400 nm) at the coercive field of about $H_c \sim 300$ Oe, which was estimated from the AMR measurement, as to be shown in Figure 4-9. The inset shows the schematic illustration of the relative orientation between the surface states spin polarization and the Co electrode magnetization (for $I_{dc} = +2$ μA): HRS for positive magnetic field ($\boldsymbol{M}$ // $-\boldsymbol{m_s}$ // $\boldsymbol{s}$) while LRS for negative magnetic field ($\boldsymbol{M}$ // $\boldsymbol{m_s}$ // $-\boldsymbol{s}$). It is noted that the HRS and LRS in our voltage hysteresis is shown opposite from that observed in Bi_2Se_3;[218] however, the interpreted spin texture in this way is consistent with the reported spin-resolved APRES data as illustrated in Figure 4-7(b)[201-203] Furthermore, if the electric current direction was flipped to $I_{dc} = -2$ μA, then the LRS and HRS were also reversed,[218] as shown in Figure 4-7(d): LRS for positive magnetic field ($\boldsymbol{M}$ // $\boldsymbol{m_s}$ // $-\boldsymbol{s}$) while HRS for negative magnetic field ($\boldsymbol{M}$ // $-\boldsymbol{m_s}$ // $\boldsymbol{s}$). More than ten $(Bi_{0.53}Sb_{0.47})_2Te_3$ devices have been measured, and the current-reversible voltage hysteresis was observed in multiple samples. This result directly demonstrates the unique spin-momentum locking feature for the topological surface states conduction in TI.

It should be pointed out that this current-reversible hysteresis cannot originate from the Co contact itself due to effects including AMR, tunneling anisotropic magnetoresistance (TAMR) and anomalous Hall effect (AHE).[7,218,239-240] To further rule out those effects and also estimate the coercive field of the 400 nm-wide Co contact, several control experiments have been carried out. We first fabricated another sample without the Al (Al_2O_3) layer under the same process condition for the sample presented in the main text. In this control sample, nonlinear *I-V* characteristic was not observed. Instead, the direct Co contact to the $(Bi_{0.53}Sb_{0.47})_2Te_3$ channel showed Ohmic behavior in the whole temperature range of 2 K to 250 K, as shown in Figure 4-8(a). Also, in this control sample, we performed the same measurement procedure to detect the spin polarization of surface states conduction as Figure 4-7; however, no voltage hysteresis was observed for both positive and negative current biases. Instead, only a parabolic MR background from the $(Bi_{0.53}Sb_{0.47})_2Te_3$ channel was measured, as shown in Figure 4-8(b). This result confirmed the critical role of the Al_2O_3 barrier in detecting the spin polarization.

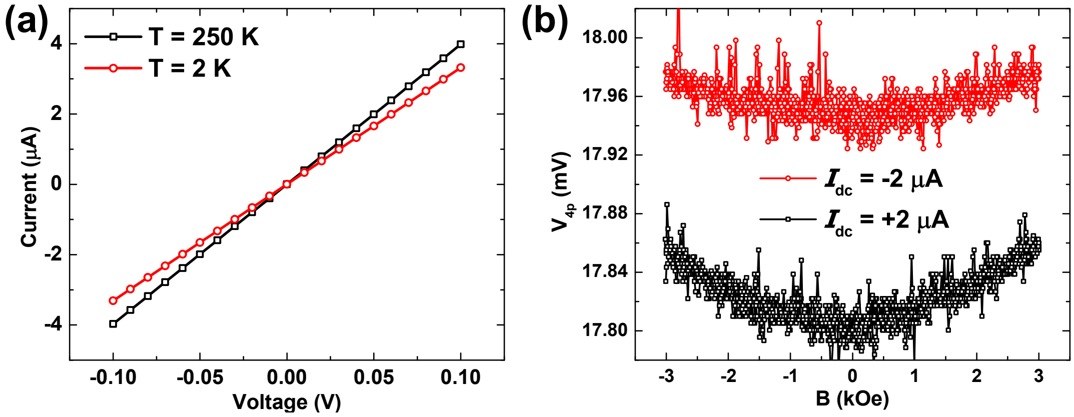

Figure 4-8. Control experiment without the Al_2O_3 barrier. (a) Temperature-dependent *I-V* curves of the direct Co contact to the $(Bi_{0.53}Sb_{0.47})_2Te_3$ channel in the control sample, showing Ohmic characteristics. (b) Raw data of the measured voltage in the control sample at $T = 1.9$ K as the in-plane magnetic field is swept back and forth. No voltage hysteresis was observed for both positive and negative current biases. (The data also appeared in my publication Ref. [223].[223])

In addition, AMR measurement was carried out under both positive and negative current biases, as shown in Figure 4-9. Here we can clearly see a switching field of about 300 Oe, which agrees well with the switching field (also about 300 Oe) in the resistance hysteresis measured in Figure 4-7. Also, no apparent difference was observed for opposite current directions, which confirmed that the observed current-reversible resistance hysteresis was not originated from the AMR signal of the Co contact. Also, the Curie temperature of Co is about 1400 K; therefore any magnetic signal (AMR, AHE, *etc*) from the Co contact itself should persist up to high temperature. This also suggests that the resistance hysteresis (which depended on the current direction and diminished above 10 K) did not come from the Co contact itself.

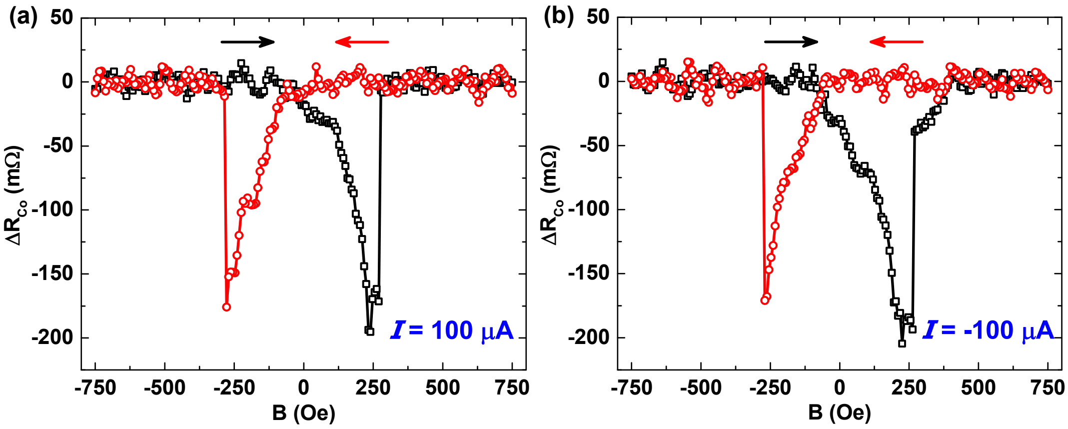

Figure 4-9. AMR of the 400 nm-wide Co electrode under a current bias of (a) 100 μA, and (b) -100 μA, respectively. They both showed a coercive field of about 300 Oe. The black and red arrows indicate the in-plane magnetic field sweeping direction (along the Co electrode easy axis). No apparent difference was observed for opposite

current directions. (The data also appeared in my publication Ref. [223].[223])

To further verify that the hysteresis is closely correlated with the magnetization switching of the Co electrode, the magnetic field was rotated in the y-z plane toward the out-of-plane direction. As illustrated in Figure 4-10(a), there is an angle θ between the applied magnetic field (in the y-z plane) and the easy y-axis of the Co electrode. Figures 4-10(b-c) show the voltage hysteresis curves at different rotation angles θ under dc bias of $I_{\mathrm{dc}} = +2\ \mu\mathrm{A}$ and $I_{\mathrm{dc}} = -2\ \mu\mathrm{A}$, respectively. Again the trivial parabolic MR background was subtracted in all the curves for clarity. The switching field H_{sw} was found to increase with the rotation angle for both bias conditions, and the hysteresis completely vanished as the rotation angle approached $\theta = 90^{\mathrm{o}}$. Figure 4-10(d) further plots the switching field H_{sw} as a function of the rotation angle θ, which can be well fitted with the $H_c/\cos(\theta)$ relation. This result suggests that the abrupt change in the voltage (resistance) occurred when the in-plane component (along the easy y-axis) of the applied magnetic field reached the coercive field of the Co electrode, that is, the magnetization switching of the Co electrode. Therefore, the abrupt switching between the LRS and the HRS in the voltage (resistance) hysteresis was indeed correlated with the change in the relative orientation between the surface states spin polarization and the Co electrode magnetization. It should be pointed out that the out-of-plane component of the applied magnetic field (less than 1 kOe) was much smaller than the Co saturation field along the hard z-axis (typically tens of kOe), hence it did not change the Co magnetization orientation but only contributed to the parabolic MR background. In addition, the small out-of-plane magnetic field did not affect the surface states because that the induced gap opening in the surface states was negligible.[241]

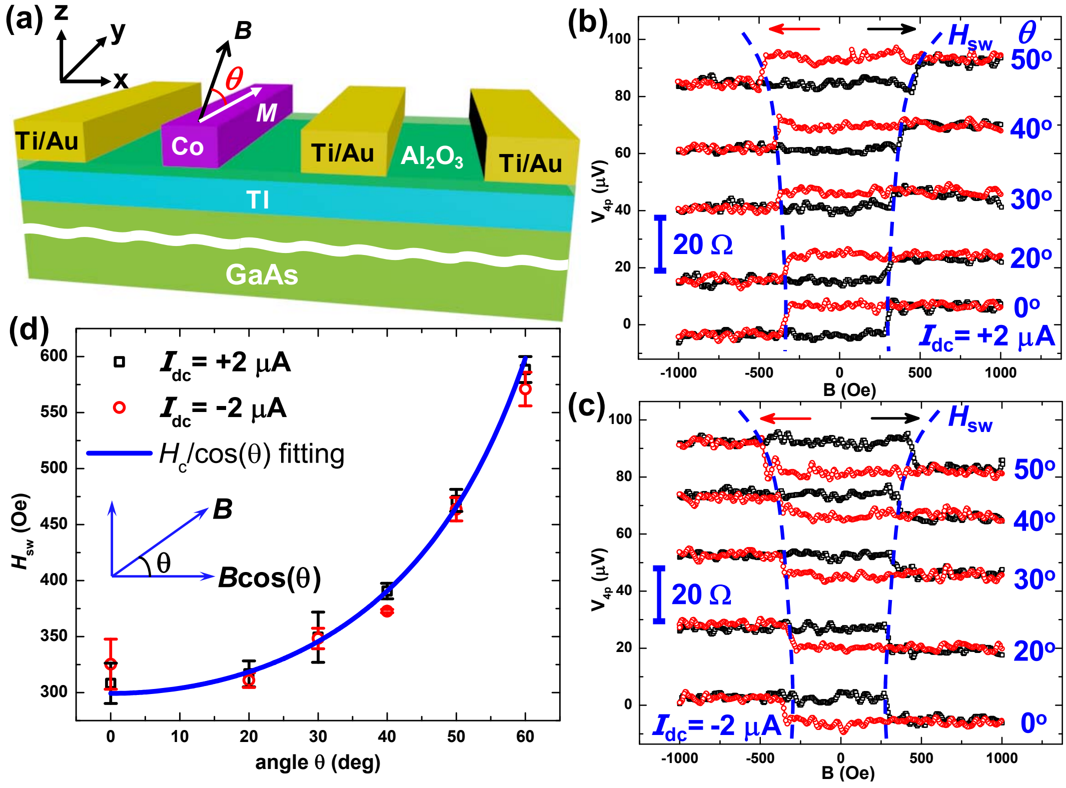

Figure 4-10. Angle-dependent measurements. (a) Schematic illustration of the magnetic field (black arrow) rotation in the *y-z* plane. (b-c) Voltage hysteresis curves at different rotation angles under dc bias of I_{dc} = +2 μA and I_{dc} = -2 μA, respectively. The red and black arrows indicate the magnetic field sweeping direction. The parabolic MR background was subtracted in all the curves. The curves are intentionally offset for clarity, and the scale bar represents a corresponding resistance change of 20 Ω. The blue dash lines mark the switching fields increasing with

rotation angle. (d) The extracted switching fields (data points) at different rotation angles is well fitted by the $H_c/\cos(\theta)$ relation (blue line), indicating only the magnetic field component along the y-axis determines the magnetization switching of the Co electrode. The error bars are calculated from positive and negative switching fields in multiple measurements. (The data also appeared in my publication Ref. [223].[223])

Furthermore, temperature-dependent voltage hysteretic data were measured from 1.9 K to 10 K, and the results are shown in Figure 4-11(a) for the bias of I_{dc} = -2 μA. We can further define the spin voltage amplitude as $\Delta V = V_{AP} - V_P = I_{ac} \times (R_{AP} - R_P)$, in which V_{AP} (R_{AP}) and V_P (R_P) represent the measured voltage (resistance) in the HRS and LRS, respectively. The temperature-dependent spin voltage amplitude is plotted in Figure 4-11(b). Overall, the spin signal amplitude decreases as the temperature increases,[218] suggesting that the effective spin polarization of the total current decreases. This could be attributed to that with the temperature increasing: 1) the bulk conduction increases due to thermally activated bulk dopants, so that the relative contribution from the spin-polarized surface states conduction decreases;[231] 2) inelastic scatterings such as phonon scatterings increase so that the spin polarization of surface states conduction also decreases.

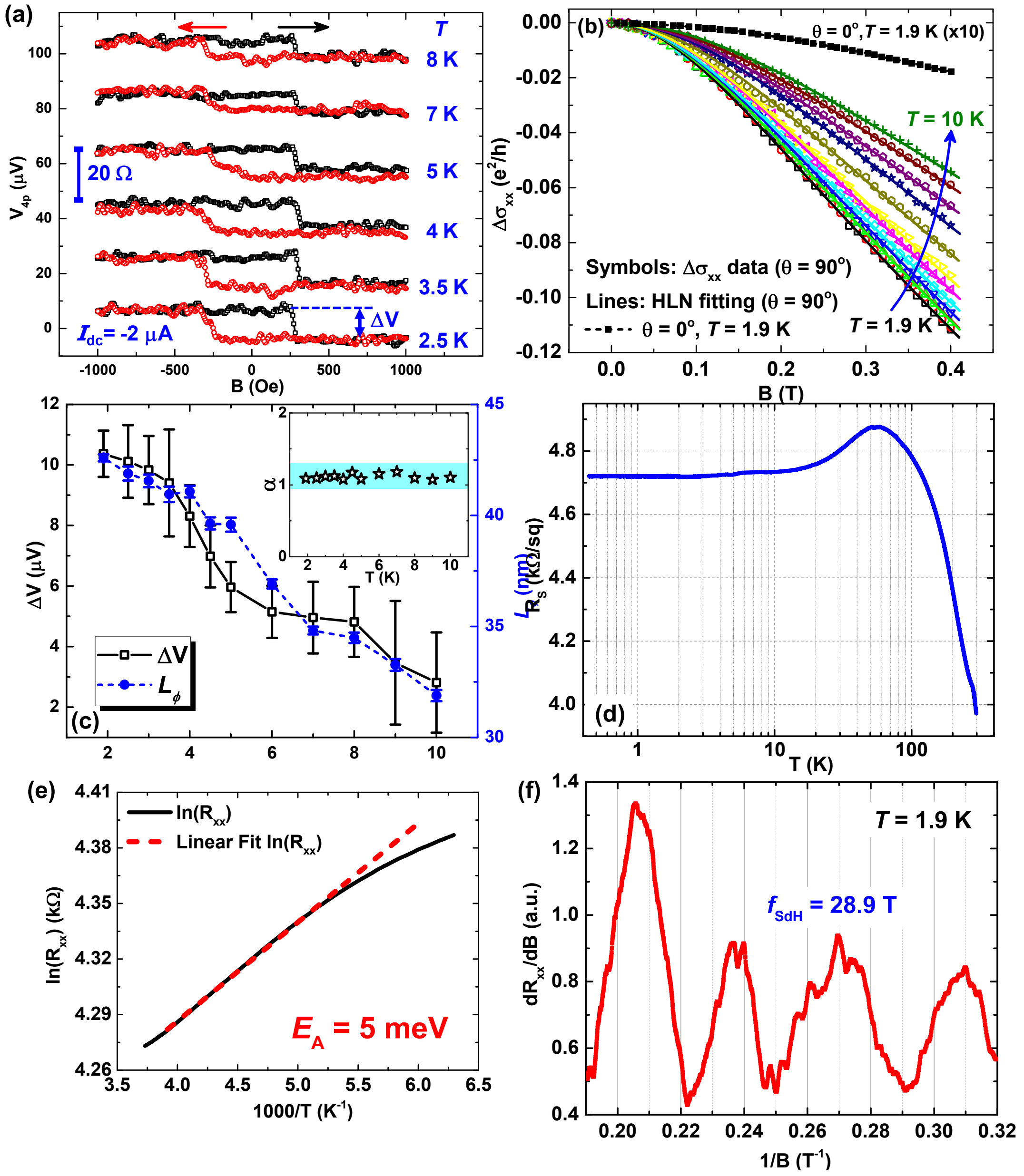

Figure 4-11. Temperature dependence of the spin signal. (a) Temperature-dependent voltage hysteresis curves under dc bias of I_{dc} = -2 μA. The red and black arrows indicate the magnetic field sweeping direction. The parabolic MR background was subtracted in all the curves. The curves are intentionally offset for clarity, and the

scale bar represents a corresponding resistance change of 20 Ω. (b) Background-subtracted low-field magneto-conductivity at different temperatures as plotted with open symbols. Lines are fitted curves by the standard HLN theory. For comparison, the parabolic in-plane magneto-conductivity ($\theta = 0^{o}$, multiplied by a factor of 10 for clarity) at T = 1.9 K is also plotted with solid symbols. (c) Extracted spin voltage signal amplitude at different temperatures up to 10 K. In general, the signal amplitude decreases as the temperature increases, indicating the reduction of effective spin polarization of the total current. The error bars are calculated from forward and backward sweeps of the magnetic field in multiple measurements. The temperature-dependent phase coherence length from the HLN fitting of the low-field magneto-conductivity is also plotted, showing similar temperature dependence. The inset shows the temperature-dependent prefactor α of about 1, indicating both top and bottom surface conductions. (d) Temperature-dependent sheet resistance of the $(Bi_{0.53}Sb_{0.47})_2Te_3$ film. The sheet resistance remains nearly constant for temperature below 2 K. (e) Arrhenius plot of $\ln(R_{xx})$ versus $1000/T$, and the fitting at the high-temperature regime yields an activation energy of about 5 meV. (f) SdH oscillation in the longitudinal resistance at T = 1.9 K. The oscillation frequency is estimated to be f_{SdH} = 28.9 T. (The data also appeared in my publication Ref. [223].[223])

To explain the temperature dependence of the surface states conduction more clearly, standard magneto-transport measurements were performed on the Hall bar structure patterned on the same $(Bi_{0.53}Sb_{0.47})_2Te_3$ film (see Figure 4-6(a) for the device structure and dimension). In the Hall measurements, the longitudinal resistance (R_{xx}) and transverse resistance (R_{xy}) were measured when sweeping the out-of-plane magnetic field. In the strong spin-orbit interaction limit of 2D electron systems, the standard Hikami-Larkin-Nagaoka (HLN) theory is often applied to model the weak-field conductivity variation:[226,229,242]

$$\Delta\sigma = \sigma(B) - \sigma(0) = -\frac{\alpha e^2}{2\pi^2\hbar}\left[\ln\left(\frac{\hbar}{4eBL_\phi{}^2}\right) - \psi\left(\frac{1}{2} + \frac{\hbar}{4eBL_\phi{}^2}\right)\right] \qquad (4-1),$$

where α is the prefactor, e is the electron charge, $\hbar$ is the reduced Planck's constant, B is the magnetic field, L_ϕ is the phase coherence length, and ψ is the digamma function. Here the low-field magneto-conductivity was fitted by the HLN theory in the temperature range between 1.9 K and 10 K, as shown in Figure 4-11(b).[226,229,242] The extracted phase coherence length is then plotted in Figure 4-11(c), which shows a similar temperature dependence as the measured spin voltage amplitude. The phase coherence length decreases with increasing temperature, indicating that the surface states conduction is diminished. Besides, as shown in the inset of Figure 4-11(c), the obtained prefactor α from the HLN fitting slowly varied around 1, which is consistent with our previous observation of both top and bottom surface states conduction in the $(Bi_{0.53}Sb_{0.47})_2Te_3$ film.[221] Besides, it should be pointed out that, in Figure 4-11(b), the measured in-plane magneto-conductivity is dominated by the trivial parabolic magnetoresistance, and the magnitude is much smaller than the out-of-plane magneto-conductivity (less than 2%). This result suggests that the bulk contribution in the out-of-plane low-field magneto-conductivity is negligible, and hence the extracted phase coherence length in Figure 4-11(c) is mainly a characteristic of the topological surface states conduction.

In order to estimate the effective spin polarization of the surface states conduction, low-temperature and high-field transport measurements were carried out to extract important information of the surface states conduction. Figure 4-11(d) shows the temperature-dependent sheet resistance of the $(Bi_{0.53}Sb_{0.47})_2Te_3$ film. The semiconducting behavior at high temperature (> 60 K) corresponded to the freeze-out effect of the bulk carriers. A small activation energy of about 5 meV was estimated by the Arrhenius plot as shown in Figure 4-11(e). This indicates that the Fermi level at low temperature is within the bulk band gap. Blow 60 K, the decease of resistance as temperature decreases is a signature of the metallic surface states, and the sheet resistance remains nearly constant of R_{sh} = 4.74 kΩ/□ for temperature below 2 K, indicating a temperature-independent surface conduction.[231] Similar saturation behavior at low temperatures was also observed in many other TI thin films and nanostructures.[221-222,231,243] As an characteristic feature of 2D surface conduction, the SdH oscillation in the longitudinal resistance at T = 1.9 K was also analyzed.[204] Figure 4-11(f) plots the first-order derivative of R_{xx} versus the inverse of the magnetic field, revealing a SdH oscillation frequency of f_{SdH} = 28.9 T. From here we can obtain the carrier density of the 2D surface states conduction $n_{\mathrm{2D,SS}} = ef_{\mathrm{SdH}}/h = 7.0 \times 10^{11}\ \mathrm{cm}^{-2}$,[244] where e is the electron charge and h is the Planck's constant. The Fermi vector can also be calculated as $k_{\mathrm{F}} = \sqrt{4\pi e f_{\mathrm{SdH}}/h} = 0.0296\ \mathrm{Å}^{-1}$.[204-205] Using the Fermi velocity of $v_{\mathrm{F}} = 4.3 \times 10^5\ \mathrm{m/s}$ extracted from the ARPES spectrum in

Figure 4-5(b), the Fermi energy can be estimated to be $E_{\mathrm{F}} = \hbar k_{\mathrm{F}} v_{\mathrm{F}} = 83$ meV.[204-205] The surface conductance can be defined as $\sigma_{\mathrm{SS}} = e n_{2\mathrm{D,SS}} \mu_{\mathrm{SS}} = 0.112$ mS, assuming a surface mobility of $\mu_{\mathrm{SS}} = 1000\ \mathrm{cm}^2/\mathrm{Vs}$,[205,221] while the total conductance is $\sigma_{\mathrm{total}} = 1/R_{\mathrm{sh}} = 0.211$ mS at $T = 1.9$ K. Therefore, the 2D surface states account for $\alpha = \sigma_{\mathrm{SS}}/\sigma_{\mathrm{total}} = 53\%$ of the total conductance,[205] indicating surface-dominated conduction in the $(Bi_{0.53}Sb_{0.47})_2Te_3$ film.[231]

Similar current-induced spin polarization has been reported very recently in the Bi_2Se_3 thin film,[218] in which the spin voltage amplitude $\Delta V = V_{AP} - V_P$, or equivalently the change in resistance $\Delta R = R_{AP} - R_P = \Delta V / I_{ac}$, was described as:[245]

$$\Delta R = \alpha P_{\mathrm{FM}} (\vec{p} \cdot \widehat{M}) R_{\mathrm{B}} \qquad (4-2),$$

where $\vec{p}$ is the degree of the spin polarization per unit current along the *x* direction, $\widehat{M}$ is the unit vector along the ferromagnetic electrode magnetization, $G_{\mathrm{B}} = 1/R_{\mathrm{B}}$ is the ballistic conductance of the TI channel, which is given by the quantum conductance times the number of modes in the TI channel:

$$G_{\mathrm{B}} = \frac{e^2}{h} \times \frac{k_{\mathrm{F}} W}{\pi} \qquad (4-3).$$

Here k_{F} is the Fermi vector and W is the width of the TI channel. With $\Delta R = 2 \times 10^{-3}\ \Omega$ and a surface conductance ratio of $\alpha = 1/23$ (calculated from 1 divided by the total film thickness), the degree of spin polarization per unit current in Bi_2Se_3 was estimated to be $\vec{p} = 0.2$ at $T = 8$ K. If we follow the same procedure, we can then estimate the current-induced spin polarization in the $(Bi_{0.53}Sb_{0.47})_2Te_3$ to be $\vec{p} = 0.43 \pm 0.03$ at $T = 1.9$ K, given that $k_{\mathrm{F}} = 0.0296\ \text{Å}^{-1}$, and $W = 2.5\ \mu\mathrm{m}$ in our device.

This value is closer to the theoretical prediction of 2/π.[245] It is also noted that the resistance change (several Ω) here in our $(Bi_{0.53}Sb_{0.47})_2Te_3$ device is more than three orders of magnitudes higher than that (several 10^{-3} Ω) observed in the Bi_2Se_3 device. This could be partially attributed to the much lower carrier density (n_{2D} ~10^{12} cm^{-2} versus ~10^{13} cm^{-2} in Bi_2Se_3) and hence higher surface states conduction ratio in our $(Bi_{0.53}Sb_{0.47})_2Te_3$ thin film.

It should be pointed out that this quantum transport model proposed assumed a coherent transport in the TI channel and could overestimate the spin polarization.[245] The applicability of this quantum transport model needs to be carefully justified because that the electron transport in the Bi_2Se_3 film (dimension of tens of microns) is far away from the coherent regime, considering a typical phase coherence length of tens of nanometers in Bi_2Se_3.[226] Besides, it did not consider the spin detection efficiency through the ferromagnetic tunneling contact, which could be much less than 100%, depending on the contact quality. To take into account the incoherent transport and the spin detection efficiency, we established a new model like that in standard spin injection and detection in semiconductors.[42] The measured voltage difference $\Delta V = V_{AP} - V_P$ can be interpreted to probe the electrochemical potential (quasi Fermi level) difference between the majority and minority spin directions. The measured spin voltage amplitude can be approximately formulated in a similar fashion as standard spin injection and detection in semiconductors:[42]

$$\Delta V = \alpha \frac{\gamma P_{\mathrm{Co}}}{e} \Delta\mu \qquad (4-4),$$

where $\alpha = \sigma_{\mathrm{SS}}/\sigma_{\mathrm{total}}$ is the surface conductance ratio, γ is the spin detection efficiency through the Co/Al_2O_3 tunnel contact, $P_{\mathrm{Co}} = (n_{\mathrm{Co}\uparrow} - n_{\mathrm{Co}\downarrow})/(n_{\mathrm{Co}\uparrow} + n_{\mathrm{Co}\downarrow})$ is the spin polarization of the Co electrode with $n_{\mathrm{Co}\uparrow}$ ($n_{\mathrm{Co}\downarrow}$) being the electron density with the majority (minority) spin direction, $\Delta\mu = \mu_\uparrow - \mu_\downarrow$ is the splitting in the spin-dependent electrochemical potential between the majority and minority spin directions, which can be further derived as:

$$\Delta\mu = \frac{n_{\mathrm{SS}\uparrow} - n_{\mathrm{SS}\downarrow}}{\mathrm{N}(E_{\mathrm{F}})} = \frac{n_{\mathrm{SS}\uparrow} - n_{\mathrm{SS}\downarrow}}{n_{\mathrm{SS}\uparrow} + n_{\mathrm{SS}\downarrow}} \times \frac{n_{\mathrm{SS}\uparrow} + n_{\mathrm{SS}\downarrow}}{\mathrm{N}(E_{\mathrm{F}})} = P_{\mathrm{SS}} \times \frac{n_{\mathrm{total}}}{\mathrm{N}(E_{\mathrm{F}})} \qquad (4-5),$$

where $P_{\mathrm{SS}} = (n_{\mathrm{SS}\uparrow} - n_{\mathrm{SS}\downarrow})/(n_{\mathrm{SS}\uparrow} + n_{\mathrm{SS}\downarrow})$ is the effective spin polarization of the surface states conduction, $\mathrm{N}(E_{\mathrm{F}})$ is the density of states at the Fermi level. For the 2D Dirac surface states with a linear *E*-*k* relation, the density of states is proportional to the energy as $\mathrm{N}(E) = |E|/[\pi(\hbar v_{\mathrm{F}})^2]$, in which $\hbar$ is the reduced Planck's constant and v_{F} is the Fermi velocity.[246] Then by integration in the energy space,

$$n_{\mathrm{total}} = \int_0^{E_{\mathrm{F}}} \mathrm{N}(E)\,\mathrm{d}E = \frac{1}{2} E_{\mathrm{F}} \mathrm{N}(E_{\mathrm{F}}) \qquad (4-6),$$

we can rewrite the spin voltage amplitude as:

$$\Delta V = \alpha \frac{\gamma P_{\mathrm{Co}} E_{\mathrm{F}}}{2e} P_{\mathrm{SS}} \qquad (4-7).$$

From our measurement results shown in Figure 4(b), $\Delta V = (10.4 \pm 0.8\,)$ µV at T = 1.9 K. Using the values of $\alpha = \sigma_{\mathrm{SS}}/\sigma_{\mathrm{total}} = 53\%$, $E_{\mathrm{F}} = 83$ meV from the above SdH oscillations analysis in the longitudinal resistance R_{xx}, and $P_{\mathrm{Co}} = 42\%$,[173] $\gamma = 11\%$ for the Co/Al_2O_3 tunnel junction from literature,[20] we can then calculate the effective spin polarization of the surface states conduction in $(Bi_{0.53}Sb_{0.47})_2Te_3$ to be $P_{\mathrm{SS}} =$

(1.02 ± 0.08) %. This is smaller than the theoretical predication of about 50% spin polarization for the 3D TI surface states from first-principle calculations.[209] Such deviation can be probably attributed to that the dimension of the top surface in our device (in micron scale) is much larger than the typical mean-free path and phase coherence length (tens to hundreds nanometers as shown in Figure 4-11(c)),[204-205,226] hence the carrier transport through the surface states suffers from considerable scatterings. Another possible reason could be the overestimation of the spin detection efficiency in the non-ideal Co/Al_2O_3 tunneling contact, considering that the $(Bi_{0.53}Sb_{0.47})_2Te_3$ surface has a terrace-like morphology. The spin injection/detection process is known to be very sensitive to the surface roughness, which would induce interface traps or local magnetostatic fields that could dramatically affect the spin detection process.[27] In addition, the potential contribution from the bulk states (especially the Rashba spin-splitting states with an opposite spin texture to the topological surface states) could also lower the observed spin polarization. To further enhance the spin signal and spin polarization in the future, one effective approach according to Equation (4-7) is to tune the Fermi energy and to enhance the surface conduction ratio, which can be achieved through doping and gate control.[221,224] Besides, improving the TI film quality (e.g., surface morphology) could also help enhance the observed spin signal.

To sum up, we have successfully demonstrated the electrical detection of spin-polarized surface states conduction in the $(Bi_{0.53}Sb_{0.47})_2Te_3$ TI film using a Co/Al_2O_3 ferromagnetic tunneling contact. By changing the directions of both the magnetic field and the electric current, reversible voltage (resistance) hysteresis was observed up to 10 K, in which the HRS and LRS were obtained from the relative orientation between the Co magnetization and the spin polarization of topological surface states. It was further verified by angle-dependent measurements that the abrupt change in the voltage (resistance) indeed corresponded to the magnetization switching of the Co electrode. These transport results affirmed the spin-momentum locking feature of the helical surface states enabled by the strong spin-orbit interaction and the time-reversal symmetry in TI. The spin voltage amplitude was quantitatively analyzed to yield an effective spin polarization of about 1.02% for the surface states conduction in $(Bi_{0.53}Sb_{0.47})_2Te_3$. The measured low spin polarization could be due to the short mean-free path and phase coherence length in TI and the relatively rough TI surface morphology that limits the spin detection efficiency. From our analysis, it is suggested that this value can be further enhanced by tuning the Fermi level and increasing the surface states conduction ratio. Our findings demonstrated an exotic feature of spin-polarized surface states in TI from electrical transport measurements. The present results may pave the road to explore novel energy-efficient spintronic devices with dissipationless transport.

Chapter 5

Summary

5.1 Conclusion

In this dissertation, we have successfully realized the electrical spin injection in Ge nanowires and meanwhile demonstrated the electrical detection of spin-polarized surface states conduction in topological insulator. The study of the spin transport in these novel materials was motivated by their promising applications to build novel spintronic devices that could potentially outperform Si devices with lower power dissipation and faster switching.

In the realization of electrical spin injection into Ge nanowires through a Schottky barrier, we have established a convenient approach to make high-quality nanoscale contacts to Ge nanowires through RTA. Single-crystalline germanide contacts, including Ni_2Ge, NiGe, Ni_3Ge, and Mn_5Ge_3, with atomically clean interfaces were fabricated for building high-performance Ge nanowire transistors. More importantly, the fabricated single-crystalline Mn_5Ge_3 contact with room-temperature ferromagnetism and high-quality interface enabled the electrical spin injection and detection in the $Mn_5Ge_3/Ge/Mn_5Ge_3$ nanowire transistor. A spin diffusion length of about $l_{sf} = 480$ nm and a spin lifetime of exceeding 244 ps was revealed in *p*-type Ge nanowires at $T = 10$ K, which were much larger than those reported for bulk *p*-type Ge.

Meanwhile, high-quality epitaxial Fe/MgO junctions were grown by MBE on the Ge nanowire for tunneling spin injection and detection. The electrical spin injection into *n*-type Ge nanowires with Fe/MgO tunneling contacts was performed in nonlocal spin valve measurements. The obtained spin lifetime and diffusion length in *n*-type Ge nanowires at $T = 40$ K were $l_{sf} = 2.57$ μm and $\tau_{sf} = 7.2$ ns, respectively, which were again much larger than those reported in bulk *n*-type Ge. The significant enhancement in the spin lifetime and diffusion length in nanowires suggested that the spin relaxation was suppressed in nanowires compared with bulk materials. It also implied the striking advantage of using low-dimensional nanostructures for building practical spintronic devices.

The successful realization of electrical spin injection in Ge nanowires paved the road to build novel Ge-based spintronic devices. In particular, a novel DMS nanowire-based nonvolatile transpinor has been proposed as a possible realization of all-spin logic devices with built-in memory for low-power applications. To build the transpinor, single-crystalline Mn_xGe_{1-x} DMS nanowires have been successfully grown by MBE using the pattern-assisted technique. The ferromagnetic Mn_xGe_{1-x}nanowires showed a Curie temperature above 400 K without any precipitate. The electric field control of ferromagnetism up to 300 K will be demonstrated in the Mn_xGe_{1-x} DMS nanowire, and it will serve as the foundation to fabricate the prototype of the transpinor by integrating the previous spin injection structures.

Furthermore, we studied the spin transport in the recently discovered TI, in which the spin-momentum locking of helical surface states is preserved by the strong spin-orbit interaction and time-reversal symmetry. The compound TI $(Bi_{0.53}Sb_{0.47})_2Te_3$ was studied for the merit of low bulk carrier density (n_{2D} ~10^{12} cm^{-2}) and clean spin texture. The electrical detection of the spin-polarized surface states conduction in $(Bi_{0.53}Sb_{0.47})_2Te_3$ was demonstrated using a Co/Al_2O_3 ferromagnetic tunneling contact. Voltage (resistance) hysteresis was observed when sweeping the magnetic field to change the relative orientation between the Co electrode magnetization and the spin polarization of surface states. The two resistance states were reversible by changing the electric current direction, affirming the spin-momentum locking in the topological surface states conduction. The spin voltage amplitude was quantitatively analyzed to estimate an effective spin polarization of 1.02% for the surface states conduction in $(Bi_{0.53}Sb_{0.47})_2Te_3$. Our findings demonstrated the exotic feature of current-induced spin polarization in topological surface states conduction from electrical transport measurements. With the understanding of spin injection and detection, it might open up great opportunities to explore novel spintronic devices based on topological insulators with dissipationless transport.

5.2 Outlook

In this work, we have demonstrated the significant enhancement in the spin lifetime and spin diffusion length in nanowires compared with bulk materials. In the very near future, we would expect more and more research efforts to be devoted in the realization of spin injection into various semiconductor nanowires as well as other nanostructures like nanoribbons. It would also attract great attention to study the spin relaxation mechanism in nanowire from both theoretical and experimental perspectives. By playing different parameters in nanowire spin injection devices, it would be interesting and also necessary to investigate the diameter effect (size-induced quantum confinements), the doping effect (impurity-induced spin relaxation), the surface effect (interface states) and the gate effect (electric field control) on the underlying spin transport. It is also noted that many core-shell nanowires with a one-dimensional hole/electron gas, such as Ge-Si and GaAs-AlGaAs core-shell nanowire,[247-249] provide another freedom to tune the nanowire structure and hence the spin transport properties for building practical spintronic devices.

In the past two decades, researches on semiconductor spintronics so far have been mainly focused on studies of the charge-spin transport and spin dynamics. Through extensive spin transport measurements, the observed spin diffusion length in many materials (typically hundreds of nanometers to several micrometers) is already much larger than the channel length of state-of-the-art MOS transistors.[1] The advanced microelectronics technology has provided us many sophisticated and reliable fabrication techniques. Therefore, the future of spintronics should involve more efforts in building practical spintronic devices for room-temperature operations that can provide nonvolatility, low energy dissipation, high switching speed, and many other advantages over conventional CMOS devices. Low-dimensional nanostructures, especially Ge/Si nanowires, could be a promising material candidate because of their long spin lifetime and diffusion length as well as their easy integration with standard CMOS technology. Besides, novel device concepts and materials are also required to realize spin-based information processing while minimizing charge current flow. The DMS nanowire-based nonvolatile transpinor is a promising approach of great interest, which involves electrical spin injection and electric-field controlled magnetic phase transition in nanostructures. The recent development of high-Curie temperature DMS materials and more recently TIs (with spin-polarized Dirac surface states) could provide great opportunities in building future energy-efficient spintronic devices.[193,197]

Chapter 6

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