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Liquid Phase Epitaxy Doping for High-Performance Emitters in Silicon Solar Cells

A Thesis submitted in partial satisfaction of the requirements

for the degree Master of Science

in

Chemical Engineering

by

Tulika Rastogi

Committee in charge:

Professor David. P. Fenning, Chair
Professor Ping Liu
Professor Kesong Yang

2018

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The Thesis of Tulika Rastogi is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

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University of California San Diego

2018

DEDICATION

Moving to a new country and adapting to their culture is never easy. Building a new existence away from everything you know and believe in, is a powerful feeling but in turn is also an alienated, lonely experience you share with yourself.

I want to dedicate this thesis to my family and friends who supported me at every step of this journey. You gave me the strength to step out of my comfort zone and aided me to stretch my boundaries.

EPIGRAPH

It does not matter how slowly you go so long as you do not stop.

- Confucius

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LIST OF ABBREVIATIONS

LPE-D	Liquid Phase Epitaxy Doping
Sq	square
PV	Photovoltaic
c-Si	Crystalline Silicon
TW	Tera-Watt
Si	Silicon
SiN_x	Silicon Nitride
Cz-Si	Czochralski Silicon
NaOH	Sodium Hydroxide
NaOCl	Sodium Hypochlorite
IPA	Isopropyl alcohol
$POCl_3$	Phosphorus oxychloride i
N_2	Nitrogen gas
H_2	Hydrogen gas
O_2	Oxygen gas
PSG	Phosphosilicate glass
HF	Hydrofluoric acid
P_2O_5	Phosphorus pentoxide
Cl_2	Chlorine gas
P	Phosphorus
SiO_2	Silicon Dioxide
ITRPV	International Technology Roadmap for Photovoltaic
Al	Aluminum
Sn	Tin

Zn	Zinc
B	Boron
Ga	Gallium
HCl	Hydrochloric acid
S	Seconds
BBr_3	Boron tribromide
fA	Femto- ampere
FF	Fill Factor
S_n	Surface recombination velocity
Al_2O_3	Aluminum oxide
DSC	Differential scanning calorimetry
SEM	Scanning electron microscope
EDX	Energy dispersive x-rays
ALD	Atomic layer deposition
UV-Vis	Ultra- violet -visible
DI	Deionized
Ti	Titanium
atm	Atmosphere
TMAH	Tetramethylammonium hydroxide
H_4SiO_4	Silicon hydroxide
H_2SiO_3	Silicic acid
Na_2SiO_3	Sodium silicate
$Si(OH)_4$	Silicon hydroxide
H_2O_2	Hydrogen peroxide
TMA	Trimethylaluminum
SE	Secondary electron

LIST OF SYMBOLS

Symbol	Description
J_{0e}	Emitter saturation current
R_{sh}	Sheet resistance
Ω	Ohm
<	Greater than
°C	Degree Celsius
%	Percentage
V_{oc}	Open Circuit Voltage
g_M	Solvent load
$W_{emitter}$	Width of the emitter
$wt\%_{Si}{}^{Tp}$	Percentage weight of silicon at peak temperature
$wt\%_{Si}{}^{Teu}$	Percentage weight of silicon at eutectic temperature
ρ_{Si}	Density of silicon
T_p	Peak temperature
T_{eu}	Eutectic temperature
∆T	Change in temperature
X_{si}	Composition of silicon
µm	Micrometer
Wt%	Weight percent
min	Minute
µL	Microlitre
vol%	Volume percent
nm	nanometer
Å	Angstrom
Conc.	Concentrated
cm^2	Centimeter x centimeter

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First and foremost, I want to thank Dr. **David Fenning** for giving me a chance to be a part of his group. Being new to the nanoengineering background, he was patient with me, guided me without pushing, and always motivated me without distressing. I feel very fortunate to have had you as an advisor; you taught me more than I ever anticipated.

Chapter 3, in part is currently being prepared for submission for publication of the material. Rastogi, Tulika; Magana, Ernesto; Gastrow, Guillaume Von; Fenning, David. P. The dissertation/thesis author was the primary investigator and author of this material.

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ABSTRACT OF THE THESIS

Liquid Phase Epitaxy Doping for High-Performance Emitters in Silicon Solar Cells

by

Tulika Rastogi

Master of Science in Chemical Engineering

University of California San Diego, 2018

Professor David. P. Fenning, Chair

Emitters formed by gas diffusion in the solar industry are a major contributor to the cost of manufacturing of the solar cell. The emitter alone contributes 27% to the capex cost of the cell manufacturing [1] resulting in heavily-doped, difficult-to-passivate front surface. Being kinetically driven, it requires high thermal budget thus increasing equipment cost, and have a low-throughput batch nature to the process.

Liquid phase epitaxy doping (LPE-D) provides an alternative to the kinetically-governed gas diffusion processes of emitter formation common in the solar industry. It is a lower-temperature technique that relies on doping during recrystallization from a liquid eutectic surface layer. It results in a more uniform doping concentration profile with the potential for significantly lower saturation currents and improved surface passivation. Being thermodynamically-governed, a wide range of solvent –dopant systems can be used to

achieve low sheet resistance (<$120\Omega/\mathrm{sq}$) emitters. We examine the performance of emitters doped via liquid phase epitaxy using simulation and present experimental demonstration using aluminum – boron as the metal solvent- dopant.

CHAPTER 1: INTRODUCTION

With the accelerated global growth and development, our non-renewable energy resources are being depleted at an alarming rate. Fossil fuels, like oil and coal are known to be nearing their production peaks with nuclear fuels following the lead. To avoid the fast approaching global crisis of carbon based energy resources, it is imperative to find alternatives forms of energy. Renewable forms of energy such as solar, wind, and hydropower energy can fulfill the need, while being inexhaustible on one hand, and cleaner and safer for the environment on the other. Of all the renewable forms of energy, solar energy has been a major contributor and has seen a steady growth over the last few decades. Figure 1 shows how Solar PV has been a major contributor to renewable energy over the last 15 years.

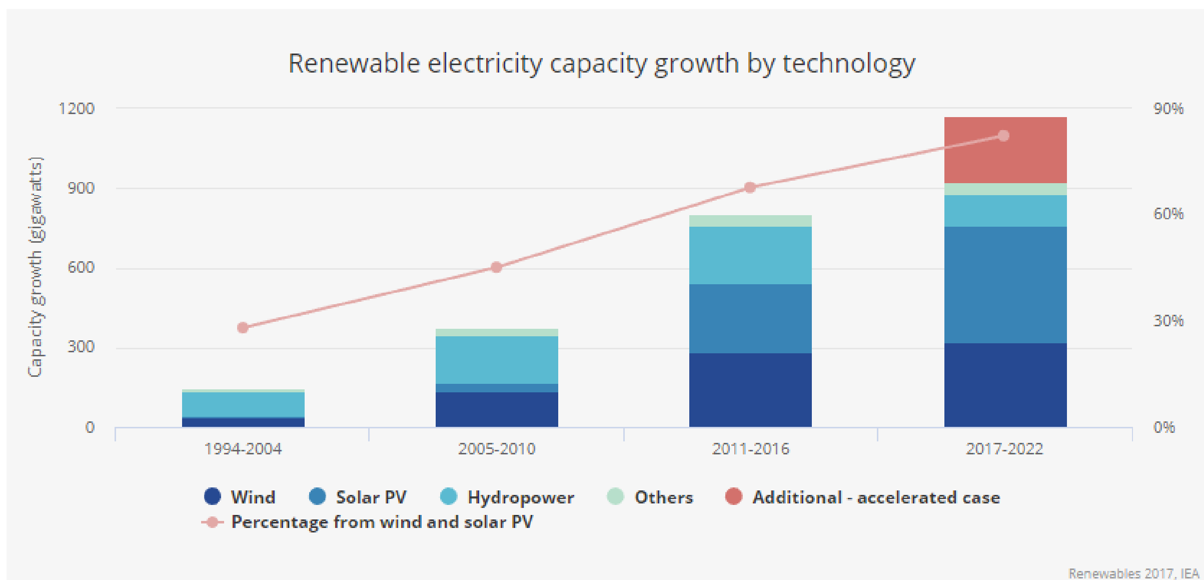


Figure 1: Renewable energy growth map [2]

With aid from government subsidies and large amount of research and development, the PV industry is predicted to account for 40% of the renewable energy market by 2022 [2]. Hence this project aims at addressing solar energy obtained from solar/photovoltaic cells.

WHY SILICON SOLAR CELLS?

The solar industry, also known as the photovoltaic (PV) industry, came into existence in 1970's and was largely based of crystalline silicon (c-Si) solar cells. Since then different types of solar cells and a variety of new materials have been investigated. The c-Si solar cells are the widely adopted mainly because of its cheap and abundant raw material, silicon, and because an enormous semiconductor industry is established around it. They have shown a record efficiency between 22-26% for the last two decades. Figure 2 shows how the efficiencies of c-Si solar cells have increased to 26.6% as of 2018.

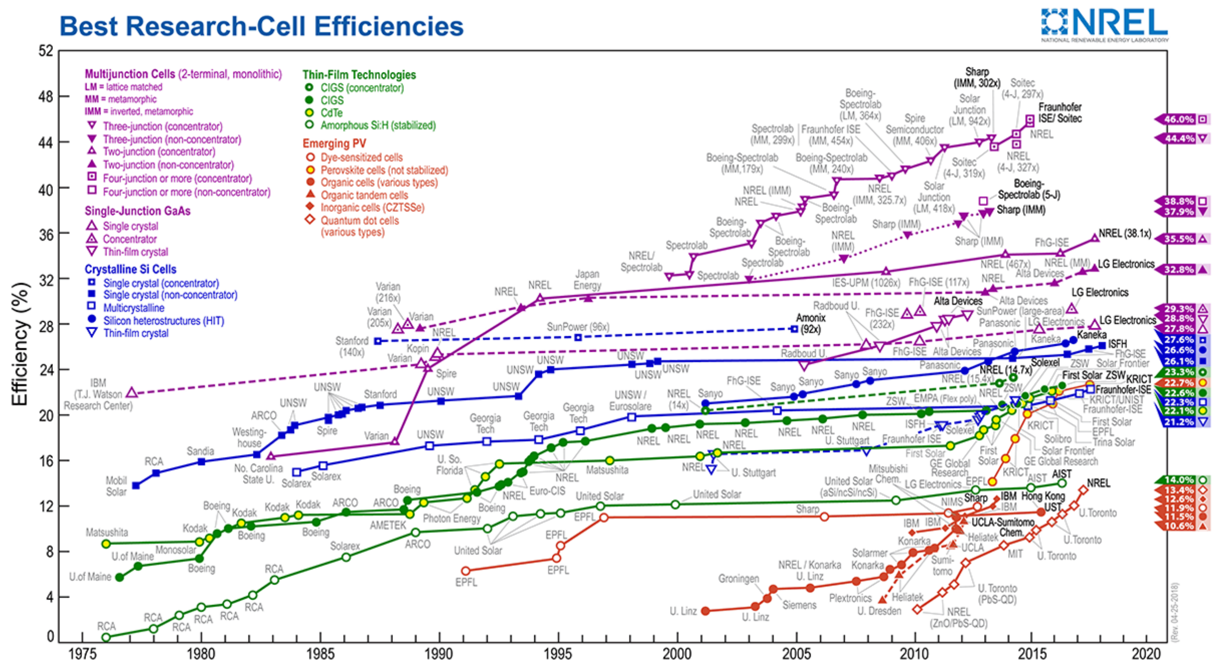


Figure 2: Evolution of solar cell efficiencies from 1976-2018 [3].

The amount of solar energy incident on the earth surface every second (1650 TW) is much higher than the combined average power consumption of the entire world (< 20 TW) in 2005 [4]. Even with the present efficiencies of 26.7% we can cater to the energy needs of the entire world, if we are able to produce cheap solar cells on a large scale. Hence to be able to reduce the price of the c-Si solar cell changes need to be made to the device architecture or the method of fabrication. Figure 3 shows the entire procedure of manufacturing of silicon

solar cell from growth of silicon to the assembling of the cell into a module. It highlights the capex cost involved at each step giving a broad idea of the major cost determining steps during processing [1]. Hence this project will aim at finding alternative manufacturing approaches to reducing the price of silicon solar cells.

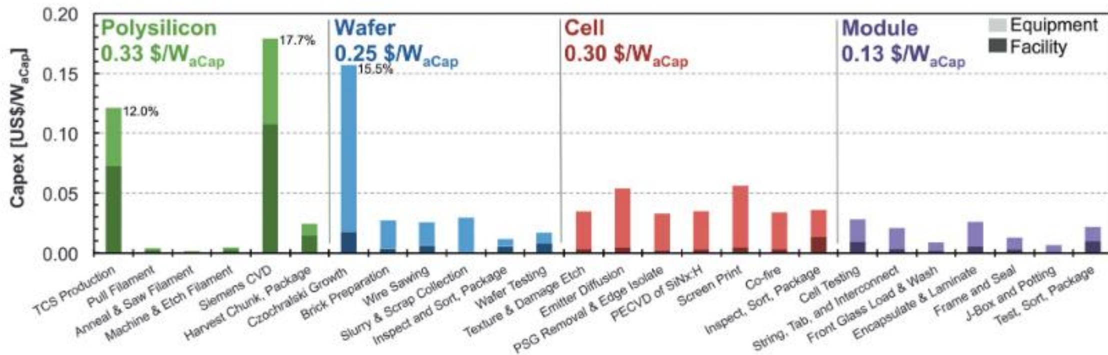


Figure 3: The initial capex cost involved at every step of manufacturing of silicon solar cell [1].

STRUCTURE OF SOLAR CELLS

A c-Si solar cell can be divided into 4 major regions:

- *Base*: It is a semiconducting material usually silicon, which is *p*-type in the majority of of c-Si cells. It is usually 100s of microns thick and is the region where the electron-hole pairs are formed when an excited photon is absorbed by the cell.
- *Emitter*: It is n type in a *p*-type base c-Si cell. Along with the base it forms the p-n junction which creates an electric field for the electron-hole pair to separate. It is usually several nanometers thick.
- *Antireflection coating*: It is a thin layer of silicon nitride (SiN_x) on top of a solar cell which facilitates trapping of light. It is usually 70nm thick.
- *Metal contacts*: These are the contacts on the front and rear side which complete the circuit and allow for electrons to flow and hence produce current. They are few microns thick and are patterned on silicon wafer with the help of screen printing.

Figure 4 shows these regions on a solar cell. When a photon of light strikes the surface of the solar cell it either transmits through it, is reflected, or is absorbed by the silicon solar cell. If the energy of the photon is greater than the band-gap value of Si, the photon would be absorbed according to the absorption coefficient. It can excite an electron to move from its valence band to its conduction band, where it is now a free carrier that can diffuse throughput across the semiconductor. This in turn leaves a hole and is filled by electrons from the

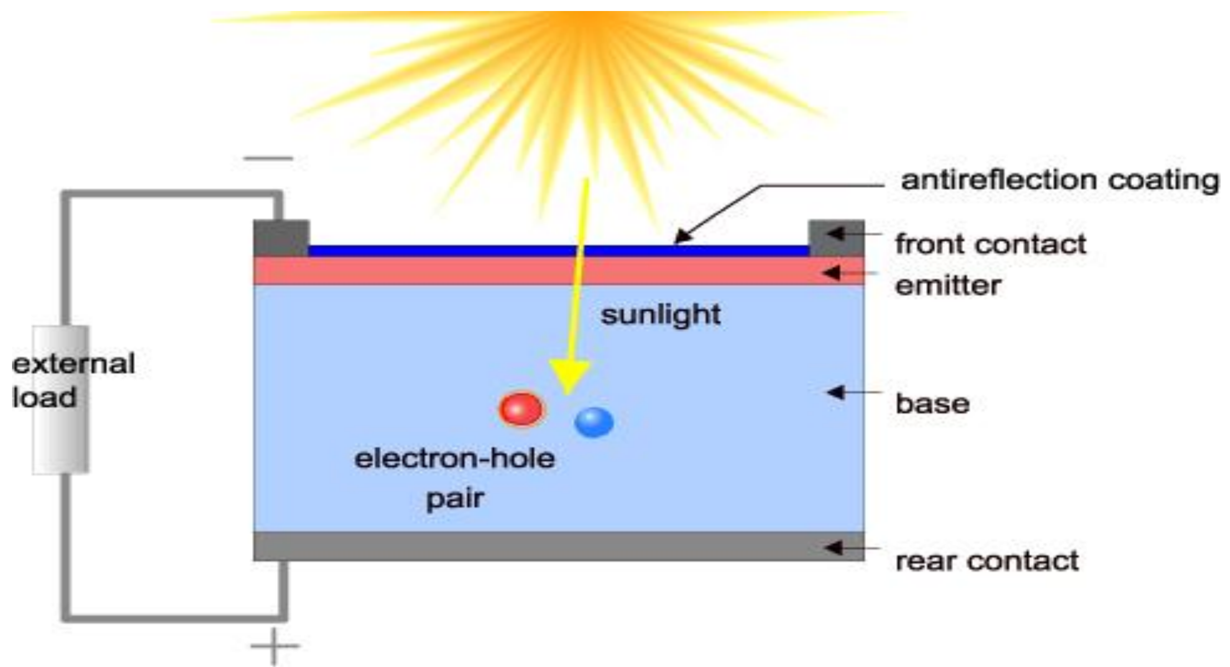


Figure 4: Schematic diagram of a Solar cell [5]

neighboring sites, giving rise to the term electron-hole pair. As much of the solar radiation reaching the Earth's surface has photons with energies higher than the band gap of silicon, this excess energy is converted into heat energy (via lattice vibrations called phonons). At the depletion region of the p-n junction, an electric field is formed which causes the minority carriers to be separated across the junction. These charges then flow through the metal contacts and complete the circuit thus generating current.

.

EMITTER FORMATION IN THE INDUSTRY

In the solar industry, approximately 90% of emitter formation is done by thermal diffusion of the dopants into the Si lattice. Figure 5 shows the contribution of different emitter formation technologies and their predicted trend for the next decade. In this section we would compare the short version of $POCl_3$ diffusion process in monocrystalline wafers [4]. The fabrication of a *p*-type silicon cell starts with a wafer ~160 µm thick of *p*-type c-Si or (100)-oriented Czochralski Si (Cz-Si).

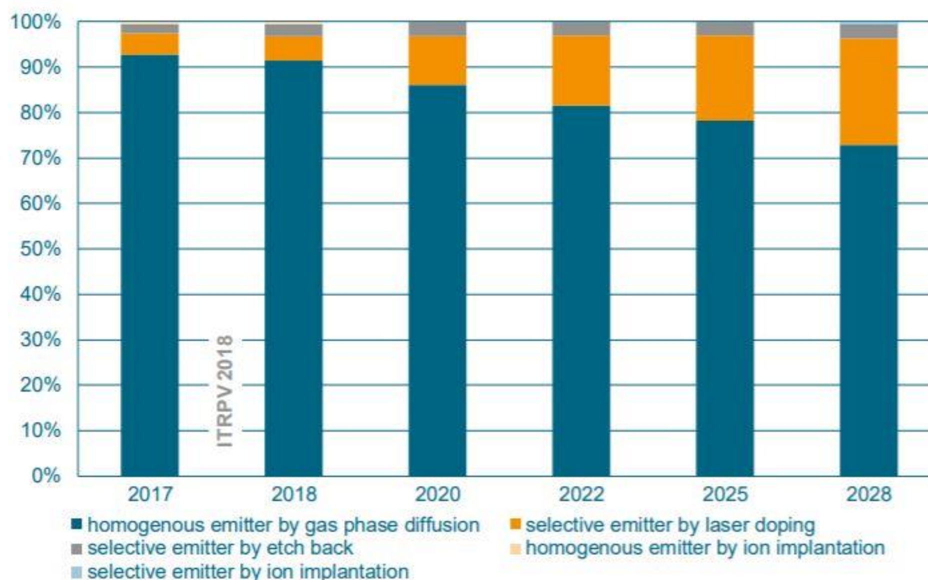
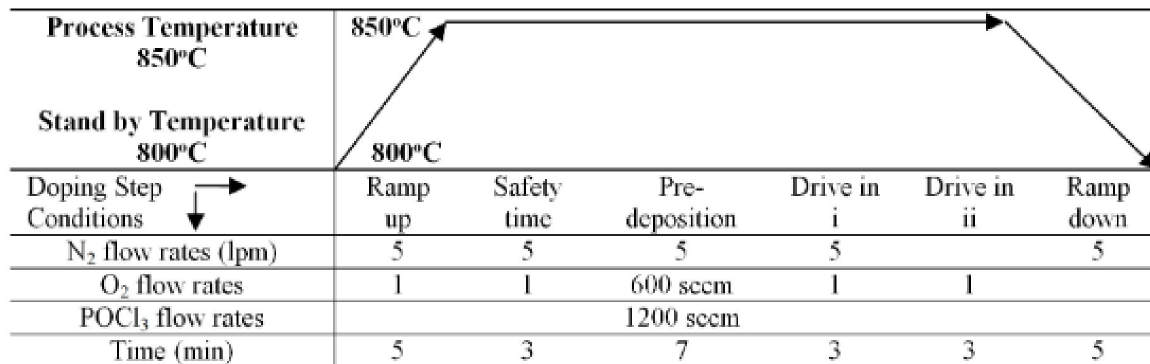


Figure 5: Different processes for emitter formation used in the industry [6].

The wafer is then cleaned with 12% NaOCl solution and the surface damage is removed by dipping it in an 8% NaOH solution. It is then subjected to surface texturing by chemical etching with NaOH and IPA. [4] A *n*-type layer is then added on the *p*- type c-Si wafer by phosphorous diffusion at high temperatures and in a gaseous environment. After emitter formation edge isolation is carried out, followed by passivation of the front and back surface by depositing a dielectric layer. In the end metal contacts are added to the wafer to serve as

electrodes to be connected to the load. Here we would talk in detail about the emitter formation step in the industry. Figure 6 shows the formation process in a schematic diagram.



Doping Step → / Conditions ↓	Ramp up	Safety time	Pre-deposition	Drive in i	Drive in ii	Ramp down
N_2 flow rates (lpm)	5	5	5	5		5
O_2 flow rates	1	1	600 sccm	1	1	
$POCl_3$ flow rates			1200 sccm			
Time (min)	5	3	7	3	3	5

Figure 6: Process used in the industry to create emitters in solar cells [4]

This step is a kinetically-limited step where the phosphorous diffuses into the *p*-type silicon wafer to form an *n*-type region. It depends upon the temperature and the gaseous environment around it and is carried out in a tube furnace. At higher temperatures and oxidizing environments fast diffusion rates can be achieved. The diffusion is carried out in two steps: pre-deposition step and the drive-in step. In the pre-deposition step liquid Phosphorus oxychloride ($POCl_3$) is picked up into a N_2 gas stream by bubbling nitrogen gas (N_2) through it and deposits via chemical vapor deposition onto the Si wafers within the heated tube furnace. This deposited $POCl_3$ in presence of oxygen (O_2) at 850°C converts to phosphosilicate glass (PSG). PSG formation rate is about 15nm in 30 minutes. [4] In the next drive in step the wafer is heated at 850°C in presence of oxygen which facilitates deeper diffusion of phosphorus in the silicon, hence enabling deeper emitter junction. PSG is later removed by etching in hydrofluoric acid(HF). The steps can be summarized in the reaction equations below [4]

$$POCl_3(\text{liquid}) + N_2(\text{bubble}) \rightarrow POCl_3(\text{vapor}) \quad (\text{pre-deposition}) \qquad (1)$$

$$4POCl_3 + 3O_2 \rightarrow 2P_2O_5 + 6Cl_2 \qquad (2)$$

$$2P_2O_5 + 5Si \rightarrow 4P + 5SiO_2 \quad (\text{drive-in}) \qquad (3)$$

$$P + 3Si \rightarrow \text{n-type doped Si} \qquad (4)$$

As this process of gas diffusion is kinetically-driven the concentration profile of the dopant slowly increases as the temperature increases resulting in high surface dopant concentration. The concentration of the dopant decreases as it diffuses further into the silicon wafer. Figure 7 shows the emitter junction profile of phosphorous doped p type silicon [7]. The emitter formed by thermal diffusion process has a high surface concentration of dopant which gradually decreasing, suggesting a kink and a tail profile.

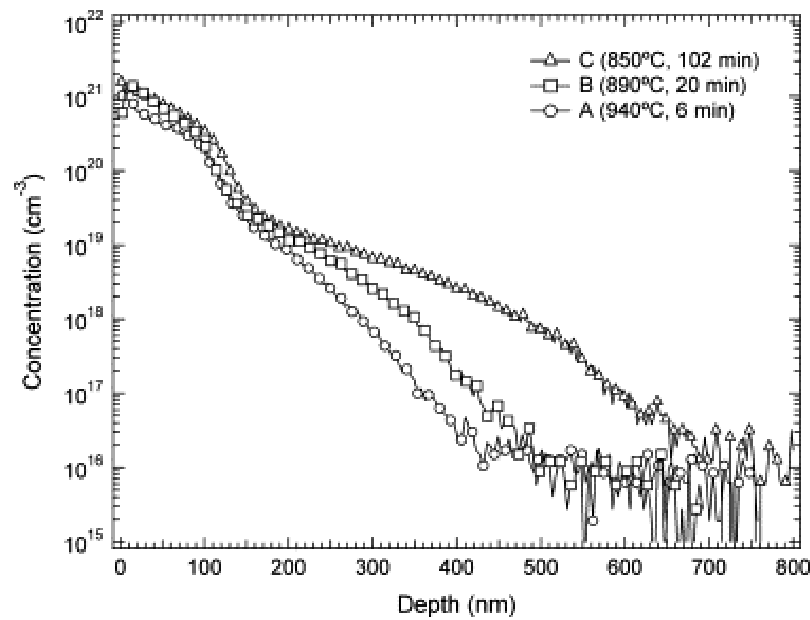


Figure 7: Change in phosphorous doping profile with distance from the emitter surface into the silicon wafer [7].

Examining the capex cost of manufacturing of silicon solar cells shown in figure 3 we can see that the gas diffusion process of emitter formation alone accounts for 17% of the capex cost of cell manufacturing to the company.

MOTIVATION

As explained in the previous section, emitters in the solar industry are formed by high temperature solid state diffusion process using $POCl_3$ gas. It requires high diffusion temperature. (800-850 °C) which needs to be maintained for a continuous production line to run. As it is a kinetically- limited process, it requires high temperatures and gas pressures for maximum output. This results in increased manufacturing costs. The emitter formation process alone account for 27% of the capex cost of cell manufacturing (fig 3). Being a batch process, it limits the in-line automation of the manufacturing process which is soon going to be necessary for large scale production of solar cells. It also involves the use of toxic gases like $POCl_3$, Cl_2 which can be harmful for the workers. Other than the cost and processing challenges, the inflexible constraints of solid-state diffusion kinetics result in a heavily-doped, difficult-to-passivate front surface and shallow emitters.

Here, we propose Liquid phase epitaxy doping (LPE-D) to create better performing emitters in a cost-efficient manner. Liquid phase epitaxy doping (LPE-D) proposes a new method to form emitters. It is a thermodynamically governed process which involves the use of a metal solvent that undergo eutectic melting with silicon at low temperatures. This metal solvent dissolves with silicon to create a melt in which the dopant diffuses in the liquid phase and eventually solidifies upon recrystallization. LPE-D is carried out at lower temperatures depending upon the eutectic temperature of the metal solvent-Si system.

Via simulation, we show that LPE-D process has the potential to reduce the emitter saturation current, leading to improved solar cell efficiency, by enabling precise, tunable control over the emitter concentration profile. Thus, solar cells produced with LPE-D emitters may exhibit significantly less recombination in the emitter than typical gas-diffused emitters. Figure 8 shows the ITRPV predicted trend for emitter saturation current which is predicted to fall down to 40fA/cm2 by 2028 [6].

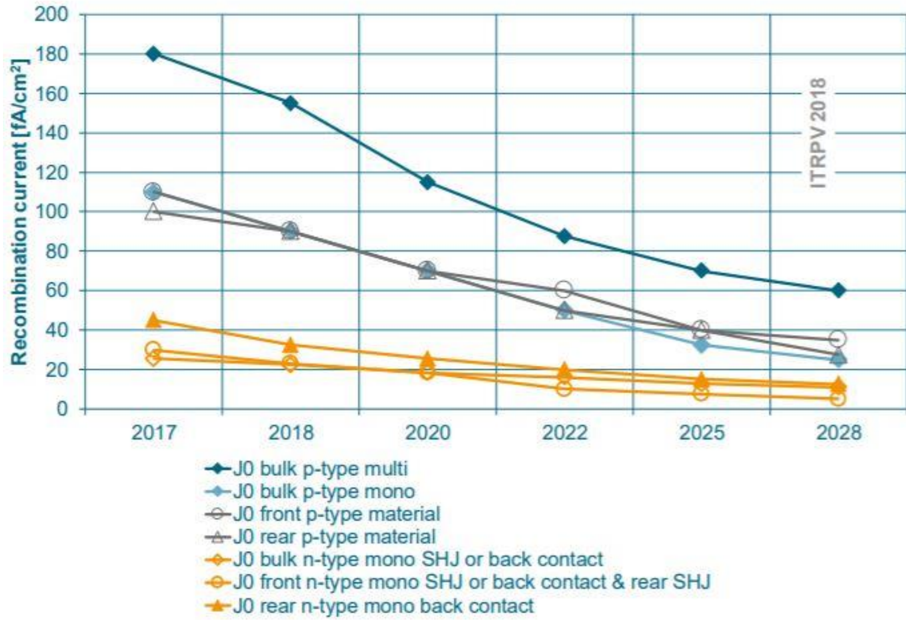


Figure 8: Prediction for emitter saturation current trend for Si solar cells [6].

The depth of the doped emitter can also be fine-tuned simply by controlling the thickness of the initial metal solvent load, as can the peak dopant concentration by controlling the peak process temperature. Thus, LPE-D emitters allow for substantial tunability, as the dopant depth and peak dopant concentration can be controlled independently.

The LPE-D process would also dramatically increase manufacturability and drive down the levelized cost of solar energy by potentially cutting the process temperature in half and the process time by a factor of 100. LPE-D profiles are nearly uniform with depth and exhibit an abrupt junction, which serves to achieve a higher V_{OC}, as opposed to a characteristic diffused profile which results in a high dopant concentration at the surface.

Table 1 summarizes the present method of emitter formation in the solar industry and the modified method proposed. The LPE-D method would require the use of screen printing and annealing at low temperatures. Hence, no additional capital equipment cost would be added to the present manufacturing process as screen printing is presently used for creating back surface fields on the rear side of the silicon solar cell. Also annealing at low temperature would reduce the heat load and hence the thermal budget involved.

Table 1: End to end process of making a solar cell

Present method in the industry	**Modified method proposed**
Wafer Cleaning and Saw Damage Removal	Wafer Cleaning and Saw Damage Removal
Surface Texturing	Surface Texturing
Phosphorus diffusion for p-n junction formation	LPE doping for p-n junction formation
Edge Isolation with wet chemical etching	Edge Isolation with wet chemical etching
Anti-Reflection coating and Front Surface Passivation	Anti-Reflection coating and Front Surface Passivation
Metallization	Metallization

CHAPTER 2: EMITTER FORMATION BY LIQUID PHASE EPITAXY DOPING

The main difference between liquid phase epitaxy- doping and conventional gas diffusion for emitter formation ensues from the way dopants are transported into the silicon lattice. LPE-D is thermodynamically governed, thus the choice of metal solvent and its thermodynamic properties with silicon play a major role in achievable emitter depths and dopant concentrations.

LPE-D uses eutectic melting of the metal solvent layer and Si, thus a metal solvent-dopant layer of 100s of microns thick is deposited onto the silicon surface. Al, Sn, or Zn can serve as good metal solvents as they have low eutectic temperatures with Si and B or Ga can be used as dopants for *p*-type emitters. A brief overview of the LPE process is given in the next paragraph, while a detailed explanation is provided in the next section.

The metal-dopant assembly melts upon heating at the eutectic temperature of the metal solvent and Si. They melt in their eutectic composition and as the temperature increase to the peak temperature more and more near surface Si gets incorporated into the metal-Si melt (Fig. 9a) following the liquidus curve of the phase diagram in equilibrium (Fig. 10). Upon cooling from the peak temperature, the metal-Si eutectic melt becomes supersaturated with Si which starts to recrystallize epitaxially onto the surface of the wafer. During recrystallization the dopant saturates the liquid melt depending upon its solid solubility in Si at that recrystallization temperature [8] and thus is incorporated into the Si lattice being formed. Upon further cooling below the eutectic temperature, the entire metal-Si melt solidifies at the eutectic composition (Fig. 9b) leaving a layer of solvent-Si alloy on the Si surface. This layer can be removed by etching with acids like HCl and HF, where Si surface can serve as the etch stop as both acid do not etch Si. (Fig. 9c).

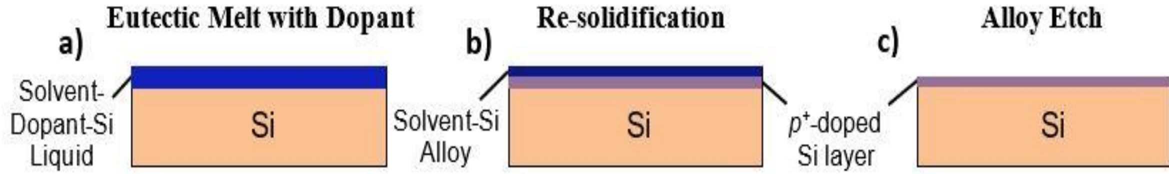


Figure 9: Schematic of liquid phase epitaxy doping process.

Previously, Liquid phase epitaxy has been studies for the formation of back surface fields using Al-Si binary eutectic melting and low temperature crystallization [9]. Recent work has proved the significance of boron-doping in aluminum paste used for back surface [10] to enhance the field effect passivation. Here, we investigate the use of liquid-phase epitaxy doping to tailor emitter profiles broadly for *n* and *p* types emitters, designed by selection of one or more dopant elements for a given eutectic temperature.

We can use Eq. (5) to calculate the width of the doped layer for a given solvent loading, g_M. [11] The depth of the emitter, $W_{emitter}$, is determined entirely by the binary phase diagram: via the mass percentage of silicon incorporated into the melt at the peak temperature, $wt\%_{Si}{}^{Tp}$, and in the eutectic after re-solidification, $wt\%_{Si}{}^{Teu}$.

$$W_{emitter} = \frac{g_M}{\rho_{Si}}\left(\frac{wt\%_{Si}^{T_p}}{100 - wt\%_{Si}^{T_p}} - \frac{wt\%_{Si}^{T_{eu}}}{100 - wt\%_{Si}^{T_{eu}}}\right) \quad (5)$$

The resulting LPE-D profiles are thermodynamically deterministic, rather than kinetically-controlled.

In Eq. (5), the difference between the silicon fraction at T_{peak} (containing the dopant) and the silicon fraction at T_{eu} (where the dopant starts to dissolve in silicon) represent the fraction of silicon that recrystallizes with the dopant to form the emitter. Hence the width of the emitter is effected by the metal solvent load and the composition of the melt at the peak and eutectic temperature. The concentration of the dopant depends upon its solid solubility in liquid Si melt as it cools and recrystallizes from T_{peak} to $T_{eu.}$

LIQUID PHASE EPITAXY: CONCEPTS

Here we discuss the liquid phase epitaxy process in detail to have a better understanding of eutectic melting and saturation of melt with Si upon cooling. The silicon-metal binary phase diagram is the starting point for the LPE process. Figure 10 shows a binary phase diagram of Si with a metal M. The metal and the silicon melt together at point E, corresponding to the eutectic. The temperature of the eutectic is the lowest temperature at which the liquid solution exists, in other words the lowest temperature for the metal -Si combination, from which Si can be grown.

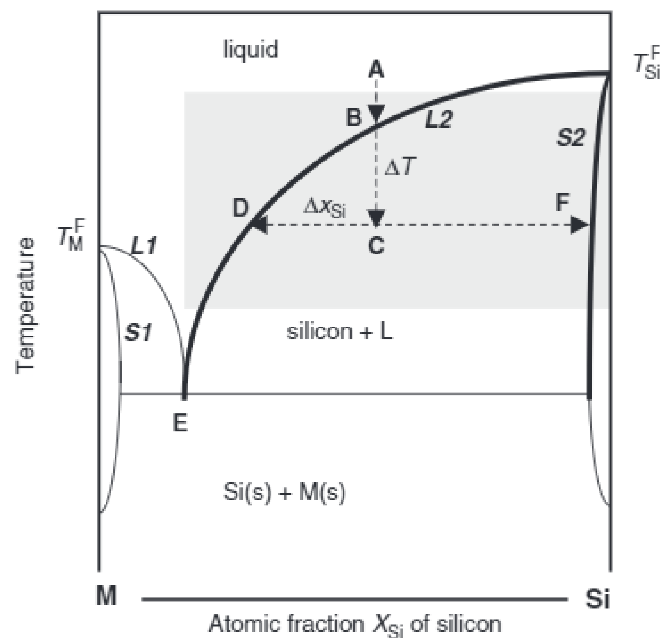


Figure 10: A Silicon-metal binary phase diagram [9].

The region to the right of the eutectic point E is the hypereutectic region, which is bound by the liquidus line L2 and solidus line S2. It is this hypereutectic area which is of interest to us. The liquidus line L2 indicates the solubility of Si in the melt as a function of temperature and its slope determines the growth temperatures, rates and the stability of the LPE process [9]. The solidus line S2 determines the extent of metal incorporation into the melting silicon. Once the melt attains a set temperature ($T_{peak} > T_{eu}$) it starts to cool and Si starts to recrystallize

with the metal and the dopant is incorporated in it depending upon their solid solubility in silicon.

A typical sequence of events for Si recrystallizing upon cooling of the liquid melt can be explained with an example. Starting at an arbitrary point A (Fig 10), upon cooling to point B on the liquidus curve, the liquid solution saturates with silicon. The solution is then supercooled by an amount ΔT to the point C. The system is at a nonequilibrium metastable condition of supersaturation [9] which is relieved by precipitation of a silicon-rich solid phase. The precipitation continues till the concentration of Si in liquid phase reaches point D. Under equilibrium conditions, the Si solid phase will contain metal at a concentration given as point F on the solidus curve S2. This metal component may be dissolved in the silicon matrix as either substitutional or interstitial impurity.

In case of LPE-D, when the Si saturates at point B, the dopant saturates the melt depending upon its solid solubility in Si at that temperature. This is how the recrystallizing Si incorporates the dopant into its lattice.

METAL SOLVENT SYSTEMS USED IN LPE-D METHOD

The LPE-D method supports several combinations of metal solvents and Si. For most of the metal -Si binaries of interest the eutectic point occurs at very small concentration of Si which would require high concentrations of metal to be melted. However, silicon-aluminum binary serves as an exception to this. The eutectic point occurs at $X_{si} = 0.12$ and at 575°C i.e. below the melting point of Al (660°C). Hence, we choose aluminum as our metal solvent to study the LPE-D process. Figure 11 shows the silicon -aluminum binary phase diagram.

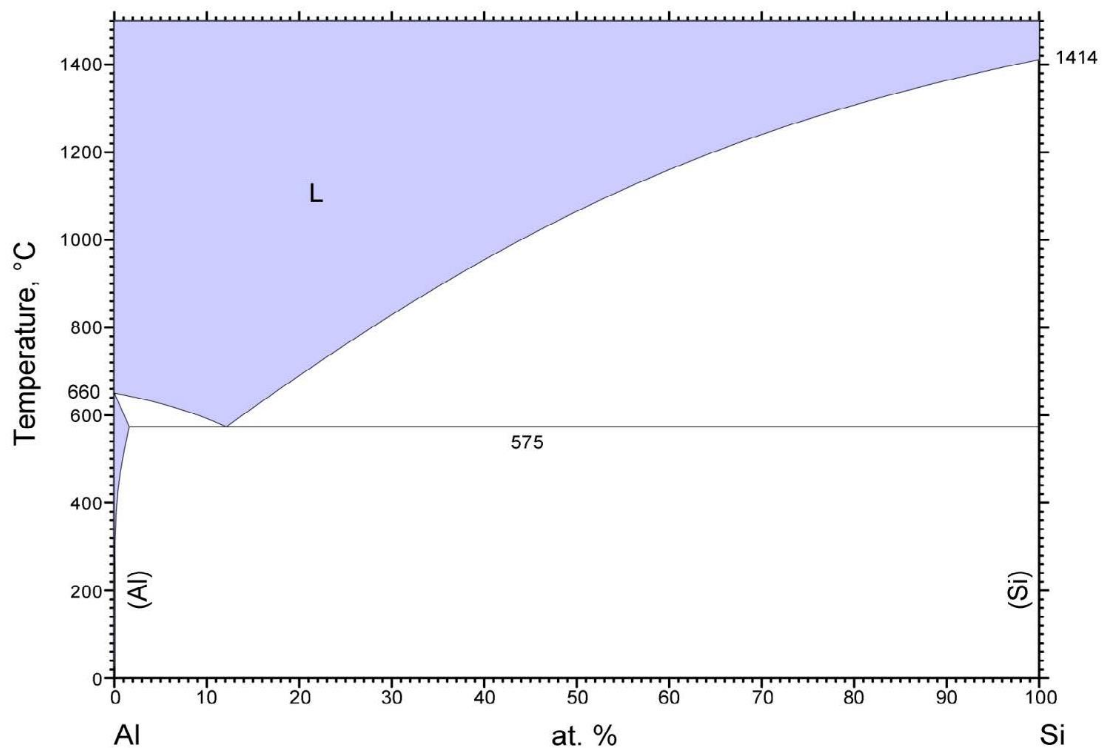


Figure 11: Al-Si binary phase diagram [12]

To form p-type emitters we choose boron and aluminum as our dopants. Thus aluminum - aluminum (Al-Al) and aluminum – boron (Al-B) are our starting chemistries for the proof of concept. In Al-Al chemistry, Al is our metal solvent and Al is also our dopant. In the Al-B chemistry, Al is our metal solvent and B is the dopant.

CHAPTER 3: THEORETICAL SIMULATIONS

The shape of the dopant profile is determined thermodynamically in liquid phase epitaxy doping, rather than kinetically as in solid state diffusion. This is because of the rapid diffusion in the liquid. The liquid melt formed in LPE-D is eventually homogenized with the dopant and the system stays in equilibrium at reasonable cooling rates (e.g. 10s °C/min). By changing the solvent load and the peak temperature we can tune the doping profiles of the emitters.

Emitter saturation current (J_{0e}) was simulated with the help of Cmd-PC1D v6.2 [13] based on the analytical expression reported by Schumacher et al [14] to estimate recombination in heavily-doped regions. The simulation results shown in Fig. 12a represents the minimum achievable J_{0e}. All profiles shown have a contactable sheet resistance below 120 Ω/sq. J_{0e} values for conventional BBr_3- and $POCl_3$-diffused emitters are also shown (top right). These simulations assume no additional trap assited recombination in the emitter compared to the base wafer, and thus provide a minimum estimate of J_{0e}. In-built models in PC1D v6.2 are used to accounts for auger recombination in the emitter. Since the surface doping in the LPE-D emitters considered here did not exceed 10^{19} cm-3, the fundamental surface recombination velocity S_n was supposed constant for all emitters [15].

Simulations courtesy Ernesto Mangana and David Fenning are used to show the emitters profile formed using different metal solvent- dopant combinations. The corresponding emitter doping profiles calculated based on Eq. 5 are shown in Figure 12(b) for *p*-type and Figure 12 (c) for *n*-type emitters. Each simulated process was carried out such that the emitter saturation current densities are minimized while maintaining a sheet resistance < 120 Ω/sq. Each metal solvent selected – Al, Zn, and Sn – has a lower eutectic temperature within the Si binary system (T_{eu} = 577, 420, and 232 °C, respectively), well below typical gas-diffusion temperatures used (850-1000 °C).

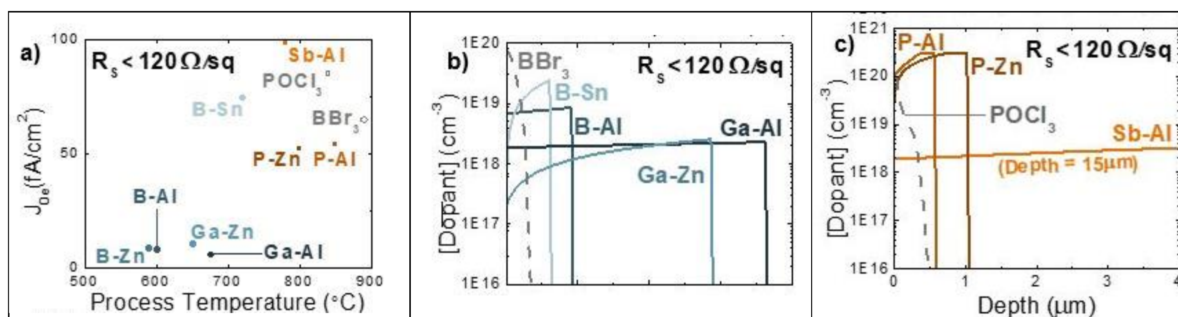


Figure 12:a) The performance potential of LPE-D emitters compared to $POCl_3$ and BBr_3. Modeled J_{0e} for potential dopant-solvent systems as a function of temperature. P-type emitters are shown in blue and n-type emitters in orange; Modeled doping profiles that achieve J_{0e}<100 fA/cm^2 and Rs<120 Ω/sq for b) *p*-type and c) *n*-type emitters in various dopant-solvent systems. Simulations courtesty of Ernesto Magaña and David Fenning.

LPE-D emitters allow for substantial tunability, as the depth and peak dopant concentration can be tuned independently (using solvent load and peak process temperature, respectively). As seen in fig 12b and fig 12c the LPE-D profiles can be rather uniform with depth. These few microns deep emitters offer an abrupt junction, which may lead to a V_{OC} entitlement. Recent studies done on deep abrupt junctions in built-in emitters formed using direct epitaxy [16] have proven to give low sheet resistance emitters, resulting in lower series resistance loss and producing higher FF [17]. Furthermore, the surface dopant concentration is completely determined by the solubility of the dopant at the eutectic temperature. Thus the high-concentration of dopants on the surface of the emitters made by diffusion can be circumvented.

Figure 13 shows the PC1D simulated theoretical results for the Al-Al LPE-D emitters. It shows how the emitter saturation current, sheet resistance, emitter depth and peak dopant concentration change with the change in peak temperature and solvent load used. Depending upon the desirable values for J_{0e}, R_{sh} and emitter depth; peak annealing temperatures and metal solvent loads are chosen.

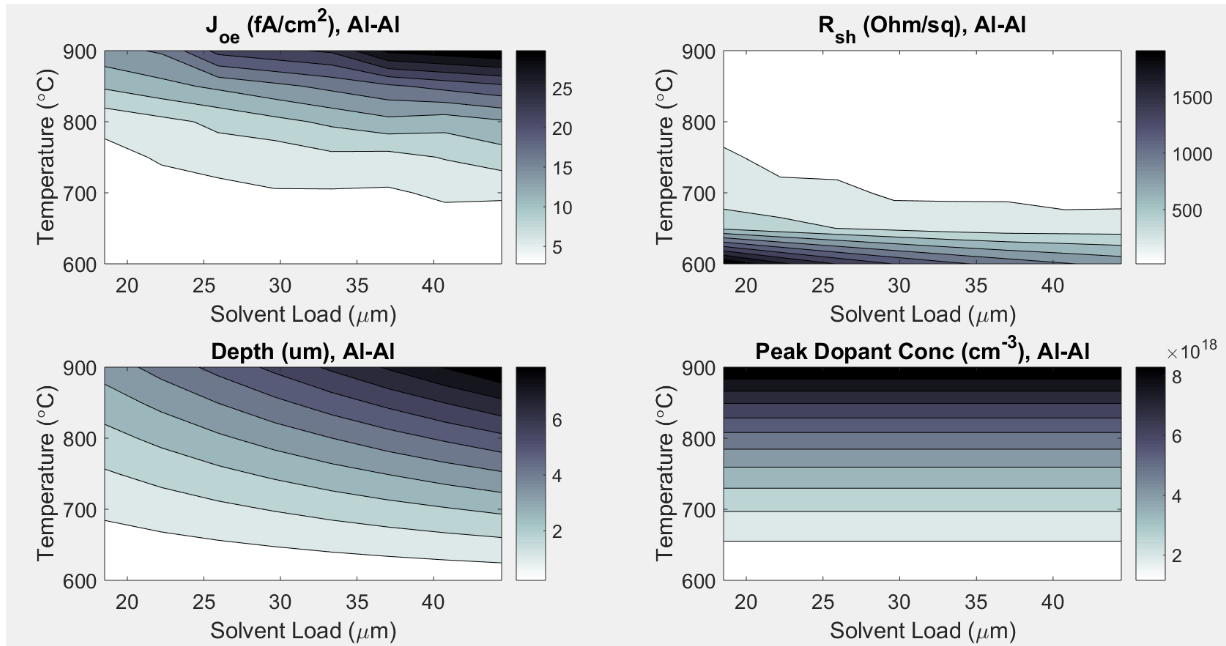


Figure 13: Simulated graphs showing the effect of peak temperature and solvent load on J_{0e}, sheet resistance, emitter depth and peak dopant concentration for Al-Al chemistry. Note that the eutectic of the Al-Si system is reached at 575 °C

For Al-Al LPE-D emitters metal solvent loads of 20µm and 40µm and peak annealing temperature of 650°C, 700°C, 800°C and 900°C were chosen for the proof of concept experiments. Table 2 summarizes the theoretical predictions of different parameters from the PC1D simulations.

Table 2: Simulated/Theoretical parameter values for Al-Al chemistry.

	Metal solvent load: 20µm			Metal solvent load: 40µm		
Temperature	R_{sh}	**Depth**	**Concentration**	R_{sh}	**Depth**	**Concentration**
°C	**Ω/sq**	**µm**	**cm^{-3}**	**Ω/sq**	**µm**	**cm^{-3}**
650	582.8	0.7	1.9E+18	293.1	1.5	1.9E+18
700	261.0	1.2	2.6E+18	132.7	2.5	2.6E+18
800	120.7	2.4	5.2E+18	51.7	4.9	5.2E+18
900	48.6	3.9	9.0E+18	21.8	7.9	9.0E+18

Figure 14 shows the PC1D simulated theoretical results for the Al-B LPE-D emitters. It shows how the J0e, Rsh, emitter depth and PDC change with peak temperature and solvent load.

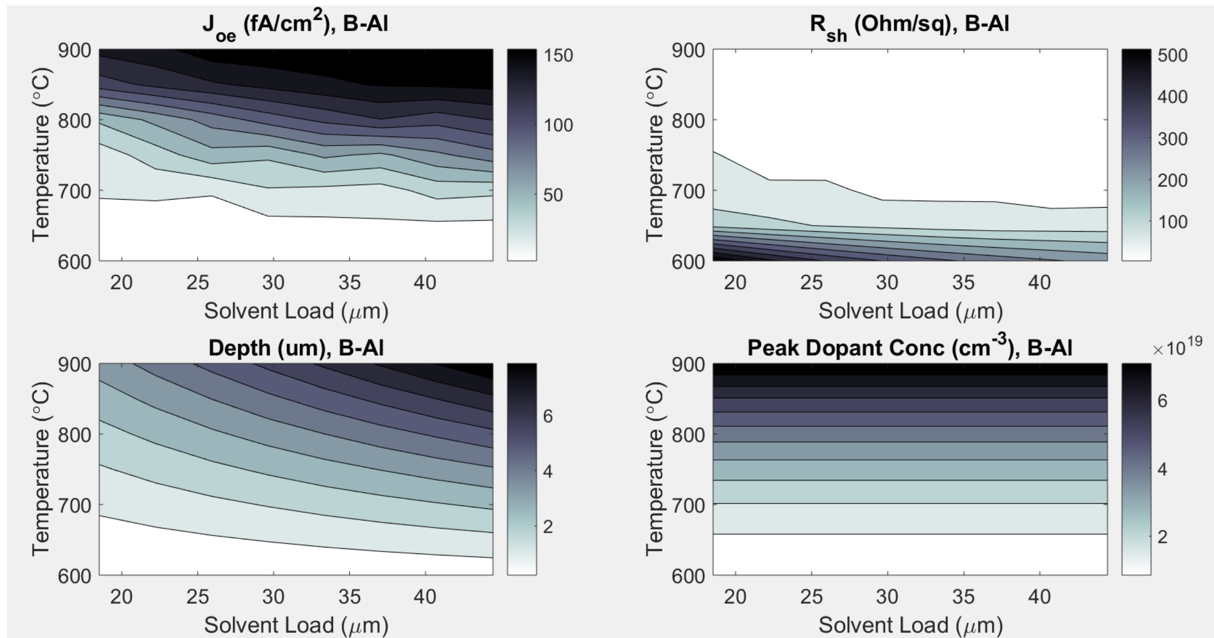


Figure 14: Simulated graphs showing the effect of peak temperature and solvent load on J_{0e}, sheet resistance, emitter depth and peak dopant concentration for Al-B chemistry. Note that the eutectic of the Al-Si system is reached at 575 °C

Metal solvent loads of 20µm and 40µm and peak annealing temperature of 650°C, 700°C, 800°C and 900°C were chosen for the proof of concept experiments. Table 3 summarizes the theoretical predictions of different parameters from the PC1D simulations.

Table 3: Simulated/Theoretical parameter values for Al-B chemistry.

	Metal solvent load: 20µm			Metal solvent load: 40µm		
Temperature	R_{sh}	**Depth**	**Concentration**	R_{sh}	**Depth**	**Concentration**
°C	**Ω/sq**	**µm**	**cm^{-3}**	**Ω/sq**	**µm**	**cm^{-3}**
650	152.9	0.7	1.5E+19	75.92	1.5	1.5E+19
700	65.3	1.2	2.1E+19	32.6	2.5	2.1E+19
800	27.3	2.4	4.2E+19	11.4	4.9	4.2E+19
900	9.3	3.9	7.7E+19	4.3	7.9	7.7E+19

The theoretical simulations are the courtesy of Ernesto Magana, who worked with the guidance from Prof. David. P. Fenning at Nanoengineering Department in UCSD. The idea of modifications to the simulated results to incorporated for trap assisted recombination in emitter is the courtesy of Guillaume Von Gastrow, a Post-Doctoral member of Fenning Research Group.

Chapter 3, in part is currently being prepared for submission for publication of the material. Rastogi, Tulika; Magana, Ernesto; Gastrow, Guillaume Von; Fenning, David. P. The dissertation/thesis author was the primary investigator and author of this material.

CHAPTER 4: EXPERIMENTAL PROOF-OF-CONCEPT

The LPE-D emitters were formed using Al as the metal solvent and both Al and B as the dopant, individually. The method was tested for two solvent loads 20µm and 40µm to show tuning of emitter depth depending upon the solvent load used. Cz- Si wafers of 125µm were coated with the metal solvent-dopant paste and annealed at four different temperatures; namely 650°C, 700°C, 800°C, 900°C in N_2/H_2 (95%:5%) atmosphere. The annealed wafers were then etched in strong acids (HF, HCl) to get rid of the eutectic metal layer atop. They were cleaned and sonicated in solvents (acetone, ethanol, isopropyl alcohol) to get rid of organic impurities. Characterization tests were done on these wafers to gauge the quality of emitter formed. The wafers were then RCA cleaned and passivated by atomic-layer depositing aluminum oxide (Al_2O_3) layer and annealed at 400°C for post deposition anneal.

In the sections below, we present the experimental setup and the apparatus used in detail, dividing it into individual steps leading to the LPE-D emitter formation

EXPERIMENTAL SETUP

N-type Cz-Si wafers of 125µm thickness and 400Ωcm were used for testing the LPE-D hypothesis. Aluminum powder of 10-15µm particle size from Sigma Aldrich was used as the metal solvent system. Boron powder of 10µm particle size from Strem Chemicals was used as the dopant for the LPE-D emitters. The paste was made with Terpineol oil which was also purchased from Sigma Aldrich. A capping layer was added which prevent dewetting of the surface. Annealing was carried out in a tube furnace in a forming gas atmosphere (N2:H2 - 95%:5%). The wafers were etched in 49% HF for 5 minutes to remove the glass layer, followed by etching in 36% HCl at 60°C for 30 minutes to remove the excess eutectic melt; both being procured from J.T. Baker chemicals. The wafers were then cleaned in soap water and sonicated in standard acetone, ethanol and IPA solutions for 5 minutes each to get rid of organic solvents. The wafers were RCA cleaned and 10nm of Al_2O_3 was deposited on the

surface of the wafer. A post deposition anneal was done to activate Al_2O_3 passivation. Table 4 shows the step by step process of making the emitters.

SAMPLE SIZE USED

The initial tests were performed on 10mm x 15mm c-Si wafers. The clean wafers were cut into the required size with a diamond scribe. They were then cleaned in 1% HF solution for 1 minute to remove the oxide layer from their surface.

For UV-Vis readings and emitter saturation current measurements the wafer size was revised to 25mm x 25mm. The entire process was scaled up by area to accommodate for the change in size of the starting sample.

Table 4: Step by Step process of making the LPE-D emitters.

S. No	STEP
1	Choose the chemistry to work with.
2	Choose the ideal loadings to work with.
3	Choose the size of the wafer
4	Prepare the paste (50 wt% terpineol : 50wt% metal powder)
5	Clean the samples with HF (1 min)
6	Doctor blade the paste and measure weight of the sample before and after
7	Add capping layer
8	Set it in the tube furnace
9	HF (49%) etch the samples to remove oxide
10	DI rinse the samples
11	HCl (36%) etch the samples (30 minutes @ 60°C) to emove the surface metal layer
12	DI rinse the samples
13	Sonicate in Acetone
14	DI rinse the samples
15	Sonicate in Ethanol
16	DI rinse the samples
17	Sonicate in Isopropyl alcohol
18	DI rinse the samples
19	Samples labelled and stored in a box

METAL SOLVENT DOPANT PASTE

Two metal solvent – dopant pastes were used for the experiments. The first paste was made with aluminum as both the metal solvent and the dopant. The second paste was made with aluminum as the metal solvent and boron as the dopant. 1wt% of B in Al powder was used.

This powder was made into a paste with terpineol oil in a 50wt% ratio. Terpineol was chosen as it has a freezing point of 18°C which facilitates the application of a capping layer on top to prevent dewetting of the melted eutectic layer during later stages of the process. Also it has a boiling point between 213°C- 218°C which allows the oil to vaporize during the ramping of annealing process before the eutectic melting starts.

APPLICATION OF PASTE ON SAMPLES

The initial small samples of 10mm x 15mm size, were coated with the paste by doctor blading the desired weight on one side of the wafer. The initial and the final weights were taken to calculate the thickness of the layer deposited on the surface of sample using density-volume calculations.

For the large samples of 25mm x 25mm size, were coated by doctor blading on a makeshift screen printing set-up. Stencils of desired thicknesses were used to guide the pattern. For coating the samples with 40um of solvent load, Ti-stencils of 120µm was used. Figure 15 shows the printing setup along with the thermoelectric cooler which was used to freeze the sample to be able to put a capping layer atop.

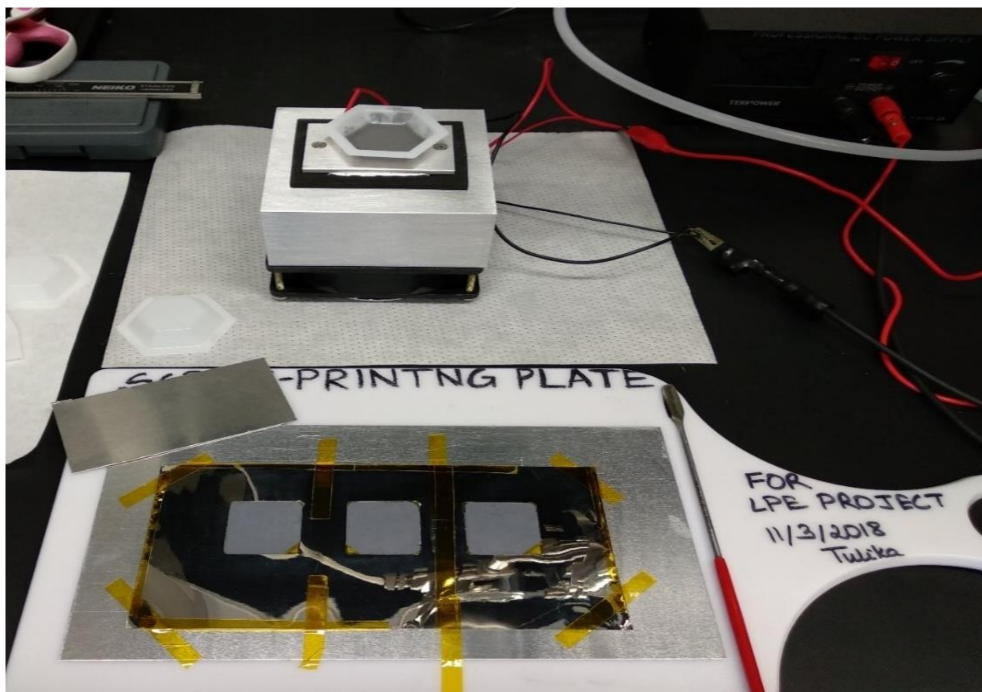


Figure 15: Manual screen printing setup for coating the samples

APPLICATION OF CAPPING LAYER

For the small samples (10mm x 15mm) 20µL of the capping layer precursor was drop casted on the frozen sample. This quantity was changed to 200µL for large samples (25mm x 25mm).

ANNEALING IN TUBE FURNANCE

The coated samples were then kept in silica crucibles and loaded in a tube furnace with an inert environment of forming gas (N_2:H_2= 95%:5%) maintained at 1atm in it. The furnace was programmed for a 10°C/minute ramp rate. Table 5 summarizes the entire process set up in the furnace.

Table 5: Annealing process flow in the tube furnace.

Temperature (°C)	Time (Mins)	Step set in the tube furnace
20°C -- 20°C	10 mins	Maintaining the starting temp. at 20°C
20°C -- 400°C	38 mins	Ramping up to the curing temp. of capping layer
400°C -- 400°C	30 mins	Curing of capping layer

Table 5 continued

400°C -- T_p°C	10°C/ min ramp rate	Ramping up to the peak temp. (T_p°C)
T_p°C -- T_p°C	30 mins	Annealing at peak temp.
T_p°C -- 20°C	10°C/ min ramp rate	Cooling down to room temp.

EUTECTIC LAYER REMOVAL

The metal eutectic layer formed on top of the LPE-D Si wafer is removed by etching in strong acid. First, the glass layer is removed by etching in 49% pure HF for 5-10 minutes as it attacks amorphous SiO2 at significant high etch rates. [18]

The samples are then etched in concentrated HCl (36% pure) for 30 minutes at 80°C to remove the metal eutectic layer that is exposed after the removal of glass layer. Figure 26 in the SEM images section shows the effect to etching time on the surface features of the sample.

To ease the entire process of etching, the samples were etched in makeshift trays to prevent breaking of the fragile wafers while handling. Figure 16 shows the trays used for holding the Si wafers during wet processing.

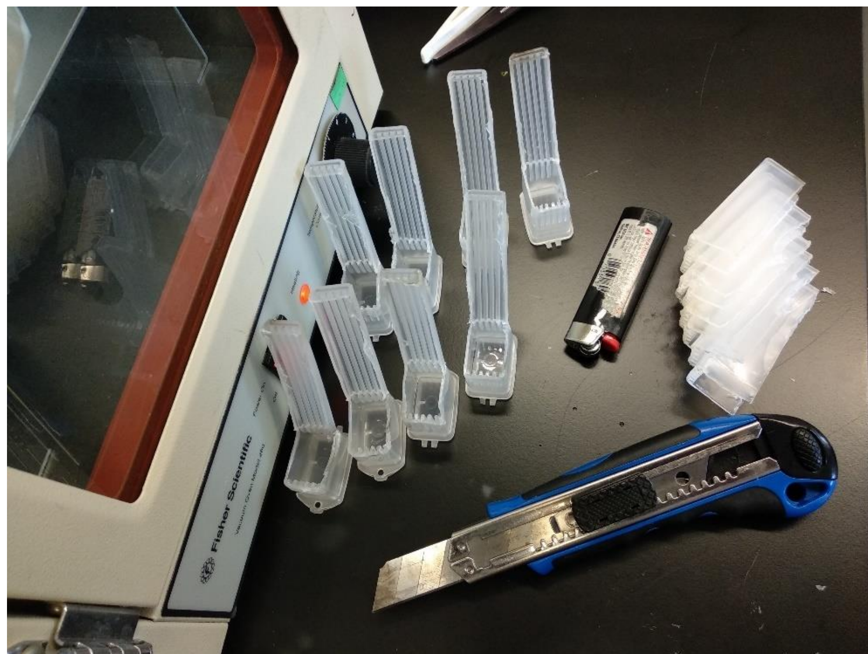


Figure 16: Makeshift trays used for holding wafers.

ORGANIC IMPURITIES REMOVAL

The LPE-D Si wafers were then sonicated in soap water to clean the samples, followed by a 5 minute sonication in each acetone, ethanol and IPA solutions. The wafers were then dried with nitrogen gun and stored in plastic boxes.

TEXTURING OF SAMPLES

Textured Si wafers were used for reflectance measurements. It was done in alkaline conditions, with specific concentrations of IPA and DI water. Texturing process is a multivariable process where each parameter is very difficult to control because of their strong interdependence. The variables that effect the process the most are the time of etching, the composition of texturing solution and the temperature at which it is done. Figure 17 summarizes the effect of all the factors on the process.

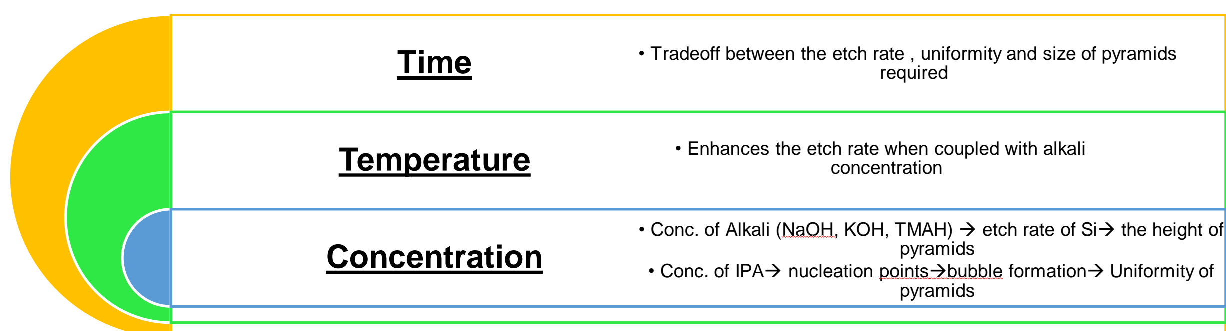


Figure 17: Effect of different variables on texturing process.

The following reaction takes place while texturing [19]:

$$Si + 4H_2O \rightarrow H_4SiO_4 \text{ (Silicon hydroxide)} + 2H_2\uparrow \quad (6)$$

$$H_4SiO_4 \rightarrow H_2SiO_3 \text{ (Silicic acid)} + H_2O \quad (7)$$

$$H_2SiO_3 + 2NaOH \rightarrow Na_2SiO_3 + 2H_2O \quad (8)$$

Silicon surface reacts with water to form silicon hydroxide, which decomposes into silicic acid and water. This Silicic acid further combines with the alkali to give an alkaline salt, resulting in etching of Si. Hence the concentration of the alkali governs the etching of silicon surface i.e. the size of the pyramidal texture. Concentration of IPA effects the homogeneity of the texture, by determining the number of nucleation points on the surface. Figure 18 shows

the effect of concentration of IPA and NaOH on texturing. As we move from left to right (a to d) the concentration of the IPA decreases and NaOH increases. This leads to more Si etching hence the size of the pyramids increases. The final concentrations used for texturing were 6 vol% IPA, 94 vol% DI water and 1wt% NaOH at 80°C.

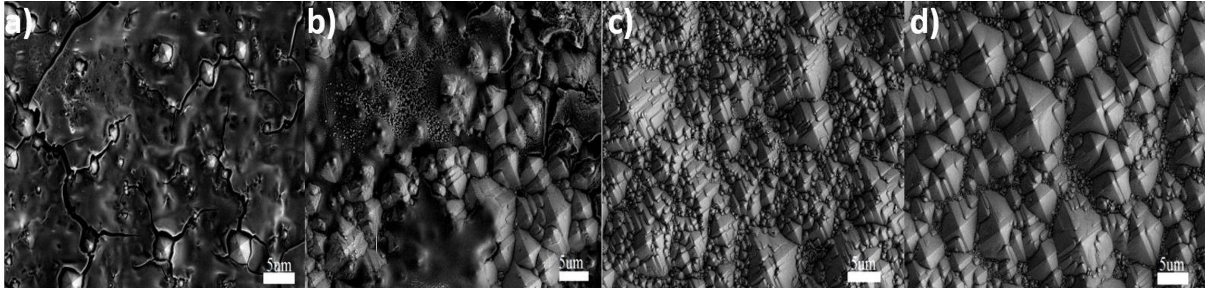


Figure 18: Effect of changing IPA and NaOH concentration on texturing of Si wafer. Scale bar 5μm

Optimal temperatures need to be maintained for the texturing process as high temperatures lead to excessive evaporation of IPA and effects homogeneity, whereas low temperatures facilitate nucleation process. At low temperatures H_4SiO_4 does not decompose into silicic acid and water in a timely manner and it polymerizes and precipitates on the Si surface which is undesirable. Figure 19 shows the polymerized precipitates of H_4SiO_4 or $(Si(OH)_4$ formed.

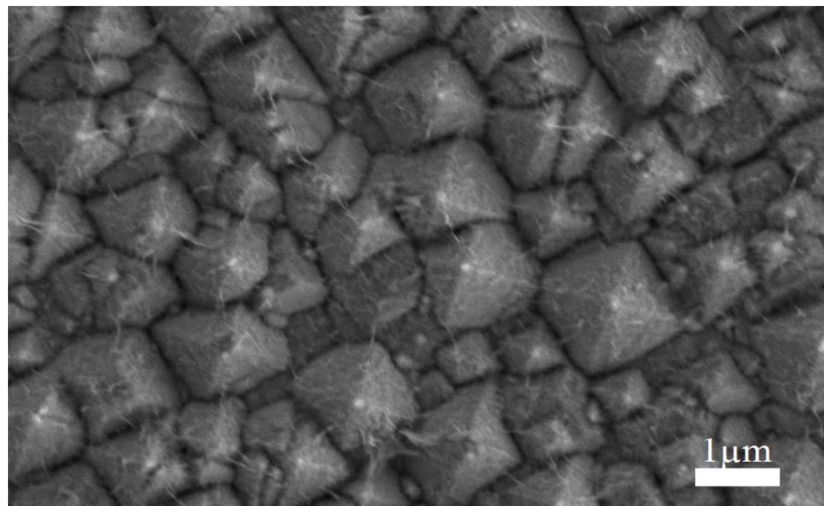


Figure 19: Polymerized precipitates of H4SiO4 or $(Si(OH)_4$ formed due to its incomplete neutralization with NaOH.

For this project a number of apparatus were used to maintain the temperature and composition of the volatile materials used for texturing. Of the few, an experimental setup with a wide open mouth was used to allow for IPA to evaporate slowly at 80°C so that lesser nucleation and more Si etching occurs towards the latter part of the process. Figure 20 shows the set up that was used to texture the Si samples, 25mm x 25mm big.

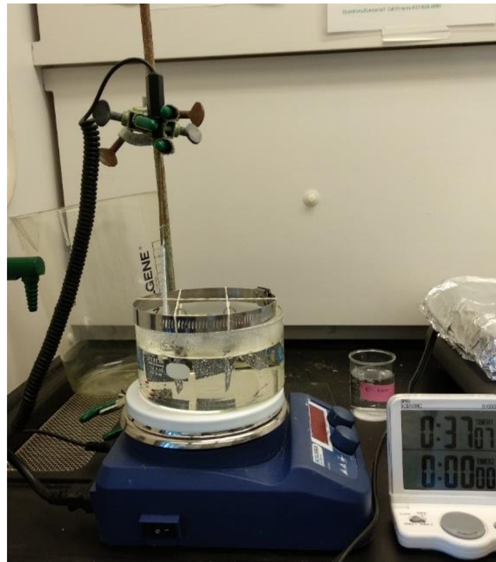


Figure 20: Apparatus used for texturing the Si wafers

The HF cleaned wafers were kept in a texturing solution bath maintained at 80°C for 30 minutes. The texturing solution bath was made with 6 vol % IPA, 94 vol% DI water and 1wt% NAOH. The resulting wafers were found to have a pyramidal texture of 10um size. Figure 21 shows the difference between a smooth Si wafer and a textured wafer.

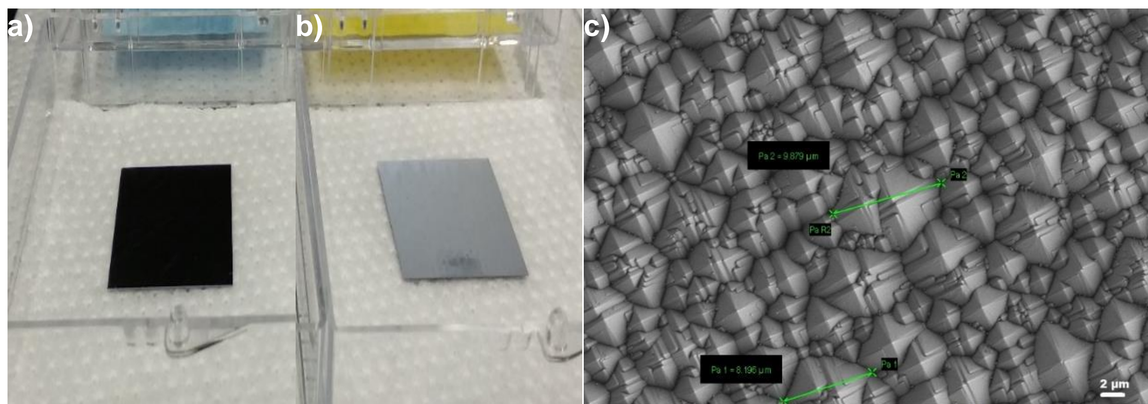


Figure 21: Comparison of a) Plain untextured Si wafer (left) to b) a textured Si wafer (right). c) Textured Si wafer with 10µm pyramids obtained after 30 minutes of texturing at 80°C.

These textured wafers were used as starting wafers for LPE-D doping to examine the change caused in topography of the annealed surface after liquid phase epitaxy doping. Figure 22 shows the textured Si wafer with 16% reflectance at different magnifications.

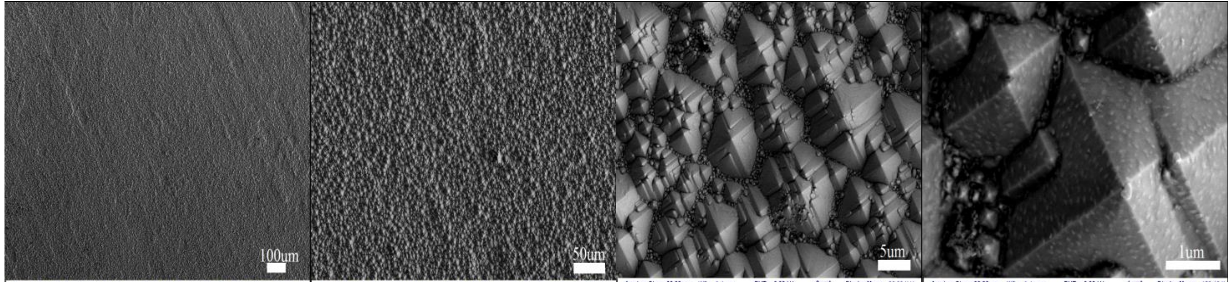


Figure 22: Textured Si wafer at different magnifications.

PASSIVATING OF SAMPLES

The etched and cleaned LPE-D samples were passivated by depositing 10nm of aluminum oxide by atomic layer deposition to reduce their surface recombination velocities. The LPE-D samples were first RCA cleaned by the standard procedure. They were dipped in a RCA-1 bath (NH_4OH:H_2O_2:H_2O in 1:1:5 ratio by volume) at 70°C for 10 minutes. They were then cleaned in D.I. water and dipped for 1 minute in concentrated HF acid. In the end they were etched in RCA-2 bath (HCl:H_2O_2:H_2O in 1:1:5 ratio by volume) at 70°C for 10 minutes.

The Beneq TFS 200 system was used for atomic layer deposition of Al_2O_3. Trimethylaluminum (TMA) and water were used as the precursors in the atmosphere of N_2 gas. The layer was deposited at 250°C for 100 cycles with a growth rate of 1.0789 Å/cycle.

A post deposition anneal was done at 400°C for 30 minutes for all the samples before taking the lifetime and emitter saturation current measurements.

CHAPTER 5: CHARACTERIZATION OF EMITTER

To characterize the samples, four-point probe measurements were used to measure the resistivity of the emitter, and hot point probe measurements were used to measure the type of the wafer. Eutectic melting was confirmed to occur by differential scanning calorimetry (DSC) measurements. The surface topography was seen with the scanning electron microscope (SEM) images and the composition was gauged by energy dispersive x-rays (EDX) mapping of the wafer. Al_2O_3 was deposited by atomic layer deposition (ALD). Reflectance measurements were taken with the UV-Vis spectrophotometer. Lifetime measurements were done on Sinton WCT-120 for measuring the saturation currents and lifetime of carriers in the wafers using QSSPC method as described by Kane et al [20]

In this section we will talk about the different characterization tests carried out on the LPE-D wafers to gauge their performance. Sheet resistance measurements, type testing with hot probe, reflectance measurements and emitter saturation current were done to characterize the quality of doping in the recrystallized Si. Optical microscopy, SEM images and EDX mapping was used to characterize the surface of the wafer.

SHEET RESISTANCE MEASUREMENTS

A Jandel S-232 four-point probe was used to measure the resistivity of the emitters formed by LPE-D method. Initial measurements were made on 10mm x 15mm n-type 125μm thick c-Si wafers. Later the samples (25mm x 25mm) were scaled up to accommodate the requirements of reflectance and emitter saturation current measurements. Figure 23 shows the sheet resistance of small samples (10mm x 15mm) as a function of annealing temperature and compares it to the theoretical predictions of Eq. (5) for two metal solvent loads of 20μm and 40μm of Al-Al system. The R_{sh} values obtained via LPE-D and the simulated values from the theory presented in Table 2 are seen to have a good agreement with each other at all temperatures except at 650°..

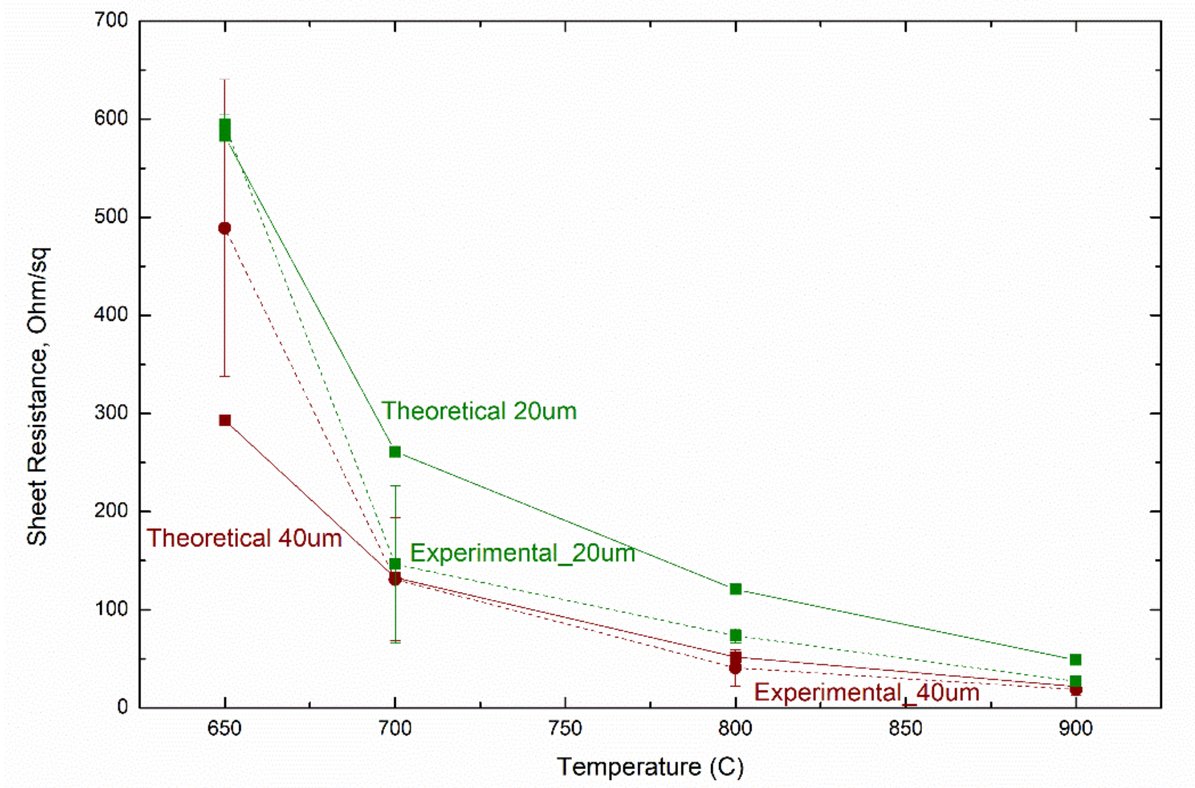


Figure 23: Sheet resistance comparison for Al-Al system at two solvent loads. Add theoretical 20µm line

As the 40 µm solvent load samples show similar values as the theoretical values, this solvent load was chosen for scaling up the sample size Figure 24 shows results for the same solvent load of 40 µm but for samples of different sizes for Al-Al metal solvent – dopant system. Both the large and small samples were seen to have similar sheet resistance values. This suggests that the larger samples are equivalent to the smaller samples and can be used for the further experimental measurements.

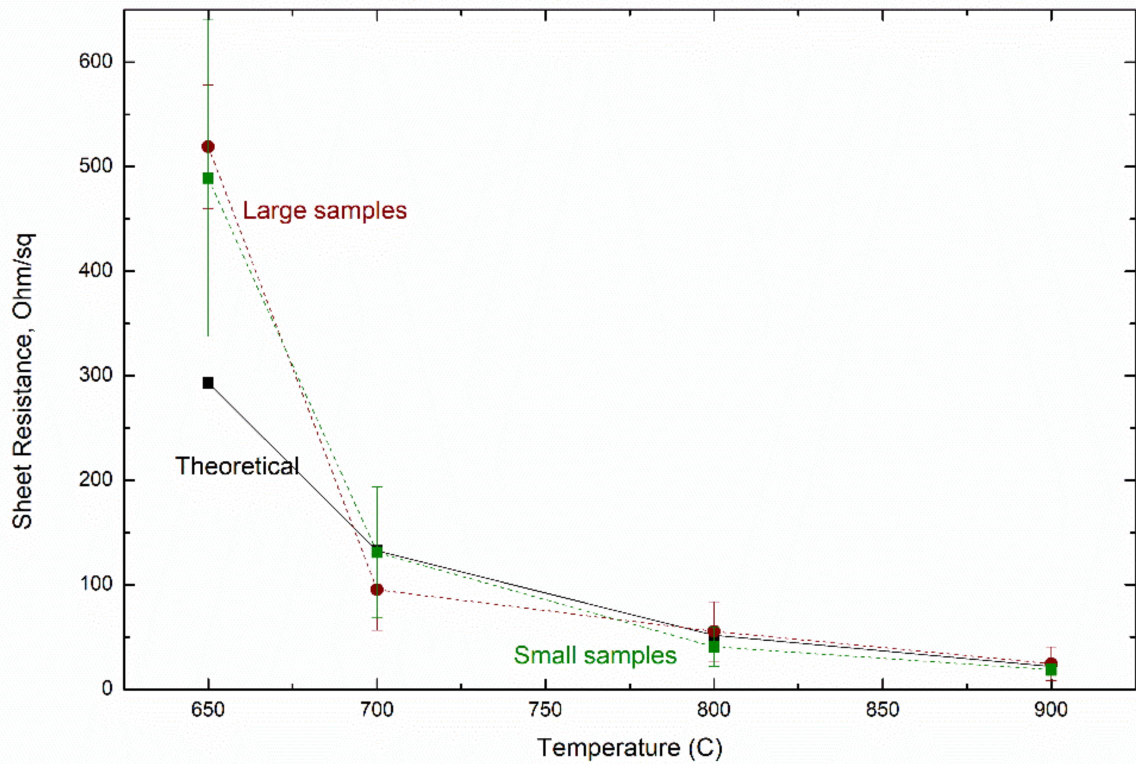


Figure 24: Sheet resistance comparison for samples of different sizes for Al-Al 40µm samples.

LPE-D facilitates the use of different metal solvent- dopant combinations which can tailor the achievable emitter saturation currents and emitter depths at feasible temperatures. Experiments were done with Al-B as the other metal solvent- dopant system for different solvent loads of 20µm and 40µm and for different sizes of the sample. Figure 25 summarizes the effect of different solvent loads on the sheet resistance values of the Al-B LPE-D samples.

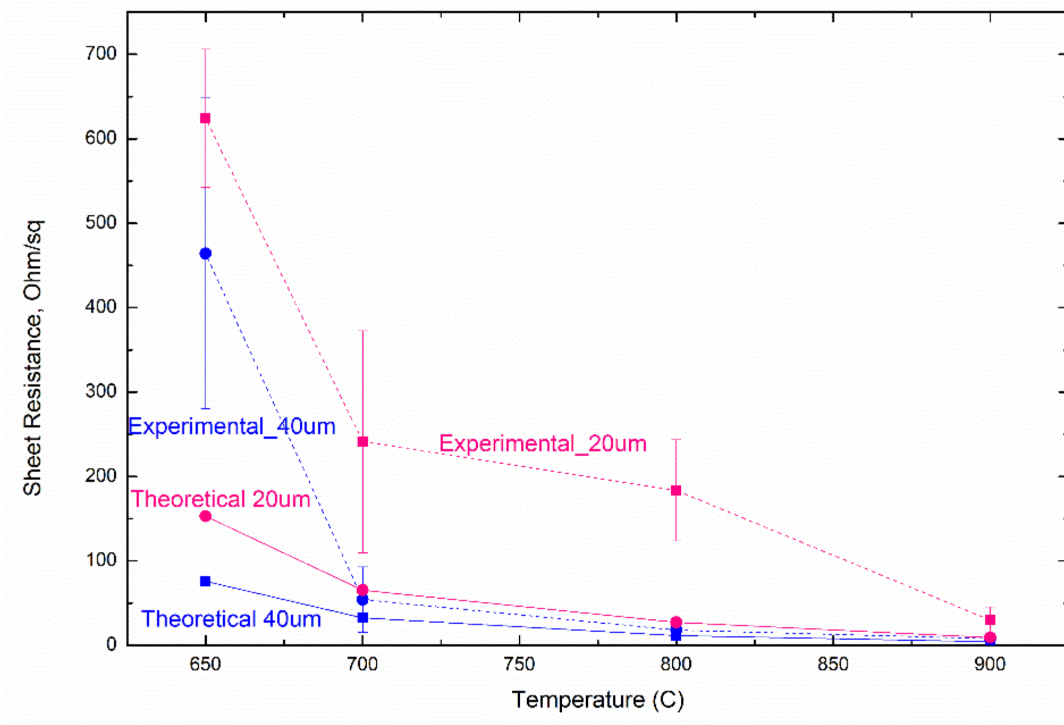


Figure 25: Sheet resistance values for AL-B LPE-D samples for different solvent loads

Figure 26 shows the compliance in sheet resistance values for small and larger sample. From this we can conclude again that large samples are a good representation of smaller samples and can be used for characterization measurements.

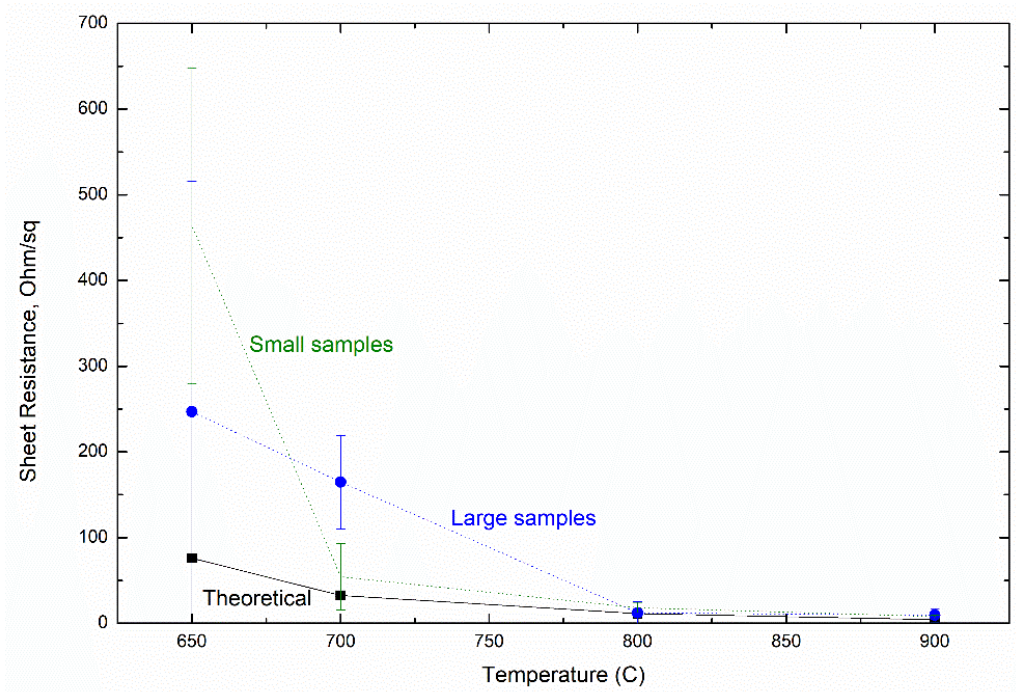


Figure 26: Sheet resistance comparison for samples of different sizes for Al-BI 40μm samples

TYPE TESTING

The LPE-D wafers were tested for their carrier type. Hot probe measurements were used to determine whether the dopes Si layer formed is n-type or p- type. This was done by using a multimeter with one heated probe touching the sample. When the heated probe encounters the surface, it creates an increased number of high energy carriers which diffuse away. Hence, depending upon the sign of the reading of the voltmeter, the type of the sample can be determined.

N-type wafers were used to make the LPE-D emitters. When the multimeter probes (positive heated) were touched on the surface of the samples, the multimeter gave a negative value. This indicates that the layer formed is p-type as their majority carriers, holes diffuse away from the positive lead giving a negative voltage reading for the Si doped layer formed. This was observed for all the small (10mm x 15mm) and large (25mm x 25mm) samples that were made at 650°C, 700°C, 800°C and 900°C.

OPTICAL MICROSCOPE IMAGES

Liquid phase epitaxy doping involves the melting of metal solvent –Si at their respective eutectic temperature, which incorporates more and more near surface Si into the eutectic melt as the temperatures rise to the peak temperature. Since this melt has a eutectic composition to it, the liquid layer has a solid Si layer below it which leads to dewetting of the surface. It was seen that this phenomena of dewetting can be stopped by putting a capping layer on top of the metal solvent-dopant paste. With optical images we could see the effect of capping layer on the wetting of the sample surface. Figure 27 shows the sample surfaces with and without the capping layer for 40μm of Al-Al metal solvent-dopant load that was annealed at 700°C for 30 minutes in a forming gas environment.

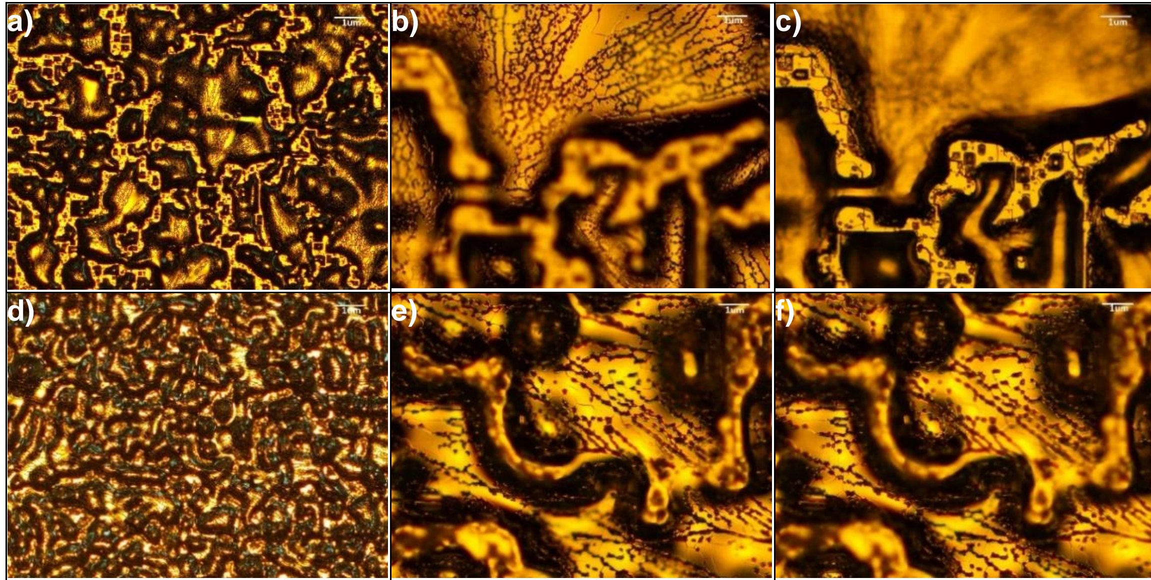


Figure 27: Effect of capping layer on wetting properties of the Al-Al 40µm sample surface made at 700°C a) sample without capping layer at 5x magnification. b) Sample without capping layer at 50x magnification c) sample without capping layer at 50x magnification but at a different z height. d) Sample with capping layer at 5x magnification e) sample with capping layer at 50x magnification f) sample with capping layer at 50x magnification but at a different z height

Samples without the capping layer (Fig 27 a, b, c) can be seen to have small droplet formation, which results because of the ruputure of the thin liquid film. Figure 27a shows the LPE-D sample without capping layer at 5x magnification. Upon increasing the magnification we can clearly see droplet formation (Fig. 27 b) which gets more evident when we change the z-height of the sample measuemnet and the image focuses on different regions of the surface. This suggests the surface has features of a specific height that do not cover the entire area.

However for samples with the cappling layer on top (Fig 27 d, e, f) the surface was found to be smooth. Figure 27 d shows the sample with the caping layer at 5x magnification. It suggests a wavy surface which can be confirmed from the images at 50 x (Fig 27 e). When we change the z height of the sample at 50x magnification (Fig 27 f) we still observe the same feature as in Fig 27 d. This suggests that the capping layer prevents the liquid melt from dewetting on the Si surface.

SEM IMAGES

Optical microscopy images suggested two main points, first; the capping layer helps prevent dewetting from occurring on the Si surface and second LPE-D results in relatively smooth and wavy topography. The same was observed with SEM images. Figure 28 shows a) surface of a sample without the capping layer b) surface of Al-Al LPE-D sample which was annealed at 700°C, 40µm of Al-Al load; and c) surface of Al-B LPE-D sample which was annealed at 800°C at 40µm of Al-Al load. The dewetting can be seen very distinctly in the sample not coated with a capping layer.

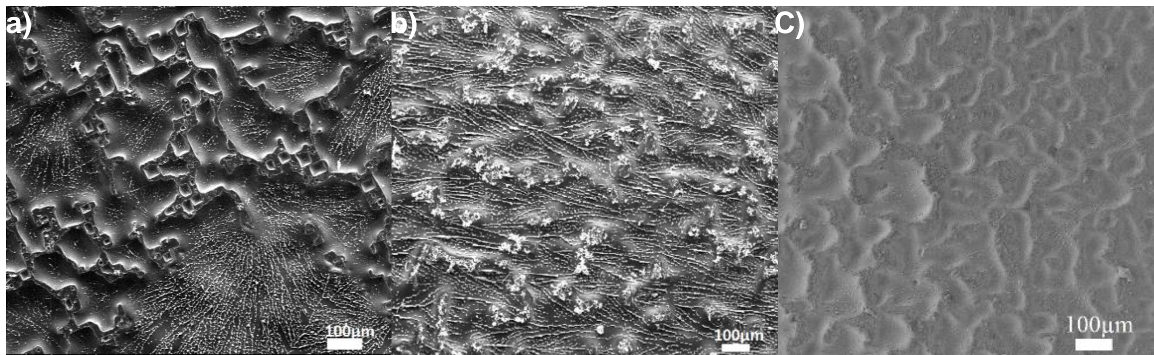


Figure 28: Comparison of LPE-D samples a) without capping layer; b) with capping layer for Al-Al 40µm system at 700°C, c) with capping layer for Al-B 40 um solvent load at 800°C. Scale bar = 100µm

Figure 29 shows a comparison of smooth silicon surface (Fig 29 a) against Al-Al LPE-D surface (Fig 29 b) and Al-B LPE-D surface (Fig 29 c). The Al-Al surface is predominantly characterized by long stream like structures which run across the sample and aluminum rich regions. Al- B LPE-D samples on the other hand just have smooth wavy topography to them.

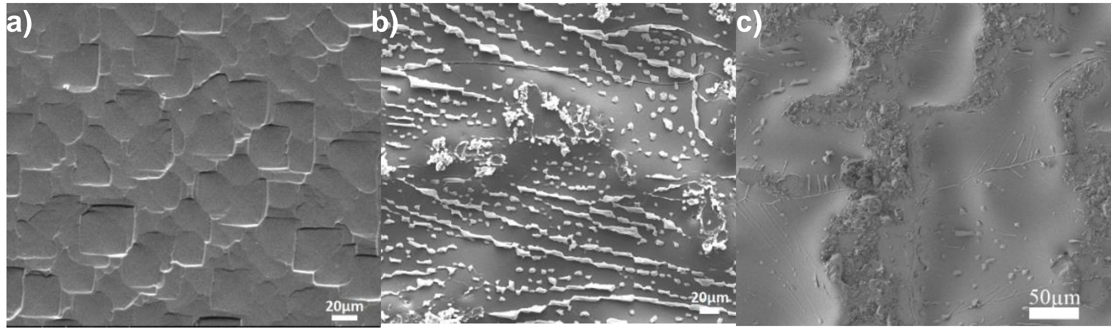
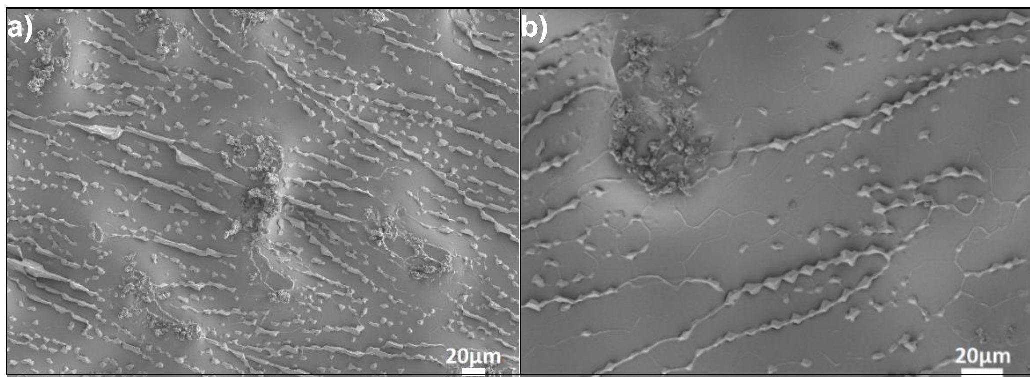


Figure 29: Comparison of Surface topography for an LPE-D silicon surface to a plain Si wafer a)Plain Si wafer; b) LPE-D sample with capping layer for Al-Al 40µm system at 700°C, c) LPE-D sample with capping layer for Al-B 40 um solvent load at 800°C. Scale bar for a,b = 20µm; Scale bar for c = 50µm

These wavy, stream like structures and aluminum rich regions on Al-Al LPE-D regions are undesirable as they would lead to impurities in the emitter layer and an increase in recombination centers. Thus they were etched in concentrated HCl at 60°C for 10mins (Fig 30 b), 20mins (Fig 30 c), 30mins (Fig 30 d). In figure 30 we can see how the surface features change when the etching conditions change. Figure 30 a shows the 40 µm Al-Al LPE-D wafer that was annealed for 30 minutes at 800°C and etched at room temperature concentrated HCl for 10 minutes. It has surface features which get erased as the temperature and duration of the etching process is increased to 60°C and 30 minutes. Hence, with this we decided to etch the metal eutectic layer in concentrated HCl at 60°C for 30 minutes.



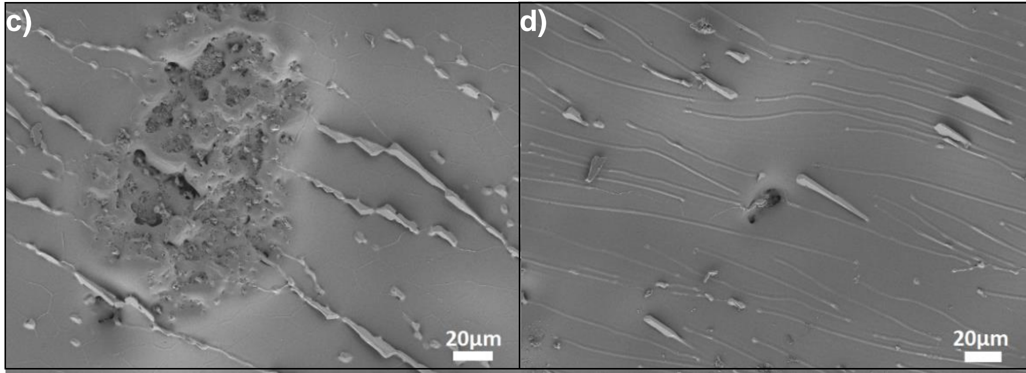


Figure 30: Comparison of 40µm Al-Al LPE-D wafer (700°C) surface after etching for different duration of time. Scale bar = 20µm

EDX MAPPING

Energy dispersive X-ray mapping was measured for LPE-D samples to identify the elemental composition of the sample's surface. It was done for 40 µm Al-Al LPE-D samples annealed at 700°C and 40 µm Al-B LPE-D samples annealed at 800°C. Figure 31 shows the EDX mapping for Al-Al LPE-D samples with fig 31 b showing the Si- Al mapping and fig 31 c showing the Al mapping. The Al mapping shows that it is spread throughout the area mapped and is relatively high in aluminum rich region. With this we can confirm that the dopant (Al) solidifies in the recrystallizing Si and the aluminum rich regions can be removed by prolonged etching in concentrated HCl for 30 minutes at 60°C.

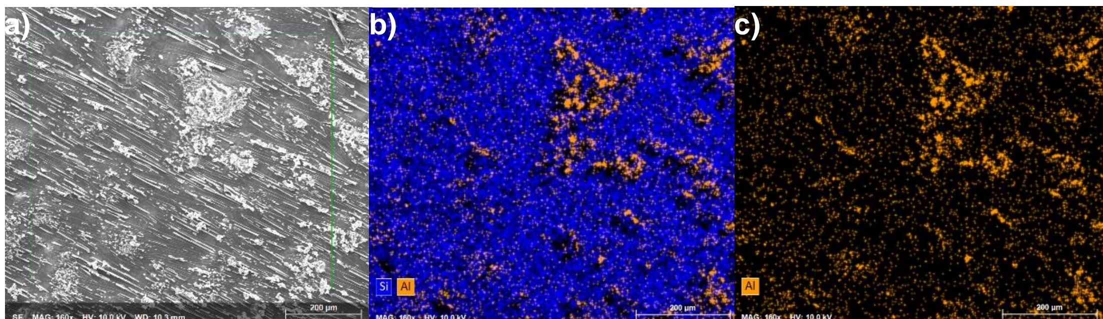


Figure 31: EDX mapping for 40µm Al-Al LPE-D samples made at 700° a) SEM image of the area b) Si-Al map of the area c) Al map of the area. Scale bar = 200µm

Figure 32 shows the EDX mapping for Al-B LPE-D samples Fig b shows the Secondary electron-Si- Al mapping, Fig c shows the Si-Al mapping and Fig d shows the Al mapping of the area being mapped. Boron is not measured during EDX mapping as it is a low atomic number element. The x-rays produced by it do not have enough energy to be detected. However, dark regions appear on the Si-Al map indicating not enough signal is being received from that region. This suggests that the surface of the Al B LPE-D emitter is wavy. It also shows Al rich regions which can be removed by prolonged etching in concentrated HCl for 30 minutes at 60°C.

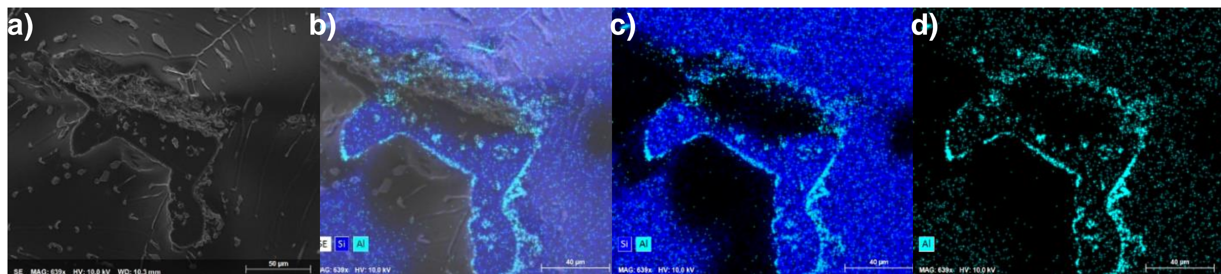


Figure 32: EDX mapping for Al-B LPE-D samples a) SEM image of the area b) SE-Si-Al map of the area c) Si-Al map of the area d) Al map of the area. Scale bar = 40μm

REFLECTANCE MEASUREMENTS

Reflectance measurements were taken to gauge the smoothness of the surface and to have a quantitative idea of the emitter depth. Si wafers with initial pyramidal texture of 10μm and reflectance value of 16% were used to make LPE-D wafers. Figure 33 a shows the initial textured Si wafer which after going through the LPE process at 650°C (Figure 33 b) loses some of its texture. Its reflectance value increases from 16% to 23% indicating loss of texture to smooth area which does not trap light very efficiently.

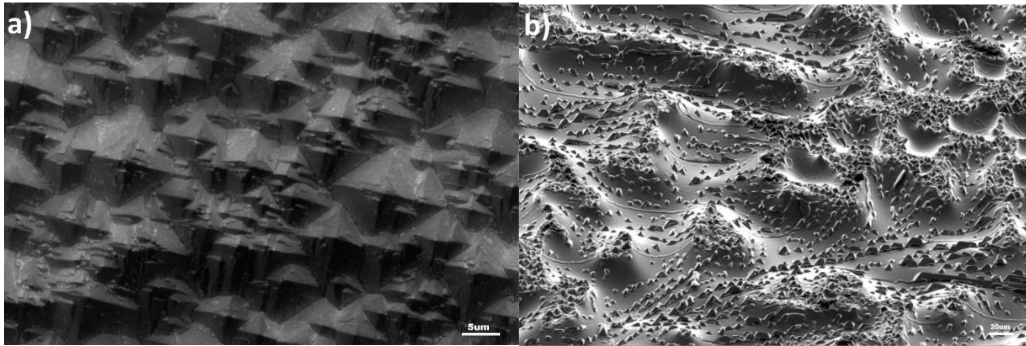


Figure 33: Comparison of the surface of a) textured wafer with 10um pyramidal texture with b) Al-Al LPE-D emitters of 1.5um depth. Scale bar in: fig a = 5μm; fig b = 20μm

The same procedure was done for Al-Al LPE-D emitters at different temperatures corresponding to different depths. The results of the same have been shown in figure 34. As the temperature increases, the emitter depth increases. This results in more loss of texture hence further increase in the value of reflectance.

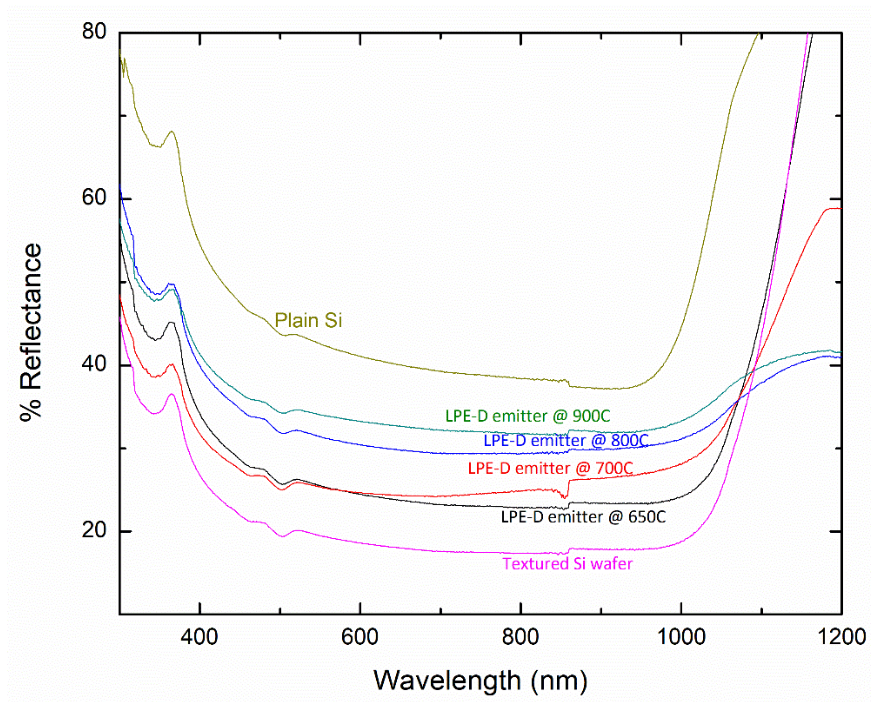


Figure 34: Reflectance measurements of LPE-D emitters at different temperatures indicating the change in emitter depth.

The pictorial representation of the same can be seen on figure 35, where the reflectance values for LPE-D emitters are shown at 600nm. As the temperature increases, the emitter depth increases and the size of the textured pyramids decreases, resulting in increase in reflectance values.

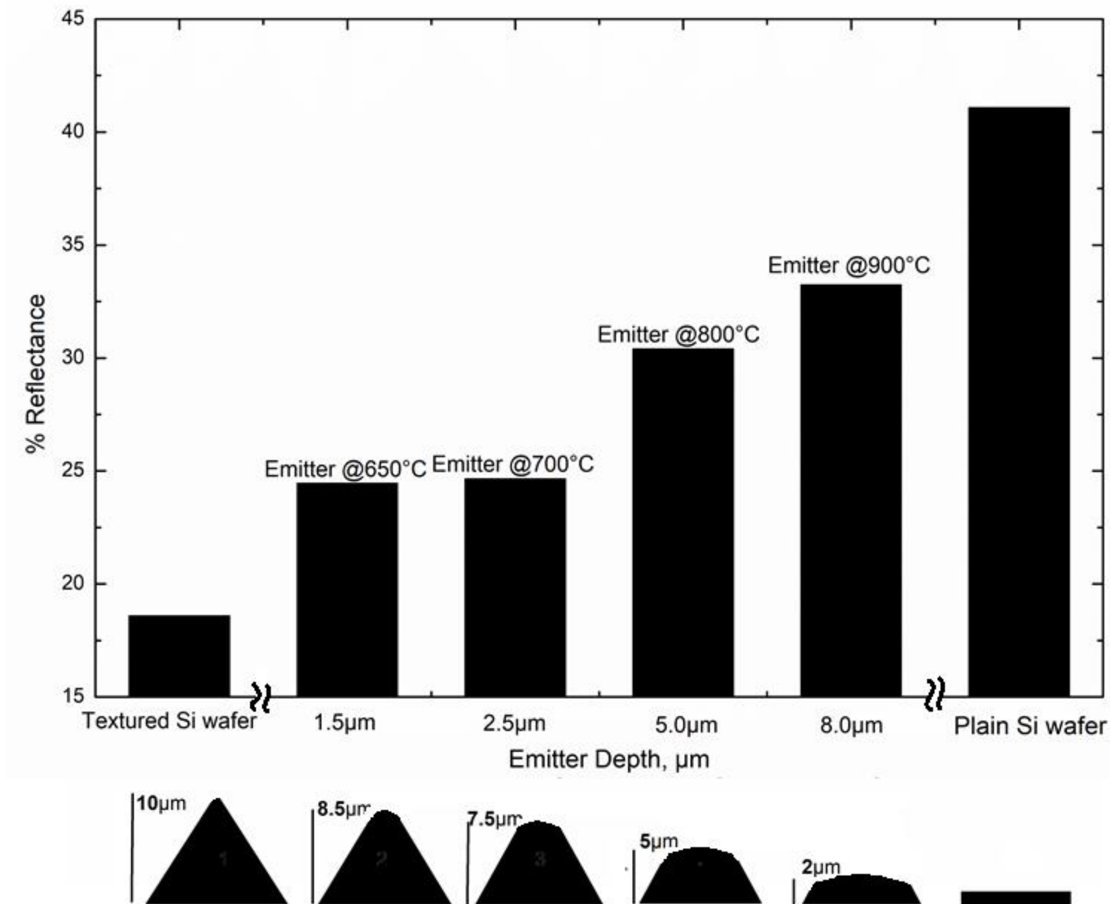


Figure 35: Reflectance measurements of LPE-D emitters at 600nm for different temperatures indicating the change in emitter depth.

EMITTER SATURATION CURRENT MEASUREMENTS

The electronic quality of the LPE-D samples is accessed by their emitter saturation current. Al-B LPE-D Si wafers were passivated Al_2O_3 and quasi-steady state photo conductance measurements performed to measure emitter saturation current density. A film formed on the surface of the LPE-D wafers at high temperature that resisted standard etching, causing high J_{0e} values. The surface film was largely removed by etching for longer durations (up to 5 hours in concentrated HCl at 60°C). Removing the surface film enabled better surface passivation to be achieved, decreasing the J0e values from 1041 fA/cm^2 to 495 fA/cm^2 for 800°C Al-B samples.

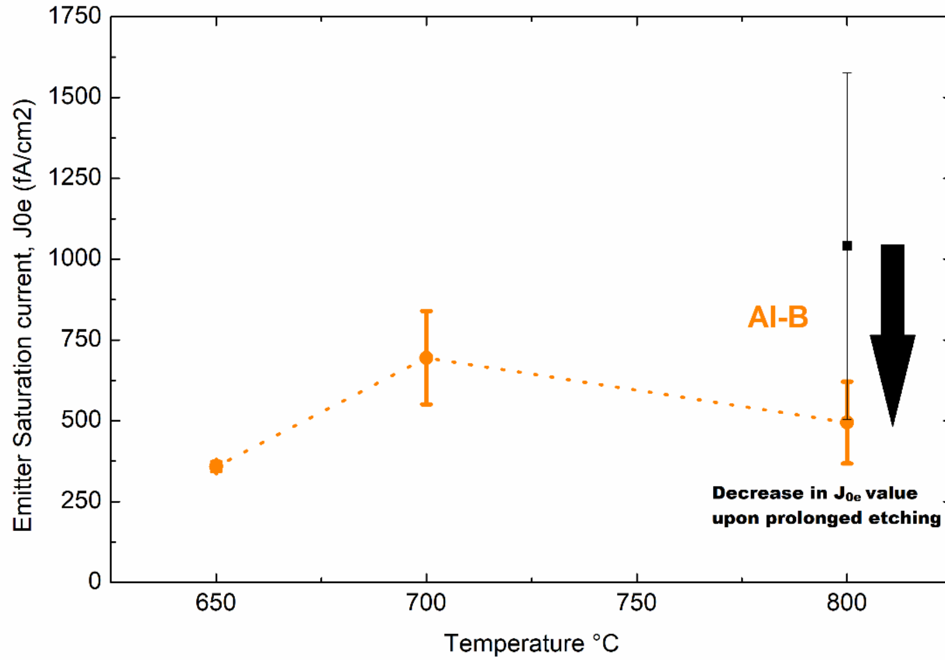


Figure 36: Emitter saturation current, J_{0e} values for Al-B LPE-D samples at different temperatures after prolonged etching of 5 hours.

Figure 36 shows the J_{0e} values for Al-B LPE-D samples at different temperatures. This J_{0e} includes contributions to saturation current stemming from lingering areas of highly-imperfect surface passivation and likely includes a component from low Shockley-Read-Hall lifetime in the emitter as impurities were not carefully controlled in the proof-of-concept experiments.

CHAPTER 6: NOVEL CHEMISTRY

LPE-D process allows the use of several different metal solvents which have low eutectic temperature with Si. Above we have shown results for Al-Al and Al-B metal solvent – dopant combinations. In this section we will talk about using Tin and Zinc as the metal solvent system.

TIN

Tin and silicon have a low eutectic temperature of roughly 230°C making it a good candidate for LPE-D experiments. But it also has a low eutectic composition of less than 1% Si which makes it difficult to work with. Figure 37a shows the phase diagram for Sn-Si system and we can infer that large metal solvent loads of tin are required to get a thin layer of eutectic melt that would cover the surface. DSC measurements were done for 500µm solvent load of Sn-B-Si samples and the peak was recorded at 235°C, which confirms the presence of eutectic melting.

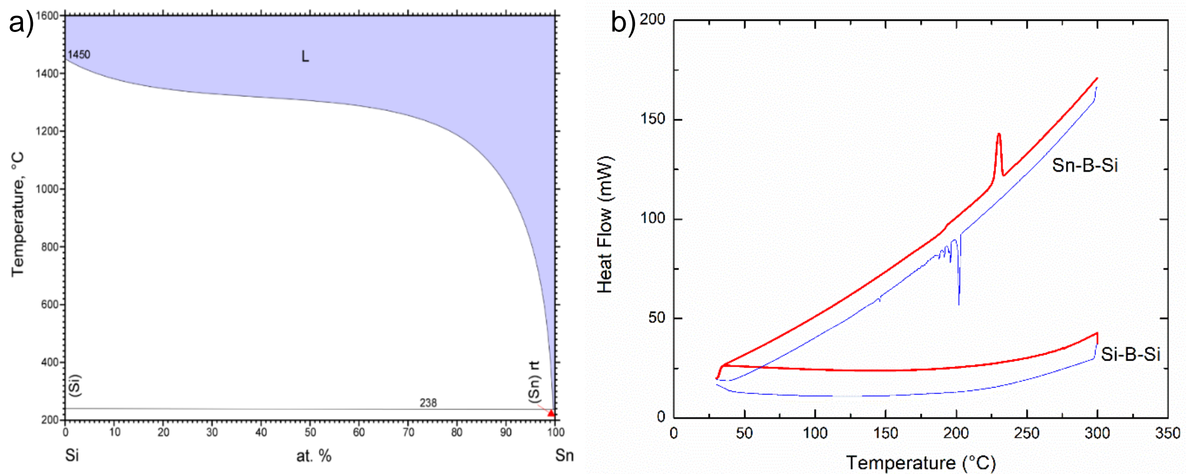


Figure 37: The Sn-Si system has a eutectic temperature at 238°C as can be seen in a) the phase diagram for Si-Sn system [21]. b) DSC measurements done for Sn-B-Si samples.

Experiments were carried out for high solvent loads up to 1000µm on a 125 µm thick Si wafer. For the smaller samples (10mm x 15mm) significant amount of dewetting occurred.

Figure 30b shows the Sn-B LPE-D sample after annealing at 650°C for 30 minutes at 500 µm solvent load in a tube furnace.

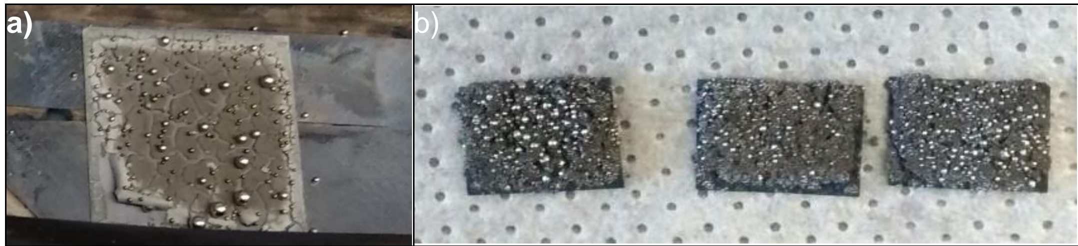


Figure 38: Sn-B LPE-D samples after annealing at 650°C.

Figure 38 a shows the large samples of Sn-B LPE-D that were made at 650°C and 500µm load with the capping layer on top. They also showed the bead formation even when dewetting was curbed by the capping layer. This bead formation nature can be possible due to the immiscible liquid phase of tin -rich melts. [7]

ZINC

Zinc and silicon are known to have a eutectic melting point at 420°C, which makes it a good choice for LPE-D method. Figure 39 shows the phase diagram for Zn-Si system. [22]

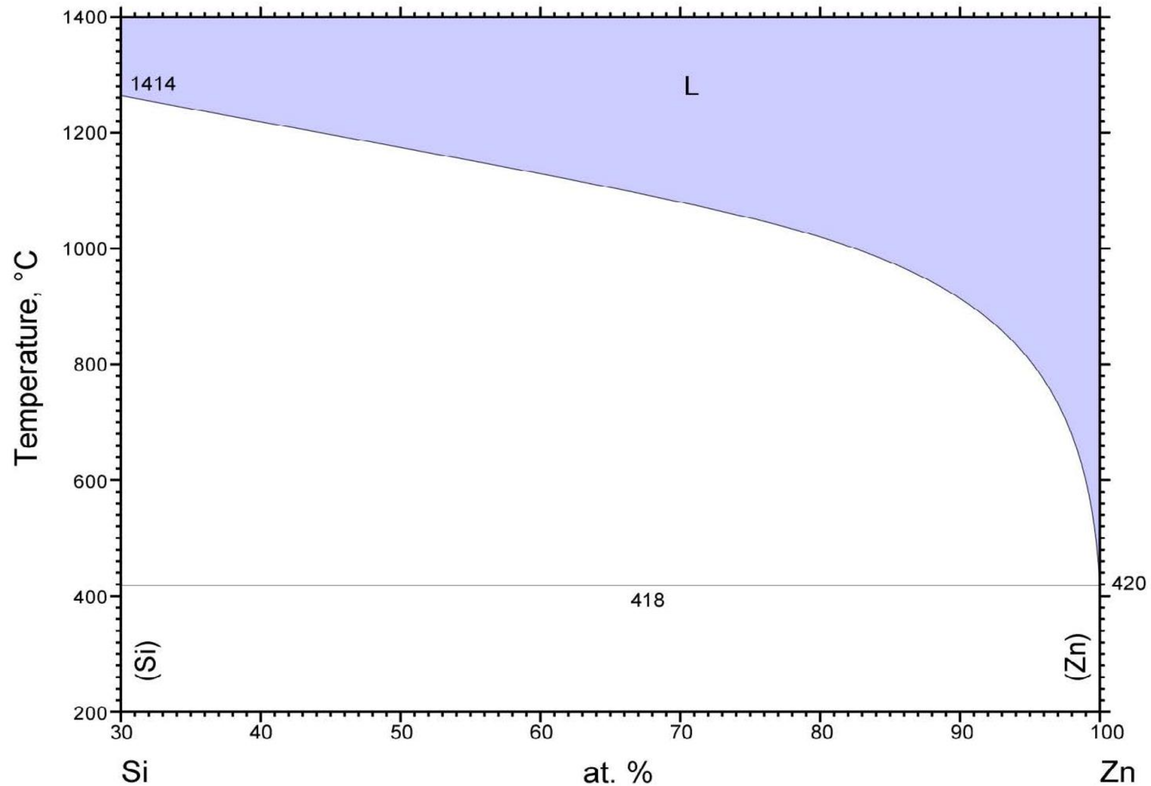


Figure 39: Phase diagram for Zn-Si system. [22]

Experiment were carried out for a load of 40µm. However Zinc has low vapor pressure which causes it to vaporize completely around 272°C, resulting in no solid zinc left for eutectic melting to occur at 420°C. Figure 40 shows the 40µm solvent load of Zn-B LPE-D samples that were set for annealing at 650°C and had a capping layer on top. It looks like the zinc evaporated past the barrier layer that was created by the solidified glass, giving it, the broken texture as seen below. Thus Zn does not seem a viable solvent metal for LPE-D.

Figure 40: Sn-B LPE-D samples after annealing at 650°C

CHAPTER 7: FUTURE WORK

LPE-D method has shown a potential of producing emitters in a cost-effective manner than traditional tube diffusions, but research needs to be done to make the process more reproducible and to demonstrate its performance in solar cells.

There is a layer formation or a film on the sample surface at high temperatures. It can be removed from some samples by prolonged etching in concentrated HCl but higher temperature (900°C) do not respond to this solution. More study needs to be done for characterizing the film and devising efficient ways to remove it.

Design of experiments needs to be done for Zn-Si system such that the evaporated zinc can be used for creating vapor pressure which counter balances further vaporization of zinc.

Further simulations are needed to obtain a range of potentially achievable emitter saturation current values rather than a single lower limit presented above. This will be achieved by varying fundamental surface recombination velocity and bulk emitter lifetime in ranges reflecting the quality of the emitter presented in this work. The ranges will be selected based on our available lifetime data and on literature results for Al_2O_3-passivated p+ emitters [15, 23]

CHAPTER 8: CONCLUSIONS

Liquid phase epitaxy doping forms layers with low sheet resistances that can be tuned for different depths. The emitter depth and hence the surface dopant concentration can also be controlled with the peak temperature of the process. It also results in rounding of the sharp pyramidal texture features thus, avoiding the saturation of electric field on these points.

LPE-D can be done at relatively lower temperatures and does not require the use or handling of toxic gases while manufacturing. It can be coupled up with screen printing facilities available in the industry thus reducing the capex cost of manufacturing of the solar cell. Lesser process times can be achieved with this as it opens the option of inline automation.

With more research on performance of LPE-D emitters and dopant-solvent systems, LPE-D may offer a potential to decrease the overall cost of manufacturing silicon solar cells.

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