InGaAs–InP Mesa DHBTs With Simultaneously High f_τ and $f_{\max}$ and Low $C_{\rm cb}/I_c$ Ratio

Z. Griffith, M. Dahlström, M. Urteaga, M. J. W. Rodwell, X.-M. Fang, D. Lubyshev, Y. Wu, J. M. Fastenau, and W. K. Liu

***Abstract*—We report an InP–InGaAs–InP double heterojunction bipolar transistor (DHBT), fabricated using a conventional triple mesa structure, exhibiting a 370–GHz f_τ and 459–GHz $f_{\max}$, which is to our knowledge the highest f_τ reported for a mesa InP DHBT—as well as the highest simultaneous f_τ and $f_{\max}$ for any mesa HBT. The collector semiconductor was undercut to reduce the base–collector capacitance, producing a $C_{\rm cb}/I_c$ ratio of 0.28 ps/V at $V_{\rm cb} = 0.5$ V. The $V_{\rm BR,CEO}$ is 5.6 V and the devices fail thermally only at > 18 mW/μm^2, allowing dc bias from $J_e = 4.8$ mA/μm^2 at $V_{\rm ce} = 3.9$ V to $J_e = 12.5$ mA/μm^2 at $V_{\rm ce} = 1.5$ V. The device employs a 30 nm carbon-doped InGaAs base with graded base doping, and an InGaAs–InAlAs superlattice grade in the base–collector junction that contributes to a total depleted collector thickness of 150 nm.**

***Index Terms*—Heterojunction bipolar transistor (HBT).**

I. Introduction

WITH THE deployment of 40 Gb/s time-division multiplexing (TDM)-based fiber IC chipsets underway, improvements in transistor design and performance are being pursued for the development of systems operating at 160 Gb/s and higher. To realize such systems, the heterojunction bipolar transistor (HBT) specifications require an f_τ and $f_{\max}$ greater than 440 GHz, a breakdown voltage $V_{\rm BR,CEO}$ exceeding 3 V, operating current density J_e greater than 10 mA/μm^2 at $V_{\rm cb} = 0$ V, and low base–collector capacitance ($C_{\rm cb}/I_c < 0.5$ ps/V) [1]. These HBTs would also permit microwave analog-to-digital converters (ADC) of increased bandwidth. Improving a transistor so that all digital circuits making use of it become faster involves proportionally, reducing all capacitances and transit times, while keeping constant the device I_e, g_m, and parasitic resistances ($R_{\rm bb}$, $R_{\rm ex}$). This can be accomplished by a combination of a thinner collector, narrower emitter and collector junctions, lower specific contact resistances, and increased operating current density [2].

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Z. Griffith, M. Dahlström, and M. J. W. Rodwell are with the Department of Electrical and Computer Engineering, University of California, Santa Barbara, CA 93106 USA (e-mail: griffith@ece.ucsb.edu).

M. Urteaga was with the Department of Electrical and Computer Engineering, University of California, Santa Barbara, CA 93106 USA. He is now with Rockwell Scientific Corporation, Thousand Oaks, CA 91360 USA.

X.-M. Fang, D. Lubyshev, Y. Wu, J. M. Fastenau, and W. K. Liu are with IQE, Inc., Bethlehem, PA 18015 USA.

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At a given scaling generation, defined by the minimum emitter feature size, different transistor layer structures are preferred so as to obtain a differing balance of device parasitics that are more suited for the particular application, i.e., millimeter-wave tuned amplifiers benefit from high $f_{\max}$ and can tolerate appreciably lower f_τ. The minimum gate delay of a digital IC in contrast is not determined by an algebraic function of f_τ and $f_{\max}$ [3], but instead by a set of time constants of which $C_{\rm cb}\Delta V_{\rm logic}/I_c$ is a major contributor. In selecting the collector thickness T_c for minimum gate delay, attention must be given to all delay terms because while $C_{\rm cb}\Delta V_{\rm logic}/I_c \propto T_c$, the high J_e associated with thin collector's results in both significant device self-heating [4] and an increased $I_E R_{\rm ex}$ voltage drop.

Prior to this work, the highest f_τ reported for an InP double heterojunction bipolar transistor (DHBT) was 351 GHz using a 150-nm collector, 25-nm base, and an InGaAsP base–collector grade [5]. The highest $f_{\max}$ reported for a mesa InP DHBT is 492 GHz using a 150-nm collector, 30-nm base, and an InGaAsP base–collector grade [6]. Here, we report a 370-GHz f_τ and 459-GHz $f_{\max}$ InP–InGaAs–InP mesa DHBT, the highest f_τ for a mesa InP DHBT [7], and a record low $C_{\rm cb}/I_c$ ratio $=$ 0.28 ps/V at $V_{\rm cb} = 0.5$ V.

II. Design

Given the junction dimensions currently feasible in our laboratory, a 150-nm collector depletion thickness was selected through digital circuit gate-delay expressions [1], [2] and the maximum current density this collector thickness can support. The maximum current density before collector field collapse is

$$J_{\max} \approx 2\varepsilon v_{\rm eff}\frac{(V_{\rm cb}+V_{\rm cb,min}+2\phi)}{T_C^2} \tag{1}$$

where $v_{\rm eff}$ is the effective collector electron velocity, $V_{\rm cb,min}$ is the voltage required for full collector depletion at $J_e = 0$, and ϕ is the internal junction potential—approximately equal to the base bandgap. The collector capacitance charging time during a data transition $\tau \propto C_{\rm cb}\Delta V_{\rm logic}/I_c$ is therefore

$$\tau \propto \frac{C_{\rm cb}\Delta V_{\rm logic}}{I_c} = \frac{\Delta V_{\rm logic}}{(V_{\rm cb}+V_{cb,\rm min}+2\phi)}\left(\frac{A_{\rm collector}}{A_{\rm emitter}}\right)\left(\frac{T_C}{2v_{\rm eff}}\right). \tag{2}$$

If the HBT operating current density can be maintained at $J_{\max}$, then $C_{\rm cb}\Delta V_{\rm logic}/I_c$, often the dominant delay in HBT digital ICs [1], [2], is proportional to T_c, the collector thickness. To increase digital circuit speed, the collector must be thinned, but

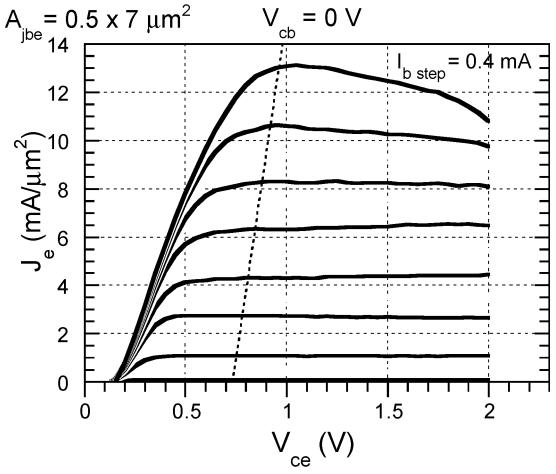

Fig. 1. Common emitter *I–V* characteristics.

not to the point the HBTs cannot operate at $J_{\max}$ due to either excessive device self-heating [3] or excessive voltage drop $I_E R_{\rm ex}$ on the emitter parasitic resistance. As T_c is reduced and $J_{\rm kirk}$ consequently increased, progressive reductions in thermal resistance $\theta_{\rm JA}$ and emitter parasitic resistance ρ_e are therefore required, in addition to narrowing the emitter junction for reduced $R_{\rm bb}$ per unit emitter area.

Low base resistance $R_{\rm bb}$ is desirable for both low gate delay and high $f_{\max}$. The InGaAs base is heavily doped for low base contact resistance, and a combination of a doping grade and thin 30-nm base both increase dc current gain and decrease base transit time. Details of the base and collector layer design are given in [8]. Contacts to the subcollector are on 12.5 nm of n^+ InGaAs above the n^+ InP. The InGaAs portion of the subcollector acts as an etch stop layer and is needed to maintain low $\rho_{\rm c}$. Recognizing that the thermal conductivity of bulk InGaAs ($0.048\ W/({\rm cm}\cdot{\rm K})$) is much lower than InP ($0.68\ W/({\rm cm}\cdot{\rm K})$), the InGaAs subcollector is kept thin to minimize thermal resistance to the substrate to enable high device operating current density J_e [4].

III. Growth and Fabrication

The epitaxial material was grown by IQE Inc. on a 3-in SI-InP wafer and the HBTs were fabricated in an all-wet-etch, triple-mesa process. Emitter contact widths vary from 0.4–2.0 μm and self-aligned base contacts extend 0.3, 0.5, or 1 μm on each side of the emitter metal. To reduce the external base–collector capacitance of the device underneath the base contact, the active collector semiconductor was over etched during formation of the base–collector junction producing 200 nm of undercut. After device passivation with polyimide, a single layer of metal forms device interconnects.

IV. Results

Standard transmission line measurement (TLM) show the base $\rho_{\rm s} \cong 603\ \Omega$ and $\rho_{\rm c} \cong 20\ \Omega\cdot\mu{\rm m}^2$, collector $\rho_{\rm s} \cong 12\ \Omega$ and $\rho_{\rm c} \cong 9\ \Omega\cdot\mu{\rm m}^2$, and the emitter $\rho_{\rm c} \cong 10-15\ \Omega\cdot\mu{\rm m}^2$. The HBTs have a dc current gain β of 8–11 and the breakdown voltage $V_{\rm BR,CEO}$ is 5.6 V. Fig. 1 shows common emitter current–voltage (*I–V*) characteristics.

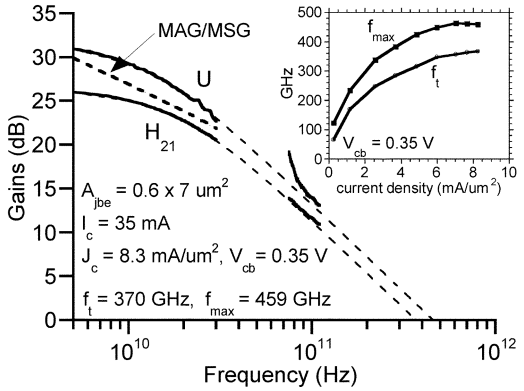

Fig. 2. Measured microwave gains.

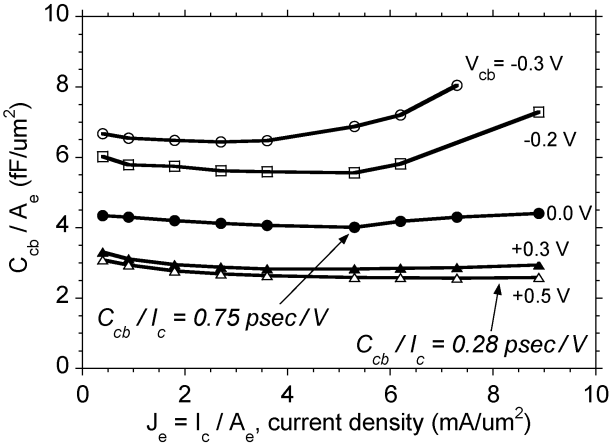

Fig. 3. $C_{\rm cb}/A_e$, the collector–base capacitance normalized to the emitter junction area as a function of bias.

Thermal resistance $\theta_{\rm JA}$ and device junction temperature were measured using the method of Liu [9]. An HBT with a 0.6-μm emitter junction width exhibits a $\Delta T \cong 132$ K emitter junction-to-ambient temperature increase when dissipating 18 $\rm mW/\mu m^2$. The devices fail thermally only at $> 18{\rm mW}/\mu{\rm m}^2$, allowing dc bias from $J_e = 4.8\ {\rm mA}/\mu{\rm m}^2$ at $V_{\rm ce} = 3.9$ V to $J_e = 12.5\ {\rm mA}/\mu{\rm m}^2$ at $V_{\rm ce} = 1.5$ V. Note that the collector junction may be substantially hotter than the emitter junction due to the combined effects of heat removal from the emitter through the emitter interconnect metal, and the high thermal resistance of the InGaAs base layer.

Our 5–30- and 75–110-GHz RF measurements were performed using on-wafer line-reflect-line (LRL) calibration structures, as well as open-short-line-thru (OSLT) calibration in the 5–30 GHz band. Because different on-wafer pad structures are required, the 5–30- and 75–110-GHz data is taken from different devices having the same dimensions. The HBTs exhibited a simultaneous maximum 370-GHz f_τ and 459-GHz $f_{\max}$ (Fig. 2) at $I_c = 35$ mA and $V_{\rm ce} = 1.3$ V ($J_e = 8.3\ {\rm mA}/\mu{\rm m}^2$, $V_{\rm cb} = 0.35$ V). The devices have a $0.6\times 7\ \mu{\rm m}^2$ emitter junction and 1.7-μm base-mesa width. At these dc bias conditions and HBT dimensions, the devices experience an emitter to ambient temperature increase of $\Delta T \cong 75$ K. In addition, comparisons of $h_{21} \equiv dI_c/dI_b$ for the measured dc common-emitter *I–V* characteristics (Fig. 1) and the low-frequency RF values (Fig. 2) are in good agreement with each other, ≈ 26 dB. Fig. 3

shows the variation of $C_{\rm cb}/A_e$ versus operating current density J_e and $V_{\rm cb}$ for use in emitter coupled logic (ECL) circuit design. For HBTs biased as ECL emitter followers ($V_{\rm cb} = 0$ V, $J_e = 5.5$ mA/μm^2), the minimum $C_{\rm cb}/I_c$ before Kirk effect is 0.75 ps/V while for ECL current steering HBTs ($V_{\rm cb} = 0.6$ V, $J_e > 8$ mA/μm^2), $C_{\rm cb}/I_c \leq 0.28$ ps/V.

The improvements in HBT performance compared to [8] are due to decreased base and emitter contact resistances, increased current density, and a collector undercut of 200 nm. The measured HBT performance is consistent with an HBT finite element model [2] using the measured contact and sheet resistivities, the known device geometry, and values of base electron diffusivity and collector electron velocity extracted from a set of measurements on similar DHBTs on the wafer.

REFERENCES

[1] T. Enoki, E. Sano, and T. Ishibashi, "Prospects of InP-based IC technologies for 100-Gbit/s-class lightwave communications systems," *Int. J. High-Speed Electron. Syst.*, vol. 11, no. 1, pp. 137–158, 2001.

[2] M. J. W. Rodwell, M. Urteaga, Y. Betser, D. Scott, M. Dahlström, S. Lee, S. Krishnan, T. Mathew, S. Jaganathan, Y. Wei, D. Mensa, J. Guthrie, R. Pullela, Q. Lee, B. Agarwal, U. Bhattacharya, and S. Long, "Scaling of InGaAs–InAlAs HBTs for high speed mixed-signal and mm-wave ICs," *Int. J. High-Speed Electron. Syst.*, vol. 11, no. 1, pp. 159–215, 2001.

[3] W. Hafez, J.-W. Lai, and M. Feng, "InP–InGaAs SHBTs with 75-nm collector and $f_\tau > 500$ GHz," *Electron. Lett.*, vol. 39, no. 20, pp. 1475–1476, 2003.

[4] I. Harrison, M. Dahlström, S. Krishnan, Z. Griffith, Y. M. Kim, and M. J. W. Rodwell, "Thermal limitations of InP HBTs in 80 and 160 $\rm Gbits^{-1}$ ICs," in *Proc. IEEE Int. Conf. Indium Phosphide and Related Materials*, Santa Barbara, CA, May 12–16, 2003, pp. 160–163.

[5] M. Ida, K.Kenji Kurishima, and N. Watanabe, "Over 300 GHz f_T and $f_{\rm max}$ InP–InGaAs double heterojunction bipolar transistors with a thin pseudomorphic base," *IEEE Electron Device Lett.*, vol. 23, pp. 694–696, Dec. 2002.

[6] ——, "High-speed InP–InGaAs DHBTs with a thin pseudomorphic base," in *Proc. IEEE GaAs IC Conf.*, San Diego, CA, Nov. 9–12, 2003, pp. 211–214.

[7] M. Dahlström, Z. Griffith, M. Urteaga, M. J. W. Rodwell, X.-M. Fang, D. Lubyshev, Y. Wu, J. M. Fastenau, and W. K. Liu, "InGaAs–InP DHBTs with $>$ 370 GHz f_τ and $f_{\rm max}$ using a graded carbon-doped base," in *Proc. IEEE Device Research Conf.*, Salt Lake City, UT, June 23–25, 2003.

[8] M. Dahlström, X.-M. Fang, D. Lubyshev, M. Urteaga, S. Krishnan, N. Parthasarathy, Y. M. Kim, Y. Wu, J. M. Fastenau, W. K. Liu, and M. J. W. Rodwell, "Wideband DHBTs using a graded carbon-doped InGaAs base," *IEEE Electron Device Lett.*, vol. 24, pp. 433–435, July 2003.

[9] W. Liu, *Handbook of III–V Heterojunction Bipolar Transistors*. New York: Wiley, 1998.