UNIVERSITY OF CALIFORNIA, SAN DIEGO

Transmitter Systems and Bidirectional RF Front-End for Millimeter-Wave Communications

A dissertation submitted in partial satisfaction of the
requirements for the degree
Doctor of Philosophy

in

Electrical Engineering (Electronic Circuits and Systems)

by

Po-Yi Wu

Committee in charge:

Professor James F. Buckwalter, Chair
Professor Peter Asbeck
Professor Gert Cauwenberghs
Professor Chung-Kuan Cheng
Professor William Hodgkiss
Professor Gabriel Rebeiz

2015

The dissertation of Po-Yi Wu is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

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Chair

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DEDICATION

To my parents, Chung-Chieh Wu and Su-Feng Hong, my wife, Yi-Shan Lin, my daughter, Doreen Wu, and all of those who shared their lives with me.

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The material in this dissertation is based on the following papers which are either published, submitted, or to-be-submitted for publication. Chapter 2 is mostly a reprint of the material as it appears in IEEE Compound Semiconductor Integrated Circuit Symposium, Oct. 2013, P. Wu; J. F. Buckwalter and IEEE Transactions on Microwave Theory and Techniques, Dec. 2014, P. Wu; A. K. Gupta; J. F. Buckwalter. Chapter 3 includes a reprint of the material as it appears in International Microwave Symposium, May 2015, P. Wu; Y. Liu; B. Hanafi; H. Dabag; P. Asbeck; J. F. Buckwalter, and an updated material to be submitted for publication shortly. Chapter 4 is mostly a reprint of the material submitted to IEEE Transactions on Microwave Theory and Techniques, P. Wu; T. Kijsanayotin; J. F. Buckwalter. The dissertation author is the primary author of these materials, and co-authors have approved the use of the material for this dissertation.

Po-Yi Wu
San Diego, CA
August, 2015

VITA

2005	B. S. in Electrical Engineering, National Sun Yat-Sen University, Kaohsiung, Taiwan
2007	M. S. in Communications Engineering, National Chiao Tung University, Hsinchu, Taiwan
2015	Ph. D. Electrical Engineering (Electronic Circuits and Systems), University of California, San Diego, La Jolla, California, USA

PUBLICATIONS

P. Wu, T. Kijsanayotin, and J. F. Buckwalter, "A 71–86-GHz Bidirectional Transceiver in 90-nm SiGe BiCMOS", *submitted to IEEE Transactions on Microwave Theory and Techniques*.

P. Wu, Y. Liu, B. Hanafi, H. Dabag, P. Asbeck and J. F. Buckwalter, "A 45-GHz Si/SiGe 256-QAM Transmitter with Digital Predistortion", *IEEE International Microwave Symposium*, May 2015.

P. Wu, A. K. Gupta and J. F. Buckwalter, "A Dual-band, Millimeter-wave Direct-conversion Transmitter with Quadrature Error Correction", *IEEE Transactions on Microwave Theory and Techniques*, vol. 62, no. 12, pp. 3118-3130, December 2014.

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ABSTRACT OF THE DISSERTATION

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University of California, San Diego, 2015

Professor James F. Buckwalter, Chair

In this dissertation, millimeter-wave transmitter systems and a bidirectional transceiver front-end circuit are presented. To reach high data rate for next generation communication systems, complex modulation schemes such as QAM are necessary to take advantage of the signal bandwidth. In a transmitter system, higher-order QAM not only requires the PA to operate in linear region, while the output power and efficiency are maintained, but also requires fine calibrations for the modulator to minimize the EVM. The first portion of the dissertation presents the dual-band (Q-band/W-band) direct-conversion transmitter in 120-nm SiGe BiCMOS process. The dual-band feature is the use of the proposed transmission-line-based dual-band load on RF and LO amplifiers to allow the transmitter to

operate at two distinct bands. Furthermore, this dual-band transmitter applies a new I/Q correction techniques, which calibrates amplitude and phase mismatch from analog baseband, and can achieve the sideband suppression ratio above 40 dBc at both Q-band and W-band. The EVM improvement can be clearly found from the constellation diagram at both bands.

In addition, a high-efficiency PA must introduce nonlinear terms and degrade the EVM. Therefore, in addition to the I/Q mismatch, other errors from a transmitter such as LO leakage, AM-AM, AM-PM distortion and memory effects must be calibrated to improve the EVM. The second portion of this dissertation discusses the demonstrations of 45-GHz and 94-GHz transmitter systems with digital predistortion (DPD) to compromise the linearity/efficiency trade-off. The 45-GHz transmitter system uses the first-portion SiGe modulator and a two-by-two PA/antenna array, which PAs are implemented in 45-nm SOI CMOS process. The digital signal is programmed in an FPGA-based processor, so an all silicon-based solution is verified at 45 GHz (Q-band). The 94-GHz transmitter system uses a two-step frequency conversion architecture to send the modulated data to 94-GHz band and a two-by-four PA/antenna array, which is implemented in 45-nm SOI CMOS process. The nonlinearities and errors of the transmitted data are significantly predistorted/calibrated and the EVM is greatly improved by DPD.

The third portion of this dissertation presents a 71 to 86-GHz (E-band) bidirectional transceiver front-end circuit implemented in 90-nm SiGe BiCMOS process. The time-division duplex architecture avoids transmit/receive switches through the use of transistor biasing in the signal path to minimize high-frequency loss. The low-noise amplifier (LNA) and power amplifier (PA) are combined into a novel PA/LNA circuit, which alleviates the parasitic loading of each circuit. In transmit mode, the bidirectional transceiver transmits a maximum saturated power of 11 dBm at 78 GHz with a 3-dB bandwidth from 71 to 86 GHz. In receive mode, the maximum 30.6-dB conversion gain and the minimum 6.6-dB noise figure are measured at 73 GHz.

Chapter 1

Introduction: Silicon-based High-speed Millimeter-wave Communications

The millimeter-wave (mm-wave) spectrum offers a wide bandwidth and can enable high-data-rate wireless communications. Figure 1.1 illustrates the applications in mm-wave bands. K-band (18–27 GHz), Q-band (33–50 GHz) and W-band (75–110 GHz) are used for satellite communications and military applications [1,2]. 60-GHz unlicensed band is used for short-range high-speed area networks that have been commercialized [3, 4]. 76–77-GHz and 77–81-GHz bands are employed in automotive radar systems for long-range cruise control and short-range side-crash prevention [5]. High capacity E-band (71–76/71–76 GHz) point-to-point links enable backhaul applications [6]. The next generation (5G) systems have been explored, potentially, in mm-wave bands.

Due to the propagation loss, high output power from the transmitter and low noise figure (NF) at the receiver are required for link budgets at mm-wave bands. Traditionally, mm-wave transceiver front-end circuits were dominated by III-V-based monolithic microwave integrated circuits (MMICs) due to their higher power density and better noise performance. However, III-V semiconductor-based technologies are relatively high cost because of the low yield and the discrete implementation. In recent years, substantial performance improvement of silicon-

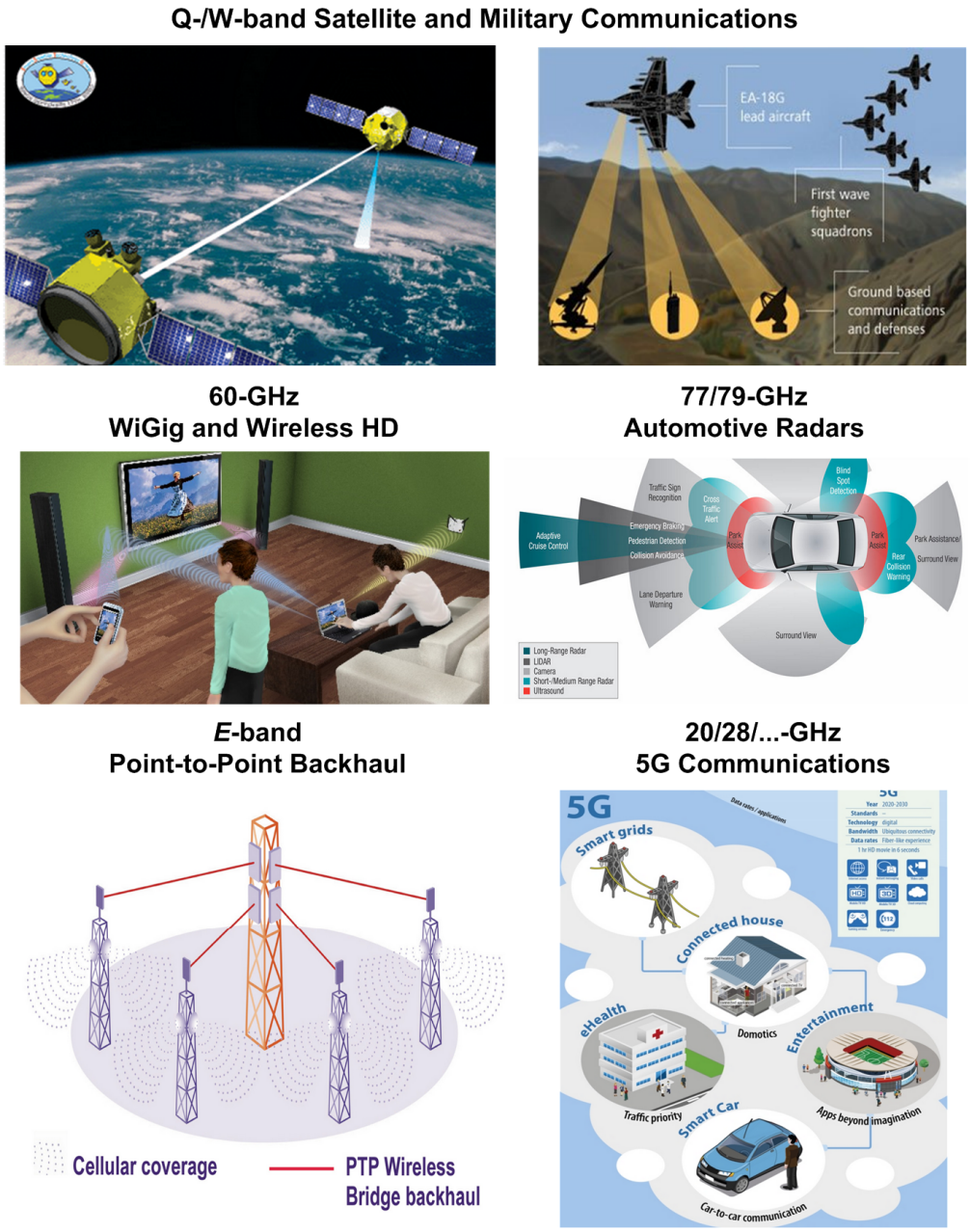


Figure 1.1: Applications of mm-wave wireless communications.

based solutions (CMOS and SiGe BiCMOS technologies) can greatly reduce cost and provide flexible platforms for system integration.

One of the challenges in the circuit implementation of a mm-wave high-speed transmitter is the linearity/efficiency trade-off. The mm-wave power amplifier (PA) achieves highest efficiency when operates at saturated power, but this also generates distortion. To reach high data rate, spectrally efficient quadrature amplitude modulation (QAM) schemes are necessary to take advantage of the bandwidth. The distortion from the PA as well as the modulator results in high error vector magnitude (EVM). In addition, due to the increased path loss and requirement of antenna beam scanning, phased-array systems are widely used based on beamforming techniques for spatial power combining and beam directivity adjustment. Multiple elements of separate transmitter, receiver and antenna occupy significant area and recent approaches have proposed bidirectional transceiver front-end circuits for single-antenna-per-element phased-array systems.

1.1 EVM Considerations for High-Order Modulation Schemes

High-data-rate communications employ spectrally efficient modulation schemes such as M-ary QAM. With the advancement of the device scaling, mm-wave transmitter circuitry including digital signal processing (DSP), analog baseband, and RF front-end can be implemented in low cost Si/SiGe processes. Device scaling introduces several circuit nonidealities such as amplifier nonlinearity, dc offset, and in-phase/quadrature (I/Q) imbalance, which result in high EVM and low reliability. Figure 1.2 plots bit error rate (BER) with respect to EVM for various M-ary QAM schemes. For a given 10^{-6} BER, 1024-QAM requires 1.2% EVM, 256-QAM requires 2.3% EVM, 64-QAM requires 4.7% EVM and 16-QAM can tolerate 9% EVM. Therefore, lower EVM is necessary to satisfy the demands for higher-order M-ary QAM.

To improve the EVM, nonlinear characteristics of the PA, e.g., amplitude compression (AM–AM) and phase compression (AM–PM), are compensated by

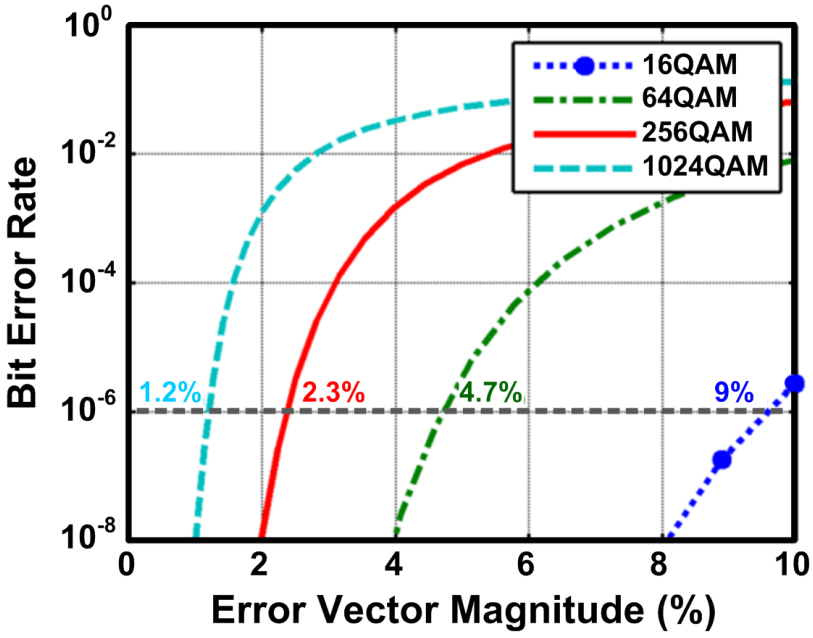


Figure 1.2: EVM requirements for various M-ary QAMs.

some well-known techniques, such as feedforward, Cartesian feedback, envelope tracking, and digital pre-distortion (DPD) [7]. If the PA nonlinear characteristics are known, DPD is preferable due to the DSP capabilities on-chip. I/Q imbalance and dc offset issues can also be modeled and calibrated by the DPD processor [8]. However, high resolution digital-to-analog converters (DACs) are needed for DPD and digital calibration, especially for high-order M-ary QAM, due to the low quantization error. For instance, while two 3-bit DACs are needed to generate a 64-QAM constellation, 6–8-bit DACs are usually required to compensate the PA nonlinearity. Digitally calibrating the dc offset and I/Q imbalances motivates even higher resolution DACs, e.g., 12-bit DACs [9]. Each additional bit of DAC resolution introduces a power/speed trade-off. Larger current sources/sinks result in larger parasitic capacitance and the current flowing through the switches must be increased to maintain the switching time. In addition, the most significant bits (MSBs) have to be thermometer coded to minimize device mismatch. These issues suggest that a high resolution DAC tends to consume more power and area. Therefore, it is desirable to correct for the dc offset and I/Q mismatch through

a static correction circuitry instead of through the high-speed baseband DACs. Analog dc offset cancellation techniques such as ac coupling, feedforward, and dc feedback are widely used in circuit design [10, 11]. A novel static quadrature error correction technique employed in an I/Q modulator will be discussed in this dissertation. The mm-wave transmitter systems utilizing DPD to compromise the linearity/efficiency trade-off will also be presented.

1.2 Bidirectional Transceivers for Phased-Array Systems

A wideband transceiver RF front-end circuit is presented for backhaul applications in *E*-band (71–76/81–86 GHz), long-range cruise control automotive radars in 76–77 GHz and short-range side-crash prevention radars in 77–81 GHz. This dissertation investigates the design of a switchless, asymmetric bidirectional transceiver front-end element for phased-array systems that could be incorporated into an IF phase-shifting phased array. In medium or long-range applications, a beamforming antenna array is required for high directivity [12, 13]. Previous phased-array works have demonstrated either in receiver arrays [14–16] or in transmit arrays [12,17,18]. Half-duplex systems such as time-division duplexing (TDD) communications and radar systems allow the transmitter and receiver to share a single antenna element and make compact bidirectional transceivers attractive in terms of area and cost. Separate transmit/receive arrays double the required silicon area. Therefore, bidirectional transceiver elements have been proposed at 45-GHz [19] and 60-GHz bands [20], however, no bidirectional transceivers have been demonstrated at *E*-band to the author's knowledge.

In a bidirectional transceiver front-end, the low-noise amplifier (LNA) and PA cannot be isolated with CMOS switches due to the poor performance of the NMOS switch at *E*-band. Consequently, this work seeks to develop the switchless bidirectional interconnection of the PA and LNA. Moreover, in an IF phased-array system, the power division occurs at the IF path in transmit mode and splits the power between each of the PAs requiring additional gain. In receive mode, a

passive mixer is desirable for higher linearity before combining the signal at the IF band. Therefore, an asymmetric bidirectional mixer is also demonstrated.

1.3 Dissertation Organization

Background material, system and design considerations, previous works and motivations have been introduced in Chapter 1.

Chapter 2 presents circuit techniques to correct amplitude and phase mismatch in a dual-band transmitter. The quadrature error impairment on EVM and sideband suppression ratio (SSR) is analyzed and a novel static I/Q correction circuitry is proposed. A transmission-line-based dual-band high-impedance load for the pre-PA amplifiers and the local oscillator (LO) drivers is also introduced in this chapter. The Q-band/W-band dual-band transmitter is implemented in 120-nm SiGe BiCMOS process. The transmitter architecture and the design of each building block are described. The measurement setup and results are included. Finally, the measured EVM and SSR improvements with the aid of the proposed I/Q correction technique are demonstrated.

Chapter 3 firstly discusses the circuit nonidealities and mismatch contributions to the EVM. In the 45-GHz transmitter system demonstration, the I/Q modulator presented in Chapter 2 and the two-by-two PA/antenna array in [21] are employed. The DPD algorithm for I/Q baseband data is programmed by an FPGA-based DSP in this experiment. The chip-on-board assemblies and the measurement setup details are also included. Furthermore, the 94-GHz transmitter system utilizing DPD is also presented. A two-step frequency conversion architecture, where the first LO is at 21 GHz and the second LO is at 75 GHz, and the two-by-four PA/antenna array in [2] are employed in this experiment. Both the 45 and 94-GHz transmitter systems demonstrate the EVM and adjacent channel power ratio (ACPR) improvements with 256-QAM scheme utilizing DPD.

In Chapter 4, a fully integrated 71–86-GHz, switchless, asymmetric bidirectional transceiver front-end is demonstrated in 90-nm SiGe BiCMOS process. The LNA and PA are combined into a novel PA/LNA circuit, which alleviates the

parasitic loading of each circuit. The TDD architecture avoids transmit/receive switches through the use of transistor biasing in the signal path to minimize high-frequency loss. The system considerations are described and motivation for the proposed transceiver architecture is discussed. The circuit implementations and the design details of each building block are presented. The transmit-mode and receive-mode measurement setup and results are also reported.

This dissertation concludes the novel features of these works in Chapter 5.

Chapter 2

A Dual-Band Millimeter-Wave Direct-Conversion Transmitter with Quadrature Error Correction

2.1 Quadrature Error

Amplitude and phase imbalance arises from the practical realization of an I/Q modulator. For instance, a polyphase filter balances I/Q amplitude only at one frequency. Using transmission-line-based hybrid couplers extends the bandwidth, however, the amplitude mismatch is unavoidable due to the loss between coupler ports. The imbalanced I/Q LO signals are expressed as $(1+\alpha/2)\cos(\omega_{LO}t+\theta/2)$ and $(1-\alpha/2)\sin(\omega_{LO}t-\theta/2)$, respectively, where the amplitude imbalance is α and phase imbalance is θ. By mixing with I/Q baseband information (I_{in}, Q_{in}), the RF output of the modulator is

$$\begin{aligned} V_{RF} &= I_{in}\left(1+\tfrac{\alpha}{2}\right)\cos\left(\omega_{LO}t+\tfrac{\theta}{2}\right)+Q_{in}\left(1-\tfrac{\alpha}{2}\right)\sin\left(\omega_{LO}t-\tfrac{\theta}{2}\right) \\ &= I_{qm}\cos(\omega_{LO}t)+Q_{qm}\sin(\omega_{LO}t) \end{aligned}, \tag{2.1}$$

where

$$\begin{aligned} I_{qm} &= I_{in}\left(1+\tfrac{\alpha}{2}\right)\cos\left(\tfrac{\theta}{2}\right)-Q_{in}\left(1-\tfrac{\alpha}{2}\right)\sin\left(\tfrac{\theta}{2}\right) \\ &= M_{II}I_{in}+M_{IQ}Q_{in} \end{aligned} \tag{2.2}$$

$$\begin{aligned} Q_{qm} &= -I_{in}\left(1+\tfrac{\alpha}{2}\right)\sin\left(\tfrac{\theta}{2}\right) + Q_{in}\left(1-\tfrac{\alpha}{2}\right)\cos\left(\tfrac{\theta}{2}\right) \\ &= M_{QI}I_{in} + M_{QQ}Q_{in} \end{aligned} . \tag{2.3}$$

Equations (2.1)–(2.3) indicate that the LO quadrature mismatch is a linear combination of the I and Q information, which makes it possible to correct the I/Q imbalance.

In a digital communication system, the EVM represents the fidelity of the digital signals. Give a reference signal expressed as [22]

$$\mathrm{S_{ref}} = G\left(I_{in} + jQ_{in}\right), \tag{2.4}$$

the transmitted signal in the presence of amplitude and phase imbalance is

$$\mathrm{S_{env}} = G\left[\left(1+\frac{\alpha}{2}\right)e^{j\frac{\theta}{2}}I_{in} + j\left(1-\frac{\alpha}{2}\right)e^{-j\frac{\theta}{2}}Q_{in}\right] \tag{2.5}$$

where G is the gain from analog baseband input to the RF output. Under small I/Q mismatch circumstances, i.e., $\alpha \ll 1$ and $\theta \to 0$, the EVM is approximated as

$$\mathrm{EVM} \approx \sqrt{\left(\frac{\alpha}{2}\right)^2 + \left(\frac{\theta}{2}\right)^2}. \tag{2.6}$$

Figure 2.1 illustrates how the amplitude and phase mismatch impacts the EVM. A quadrature phase-shift keying (QPSK) constellation becomes a rectangle instead of a square as shown in Fig. 2.1(a), in the presence of amplitude mismatch. On the other hand, the constellation becomes a parallelogram, as shown in Fig. 2.1(b), in the presence of phase mismatch θ.

To evaluate the EVM from a single tone measurement, the sideband suppression ratio (SSR) is an adequate representation for the EVM. By applying quadrature sinusoidal signals at baseband, i.e., $I_{in} = \cos\left(\omega_{IF}t\right)$ and $Q_{in} = \sin\left(\omega_{IF}t\right)$, either the upper sideband (USB) (i.e., $\omega_{LO} + \omega_{IF}$) or lower sideband (LSB) (i.e., $\omega_{LO} - \omega_{IF}$) tone appears at the modulator output spectrum. The SSR is defined as the amplitude ratio of the desired signal to image signal. By calculating the USB and LSB signals from (2.1), the SSR is

$$SSR = \frac{\text{Desired Signal}}{\text{Image Signal}} = \frac{\sqrt{\cos^2\left(\frac{\theta}{2}\right) + \left(\frac{\alpha}{2}\right)^2\sin^2\left(\frac{\theta}{2}\right)}}{\sqrt{\left(\frac{\alpha}{2}\right)^2\cos^2\left(\frac{\theta}{2}\right) + \sin^2\left(\frac{\theta}{2}\right)}}. \tag{2.7}$$

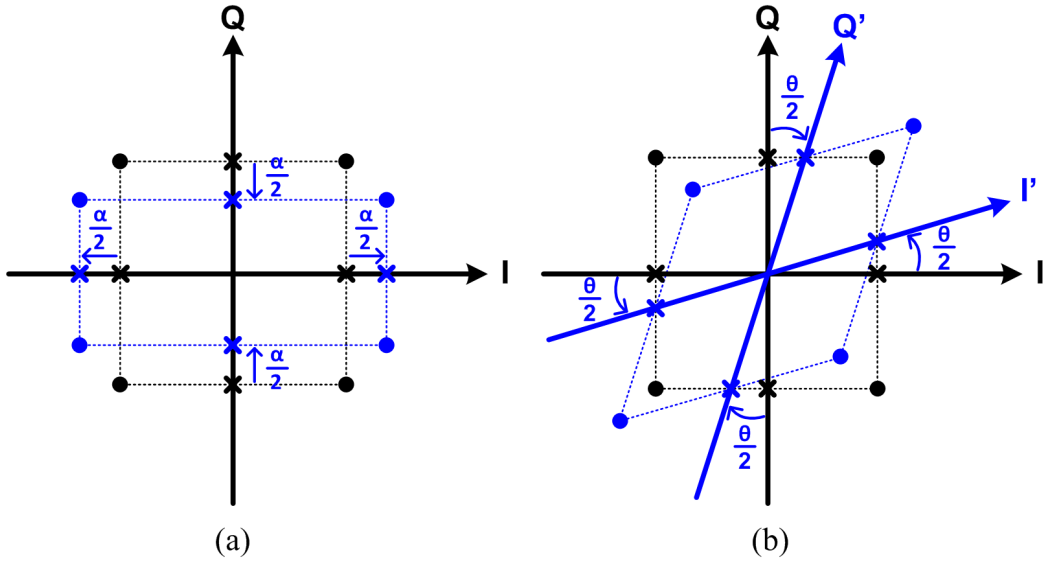


Figure 2.1: Constellation twist due to (a) amplitude and (b) phase mismatch.

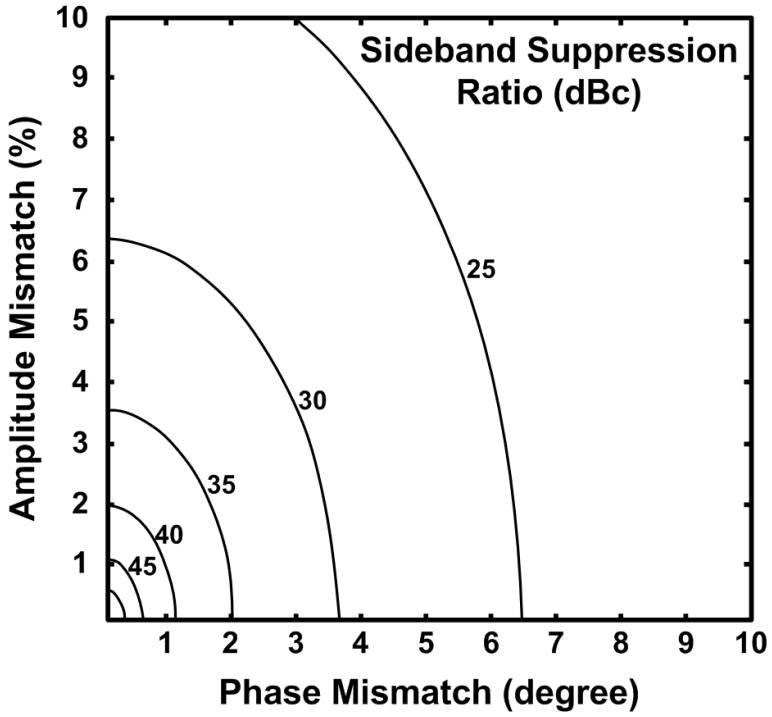


Figure 2.2: Simulated SSR contour versus amplitude and phase imbalances.

Equation (2.7) can be further decomposed into the SSR due to amplitude mismatch, $SSR|_{amp} = 2/\alpha$, and the SSR due to phase mismatch, $SSR|_{phase} = \cos\left(\frac{\theta}{2}\right) / \sin\left(\frac{\theta}{2}\right)$. The SSR contour is plotted versus α and θ as shown in Fig. 2.2. If the amplitude and phase imbalance is to contribute less than 1% EVM, α and θ must less than 2% (0.2 dB) and 1°, respectively. As a result, the required SSR should be less than 37.5 dB.

2.2 Quadrature Error Correction

To compensate the quadrature errors, (2.2) and (2.3) are expressed in matrix form [23]

$$\begin{bmatrix} I_{qm} \\ Q_{qm} \end{bmatrix} = M \begin{bmatrix} I_{in} \\ Q_{in} \end{bmatrix} \tag{2.8}$$

where

$$M = \begin{bmatrix} \left(1+\frac{\alpha}{2}\right)\cos\left(\frac{\theta}{2}\right) & -\left(1-\frac{\alpha}{2}\right)\sin\left(\frac{\theta}{2}\right) \\ -\left(1+\frac{\alpha}{2}\right)\sin\left(\frac{\theta}{2}\right) & \left(1-\frac{\alpha}{2}\right)\cos\left(\frac{\theta}{2}\right)) \end{bmatrix}. \tag{2.9}$$

Again, α is the total amplitude error and θ is the phase mismatch. To calibrate the errors, the raw I/Q data can be multiplied by the inverse matrix

$$M^{-1} = \frac{1}{\Delta}. \begin{bmatrix} \left(1-\frac{\alpha}{2}\right) & \left(1-\frac{\alpha}{2}\right)\tan\left(\frac{\theta}{2}\right) \\ \left(1+\frac{\alpha}{2}\right)\tan\left(\frac{\theta}{2}\right) & \left(1+\frac{\alpha}{2}\right) \end{bmatrix} \tag{2.10}$$

where $\Delta = \left(1+\frac{\alpha}{2}\right)\left(1-\frac{\alpha}{2}\right)\cos(\theta) / \cos\left(\frac{\theta}{2}\right)$. Under small I/Q mismatch circumstances, the inverse matrix can be simplified as

$$M^{-1} \approx \begin{bmatrix} \left(1-\frac{\alpha}{2}\right) & \frac{\theta}{2} \\ \frac{\theta}{2} & \left(1+\frac{\alpha}{2}\right) \end{bmatrix}. \tag{2.11}$$

The matrix described in (2.11) can be implemented with the block diagram shown in Fig. 2.3, comprising four variable gain amplifiers (VGA) with gains of G_{II}, G_{IQ}, G_{QI} and G_{QQ}, respectively. When I and Q channels are perfectly matched, the four correction VGAs are all turned off. If there is amplitude mismatch, G_{II} or G_{QQ} are turned on to adjust the amplitude of I or Q channel as the waveform shown in Fig. 2.4(a). For instance, if Q channel has greater amplitude

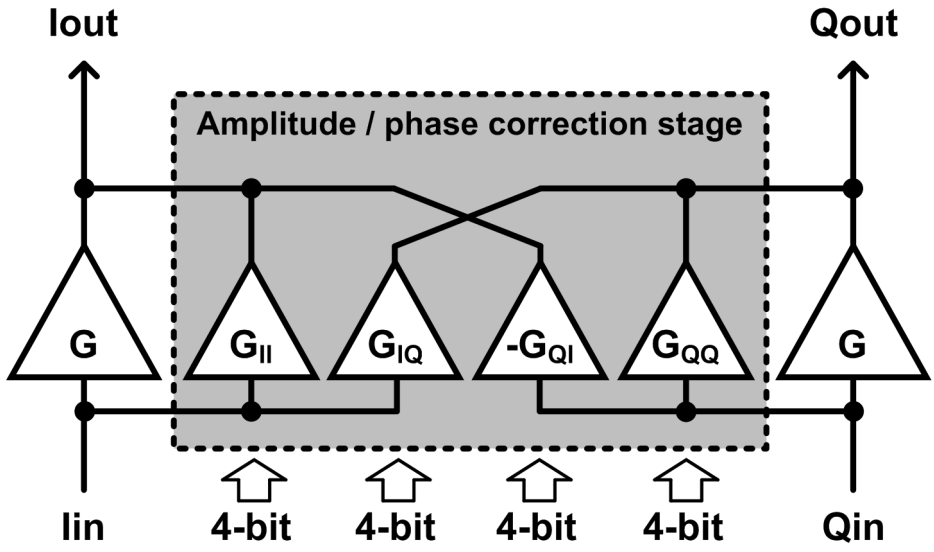


Figure 2.3: Block diagram of the I/Q imbalance correction stage.

then I channel, G_{II} turns on and the remaining correction VGAs are still off. The I/Q outputs are expressed as

$$I_{out} = (G + G_{II}) \cos \omega t \tag{2.12}$$

$$Q_{out} = G\,(1 + \alpha) \sin \omega t. \tag{2.13}$$

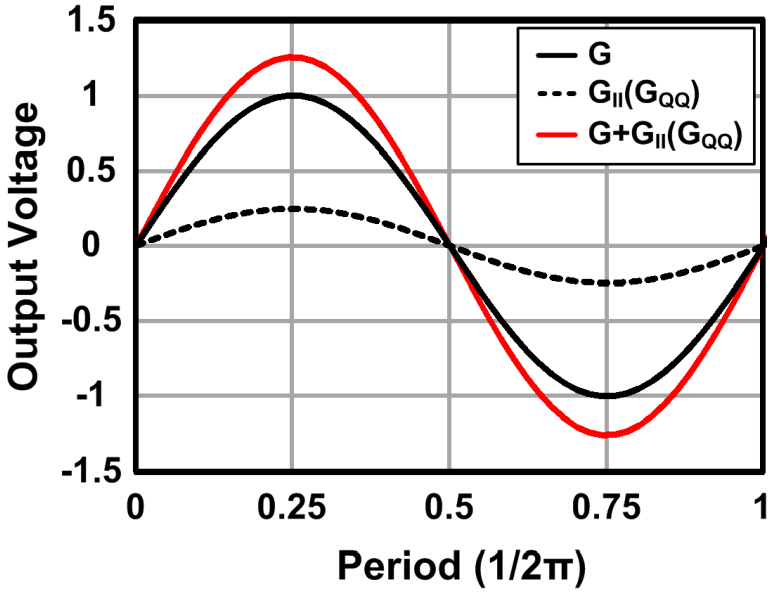
By choosing $G_{II}/G = \alpha$, the amplitude of the I/Q paths can be equalized.

On the other hand, G_{IQ} and G_{QI} correct the phase mismatch between I/Q channel as the waveform shown in Fig. 2.4(b). For example, turning on G_{QI} and keeping the remaining correction amplifiers off makes the I/Q output as

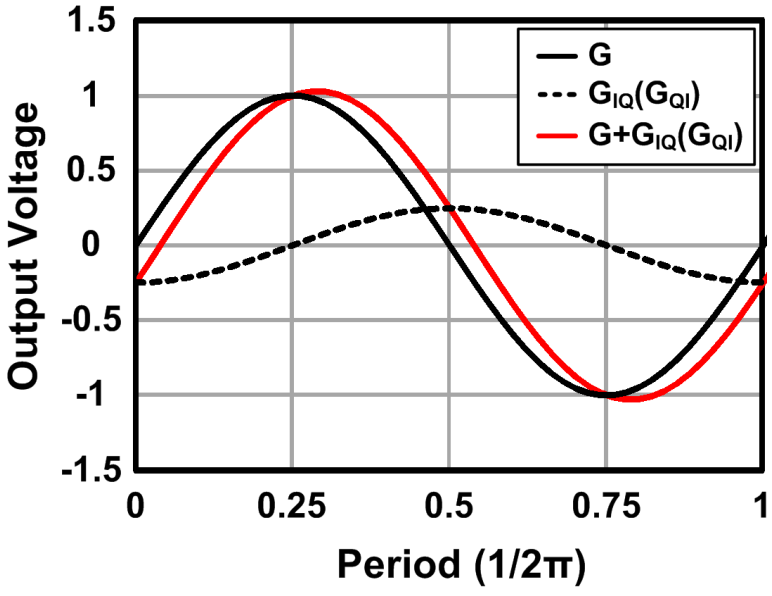
$$I_{out} = G \cos(\omega t + \theta) + G_{QI} \sin \omega t \tag{2.14}$$

$$Q_{out} = G \sin \omega t. \tag{2.15}$$

If I_{out} is to be $G \cos \omega t$, the phase mismatch must be $G_{QI}/G \approx \theta$, where θ is assumed to be small. Note that the input impedance of the VGAs is high regardless of whether the VGAs are on or off. This implies that the amplitude and phase mismatch can be corrected independently.



(a)



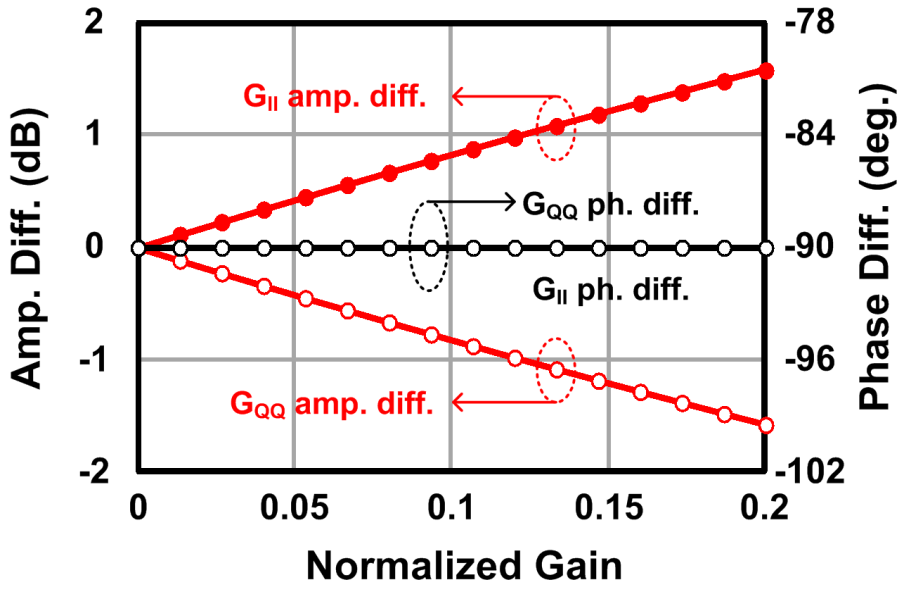
(b)

Figure 2.4: Waveform of the (a) amplitude and (b) phase correction stages.

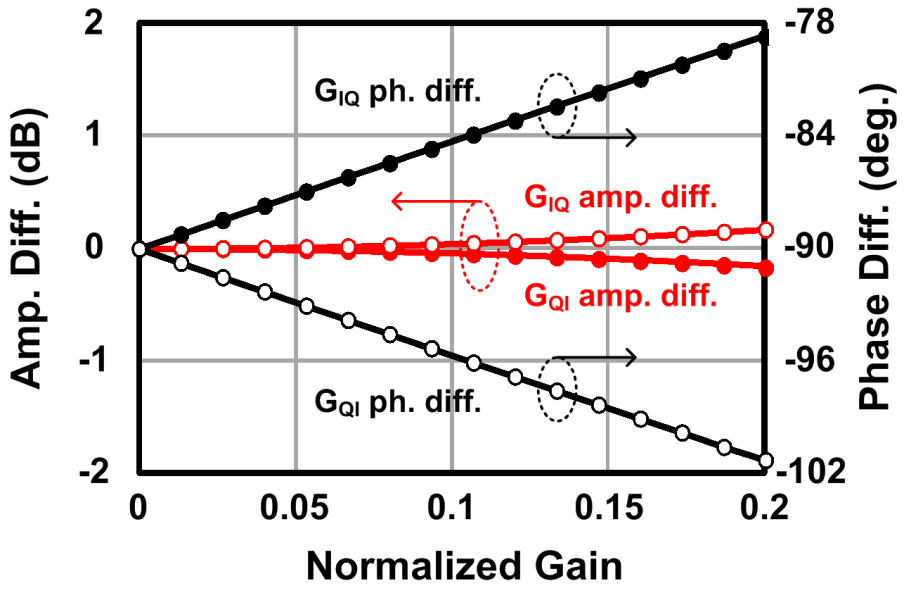
Process variation and device mismatch suggest that the maximum gain error is around 20% (1.6 dB) and the maximum phase mismatch is 10°. As a result, the gain of each VGA, i.e., G_{II}, G_{IQ}, G_{QI} and G_{QQ}, should be designed at least $0.2G$ and controlled by 4 bits of precision. Figure 2.5(a) plots the amplitude and phase differences through 4-bit control of gains G_{II} and G_{QQ}. The amplitude difference is adjustable up to 1.6 dB with 0.2-dB resolution while the phase difference is constant. Figure 2.5(b) indicates the amplitude and phase differences through 4-bit control of gains G_{IQ} and G_{QI}. The phase difference can be changed up to 10° with 1° resolution while the amplitude difference is negligible. This amplitude error could be further calibrated through G_{II} or G_{QQ} if necessary. Note that the I/Q correction is applied through a separate digital control word and not in conjunction with I/Q data.

2.3 Dual-Band Load Design

Another feature of the proposed work is the use of a dual-band load to allow the transceiver to operate at two distinct bands. The proposed transmission-line-based dual-band load provides high impedance at two *arbitrary* frequencies, f_1 and f_2, and is used to load the pre-amplifiers and the LO driving amplifiers. Figure 2.6 shows the concept of the proposed dual-band load. It is composed of three transmission line sections – TL_1, TL_2 and TL_3 – with lengths of L_1, L_2 and L_3, respectively [24, 25]. The high-impedance Z_L at the two frequencies is provided by the combination of $TL_3 + TL_1$ or $TL_3 + TL_2$ with short terminations along each route. L_1 and L_2 are chosen to be quarter-wavelength at two frequencies, i.e., $L_1 = \lambda_1/4$ and $L_2 = \lambda_2/4$, where λ_1 and λ_2 are the wavelength of transmission lines at the frequency of f_1 and f_2, respectively. At f_1, the impedance looking into TL_1 is infinite and only TL_2 and TL_3 need to be taken into account. On the other hand, at f_2, the impedance looking into TL_2 is infinite, thus only TL_1 and TL_3 need to be considered. In these two cases, the following two equations can be written assuming the transmission lines are lossless for simplicity:



(a)



(b)

Figure 2.5: Simulated I/Q mismatch by turning on: (a) amplitude and (b) phase correction amplifiers.

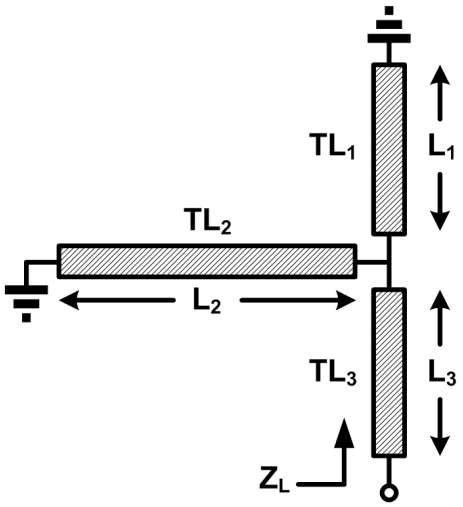


Figure 2.6: Proposed dual-band load concept.

$$\beta_1(L_2 + L_3) = \frac{\pi}{2} + m\pi \tag{2.16}$$

$$\beta_2(L_1 + L_3) = \frac{\pi}{2} + n\pi \tag{2.17}$$

where β_1 and β_2 are the phase constants at f_1 and f_2, respectively, and m and n can be zero or any positive integers. Considering the ratio of f_1 and f_2 is r, i.e., $f_1 = r \cdot f_2$, then $L_2 = r \cdot L_1$ and $\beta_1 = r \cdot \beta_2$. Subtracting (2.17) from (2.16), m and n can be determined based on the ratio r:

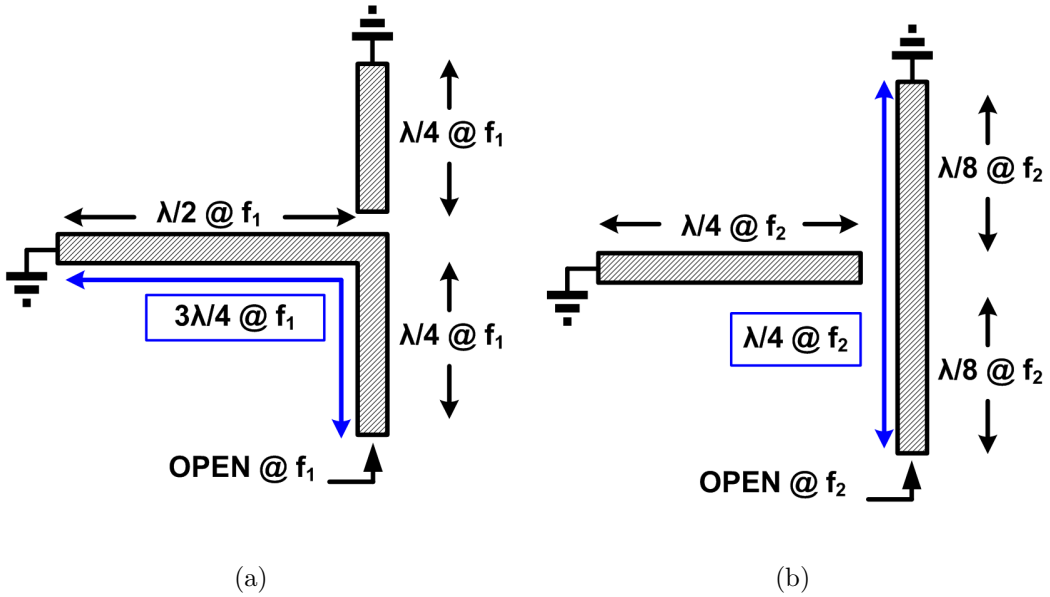
$$n = \frac{m + 1 - r}{r}. \tag{2.18}$$

By summing (2.16) and (2.17), L_3 can be found as

$$L_3 = (nr + m) \cdot \frac{\lambda_1}{4} = (nr + m) \cdot L_1. \tag{2.19}$$

Note that L_2 and L_3 are in terms of L_1. This is realized by changing the intersection point of TL_2 between TL_1 and TL_3.

In this work, the dual-band load is designed to provide a high impedance at $f_2 = 45$ GHz (Q-band) and $f_1 = 90$ GHz (W-band), which are a factor of two apart, i.e., $r = 2$. From (2.18), $m = 1$ and $n = 0$ can be chosen for minimizing the



(a) (b)

Figure 2.7: Dual-band load operating at: (a) f_1 and (b) $f_2 = \frac{1}{2}f_1$.

length of transmission lines. At f_1, the length of the three transmission lines are found from (2.19) as illustrated in Fig. 2.7(a). The impedance seen from TL_1 is neglected and the final load impedance is the combination of TL_2 and TL_3, i.e., $L_2 + L_3 = 3\lambda_1/4$. Therefore, high impedance is provided at f_1. Since f_1 is two times of f_2, λ_1 is half of λ_2 and the length of the three transmission lines at f_2 is $L_1 = \frac{\lambda_1}{4} = \frac{\lambda_2}{8}$, $L_2 = \frac{\lambda_1}{2} = \frac{\lambda_2}{4}$, $L_3 = \frac{\lambda_1}{4} = \frac{\lambda_2}{8}$ as illustrated in Fig. 2.7(b). The impedance seen from TL_2 can be neglected and the final load impedance is the combination of TL_1 and TL_3, i.e., $L_1 + L_3 = \lambda_2/4$ and high impedance is seen at f_2. Note that r does not have to be greater than one. If the two frequencies separated by a factor of two, we arrive at the same design variables whether r is 2 or 0.5. Figure 2.8 plots the design variables of three transmission lines for different frequency ratio where the red dots indicate the minimum length of the transmission lines.

Since $\lambda/4$ transmission lines occupy a significant area, a compact meandered transmission line is proposed as shown in Fig. 2.9(a). TL_1 and TL_2 share the ground terminal. Adjacent transmission line coupling and substrate loss is mitigated with a grounded coplanar waveguide (GCPW) structure. The length of

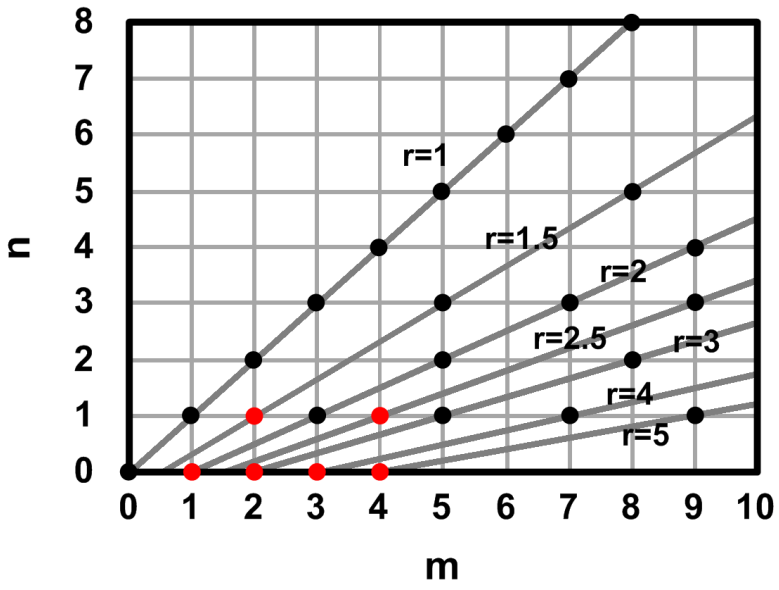
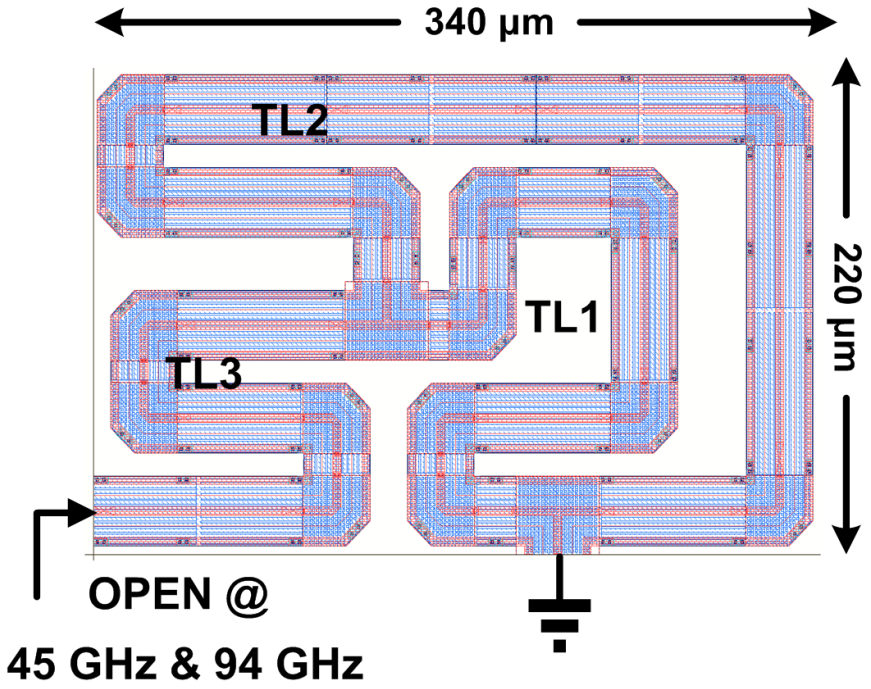
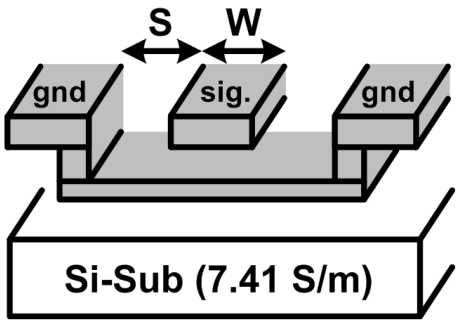


Figure 2.8: The dual-band load design variables.

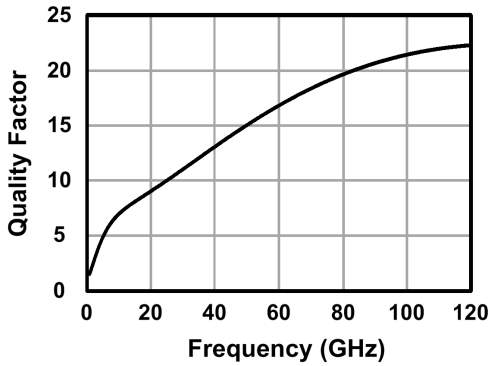
the $\lambda/4$ is around 800 μm at 45 GHz (f_o) and 400 μm at 94 GHz ($2f_o$) given $\varepsilon_{SiO2} \sim 4.2$. Figure 2.9(b) is the cross-section view of the GCPW. In 0.12-μm SiGe BiCMOS process, a seven-layer metal option had been chosen in this design. The top layer metal is a 4-μm-thick aluminum used for signal traces and the sided ground plane. The bottom ground plane is implemented on a 1.25-μm-thick copper and connects to the sided ground plane through vias. In this design, the signal traces have width of 4 μm and spacing to the sided ground plane of 10 μm. The characteristic impedance (Z_o) of the designed GCPW structure is 58 Ω. The quality factor of the designed GCPW is 14 at 45 GHz and 21 at 94 GHz as plotted in Fig. 2.9(c). The impedance provided by the dual-band load has a 3-dB bandwidth of 3.2 GHz at 45 GHz and 4.2 GHz at 94 GHz. Simulations verify the high impedance, as shown in Fig. 2.10. For a lossless dual-band load, an ideal transmission line produces an impedance transformation from the ac ground to an infinite impedance irrespective of Z_o. However, the characteristic impedance does have an impact for lossy transmission lines. The short-terminated quarter-wavelength transmission lines with higher Z_o give higher load impedance



(a)



(b)



(c)

Figure 2.9: Dual-band load. (a) Layout. (b) GCPW cross-section view. (c) Quality factor simulation.

since $Z_L = Z_o \tanh \beta l$. The simulation results in Fig. 2.10 show the Z_L of the dual-band load implemented with characteristic impedances of 40, 49, and 58 Ω, where the length of the transmission line sections is fixed.

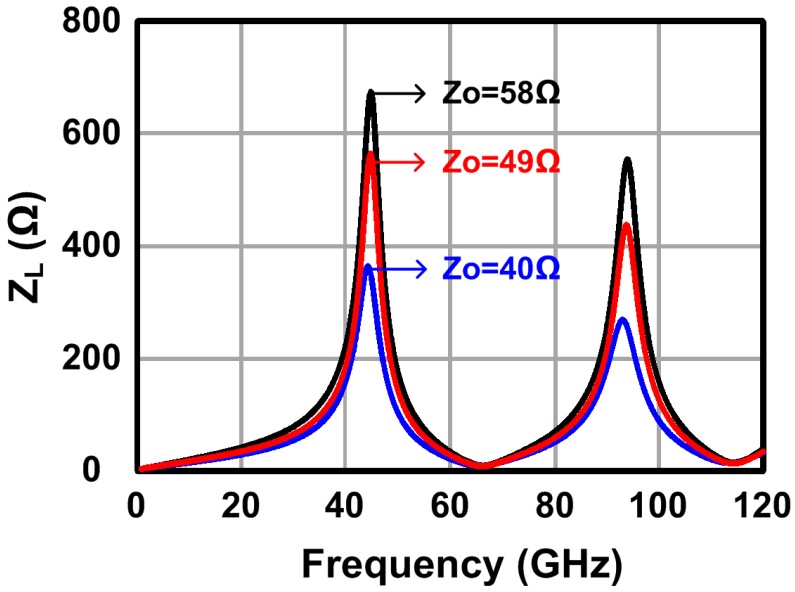


Figure 2.10: Simulated dual-band load impedance for various Z_o of transmission lines.

2.4 Dual-Band Transmitter Architecture and Design

Figure 3.3 shows the block diagram of the Q-/W-band dual-band transmitter [25]. Complex I/Q digital data are converted to analog signals by I/Q DACs. The resolution of the DAC determines the signal-to-noise ratio (SNR), where the noise includes the quantization noise and the integral nonlinearity (INL). The quantization noise is a periodic sawtooth waveform having a peak-to-peak value of 1 least significant bit (LSB). For an INL = 0.5LSB, SNR can be written as

$$\mathrm{SNR(dB)} = 6.02\,(N-1) + 1.76 \tag{2.20}$$

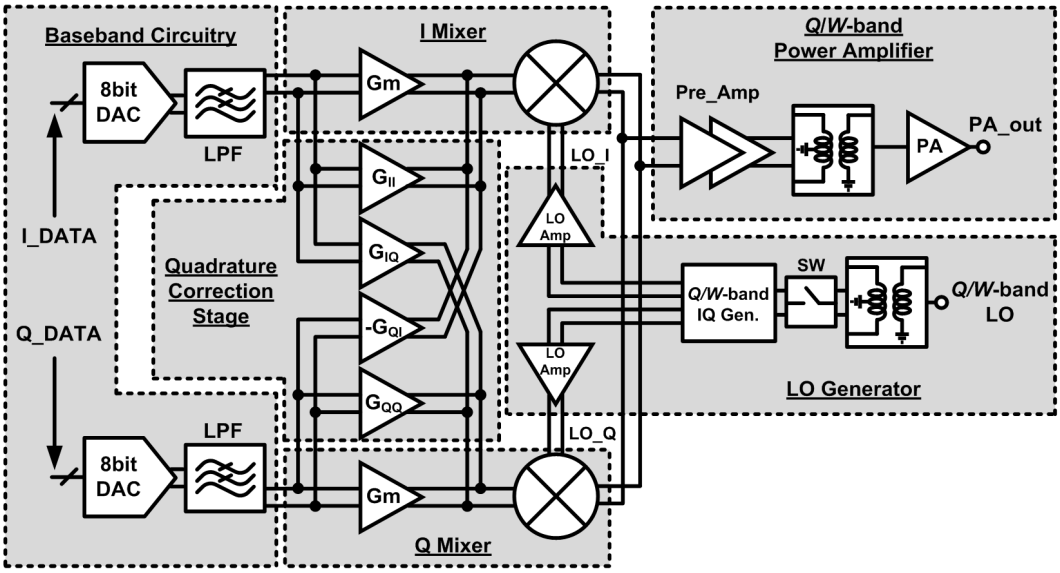


Figure 2.11: System block diagram of the dual-band transmitter.

where N is the DAC resolution, and the EVM is expressed as [9]

$$\mathrm{EVM_{SNR}} = \frac{1}{10^{\mathrm{SNR(dB)}/20}} \times 100\%. \tag{2.21}$$

As a result, a 7-bit DAC is enough to achieve less than 1% EVM. In order to compensate the nonlinearity, 8-bit DACs are implemented in this work.

The baseband signal is filtered with a low-pass reconstruction filter to reduce the high-frequency noise and clock spurs. To handle DPD, the I/Q channels must support three times the signal bandwidth to compensate at the very least the third-order nonlinearity causing compression. For a 20-MHz signal bandwidth, the filter cutoff frequency is chosen to be 60 MHz in this paper. The use of a 300-MHz DAC sampling rate along with the filter is used to oversample the input data. Oversampling helps to filter the signal copies at clock harmonics better. To limit the signal aliases below –40 dBc, third-order low-pass filters are adopted in this work.

The I/Q baseband signals are then directly up-converted to a mm-wave band by active double-balanced Gilbert mixers with the proposed I/Q quadrature correction stage. The dual-band I/Q LO signals are generated by two polyphase

filters that work at 45 GHz and 94 GHz, respectively, with switches for minimizing the interference, and then amplified by dual-band LO driving amplifiers. The up-converted mm-wave signal is amplified by the dual-band PA. The detail schematic of each building block will be shown and described in Section 2.4.1 through 2.4.5.

2.4.1 D/A Converter Design

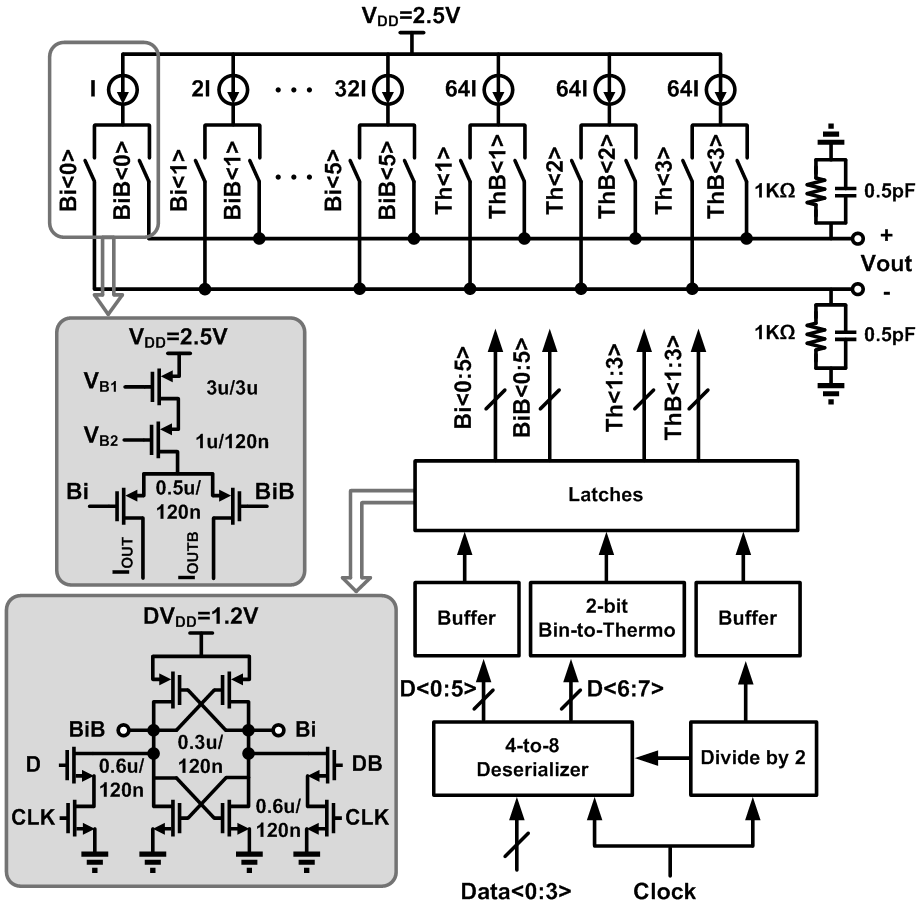


Figure 2.12: 8-bit DAC circuit diagram.

Figure 2.12 shows the block diagram of the 8-bit current-steering DAC [26]. A 300-Mb/s 4-to-8 deserializer is used at the input to reduce the pad frame. The data are demultiplexed to a parallel bus with shift registers and the divided input clock. The six LSBs directly switch six binary-weighted LSB current sources while

the two MSBs are decoded to a thermometer code to switch three MSB current sources for the purpose of transistors matching. The static performances of a current-steering DAC, i.e., INL and DNL, depend on how well the current sources are matched. For 8-bit resolution, the standard deviation of the current mismatch for an INL < 0.5LSB is under 1% for 99.7% yield [27, 28].

A cascode PMOS current source is used for increasing the output impedance. The PMOS transistor requires higher V_{SG} and is less sensitive to device threshold mismatch for a given current. For 1-μA LSB current, the DAC full scale current is 255 μA from a 2.5-V supply and operates at a sampling rate of 150 MHz to oversample the transmitted symbols. A differential 2-kΩ load resistor provides a 510-mV differential full-scale voltage swing at the DAC output. The load resistor and a differential 0.25-pF load capacitor form a single pole RC low-pass filter for pre-suppressing the signal aliases and clock spurs.

2.4.2 Filter Design

High-order baseband filters are necessary to suppress the clock spurs and signal aliases. Passive filters have high linearity and no power consumption but are hard to be implemented on chip due to area limitations. Therefore, an active $Gm - C$ filter is chosen with a third-order roll off , i.e. –60 dB/decade, and a cutoff frequency of 60 MHz. Figure 2.13 shows the equivalent model and the circuit diagram of the implemented filter. The design methodology can be found from [29, 30]. With a 150 MHz DAC sampling rate, the third harmonic of the clock spur can be suppressed below –46 dBc from simulation. The full-scale output swing can achieve differential V_p =700 mV from simulation as well as measurement. The circuit schematic of the Gm cells is also presented in Fig. 2.13. The source degeneration resistors at the source of the PMOS input pairs are used to improve the linearity. A common-mode feedback circuit is used to set the dc bias. With a 2.5-V supply, the filter consumes 38.5-mW power.

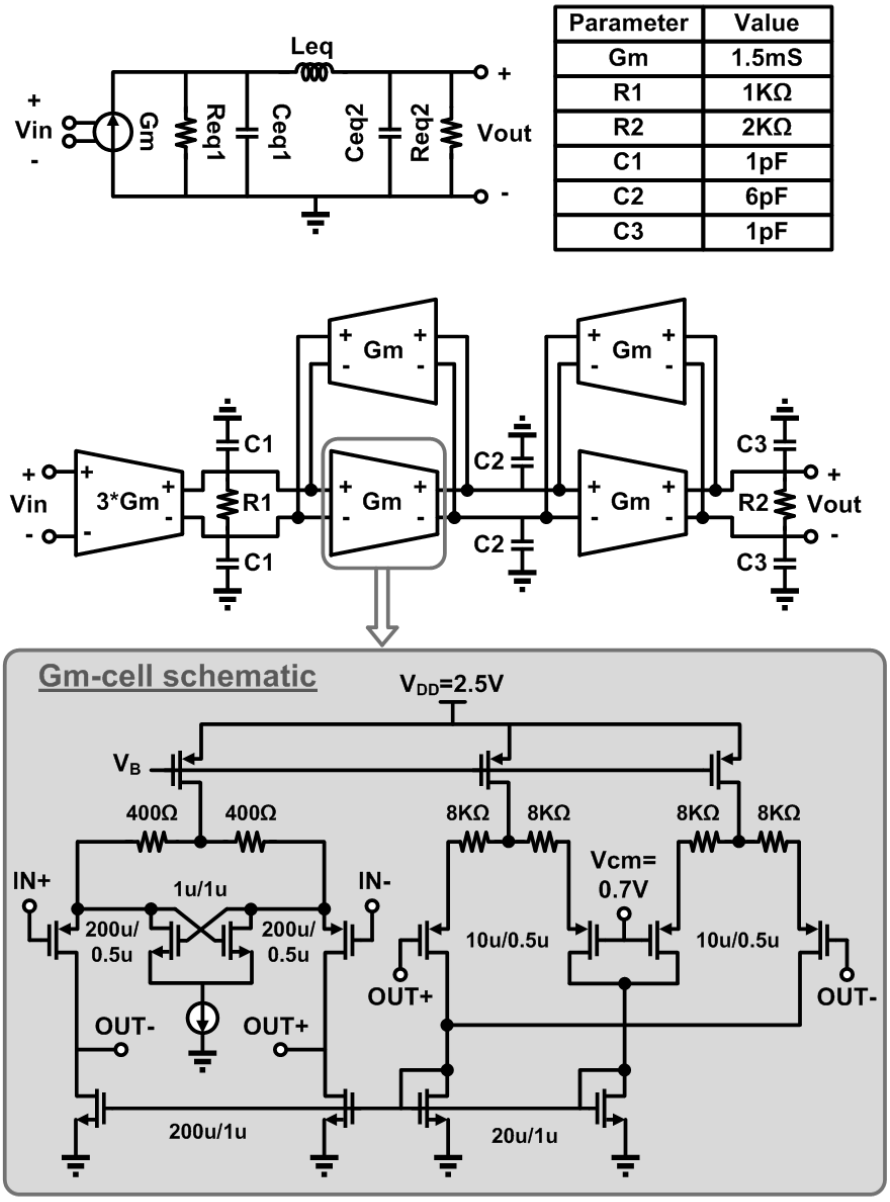


Figure 2.13: Third-order active $Gm - C$ filter.

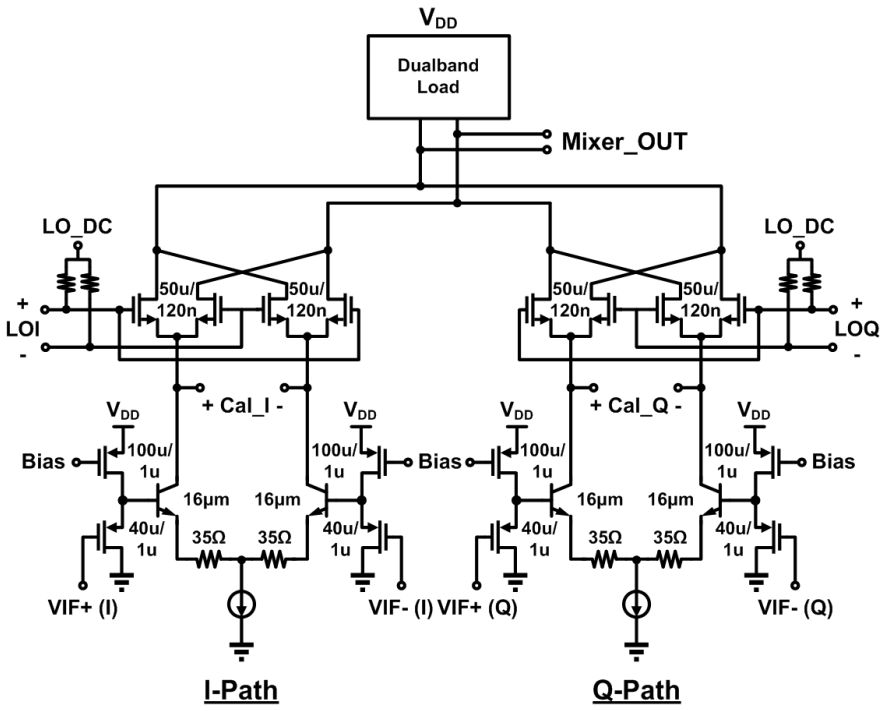


Figure 2.14: Schematic of the I/Q dual-band modulator.

2.4.3 Modulator and I/Q Corrector Design

A double-balanced Gilbert cell mixer with dual-band loads is implemented to up-convert the baseband signal to 45 or 94 GHz. The detail schematic is shown in Fig. 2.14. The transconductor pair is designed with HBT with resistive degeneration for better linearity. HBTs have higher transconductance than MOSFETs for the same biasing current. The third-order harmonic term is reduced by a factor of $(1 + g_{m1}R_E)^4$ where g_{m1} is transconductance at fundamental tone and R_E is the emitter degeneration resistance. Therefore, emitter degeneration of an HBT achieves better linearity than a source degenerated MOSFET for a given power consumption. Due to the non-zero HBT base current, a PMOS source follower is added to make the reconstruction filter see a high impedance at the load. The LO switches are implemented in NMOS because MOSFETs provide better linearity than HBT even if they require higher LO power. The I/Q up-converted signals are summed in terms of current and then converted to voltage by the dual-band

loads. The simulation shows the mixer achieves a conversion loss of 5 dB and output referred 1-dB compression point (OP_{1dB}) of –3 dBm at 45 GHz and 10-dB conversion loss with –9-dBm OP_{1dB} at 94 GHz given a 5-dBm LO power. The I/Q mixer consumes 30-mA current from a 2.5-V supply.

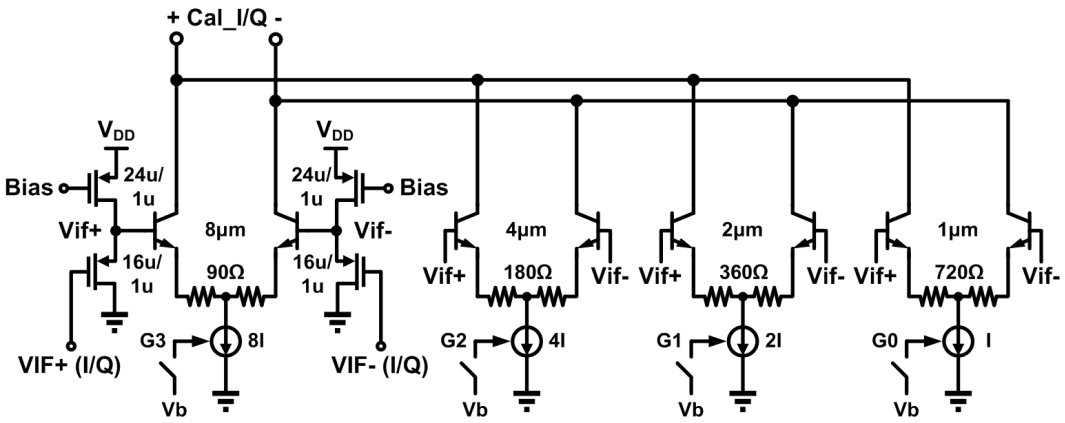
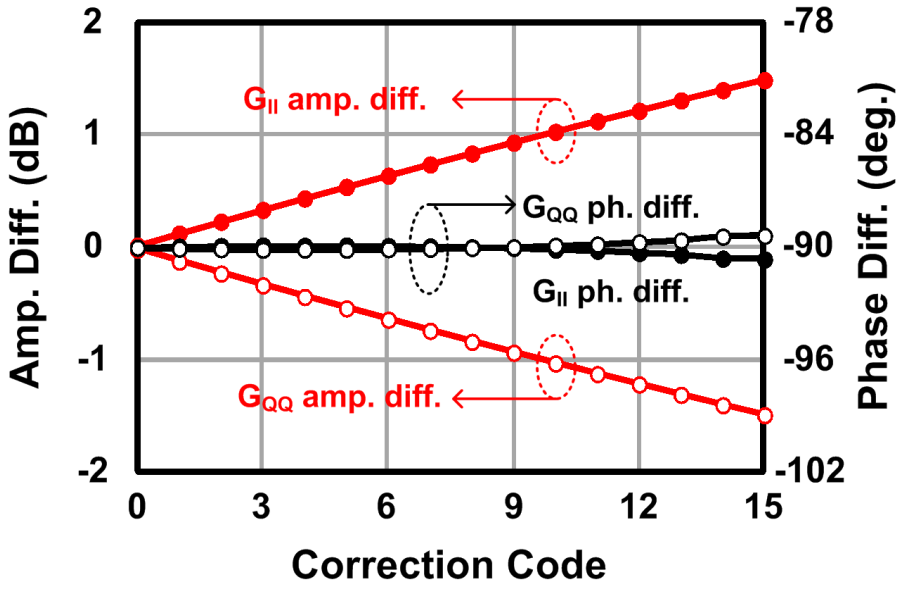


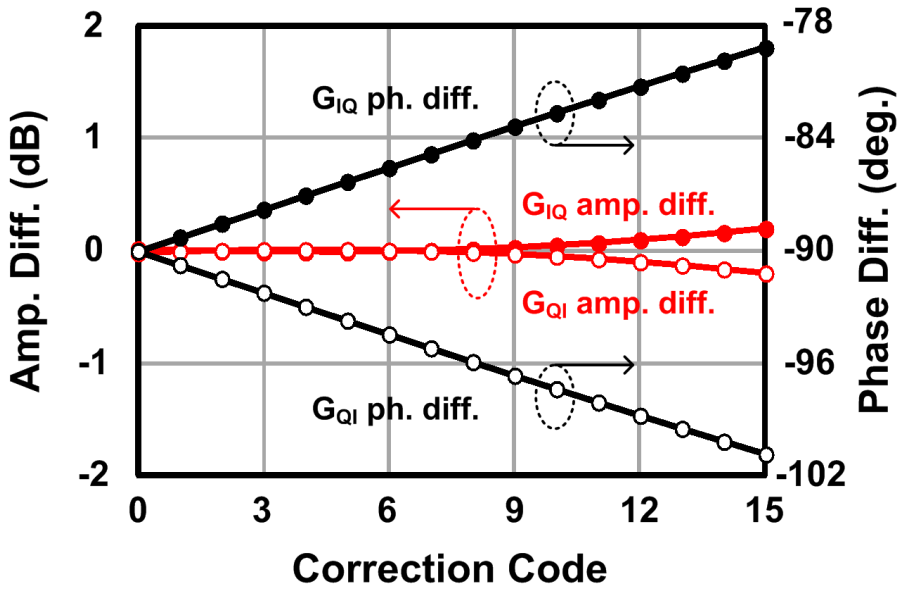
Figure 2.15: Schematic of the quadrature correction VGA.

The schematic of the 4-bit controlled quadrature correction VGA is shown in Fig. 2.15. The four VGAs (G_{II}, G_{QQ}, G_{IQ} and G_{QI}) are identical and share the input with the mixer core. The VGAs current adding with the I/Q mixers current forms the total baseband current. Note that the effective transconductance of an emitter degenerated amplifier is $g'_m = g_m/(1 + g_m R_E) \approx 1/R_E$, so the correction signal is actually determined by the binary-weighted degeneration resistors. The binary-weighted bias current is designed for equalizing the V_{BE} of each transconductor and makes the gain control linearly. The less significant bias current is 800 μA, and the current sources are switched on ($V_b = 0.7$ V) or off ($V_b = 0$ V). From the simulation, the amplitude difference in I/Q paths can be corrected up to ± 1.5 dB and the phase difference can be corrected up to $\pm 11^\circ$ as shown in Fig. 2.16.

Four I/Q correction VGAs require sixteen pins, so a correction-control circuit is placed to reduce number of pin from sixteen to six as shown in Fig. 2.17. To correct the four VGAs independently, A0 and A1 enable one of the four latches, and the correction signal B $\langle 0:3 \rangle$ controls how much I/Q mismatch should be cor-



(a)



(b)

Figure 2.16: Simulated I/Q mismatch by turning on (a) G_{II} and G_{QQ}, and (b) G_{IQ} and G_{QI}.

rected. Note that the I/Q correction is applied through a separate digital control word and are not in conjunction with I/Q data.

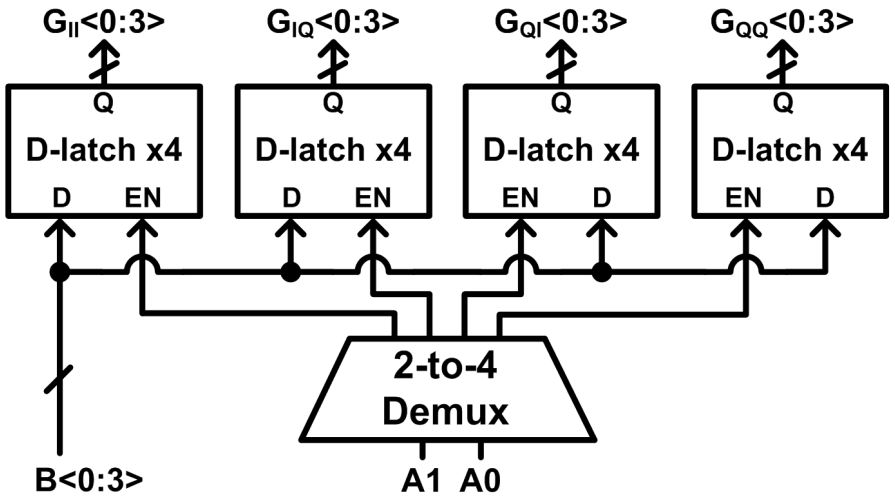


Figure 2.17: I/Q correction control circuit diagram.

2.4.4 Quadrature LO Generator Design

The LO generation circuitry is illustrated in Fig. 2.18 and provides dual-band differential quadrature LO signals from an external signal generator. The input Marchand balun, which converts the signals from single-ended to differential, is relatively wideband from Q-band to W-band. Parallel two-stage polyphase filters are implemented at 45 and 94 GHz, respectively, to generate the quadrature signals at each band. The layout of a polyphase filter introduces imbalance in the routing of the R and C components as well as mismatch between the R and C components and this causes I/Q amplitude and phase imbalance. As can be seen in Fig. 2.19, the routing for at least one connection must cross all other interconnects and is much longer. We used a polyphase filter layout that is also illustrated in Fig. 2.19 where each resistor is constructed by three larger parallel resistors and each capacitor is constructed by two larger serial capacitors to minimize I/Q imbalance. Since the resistors and the capacitors are small in a polyphase filter at the mm-wave band, the larger elements reduce process variations and result in better balance

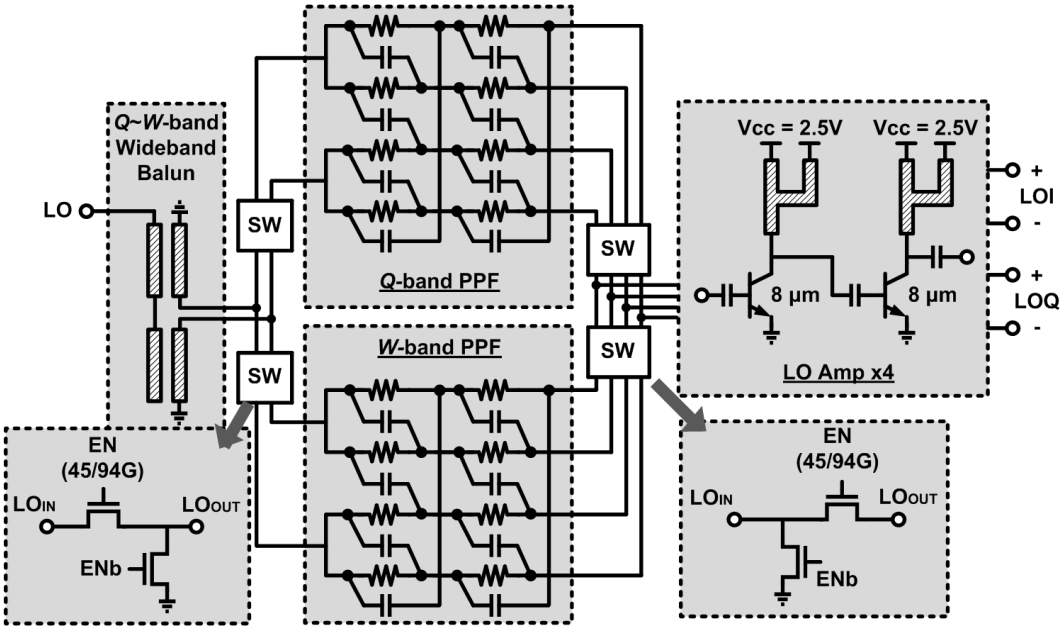


Figure 2.18: Schematic of the dual-band LO generator.

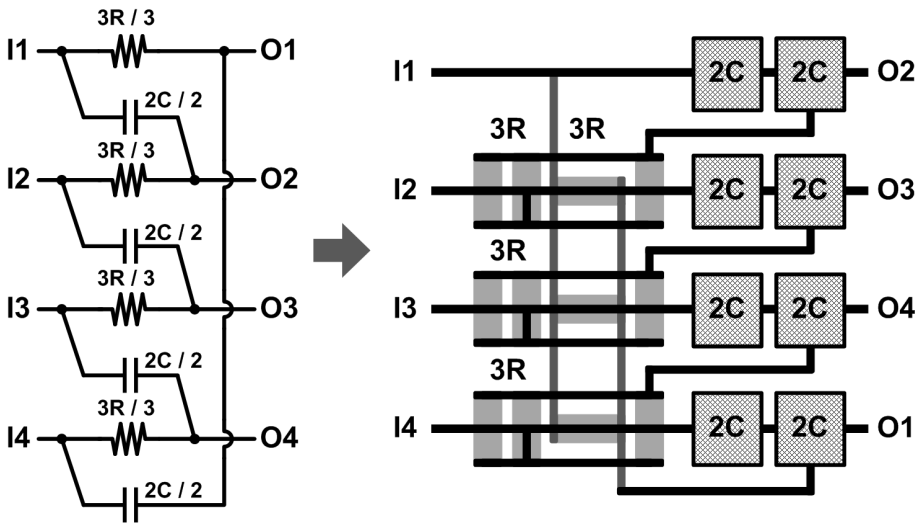
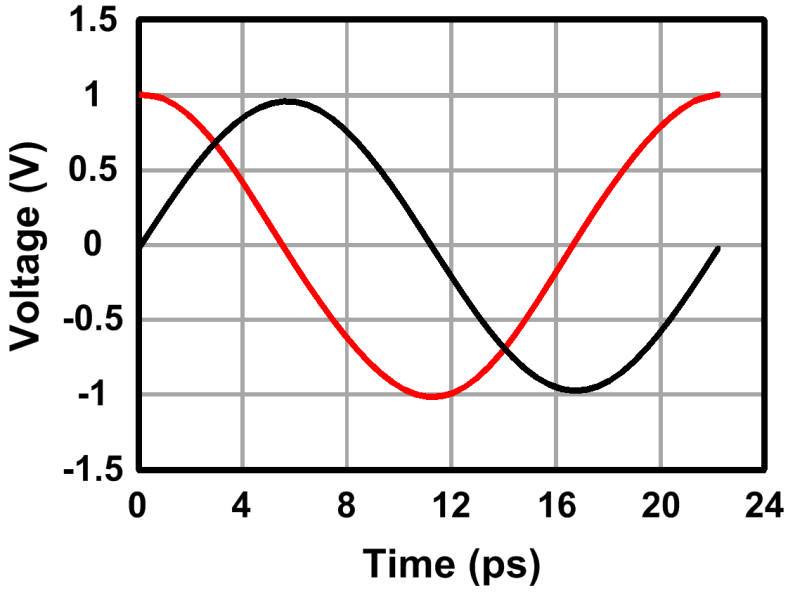
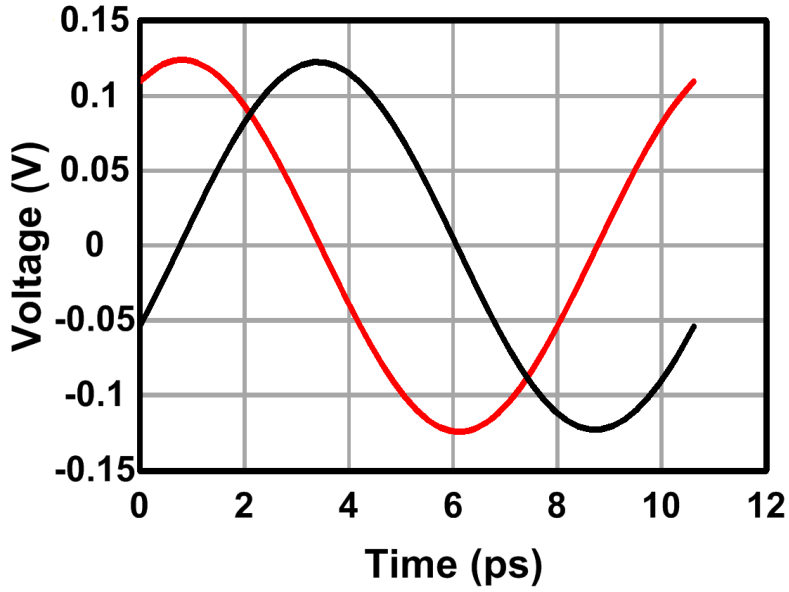


Figure 2.19: Polyphase filter layout.



(a)



(b)

Figure 2.20: Simulated I/Q LO generator output voltage at: (a) 45 GHz and (b) 94 GHz.

between I/Q signals. The switches are added at both the input and output of the polyphase filters for minimizing the loading effect and the interference between two frequencies. The switches allow the applied LO signal to be routed through the 45- or 94-GHz polyphase filter. The R_{ON} of the switch adds insertion loss, but does not introduce I/Q mismatch to the degree that the two switch transistors are matched. The switches are placed closed to each other in the layout to minimize device mismatch. The differential quadrature LO signals are then amplified by two-stage driving amplifiers with the dual-band loads to provide high LO swings to the mixer switches. The I/Q LO generator simulation results are shown in Fig. 2.20, where the LO input power is 7 dBm at both 45 and 94 GHz. At 45 GHz, the differential peak voltage to the mixer switches is 1 V with the amplitude mismatch of 40 mV (4%) and phase error of 1.2°. At 94 GHz, the differential peak voltage to the mixer switches is 130 mV with the amplitude mismatch of 5 mV (4%) and phase error of 1.3°. The low voltage swing issue will be discussed in Section 2.4.5. Each of the two-stage LO driving amplifier flows 12-mA dc current from a 2.5-V supply.

2.4.5 Power Amplifier Design

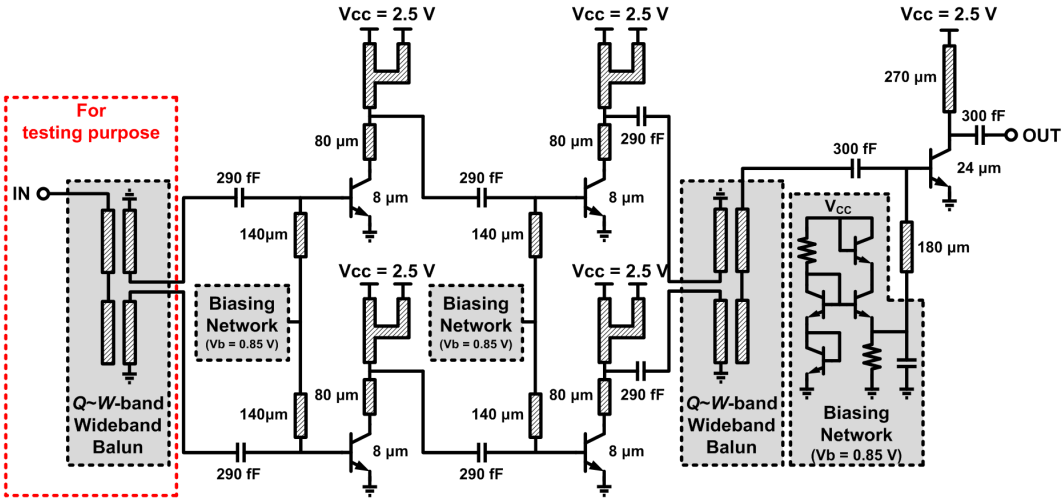


Figure 2.21: Schematic of the three-stage PA breakout.

In the 0.12-μm SiGe HBT process (f_T/f_{max} of 200/280 GHz) [31], the HBT device breakdown voltages are BV_{CEO} = 1.7 V and BV_{CBO} = 5.9 V [32]. At a high-supply voltage, the avalanche breakdown in the collector–base junction limits the response of the HBT. To handle a collector–emitter voltage above BV_{CEO} requires the ability to sweep carriers out of the base terminal with a relatively low impedance current sink.

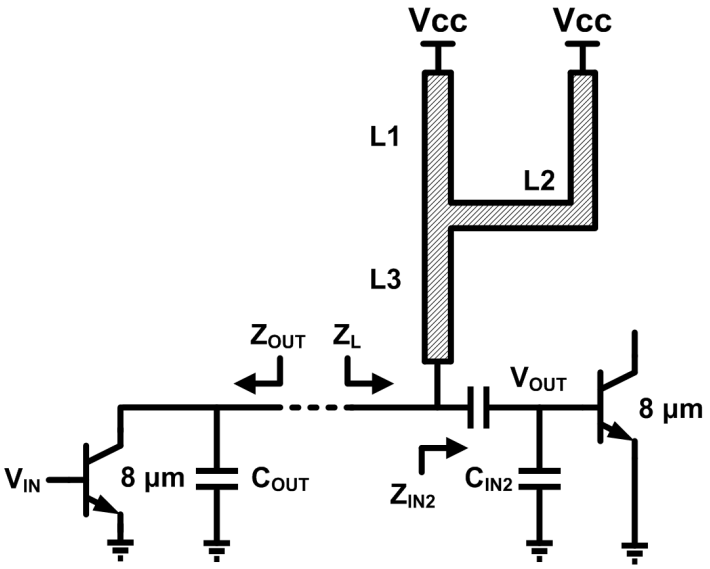
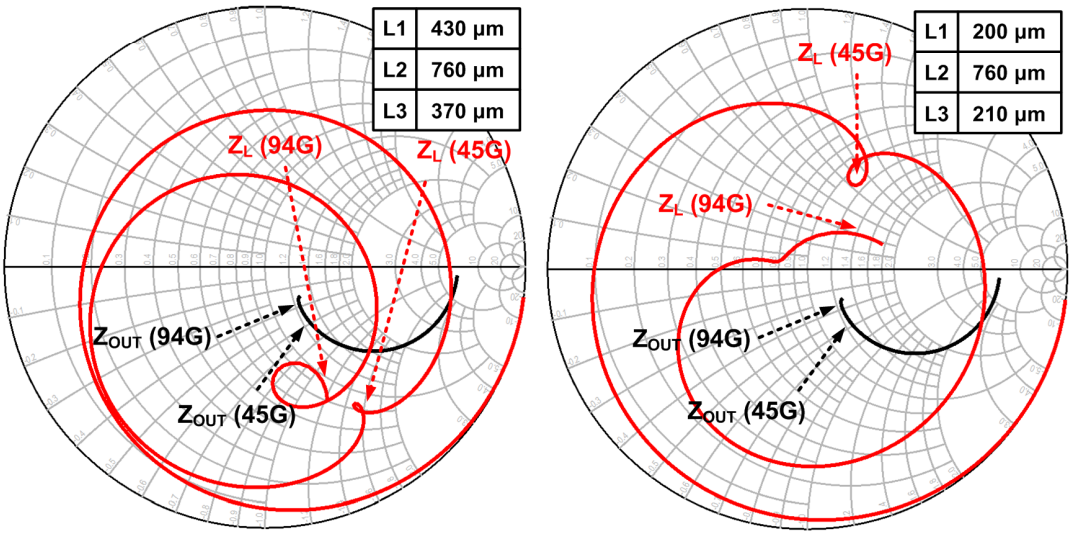


Figure 2.22: Dual-band load design with load capacitance.

Figure 2.21 shows the detailed schematic of the three-stage PA. Since the output of the up-converter is differential, the pseudo-differential pre-amplifiers are adopted in this design. Two Marchand baluns convert the signals from single-ended to differential at the input and differential to single-ended at the output of the pre-amplifiers, respectively. Note that the input balun and the transmission line is for the purpose of testing the standalone PA and can be laser trimmed for testing the whole transmitter. The loss of the transmission line with the input balun is 3.2 dB at 43 GHz and 82 GHz from simulation. The dual-band high impedance loads are seen at the collector of each pre-amplifier. The final stage of the PA has a relatively low load-line impedance, which is provided by an on-chip or off-chip matching network to reach high output power.



(a) (b)

Figure 2.23: Output impedance matching for: (a) quarter-wavelength and (b) inductive dual-band load.

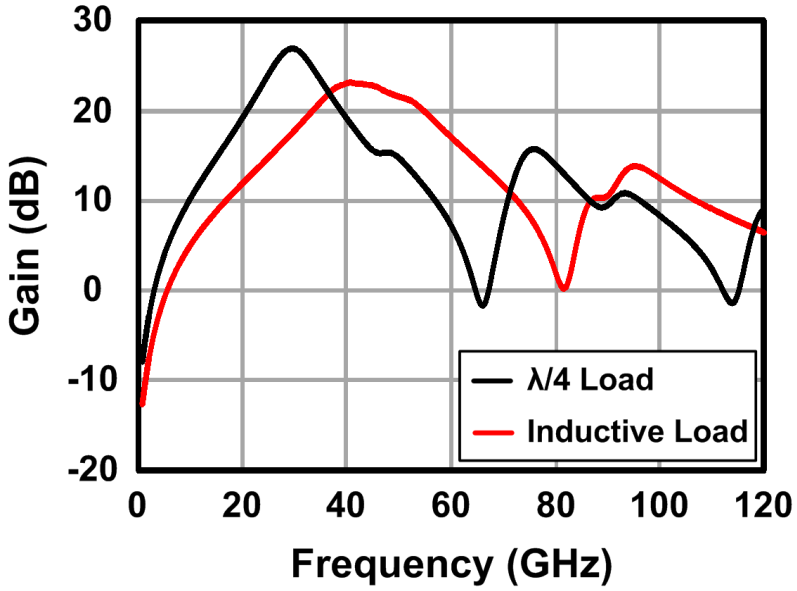


Figure 2.24: Simulated voltage gain of the dual-band amplifier.

For a dual-band amplifier design, the load impedance should be inductive at both frequencies rather than a quarter-wavelength dual-band load. The inductive dual-band load resonates the capacitance between the output impedance (Z_{OUT}) of the amplifier and the input impedance of the next stage amplifier (Z_{IN2}) as shown in Fig. 2.22. The dual-band load in conjunction with the input impedance of the next amplifier (Z_L) are designed to conjugately match Z_{OUT} of the amplifier. Figure 2.23(a) is the simulated Z_{OUT} and Z_L of the quarter-wavelength dual-band load. The quarter-wavelength dual-band load is a high impedance at 45 and 94 GHz and Z_{IN2} is capacitive. The output voltage is limited to the low impedance of C_{OUT} and C_{IN2}. The inductive dual-band load is implemented by shortening L_1 and L_3. L_2 is fixed to provide a short termination at f_2 at the end of TL_3. From the simulation shown in Fig. 2.23(b), the inductive dual-band load achieves complex conjugate matching with Z_{OUT} at 45 and 94 GHz. Figure 2.24 plots the simulation results of the dual-band amplifier where the gain is defined as V_{OUT}/V_{IN} in Fig. 2.22. With the inductive dual-band load, the amplifier gain is greatly improved at both frequencies.

2.5 Experimental Results

The dual-band transmitter is fabricated in a 0.12-μm SiGe BiCMOS process and occupies an area of 5.5 mm^2. Figure 2.25 shows the chip microphotograph and the four-layer printed circuit board (PCB) assembly. The chip pad frame supports 300-Mb/s digital I/O, dc bias voltages and currents, dc controlled I/Q correction, and the Q-band/W-band RF/LO ground–signal–ground (GSG) pads. All digital signals and dc pads are wire-bonded to a standard four-layer FR-4 PCB. Since the FR-4 substrate becomes excessively lossy for signals above 10 GHz, the Q-band/W-band LO and RF signals are probed on chip directly. $Z_o = 50\,\Omega$ stripline transmission lines are designed on a PCB to carry the high-speed digital data and clock. Digital data are routed on layer 3 to one side of the PCB and are picked up by an FMC LPC connector while the clock is fed by an SMA connector. The dc bias and the correction signals are routed on top layer and are supplied from

the opposite side for easier connections. The chip is epoxied to the PCB and the whole transmitter is tested on the chip-on-board assembly.

2.5.1 Dual-Band PA

The final PA breakout is measured to demonstrate the dual-band operation by inserting a balun and a differential transmission line at the PA input. The loss of the transmission line with the input balun is 3.2 dB at 43 GHz and 82 GHz from simulation. S-parameters are measured on wafer by using an Agilent E8361A network analyzer. The measured S-parameters are plotted in Fig. 2.26. The collector supply voltage is set to 2.5 V and provides self-biasing networks for the base of all BJTs. The total quiescent current is 27 mA. The small-signal gain is 17.9 dB at 43 GHz and 1.2 dB at 82 GHz where the input loss is included. The input/output return loss is 8.6 dB/13.8 dB at 43 GHz and 8.5 dB/13.4 dB at 82 GHz, respectively.

The large-signal behavior is measured on wafer as well where the loss of the input balun and the differential transmission line is de-embedded. The 43-GHz output power, gain and power-added efficiency (PAE) measurement results are shown in Fig. 2.27(a). The power gain for low input powers is 19 dB. The OP_{1dB} is 12 dBm. The peak PAE is 15% at 14-dBm output power, which is also the saturated output power ($Psat$). Figure 2.27(b) shows the 82-GHz output power, gain and PAE measurement results. The power gain for low input powers is about 5 dB. Due to the low gain at 82 GHz and the limitation of the signal generator, the output power as well as the gain did not saturate with the available input power. The output power and PAE measurement results are quite consistent with simulation while the gain drops 6 dB at 43 GHz and 3 dB at 82 GHz. The Q-band measurement results are comparable with state-of-the-art single-band PAs as listed in Table 2.1. The dual-band transceiver presented in [37] actually applies two single-band PAs at 24 GHz and 79 GHz, respectively. To the best knowledge of the author, the proposed implementation is the only dual-band PA working at mm-wave bands.

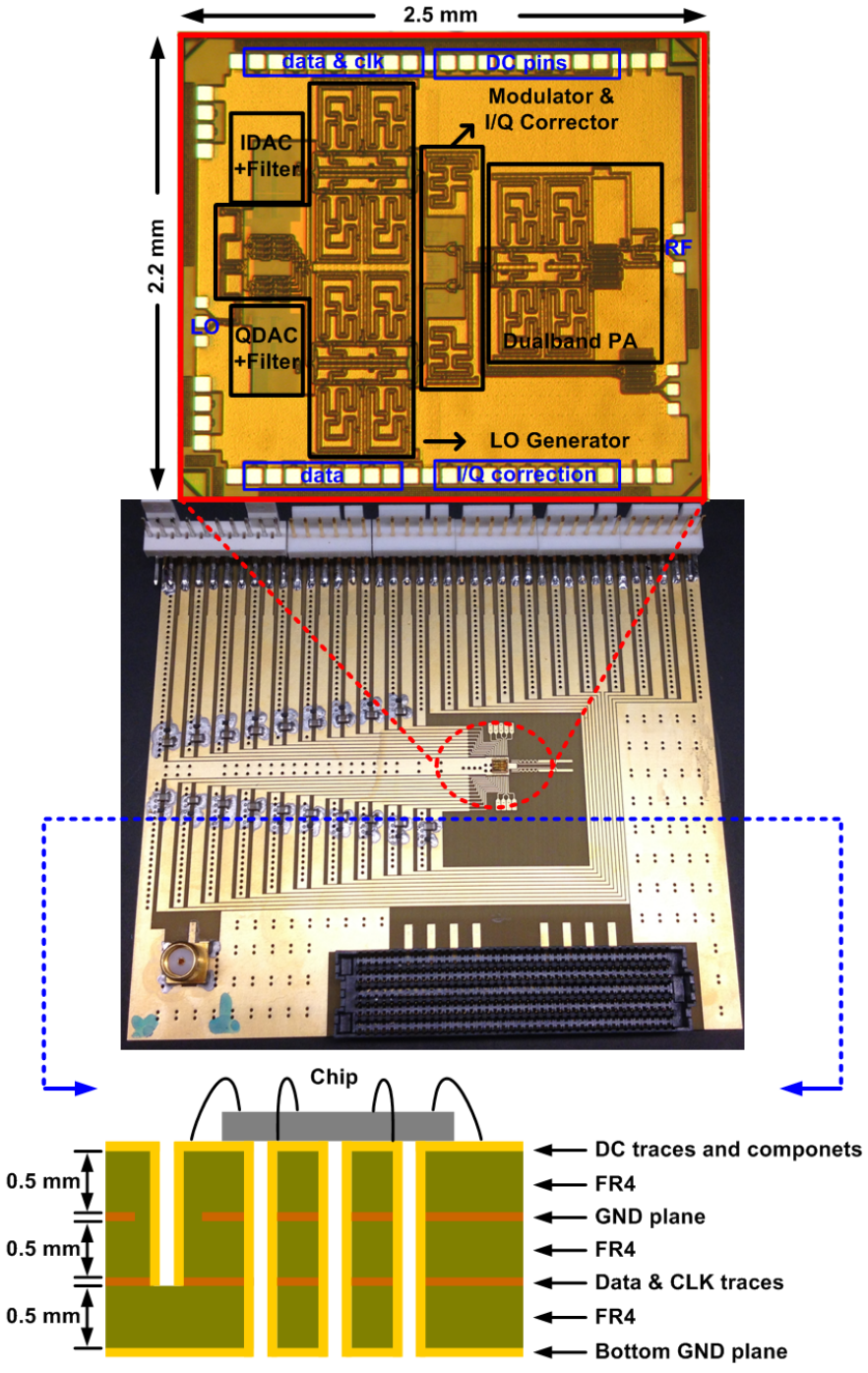


Figure 2.25: Microphotograph of the dual-band transmitter and the chip-on-board assembly.

Table 2.1: Performance summary and comparison of published mm-wave PAs.

Ref.	Technology	Description	Freq. (GHz)	Gain (dB)	Supply (V)	Psat (dBm)	PAE (%)	Area (mm^2)
This work	0.12-μm SiGe	Dual-band Class A PA	43	19	2.5	14	15	1
			82	5	2.5	8	2.3	1
[33]	0.12-μm SiGe	Single-band Class A PA	45	9.2	2.4	13.6	25	0.27
[33]	0.12-μm SiGe	Single-band Class B PA	45	7.8	2.4	14.75	30.8	0.27
[34]	0.13-μm SiGe	Single-band Class B PA	45	16.6	2.5	17.5	26	0.2
[35]	0.13-μm SiGe	Differential PA with power combining	60	20.5	1.8	20.5	19.4	0.72
[36]	0.13-μm SiGe	Differential PA with power combining	84	27	2.5	18	9	0.68
[37]	0.18-μm SiGe	Dual-band Transceiver	24	18	1.8	14.5	13.9	7.4
			79	10	1.8	10.5	4.7	7.4

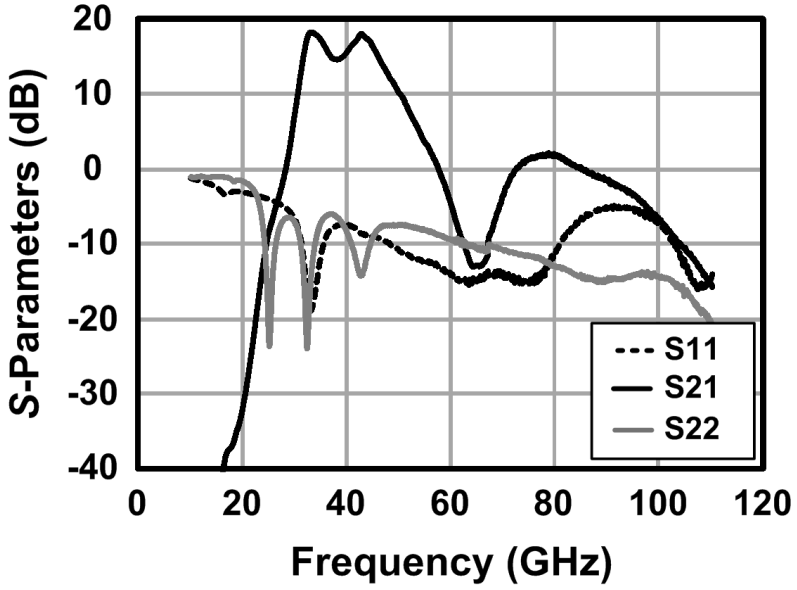
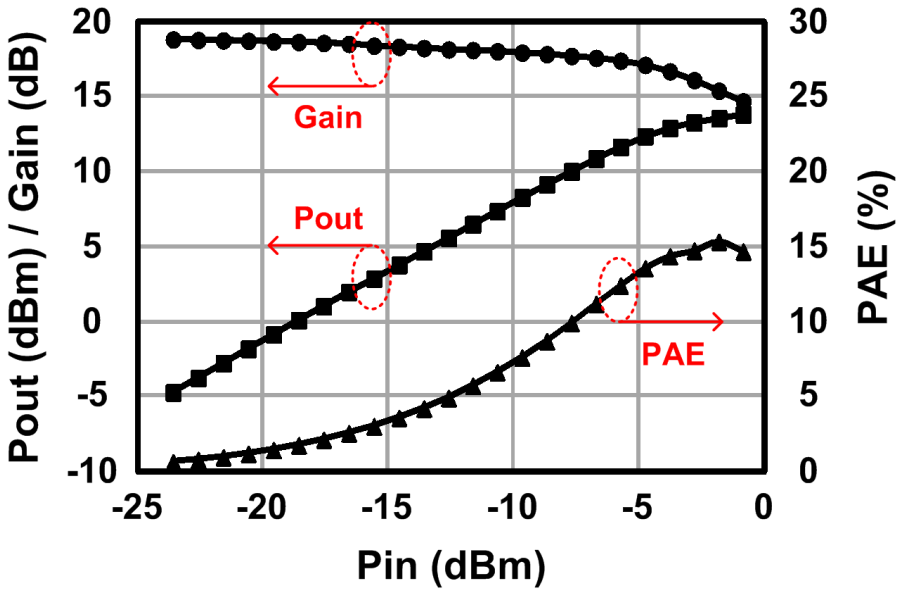


Figure 2.26: Measured S-parameter across Q-band and W-band of the dual-band PA breakout.

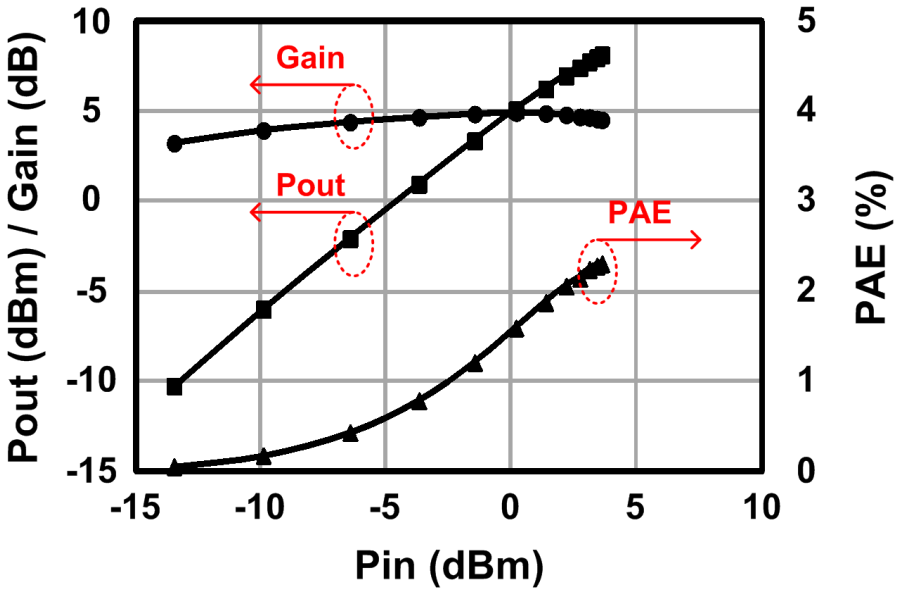
2.5.2 Transmitter Measurement Results at 45 GHz

The 45-GHz LO carrier signal is provided with an Agilent E8257D signal generator with 12-dBm output power. The available LO power on chip is 7 dBm due to the 5-dB loss of the 2.4-mm coaxial cables and the GSG probe at 45 GHz. A 10-dB Krytar coupler is connected to the RF output for measuring the output power and monitoring the output spectrum at the same time. The RF output power is sensed by an Agilent N8487A power sensor, which connects to the through port of the coupler, and is read by an Agilent E4419B power meter. An Agilent E4448A spectrum analyzer is connected to the coupled port to measure the EVM and SSR. All external losses are de-embedded including the 5-dB loss of the GSG probe and the cable and the 1-dB loss of the coupler at 45 GHz. Xilinx ML605 field-programmable gate-array (FPGA) board along with a laptop is used to provide digital data pattern of 300-Mb/s data rate and 300-MHz clock.

The measured RF output power is plotted as a function of the DAC full-scale voltage in Fig. 2.28. The $Psat$ is 10 dBm and the OP_{1dB} is 9 dBm. DPD



(a)



(b)

Figure 2.27: Measured output power, gain, and PAE of the dual-band PA breakout at: (a) 43 GHz and (b) 82 GHz.

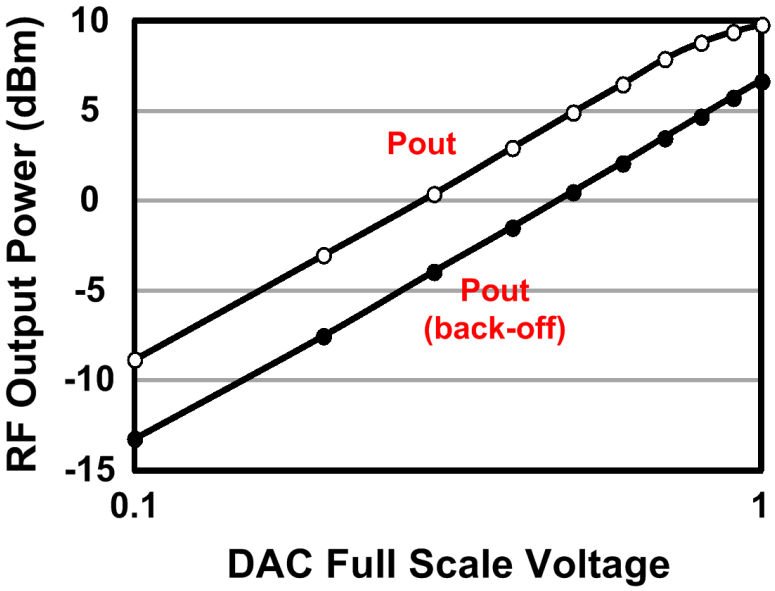


Figure 2.28: Measured 45-GHz RF output power versus DAC full-scale voltage.

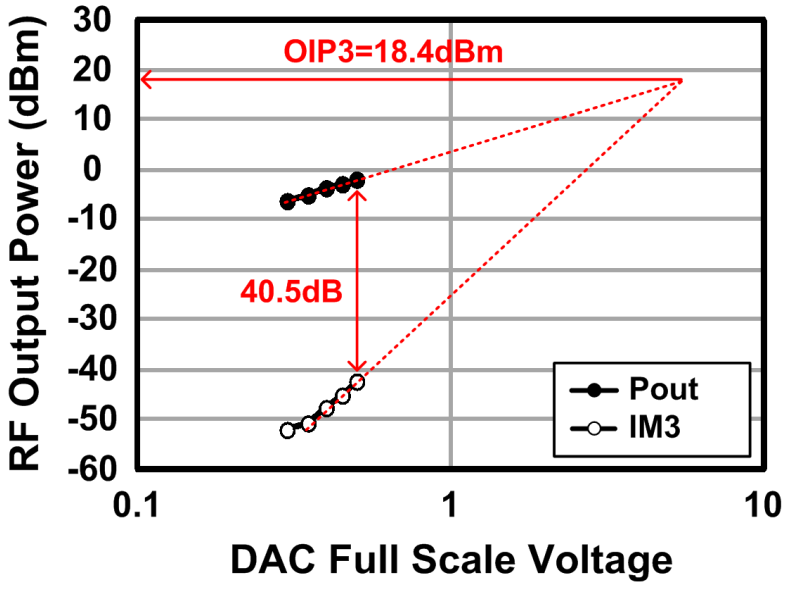


Figure 2.29: Measured 45-GHz OIP_3.

can be used to compensate the nonlinearity at high-power operation, however, the power of 3-dB back off is adopted in this work in order to demonstrate the I/Q correction technique without any kind of DPD. Figure 2.29 shows the measured output referred third-order intercept point (OIP_3) of 18.4 dBm by a two-tone test. The IF signal with –6-dB amplitude at f_{IF1} =2.4 MHz and f_{IF2} =2.5 MHz is applied at both I and Q inputs.

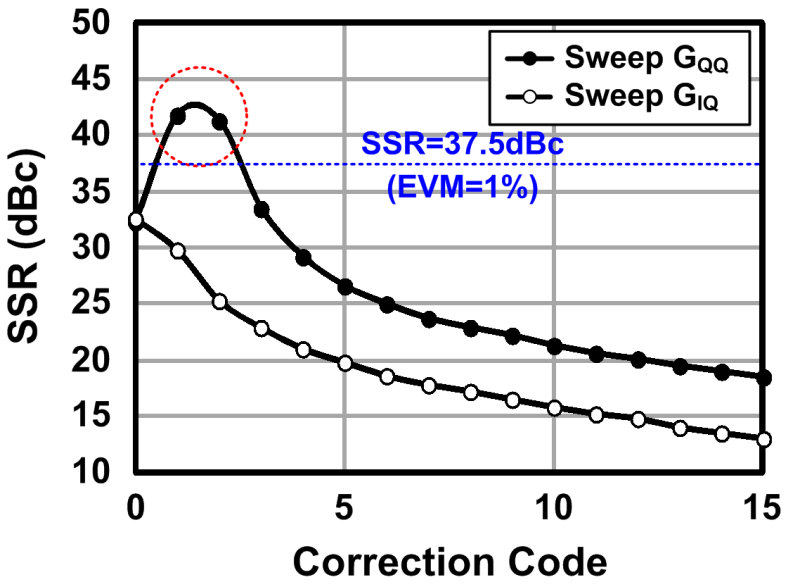
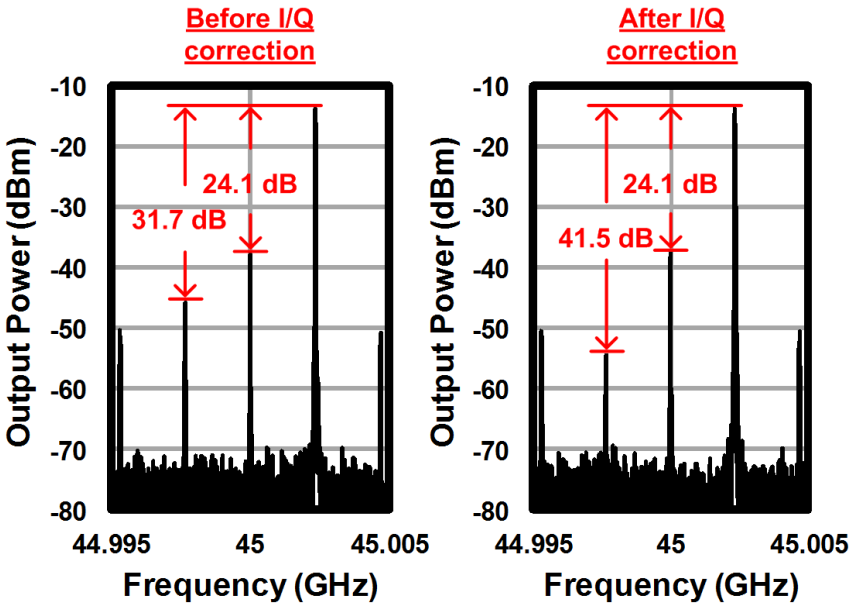
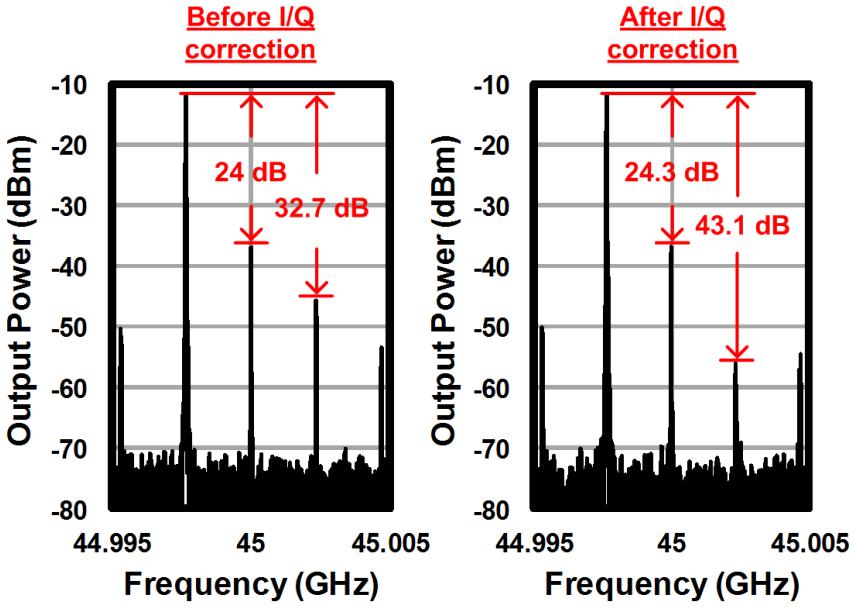


Figure 2.30: Measured 45-GHz SSR as a function of correction code.

As described in Section 2.1, the I/Q amplitude and phase imbalance must be corrected to achieve low EVM or correspondingly low SSR. By sweeping G_{IQ} or G_{QI} as plotted in Fig. 2.30, the SSR becomes worse when turning on the phase-correction VGAs. This suggests that the transmitter has insignificant phase mismatch and the I/Q mismatch is mainly from the amplitude error. Therefore, either G_{II} or G_{QQ} should be turned on to compensate the amplitude mismatch. By turning on G_{II}, the SSR also gets worse, however, by turning on G_{QQ} to $[b_3, b_2, b_1, b_0] = [0, 0, 1, 0]$, the SSR can be improved from 32 to 42 dBc, as shown in Fig. 2.31. This suggests that the amplitude imbalance is corrected from 4% to less than 2% [9]. Note that the I/Q correction codes are dc voltages and works for

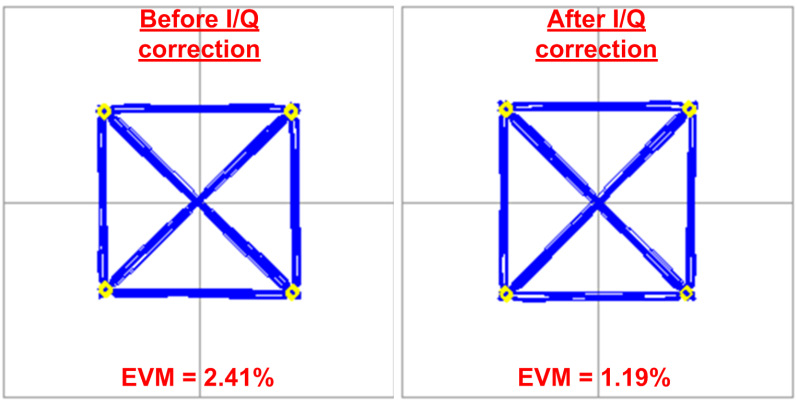


(a)

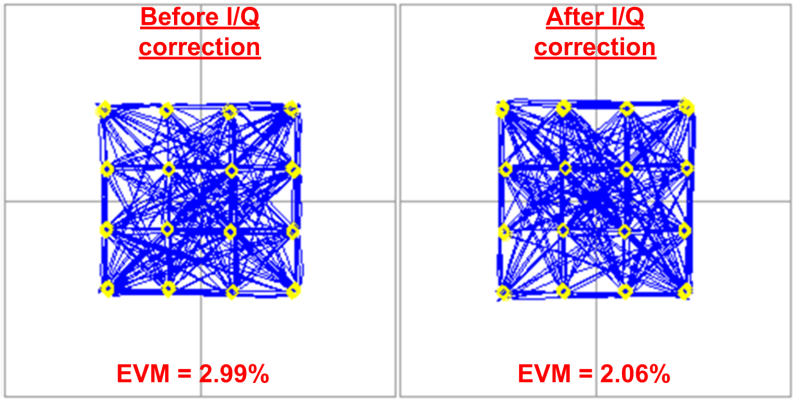


(b)

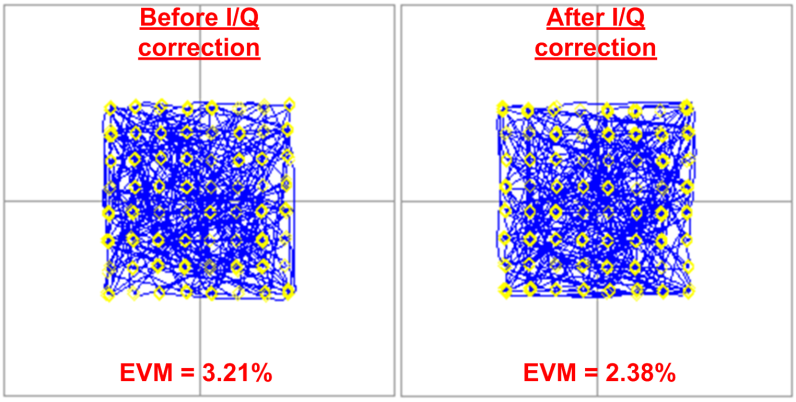
Figure 2.31: Measured 45-GHz RF output spectrum with I/Q correction. (a) LSB suppression. (b) USB suppression.



(a)



(b)



(c)

Figure 2.32: Measured 45-GHz I/Q corrected constellations at 2.4 Ms/s. (a) QPSK. (b) 16-QAM. (c) 64-QAM.

all various input data patterns. The power level in Fig. 2.31 is the actual number seen from the spectrum analyzer without de-embedding the total 19-dB loss from the 10-dB Krytar coupler, 2.4-mm cables and the RF probe. LO leakage is mainly caused by the mismatch from LO to RF path; however, it has an equivalent effect to the modulated dc offset in baseband [38, 39]. Therefore, LO leakage can be compensated by introducing a dc offset to the baseband I/Q channels through calibration. For LO leakage better than 24 dBc, a dc offset of 14 mV can be applied through the DACs.

Figure 2.32 is the measured constellation and EVM for QPSK, 16-QAM, and 64-QAM with symbol rates of 2.4 Ms/s with a carrier of 45 GHz. The EVM is measured by the Agilent E4448A spectrum analyzer, which has an internal 10-MHz demodulator and captures the baseband symbol. The amplitude mismatch is corrected by the I/Q compensation and the EVM is improved from 2.4% to 1.2% for QPSK, 2% to 2.1% for 16-QAM and 3.2% to 2.4% for 64-QAM, respectively, where the LO leakage is excluded in this measurement. To demonstrate how the proposed I/Q correction stages work, the amplitude and phase correction VGAs are intentionally turned on as the constellation twist for 16-QAM shown in Fig. 2.33. Turning on the correction code of G_{QQ} to $[b_3, b_2, b_1, b_0] = [1, 1, 1, 1]$, the constellation clearly becomes a rectangle instead of a square. By choosing the correction code of G_{QI} to $[b_3, b_2, b_1, b_0] = [1, 1, 1, 1]$, the constellation becomes a parallelogram. Even if the intentional I/Q mismatch will not be added in practical usage, the figure clearly tells the capability of calibrating the amplitude and phase errors.

Figure 2.34 plots the QPSK, 16-QAM, and 64-QAM EVM versus the symbol rate. Due to the limited number of digital V_{DD} pads and noise introduce by the digital lines, the EVM grows significantly when the symbol rate above 5 Ms/s. With the I/Q correction, the EVM can be improved about 1% and meet the specification of 2.5% [40]. Figure 2.35 is the EVM versus the average output power with the symbol rate of 2.4 Ms/s. With increasing output power, the EVM of 16-QAM and 64-QAM degrades due to amplitude compression. On the other hand, QPSK still has constant EVM at high-power operation since QPSK operates

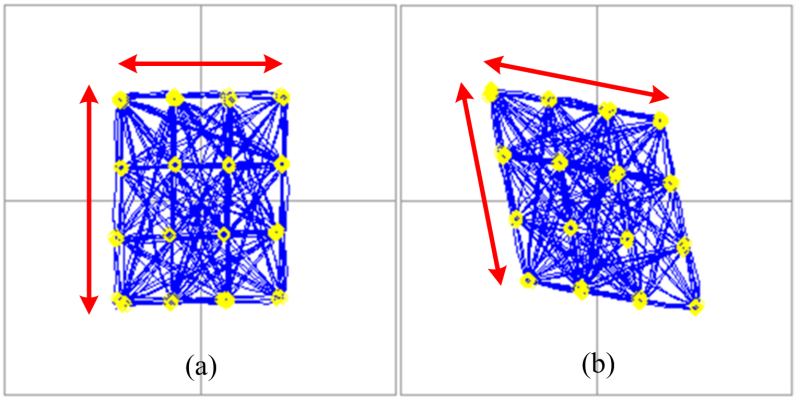


Figure 2.33: Measured 45-GHz 16-QAM constellations at 2.4 Ms/s by intentionally making: (a) amplitude and (b) phase imbalance.

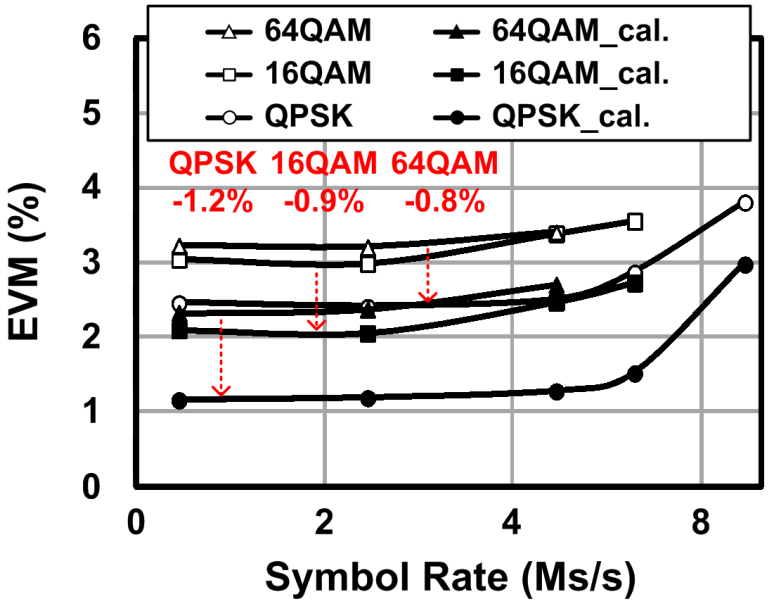


Figure 2.34: Measured 45-GHz I/Q corrected EVM versus symbol rate.

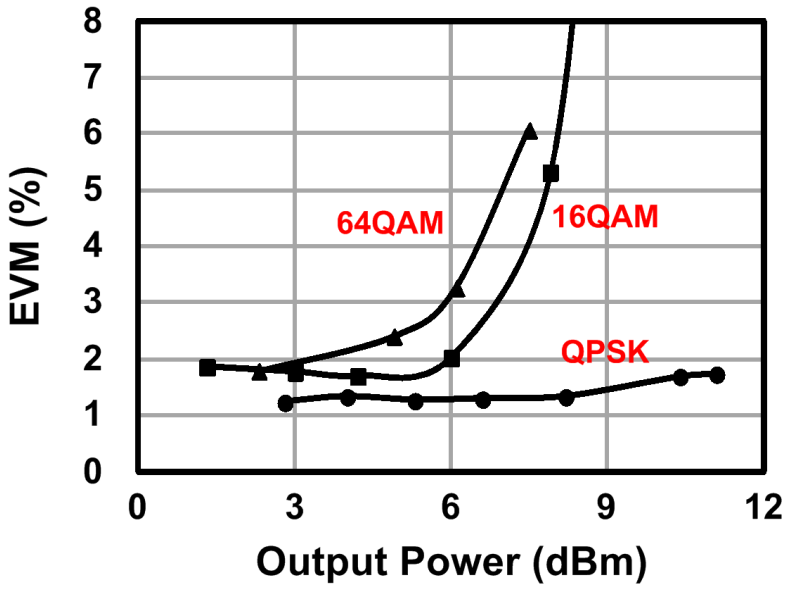


Figure 2.35: Measured 45-GHz I/Q corrected EVM versus output power.

with little amplitude variation.

2.5.3 Transmitter Measurement Results at 94 GHz

The 94-GHz LO carrier is provided by an Agilent E8257D signal generator at 47 GHz and then doubles the frequency to 94 GHz by a VDI D90 frequency doubler with 7-dBm available LO power on chip. The RF output signal is down-converted by a Pacific Millimeter 75110H balanced mixer to 1 GHz and measured by an Agilent E4448A spectrum analyzer. The LO carrier of the down-conversion mixer is provided by a Pacific Millimeter W3 frequency tripler with 4-dBm input at 31 GHz. The digital data patterns of the 300-Mb/s data rate and 300-MHz clock are also generated by the Xilinx ML605 FPGA board along with a laptop.

The I/Q imbalance at 94 GHz can be found by sweeping the gain of the amplitude and phase correction VGAs, as plotted in Fig. 2.36. By sweeping G_{II} and G_{QQ}, the SSR can be improved from 24 to 31 dBc when setting G_{II} to $[b_3, b_2, b_1, b_0] = [0, 0, 0, 0]$ and G_{QQ} to $[b_3, b_2, b_1, b_0] = [0, 0, 0, 1]$. This implies that the I/Q amplitude error is minimized, but the phase mismatch is not. Therefore, we

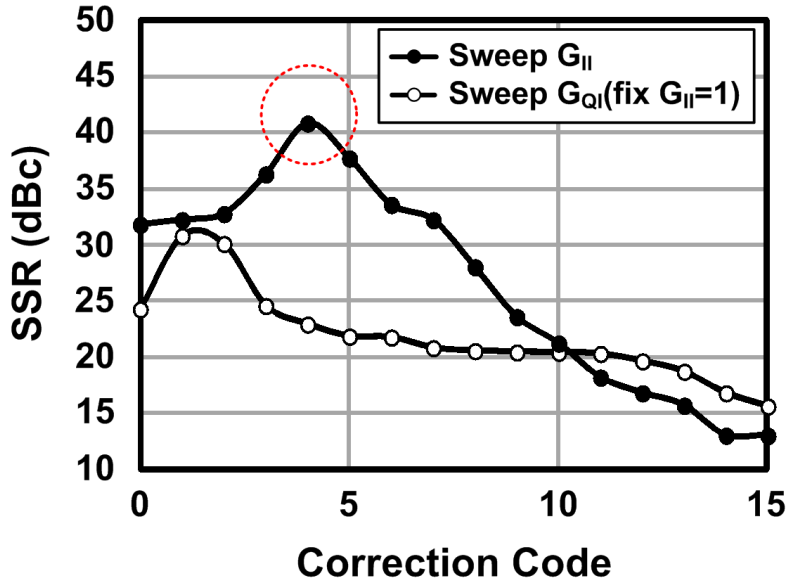


Figure 2.36: Measured 94-GHz SSR as a function of correction code.

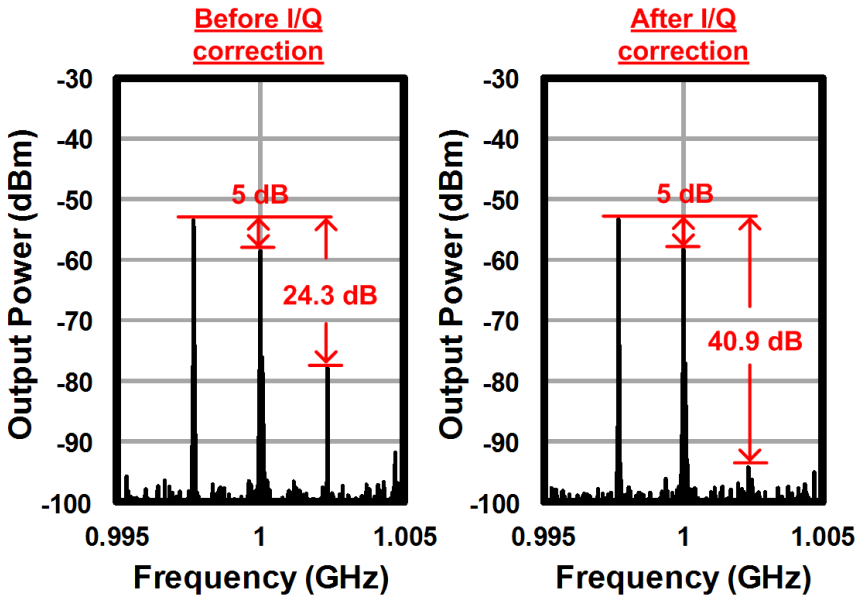


Figure 2.37: Measured 94-GHz RF output spectrum with I/Q correction.

fix G_{II} and sweep G_{IQ} and G_{QI} to find the optimized phase correction code. To fix G_{II} of $[0, 0, 0, 1]$ and choose G_{QI} to be $[0, 1, 0, 0]$, the SSR can be further improved from 31 to 41 dBc as the spectrum shown in Fig. 2.37. Therefore, the amplitude mismatch is less than 2% and phase imbalance is below 1°. Due to insufficient LO swing to the modulator, the RF output power is –42 dBm. The power shown in Fig. 2.37 is the raw value from the spectrum analyzer without de-embedding the 3-dB loss from the WR-10 probe and waveguide sections, 6.5-dB conversion loss from the Pacific Millimeter down-conversion mixer, and the 1-dB loss from the SMA cable to the spectrum analyzer at 1 GHz. The LO leakage, which is 5 dB lower than the RF power, mainly comes from the on-chip ground plane instead of the circuit. To suppress the LO leakage, to separate the LO ground from the RF ground is necessary. The polyphase filter has different amplitude and phase imbalances at different frequencies. Figure 2.38 plots the measured SSR versus LO frequency before and after the I/Q correction. Even if the polyphase filter is designed at 94 GHz, it has less I/Q mismatch below 88 GHz due to the imbalance layout and the model inaccuracies of the small resistors and capacitors at W-band. However, the proposed I/Q correction technique can correct the mismatches by applying different correction codes at different frequencies. As describing in the Section 2.5.2, the I/Q correction codes are all dc voltages and are available for all different input data patterns.

Figure 2.39 is the measured constellation and EVM for QPSK and 16-QAM with symbol rates of 3 Ms/s at 94 GHz. The modulated 94-GHz RF signal is also down-converted by the Pacific Millimeter 75110H balanced mixer to 1 GHz and demodulated by the Agilent E4448A spectrum analyzer. The 75110H balanced mixer has 6.5-dB conversion loss and greater than –20-dBm IP_{1dB} at 94 GHz, and thereby, the inherent nonlinearity is ignorable. Due to the low power and high LO leakage at RF output, the baseband information captured by the spectrum analyzer is noisy. However, the amplitude and phase correction can be clearly observed. For QPSK, the EVM can be improved from 13.5% to 12.3%. For 16-QAM, the EVM lowers from 15.1% to 13.8%, where the LO leakage is excluded. The implemented dual-band mm-wave I/Q transmitter performance is summarized and compared

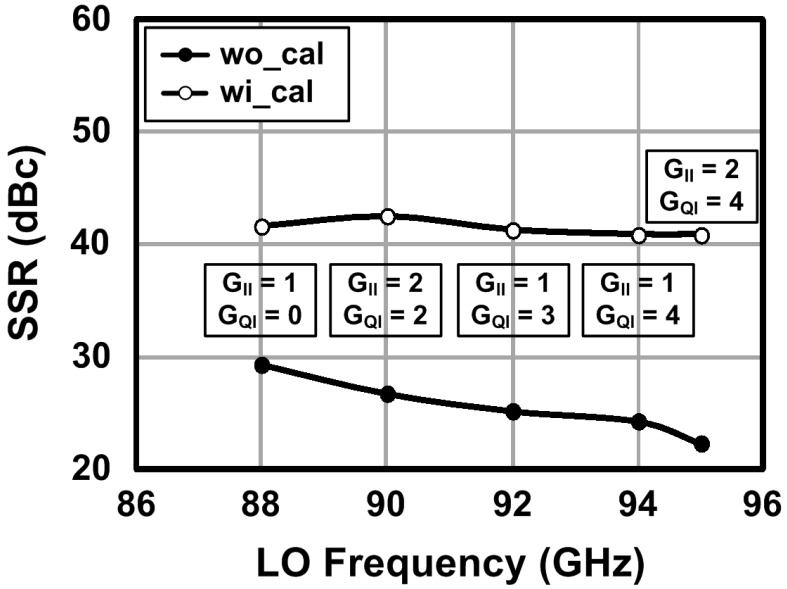
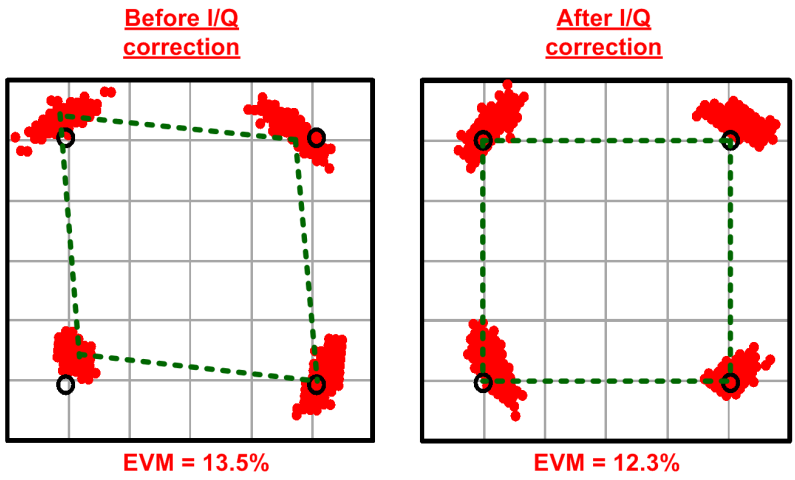


Figure 2.38: Measured SSR as a function of LO frequency in 90-GHz band.

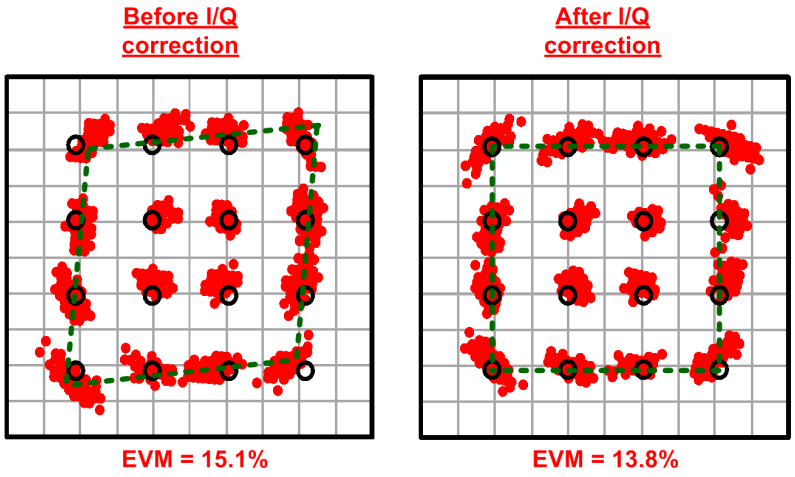
with prior works in Table 2.2. The I/Q modulator achieves a high SSR at 45 GHz and 94 GHz and low EVM with similar data rates at 45 GHz without using DPD.

2.6 Conclusions

A dual-band transmitter is demonstrated in 0.12-μm SiGe BiCMOS process at Q-band and W-band. The dual-band operation is achieved by a transmission-line-based dual-band load and a general analysis is presented to design this load for two arbitrary frequencies. Dual-band operation also necessitates the quadrature correction technique to minimize the amplitude and phase imbalances of the I/Q paths. The measurement results at 45 GHz and 94 GHz exhibit symmetric constellation diagrams and low EVM, which verify the capability of I/Q correction at different frequency bands.



(a)



(b)

Figure 2.39: Measured 94-GHz I/Q corrected constellations at 3 Ms/s for (a) QPSK and (b) 16-QAM.

Table 2.2: Performance summary and comparison of published mm-wave transmitters.

Reference	This work		[9]	[41]	[42]	[43]
Technology	0.12-μm BiCMOS		0.12-μm BiCMOS	0.15-μm AlGaAs/InGaAs	0.15-μm pHEMT	0.18-μm BiCMOS
Frequency	45 GHz	94 GHz	45 GHz	60 GHz	60 GHz	90 GHz
OP_{1dB}	9 dBm	–	1 dBm	–5.6 dBm	–13 dBm	8 dBm
OIP_3	18.4 dBm	–	11 dBm	–	–	–
SSR	43.1 dBc	40.9 dBc	40 dBc	>40 dBc	>40 dBc	>40 dBc
EVM	1.19% (QPSK)	12.3% (QPSK)	2.2% (QPSK)	4% (QPSK)	–	2.93% (256-QAM)
	2.06% (16-QAM)	13.8% (16-QAM)	2.3% (16-QAM)	5.5% (16-QAM)	6% (16-QAM)	
	2.38% (64-QAM)	–	2.1% (64-QAM)	–	4.2% (64-QAM)	
Symbol Rate	2.4 Ms/s	3 Ms/s	8 Ms/s	15 Ms/s	6% (16-QAM)	5 Ms/s
					4.2% (64-QAM)	
On-chip DAC	Yes		Yes	No	No	No
DPD	No		Yes	No	No	No
DC Power	358.7 mW		138 mW	–	420 mW	1 W
Chip size	5.5 mm^2		5 mm^2	2.9 mm^2	4.5 mm^2	3.4 mm^2

Acknowledgements

This chapter is mostly a reprint of the material as it appears in IEEE Compound Semiconductor Integrated Circuit Symposium, Oct. 2013, P. Wu; J. F. Buckwalter and IEEE Transactions on Microwave Theory and Techniques, Dec. 2014, P. Wu; A. K. Gupta; J. F. Buckwalter. This dissertation author was the primary author of this material. The authors are grateful to the Defense Advanced Research Projects Agency (DARPA) Leading Edge Access Program (LEAP) for accessing to the IBM 8HP technology and the DARPA Efficient Linearized All-Silicon Transmitter ICs (ELASTx) program (Dr. S. Raman) and the U.S. Army Research Office (Dr. D. Palmer) for support. The authors would also like to thank Professor P. Asbeck for discussions on the design and measurements and H. Dabag for helping with the FPGA programming. Additionally, the support of the National Science Foundation (NSF) is greatly appreciated.

Chapter 3

45 and 94-GHz Transmitters Utilizing Digital Predistortion

3.1 EVM Considerations

EVM is a key metric for transmitter systems. Various circuit nonidealities, such as nonlinearity, in-band noise, LO phase noise, I/Q amplitude and phase imbalances, and LO leakage, degrade the EVM. Chapter 2 specifically discusses the impact of I/Q mismatch. This section presents a comprehensive expression of the circuit nonideality contributions to the EVM. As shown in Fig. 3.1, the errors in a transmitter employing I/Q modulation scheme can be decomposed into a series of sources. Baseband I and Q signals, v_I and v_Q, are two sequences of independent data. For an M-ary QAM, each I and Q signal takes one of $\sqrt{M}$ values with equal probability. For instance, v_I and v_Q independently take one of eight values $[-7, -5, -3, -1, 1, 3, 5, 7]$ for 64-QAM. α and θ denote the I/Q amplitude and phase mismatches generated from the I/Q modulator. LO leakage or carrier feed-through can be represented as a dc offset in baseband, therefore it can be modeled as a constant voltage in I/Q path. The multiplication term $e^{j\psi_{rms}}$ represents the LO phase noise. At the PA stage, the linear and nonlinear terms can be expressed as a K-order polynomial given by $g_1 v + g_3 v^3 + ... + g_k v^k$, where g_1 and g_k are the linear and nonlinear coefficients, respectively, and v is the

input voltage. g_3–g_k denote the PA AM–AM distortion and the $\Phi(|v|)$ denotes the AM–PM distortion.

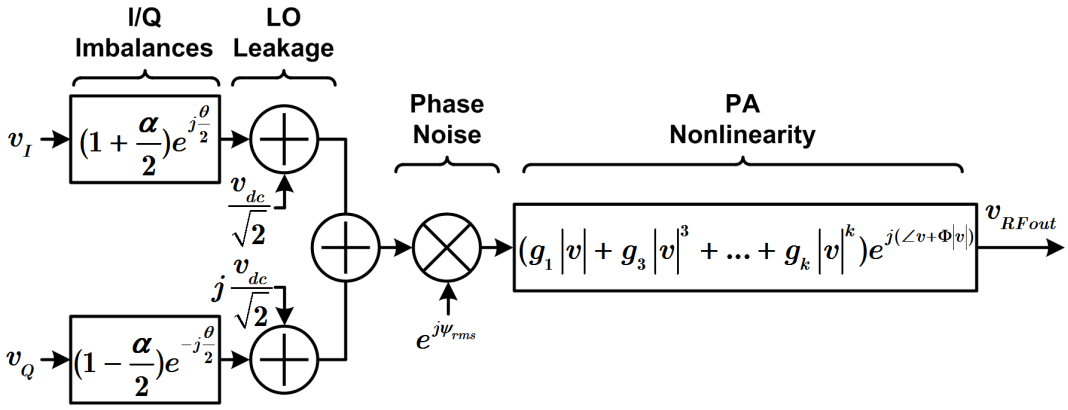


Figure 3.1: Errors in a transmitter system.

When the errors are presented in the signal path, the transmitted envelope is distorted relative to the ideal reference. The EVM is defined as the normalized error between the transmitted and the reference symbols and can be expressed as [9]

$$EVM = \sqrt{\frac{E\left[|v_{env} - v_{ref}|^2\right]}{E\left[|v_{ref}|^2\right]}} \tag{3.1}$$

where v_{env} is the transmitted envelope, v_{ref} is the reference envelope, and $E[\cdot]$ is the expectation operator. The reference output envelope should be calculated to normalized the power of the transmitted envelope and is expressed as the summation of v_I and v_Q multiplies by a linear scaling factor of G:

$$v_{ref} = G \cdot (v_I + jv_Q). \tag{3.2}$$

In the subsequent discussions, the discrete-time notation for the transmitted and reference envelope are removed for brevity.

3.1.1 I/Q Imbalances

With I/Q amplitude and phase imbalances, the transmitted envelope can be described as

$$v_{out} = (1 + \frac{\alpha}{2})e^{j\theta/2}v_I + j(1 - \frac{\alpha}{2})e^{-j\theta/2}v_Q. \tag{3.3}$$

The EVM due to the I/Q imbalance can be approximated as

$$EVM_{IQ,mis} \approx \sqrt{\left(\frac{\alpha}{2}\right)^2 + \left(\frac{\theta}{2}\right)^2}. \tag{3.4}$$

Note that here we assume the I/Q imbalance is small, i.e., $\alpha \ll 1$ and $\theta \to 0$, and is independent of the I/Q nonlinearity. For a large I/Q mismatch and highly compressed transmitter, this expression might not be very accurate.

3.1.2 LO Leakage

In a direct-conversion I/Q modulator, dc offsets presented in the I and Q channels cause the LO leakage in the RF band. The EVM degradation due to LO leakage can be found as [22]

$$EVM_{LO,leak} = \sqrt{\frac{P_{LO,leak}}{P_{avg}}}. \tag{3.5}$$

For instance, if the LO leakage power is 40 dBc below the average transmitted power, the $EVM_{LO,leak}$ is 1%. LO leakage is particularly significant for a direct-conversion system since it directly contributes a dc offset in the receiver.

3.1.3 LO Phase Noise

Another main contribution to the EVM degradation is the phase noise of the frequency synthesizer applied as LO of the modulator. The impact of the LO phase noise (ψ_{rms}) on the EVM can be estimated as [22]

$$EVM_{Nphase} = \psi_{rms}. \tag{3.6}$$

For instance, if the root-mean-square phase noise is 1°, the EVM_{Nphase} is 1.74%.

3.1.4 PA Nonlinearities

The PA conventionally dominates the nonlinearity in a transmitter. At the PA input, the magnitude and phase of each symbol can be written as $M = a_1\sqrt{v_I^2 + v_Q^2}$ and $\phi = \tan^{-1}\left(\frac{v_Q}{v_I}\right)$. After the compression, the PA output envelopes can be found as

$$v_{PA} = \left(g_1 M + g_3 M^3\right) \exp\left(j\left(\phi + \Phi\right)\right) \tag{3.7}$$

where reference envelope is

$$v_{ref} = G \cdot M \exp\left(j\phi\right). \tag{3.8}$$

g_1 and g_3 are the power series coefficients describing AM–AM compression and Φ is the factor for AM–PM distortion. Here we assume the transmitter nonlinearity is weak, i.e., only third-order harmonic term is included. The scaling factor G can be calculated as

$$G = \sqrt{g_1^2 + 2g_1 g_3 h_1 + g_3^2 h_2} \tag{3.9}$$

where

$$h_x = \frac{E\left[M^{2x+2}\right]}{E\left[M^2\right]}. \tag{3.10}$$

The resultant EVM due to the AM–AM compression can be expressed as

$$EVM_{AM-AM} = \frac{1}{G}\sqrt{\left(g_1 - G\right)^2 + 2\left(g_1 - G\right) g_3 h_1 + g_3^2 h_2}. \tag{3.11}$$

The PA exhibits a phase shift as function of output power that also distorts the constellation. The EVM due to the AM–PM distortion can be found as [9]

$$EVM_{AM-PM} = \sqrt{c_2^2 h_2 + c_4^2 h_4 - 2c_2 c_4 h_3}, \tag{3.12}$$

where c_2 and c_4 are the power series coefficients of the AM–PM distortion and the factor h_x is determined in (3.10).

The accurate expression of the EVM due to AM–AM and AM–PM distortions is very complicated since they are correlated. In addition, these distortions depend on the probability distribution function (PDF) of the envelopes, signal characteristics, channel frequency response, etc. More analysis of EVM caused by the nonlinearities can be found in [9, 22, 44, 45].

3.1.5 Overall EVM

The overall EVM of the transmitted symbols is the root-sum-square EVM contributions from each source and can be expressed as

$$\begin{aligned} EVM_{total} &= \sqrt{\sum_k EVM_k^2} \\ &= \sqrt{EVM_{IQ,mis}^2 + EVM_{LO,leak}^2 + EVM_{Nphase}^2 + EVM_{AM-AM}^2 + \cdots}. \end{aligned} \tag{3.13}$$

Here, all the factors contributing to the EVM are assumed to be uncorrelated. I/Q imbalances, LO leakage, and LO phase noise are from different error sources and exhibit very weak correlation. In a weakly distorted transmitter, the EVM due to AM–AM and AM–PM compressions can also be assumed independent since the AM–AM compression is mainly caused by odd-order harmonic terms and the AM–PM distortion is mainly caused by even-order harmonics.

3.2 A 45-GHz Direct-Conversion Transmitter Utilizing DPD

The goal of this work is to demonstrate an all-silicon-based efficient and high linearity transmitter at 45 GHz (Q-band). Figure 3.2 shows the block diagram of this direct-conversion transmitter. Digital data from an FPGA-based DSP are directly up-converted to 45-GHz band by the I/Q modulator implemented in 120-nm SiGe BiCMOS process and presented in Chapter 2 [25]. The modulated signal feeds a two-by-two PA/antenna array to produce high radiated power by spatial power combining [21]. The calibration receiver captures the transmitter errors, which include nonlinearity, I/Q mismatch, LO leakage, memory effects, etc., and converts these to digital format. These errors are modeled by DPD algorithms [46, 47] and the coefficients of the DPD model can be extracted to the look-up table (LUT). The digital predistortor provides the predistorted input data from the inverse function of polynomial and, thus, allows the transmitter to operate at high power and high efficiency. Meanwhile, high linearity and low EVM can be

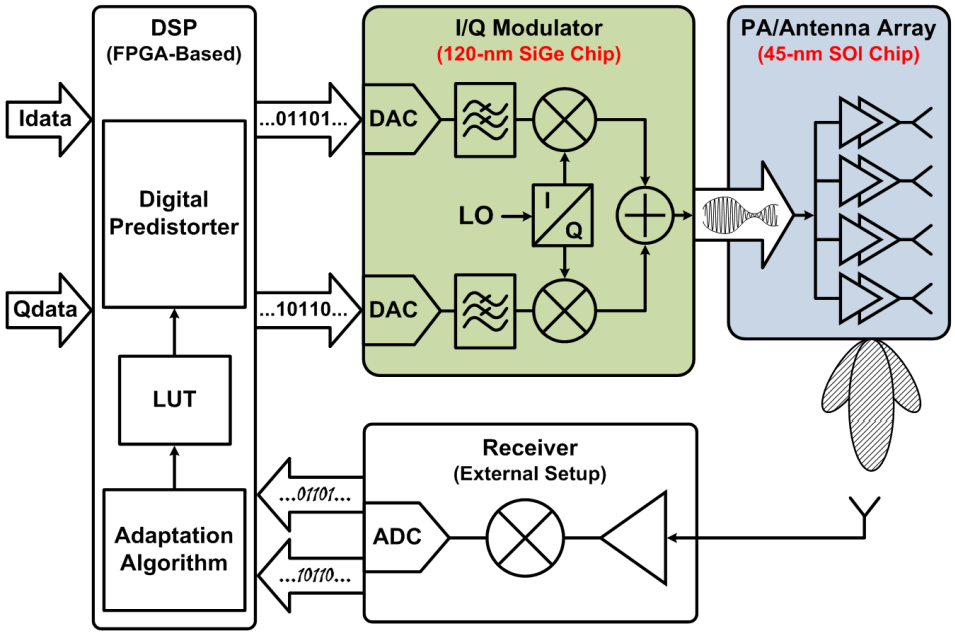


Figure 3.2: System block diagram of the 45-GHz direct-conversion transmitter.

achieved.

3.2.1 Dual-Input I/Q Memory Polynomial

DPD intentionally predistorts the input signal to compensate the PA nonlinearity. The memory polynomial model (MPM) has been widely used for modeling and predistorting the PA. MPM can be formulated as [48]

$$y(n) = \sum_{m=0}^{M-1} \sum_{k=1}^{K} c_{m,k} x(n-m) \left| x(n-m) \right|^{k-1} \tag{3.14}$$

where $x = x_I + j \cdot x_Q$ and $y = y_I + j \cdot y_Q$ are the complex input and output baseband envelopes, $c_{m,k}$ are the MPM complex coefficients, K is the maximum nonlinear order, and M is the memory depth of the model. In addition to the nonlinearity and memory effects, I/Q imbalance and LO leakage are also main impairments originating from the I/Q modulator. The MPM can be expanded to a dual-input I/Q MPM [47, 49].

To investigate the dual-input I/Q MPM, we firstly consider the simplest case of (3.14) that $M = 0$, $K = 3$, and $c_{m,k} = 1$. We obtain the following expression:

$$y_I(n) = x_I(n) + x_I(n)|x(n)| + x_I(n)x_Q^2(n) + x_I^3(n) \tag{3.15}$$

$$y_Q(n) = x_Q(n) + x_Q(n)|x(n)| + x_I(n)x_I^2(n) + x_Q^3(n). \tag{3.16}$$

It can be observed from (3.15) and (3.16) that y_I and y_Q are both polynomial functions of x_I, x_Q, and the terms of $|x(n)|^{k-1} = \sqrt{x_I^2(n) + x_Q^2(n)}^{k-1}$. This observation inspires the idea of expanding (3.14) by inserting additional monomials of the input I/Q components. By keeping the dynamic properties, the dual-input I/Q MPM can be derived as

$$y_I(n) = \sum_{m=0}^{M-1}\sum_{k=1}^{K}\sum_{l=0}^{k} a_{m,k,l}x_I^{k-l}(n-m)\,x_Q^l(n-m) + c_I \tag{3.17}$$

$$y_Q(n) = \sum_{m=0}^{M-1}\sum_{k=1}^{K}\sum_{l=0}^{k} b_{m,k,l}x_Q^{k-l}(n-m)\,x_I^l(n-m) + c_Q, \tag{3.18}$$

where x_I, x_Q, y_I, and y_Q are real baseband symbol sequences. $a_{m,k,l}$ and $b_{m,k,l}$ are respective real coefficients in I and Q channel. c_I and c_Q express the dc offset and equivalently refer to the LO leakage in RF band. The dual-input I/Q MPM directly defined in the I/Q components is beneficial to model the errors from the I/Q modulator and the PA. This model contains odd- and even-order terms and is also capable to calibrate the nonlinear I/Q mismatch. The LUT contains the model coefficients $a_{m,k,l}$ and $b_{m,k,l}$, which are found from the errors. The predistorted input data can be obtained from the inverse function of polynomial in (3.17) and (3.18).

3.2.2 45-GHz I/Q Modulator

The direct-conversion I/Q modulator employed in this work is presented in Chapter 2. Figure 3.3 shows the simplified block diagram of this I/Q modulator. Complex I/Q digital data are converted to analog signals by 8-bit I/Q DACs. The I/Q analog baseband envelopes are then filtered by low-pass reconstruction

filters. For a 20-MHz signal bandwidth, the cutoff frequency is chosen to be 60-MHz since DPD requires three times the signal bandwidth to model at least the third-order nonlinearity. The I/Q baseband signals are then directly up-converted to 45-GHz band by double-balanced Gilbert mixers with the static I/Q correction stage. Transconductor pairs in the mixer and I/Q correction VGAs are designed using HBT devices with resistive degeneration for better linearity. The LO switches are implemented in NMOS to lower the supply voltage. The I/Q LO signals are generated by a two-stage polyphase filter, and each LO path is amplified by a two-stage driving amplifier. In the RF path, the up-converted signal is amplified by a three-stage driving amplifier. Even though the LO and RF driving amplifiers were designed for a 45/94-GHz dual-band operation, the 45-GHz operation (only) is demonstrated in this work.

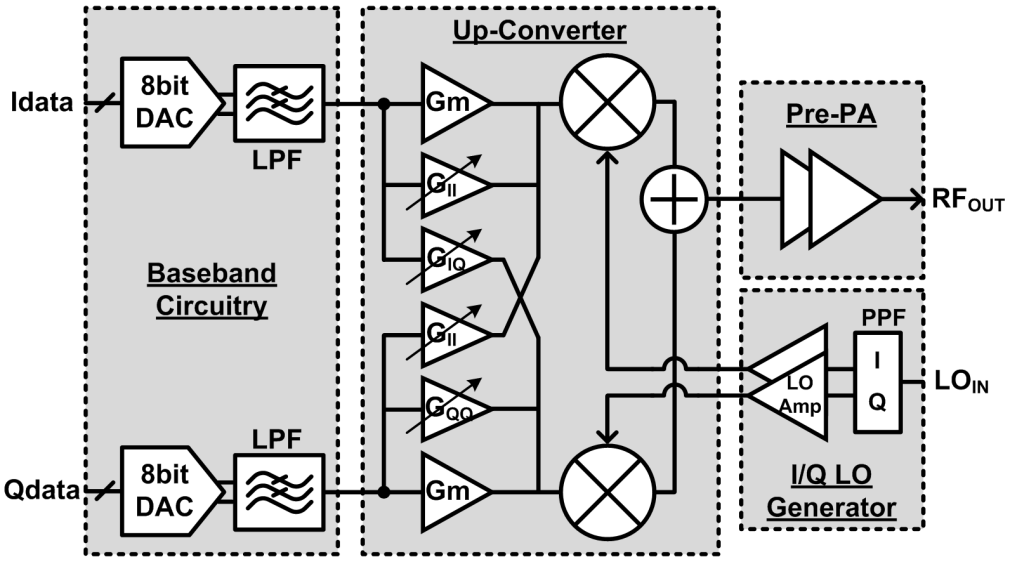
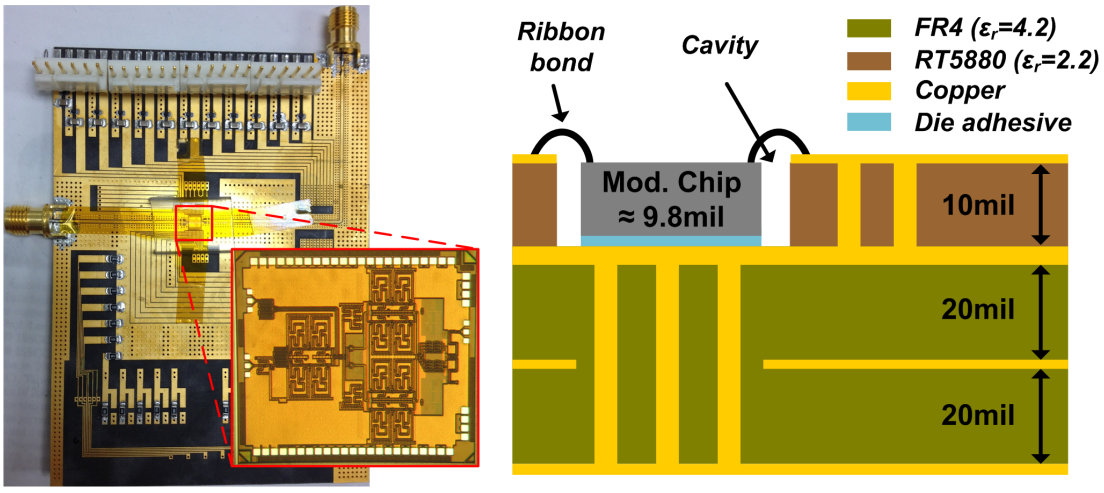


Figure 3.3: Block diagram of the 45-GHz direct-conversion I/Q modulator .

The I/Q modulator chip is fabricated in a 120-nm SiGe BiCMOS process and occupies an area of 2.5×2.2 mm^2. The chip is mounted on a PCB and all of the signals, including digital data, dc biases, LO and RF signals, are wire-bonded to this four-layer board. As shown in Fig. 3.4(a), $Z_o = 50\,\Omega$ stripline transmission lines are designed on a PCB to carry the high-speed digital data and



(a) (b)

Figure 3.4: 45-GHz I/Q modulator packaging: (a) Chip-on-board assembly photo. (b) PCB cross-section view.

clock. The digital data and clock are routed on the third layer with the standard FR-4 dielectric ($\varepsilon_r = 4.2$) and are picked up by an FMC LPC connector at the back side of the PCB. The static I/Q correction is also controlled through the FPGA in this experiment for easier programming. Since the FR-4 substrate becomes excessively lossy for signals above 10 GHz, the 45-GHz LO and RF traces are designed as GCPW structure and rout on the top layer of the PCB with RT5880 dielectric ($\varepsilon_r = 2.2$), as the cross-section view in Fig. 3.4(b). The chip is placed in a cavity, whose depth is close to the chip thickness, to minimize the inductance of LO and RF ribbon bonds. Figure 3.5 is the measured RF output power from the PCB comparing to the power directly probed on the chip. The RF bond wire, GCPW transmission line, and the 2.4-mm coaxial connector cause the total 0.9-dB insertion loss. This I/Q modulator chip-on-board assembly provides 5.8-dBm maximum output power at 45 GHz with high linearity.

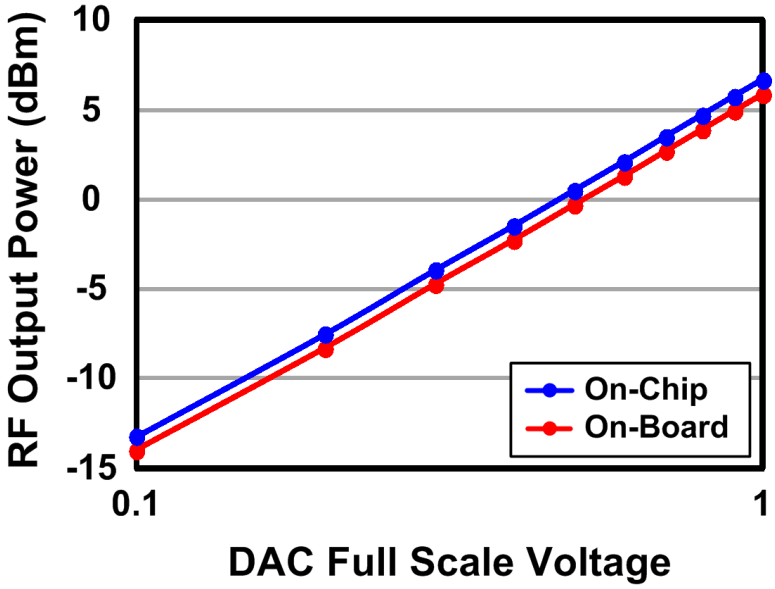


Figure 3.5: Measured RF insertion loss from the 45-GHz I/Q modulator chip to the PCB.

3.2.3 45-GHz PA/Antenna Array

The PA array chip comprises a three-stage amplifier system at 45 GHz [21]. Figure 3.6 shows the block diagram of the PA/antenna array system. The first stage is the primary amplifier driver, which is followed by a Wilkinson-based power splitter, and feeds the secondary driving amplifiers. The secondary drivers then feed the final power splitters as well as transformer-type single-ended-to-differential networks to the two-by-two pseudo-differential final PAs. The pseudo-differential PA outputs are coupled by flat ribbon bonds to two-by-two differential patch antennas, which is fabricated on the accompanying PCB. On-chip ground–signal–signal–ground (GSSG) pads as well as ribbon-bond impedances were taken into account in the antenna design such that each single-ended PA presents 50-Ω impedance at the output. All the antenna units are designed to radiate in-phase. The single-ended chip input is also ribbon-bonded to the PCB. The on-board input matching network is designed for the maximum power delivery to the chip.

The stacked-FET technique is widely used in SOI CMOS process to in-

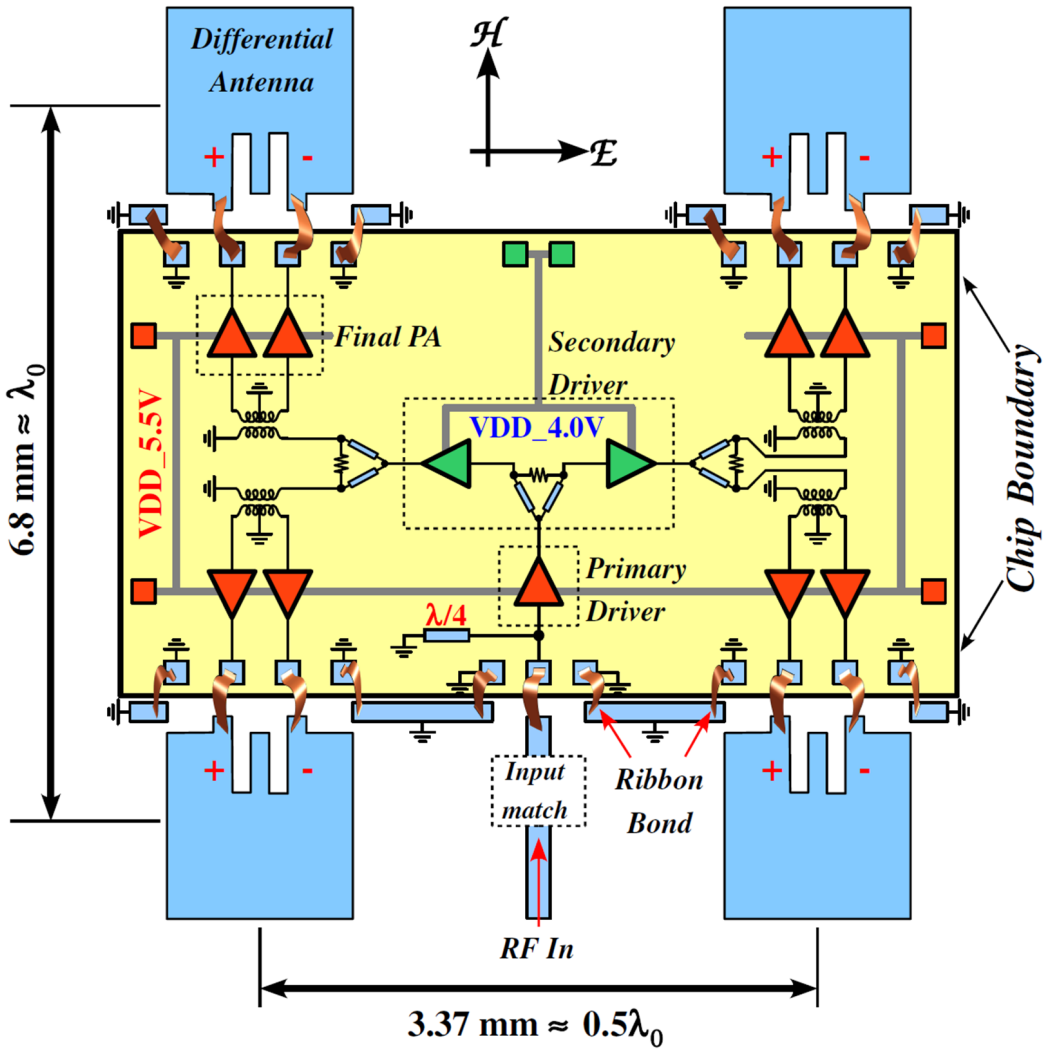
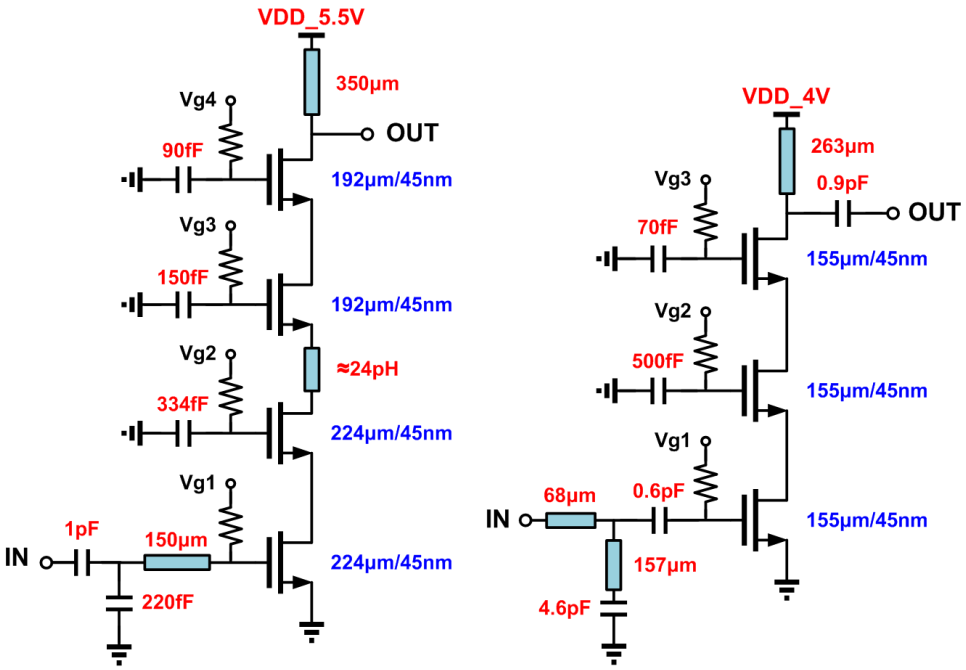


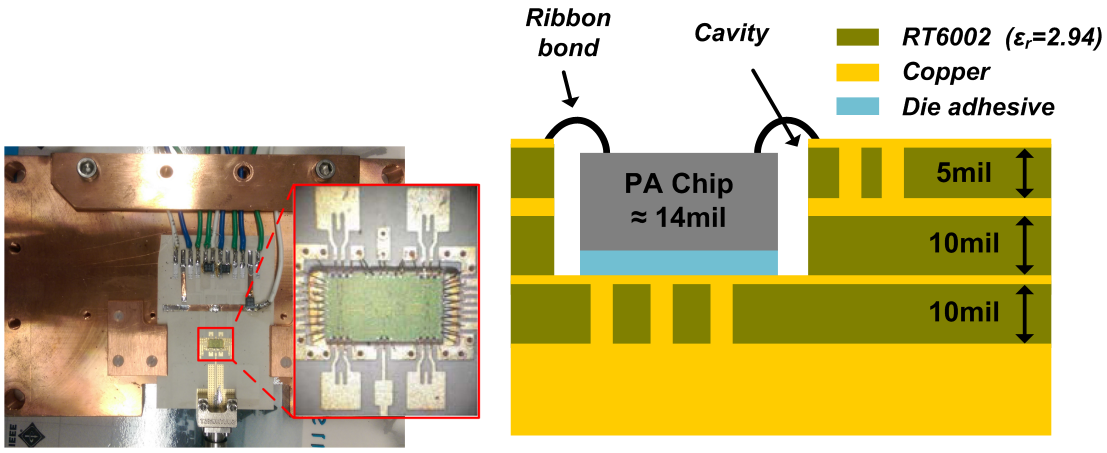
Figure 3.6: Simplified 45-GHz two-by-two PA/antenna array block diagram.

crease the output power since stacking FETs allows the amplifier to operate at a higher supply voltage [50]. By allowing finite voltages at the gate of stacked FETs using finite gate capacitors, the device breakdown issue is avoided and a reliable operation is allowed at a high supply voltage. The primary driver and each of the single-ended final PA are designed as four-stacked amplifiers for high gain and high $Psat$, respectively. As shown in Fig. 3.7(a), the four-stacked amplifiers operates from a 5.5-V supply, while each FET is biased at 1.36 V. 50-Ω input and output impedances are designed for characterizing the performance of the stand-alone amplifiers. All transmission lines shown in Fig. 3.7 are GCPW-based. The four-stacked amplifiers are designed to deliver above 20-dBm $Psat$ with greater than 10-dB gain at 45 GHz. The secondary drivers are designed as three-stacked amplifiers driving from a 4-V supply to save dc power, as shown in Fig. 3.7(b). Each three-stacked amplifier delivers 19-dBm $Psat$ with 8-dB gain at 45 GHz from simulation.



(a) (b)

Figure 3.7: Schematic of the PA cells. (a) Four-stacked amplifier for the primary driver and final PAs. (b) Three-stacked amplifier for the secondary drivers.

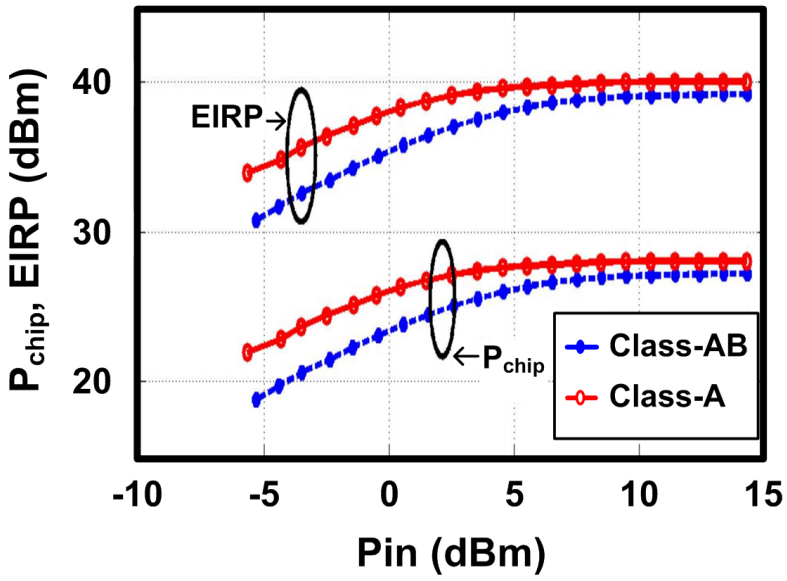


(a) (b)

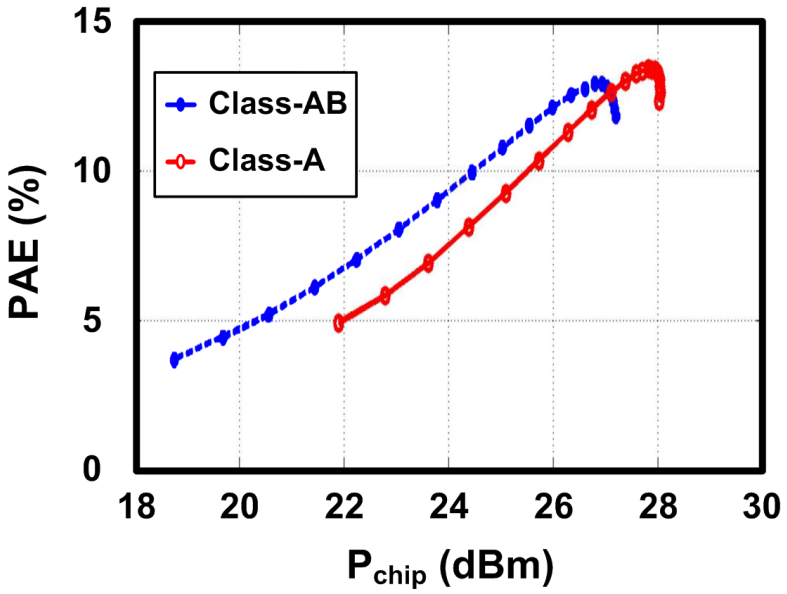
Figure 3.8: 45-GHz two-by-two PA/antenna packaging: (a) Chip-on-board assembly photo. (b) PCB cross-section view.

The two-by-two PA array chip is implemented in a 45-nm SOI CMOS processo and ccupies an area of 4.5×2.5 mm^2. The floating body of the SOI FETs takes the advantage of eliminating the body effect, which adversely impact the stacked-FET operation. As shown in Fig. 3.8(a), the PA array chip is mounted on a PCB with RT6002 dielectric ($\varepsilon_r = 2.94$), and the antenna array is fabricated on this. The chip is also placed in a cavity to minimize the inductance of input ribbon bonds, as illustrated in Fig. 3.8(b). Due to space limitations, the antennas are spaced at around one wavelength on the H-Plane as shown in Fig. 3.6 and result in grating lobes. Thermal dissipation is a significant consideration since the two-by-two PA chip consumes a high dc power (∼5 W). A high thermal conductivity adhesive (K ≈60 W/mK) is used and the chip is mounted on a copper-block PCB for better heat sinking.

To measure the antenna gain accurately is difficult since the gain depends on the absorber placement and receiver antenna setup. The experimental antenna gain can be estimated to deviate from the simulated 11 dBi by ±1 dB. To provide a conservative estimate, 12-dBi antenna gain is used in this experiment. Equivalent isotropically radiated power (EIRP) is measured at the peak of the radiation



(a)



(b)

Figure 3.9: Measured two-by-two PA/antenna array at 45 GHz. (a) EIRP and estimated on-chip output power. (b) PAE versus the on-chip output power.

pattern. At a 5.5-V supply under class-AB biasing, the maximum 39-dBm EIRP can be measured, as shown in Fig. 3.9(a). The chip is also biased in class-A operation to boost the gain as well as the output power and a maximum 40-dBm EIRP is measured. The power generated from the chip, can be determined using $P_{chip} = EIRP - G_{Tx}$, where G_{Tx} is the transmitter antenna gain. The corresponding P_{chip} equates to 27 dBm for class-AB biasing and 28 dBm for class-A operation. The power-added efficiency (PAE) is computed as $PAE = (P_{chip} - P_{in})/P_{dc}$. The peak PAE is $l3.5\%$ for class-A operation and $l3\%$ for class-AB operation, as shown in Fig. 3.9(b). In back-off region, the PAE in class-AB operation is as expected to be higher than in class-A.

3.2.4 45-GHz Experimental Results

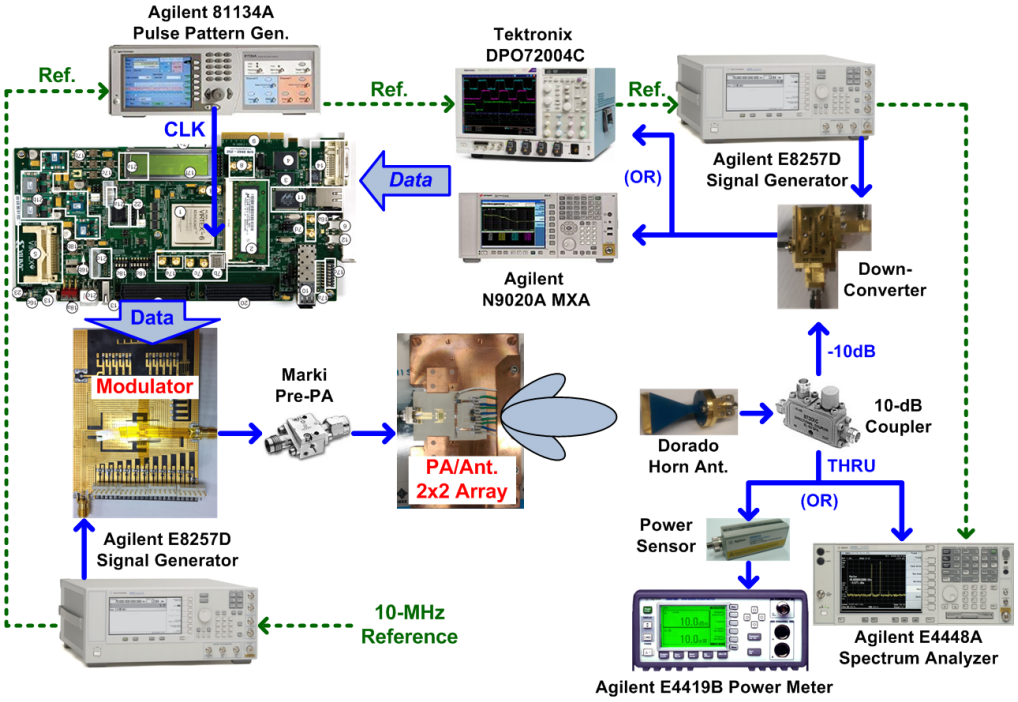


Figure 3.10: 45-GHz transmitter measurement setup.

The 45-GHz transmitter measurement setup is presented in Fig. 3.10. The digital data and the clock are provided to the I/Q modulator PCB through the

Xilinx ML605 FPGA. An Agilent 81134A pulse pattern generator supplies the clock to the FPGA so that all the frequencies in this testbench can be synchronized by a 10-MHz reference. An Agilent E8257D signal generator externally provides a 45-GHz LO carrier to the I/Q modulator to modulate the I/Q data to 45 GHz to the PA/antenna array. The 45-GHz radiated signal received by a Dorado Q-band horn antenna can be directly measured the power by a power sensor or analyzed by a spectrum analyzer. Even if the Agilent E4448A spectrum analyzer can demodulate the 45-GHz signal directly, it is preferable to down-convert the received signal to a lower frequency since the Agilent E4448A is limited by an internal bandwidth of 10 MHz. Another Agilent E8257D provides a 43.8-GHz LO to the external down-converter. The down-converted 1.2-GHz DPD reference signal is then demodulated by an Agilent N9020A MXA or a Tektronix DPO72004C oscilloscope. The resulting data analysis and DPD are processed in Matlab [51]. The predistorted data are then downloaded to the FPGA and resent to the I/Q modulator to linearize the Si/SiGe transmitter.

With a 75-MHz clock, the DPD signal is limited in a 25-MHz bandwidth. Figure 3.11 presents the 64-QAM, 25-Ms/s measurement results, where a raised cosine filter is applied on the I/Q data. In this measurement, the DPD reference signal is sampled and demodulated by the Tektronix DPO72004C oscilloscope. The AM–AM, AM–PM distortions, LO leakage and I/Q errors are calibrated by the DPD, and the EVM is improved from 20.4% to 3.68%. The baseband spectrum also shows that the transmitter initially introduces significant LO leakage and nonlinear distortion, however, the DPD compensates these errors and achieves a better adjacent channel power ratio (ACPR).

The Tektronix oscilloscope has 20-GHz bandwidth, however, the amplitude resolution is only 8-bit, so the quantization noise limits the performance. Figure 3.12 presents a 9.375-Ms/s, 256-QAM constellation measured with the Agilent N9020A MXA, which has 12-bit amplitude resolution, and an analysis bandwidth of 25 MHz. With this internal filter, the out-of-band nonlinearity cannot be completely captured, therefore the nonlinearity terms cannot be calibrated beyond the filter's edge of ± 12.5 MHz. However, most of the out-of-band nonlinearity as well

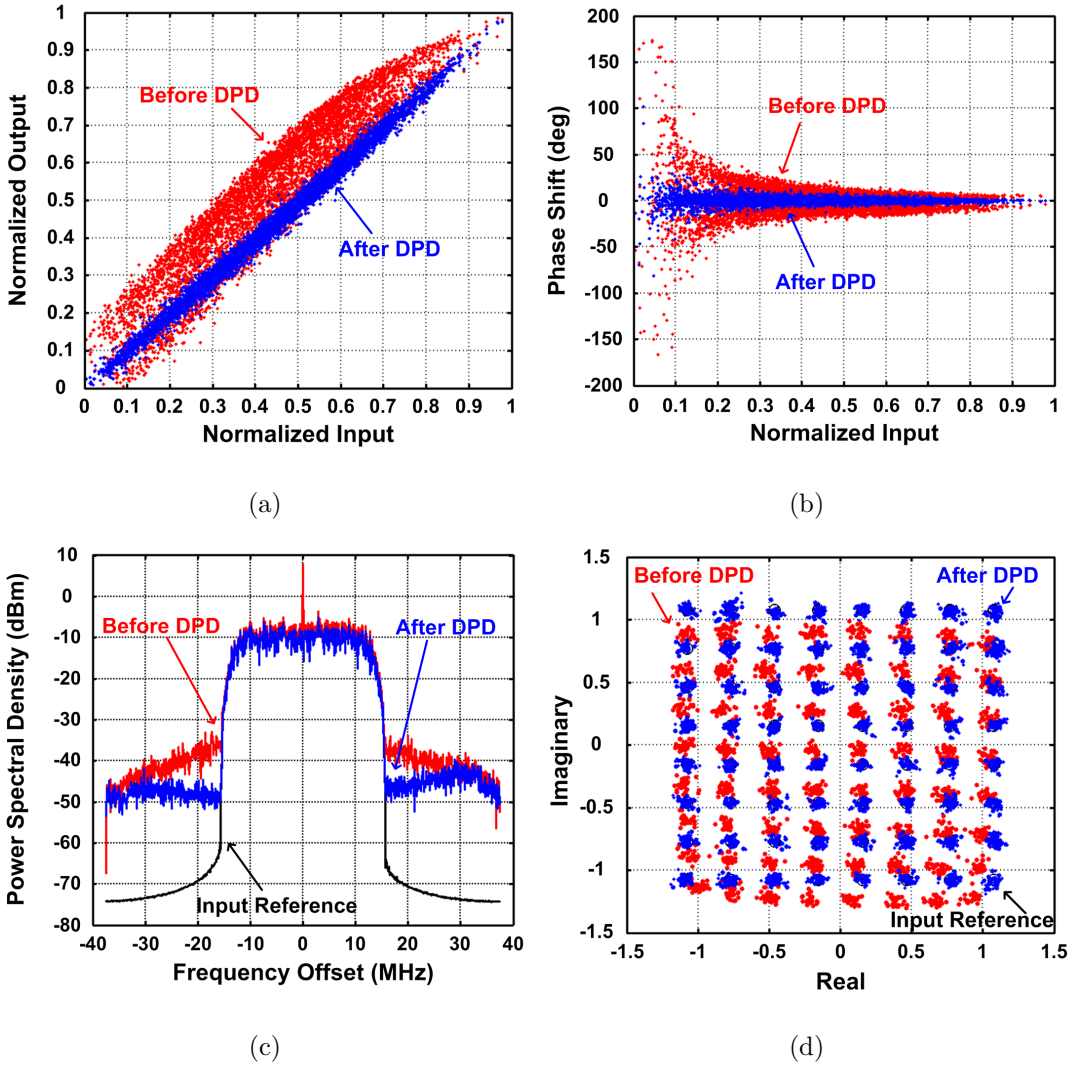


Figure 3.11: Measured 64-QAM at 25-Ms/s. (a) AM–AM, (b) AM–PM, (c) constellation, and (d) baseband spectrum.

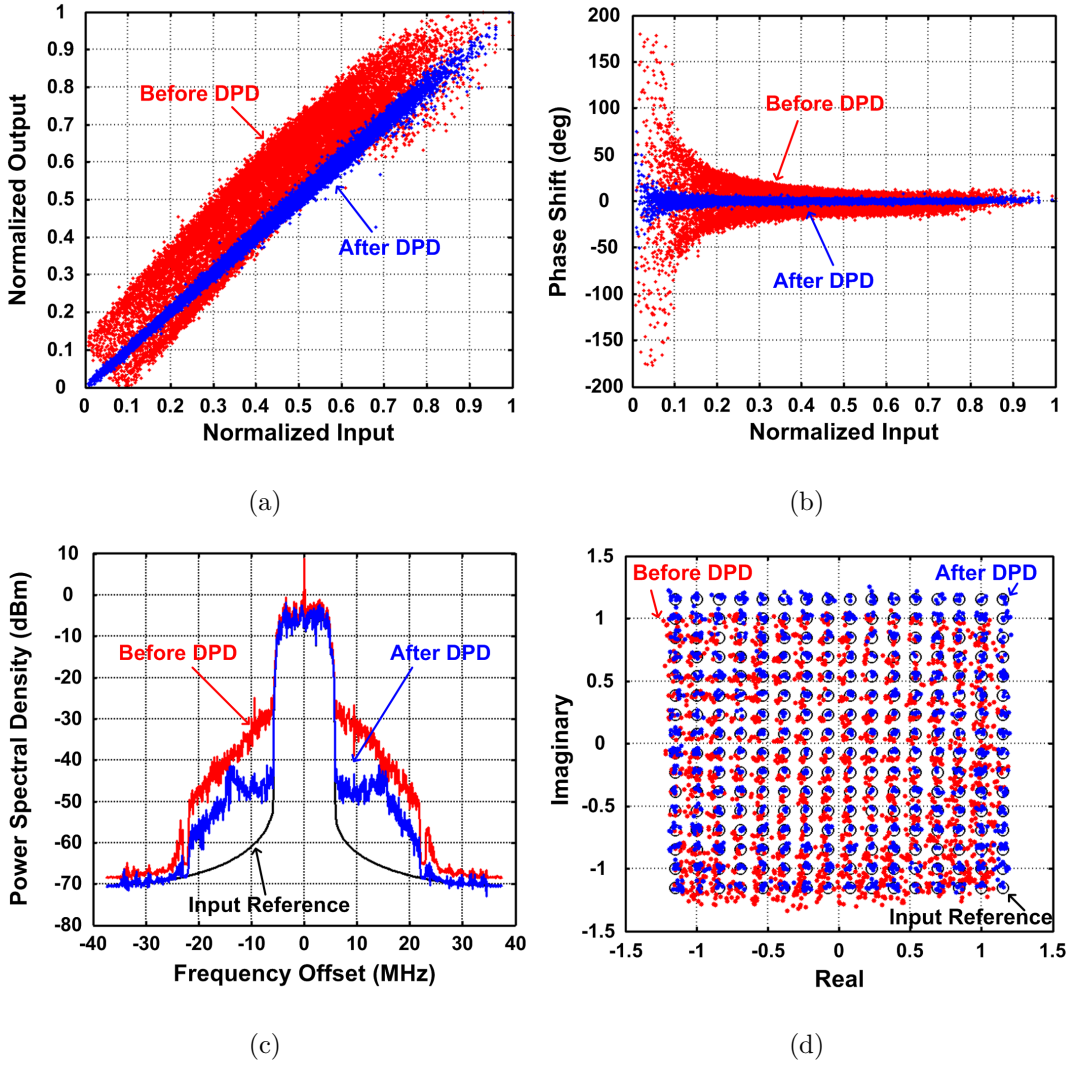


Figure 3.12: Measured 256-QAM at 9.375-Ms/s. (a) AM–AM, (b) AM–PM, (c) constellation, and (d) baseband spectrum.

as the LO leakage are still well predistorted, thus the EVM can be improved from 19.7% to 2.67% by the DPD.

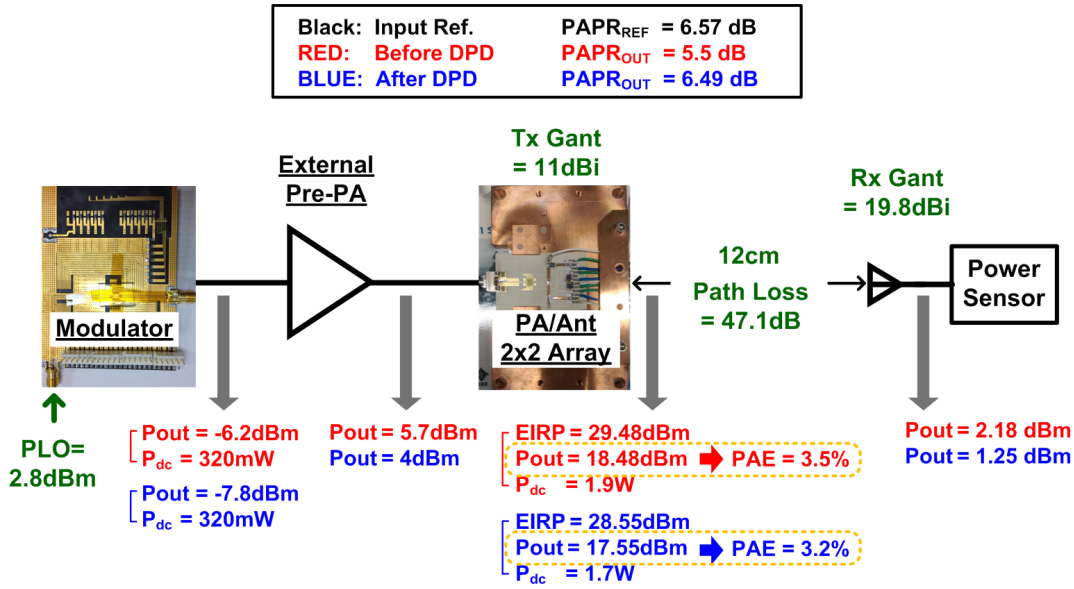


Figure 3.13: Measured 45-GHz power and PAE at each node for 9.375-Ms/s, 256-QAM data.

A 29.5-dBm average EIRP is measured from the two-by-two PA/antenna array. The 11-dBi experimental antenna gain is estimated in this measurement, therefore an average 28.5-dBm output power can be found from the PA array chip. From the continuous-wave measurement presented in Section 3.2.3, 25-dBm OP_{1dB} and 11% PAE at OP_{1dB} are measured from the chip. With the modulated signal, the PA provides 18.5-dBm average power and the average PAE is 3.5% as expected from the back-off in class-AB operation, as Fig. 3.9(b) shows. After DPD, 28.6-dBm average EIRP, 17.6-dBm average on-chip output power, and 1.7-W dc power are measured from the two-by-two PA/antenna array, so the average PAE drops to 3.2%. The PAE drop is mainly from the LO leakage cancellation and the gain back-off in the power back-off region. The measured peak-to-average power ratio (PAPR) is 5.5 dB before DPD and is recovered to 6.49 dB, which is close to the input reference PAPR of 6.57 dB. The power consumption of the I/Q modulator is 322 mW. The measured power values at each node for the 9.375-Ms/s, 256-QAM

scheme are illustrated in Fig. 3.13.

3.3 A 94-GHz Transmitter Utilizing DPD

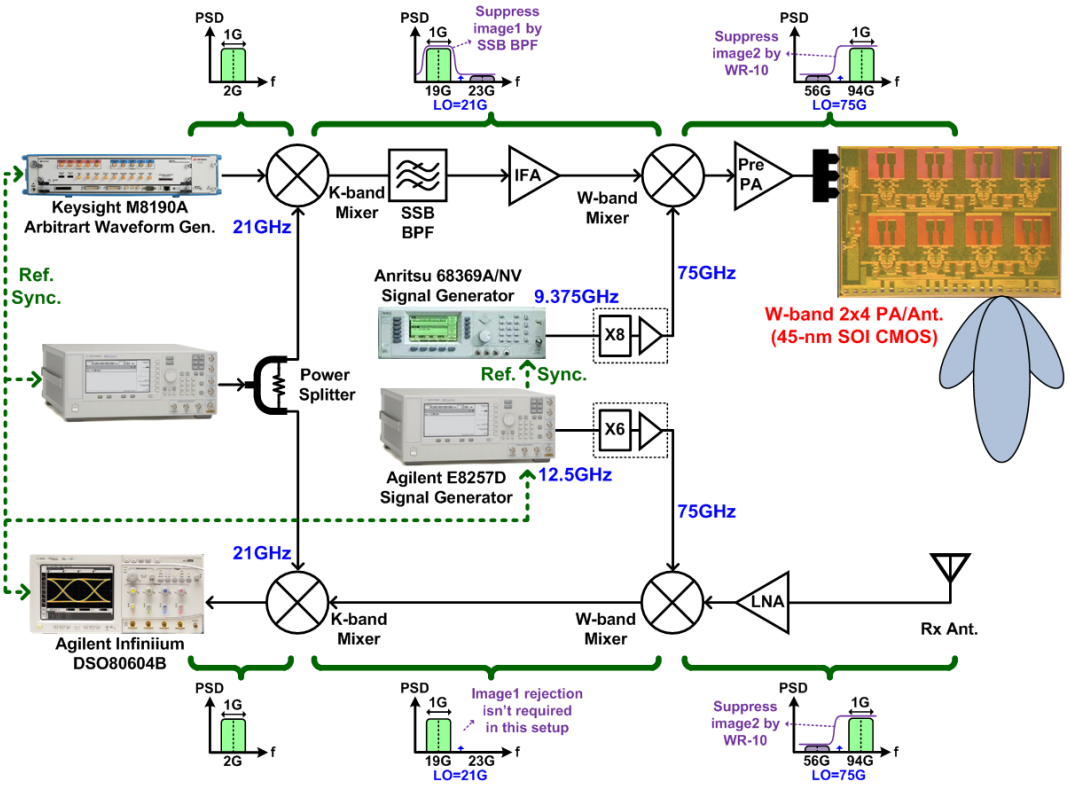


Figure 3.14: 94-GHz transmitter measurement setup.

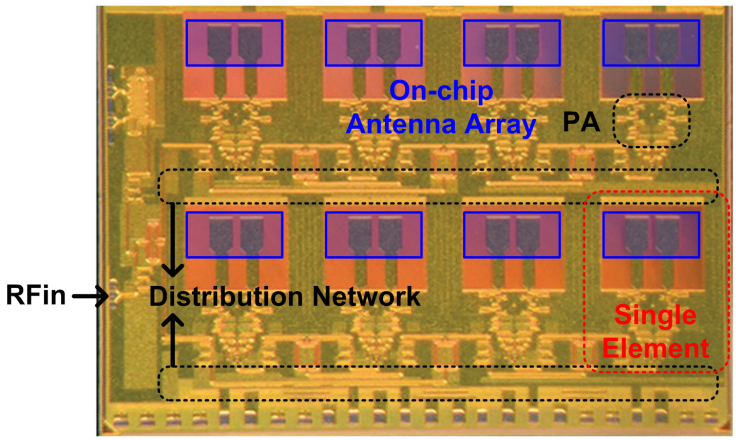
This section describes a 94-GHz (W-band) transmitter system that achieves multiple Gigabits-per-second data rate utilizing DPD. Figure 3.14 illustrates the system architecture, measurement setup and frequency plan. The I/Q data are modulated to a 2-GHz first IF band in digital domain through the Matlab. A Keysight M8190A arbitrary waveform generator (AWG) provides the 2-GHz modulated signal to a Quinstar 19-GHz (K-band) up-conversion mixer, where the LO frequency is fixed at 21 GHz. A single-sideband (SSB) bandpass filter is placed at the mixer RF port to pass the desired 19-GHz sideband and suppress the 23-GHz image as well as the LO leakage. A Marki A-2050 amplifier, which has ∼20-dB

gain at the second IF of 19 GHz, is used to compensate the conversion loss from the K-band mixer and the SSB filter. A Quinstar W-band balanced mixer up-converts the signal from 19-GHz to 94-GHz with a 75-GHz LO. The RF and LO ports of the W-band mixer are both implemented in a WR-10 waveguide flange, which has a 59-GHz TE_{10}-mode cutoff frequency [52], so the 56-GHz image can be suppressed. A Millitech gallium nitride (GaN) PA is used as the driver to produce high power in W-band to the final two-by-four PA/antenna array chip [2]. The PA/antenna array chip is implemented in 45-nm SOI CMOS process and radiates high power by using the spatial power combining technique.

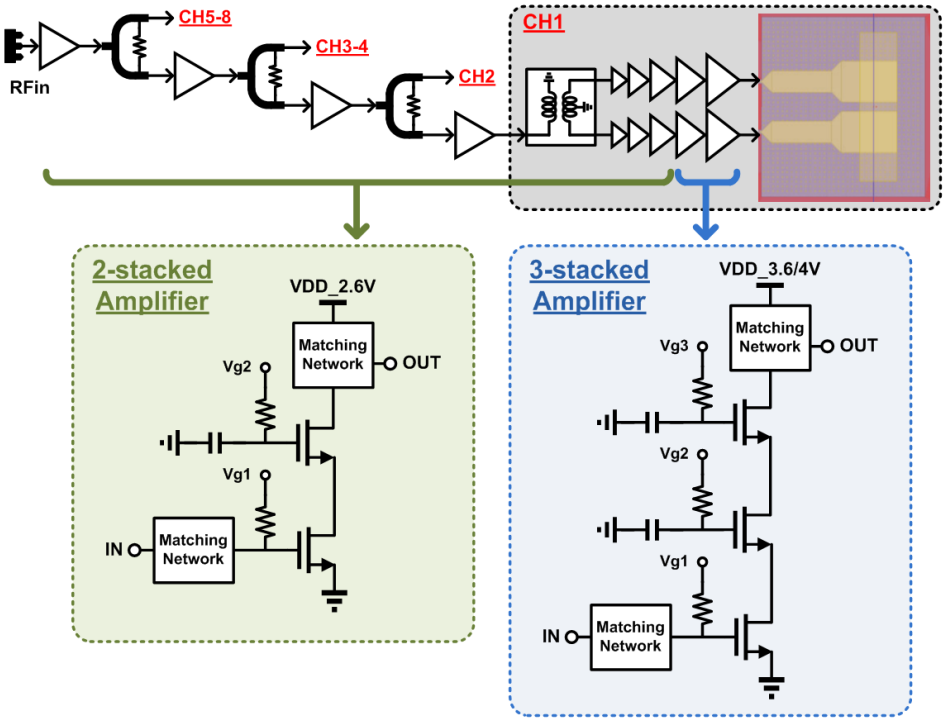
At the receiver side, a CMI conical horn antenna is placed to capture the radiated signal W-band. A Millitech LNA, which has ∼30-dB gain and ∼6-dB NF, amplifies the received signal and reduces the noise contributions from the later stages. Similar to the transmitter, another Quinstar W-band balanced mixer down-converts the signal from 94 GHz to 19 GHz band by applying a 75-GHz LO. The 19-GHz IF signal is further down-converted by a Quinstar K-band mixer to the 2-GHz band with a 21-GHz LO. The resultant 2-GHz signal is captured from an Agilent Infiniium DSO80604B oscilloscope and digitally demodulated through the Matlab. The 21-GHz LO is generated from an Agilent E8257D signal generator and is split for both the transmitter and receiver K-band mixers. The 75-GHz LO signals for the W-band mixers are generated through different multiplier chains due to the power requirements of the mixers (each mixer requires ∼10-dBm LO power) and the setup flexibility. The LO of the transmitter W-band mixer is provided from a Anritsu 68369A/NV signal generator at 9.375 GHz and multiplied by eight through a VDI multiplier chain to 75 GHz. The LO of the receiver W-band mixer is provided from another Agilent E8257D signal generator at 12.5 GHz and multiplied by six through another VDI multiplier chain to 75 GHz.

3.3.1 PA/Antenna Array Chip

The two-by-four PA/antenna array chip [2] is implemented in 45-nm SOI CMOS process and occupies an area of 5.95×4.38 mm^2 as shown in Fig. 3.15(a). A one-to-eight active distribution network delivers the input to the eight-channel

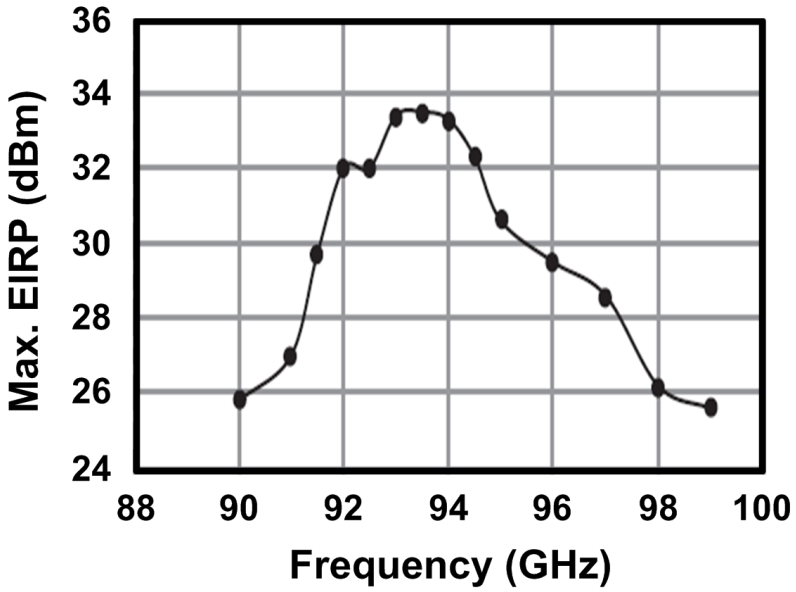


(a)

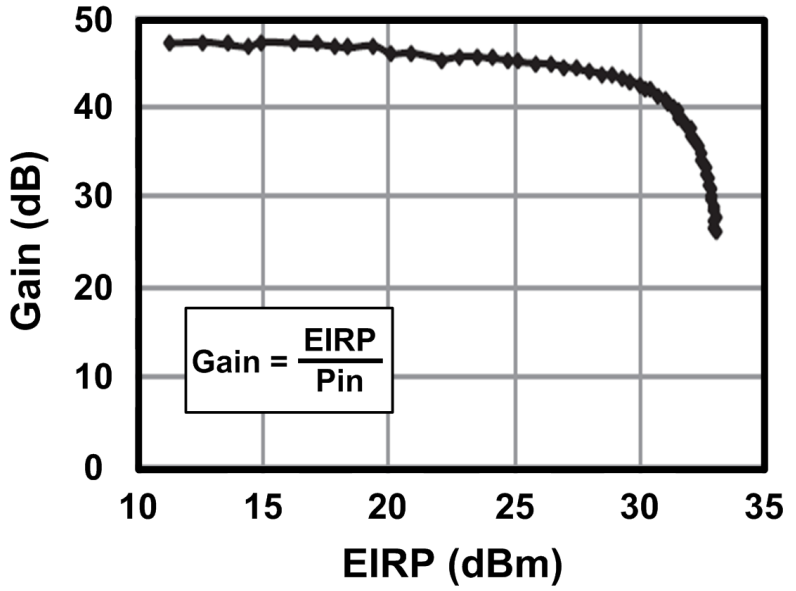


(b)

Figure 3.15: (a) Chip microphotograph of the two-by-four PA/antenna array. (b) Block diagram of the single chain.



(a)



(b)

Figure 3.16: Measured two-by-four PA/antenna array in W-band. (a) Maximum EIRP versus frequency. (b) Power gain versus EIRP.

pseudo-differential PAs. The outputs of the PAs are electromagnetically coupled to an array of high-efficiency differential microstrip antennas on a quartz wafer on top of the chip. The antennas are spaced at approximately half wavelength. As the single-chain block diagram shown in Fig. 3.15(b), three-stage Wilkinson dividers split the input signal to the eight channels. To compensate the losses from the routing and power splitting, two-stacked driving amplifiers are added between each stage. Each channel consists of a five-stage pseudo-differential PA. The first three stages are also two-stacked amplifiers and the final two stages are three-stacked PAs.

For the spatial power-combining in W-band, an on-chip microstrip antenna array is used in this design. The antenna structure employs differential feed lines on the top metal layer of the chip and the fields are coupled to the antenna through a thick quartz substrate. The chip is mounted on a copper-block PCB for better heat sinking. The radiated power is measured by a W-band conical horn antenna, which has 22-dBi antenna gain and is placed at the far field of 25 cm above the chip. The PA/antenna array chip achieves a maximum EIRP of 33 dBm at 94 GHz. Due to the limitation of the antenna pattern measurement setup, the transmitter antenna gain is estimated to be 9 dB from the HFSS [53] simulation. Therefore the $Psat$ from the two-by-four PA array into the antenna grid can be obtained as 24 dBm (250 mW). More than 9-W dc power consumption lead to a 2% efficiency for the whole chip. Figure 3.16(a) shows that greater than 30 dBm maximum EIRP is measured from 91 to 95 GHz. Figure 3.16(b) shows more than 45-dB small-signal power gain at 94 GHz can be achieved, where the gain is defined as the ratio of the EIRP to the input power to the chip.

3.3.2 Memory Polynomial for Wideband Signals

The bandwidth of the 94-GHz transmitter system is determined by the SSB bandpass filter, which has ∼1-GHz bandwidth from 18.5 to 19.6 GHz. As the standalone K-band SSB mixer testing shown in Fig. 3.17, ∼5-dB conversion loss can be found in the passband while the image and the LO leakage are suppressed to >40-dBc lower than the passband. However, to suppress the 21-GHz LO leakage

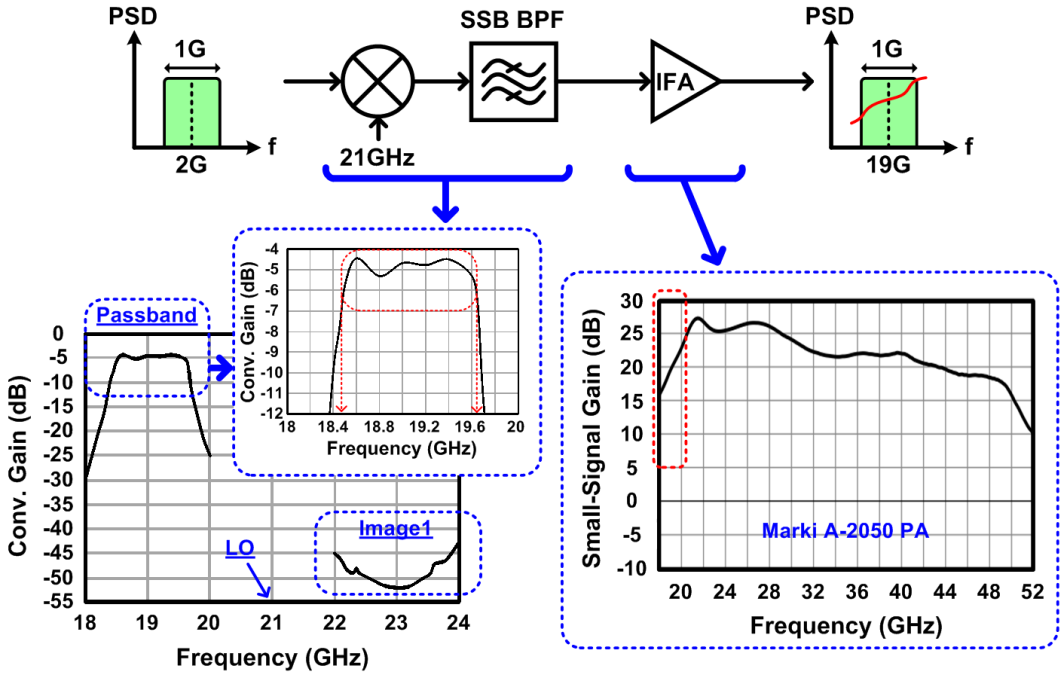


Figure 3.17: Frequency response in the 19-GHz band.

and the image in 23-GHz band, the SSB filter is design as a high-order bandpass filter and results in ∼2-dB gain ripple in the passband. Furthermore, the Marki A-2050 amplifier provides ∼20-dB gain in 19-GHz band but performs a high-pass frequency response. For a low-bandwidth signal, the gain variation issue is insignificant. However, this results in severe memory effects for a wideband signal and must be equalized. For instance, a memory depth (M) of 7 is sufficient to a 20-Ms/s QAM signal based on measurement. A 250-Ms/s signal requires $M \approx 100$ to equalize the memory effects. The MPM in (3.14) includes the memory effect terms of M, however, the computation of the M in conjunction with the harmonic terms (K) results in huge numbers of MPM coefficient, i.e. $K \cdot M$ numbers of $c_{m,k}$. The huge numbers of $c_{m,k}$ significantly make the computation inaccurate and consume huge memory in the DPD processor.

In order to improve the accuracy and reduce the DPD complexity, the equalization function is separated from the MPM as Fig. 3.18 illustrates. The equalizer is implemented by a digital finite impulse response (FIR) filter, which

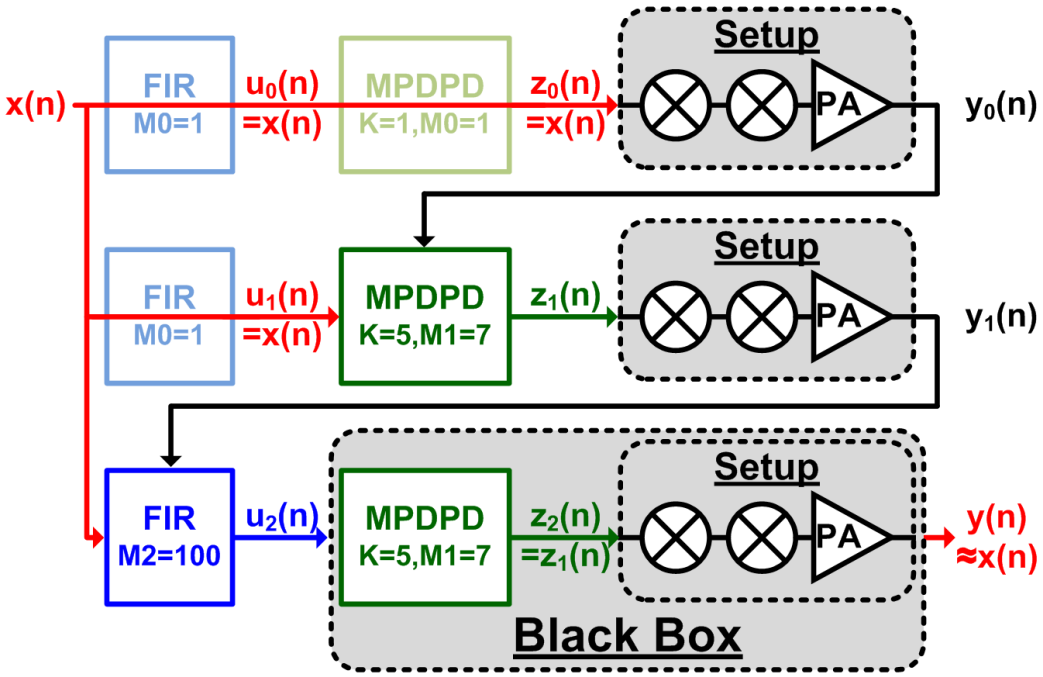


Figure 3.18: Proposed DPD algorithm with equalization.

impulse response can be represented as

$$u(n) = \sum_{m=0}^{M-1} a_m x(n-m). \tag{3.19}$$

where a_m are the FIR coefficients and the $M-1$ pass points are taken into account for a causal system. The MPM in (3.14) is rewritten and relabeled for clarification as

$$z(n) = \sum_{m=0}^{M-1} \sum_{k=1}^{K} b_{m,k} u(n-m) |u(n-m)|^{k-1}. \tag{3.20}$$

where $b_{m,k}$ are the MPM coefficients, K is the maximum harmonic order, and M is the memory depth. It is note that the input references $x(n)$, FIR outputs $u(n)$, transmitter inputs $z(n)$, and the PA outputs $y(n)$ are baseband I/Q complex envelopes.

The first step of DPD is to send an input reference $x(n)$ to the transmitter input. It can be realized by nominating $a_{FIR} = [1, 0, 0, \cdots]$ and $b_{MPM} = [1, 0, 0, \cdots]$, so that the FIR output $u_0(n)$ and the transmitter input $z_0(n)$ are

equal to $x(n)$. Based on the resultant nonlinear and unequalized PA output $y_0(n)$ and the input reference $x(n)$, the MPM coefficients $b_{MPM} = [b_1, b_2, b_3, \cdots]$ and the predistorted transmitter input $z_1(n)$ can be obtained, where a reasonably small $M1$ can be chosen. The second step is to send the predistorted $z_1(n)$ to the transmitter and capture the linear but unequalized PA output $y_1(n)$. Based on the $y_1(n)$ and the $x(n)$, the FIR coefficients $a_{FIR} = [a_1, a_2, a_3, \cdots]$ and FIR output $u_2(n)$ are obtained, where the required memory depth $M2$ is employed. Since the nonlinearity terms have been predistorted, the final step is to send the $u_2(n)$ to the transmitter through the MPM, where the b_{MPM} were derived in the second step. Therefore, the final PA output $y(n)$ can be predistorted and equalized and results in a high ACPR and low EVM.

For instance, if 5 harmonic terms and 100 memories are required to model the transmitter system, i.e., $K = 5$ and $M = 100$, the number of coefficients is $M \cdot K = 500$ when the MPM (only) is adopted. With the separated FIR equalizer from MPM and choosing $K = 5$ and $M1 = 7$ for the MPM and $M2 = 100$ for the FIR filter, same harmonic terms and memory depth are modeled. The total number of coefficients can be reduced to $M1 \cdot K + M2 = 135$. Therefore, the proposed algorithm can greatly alleviate the complexity of computing the DPD coefficients.

In general, the signal in the IF stages, e.g. the SSB mixer or the IF amplifier, is relatively linear but has more gain variations due to the lower power and wider fractional bandwidth. On the other hand, the PA has higher distortions for the higher PAE but is less sensitive to the gain variation due to the lower fractional bandwidth. Therefore, it is desirable to distinguish the nonidealities and the memory effects from different stages and calibrate with different models.

3.3.3 94-GHz Experimental Results

The measurement setup of the 94-GHz transmitter is illustrated in Fig. 3.14. The Keysight M8190A AWG provides two channels of arbitrary waveform with a maximum 8-GSa/s sampling rate and 14-bit resolution. The Agilent Infiniium DSO80604B oscilloscope has a 20-GSa/s sampling rate when sensing two-

channel inputs and reaches 12-bit vertical resolution with averaging. The averaging function of the oscilloscope requires a periodic data frame. Therefore, one of the channels of the AWG is used to generate the 2-GHz I/Q modulated input to the transmitter and the other channel provides a triggering pulse to the oscilloscope directly to specify the length of the data frame. To handle DPD, the channel bandwidth must support three times the signal bandwidth to compensate at the very least the third-order nonlinearity causing compression. As described in Section 3.3.2, the bandwidth of the whole system is determined by the ∼1-GHz passband of the K-band SSB up-conversion mixer. Thus, the DPD signal is limited in a ∼330-MHz bandwidth. In this experiment, a 375-Ms/s I/Q modulated signal is used to reach a high data rate while sacrificing the out-of-band nonlinearity improvement at the edge of the channel bandwidth.

Figure 3.19 presents the 256-QAM, 375-Ms/s measurement results of the 94-GHz transmitter system, where a raised cosine filter is applied on the baseband I/Q data. Due to the strong gain ripple in the IF band as well as the two-by-four PA/antenna chip, $K = 5$ and $M1 = 50$ are chosen in the MPM. For the equalization, $M2 = 200$ is used in the FIR filter. As plotted in Fig. 3.19(a) and (b), MPDPD significantly improves the AM–AM and AM–PM distortions in high power region and most of the low power errors which are caused from memory effects. The FIR filter further calibrates the memory errors where the linearity is maintained. Figure 3.19(c) plots the demodulated spectrum in baseband to show the improvements of the DPD and equalization. Before applying DPD, the received signal has severe out-of-band distortion and in-band power variations. It results in the average of 25.4-dB ACPR with ±416-MHz frequency offset. By applying MPDPD, the out-of-band distortion is suppressed and the ACPR at ±416-GHz offset is improved to 31.5 dB. The in-band frequency response is also greatly equalized and the EVM is reduced from 43.5% to 7.65%, as the constellation diagrams shown in Fig. 3.19(d) and (e). By applying the FIR filter to equalize the residue in-band errors, the EVM is further improved to 2.52% and the out-of-band ACPR is kept in 31.8 dB as Fig. 3.19(c) and (f) show. A 256-QAM, 375-Ms/s signal is equal to 3-Gb/s data rate and the 2.5% EVM satisfies slightly higher than $< 10^{-6}$ BER

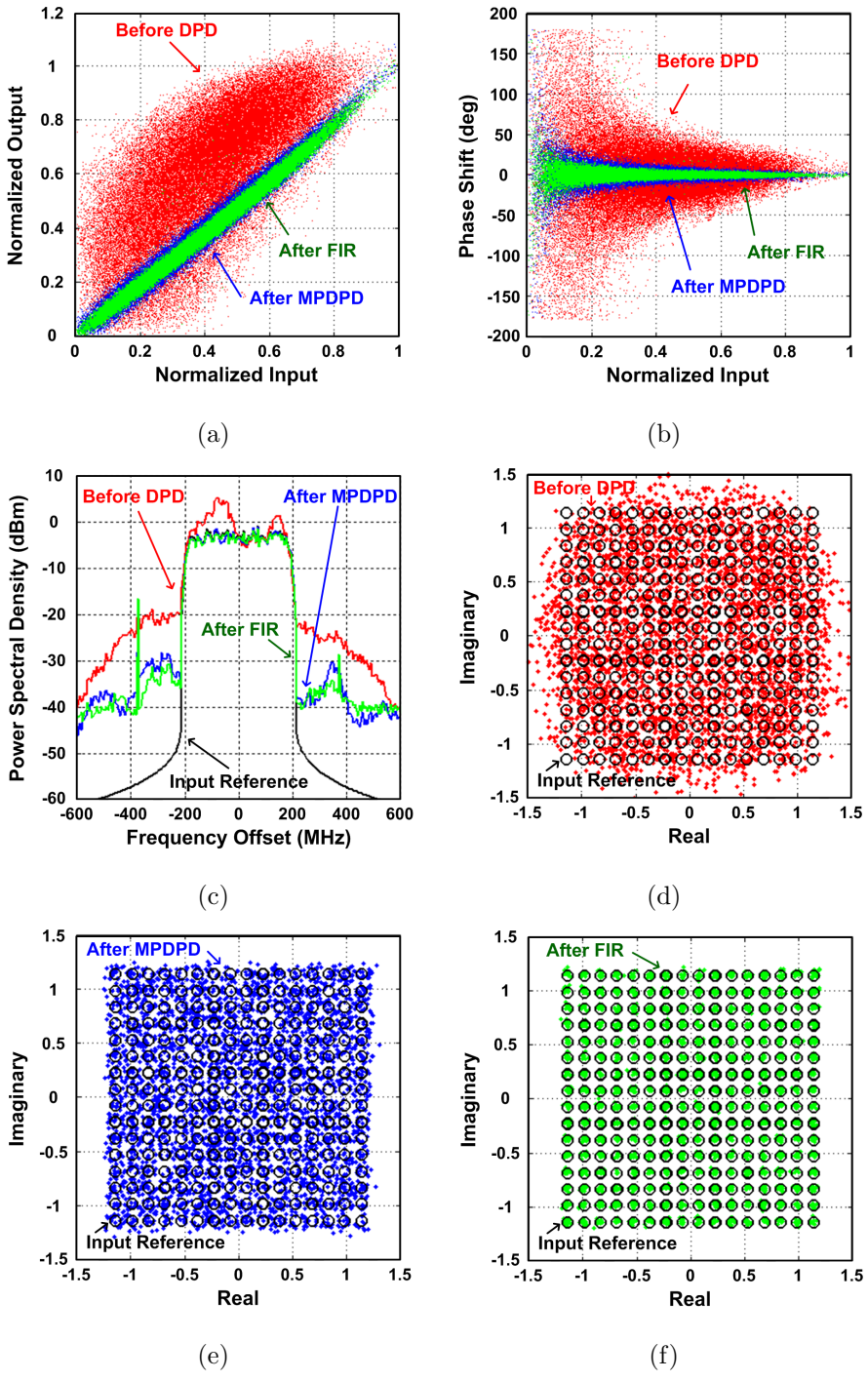


Figure 3.19: Measured 256-QAM at 375-Ms/s. (a) AM–AM, (b) AM–PM, (c) baseband spectrum, (d) constellation before DPD, (e) constellation after DPD, and (f) constellation after equalization.

according to Fig. 1.2.

3.4 Conclusions

This chapter presents two mm-wave transmitters utilizing DPD to compromise the linearity/efficiency trade-off. The Si/SiGe direct-conversion transmitter is demonstrated at 45 GHz with the two-by-two PA array (in 45-nm SOI CMOS), I/Q modulator (in 120-nm SiGe BiCMOS), and the DSP (through FPGA). Before DPD, the whole transmitter achieves 29.5-dBm average EIRP and 18.5-dBm on-chip average output power. After DPD, the whole transmitter achieves 28.6-dBm average EIRP and 17.6-dBm on-chip average output power. The EVM is significantly improved by DPD from 20.4% to 3.68% for a 64-QAM, 25-Ms/s signal and 19.7% to 2.67% for a 256-QAM, 9.375-Ms/s signal. The two-step frequency conversion transmitter is also demonstrated at 94 GHz with the two-bu-four PA/antenna array (in 45-nm SOI CMOS) and external mixers. With DPD, the EVM is significantly improved by the MPM from 43.5% to 7.65% for a 256-QAM, 375-Ms/s (3 Gb/s) signal. With the separate equalizer, the EVM is further improved by the FIR to 2.52%.

Acknowledgements

This chapter includes a reprint of the material as it appears in International Microwave Symposium, May 2015, P. Wu; Y. Liu; B. Hanafi; H. Dabag; P. Asbeck; J. F. Buckwalter. The 94-GHz transmitter demonstration that will be submitted shortly for publication. This dissertation author is the primary author of these materials. The authors are grateful to the DARPA LEAP for accessing to the IBM 8HP and 12SOI technology and the DARPA ELASTx program (Dr. S. Raman) and the U.S. Army Research Office (Dr. D. Palmer) for support. The authors would also like to thank Professor G. Rebeiz for his measurement support. Additionally, the support of the NSF is greatly appreciated.

Chapter 4

A 71–86-GHz Bidirectional Transceiver in 90-nm SiGe BiCMOS

4.1 System Considerations for E-band Transceivers

Both 77-GHz automotive pulse-compression radar (PCR) and the E-band (71–76/81–86 GHz) backhaul systems are compatible with bandwidth up to 2 GHz. While many state-of-the-art E-band systems use fixed high-gain antennas to satisfy the link budget requirements, significant commercial interest exists in scalable phased-array solutions that provide electronically controllable beamsteering. Consequently, recent works have investigated a number of beamforming architecture variations such as RF, LO, IF and baseband phase shifting [54, 55].

RF phase-shifting configurations typically consume moderate power and offer high linearity because the beam is formed before the mixer and only one LO signal is required in the transmitter (TX) or receiver (RX) [3, 56]. Since the phase shifters and the power combiners/splitters are operated at the RF band, the system budgets, in terms of gain, noise figure, and power would become more stringent. The LO and IF phase-shifting topologies avoid phase shifting in the RF

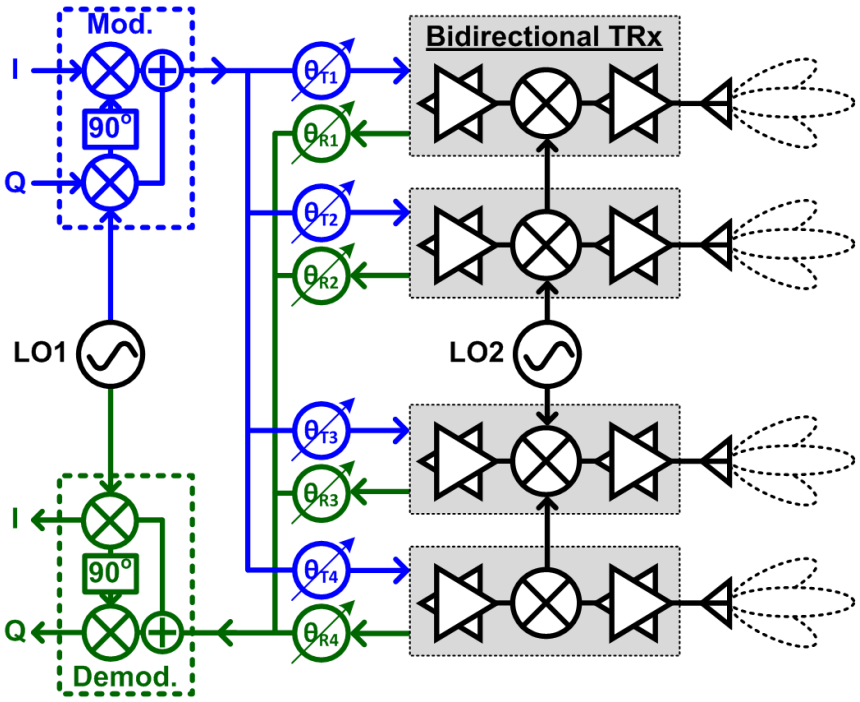


Figure 4.1: An IF-shifting phased-array transceiver system.

signal path [12, 55]. The main challenge of these approaches is the distribution of multiple LO signals with accurate phases at mm-wave bands with low skew between the channels. In addition, the LO spur could couple to the RF signal paths and result in signal distortion. Baseband phased-array architectures adjust the phase (delay) through digital signal processing and are flexible for multiple-input-multiple-output (MIMO) systems [57]. However, to implement a baseband-shifting system is still challenging even if in advanced technologies since multiple power-hungry and large dynamic range analog-to-digital converters (ADCs) and DACs are required to process a huge amount of data.

An IF-shifting phased-array system as shown in Fig. 4.1 is preferred because phase shifting occurs at a lower IF band. There are advantages and disadvantages to the aforementioned approaches, but IF phase shifting has the advantage of allowing the scaling of the number of array elements by adding separate transceiver chips and managing the beamforming at the IF frequency. This makes the implementation of the phase shifters at the IF band lower power and also allows for

the formation of multiple beams with multiple IF beamforming networks. However, the IF phase shifting requires a heterodyne transceiver architecture with image rejection and requires both the LO and RF signals to split into in-phase and quadrature-phase (I/Q) [7]. In a phased-array system, each sideband suppression or image-rejection transceiver element not only increases the circuit complexity, but also generates different I/Q mismatch between each path. In this work, a frequency plan is proposed using a fixed LO to mitigate the image rejection while covering applications between 71 and 86 GHz. For 76 to 81 GHz automotive radar systems, the LO frequency is chosen at 68 GHz, so the image band is located in 55–60 GHz, which can highly attenuate the electromagnetic energy by atmospheric oxygen [58]. This suggests that the IF would range from 8 to 13 GHz for these radar systems. For an RF signal in 71–76 GHz band, the IF band is between 3 and 8 GHz. For an RF signal in 81–86 GHz, the IF band is between 13 and 18 GHz. The fixed LO architecture allows beamformers that could be implemented at different IF bands to cover different RF bands simultaneously.

In the TX mode, the RF output power is determined from

$$P_{Tx} = P_{IF} - 10\log_{10} N + G_{MIX} + G_{PA}, \tag{4.1}$$

where P_{IF} is the input IF power to an idealized IF beamformer with 0-dB gain, N is the number of phased-array elements, G_{MIX} is the mixer conversion gain, and G_{PA} is the PA gain. The minimum detectable signal (MDS) power level at the receiver is found from

$$MDS = -174(\text{dBm/Hz}) + 10\log_{10} BW + NF, \tag{4.2}$$

where BW is the signal bandwidth and NF is the receiver noise figure. Given a BW of 2 GHz and a 7-dB NF at 79-GHz band [59], MDS is –74 dBm. In the RX mode, the IF output power is determined from

$$P_{IF} = P_{Rx} + G_{LNA} + G_{MIX} + 10\log_{10} N, \tag{4.3}$$

where P_{Rx} is the received signal power and G_{LNA} is the LNA gain. Comparing (4.1) and (4.3), the power splitting and combining in the TX and RX mode is

compensated by asymmetric gain in each mode. It is desirable to compensate the power splitting in the TX mode with higher RF gain. To consider the advantages of asymmetric gain and where it should be applied, consider the linearity of the RX chain. The input-referred third-order intercept point (IIP_3) is determined from

$$\frac{1}{IIP_{3,Rx}} = \frac{1}{IIP_{3,LNA}} + \frac{G_{LNA}}{IIP_{3,MIX}}, \tag{4.4}$$

where $IIP_{3,LNA}$ and $IIP_{3,MIX}$ are the individual IIP_3 contributions of the LNA and mixer. This suggests that the $IIP_{3,MIX}$ should be higher than the $IIP_{3,LNA}$ by a factor of G_{LNA}. As a result, the asymmetric gain should be provided in the mixer for high linearity.

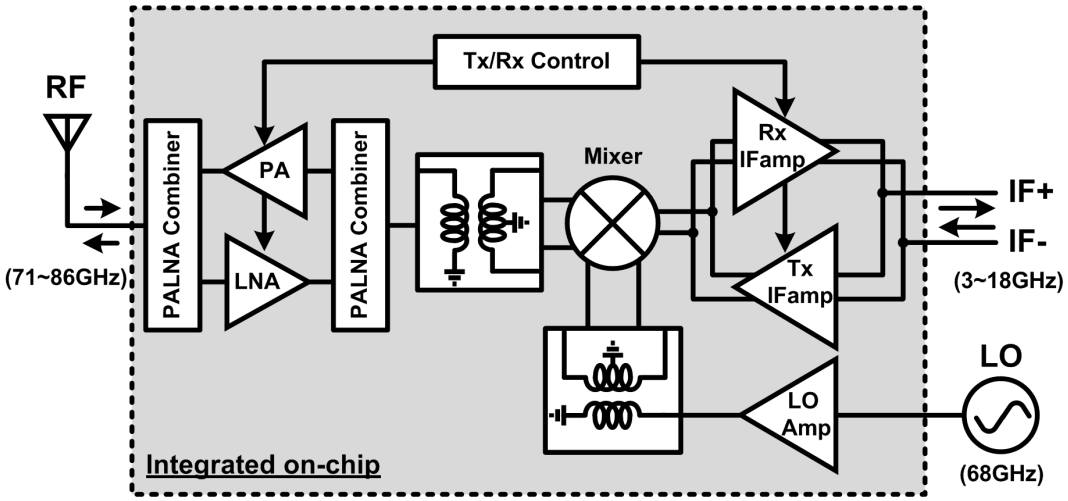


Figure 4.2: Proposed bidirectional transceiver block diagram.

Figure 4.2 shows the block diagram of the 71–86-GHz (E-band) bidirectional transceiver front-end. The input stage of the receiver is an LNA to amplify the signal received from the antenna while minimizing the noise contribution of the later stages. The output stage of the transmitter is a PA to produce high output power. The LNA and PA both share a common interface to the antenna port and mixer port. A bidirectional mixer driven by a fixed LO amplifier is followed by transmitter and receiver IF amplifiers.

There are two novel features in this work. First, we demonstrate the implementation of a low-loss transmission-line-based power splitting network that allows the LNA input and PA output to be combined into a single port. By exploiting impedance variations at the LNA input and the PA output, the transmission line lengths are chosen to isolate one or the other for half-duplex operation. Therefore, the PA/LNA combiner is proposed in this chapter to minimize the loading effect, while the PA/LNA is optimized with 50-Ω loads to a single antenna and the bidirectional mixer. Second, the implementation of the bidirectional mixer is asymmetric to give different conversion gain and linearity in the TX and RX modes. We demonstrate an asymmetric mixer that operates as either a passive or an active mixer depending on whether the circuit operates in TX or RX mode using the same mixer switches. The transmitter and receiver IF amplifiers compensate the conversion loss of the mixer and are also combined at the input and output. The input/output impedances of the turned-OFF amplifiers are high enough at IF frequency, therefore, switches or the proposed combiner are not required to isolate the loading between each other.

4.2 Circuit Implementations

4.2.1 90-nm SiGe BiCMOS Process

The 71–86-GHz bidirectional transceiver front-end is implemented in a 90-nm SiGe BiCMOS process with nine copper metal layers and one aluminum metal backend layer. A 4-μm intrinsic HBT transistor operates at peak f_T/f_{max} of 310/340 GHz at the bias current of 1.5–2.5 mA/μm as plotted in Fig. 4.3. The extrinsic model for the transistor incorporates the interconnection of the HBT transistor from M1 to the top copper layer (OL) where the GCPW lines are fabricated. Considering the extrinsic interconnect parasitics, the peak f_T/f_{max} drops to 280/320 GHz. The 50-Ω GCPW lines are shown in Fig. 4.4(a) and used in the PA/LNA combiners and the matching networks of the PA, LNA and the LO driver. The top and bottom ground planes on OL and M1_2B prevent coupling to other nodes in the circuit as well as the substrate. Electromagnetic simulation

using EMX [60] shows the 50-Ω GCPW lines have 0.57–0.67-dB loss per millimeter length between 70–90 GHz. Quarter-wavelength transmission lines demonstrate a quality factor (Q) of 19–24 as plotted in Fig. 4.4(b). In addition, metal-insulator-metal (MIM) capacitors (2.72 fF/μm^2) and vertical-natural (VN) capacitors (0.94 fF/μm^2) can be fabricated in the back-end-of-line of the process. The MIM capacitors are mainly used as decoupling capacitors at the supply lines due to the higher density and the lower Q, which helps the stability. In the signal paths, VN capacitors are chosen due to the higher Q and lower loss as plotted in Fig. 4.4(b).

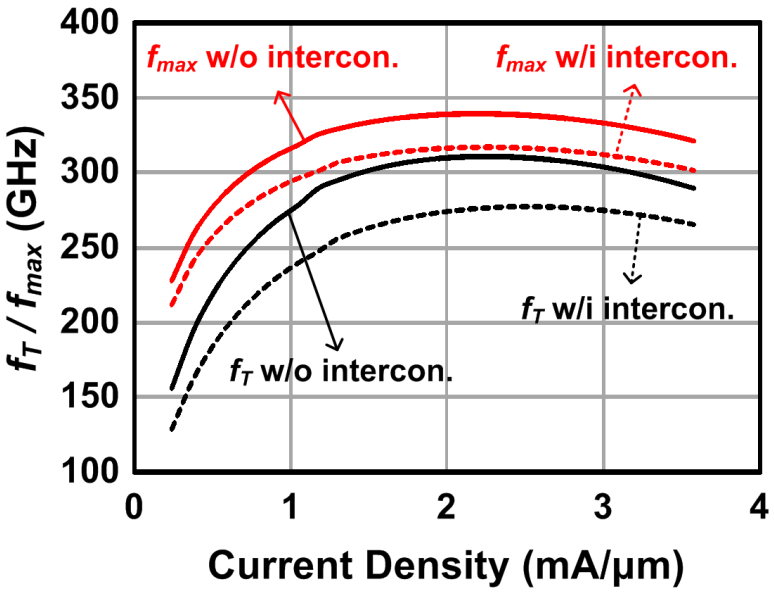
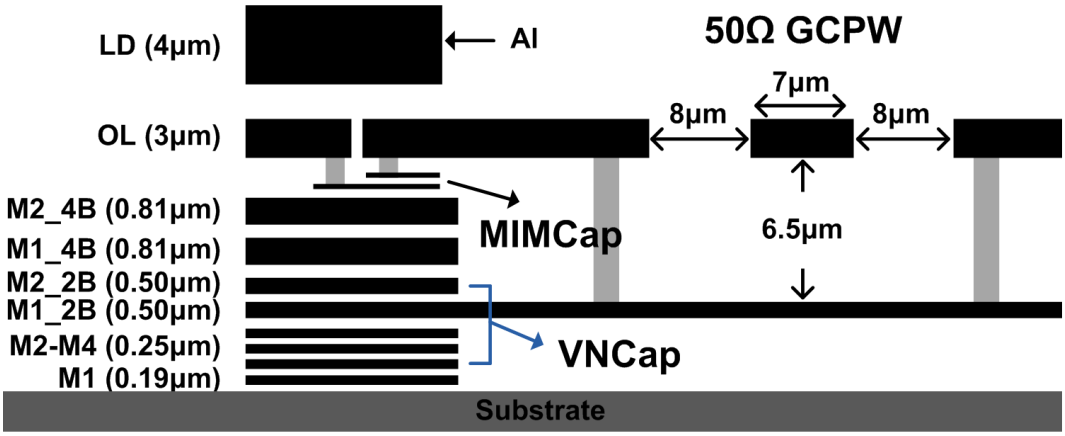


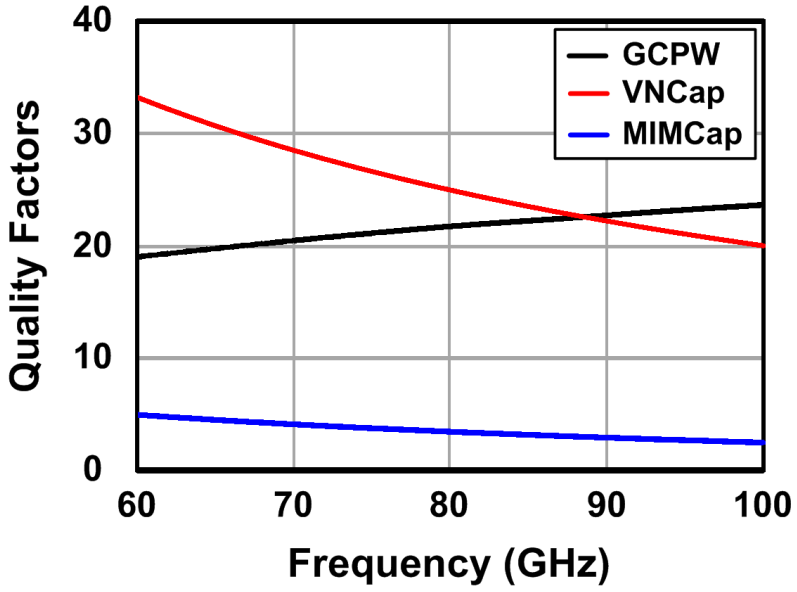
Figure 4.3: Simulated f_T and f_{max} of a 4-μm HBT device.

4.2.2 LNA Design

The schematic of the three-stage LNA is shown in Fig. 4.5 without the biasing circuitry. The first stage is designed for minimum noise with an emitter length of 10 μm and is biased close to peak f_T with 15 mA. A 40-μm emitter degeneration transmission line is used to simultaneously achieve noise and gain



(a)



(b)

Figure 4.4: The 90-nm SiGe BiCMOS process: (a) Back-end-of-line stackup. (b) Simulated Q of a 50-Ω GCPW line, 130-fF MIM and VN capacitors.

matching such that

$$Z_I = r_b + \frac{g_m L_e}{C_{be}} + \frac{1}{sC_{be}} + sL_e \approx Z^*_{S,OPT}, \tag{4.5}$$

where r_b is the HBT base resistance, g_m is the transconductance, C_{be} is the base-emitter capacitance, L_e is the emitter degeneration inductance, and $Z_{S,OPT}$ is the optimum source impedance (Z_S) for minimum noise. The LNA input matching network is composed of a series 100-fF capacitor and a shunt 145-μm transmission line and presents a transformation of Z_S from 50 Ω to a 25-Ω $Z_{S,OPT}$ as shown in Fig. 4.6(a). The first stage of the LNA contributes a minimum 3.8-dB NF and 7.6-dB available power gain. The second and third stages of the LNA are designed for high-gain, thus the common emitter structure is adopted without emitter degeneration. The emitter length of both stages is 4 μm and are biased at 5 mA. The input, output, and interstage matching networks are implemented in GCPW lines and VN capacitors. As Fig. 4.6(b) shows, the input and output of the LNA are matched to 50 Ω. The interstage networks between each stage are designed for complex conjugate matching, i.e. $Z_1 \approx Z_2^*$ and $Z_3 \approx Z_4^*$. The overall three-stage LNA achieves a 26.3-dB gain and 5.5-dB NF, which is close to the minimum NF of 5.4 dB at 78 GHz. The input and output return loss are better than 10 dB over the 71–86 GHz as simulated in Fig. 4.7. The LNA consumes 25-mA dc current from a 1.8-V supply from simulation.

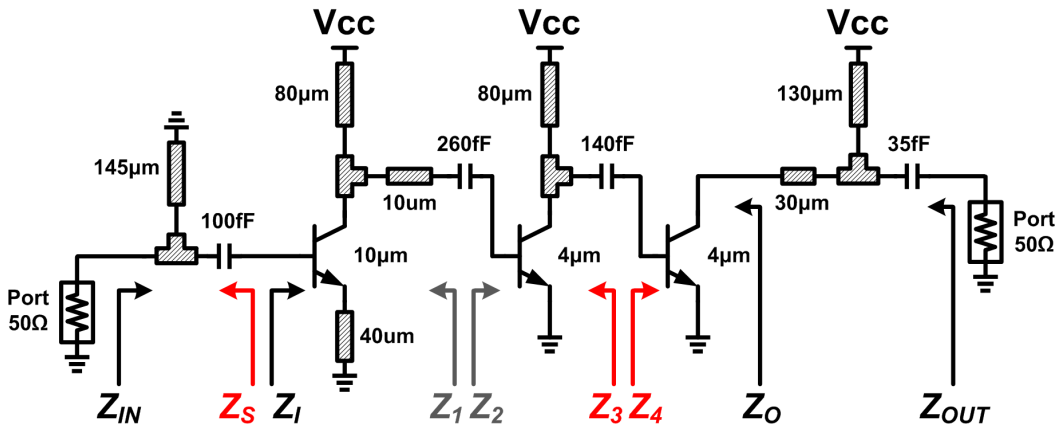
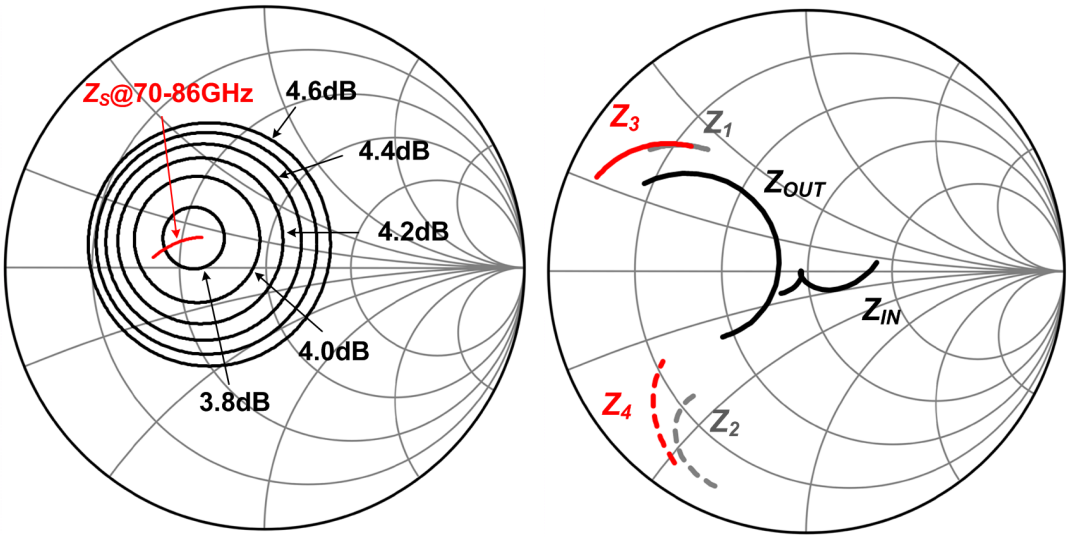


Figure 4.5: Schematic of the LNA without biasing circuitry.



(a) (b)

Figure 4.6: LNA noise and gain matching design: (a) 78-GHz noise circle and 70-86-GHz source impedance and (b) 70-86-GHz input, output and interstage matching.

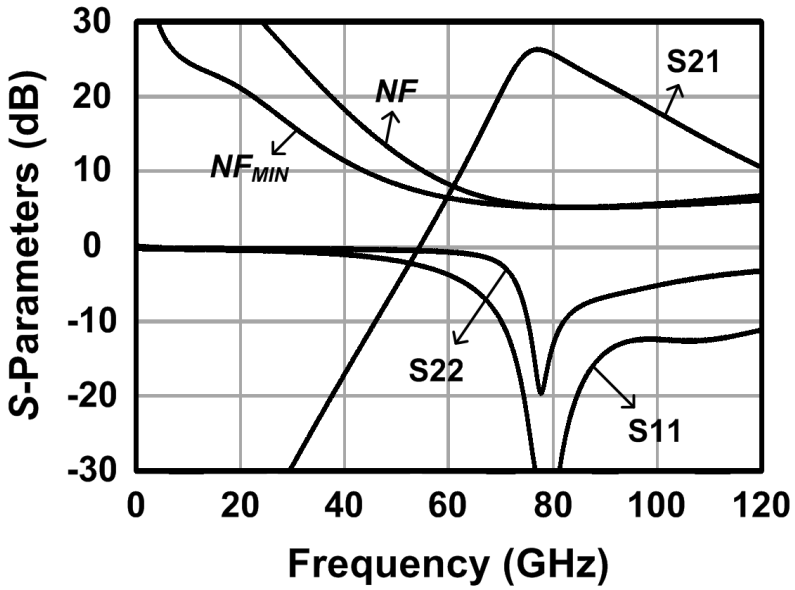


Figure 4.7: Simulated S-parameters and NF of the LNA.

4.2.3 PA Design

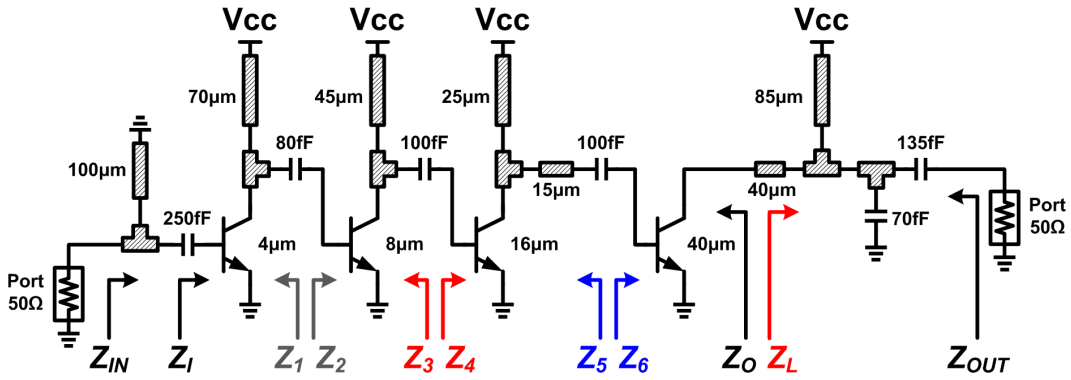
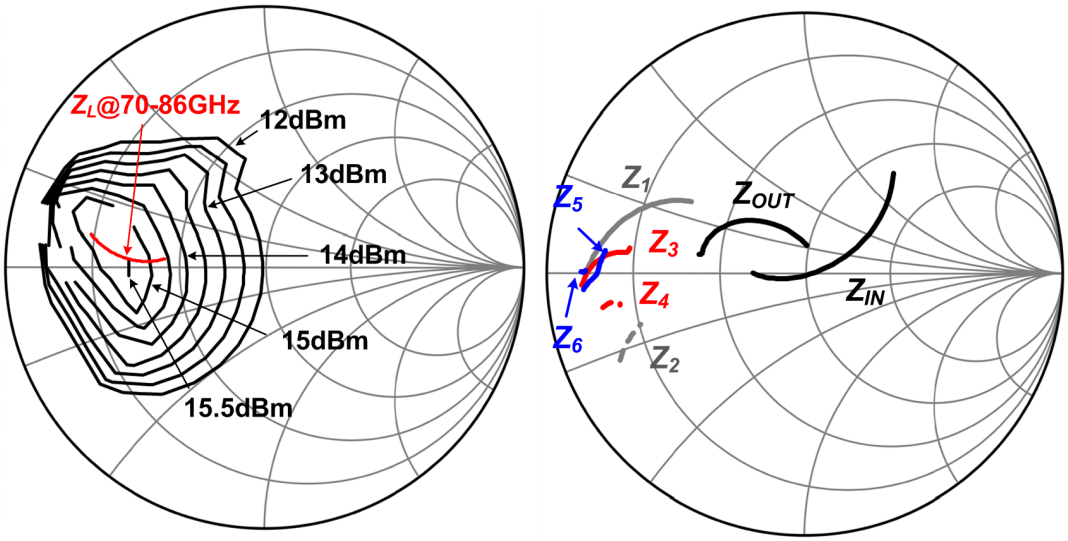


Figure 4.8: Schematic of the PA without biasing circuitry.

The schematic of the PA is shown in Fig. 4.8 without the biasing circuitry and has a three-stage driver to saturate the final PA. The final transistor has an emitter length of 40 μm which is biased in class-A with a quiescent current of 55 mA. From the simulated load pull contour in Fig. 4.9(a), the final PA provides 15.5-dBm $Psat$ with a 15-Ω load impedance (Z_L). As a result, the PA output matching network is designed to transfer Z_L from 50 Ω to 15 Ω. The transistors of the three driver stages are 4 μm, 8 μm, and 16 μm and are biased at 5 mA, 12 mA, and 24 mA, respectively, for high gain and saturated power at the input of the final PA. The input of the first driver is matched to 50 Ω and all the interstages are designed for complex conjugate matching, i.e.,$Z_1 \approx Z_2^*$, $Z_3 \approx Z_4^*$, and $Z_5 \approx Z_6^*$, as shown in Fig. 4.9(b). The small-signal gain of each stage is 11 dB, 9.5 dB, 8 dB and 5.5 dB, respectively, at 78 GHz and the overall four-stage PA achieves 33.7-dB small-signal gain, 15-dBm $Psat$ and 12% PAE as plotted in Fig. 4.10. The PA consumes 96-mA quiescent current from a 1.8-V supply from simulation. According to Fig. 4.10, the PA is driven to the P_{1dB} at an input power of –18 dBm for maximum PAE.



(a) (b)

Figure 4.9: PA matcing design: (a) 78-GHz load-pull contour and 70–86-GHz load impedance. (b) 70–86-GHz input, output and interstage matching.

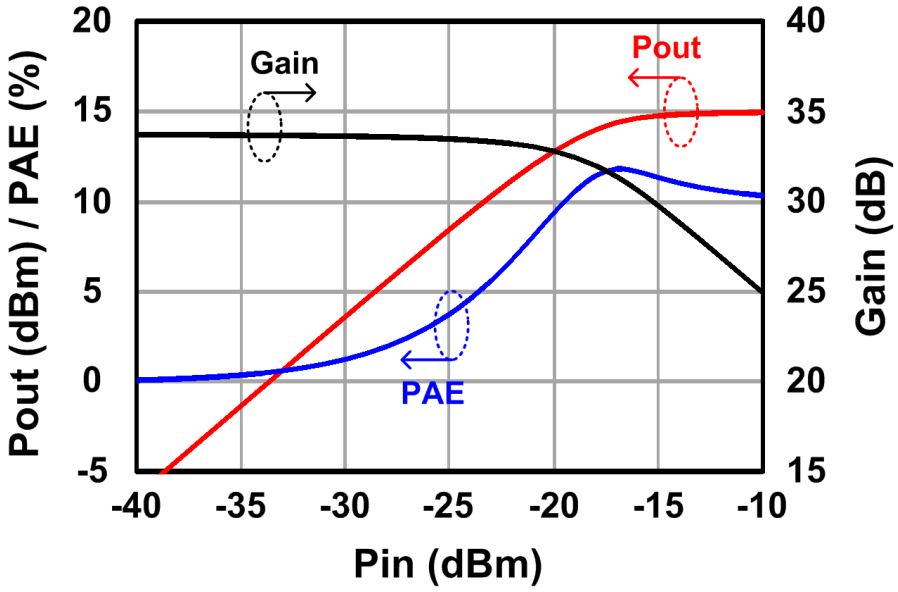


Figure 4.10: Simulated gain, output power and PAE of the PA at 78 GHz.

4.2.4 PA/LNA Combiner

The PA and LNA were designed for 50-Ω load and source impedances to optimize the PA *Psat* and the LNA *NF* to cover the 71–86 GHz band. To share a common antenna, a novel PA/LNA combining technique is proposed and illustrated in Fig. 4.11. A PA/LNA combiner network interfaces the PA output and LNA input to the antenna port while another combines the PA input and LNA output at the mixer port. Each combiner is composed of two transmission lines with characteristic impedance Z_o equal to the ports, e.g. 50 Ω. Selection of the length of these four transmission lines optimizes the PA and LNA operation in the presence of the additional transmission line loss.

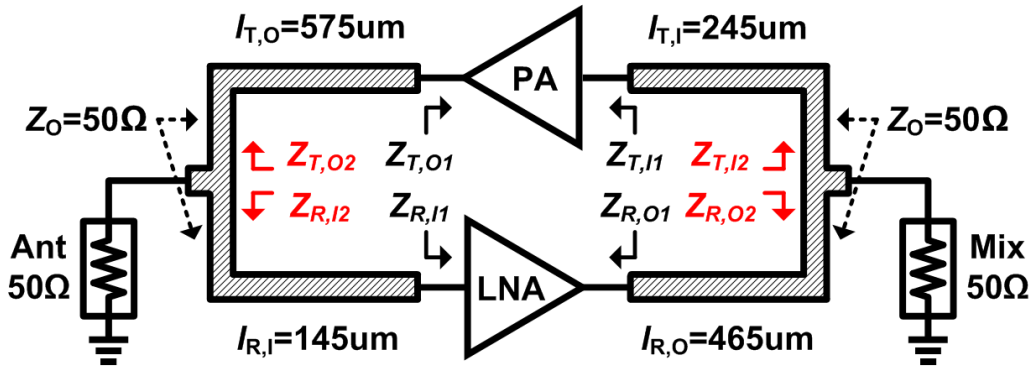
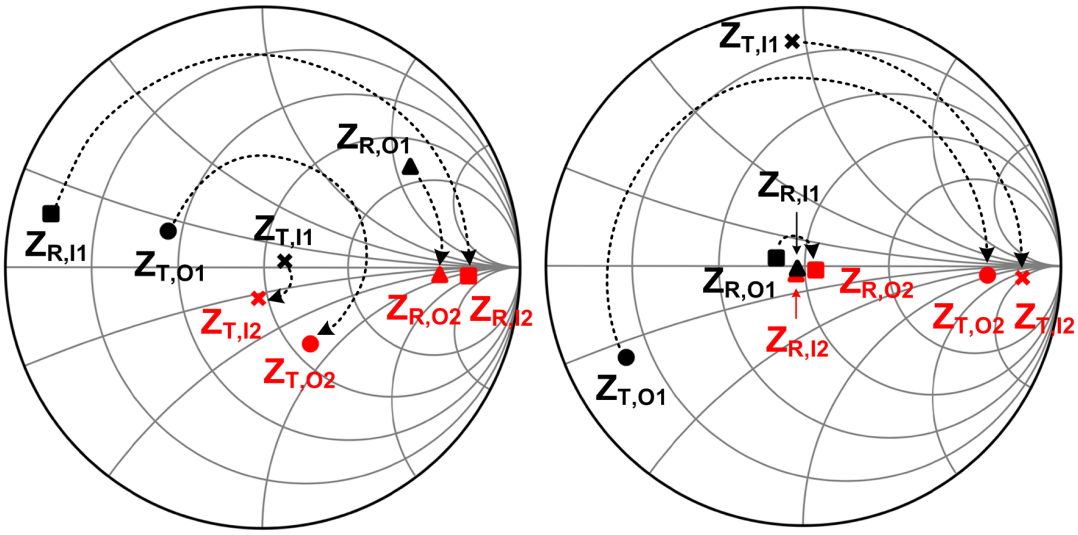


Figure 4.11: Proposed transmission-line-based PA/LNA combiner.

In TX mode, the PA is active and the LNA is inactive. Both the input and output of the PA are matched to 50 Ω for wideband operation (20% fractional bandwidth). The additional transmission lines at the PA input and output extend the 50-Ω reference plane without significantly affecting the matching conditions. As plotted in Fig. 4.12(a), the impedance transformation from $Z_{T,O1}$ to $Z_{T,O2}$ and $Z_{T,I1}$ to $Z_{T,I2}$ rotates the matching impedance at the input and output of the PA around 50 Ω. Referring to Fig. 4.5, Z_I and Z_O are high impedances when the LNA is inactive in TX mode. The $Z_{R,I1}$ and $Z_{R,O1}$ are transferred from such high impedances through the LNA input and output matching networks and become low impedances ($Z_{R,I1} = (79 + j \cdot 118)$ Ω and $Z_{R,O1} = (4.2 + j \cdot 6)$ Ω). These low



(a) (b)

Figure 4.12: Impedance transformation at 78 GHz by the PA/LNA combiner in (a) TX mode and (b) RX mode.

impedances cause extra loading effects at the PA input and output and degrade the $Psat$ and gain. With the additional transmission lines with length of $l_{R,I}$ =145 μm at the LNA input and $l_{R,O}$ =465 μm at the LNA output, the impedances are transformed according to

$$Z_2 = Z_o \frac{Z_1 + Z_o \tanh \gamma l}{Z_o + Z_1 \tanh \gamma l}, \tag{4.6}$$

where Z_2 can be substituted by $Z_{R,O2}$ or $Z_{R,I2}$, Z_1 can be substituted by $Z_{R,O1}$ or $Z_{R,I1}$, l can be substituted by $l_{R,I}$ or $l_{R,O}$, and γ is the propagation constant of the transmission lines. Therefore, the LNA input and output impedances are transferred from low impedances to high impedances ($Z_{R,I2} = (270j \cdot 31)$ Ω and $Z_{R,O2} = (442j \cdot 87)$ Ω). Since $Z_{R,I2}$ and $Z_{R,O2}$ are much greater than 50 Ω, the loading issue from the LNA is significantly alleviated. From $Z_{R,I2}$, simulations estimate a 0.77-dB output power degradation. Furthermore, the $Z_{R,O2}$ contributes an additional 0.48-dB loss from the PA input so the overall gain drops 1.25 dB. The simulation results match our calculation well as in Fig. 4.13. The combined PA/LNA achieves 32.3-dB small-signal gain, 14.4-dBm $Psat$ and 12% PAE in TX

mode at 78 GHz. Compared to Fig. 4.10, a 0.6-dB output power and a 1.5-dB gain drop are found where the insertion loss of the transmission lines is included.

In RX mode, the additional transmission lines at the active LNA input and output also extend the 50-Ω reference plane. The input and output impedances are transferred from $Z_{R,I1}$ to $Z_{R,I2}$ and $Z_{R,O1}$ to $Z_{R,O2}$ as shown in Fig. 4.12(b), and are still matched to 50 Ω. Now, the PA is inactive and the lengths of the input and output transmission lines are obtained as 245 μm and 575 μm, respectively. Based on (4.6), the inactive PA input and output impedances $Z_{T,I1} = (6.8+j \cdot 47)$ Ω and $Z_{T,O1} = (6.7j \cdot 12)$ Ω are transferred to $Z_{T,I2} = (566j \cdot 206)$ Ω and $Z_{T,O2} = (298j \cdot 48)$ Ω. Due to the $Z_{T,I2}$, a 0.37-dB loss is introduced at the LNA output. From $Z_{T,O2}$, the LNA input has a 0.69-dB loss, which also introduces a NF degradation, and results in overall 1.06-dB gain lower. The simulation in Fig. 4.14 demonstrates the combined PA/LNA achieves 25.2-dB gain and 6.26-dB NF at 78 GHz in RX mode. Comparing to Fig. 4.7, 1.1-dB gain and 0.76-dB NF degradations are found from the insertion loss of the transmission lines and the loading effect of the PA.

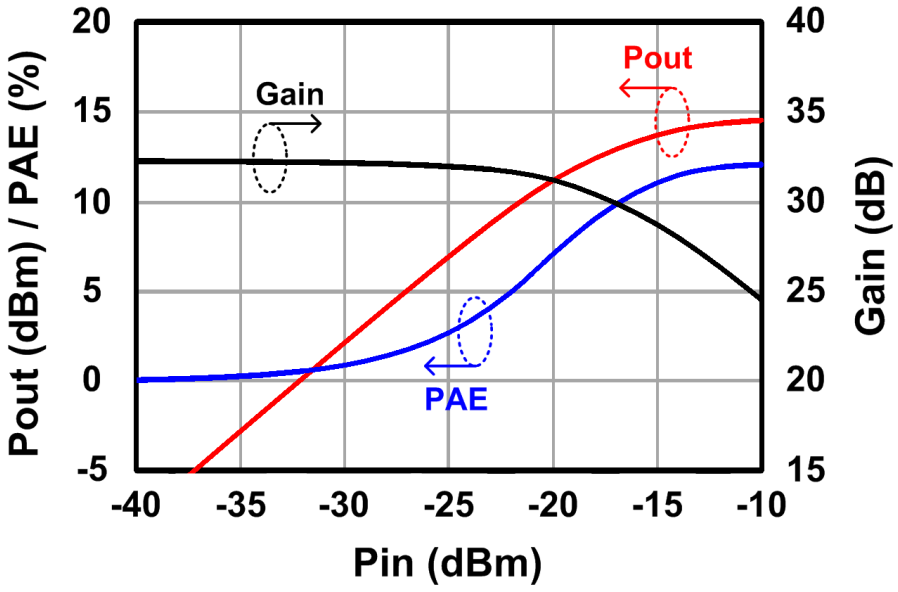


Figure 4.13: Simulated gain, output power and PAE of the combined PA/LNA at 78 GHz in TX mode.

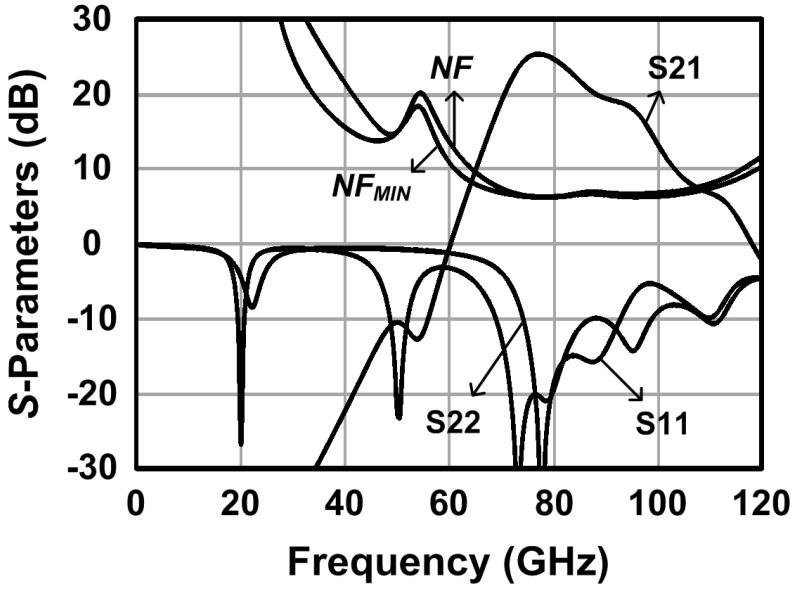
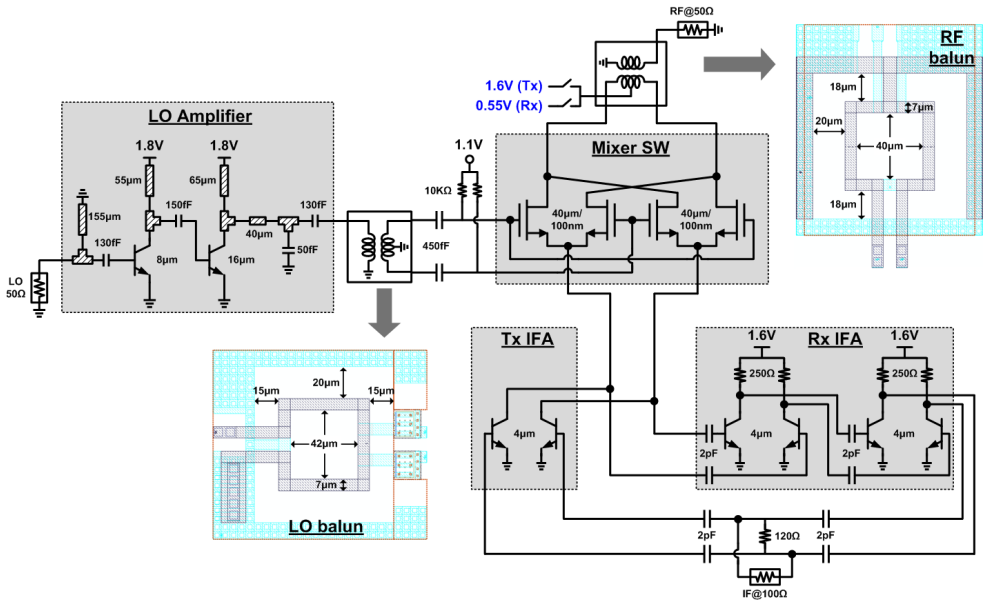


Figure 4.14: Simulated S-parameters and NF of the combined PA/LNA in RX mode.

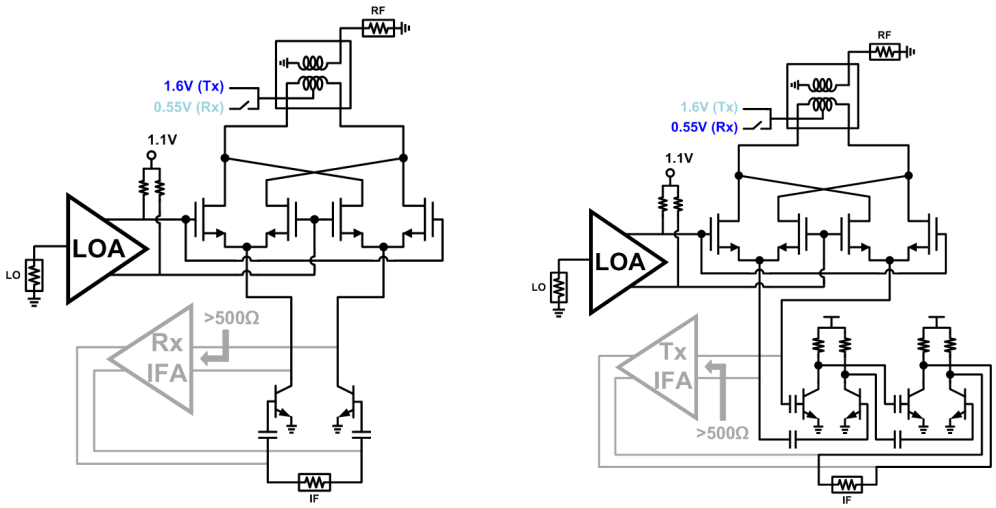
4.2.5 Mixer, IF and LO Amplifiers

In TX mode, an active mixer is preferred over a passive mixer to provide higher conversion gain to drive the PA. Additionally, the power division in the phased array transmitter splits between each of the PAs requiring additional gain. In RX mode, a passive mixer is desirable for higher linearity before combining the signal at the IF band. Therefore, a bidirectional mixer is proposed in this work based on a single FET quad that can be operated as a passive mixer (i.e. zero dc current) in the RX mode or as an active mixer (i.e. non-zero dc current) in TX mode.

The double-balanced mixing stage consists of four NFETs arranged in a switching quad as shown in Fig. 4.15(a) and is shared between the TX and RX paths. The advantage of the highly scaled BiCMOS process is that 90-nm NFET switches have symmetric drain/source structure that can be operated as passive or active devices. Furthermore, at E-band, the loss of these devices as switches is



(a)



(b) (c)

Figure 4.15: (a) Schematic of the bidirectional mixer, LO and IF amplifiers. (b) Operating in TX mode. (c) Operating in RX mode.

improved. Each NFET switch is sized at 40 μm/100 nm for an $R_{ON} \approx 12\,\Omega$ for the trade-off between conversion loss and switching speed. The double-balanced structure has the advantage of lower LO-to-RF leakage and even-order harmonic distortion compared to a single-balanced mixer. At the RF port, an on-chip transformer-type balun converts from the differential mixer to the single-ended PA/LNA and provides a wideband match to 50 Ω. The single-ended coil is realized using the 4-μm-thickness top aluminum metal (LD) with 7-μm width. The differential coil is implemented using the 3-μm-thickness OL and has a width of 7 μm and vertical spacing of 1.25 μm to LD. At the LO port, another transformer balun is used to match the differential mixer switches to a single-ended LO driving amplifier. The LO balun has a similar design to the RF balun in terms of metal implementation and widths. EMX simulations indicate that the RF/LO baluns have insertion losses of 0.75 and 0.66 dB, respectively, and gain imbalances of 0.62 and 0.3 dB and phase imbalances of 5.2 and 3.7 degree at 78 and 68 GHz, respectively.

In TX mode, the HBTs of the transmitter IF amplifier are biased in the active region to operate as current sources while the receiver IF amplifier is disabled through biasing as shown in Fig. 4.15(b). Sharing dc current with the mixer switches and the RF balun realizes an active Gilbert-type mixer with high conversion gain. The emitter length of the transmitter IF amplifier transistors are 4 μm and biased at 5.8 mA from a 1.6-V supply. The NFET mixer switches are biased with 10-kΩ resistors at 1.1 V, where the V_{GS} is near the threshold voltage of 450 mV. In RX mode, the transmitter IF amplifier is inactive and no dc current flows through the switching quad. The passive mixer is followed by a two-stage receiver IF amplifier as shown in Fig. 4.15(c). The voltage at the source and drain of the mixer switches are biased to 550 mV while the V_{GS} is biased 100-mV higher than the threshold voltage for lower conversion loss.

For QAM schemes, a high-linearity receiver mixer is desirable due to the sensitivity and dynamic range limits as (4.4) expressed. For instance, based on the designed LNA with ~26-dB gain, –48-dBm minimum output power from the LNA to the mixer ($P_{IN,MIN}$) is derived from (4.2) giving a 2-GHz BW and a 7-dB NF. For a 40-dB dynamic range, the maximum output power from the LNA to

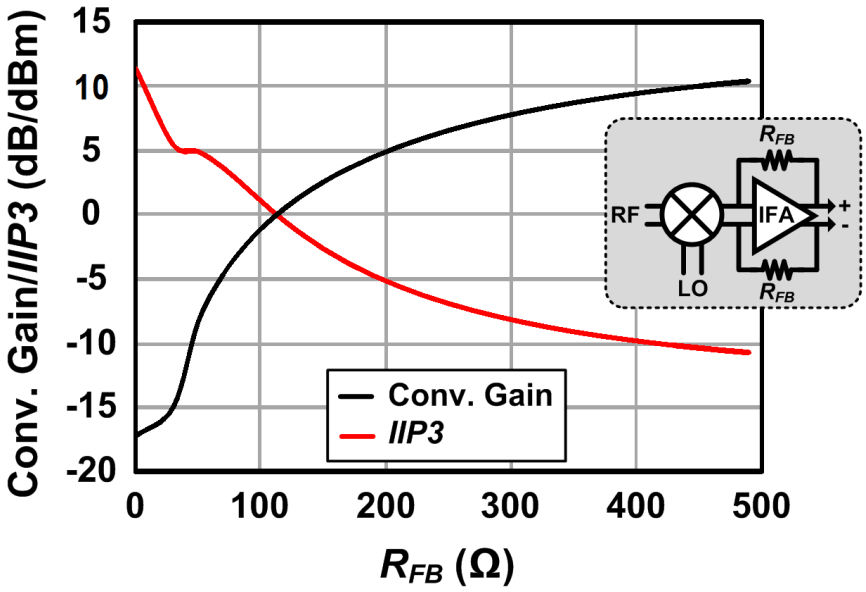


Figure 4.16: Simulated conversion gain and IIP_3 versus the feedback resistance.

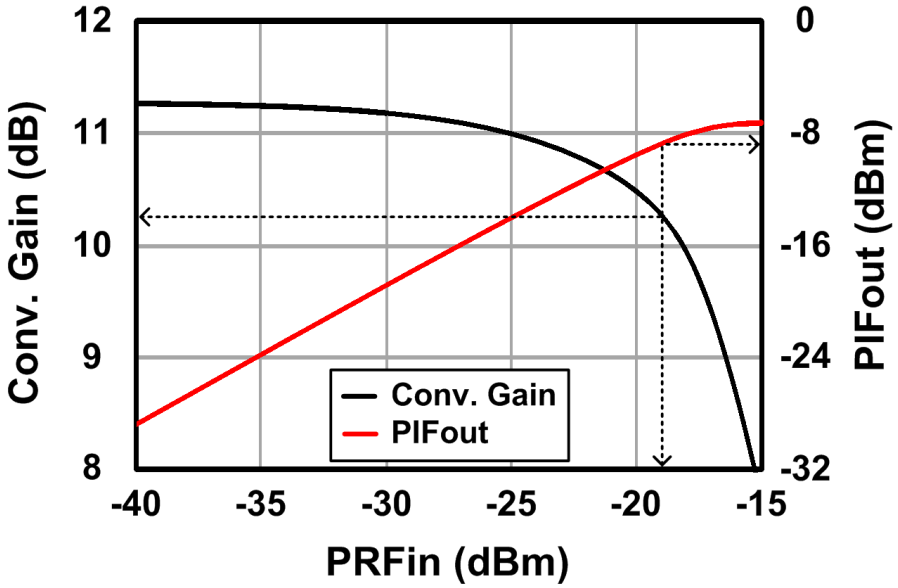
the mixer ($P_{IN,MAX}$) would be –8 dBm. So the required mixer IIP_3 of 12 dBm can be found from [7]:

$$IIP_{3,MIX} = \frac{(3 \cdot P_{IN,MAX} - P_{IN,MIN})}{2}. \tag{4.7}$$

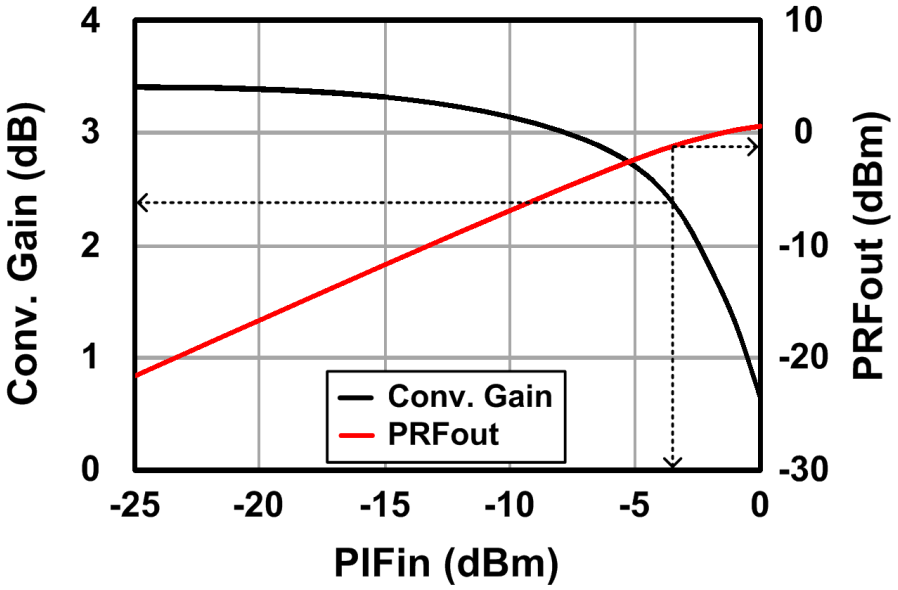
The high-linearity mixer is designed by using the first-stage receiver IF amplifier with shunt-feedback resistors R_{FB} to load the passive mixer with a low input impedance to allow the current-mode operation. The shunt-feedback IF amplifier has an input impedance of $R_{FB}/(1+A)$, where A is the voltage gain of the IF amplifier. As Fig. 4.16 shows, lower input impedance from the IF amplifier gives the mixer better linearity while sacrificing the conversion gain. With the unit-feedback first-stage IF amplifier ($R_{FB} = 0$) and the common-emitter second-stage IF amplifiers, the receiver mixer achieves 11.4-dBm IIP_3, however, contributes 17-dB conversion loss. In this design, two stages of the receiver IF amplifier are both common-emitter structure with resistive load to compensate the loss. Each stage of the receiver IF amplifier is a pair of 4-μm emitter length HBTs with 250-Ω load resistors and 5.6-mA biasing current from a 1.6-V supply. The interconnections between the transmitter and receiver IF amplifiers do not require switches or any

combining technique such as PA/LNA combiner because an inactive HBT provides high enough impedance at the base and collector at the IF frequency, i.e., > 500 Ω.

Spectre simulations indicate the conversion gain of the bidirectional mixer saturates with an 8-dBm LO power at 68 GHz. In general, the 68-GHz LO is generated from a lower frequency phase-locked loop (PLL) and then multiplied to share the LO sources of the RF mixer and the modulator/demodulator, i.e. sliding IF architecture [12,61]. Therefore, a two-stage common-emitter LO driving amplifier is designed to provide a high power from the weak harmonic of the low-frequency source. As the schematic illustrated in Fig. 4.15(a), the first HBT has an emitter length of 8 μm and is biased at 12 mA from a 1.8-V supply for the higher f_T and gain. The second stage of LO driver is designed for high power to drive the mixer switches. The emitter length of second HBT is 16 μm and biased at 24 mA. The input, output and interstage matching networks are implemented in GCPW lines and VN capacitors. From simulation, the input return loss is better than 15 dB at 68 GHz. The LO amplifier achieves a 19.5-dB gain at low-power and a 10.9-dBm saturated output power. Therefore, an input LO power level of –10-dBm is sufficient to provide an 8-dBm output power to saturate the mixer. Figure 4.17 shows the post-layout simulations of the bidirectional mixer and the IF amplifiers including the LO driving amplifier with a –10-dBm input power. The RF, LO and IF frequencies are 78, 68 and 10 GHz, respectively. In Fig. 4.17(a), the overall mixer and IF amplifier achieves a 11.3-dB conversion gain at low power level and –19-dBm input-referred 1-dB compression power (IP_{1dB}) in RX mode. In TX mode, the overall mixer and IF amplifier achieves a 3.4-dB conversion gain at low power and –1.6-dBm output-referred 1-dB compression point (OP_{1dB}) as plotted in Fig. 4.17(b), which is high enough to saturate the PA as Fig. 4.13 indicates.



(a)



(b)

Figure 4.17: Bidirectional mixer simulation in (a) RX mode and (b) TX mode.

4.3 Experimental Results

The 71–86-GHz bidirectional transceiver front-end is implemented in a 90-nm SiGe BiCMOS process and the die occupies 1.5 mm×0.9 mm including pad area as the microphotograph shown in Fig. 4.18. The S-parameters are tested using 1-mm coaxial probes with the Agilent E8361A two port network analyzer to 67 GHz and continuously extended to 110 GHz with the N5260-60003 module. For power, conversion gain, and NF measurements, the RF and LO are probed with WR-10 waveguide GSG probes and the IF is probed by a differential ground–signal–signal–ground (GSSG) probe with the SMA coaxial interface. The dc biases are provided by a 12-pin dc probe. The whole RF front-end chip consumes 350.2 mW in TX mode and 137.7 mW in RX mode including all the RF, IF and LO amplifiers.

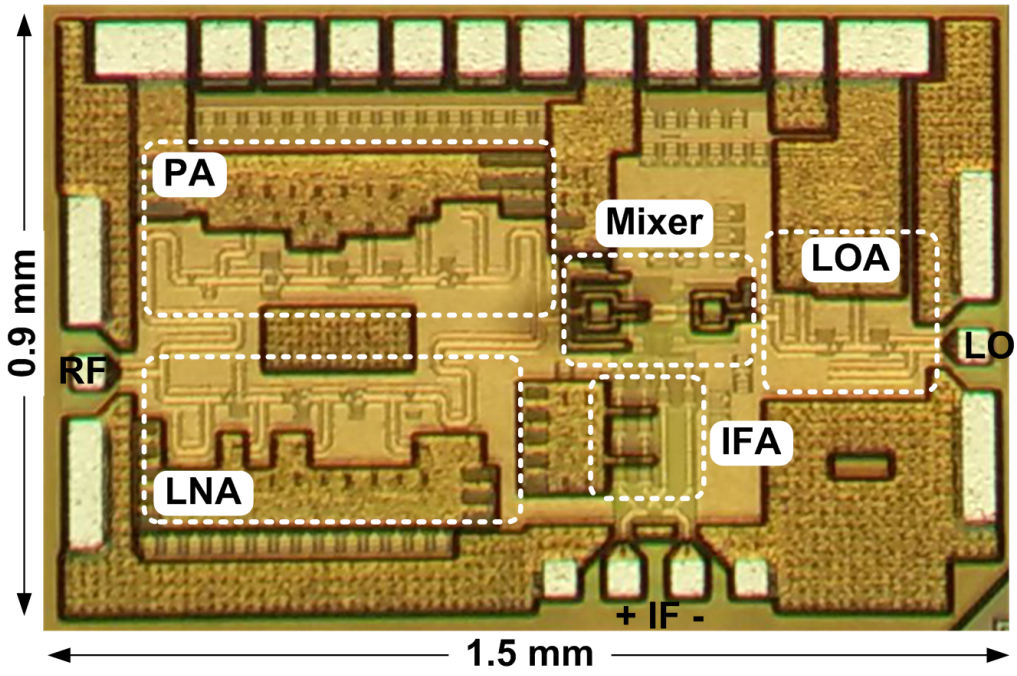


Figure 4.18: Chip microphotograph of the 71–86-GHz bidirectional transceiver in 90-nm SiGe BiCMOS.

4.3.1 TX Mode

The measured S-parameters for RF output and LO input matching in TX mode are shown in Fig. 4.19 and compared with simulations. The measured RF return loss is better than 10 dB from 71 to 86 GHz and LO return loss is 19 dB at 68 GHz. All passive elements and parasitics are modeled by EMX in this design and show excellent agreement between simulation and measurement.

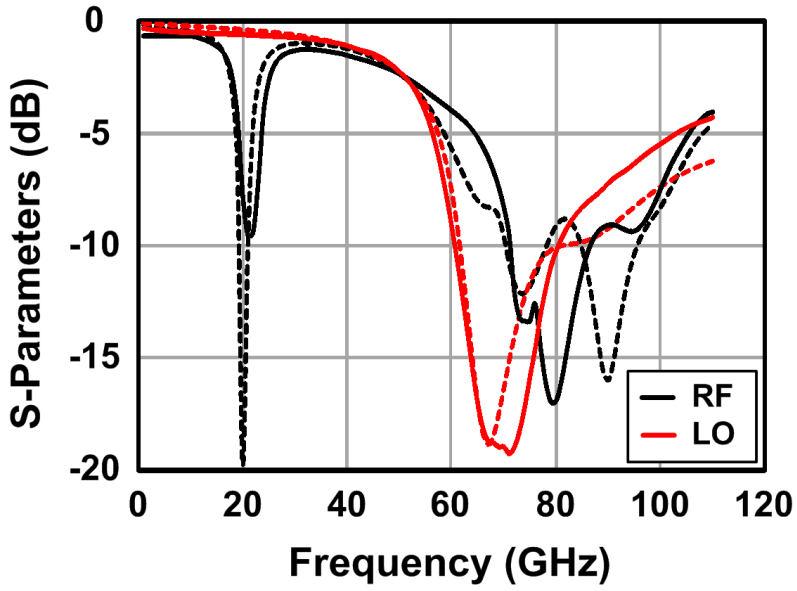


Figure 4.19: Measured (solid lines) and simulated (dash lines) RF and LO return loss in TX mode.

For the power measurement, the RF output power is sensed by an Agilent W8486A power sensor and read by an Agilent E4419B power meter. The LO signal is generated from Agilent E8257D and is multiplied using a Pacific Millimeter E3 tripler to 68 GHz. The IF signal is provided by another Agilent E8257D signal generator and is converted to differential by a hybrid coupler. Figure 4.20 shows the measured conversion gain, RF $Psat$, and the LO leakage versus LO power at the LO and IF input frequencies of 68 and 10 GHz. The transmitter achieves 24.8-dB conversion gain, 11-dBm $Psat$ and –11-dBm LO leakage power at the RF port with –7-dBm available LO power on-chip. LO leakage is a serious concern

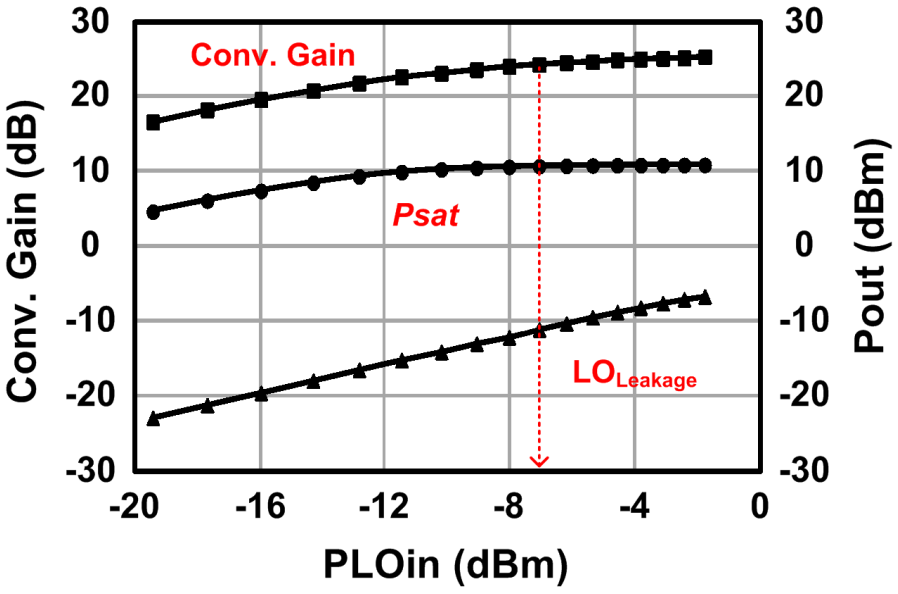


Figure 4.20: Measured conversion gain, *Psat* and LO leakage power at 78-GHz RF frequency in TX mode.

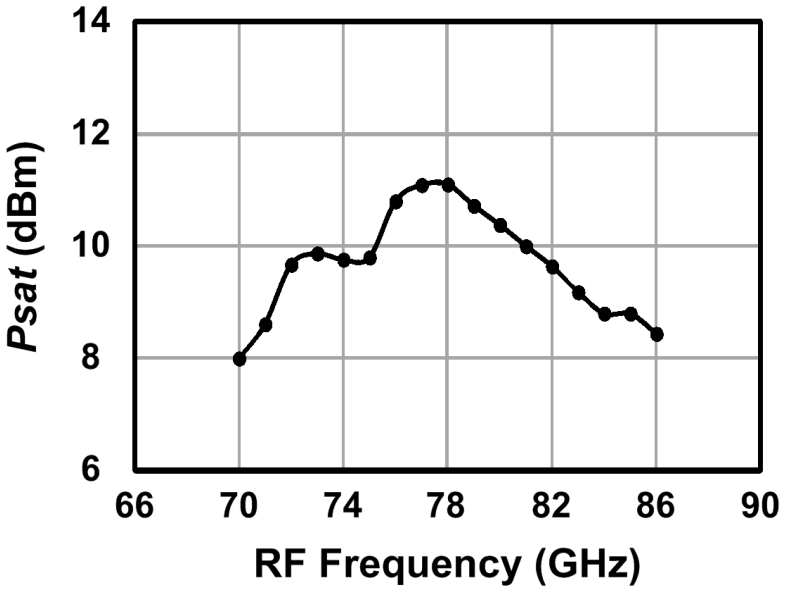


Figure 4.21: Measured *Psat* over RF frequency in TX mode.

since the wideband transceiver has an LO which can be amplified by the PA at 68 GHz. The –7-dBm on-chip LO power is chosen for subsequent testing since the transmitter is saturated while the LO leakage is above –22 dBc. To cover backhaul applications in *E*-band (71–76/81–86 GHz), long-range cruise control automotive radars in 76–77 GHz and short-range side-crash prevention radars in 77–81 GHz, which apply frequency and phase modulations, the saturated transmitted power is measured by sweeping the IF input frequency from 2 to 18 GHz as plotted in Fig. 4.21. The maximum *Psat* is 11 dBm at 78-GHz RF frequency and the 3-dB bandwidth is from 70 to 86 GHz. The measured PA and the active mixer are biased at 102 mA and 13 mA, respectively, from a 2.5-V supply and the LO amplifier flows 37-mA dc current from a 1.7-V supply.

4.3.2 RX Mode

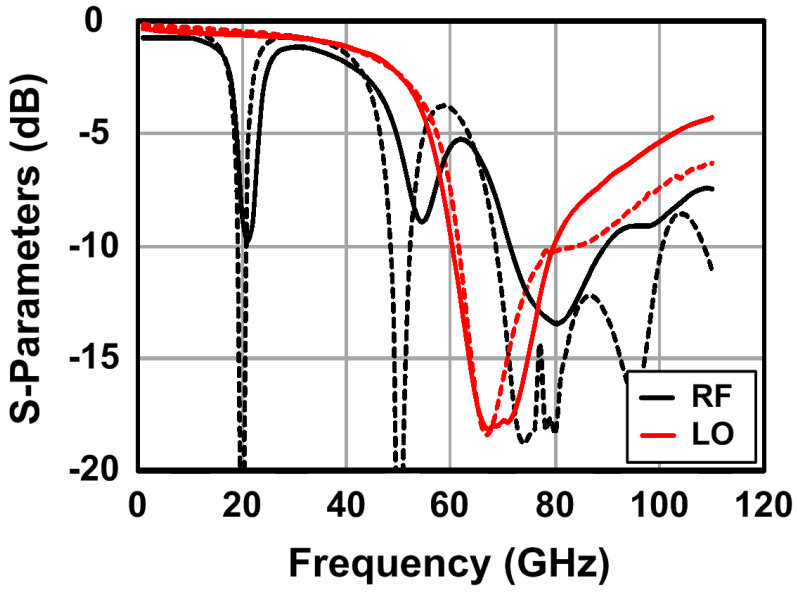


Figure 4.22: Measured (solid lines) and simulated (dash lines) RF and LO return loss in RX mode.

Figure 4.22 shows the measured *S*-parameters for RF and LO matching in RX mode with comparison to the simulation. The measured RF return loss is

better than 10 dB from 72 to 89 GHz and LO return loss is 18 dB at 68 GHz.

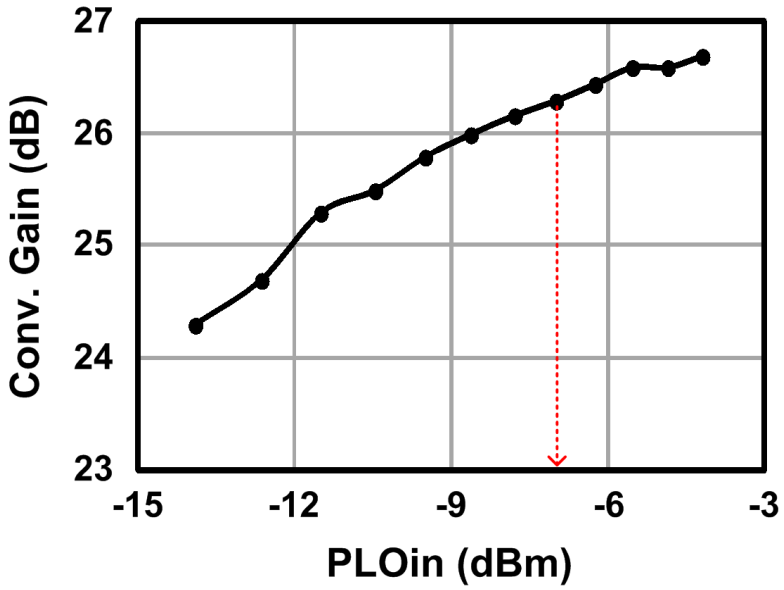


Figure 4.23: Measured conversion gain versus the LO power at 78-GHz RF frequency in RX mode.

For the receiver conversion gain measurement, the 68-GHz LO is generated as the same way as the transmitter. The RF signal is provided from another Agilent E8257D signal generator and is multiplied by a Pacific Millimeter W3 tripler to the interested frequency band. The RF input power is monitored through a –10 dB directional coupler at the through port and is sent to the chip at the coupled port. The 68-GHz LO is generated as the same way as the transmitter measurement and the output IF signal is tested from an Agilent E4448A spectrum analyzer through the hybrid coupler for converting from differential to single-ended. Figure 4.23 shows the measured conversion gain versus LO power at the RF and LO input frequencies of 78 and 68 GHz. With –7-dBm available on-chip LO power as the transmitter, the receiver conversion gain is 26.4 dB. To cover the entire E-band from 71 to 86 GHz, the receiver conversion gain and NF are measured by sweeping the RF input frequency as plotted in Fig. 4.24. The maximum conversion gain shifts down to 73 GHz of 30.6 dB due to the low-pass response of the IF amplifier.

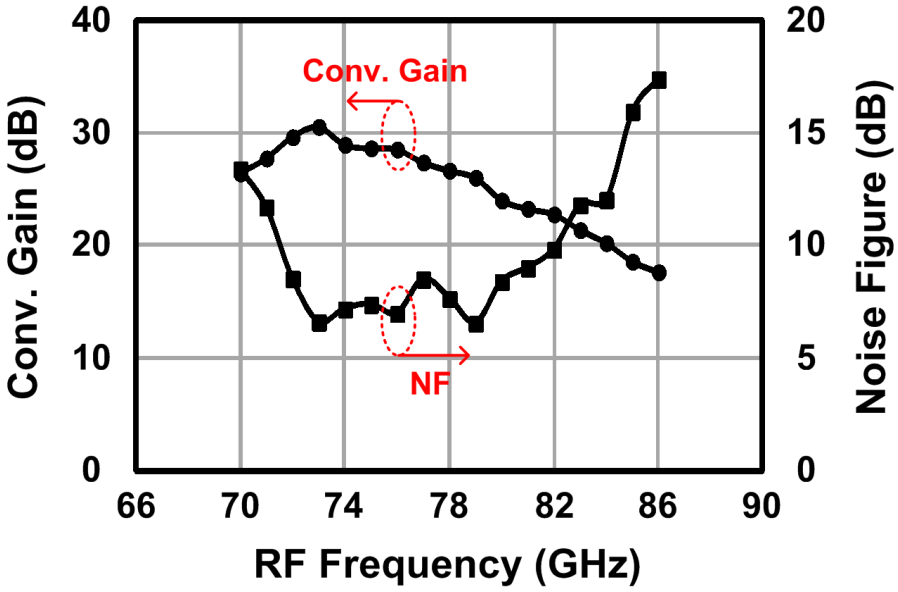


Figure 4.24: Measured conversion gain and NF over RF frequency in RX mode.

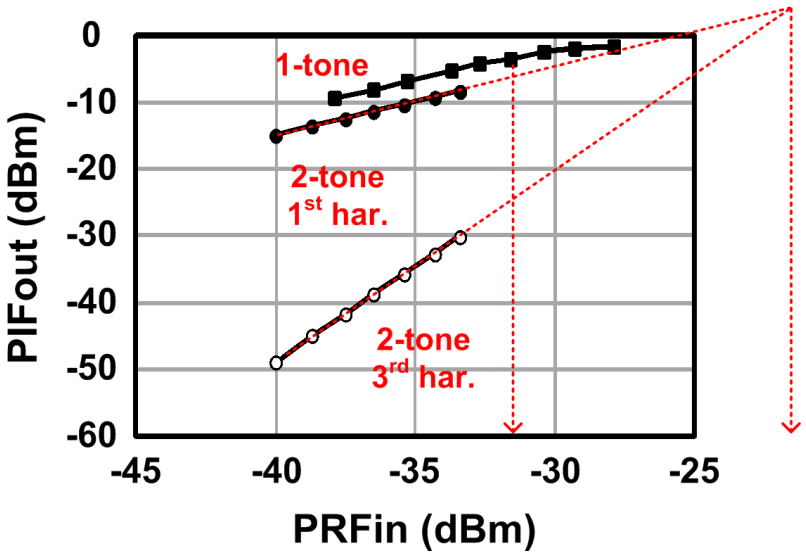


Figure 4.25: Measured third-order intercept point at 78-GHz RF frequency in RX mode.

The receiver NF is measured using the gain method [7] and can be expressed as

$$NF = 174(\text{dBm/Hz}) - \text{Conv. Gain} - 10\log_{10} RBW + P_{N,OUT}, \qquad (4.8)$$

where RBW is the resolution bandwidth of the spectrum analyzer and $P_{N,OUT}$ is the measured noise power at the receiver output. The measured NF is 7.6 dB at 78 GHz and better than 9 dB over 72–81 GHz. The gain compression and the third-order intermodulation are recorded in Fig. 4.25. The measured OP_{1dB} at 78-GHz RF frequency is –3.5 dBm and the IIP_3 is –21.5 dBm. The measured LNA is biased at 27 mA from a 2-V supply. The LO amplifier flows 37-mA current from a 1.7-V supply and the IF amplifier consumes 13-mA current from a 1.6-V supply. The performance is summarized and compared with prior bidirectional transceiver works in Table 4.1. The proposed work achieves a high power in TX mode and excellent NF and linearity in RX mode in 71–86 GHz.

4.4 Conclusions

A switchless, bidirectional transceiver front-end has been demonstrated at E-band (71 to 86 GHz) in a 90-nm SiGe BiCMOS process. Novel power combining networks between the PA and LNA offer low loss for better sensitivity and power handling without integrated mm-wave switches. To optimize the performance of the bidirectional operation for TX and RX modes, asymmetric operation of the mixer is demonstrated whereby an NMOS mixer can be operated as a passive or active mixer. In TX mode, a $Psat$ of 11 dBm at 78 GHz and a 3-dB bandwidth from 70 to 86 GHz are measured from this chip. In RX mode, the measured NF is 7.6 dB and the overall conversion gain is 26.4 dB at 78 GHz.

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Table 4.1: Performance summary and comparison of published bidirectional transceivers.

Reference	This work	[20]	[19]
Technology	90-nm SiGe BiCMOS	90-nm CMOS	120-nm SiGe BiCMOS
Frequency	71–86 GHz	60 GHz	41–46 GHz
Description	TRx Element	4-Element TRx	TRx Element
Chip Area	1.5×0.9 mm^2	1.6×1 mm^2	1.6×0.8 mm^2
Transmit Mode			
Conversion Gain	24.8 dB	7 dB	35 dB
OP_{1dB}	9.3 dBm	0.5 dBm	8.5 dBm
$Psat$	11 dBm	3.5 dBm	9.5 dBm
DC Power	350.2 mW	78 mW	119.4 mW
Receive Mode			
Conversion Gain	26.4 dB	7 dB	34 dB
NF	7.6 dB	8.7 dB	4.7 dB
OP_{1dB}	–3.5 dBm	–13 dBm	–5 dBm
IIP_3	–21.5 dBm	–	–26.3 dBm
DC Power	137.7 mW	78 mW	54 mW

Chapter 5

Conclusions

This dissertation presents the mm-wave transmitter systems and a bidirectional transceiver front-end circuit implemented in Si/SiGe processes.

The first portion of this dissertation presents the dual-band (Q-band/W-band) direct-conversion transmitter implemented in 120-nm SiGe BiCMOS process. There are two novel features in this work. The dual-band feature is the use of the proposed transmission-line-based dual-band load on RF and LO amplifiers to allow the transmitter to operate at two distinct bands. The static I/Q correction feature applied in this transmitter calibrates amplitude and phase mismatch from analog baseband and greatly improves the SSR and EVM. Both improvements from the I/Q correction feature are demonstrated at both Q-band and W-band. To the best of author's knowledge, these two features are the first-proposed and first-demonstrated ideas in mm-wave circuitry.

The second portion of this dissertation demonstrates 45-GHz (Q-band) and 94-GHz (W-band) transmitter systems with DPD to compromise the linearity/efficiency trade-off. The 45-GHz transmitter system uses the first-portion SiGe modulator and a two-by-two PA/antenna array which PAs are implemented in a 45-nm SOI CMOS chip. By programming in an FPGA-based processor, an all-silicon-based solution is verified. Furthermore, the 94-GHz transmitter system uses external two-step frequency conversion to 94-GHz band and a two-by-four PA/antenna array, which is implemented in 45-nm SOI CMOS process. To the best of author's knowledge, these works are the first demonstrations of mm-wave

transmitter systems utilizing DPD to compromise the linearity/efficiency trade-off.

The third portion of this dissertation presents a 71 to 86-GHz (E-band) bidirectional transceiver front-end circuit implemented in 90-nm SiGe BiCMOS process. Two more novel features are proposed in this work. A low-loss, transmission-line-based PA/LNA combining technique is proposed to isolate one or the other for half-duplex operation, while the PA/LNA is optimized with 50-Ω loads to a single antenna and the bidirectional mixer. In addition, a novel asymmetric mixer is proposed give different conversion gain and linearity in the TX and RX modes. The asymmetric mixer is demonstrated to operate as either a passive or an active mixer depending on whether the circuit operates in TX or RX mode using the same mixer switches. To the best of author's knowledge, these two features are the first-proposed and first-demonstrated ideas for bidirectional transceiver front-end circuits for half-duplex applications.

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