UNIVERSITY OF CALIFORNIA
RIVERSIDE

Graphene Device Fabrication and Applications in Communication Systems

A Dissertation submitted in partial satisfaction
of the requirements for the degree of

Doctor of Philosophy

in

Electrical Engineering

by

Guanxiong Liu

June 2012

Dissertation Committee:
Dr. Alexander A. Balandin, Chairperson
Dr. Roger Lake
Dr. David Kisailus

The Dissertation of Guaxiong Liu is approved by:

_____

_____

_____

Committee Chairperson

University of California, Riverisde

Acknowledgements

First and foremost, I would like to express my deep appreciation to my advisor, Professor Alexander A. Balandin. He is a very knowledgeable, insightful and encouraging professor, and guided me to the right direction many times in my research work. At the same time, he gave me a lot of freedom in doing all kinds of research experiment that I want, even when the experiment seemed to be of only minor meaning. Also, Professor Balandin offered me a lot of great opportunities to attend conference all around the world. He also coached me on my presentation skills and the ways to talk with world class researchers.

I would also like to thank our previous group member Dr. Qinghui Shao, who was very helpful and patient in training me with the cleanroom fabrication techniques when I was a rookie member in the lab. Moreover, he was very kind in sharing with me his knowledge about the semiconductor physics which helped me to understand the basics of graphene that I started to work on for the following five years.

I am grateful to other previous group members Dr. Desalegne Teweldebrhan, Dr. Irene Calizo, Dr. Muhammad Rahman Dr. Suchismita Ghosh, Dr. Samia Subrina, Dr. Viveck Goyal, Dr. Craig Nolen, Dr. Md. Zahid Hossain, and Dr. Javed Khan, as well as current members Zhong Yan, Jie Yu and Pradumna Goli for their helpful discussions and contributions towards my research work.

I am thankful to cleanroom stuff Dexter Humphrey, Dong Yan and Mark Heiden for their great help in training me with cleanroom fabrication skills and useful discussions on my experiments.

I would also like to thank the researches that I worked with when I did internship at IBM T.J. Watson Research Center during 2010 summer. They are my mentor Dr. Christos Dimitrakopoulos, who guided me in using excellent chemicals to pattern graphene; my manager Dr. Alfred Grill, who provided me almost all kinds of resources to complete my project; my collaborators Dr. Yu-Ming Lin and Dr. Yanqing Wu, who helped me with device fabrications and measurement; Dr. Joy Cheng, who advised me in using chemicals which was entirely new to me.

I also want to thank our research collaborators Prof. Sergey Rumyantsev (Rensselaer Polytechnic Institute), who taught and advised me how to setup the low-frequency noise system and the measurement techniques; Prof. Michael Shur (Rensselaer Polytechnic Institute), who provided helpful and insightful discussions to our projects; Prof. Kartik Mohanram (now at Pittsburg University), who brought the idea of triple-mode amplifier by using graphene; Xuebei Yang (Rice University), whom I worked together with to demonstrate the graphene amplifier.

Finally but not least, I would like to thank my parents Liang Liu and Juan Li for providing their love, support, and understanding through all my educational endeavors. It is my father's passion towards science that encourages me to finish my PhD study; it is my mother's love that alleviates my anxiety when I encountered the new environment

away from home. Without their spiritual and financial supports, I would not be able to continue and successfully finish my educational life.

Dedication

To my parents Liang Liu and Juan Li.

谨以此文献给我的父亲刘良，母亲李娟。

ABSTRACT OF THE DISSERTATION

Graphene Device Fabrication and Applications in Communication Systems

by

Guanxiong Liu

Doctor of Philosophy, Graduate Program in Electrical Engineering
University of California, Riverside, June 2012
Professor Alexander A. Balandin, Chairperson

High carrier mobility, saturation velocity and thermal conductivity make graphene a promising material for high-frequency, analog and communication applications. The ambipolar properties of graphene provide opportunities for increased functionality in unconventional circuit architectures. In this dissertation, I describe the fabrication process of graphene devices, including the optical and Raman spectroscopic characterization and electron-beam lithography. The different electrical characteristics of the single-layer and bilayer graphene field-effect devices reflect differences in the electron band structures of the two systems. The fabricated graphene transistors have been used to design and experimentally demonstrate electronic circuits with communication functionalities such as phase-shift keying, frequency-shift keying and phase detection. Compared with conventional semiconductor electronic designs based on multiple unipolar transistors, the demonstrated graphene amplifiers and phase detectors have advantage of a simplified

structure. An important issue for high-frequency and analog applications is the low-frequency noise, which up-converts and contributes to the phase noise of the systems. It was found that the low-frequency noise in graphene devices is dominated by 1/f noise in the frequency range from 1 Hz to 100 kHz (f is the frequency). The device exposure to different gases results in appearance of characteristic peaks in the noise spectral density. The latter can be utilized for selective gas sensing with graphene. The metal-graphene contact contributions to the 1/f noise can be strongly reduced via the use of the graded thickness graphene channels in the device structure. I have also investigated a possibility of tuning graphene properties via controllable exposure to the low-energy electron-beam irradiation. It was found that the charge neutrality point and resistivity can be tuned over a wide range of values. The obtained results are important for the proposed applications of graphene in analog electronics, communications and sensors.

Contents

List of Figures

List of Tables

Chapter 1

Introduction and Overview

1.1 Introduction

Graphene, a single layer of carbon atoms arranged in honeycomb lattice, is probably the most discussed new material ever since its experimental discovery in 2004 [1]. Its giant carrier mobility [2], large thermal conductivity [3] and extreme thickness of only one atomic layer, as well as high intrinsic mechanical strength [4] make it very interesting among many fields such as physics, chemistry, materials and electrical engineering. The theoretical investigations of graphene, about half-century ahead of its experimental demonstration, were conducted to understand the electronic properties of graphite[5, 6], which is an important material for nuclear reaction. It had been predicted thermodynamically unstable due to the pure two dimension crystal structure [7, 8] and should not exist in real world. However, this exiting material has been experimentally discovered in 2004 by a very rudimentary but robust method of using adhesive tape [1]. Since graphene produced by this method is boned to a substrate, it is not contradicted to the thermodynamics argument of 2D crystals [9, 10]. Ever since the exploration of the excellent properties of graphene, numerous novel applications have been demonstrated based on graphene, such as high speed electronics [11, 12], thermal management [13], mechanical oscillator [14], as well as graphene sensors [15]. The first graphene production was made by exfoliating

graphite by adhesive tape [1]. The chemical methods, chemical vapor deposition (CVD) [16] and epitaxail growth method [17], had been invented to growth high quality and large scale graphene. Yet, the simplest method, exfoliation mean, still provides better graphene than the other two methods.

1.2 Overview

In chapter 2, the graphene device fabrication processes are described in details. Both back-gate and top-gate devices are included. In chapter 3, electrical measurement and results on single layer garphene and bilayer graphene transistors are discussed in depth. Chapter 4 presents the application of graphene in analog communication systems. We experimentally demonstrate functionalities of phase shift keying, frequency shift keying and phase detector. Chapter 5 discusses the low-frequency noise in graphene, which is an important issue for device working in analog systems. Chapter 6 presents the study of tuning graphene electrical and material properties by means of electron beam irradiation. Chapter 7 is the summary.

Reference

[1] K.S. Novoselov, A.K. Geim, S.V. Morozov, D. Jiang, Y. Zhang, S.V. Dubonos, I.V. Grigorieva and A.A. Firsov, *Science*, **306**, 666 (2004).

[2] K. Bolotin, K.J. Sikes, Z. Jiang, M. Klima, G. Fudenberg, P.K. J. Hone and H.L. Stormer, *Solid State Commun.*, **146**, 351 (2008).

[3] A.A. Balandin, S. Ghosh, W. Bao, I. Calizo, D. Teweldebrhan, F. Miao and C.N. Lau, *Nano Lett.*, **8**, 902 (2008).

[4] C. Lee, X. Wei, J.W. Kysar and James Hone, *Science*, **321**, 385 (2008).

[5] P. R. Wallace, *Phys. Rev.*, **71**, 622 (1947).

[6] J.C. Slonczewski and P.R. Weiss, *Phys. Rev.*, **109**, 272 (1958).

[7] L. Landau, Physikalische Zeitschrift der Sowjetunion **11**, 26 (1937).

[8] N.D. Mermin, *Phys. Rev.*, **176**, 250 (1968).

[9] C. Oshima and A. Nagashima, *J. Phys.: Condens. Matter*, **9**, 1 (1997).

[10] A.E. Karu and M. Beer, Pyrolytic *J. Appl. Phys.*, **37**, 2179 (1966).

[11] Y.-M. Lin, C. Dimitrakopoulos, K.A. Jenkins, D.B. Farmer, H.-Y. Chiu, A. Grill and P. Avouris, *Science*, **327**, 662 (2010).

[12] L. Liao, Y.-C. Lin, M. Bao, R. Cheng, J. Bai, Y. Liu, Y. Qu, K.L. Wang, Y. Huang and X. Duan, *Nature*, **467**, 305 (2010).

[13] Z. Yan, G. Liu, J.M. Khan and A. A. Balandin, *Nat. Comm.* (2012) in print.

[14] Y. Xu, C. Chen, V. V. Deshpande, F. A. DiRenno, A. Gondarenko, D. B. Heinz, S. Liu, P. Kim and J. Hone, *Appl. Phys. Lett.*, **97**, 243111 (2010).

[15] S. Rumyantsev, G. Liu, M. Shur, R.A. Potyrailo and A.A. Balandin, *Nano Lett.*, **100**, 033103 (2012).

[16] X. Li, W. Cai, J. An, S. Kim, J. Nah, D. Yang, R. Piner, A. Velamakanni, I. Jung, E. Tutuc, S.K. Banerjee, L. Colombo and R.S. Ruoff, *Science*, **324**, 1312 (2009).

[17] C. Berger, Z. Song, X. Li, X. Wu, N. Brown, C. Naud, D. Mayou, T. Li, J. Hass, A.N. Marchenkov, E.H. Conrad, P.N. First and W.A. de Heer, *Science*, **3012**, 1191 (2006)

Chapter 2

Graphene Device Fabrications

2.1 Graphene Samples Preparation

We use mechanical exfoliation method to produce graphene. The fabrication starts with peeling graphite from bulk material HOPG (highly ordered pyrolytic graphite) by adhesive tape, and then the tape are gently scrubbed onto a SiO_2 substrate. The thickness of the SiO_2 has to be carefully selected in order to have good optical contrast of graphene, so that we can see this atomic thin material under the optical microscope [1]. We choose the substrate with 300 nm SiO_2. A typical optical image is shown in Fig. 2.1.

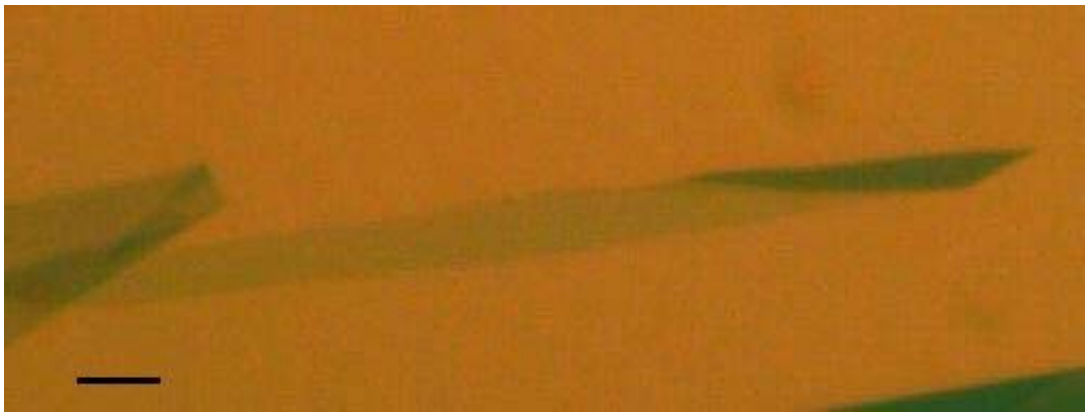

Fig. 2.1 Optical image of graphene on SiO_2 substrate. The light blue ribbon in the center is single layer graphene. The scale bar is 3 μm.

This method yields good quality of graphene that can be validated by Raman spectroscopy. The amount of defects in crystal material is a significant issue. As the defect in a pure crystal has a different dispersion relation, a distinctive peak will

appear on the Raman spectrum. In graphene, a D peak at 1350 cm^{-1} characterizes the defects in this sp^2 carbon. Fig. 2.2 shows the Raman spectrum of a SLG and BLG. Note that the absence of D peak in both spectrum. Another important reason of using Raman to characterize graphene is that this technique can distinguish the number of layers of graphene through de-convolution method of 2D band. In SLG, the 2D band (2700 cm^{-1}) can be fitted by only one elementary Lorenzian peak, where in BLG this band needs 4 Lorenzian peaks to fit [2, 3]. Meanwhile, the intensity ratio of 2D band over G peak (1580 cm^{-1}) for SLG is about 3-4, which is much larger than the ratio of BLG with about 1.

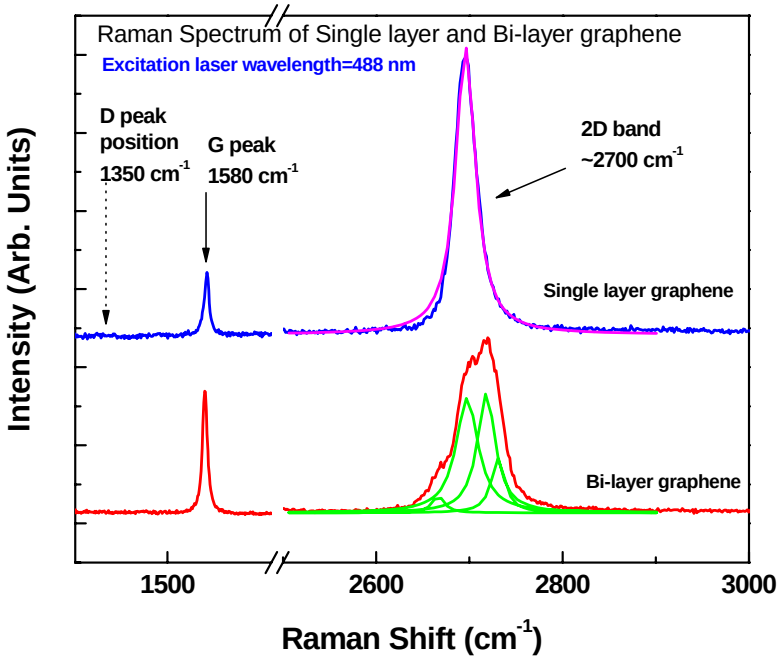

Fig. 2.2. Raman spectra of single layer graphene (SLG) and bi-layer graphene (BLG). The number of layer can be distinguished by de-convolution method. The 2D band of SLG can be fitted by only one elementary Lorenzian peak, where the BLG needs four peaks to fit. Also the intensity ration of 2D over G peak for SLG is much larger than BLG. Meanwhile, the good crystal quality can be characterized by the absence of D peak at 1350 cm^{-1}.

2.2 E-beam Lithography

E-beam Lithography (EBL) is a lithography process that uses a focused electron beam to form patterns needed for material deposition on, or removal from the target substrate. Comparing with optical lithography which uses UV light, EBL offers higher patterning resolution because of the shorter wavelength possessed by the 10-50 keV electrons. The current technology allows a small-diameter focused beam of electrons to scan over a surface, while the EBL system does not need masks to perform its mask (unlike optical lithography, which uses photo-masks to project the patterns). An EBL system simply "draws" the pattern over the resist coated wafer using the electron beam. A typical EBL system consists of the following parts: 1) an electron gun or electron source that supplies the electrons; 2) an electron column using lenses and electrodes to "shapes" and focuses the electron beam; 3) a mechanical stage that positions the wafer under the electron beam; and 5) a computer system that controls the equipment.

Fig. 2.3 shows a typical EBL process from very beginning to final lift-off. Electron beam resist Polymethyl methacrylate (PMMA), with high resolution, is spin coated on the sample surface. Then e-beam expose the selected area, making the exposed area is soluble in the developer solution. After development, electron beam evaporator is used to deposit a layer of metal on the sample surface. Then lift-off is performed to remove the unexposed PMMA together with metal on it and leave the designed pattern filled with metal.

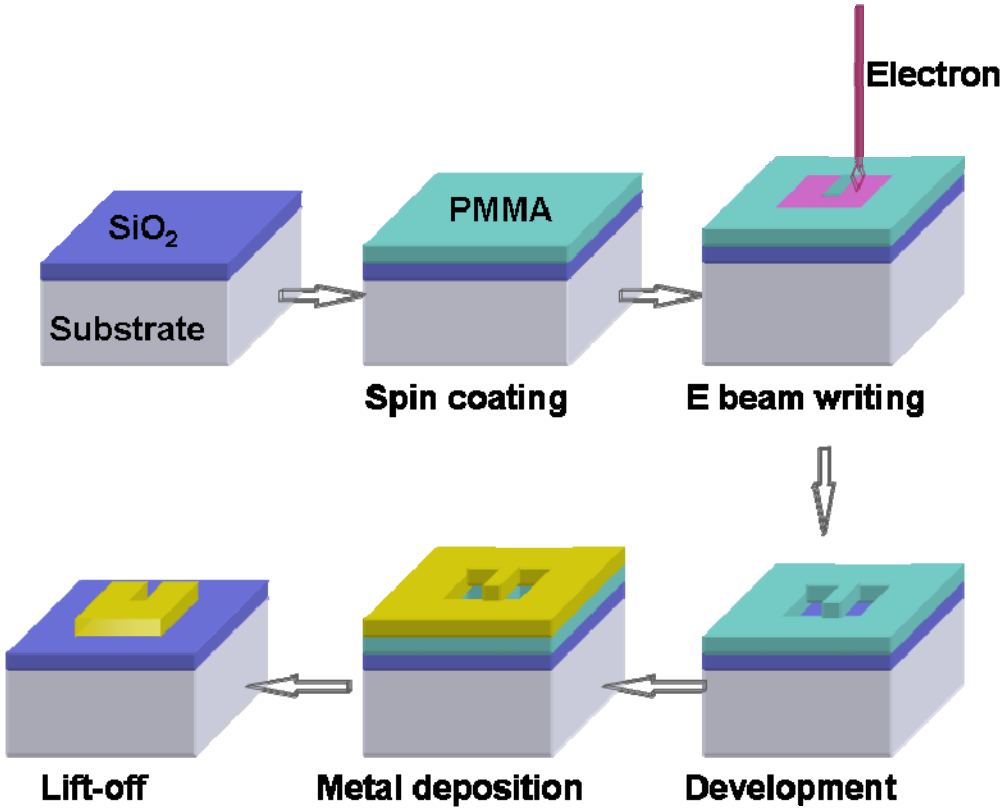

Fig. 2.3 The process of a typical electron beam lithography. The e-beam resist PMMA is coated on the substrate. E-beam writes on the designed region to expose the PMMA. The irradiated PMMA will be dissolved in the developer and then followed by metal deposition. Lift-off process will remove the metal on un-exposed PMMA and leave the designed pattern with metal.

Since the exfoliated graphene flakes have random location on the substrate, we will need to fabricate alignment marks close to the graphene flakes, which help the electrodes and other patterns to be located accurate on the desired location. Fig. 2.4 is the optical image of a typical graphene device.

2.3 Dual-Gate Graphene Field Effect Transistors

In order to make graphene devices to work in a similar way such as MOSFET,

we need to make top-gate graphene devices. Since we always have the back-gate, an additional gate will make the device a dual-gate device. The key challenge here is to make good quality top-gate oxide with low gate leakage current and the method by which oxide is deposit does not introduce substantial defects to the graphene.

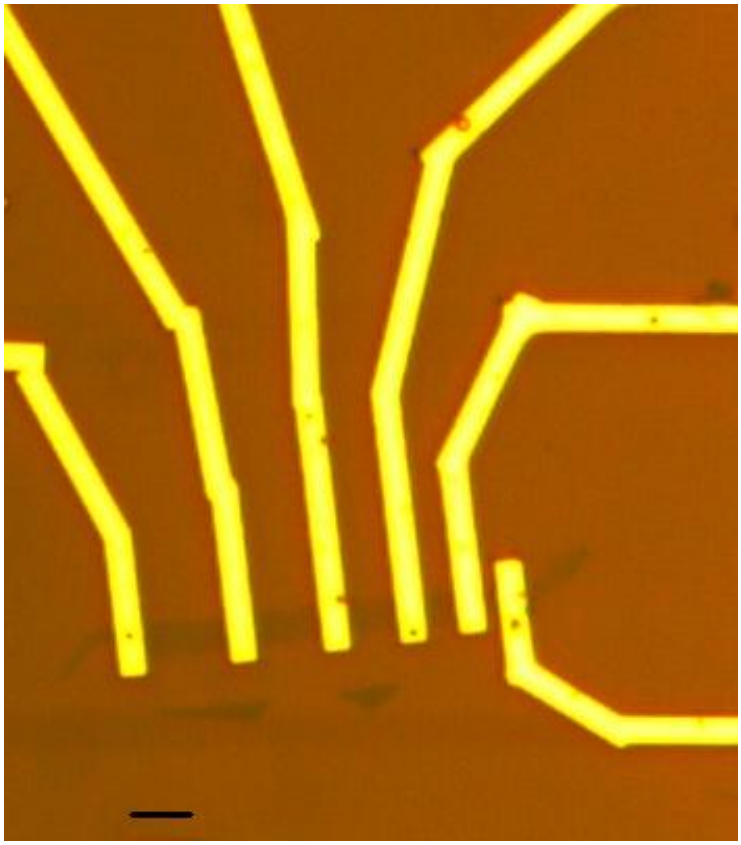

Fig. 2.4. Optical image of a typical graphene device made by EBL. The bluish color flake is graphene. The scale bar is 3 μm.

There are several methods of gate oxide deposition, such as PECVD, E-beam evaporation, atomic layer deposition (ALD), etc. PECVD requires plasma involved in the deposition process, however, plasma enhanced gases molecule will attack graphene surface and even remove it. E-beam evaporation needs to reach a very low pressure (10^{-9} torr) to get a high quality of oxide. In contrast, ALD does not needs that

high vacuum and the process will not generate energetic molecules, which is perfect for making top gate oxide for graphene.

However, the high quality clean graphene surface is hydrophobic, forbidden the direct ALD growth. A seeding layer that can help the following layer to grow uniform oxide is needed to coat on graphene. We here choose to deposit a thin layer of aluminum with 2 nm, and this aluminum can easily get oxidized in air so that it would not short the graphene channel, and this oxidized aluminum can provide a good surface for the next step of ALD [4]. The dual-gate graphene device fabrication is illustrated in the Fig. 2.5. The quality of this oxide stacking layer is proved by the very small gate leakage current and decent graphene device mobility.

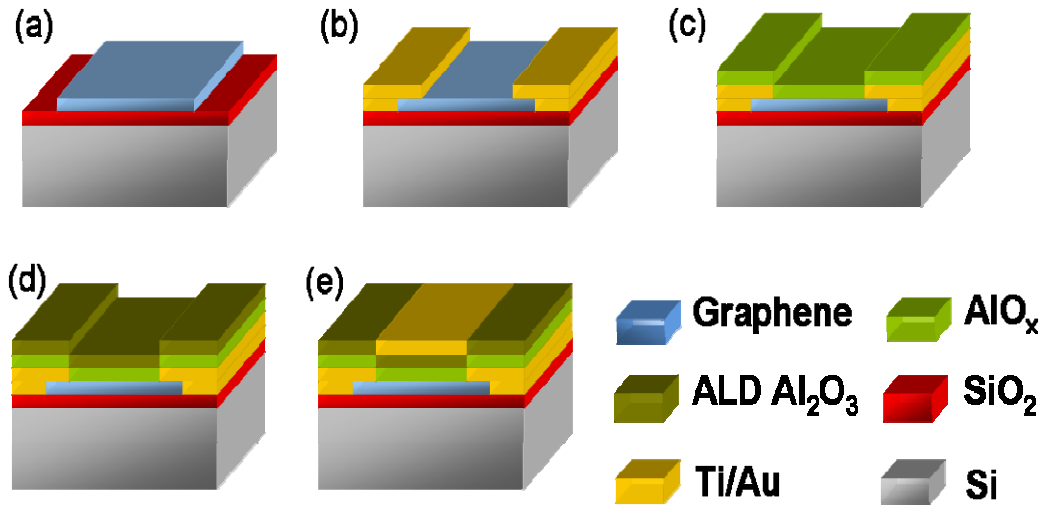

Fig. 2.5. Fabrication process of dual-gate graphene device. (a) Identify graphene flake on SiO_2 substrate. (b) Make source/drain contact by EBL and evaporation, the metal we use is Ti/Au (6/60 nm). (c) Deposit a thin layer of Al (2 nm) by evaporation, and store in air for self-oxidation. (d) Grow ALD oxide at low temperature 110°C. (e) Make gate electrode by EBL and evaporation.

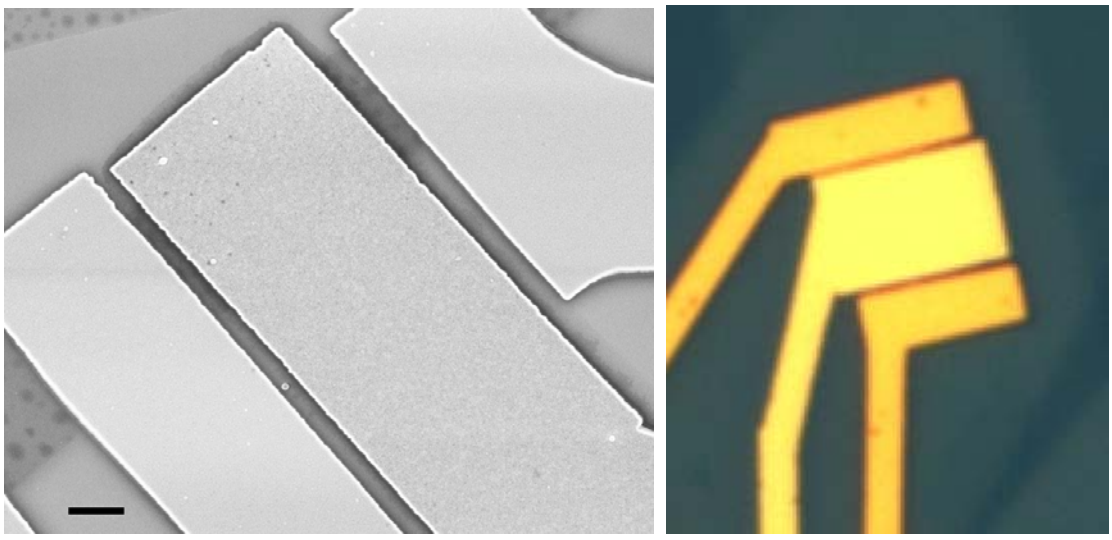

Fig. 2.6. (a) SEM image and (b) optical image of dual-gate graphene device. Scale bar is 1 μm.

2.4 Etching Graphene

Exfoliated graphene often has random shape as we transfer them on the substrate. When we want to study a regular shape or sometimes a specific designed shape, we need to pattern the graphene, and etch the excessive portion. This can be done by using EBL to draw a mask pattern and then use Oxygen Plasma to remove the uncovered regions.

We use reactive ion etching (RIE) tools to perform the graphene etching, the recipe is listed in below table. The etching speed of graphene is actually very fast considering the thickness is only 0.34 nm. It usually takes 6-8 sec to remove one layer using our recipe. The PMMA mask turns out to protect the un-exposed graphene very well. Fig. 7 shows the etching results that patterns a graphene flake into UCR logo and Nano-Device Laboratory logo.

RIE r.f. power	50 W
O_2 flow rate	50 sccm
Pressure	30 mTorr
Time	6-8 sec/layer
Mask	PMMA

Table 2.1. Oxygen Plasma etching recipe for etching graphene.

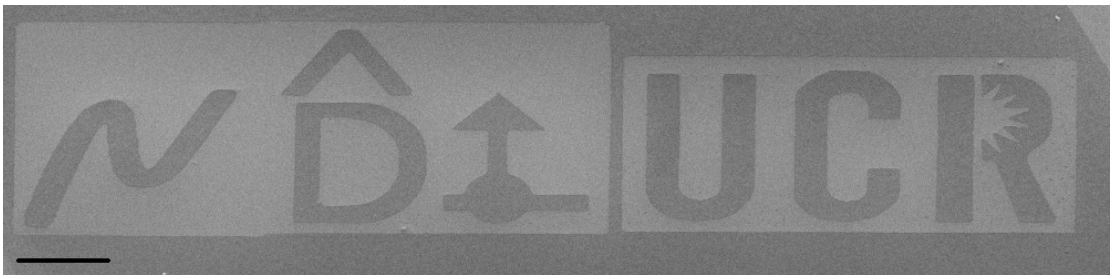

Fig. 2.7. Etching graphene into the pattern of Nano-Device Laboratory logo and UCR logo. The dark color regions are graphene and the light color is the substrate. The scale bar is 2μm.

Reference

[1] P. Blake, E.W. Hill, A.H.C. Neto, K.S. Novoselov, D. Jiang, R. Yang, T.J. Booth and A.K. Geim, *Appl. Phys. Lett.*, **91**, 063124 (2007)

[2] A.C. Ferrari, J.C. Meyer, V. Scardaci, C. Casiraghi, M. Lazzeri, F. Mauri, S. Piscanec, D. Jiang, K.S. Novoselov, S. Roth and A.K. Geim, *Phys. Rev. Lett.*, **97**, 187401 (2006).

[3] I. Calizo, F. Miao, W. Bao, C.N. Lau and A.A. Balandin, *Appl. Phys. Lett.*, **91**, 071913 (2007).

[4] S. Kim, J. Nah, I. Jo, D. Shahrjerdi, L. Colombo, Z. Yao, E. Tutuc and S. Banerjee, *Appl. Phys. Lett.*, **94**, 062107 (2009).

Chapter 3

Electrical Characterization Graphene Devices

3.1 Electrical Measurement of Back-Gate Graphene Device

Graphene is a very good conducting material considering its single atomic layer thickness. The sheet resistance at low temperature is around the 6.4 KΩ. What's more interesting is that the conductivity can be tuned by changing the Fermi level of graphene. Due to the linear dispersion E-k (energy-momentum) relationship, lifting (lowering) the Fermi energy in conduction (valence) band can increases the concentration of electron (hole), and thus increases the conductance of graphene. The Fermi level tuning is carried out by changing the gate voltage. Fig. 3.1 (a) shows an electrical measurement biasing condition of graphene back-gate device. The source is grounded and V_{DS} is applied on the drain. The V_{BG} is applied on the heavily doped silicon substrate which is used as a gate. Fig. 3.1 (b) shows a typical electrical result of transfer characteristics (I_{DS}-V_{BG}) of SLG back-gate device measured at room temperature. When fixing the V_{DS}, electrical current I_{DS} is recorded at different V_{BG} sweeping from -40V to 40V. Note that around zero back-gate voltage, the resistivity or sheet resistance for a 2D material, reach its maximum value at the charge neutrality point (Dirac point) with R_{CNP}=4 KΩ. This is because of the Fermi level is in line with the Dirac cone where the conduction band and valence band meet. This point has the minimum carrier (electron or hole) concentration. The R_{CNP} at room temperature is

smaller than at low temperature, which is due to the thermally excited carrier that can be frozen out at several Kelvin condition.

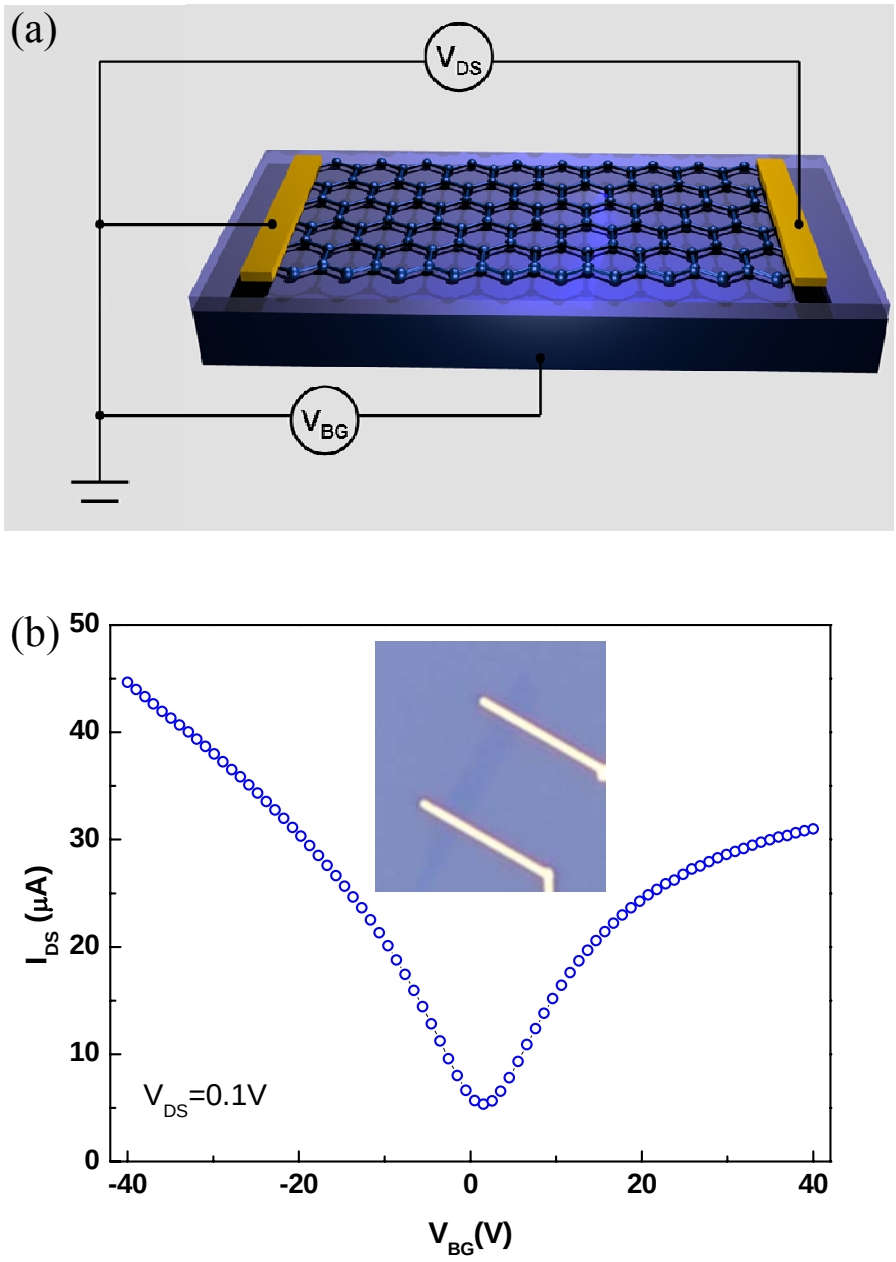

Fig. 3.1. (a) Schematics of electrical measurement of back-gate graphene device. (b) Typical I_{DS}-V_{BG} curve of SLG device with mobility as high as 6900 cm^2/Vs. The inset shows the optical image of this device.

As the gate voltage increases, the conductance of the graphene increases as

expected. According to Drude model $\sigma=\mu ne$, if we have the value for carrier concentration and the conductance, we can estimated the carrier mobility of graphene. The carriers are induced by the back gate capacitor, which can be considered as the parallel plate structure, $c_{BG}=\varepsilon_r\varepsilon_0/t$. For our substrate of 300 nm SiO_2, the $c_{BG}=0.115\times10^{-3}$ F/m^2. The mobility can be expressed as $\mu=(L/W)g_m/(c_{BG}V_{DS})$, where g_m is the transconductance of the device. For this particular device shown in Fig. 3.1 (b), the mobility is around 7000 cm^2/Vs. A common range of our SLG devices under ambient condition is 3000~10,000 cm^2/Vs.

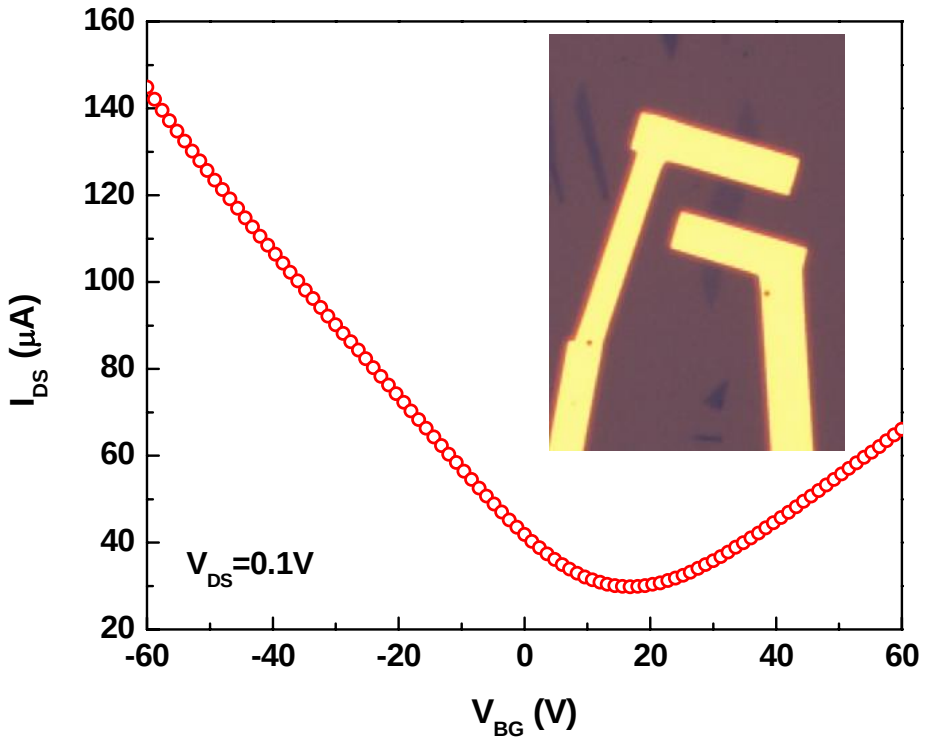

Fig. 3.2. Typical transfer characteristics of BLG back-gate device. The inset shows the optical image of the device.

For bilayer graphene (BLG), the electrical characteristic is different, especially in

the vicinity of Driac point. As shown in Fig. 3.2, the BLG exhibits slowly increased conductivity with increase of charge density comparing with SLG. The explanation is that a band gap will be induced when a perpendicular electrical field is applied on the BLG [1]. The carrier mobility of is lower comparing with SLG, usually below 2000 cm^2/Vs.

It is worth to mention the theoretical work that developed for graphene and its bi-layer counterpart by using tight-bonding approach [2]. For SLG, the Hamiltonian that describes the electronic properties near the Fermi level can be approximated as

$$H = \begin{pmatrix} 0 & \hbar v_F (k_x - ik_y) \\ \hbar v_F (k_x + ik_y) & 0 \end{pmatrix} \quad (1)$$

where k is the momentum and v_F is the Fermi velocity, $\hbar$ is the reduced Plunk constant. This Hamiltonian results in the Dirac-like linear dispersion relation between energy and momentum, $E=\pm \hbar v_F|k|$ [3]. The positive and negative correspond to the conduction band and valence band, respectively. When the two band meets, k=0, meaning no band gap.

In BLG, considering the Bernal stacking order, there are four bands, two low energy bands and two high energy bands. Considering the high energy band is about 0.3 eV higher than the low energy, which is usually difficult to active by the $\sim 10^{12}$ cm^2 density induced by back-gate, the transport is dominated by the low energy band. The Hamiltonian of low energy can be expressed as [1]

$$H = \begin{pmatrix} \Delta & -\frac{\hbar^2}{2m}(k_x - ik_y)^2 \\ -\frac{\hbar^2}{2m}(k_x + ik_y)^2 & -\Delta \end{pmatrix} \quad (2)$$

where Δ is the onset energy between the two layers. In absence of perpendicular electrical field, Δ=0, the Hamiltonian reduced to a spectrum similar to SLG, but with a parabolic dispersion relation $E=\pm\hbar^2k^2/2m$. With an applied perpendicular E field, Δ≠0, the band gap opens between conduction band and valence band. The band gap size depends on the E field [3].

3.2 Electrical Measurement of Dual-Gate Single Layer Graphene Device

The thickness of SiO_2 of typical back-gate graphene devices is about 300 nm, which to some extent is required since it offers the best optical contrast for this atomic thin material. However, this thickness is too big if we want to consider practical applications, such as transistors. The modern MOSFET has the gate oxide with EOT of a few nm [4]. We need to build dual-gate graphene devices with smaller thickness of oxide to demonstrate practical applications with graphene transistors. On the other hand, with an additional gate, we can bias the graphene under various conditions so that see more interesting phenomenon.

The details of the dual-gate device fabrications are described in Chapter 2. Here we show the IV characteristics of the dual-gate graphene device, where the top-gate oxide is made of self oxidized AlO_x, and ALD grown Al_2O_3. Fig. 3.3 shows the

measurement schematics of the dual-gate graphene device.

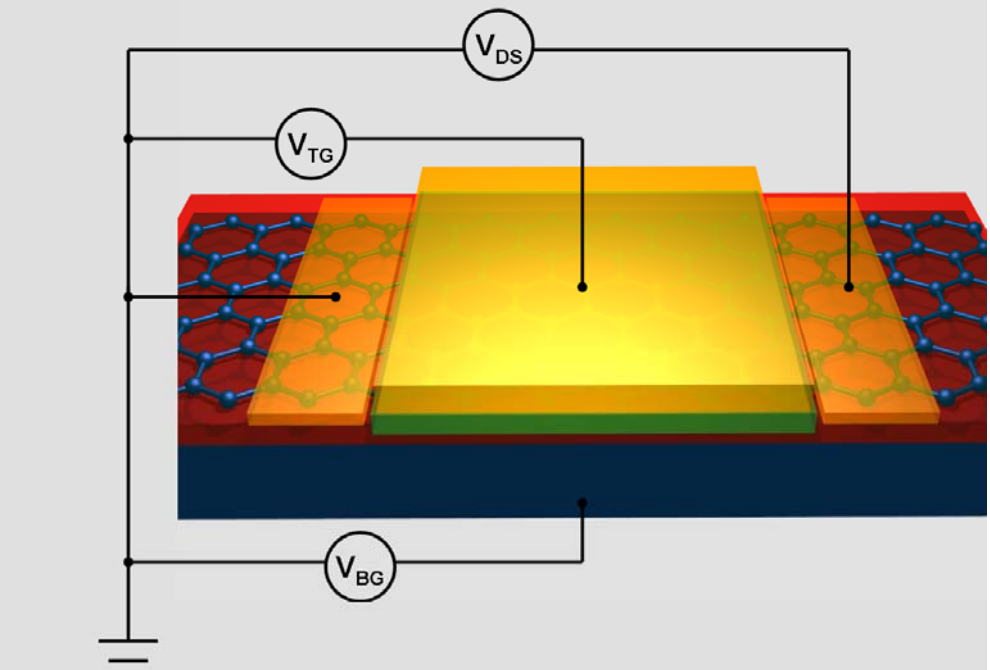

Fig. 3.3. Schematics of electrical measurement of dual-gate graphene device. The back-gate electrode can be used as an extra control node so that it can tune the transport independently with the top-gate.

Fig. 3.4 (a) shows the transfer characteristics (I_{DS}-V_G) of the dual-gate SLG device under different back-gate bias. The V_{DS} is fixed at 0.1V during this measurement. The inset pictures show the device before and after the top gate oxide and gate electrode fabrication. This device has the source drain separation of 5.38 μm, gate length 4.20μm and channel width 2.45 μm. The thickness of the oxide is about 23 nm. As shown in this figure that the CNP shifts to the negative voltage direction as the back-gate bias changes from -40V to 40V. Fig. 3.4 (b) shows the CNP position as a function of the V_{BG}. CNP appears when the charge induced by the top-gate and back-gate are canceled each other. Adopting the parallel plate capacitor model for

both gates, $c_{TG}/\Delta V_{TG}=c_{BG}/\Delta V_{TG}$, the slop of the fitting line in Fig. 3.4 (b) is the ratio of c_{BG}/c_{TG}. Since we know the c_{BG} =0.115×10^{-3} F/m^2, the c_{TG} is 2.56×10^{-3} F/m^2 [5, 6]. The current value at V_{TG}=10V has large difference, owing to the back-gate effect on the contact resistance and the access resistance. The as-fabricated dual-gate device is usually n-type doped due to the Al doping. As the V_{BG} changes from -40V to 40V, the access resistance decreases. Since the SLG has no band gap and band structure also does not influenced by the perpendicular electrical field, the conductance at the CNP stays constant with different back-gate bias, as shown in Fig. 3.4 (a). Fig. 3.4 (b) inset shows that the top-gate leakage is lower than 1 pA/μm^2 within the range of -10V to 10V. This value indicated very good insulating quality of the gate oxide.

Fig.3.5 (a) shows the transfer characteristics as a function of back-gate voltage under different top-gate bias. The I_{DS} experiences two valleys as the V_{BG} sweeps from -70V to 40V [7, 8]. This phenomenon is also related to the access regions which are not covered by the top-gate in graphene device. With different gate bias combinations, the graphene channel experiences different states, such as p-p-p, i-p-i, n-p-n, n-i-n, n-n-n, so that there are two local current minimums appearing as the V_{BG} sweeps. n, p and i here indicate n-type, p-type doping and intrinsic, respectively. It was also find that, with large top-gate bias, V_{TG}=-6V for example, a larger back-gate voltage is needed to change from on state to the next one, so that it appeared a more pronounced the “two valleys” effect. With small top-gate bias, this “two valleys” effect becomes weaker.

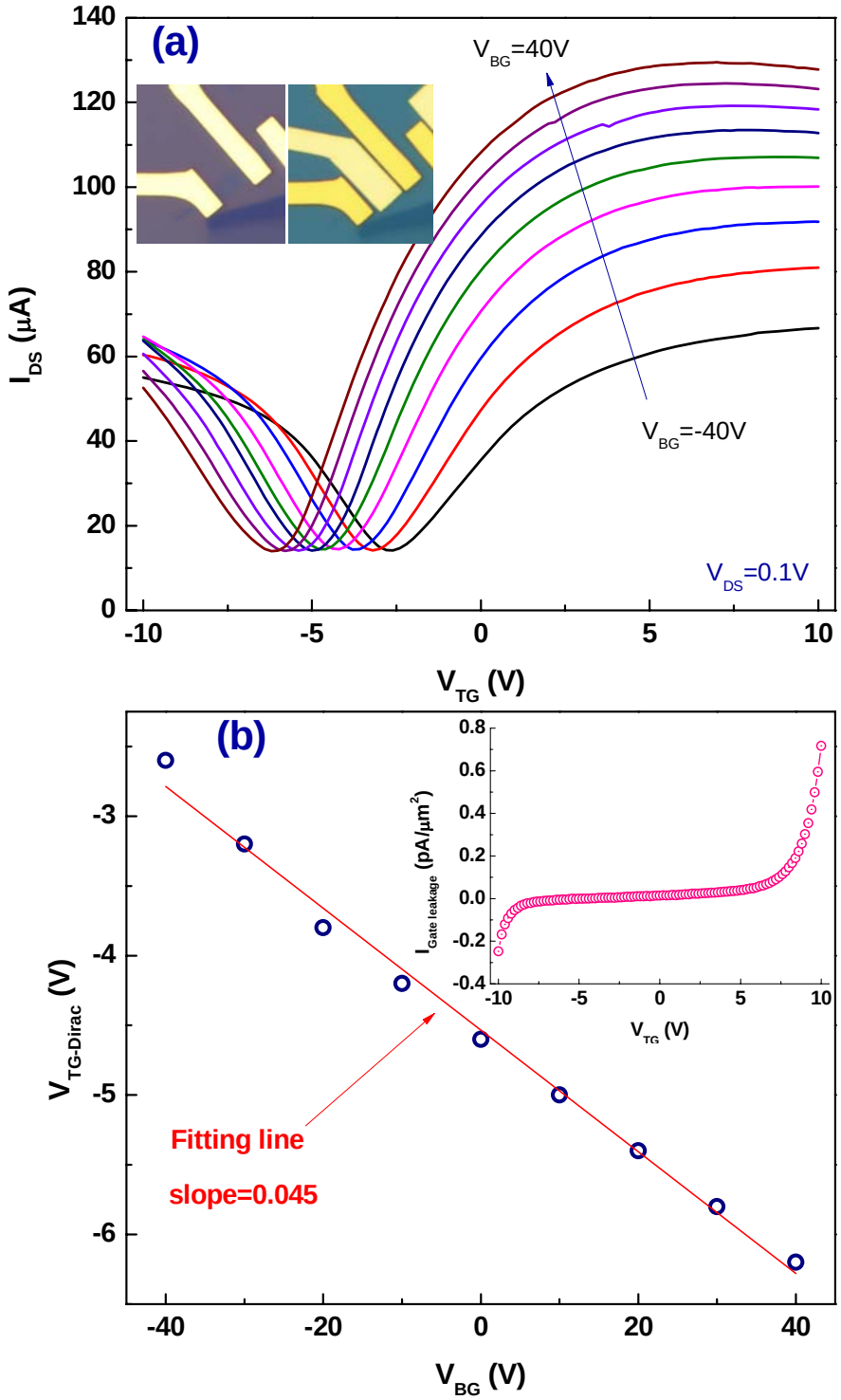

Fig. 3.4 (a) The current I_{DS} as a function of top-gate V_{TG} sweep under different back-gate V_{BG} bias. The shift of CNP with different V_{BG} reflects the electrostatic relatioship between top-gate capacitance and back-gate capacitance. The inset show the optical images of the graphene device before and after the fabircation of top-gate oxide and electrode. (b) The current I_{DS} as a function of V_{BG} sweep under different V_{TG} bias.

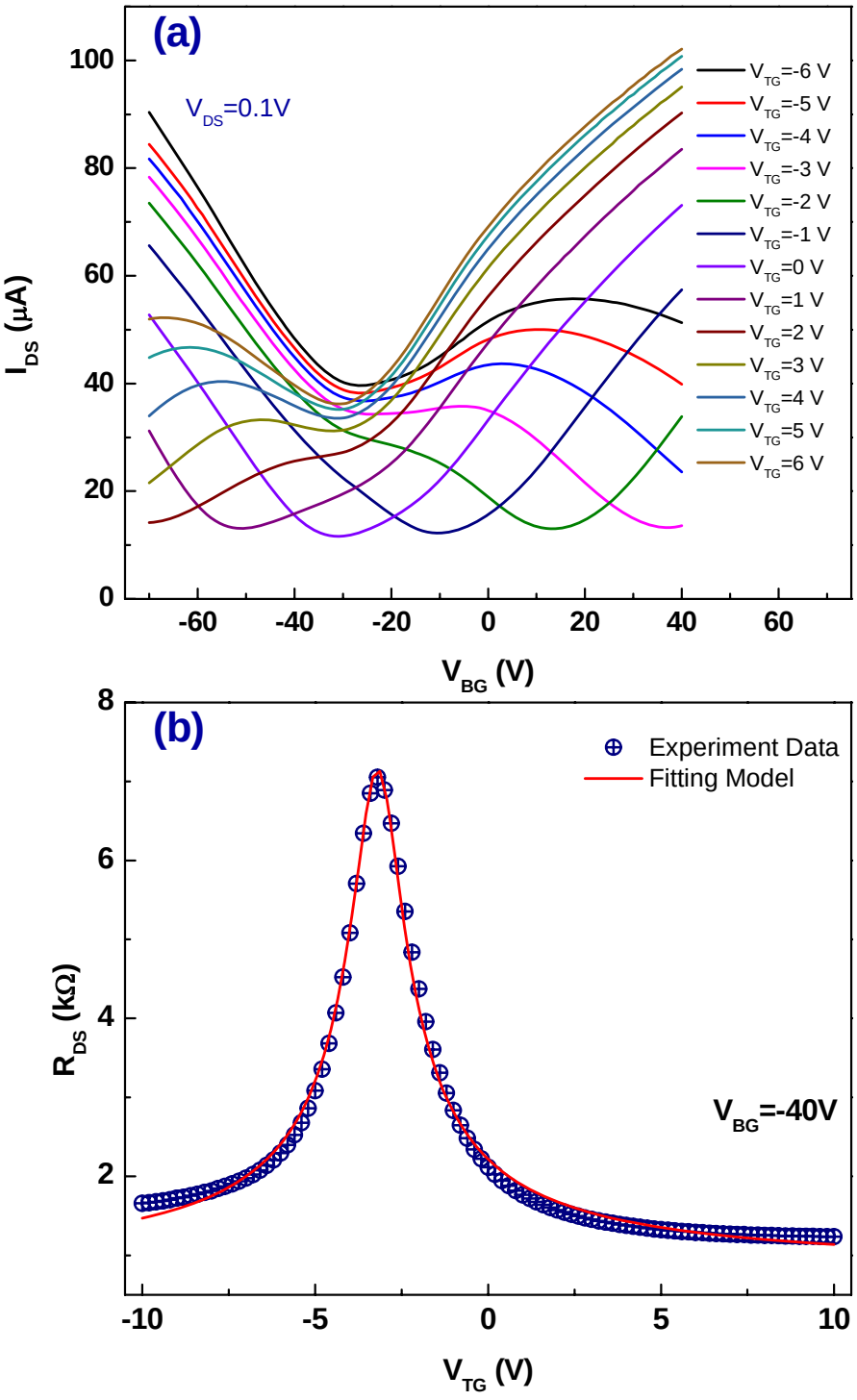

Fig. 3.5 (a) THe CNP position as a function of V_{BG}. The slop of the linear fitting line indicates the capacitance ratio of c_{BG} to c_{TG}. The inset shows the leakage current of the top-gate oxide, which is below 1 pA/μm2 within the range of -10V to 10V. (b) The fitting results based on the resistance model of graphene dual-gate transistor.

The mobility of the device can be estimated from the following expression for dual-gate graphene device, $R_{DS}=2R_C+L/W/[\mu\times e\times\sqrt{(n_0^2+n_g^2)}]$, where R_{DS} is the total resistance, R_C is the sum of contact resistance and access resistance, L is the gate length, W is the channel width, μ is the mobility, e is the elementary charge, n_0 is the residue charge which is due to the impurity scattering and thermal emission, $n_g= |c_{TG} \times(V_{TG}-V_{TG-CNP})/e+ c_{BG}\times(V_{BG}-V_{BG-CNP})/e|$, $c_{TG}=2.56\times10^{-3}$ F/m^2 is top-gate capacitance as extracted, $c_{BG}=0.115\times10^{-3}$ F/m^2 is back-gate capacitance, V_{TG-CNP} (V_{BG-CNP})is the charge neutrality point of top-gate (back-gate) voltage [9]. Fig 3.5 (b) shows the fitting results under the condition of V_{BG}=-40V using the model established above. The extracted mobility is 1360 cm^2/Vs, residue carrier concentration is 1.18×10^{-12} cm^2 and the contact resistance is 390 Ω (contact resistivity ~1kΩ-μm).

The output characteristics (I_{DS}-V_{DS}) of graphene dual-gate transistor is also measured and shown in Fig. 3.6. In the low-field case (small V_{DS}), the SLG exhibits linear relation of I_{DS}-V_{DS}, as shown in Fig. 3.6(a). However, as we bias the graphene device under the high-field condition with larger V_{DS} (E~10^4 V/cm), the linear relationship do not hold any more. Current saturation effect starts to appear around V_{DS}=1V, and even below with certain gate voltage, as shown in the Fig. 3.6 (b).

Saturation is important for analog applications, since it directly relates to the gain of the transistors. The gain $A_V=g_mR_O$, where g_m is the transconductance and R_O is the output resistance. A larger gain is preferred, so as the R_O. When saturation happens, the I_{DS} is less effected by the V_{DS}, meaning the dynamic resistance is large.

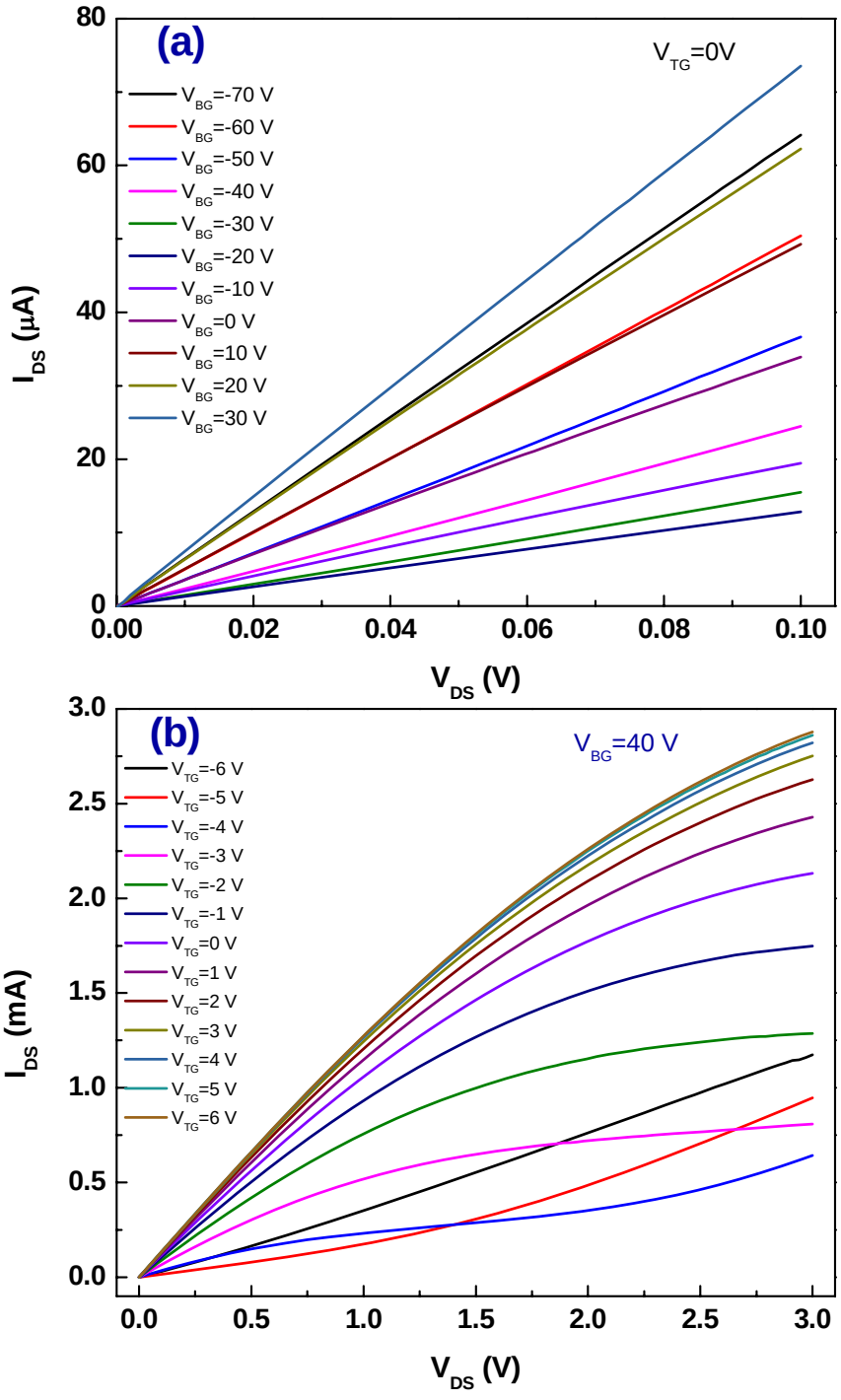

Fig. 3.6 (a) Low-bias (I_{DS}-V_{DS}) output characteristics of dual-gate SLG transistor. Linear relation is observed under various gate voltage. (b) High-bias output characteristics of dual-gate SLG transistor under different top-gate voltage at fixed back-gate V_{BG}=40V. Current saturation appears, especially at V_{TG}=-3V. Another type of de-saturation IV curve appears when V_{TG}=-4V, showing the current saturates at certain value of V_{DS}, but with V_{DS} increases, current becomes not saturates again.

In conventional MOSFET, saturation happens when the V_{DS} is large enough to pinch-off the channel, so that the current do not increase much there after [10]. However, unlike the Si and other semiconductor material, there is no full saturation happening on graphene. The reason is that graphene is a zero band gap material, and the ambipolar property allows both electrons and holes to transport in the same graphene flake [9]. Also, almost no energy loss when the transition from electron to hole happens in graphene [11]. Therefore, no pinch-off happens on graphene, which in turn results in no full current saturation. Nevertheless, certain level of saturation still appears at high-field. For example, as Fig. 3.6 (b) shows, when V_{TG}=-3V, the differential resistance at high V_{DS} is 20 times larger than at small V_{DS}. Another type of IV de-saturation curve appears on graphene dual-gate devices, such as the one when V_{TG}=-4V. The current saturates at certain value of V_{DS}, but with V_{DS} increases, current becomes not saturates again.

Both the saturation and the de-saturation effects on graphene dual-gate device can be explained by Fig. 3.7. The side-view of the graphene top-gate device is sketched in Fig. 3.7 (a). Under certain gate bias and small V_{DS}, the charge is uniformly distributed across the channel, as shown in Fig. 3.7 (b), where pink color represents p-type doping. As the V_{DS} increases, the gate voltage on the drain side V_{GD} becomes substantially different with the source side V_{GS} so that the charge distribution is not uniform any more. If the source side is p-type doping, the drain side is be much less p-type doped and even neutral, shown in dark region in Fig. 3.7 (c).

The graphene channel now can be regards as two connecting channels with different CNP point, where one is several volts smaller than the other. So the overall behavior is that the CNP conductance valley becoming wider and shifting to the positive side as the V_{DS} increases, as shown in the experimental results Fig. 3.7 (d). As a result, a region where many curves overlap each other appears. If we draw a vertical line "I" (meaning at certain gate bias) on Fig. 3.7 (d) across this region, we will see very good current saturation at this gate bias. Similarly, if we bias at a different gate voltage, which is equivalent to draw another vertical line, for example line "II", we see that this line passes through a dense region and then entering a less dense region. This is what happens when the de-saturation occurs. Note in Fig. 3.7 (d), the I_{DS}-V_{GS} are measured under different V_{DS} bias from 0.1V to 3.7V with 0.3V as step size. The intersect points of any vertical line with the family of the IV curves can be regarded as a linear sweep of I_{DS}-V_{DS}. When the V_{DS} keeps increasing, the local gate bias at the drain side could induce n-type doping. Since there is no band gap in graphene, the transition of carrier from hole to electron happens with almost not energy loss. Hence the pinch-off, which occurs in other semiconductors, such as Si, is not likely happens in graphene.

Since the saturation is very important to the analog applications, and it is found in graphene that the saturation is not as good as in other semiconductors, new designs of device structure and operation ranges are needed to be explored.

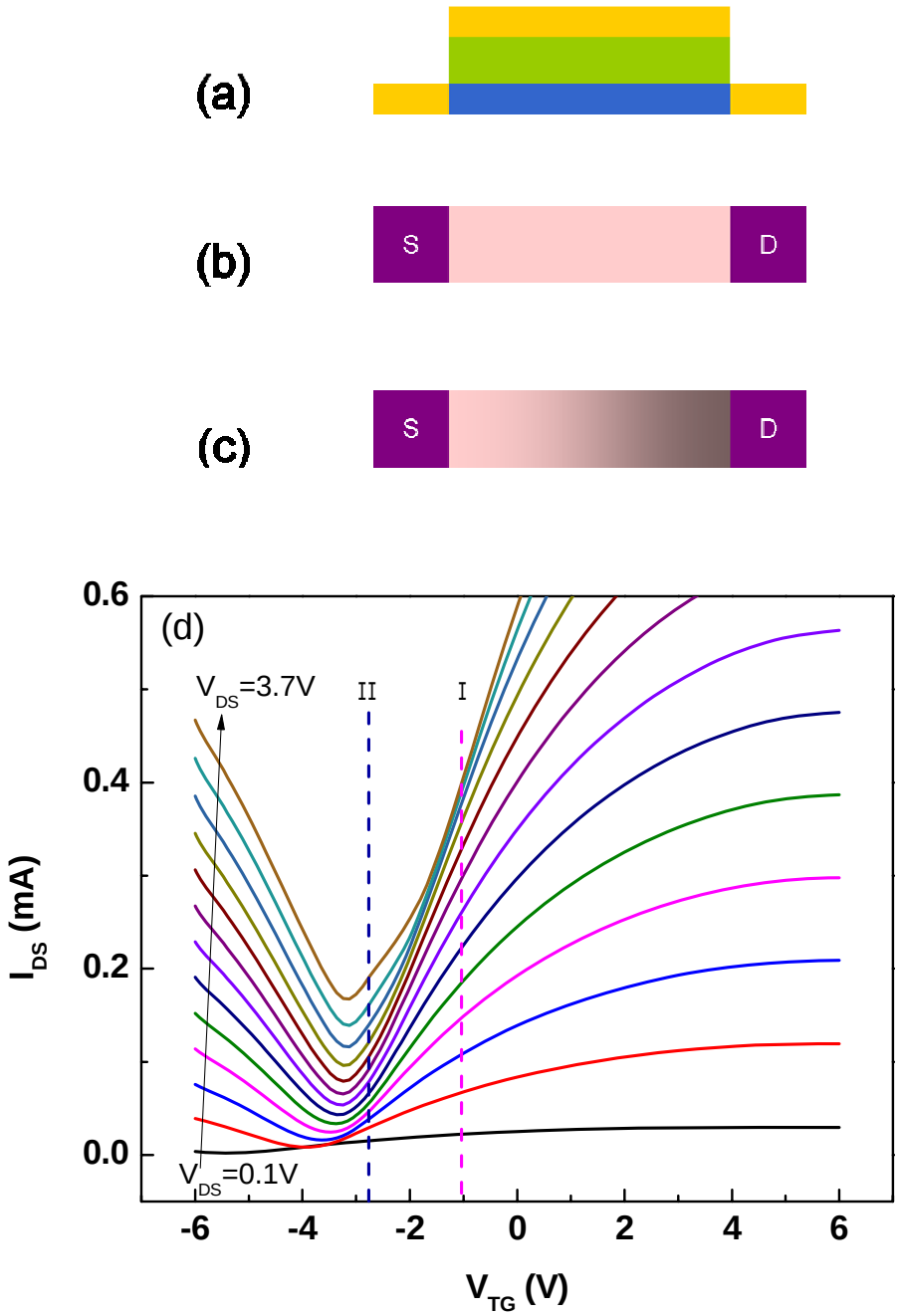

Fig. 3.7. Explanation of the saturation and de-saturation effects on graphene dual-gate devices. (a) Schematic of graphene to-gate device. (b) Uniform charge distribution in graphene channel when V_{DS} is small. Pink color represents the p-type doping. (c) As the V_{DS} increases to a large enough value, the charge would not be distributed uniformly in the graphene channel as the gate bias is different at different location of the channel. Dark color represents the less p-type doping. (d) Experimental results of I_{DS}-V_{GS} under different V_{DS} bias from 0.1V to 3.7V with 0.3V as the step. The CNP position shifts to the positive side and the conductance valley becomes wide as the V_{DS} increases. Two vertical lines "I" and "II" across the curves represent the cases of good current saturation and de-saturation.

3.3 Electrical Measurement of Dual-Gate Biayer Graphene Device

Dual-gate BLG device is very interesting to study since the band structure is parabolic instead of linear in SLG case. Moreover, a band gap can be induced by applying a perpendicular electrical field in BLG system [12-16]. The device fabrication process is the same as the SLG graphene device mentioned above. The only difference here is that the oxide is HfO_2 and self oxidized AlO_x with total thickness of ~13 nm. Fig. 3.8 shows the electrical measurement results. There are several distinctive differences with SLG and one of the most interesting ones is the induced band gap by perpendicular electrical field. As one can see in Fig. 3.8 (a), the conductance at CNP experiences an evolution of increase and decrease as the back-gate voltage changes from -70V to 50V. This is a direct result of band gap induced in BLG system. The band gap induced by the E filed can be estimated by $R_{CNP} \propto \exp(E_g/2k_BT)$ at different gate bias [14, 16]. Since the I_{CNP} is maximum when V_{BG}=-20V, it can be treated as no gap case. The induced band gap can be expressed as $E_g=2k_BT\times\ln(R_{CNP(VBG)}/R_{CNP(-20)})$, where is 26 meV at room temperature. At the charge-neutrality condition, $D \approx \varepsilon_{SiO2}(V_{BG}-V_{BG-CNP})/d_{SiO2}$, where ε_{SiO2} (~3.9) is the dielectric constant of the back gate oxide, V_{BG-CNP} is the Dirac offset voltage (-20 V here), and d_{SiO2} (300 nm) is the thickness of the back gate oxide. Fig. 3.9 shows the relation between average electical displacement D_{ave} field and the induced band gap in BLG device. With =0.9 V/nm, the band gap is about 35 meV. The inset shows the R_{CNP} as a function of back-gate voltage, comparable with results from others [14, 16].

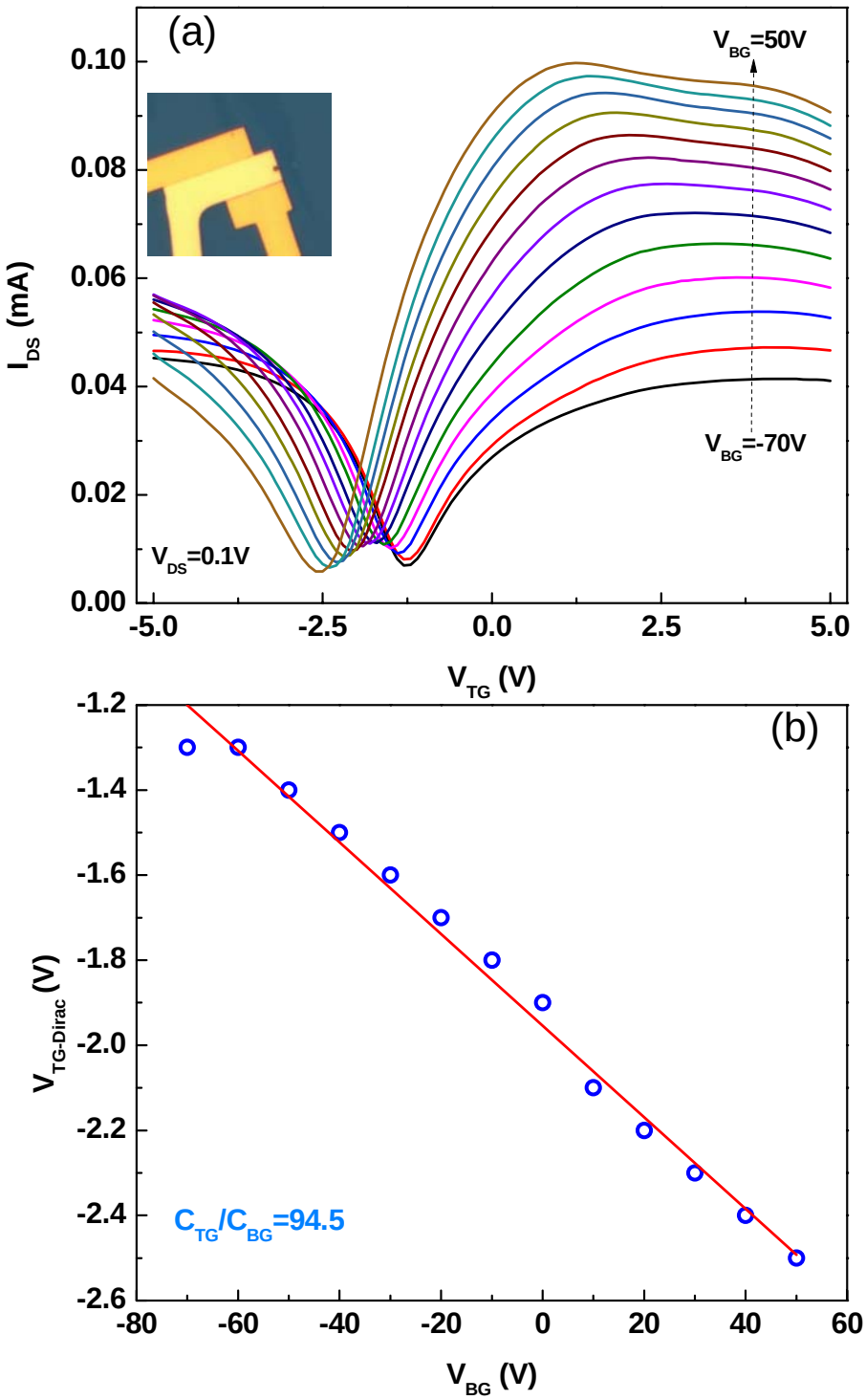

Fig. 3.8. Electrical characteristics of dual-gate BLG device. (a) I_{DS} as a function of V_{TG} under different V_{BG} bias. The I_{DS} is not constant under different V_{BG} indicating an E filed induced band gap in BLG system. The conductance at high carrier concentration exhibits negative transconductance behavior. (b) The charge neutrality point V_{TG-CNP} as a function of V_{BG}. The slop reflects the capacitance ratio of of c_{TG}/c_{BG}=94.5.

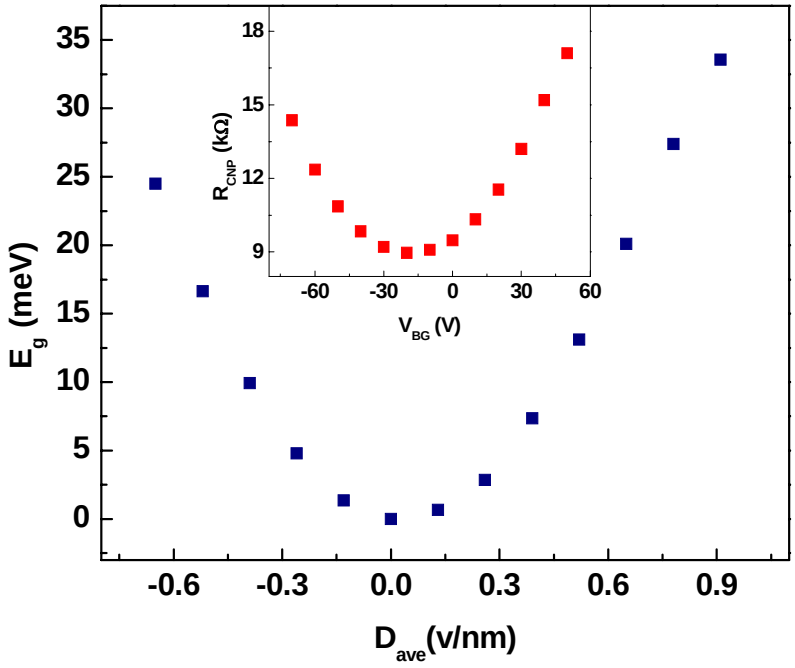

Fig. 3.9. The electrical filed induced band gap versus back-gate bias. The inset shows the peak resistance value under different back-gate bias.

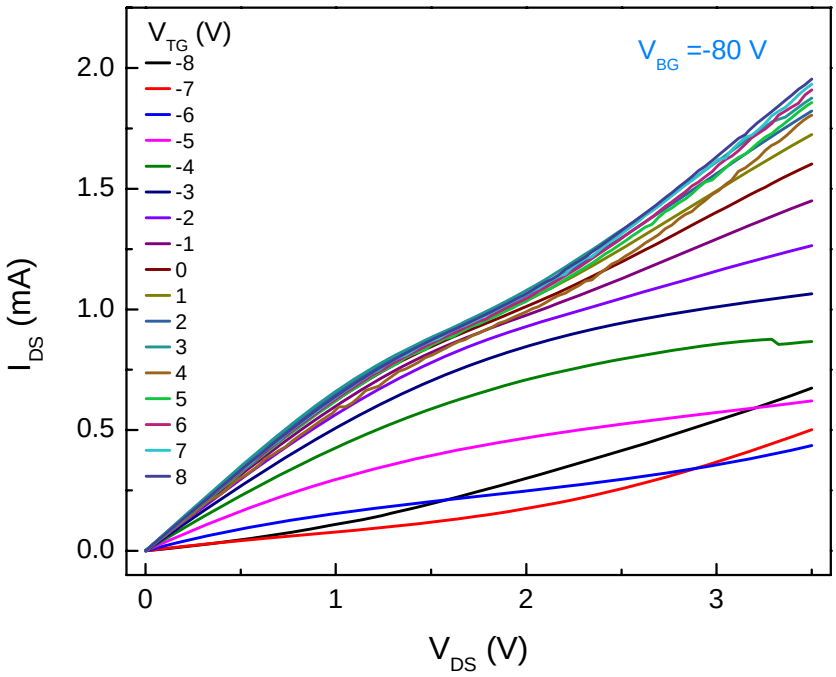

Fig. 3.10. High field electrical measurement of dual-gate BLG devices. No strong saturation effect appears

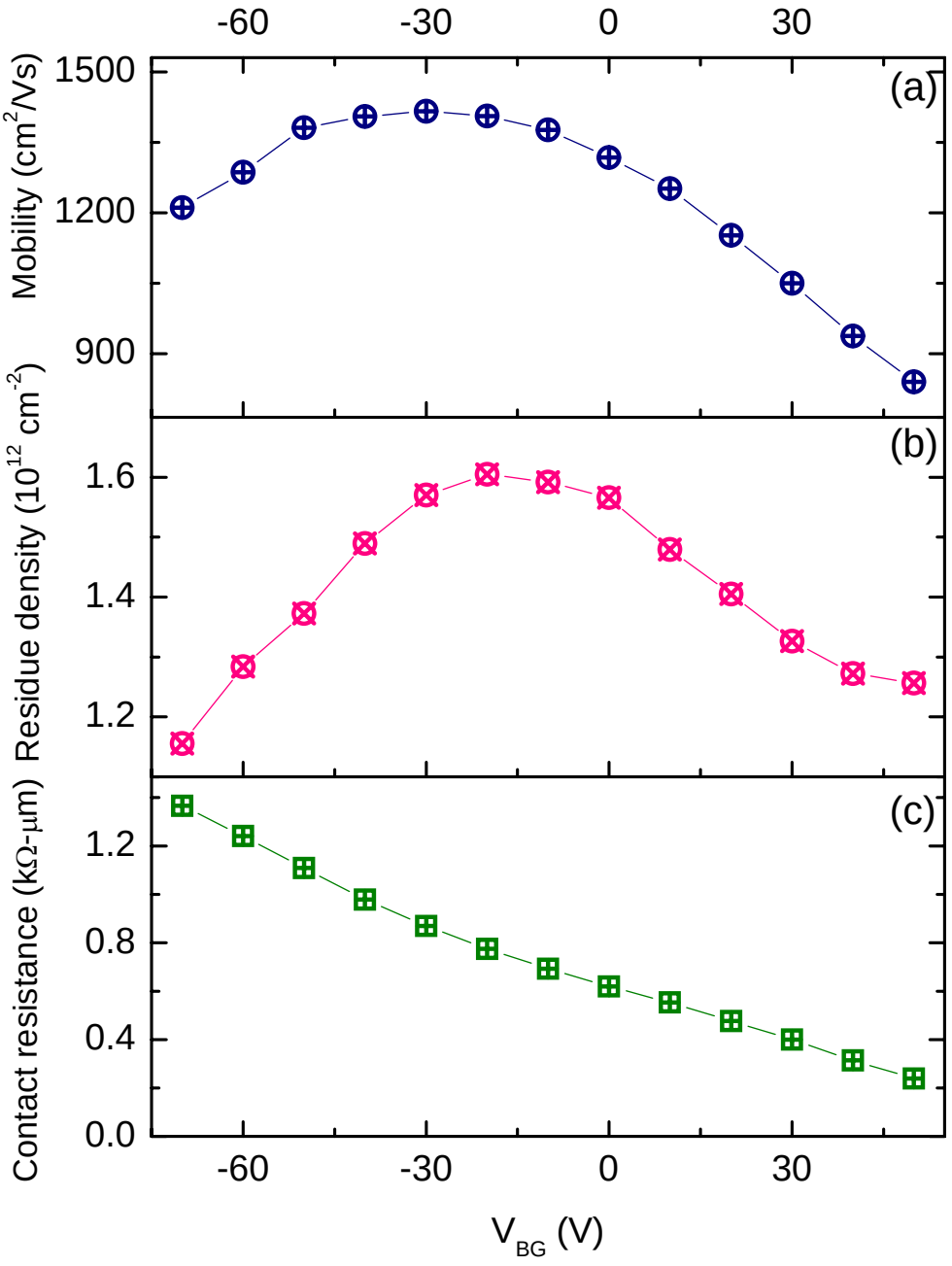

Fig. 3.11 (a) The carrier mobility as a function of V_{BG}. The maximum value happens when the gate induced band gap is zero, at V_{BG}=-30~20V. With the increasing of the band gap, mobility decreases. (b) The residue carrier concentration reflects the conductivity at the CNP, which also related to the band gap. (c) The width normalized contact resistance decreases as the back-gate voltage increases.

The High filed measurement (larger V_{DS}) is also conducted in BLG system. Since the weak saturation effect in SLG is in part due to the absence of band gap, it is expected that a more prominent saturation effect would be appear in BLG. However, the saturation is also not strong in our BLG devices. This is probably because the band gap induced is too small, shown in Fig. 3.10.

The carrier mobility of our BLG dual-gate devices is estimated by the same method mentioned above for SLG dual-gate devices. The extraction of the top-gate capacitance is by fitting the relation of the V_{TG-CNP} with V_{BG}, as shown in Fig. 3.8 (b). The slop indicates the capacitance ratio of c_{TG}/c_{BG}=94.5. The c_{TG} is 10.87×10^{-3} F/m^2, considering the c_{BG} is 0.115×10^{-3} F/m^2. The dielectric constant ε_{HfO2} is estimated to be 16, which is a reasonable value for low-temperature ALD grown HfO_2 [9].

Since the band-gap induced by the gate voltage, the mobility is not a constant as the back-gate bias changes. As one can see from the Fig. 3.11 (a), the mobility reaches the maximum value around V_{BG}=-20~-30V, this is the region where no significant band gap created. With the back-gate voltage increasing (smaller than -30V or larger than -20V), the mobility starts to decrease monotonically. This is expected since the band gap would reduce the mobility. The residue concentration, shown in Fig. 3.11(b), is directly related to the conductivity at the CNP. The maximum value happens at the V_{BG}=-20V, which consists with the results in Fig. 3.8(a). The contact resistance is represented with the width normalized unit, kΩ-μm, same as the conventionally used unit for MOSFET. Since our devices have the

channel region covered by the top-gate, the access region between the drain/source and the edge of the top-gate is very small, <50nm, comparing with the μm scale device channel. The contact resistance here should not include much of the access resistance. Fig. 3.11(c) shows the contact resistance changes from 1.2 kΩ-μm to 0.2 kΩ-μm as the back-gate voltage sweeps from -70 to 50V.

Another interesting behavior on dual-gate BLG is the negative transconductance with increasing of carrier density at very high carrier concentration $n>10^{13}$ cm^{-2}, as shown in Fig. 3.8 (a). The conductivity of BLG reaches a maximum value and then decreases with the increase of gate voltage. In the back-gate device, the maximum carrier concentration induced by the back-gate voltage is usually less than 7.2×10^{12} cm^{-2}, considering the conventionally used 300 nm SiO_2 and common instrument limit of 100V. With high-k dielectric material, HfO_2 or Al_2O_3 as top-gate oxide, one can reach a much higher carrier concentration of $n>10^{13}$ cm^{-2}. Owing to the high quality of our dual-gate device, we can apply large gate voltage up to ±10 V even with gate thickness of 13nm. As mentioned above that the c_{TG} is 10.87×10^{-3} F/m^2, we can apply the carrier concentration up to 7×10^{13} cm^{-2}, about one order of magnitude larger than by 300 nm SiO_2 back-gate.

This negative transconductance behavior is only observed before with electrolyte gate, where the dielectric constant is much larger [17-19] than common solid state oxide. Our result is the first one, as best to our knowledge, that observes this phenomenon with a solid state gate dielectric. As shown in Fig. 3.8 (a), the negative

transconductance effect tends to be stronger as the V_{BG} increases from -70V to 50V. At V_{BG}=50V, the conductance drop ~10% as we compare the conductance of peak value with that of at V_{TG}=5V. This behavior can be understood by activation of high energy in BLG system.

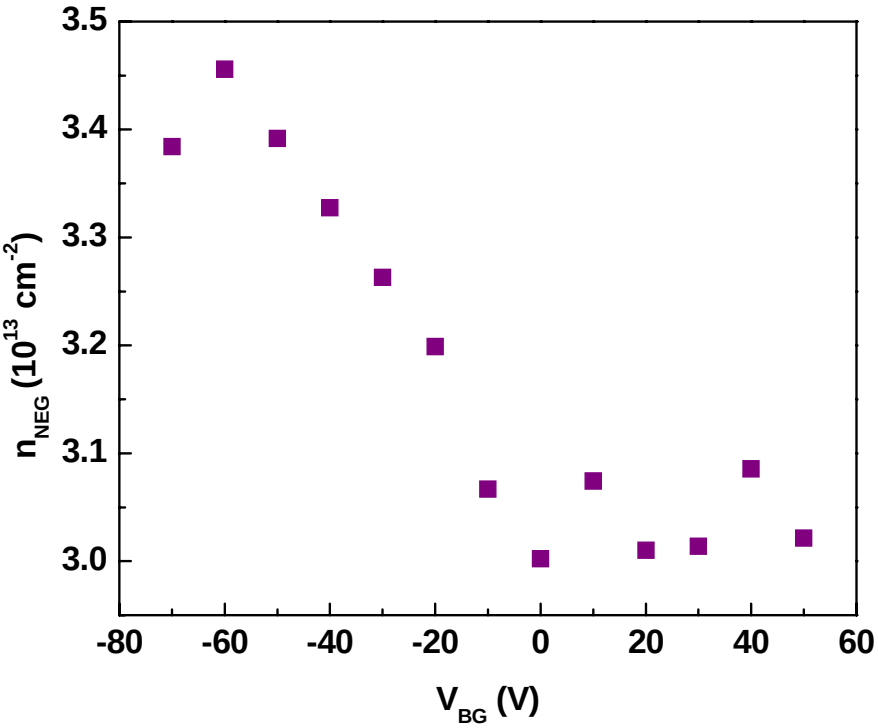

Fig. 3.12. The carrier concentration when the negative transconductance appears as a function of back-gate bias. The value of n_{Neg} is about ~3×10^{13} cm^{-2}, which corresponds to the gap energy from high energy band to low energy band in BLG.

BLG has four bands, while two low energy ones meet at zero energy and two high energy ones split away from zero energy with $\pm\gamma_1$. With increasing of carrier concentration, the Fermi level is being pulled down (up) towards the high energy band of BLG in valence band (conduction band). The hole (electron) density at which the higher band starts to be filld is $n=g\gamma_1/(2\pi\hbar^2v^2)\approx3\times10^{13}$ cm^{-2}. γ_1 is 0.377 eV [20], g is

4 here considering the valley degeneracy 2 and spin degeneracy 2, v is the Fermi velocity 1.01×10^6 m/s [21]. The carrier density is calculated at which the peak conductance appeas by $n_{Neg}= c_{TG}\times(V_{TG\text{-}Neg}-V_{TG\text{-}CNP})/e+ c_{BG}\times(V_{BG}-V_{BG\text{-}CNP})/e$. Fig. 3.12 shows the n_{Neg} as a function with V_{BG}. The n_{Neg} is $\sim3\times10^{13}$ cm^{-2}, which indicates that the negative transconductance is probably due to the activation of high energy band of BLG. While in this band, the intraband scattering starts to play an important role to reduce the carrier transport.

Reference

[1] E. McCann, and V.I. Fal'ko, *Phys. Rev. Lett.*, **96**, 086805 (2006).

[2] P.R. Wallace, *Phys. Rev.*, 71, **622** (1947).

[3] A.H. Castro Neto, F. Guinea, N.M.R. Peres, K.S. Novoselov and A.K. Geim, *Rev. Mod. Phys.*, **81**, 109 (2009).

[4] International Technology Roadmap for Semiconductors 2011 Edition, Front End Processes (2011).

[5] S. Kim, J. Nah, I. Jo, D. Shahrjerdi, L. Colombo, Z. Yao, E. Tutuc, and S. Banerjee, *Appl. Phys. Lett.*, **94**, 062107 (2009).

[6] D. Farmer, Y.-M. Lin, and P. Avouris, *Appl. Phys. Lett.*, **97**, 013103 (2010).

[7] B. O¨zyilmaz, P. Jarillo-Herrero, D. Efetov, D.A. Abanin, L.S. Levitov and P. Kim, *Phys. Rev. Lett.*, **99**, 166804 (2007).

[8] B. Huard, J.A. Sulpizio, N. Stander, K. Todd, B. Yang and D. Goldhaber-Gordon, *Phys. Rev. Lett.*, **98**, 236803 (2007).

[9] I. Meric, M.Y. Han, A.F. Young, B. Ozyilmaz, P. Kim and K. L. Shepard, *Nat. Nanotechnol.*, **3**, 654–659 (2008).

[10] Y. Taur and T.H. Ning, Fundamentals of Modern VLSI Devices. New York, NY: Cambridge University Press, 2009.

[11] M.I. Katsnelson, K.S. Novoselov and A.K. Geim, *Nat. Phys.*, **2**, 620 (2006).

[12] A.H. Castro Neto, F. Guinea, N.M. R. Peres, K.S. Novoselov and A.K. Geim, *Rev. Mod. Phys.*, **81**, 109, (2009).

[13] J.B. Oostinga, H.B. Heersche, X. Liu, A.F. Morpurgo and L.M.K. Vandersypen, *Nat. Mat.* , **7**, 151 (2008).

[14] F. Xia, D.B. Farmer, Y.-M. Lin and P. Avouris, *Nano Lett.*, 10, 715 (2010).

[15] Y. Zhang, T.-T. Tang, C. Girit, Z. Hao, M.C. Martin, A. Zettl, M.F. Crommie, Y.R. Shen and F. Wang, *Nature*, **459**, 820 (2009).

[16] B.N. Szafranek, D. Schall, M. Otto, D. Neumaier and H. Kurz, *Appl. Phys. Lett.*, **96**, 112103 (2010).

[17] J. Ye, M.F. Craciun, M. Koshino, S. Russo, S. Inouea, H. Yuan, H. Shimotani, A. F. Morpurgo and Y. Iwasa, *PNAS*, **108**, 13002 (2011).

[18] D.K. Efetov, P. Maher, S. Glinskis and P. Kim, *Phys. Rev. B*, **84**, 161412 (2011).

[19] Z.Q.Li, E.A. Henriksen, Z. Jiang, Z. Hao, M.C. Martin, P. Kim, H.L. Stormer and D.N. Basov, *Phys. Rev. Lett.*, **102**, 037403 (2009).

[20] B. Partoens and F.M. Peeters, *Phys. Rev. B.*, **74**, 075404 (2006).

[21] G.M. Rutter, S. Jung, N.N. Klimov, D.B. Newell, N.B. Zhitenev and J.A. Stroscio, *Nat. Phys.*, **7**, 649 (2011).

Chapter 4

Analog Applications of Graphene

4.1. Introduction

Owing to its very high carrier mobility up to 15,000 cm^2/Vs even at room temperature, graphene has been proposed as the material for high frequency electronics [1]. Several groups have demonstrated that graphene transistors can be operated at >100 GHz [2-4]. Analog applications such as frequency doubler [5], amplifier [6], phase shift keying, frequency shift keying [7] and phase detector [8] have been experimentally shown using graphene transistors and circuits.

4.2. Phase Shift Keying and Frequency Shift Keying

Besides the high carrier mobility, another important property of graphene is the ambipolar transport, where n-type and p-type can be achieved by just change the gate bias. Taking advantage of this ambipolarity of graphene, we demonstrated the circuits that achieve the functionalities such as frequency shift keying (FSK) and phase shift keying (PSK) by using single graphene device which greatly simplify the circuitry.

The single-transistor amplifier, which consists of one transistor and one load resistor, is one of the most basic and important building blocks in analog circuits. There are three types of single-transistor amplifiers: common-source, common-drain, and common-gate, each of which exhibits different characteristics. One of the key

differences between the three types of amplifiers is the small-signal voltage gain, defined as V_{out}/V_{in}. The common-source amplifier provides negative gain, whereas the common-drain and common-gate amplifiers provide positive gain. Since different applications usually prefer different types of single-transistor amplifiers, it would be very attractive if the same amplifier can be configured in-field into more than one type. However, in Si based metal-oxide-semiconductor field effect transistor (MOSFET) technology, the type of an amplifier is only dependent on its physical configuration, i.e., the node where the input V_{in} is applied, the node where the output V_{out} is obtained, and the placement of the resistor. Therefore, in-field configuration of an amplifier is usually infeasible since the physical configuration of the amplifier is determined during fabrication.

With graphene as the channel material, by properly adjusting the gate-source voltages, the transistor can be switched from n-type to p-type, with electron and hole conduction dominating the current, respectively. The ambipolar nature of the charge carrier transport may create problems for conventional applications based on graphene transistors. At the same time, however, it opens up opportunities for increased functionality in nontraditional circuit architectures. For example, graphene transistors have been utilized to demonstrate a frequency multiplier [5, 9, 10], a functional logic gate [11], and an inverter [12]. We demonstrate a single-transistor amplifier with three modes of operation utilizing the ambipolarity of a three-terminal graphene transistor. Depending on whether the graphene transistor is biased at the left branch, the

minimum conduction point, or the right branch of the ambipolar curve, the amplifier will be configured in the common-drain, the frequency multiplier, or the common-source mode of operation. The proposed triple-mode amplifier is demonstrated using a three-terminal back-gated graphene transistor. We also show theoretically and experimentally that our graphene amplifier can greatly simplify communications applications such as phase shift keying (PSK) and frequency shift keying (FSK). Compared to conventional designs for these applications, the proposed triple-mode graphene amplifier (i) has a significantly simpler structure, (ii) promises a larger bandwidth and higher frequency of operation, and (iii) promises low power consumption.

To demonstrate the triple-mode graphene amplifier, we have fabricated back-gated graphene transistors from exfoliated graphene flakes. A representative fabricated device, the scanning electron microscope (SEM) image, the Raman spectrum of the single-layer graphene, the I_{DS}-V_{GS} characteristics, and g_m-V_{GS} characteristics are shown in Fig.4.1(a)-(e). Fabrication and measurement details are provided in the Chapter 2 and Chapter 3. Strong ambipolar conduction was observed in the graphene transistors as evidenced by the "V"- shaped I_{DS}-V_{GS} curve. In the ambipolar graphene transistor, the transport is dominated by electrons and holes for high and low gate voltages, respectively, and the minimum conduction point V_{CNP} corresponds to the charge neutrality point where electrons and holes contribute equally to the transport. The ambipolar graphene transistor should be regarded as

n-type or p-type at high gate voltage ($V_{GS} > V_{CNP}$) or low gate voltage ($V_{GS} < V_{CNP}$), respectively, and as hybrid-type when the gate voltage is equal to V_{CNP}. The small-signal transconductance g_m is a key factor dominating the high-frequency performance of a transistor and the gain of the amplifier. As shown in Figure 1e, g_m is positive when $V_{GS} > V_{CNP}$ and negative when $V_{GS} < V_{CNP}$, reflecting electron current and hole current, respectively.

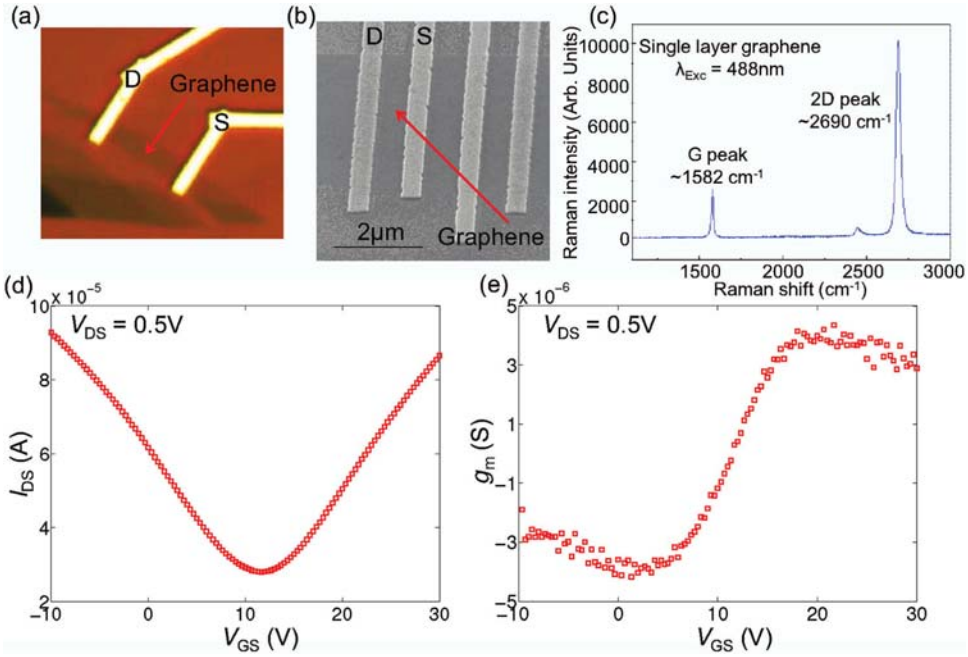

Fig. 4.1 (a) Optical micrograph image of a representative fabricated back-gated graphene transistor. (b) SEM image of source and drain electrodes of a representative back-gated graphene transistor. (c) The Raman spectrum of the singlelayer graphene. (d) I_{DS}-V_{GS} characteristics of the graphene transistor for V_{DS}=0.5 V. The current is minimum at the charge neutrality point. (e) g_m-V_{GS} characteristics for V_{DS} =0.5 V. The transconductance g_m is 0 at the charge neutrality point. Reprinted with permission from X. Yang, G. Liu, A. A. Balandin, and K. Mohanram, *ACS Nano*, **4**, 5532 (2010). Copyright (2010) American Chemical Society.

The small-signal model for the back-gated graphene transistor, also referred to as the hybrid-π model, under different V_{GS} is shown in Fig.4.2 panels a and b. Here, r_O is

the output resistance and g_m is the small signal transconductance of the graphene transistor. Since the graphene transistor is p-type when $V_{GS}<V_{CNP}$, the small-signal model is similar to that of a p-type MOSFET [13] in Fig.4.2 (a). Note that for a p-type MOSFET, the voltage-controlled current source is controlled by V_{GS}, yet in the graphene transistor, it is controlled by V_{GD}, because here we denote the terminal with higher voltage as the drain for consistency. Since the transistor is n-type when $V_{GS}>V_{CNP}$, the small-signal model is similar to that of an n-type MOSFET [13] in Fig.4.2 (b). For V_{GS} close to V_{CNP}, the graphene transistor should be considered as hybrid type instead of either n-type or p-type. Therefore, neither the n-type nor the p-type small-signal model is suitable to describe the performance of the graphene transistor. Finally, Fig.4.2 (c) illustrates the circuit for small-signal analysis of the triple-mode graphene amplifier, which will be described in details.

The triple-mode amplifier is built using a singe back-gate graphene transistors and an off-chip resistor. The schematic of the graphene amplifier is shown in Fig.4.3 (a). The supply voltage V_{DD} is set to 1 V, and the resistor R_{load} is 20 kΩ. V_{bias} is a fixed DC voltage and V_{ac} is a small sinusoidal AC signal. The gate-source voltage of the graphene transistor is hence equal to $V_{bias}+V_{ac}$. We show that depending on the relationship between V_{bias} and the charge neutrality point V_{CNP}, this amplifier can have three modes of operation. In each mode, the amplifier exhibits different performance in terms of the small-signal voltage gain $\Delta V_{out}/\Delta V_{in}$, which is given by the expression $\Delta(V_{DD}-I_{DS}R_{load})/\Delta V_{in}$.

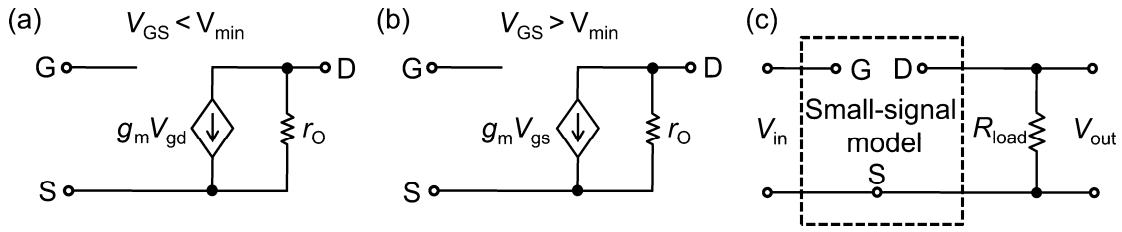

Fig. 4.2. (a,b) Small-signal model for the back-gated graphene transistor, also referred to as the hybrid-π model, under different V_{GS}. Here, g_m is the transconductance and r_O is the output resistance. The small-signal model in (a) is used when $V_{GS}<V_{CNP}$. Under this condition, the graphene transistor is p-type and the small-signal model is similar to that of a p-type MOSFET. As V_{GS} increases, the back-gated graphene transistor turns from p-type to n-type and the small-signal model in (b) is used when $V_{GS}>V_{CNP}$. Under this condition, the graphene transistor is n-type and the small-signal model is similar to that of an n-type MOSFET. Note that when V_{GS} is close to V_{CNP}, the graphene transistor should be considered as hybrid-type instead of either n-type or p-type. Therefore, neither the n-type nor the p-type small-signal model is suitable to describe the performance of the graphene transistor. (c) is the circuit for small-signal analysis of the triple-mode graphene amplifier from Fig.4.3 (a). Note that in small-signal circuit analysis, the power supply is shorted and the nodes for V_{DD} and ground are replaced by a single reference. Reprinted with permission from X. Yang, G. Liu, A. A. Balandin, and K. Mohanram, *ACS Nano*, **4**, 5532 (2010). Copyright (2010) American Chemical Society.

When $V_{bias} <V_{CNP}$, mode 1, the transistor is biased at the left branch of the ambipolar conduction curve, so the small-signal transconductance g_m of the transistor is negative. In the positive phase of V_{ac}, I_{DS} decreases as V_{GS} increases. As a result, the voltage drop across the resistor decreases and V_{out} increases. It can be similarly inferred that in the negative phase of V_{ac}, V_{out} will decrease. Therefore, the small-signal voltage gain in mode 1 is positive, and the input and the output signals have the same phase. From the transport perspective, when $V_{bias} <V_{CNP}$, the current is mainly due to hole conduction, so the transistor can be regarded as p-type. Under this condition, the circuit is configured as a common-drain amplifier. Analytically, the

gain of the amplifier in this mode is given by the expression $|g_m|R_{total}/(|g_m|R_{total}+1)$, where R_{total} is the parallel combination of the load resistor R_{load} and the inherent output resistance r_O of the graphene transistor. This expression can be derived from the small-signal analysis of the complete circuit illustrated in Fig.4.2 (c), using the small-signal model for the graphene transistor shown in Fig.4.2 (a). The measured result for mode 1 is presented in Fig.4.3 (c). The applied bias voltage V_{bias} is 6.5 V and the frequency of the input AC signal V_{ac} is 10 kHz.

When $V_{bias} > V_{CNP}$, mode 2, the transistor is biased at the right branch of the ambipolar conduction curve, so the small-signal transconductance g_m of the transistor is positive. In the positive phase of V_{ac}, I_{DS} increases as V_{GS} increases. As a result, the voltage drop across the resistor increases and V_{out} decreases. It can be similarly inferred that in the negative phase of V_{ac}, V_{out} will increase. Therefore, the small-signal voltage gain in mode 2 is negative, and the output signal will exhibit a phase shift of 180° with respect to the input signal. From the transport perspective, when $V_{bias} > V_{CNP}$, the current is mainly due to electron conduction, so the transistor can be regarded as n-type. Under this condition, the circuit is configured as a common-source amplifier. Analytically, the gain of the amplifier in this mode is given by the expression $-|g_m|R_{total}$, where R_{total} is the parallel combination of R_{load} and r_O. As in mode 1, this expression can be derived from the small-signal analysis of the complete circuit illustrated in Fig.4.2 (c), using the small-signal model for the graphene transistor shown in Fig.4.2 (b). The measured result for mode 2 is presented

in Figure in Fig.4.3 (e). The applied bias voltage V_{bias} is 17.5 V and the frequency of the input AC signal Vac is 10 kHz.

When V_{bias} =V_{CNP}, mode 3, the transistor is biased at the minimum conduction point. In the positive phase of V_{ac}, the small-signal transconductance is positive. As a result, the small-signal voltage gain is negative, as analyzed in mode 2. In contrast, in the negative phase of V_{ac}, the small-signal transconductance is negative. As a result, the small-signal voltage gain of the amplifier is positive, as analyzed in mode 1. Thus, when V_{bias} is equal to V_{CNP}, the input signal sees a positive gain in its positive phase and a negative gain in its negative phase, resulting in frequency doubling. The measured result for mode 3 is presented in Fig.4.3 (d). The applied bias voltage V_{bias} is 11.1 V and the frequency of the input AC signal V_{ac} is 4kHz. The spectral purity of the obtained output was analyzed using the fast Fourier transform. Frequency doubling effect is clearly observed since it is observed that 83% of energy of the output signal is at the frequency of 8 kHz. This effect has also been previously reported [5].

The proposed single-transistor graphene amplifier utilizes the key concept of biasing in analog circuits, that is, only a small range of I-V characteristics near the bias point are necessary to optimize the circuit performance. For this reason, ambipolar conduction can provide a larger design-space than unipolar conduction because of the richer diversity of I-V characteristics.

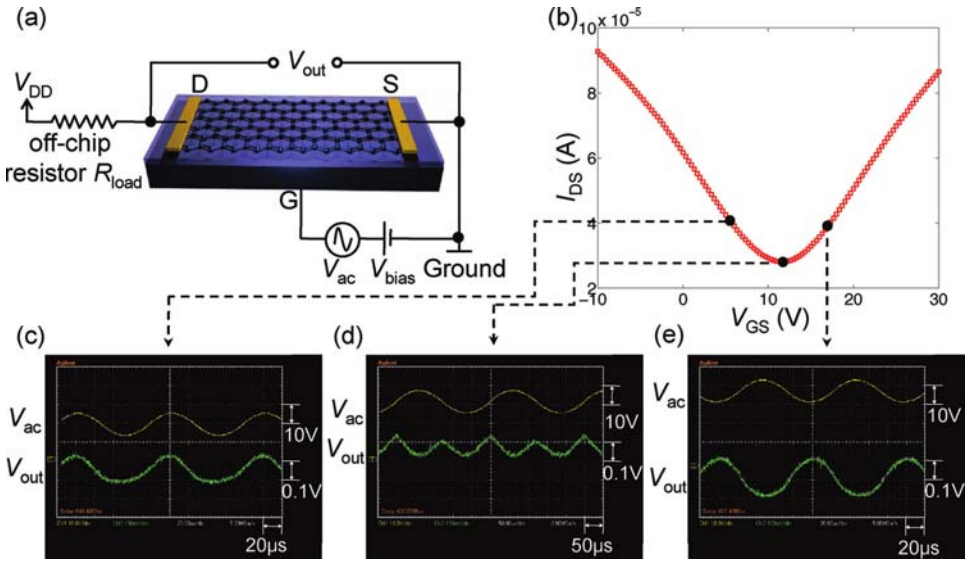

Fig. 4.3. (a) The schematic for the triple-mode single-transistor graphene amplifier based on an off-chip resistor R_{load}. (b) The I_{DS}-V_{GS} characteristics of the graphene transistor. The three dots represent three representative bias voltages for the three different modes of operation. From the left to the right, for the three bias voltages, the amplifier is configured in the common-drain mode, the frequency multiplication mode, and the common-source mode, respectively. (c) The AC coupled input (yellow waveform) and output (green waveform) signals when the amplifier is biased at the left branch of the ambipolar curve. In this configuration, the amplifier is in the common-drain mode, and the output signal has the same frequency and phase as the input signal. (d) The AC coupled input and output signals when the amplifier is biased at the CNP. In this configuration, the amplifier is in the frequency multiplication mode, and the frequency of the output signal is doubled as compared to that of the input signal. (e) The AC coupled input and output signals when the amplifier is biased at the right branch of the ambipolar curve. In this configuration, the amplifier is in the common-source mode, and the output signal has the same frequency but a 180° phase shift as compared to the input signal. Reprinted with permission from X. Yang, G. Liu, A. A. Balandin, and K. Mohanram, *ACS Nano*, **4**, 5532 (2010). Copyright (2010) American Chemical Society.

Compared to the traditional amplifiers based on unipolar devices, the proposed single-transistor amplifier provides greater in-field controllability as it can switch between the three modes during operation. To the best of our knowledge, this is the first work to demonstrate that a single-transistor amplifier based on a three-terminal

device can be in-field configured to function as both a common-source and a common drain amplifier. The small-signal gain observed in the three modes of operation is 0.01, which is mainly due to the very thick back-gate oxide of 300 nm SiO_2. As we adopt the top-gate structure, where the top-gate oxide is ~23nm of high k Al_2O_3, the gain is improved by a factor of 10, as shown in Fig. 4.4.

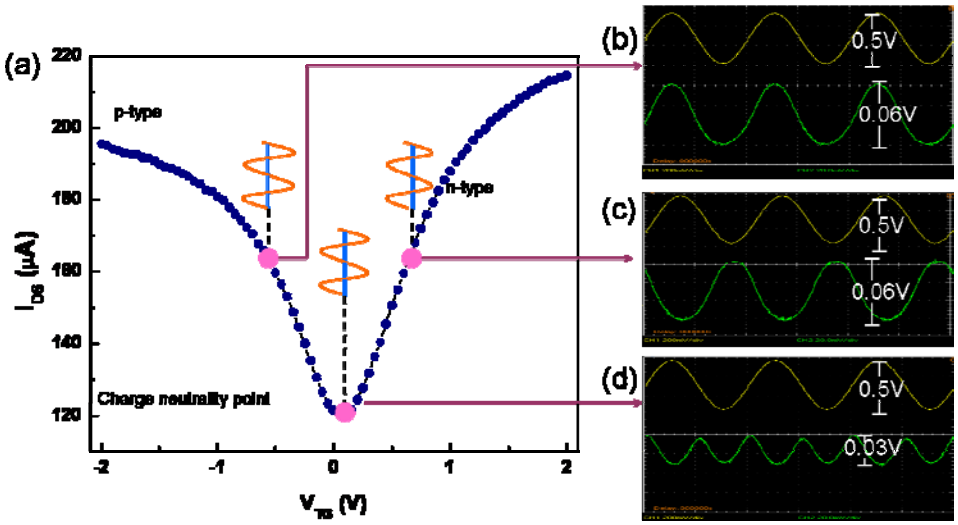

Fig. 4.4. The three-mode amplifier build on top-gate graphene device. (a) The I_{DS}-V_{GS} characteristics of the top-gate graphene transistor. Three points on p-type, n-type and CNP represent the bias points for the common-drain mode, common-source mode and frequency multiplication mode. (b) The AC coupled input (yellow waveform) and output (green waveform) of common-drain mode. The output keeps the phase with input. (c) The AC coupled input and output of common-source. The output reverses the phase with input (180° phase shift). (d) The AC coupled input and output signals when the amplifier is biased at the CNP, the frequency multiplication mode. Note that the gain here is ~0.1, which is one order of magnitude larger than in back-gate transistor senario. The frequency here is 100 KHz.

The input and output of the three operations modes are shown in Fig. 4.4 (b), (c) and (d). The top-gate capacitance here is $c_{TG}=3.6\times10^{-3}$ F/m^2, which is ~30 times larger than back-gate device. However, the mobility reduced by ~3 times since the gate oxide introduced more scattering. Hence, the overall increment of gain is about 10.

Further enhancement of gain can be achieved by continue thinning down the oxide thickness and replacing with higher k material such HfO_2. The amplifier with gain larger than 1 has been demonstrated with such gate oxide enineering attempts [6].

Combining any two of the three modes mentioned above, we can achieve the modulation functions of PSK and FSK which are widely used in wireless communications such as Bluetooth, radio frequency identifications (RFID) and audio and radio systems [14].

We first consider the application of PSK. For brevity, we consider binary PSK (BPSK) that is the most basic variant of PSK in this article, but the idea can be extended to other forms of PSK such as quadrature PSK (QPSK). In BPSK, the phase of the small AC carrier signal is modulated and shifted between 0° and 180° to represent the data stream, which takes the binary value of (0,1). By using the triple-mode amplifier, BPSK modulation can be achieved by applying the sinusoid carrier as the small AC signal V_{ac} and the data stream, which is the large square wave signal, as the bias V_{bias}. If the swing of the square wave signal V_{bias} is chosen such that the amplifier can be switched between the positive-gain and negative-gain modes, the carrier signal will either experience no phase shift or a phase shift of 180°. The experimental results for BPSK modulation is presented in Fig. 4.5. The biasing voltage V_{bias} is switched between -0.33 and 0.33 V, representing digital data “0” and “1”, respectively. It is generated as a square wave signal from the signal generator. When V_{bias} is -0.33 V, the graphene transistor is biased at the left branch, so the

amplifier operates in mode 1 with a positive gain. When V_{bias} is 0.33 V, the graphene transistor is biased at the right branch, so the amplifier operates in mode 2 with a negative gain. The frequency of V_{ac} is 0.5 MHz. Note that the output signal has slightly different DC voltages when the amplifier is configured in mode 1 and mode 2, which may not be preferred during demodulation. However, the DC voltage can be easily filtered out using a high-pass filter.

We next consider binary FSK (BFSK) that is the most basic variant of FSK for illustration. In BFSK, the frequency of the small AC carrier signal is modulated and shifted between f_{c1} and f_{c2} to represent the data stream, which takes the binary value of (0,1). If $f_{c2}=2f_{c1}$, such as in the case of Kansas City standard (KCS) for audio cassette drives where f_{c1}=1200 Hz and f_{c2}=2400 Hz, BFSK modulation can be successfully achieved using the proposed triple-mode amplifier. Again, as in the case of BPSK, we can apply the sinusoid carrier as a small AC signal and the data stream, which is the large square wave signal, as the bias. If the square wave signal V_{bias} is chosen such that the amplifier is biased in mode 3/ mode 2 or mode 3/mode 1, the frequency of the output signal will either be doubled or remain the same, realizing BFSK. The experimental results for BFSK modulation is presented in Fig. 4.6 . The biasing voltage V_{bias}, generated as a square wave signal from the signal generator is switched between -0.65 V and 0 V, representing digital data “0” and “1”, respectively. When V_{bias} is 0 V, the graphene transistor is biased at the CNP, so the amplifier operates in mode 3. When V_{bias} is -0.65 V, the graphene transistor is biased at the left

branch, so the amplifier operates in mode 1 with a positive gain. The problem of mismatched DC voltage at the output can be similarly solved by using a high-pass filter.

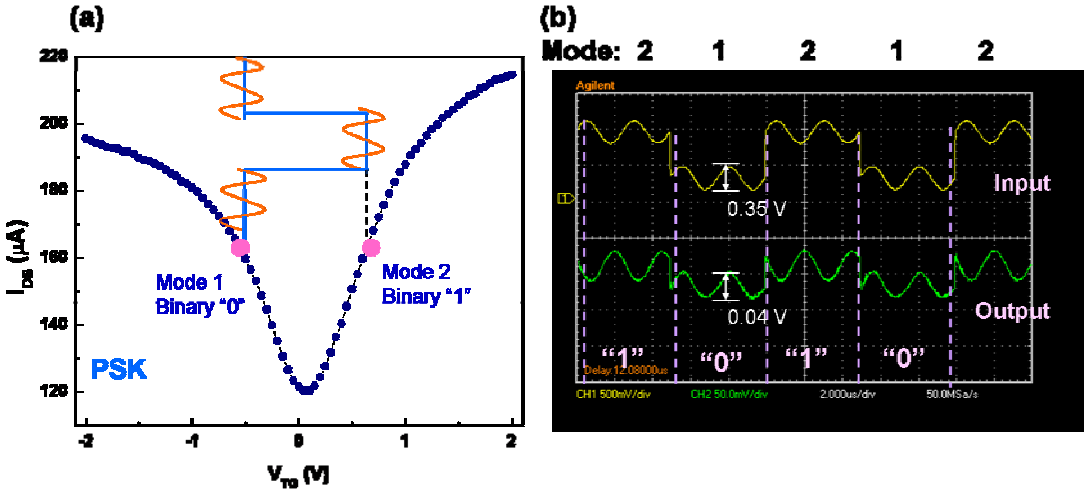

Fig. 4.5. Two bias voltages, -0.33 and 0.33 V, represent "0" and "1". (b) Experimental results for BPSK modulation. Note that when the bias voltage is -0.33 V (0.33V), the amplifier is configured in mode 1 (mode 2) and the output signal has the same phase (phase shift of 180°) as the input signal. The frequency here is 0.5 MHz.

For comparison, traditional PSK and FSK modulation is usually achieved using analog multipliers that require multiple transistors and/or filtering devices. However, by leveraging the ambipolar conduction, the proposed amplifier provides a single transistor design to achieve PSK and FSK modulation. It greatly simplifies the circuit design and the simple structure will potentially also lower power consumption. Note that the concept described in this article also applies to other materials exhibiting ambipolar conduction properties, such as silicon nanowires [15], organic semiconductor heterostructures [16], and carbon nanotubes (CNTs) [17]. Among these materials, both CNTs and graphene have high mobility that is preferable for high

frequency analog applications. However, the two-dimensional planar structure of graphene enables the current to be easily increased by increasing the width of the graphene channel, which is advantageous over CNT transistors.

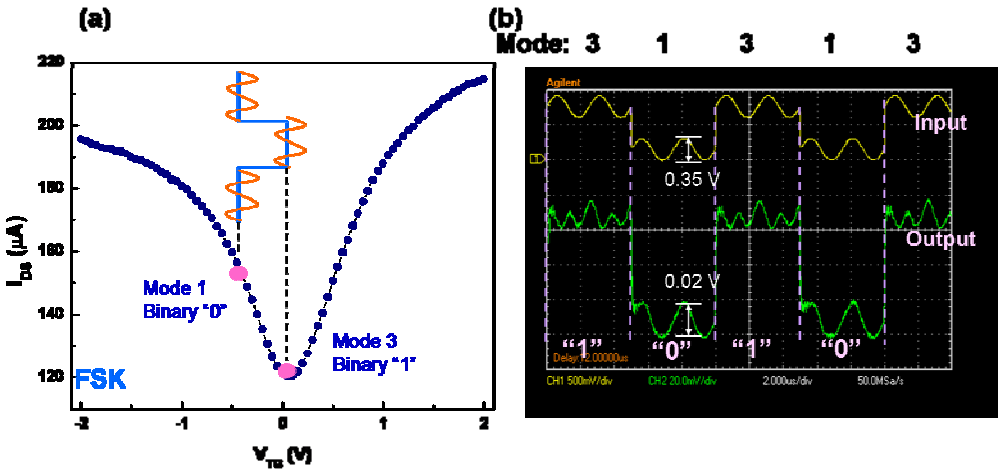

Fig.4.6. Two bias voltages, -0.65 and 0 V, represent "0" and "1". (b) Experimental results for BFSK modulation. Note that when the bias voltage is -0.65 V (0 V), the amplifier is configured in mode 1 (mode 3) and the output signal has the same frequency (double frequency) as the input signal. The frequency here is 0.5 MHz.

Given the excellent advantages of the triple-mode amplifier, there are several directions that merit further investigation to optimize its performance. Currently, the gain of the amplifier is low and of the order of 0.1 in top-gate graphene device. This is because (i) the graphene transistor exhibits low small-signal transconductance g_m and (ii) the transistor operates in the linear region, with a small inherent output resistance r_O. We believe that this problem can be solved by improving the device structure and channel quality, increasing the g_m, and pushing the transistor into the saturation region, as shown in Chapter 3. Indeed, a frequency multiplier (mode 3 application of the triple-mode amplifier) with a small-signal gain of 0.15 has been recently reported

using the relatively mature CNT [10].

4.3. Phase Detecor

The ambipolar transport of graphene can also contribute to the de-modulation end of the communication system. We demonstrated that simple graphene transistor circuit can realize the function of multiplier phase detector. The multiplier phase detector is a significant component of the phase-locked loop, which is one of the most important building blocks in modern analog, digital, and communication circuits [18]. A multiplier phase detector takes two input signals, for example u_1 and u_2, and produces an output voltage that is proportional to the phase difference between u_1 and u_2. Usually, u_1 and u_2 are a sinusoidal signal and a square-wave signal, respectively [18]. Without loss of generality, we assume that

$$u_1(t) = U_{10} \sin(\omega_1 t + \theta_1) \text{ and } u_2(t) = U_{20} \text{ rect}(\omega_2 t + \theta_2) \quad (1)$$

where rect represents rectangular, and U_{10} and U_{20}, ω_1 and ω_2, and θ_1 and θ_2 are the amplitudes, radian frequencies, and phases of u_1 and u_2, respectively. u_1 and u_2 are multiplied by the phase detector, and the high-frequency component of the result u_{out} is filtered out through a low-pass filter, leaving only the DC component u_d. If $\omega_1 = \omega_2$, u_d is given by

$$u_d(t) = U_{10}U_{20} \times 2/\pi \times (\sin(\theta_1 - \theta_2)) \approx K_d\theta_e \quad (2)$$

where K_d denotes the detector gain, and θ_e is the phase difference between the two input signals in radians. Traditionally, u_1 and u_2 are multiplied by an analog multiplier

built using multiple unipolar transistors. For example, a typical Gilbert cell analog multiplier [19] consists of six transistors and two resistors. However, taking the advantage of the ambipolarity of the graphene transistor, the proposed simplified circuit structure requires only a single top-gated graphene transistor and one resistor. The schematic of the graphene multiplier phase detector and an illustrative I_{DS}–V_{GS} curve of an ambipolar graphene transistor are presented in Fig. 4.7.

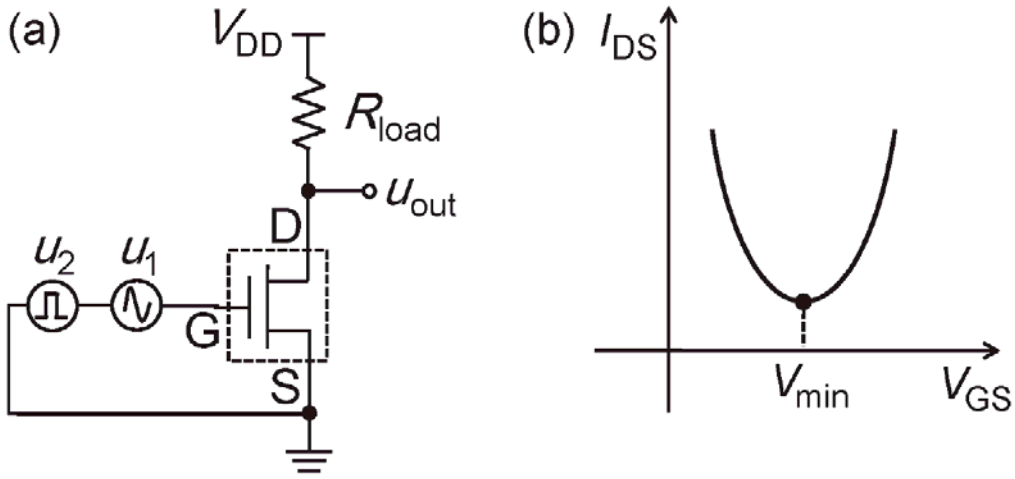

Fig. 4.7. (a) Schematic of the proposed graphene multiplier phase detector based on a single top-gated graphene transistor and an off-chip resistor R_{load}. u_{out} is the output of the phase detector. (b) Illustration of the typical ambipolar I_{DS}–V_{GS} curve. V_{min} is the voltage, where I_{DS} is the minimum. Reprinted with permission from X. Yang, G. Liu, M. Rostami, A. A. Balandin, and K. Mohanram, IEEE Electron Device Lett., 32, 1328 (2011).Copyright (2011) IEEE.

In this proposed implementation of the multiplier phase detector, sinusoidal signal u_1 has small amplitude. Square-wave signal u_2 serves as the bias voltage, and it is chosen so that the lower and higher levels of u_2, denoted as V_{low} and V_{high}, satisfy $V_{low} < V_{CNP}$ and $V_{high} > V_{CNP}$, respectively. Here, V_{CNP} is the minimum conduction

point of the ambipolar graphene transistor. When $u_2 = V_{low}$ (V_{high}), I_{DS} of the graphene transistor decreases (increases) as the gate voltage increases, and the voltage drop across the resistor decreases (increases), thereby increasing (decreasing) u_{out}. Therefore, the voltage gain of the circuit $\partial u_{out}/\partial u_1$ is positive (negative). As a result, the gain of the circuit G is also a square wave that switches between positive and negative values. Since $u_{out} = Gu_1$, the product of u_1 and u_2 has been transformed into the product of u_1 and G, which is inherently produced by the proposed circuit.

To demonstrate the proposed graphene multiplier phase detector in Fig. 4.7 (a), R_{load} is set to 20 kΩ, V_{DD} to 1.8 V, and the frequency of both u_1 and u_2 to 100 kHz. In Fig. 4.8, we present the output u_{out} of the circuit at different phase differences θ_e between u_1 and u_2. Since I_{DS} of the graphene transistor is not identical at V_{low} and V_{high}, there will be a "stair" in the output u_d between the two halves in a cycle. However, this "stair" is caused only by u_2 and is not related to the phase difference between u_1 and u_2. Therefore, it will not affect the performance of the phase detector, which is the difference in the DC component u_d of u_{out} at different phase differences θ_e. In Fig. 4.8, it can be observed that at $\theta_e=(\pi/2)$ rad, the circuit is biased in the negative gain condition for the positive half of u_1 and in the positive gain condition for the negative half of u_1. Hence, output u_{out} has the smallest DC component at $\theta_e=(\pi/2)$ rad. In contrast, at $\theta_e= -(\pi/2)$ rad, the circuit is biased in the positive gain condition for the positive half of u_1 and in the negative gain condition for the negative half of u_1. Hence, output uout has the largest DC component at $\theta_e= -(\pi/2)$ rad. The circuit voltage gain

$\partial u_{out}/\partial u_1$ is$\approx$0.1. In Fig. 4.9, we have shown the DC component u_d at different θ_e. As the phase difference goes from $\pi/2$ to $-(\pi/2)$ rad, u_d increases monotonically from 298 to 319 mV, which corresponds to a detector gain $K_d\approx-7$ mV/rad.

The improvement of the gain is desirable for phase detector. The current result is limited by the gate capacitance and the saturation condition of graphene device. The gate capacitance can be increase by 10 times as mentioned in previous section. The saturation condition can be reached by applying high V_{DS} as shown in Chapter 3. Of course, there are some other limitations such as the contact resistance of metal to graphene, which is on the order of 1kΩ-μm with current Ti/graphene interface. Substantial improvement is needed to reduce the contact resistance which will benefit the transconductance of the transistor and the voltage gain of graphene amplifier.

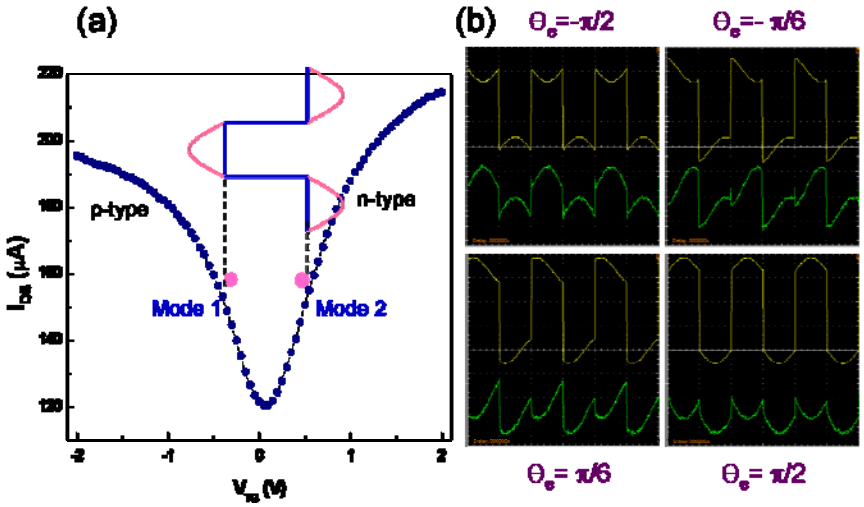

Fig. 4.8. (a) The I_{DS}-V_{GS} of the top-gate graphene deviec. The bias points for the phase detector is at mode 1 and mode 2. (b) Output u_{out} versus $u_{in} = u_1 + u_2$ for, θ_e= -(π/2), θ_e= -(π/6), θ_e=(π/6), and θ_e=(π/2). Reprinted with permission from X. Yang, G. Liu, M. Rostami, A. A. Balandin, and K. Mohanram, IEEE Electron Device Lett., 32, 1328 (2011).Copyright (2011) IEEE.

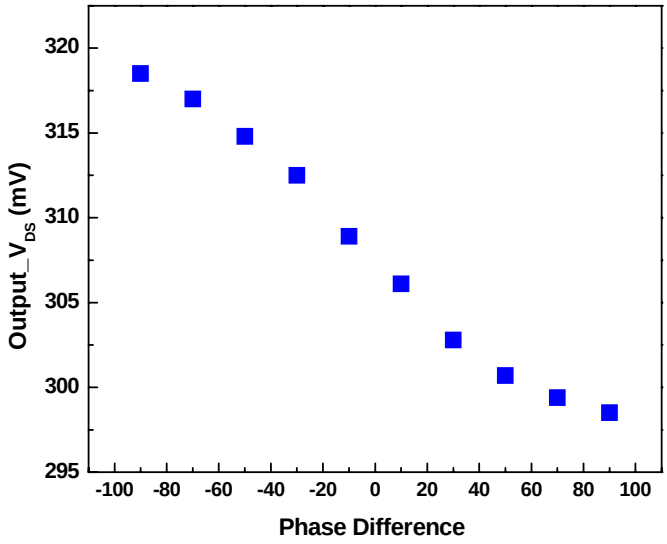

Fig. 4.9. DC component uout at different θ_e (in degree) between u_1 and u_2. The detector gain is $K_d \approx -7$ mV/rad. Reprinted with permission from X. Yang, G. Liu, M. Rostami, A. A. Balandin, and K. Mohanram, IEEE Electron Device Lett., 32, 1328 (2011).Copyright (2011) IEEE.

4.4. Summary

The ambipolar transport property of graphene together with its high carrier mobility allows for the possibility of using graphene transistors in analog communications applications. We experimentally demonstrated by using only one single graphene transistor and one load resistor, the circuit can be functioned as PSK, FSK and phase detector which is widely used for analog communication systems. Note that the voltage gain of the current graphene circuits is still below unit, which in principle is not limited by graphene itself but by optimization device design as well as current technologies that available at UCR cleanroom.

References

[1] A.K. Geim and K.S. Novoselov, *Nature Materials*, **6**, 183 (2007).

[2] Y.-M. Lin, C. Dimitrakopoulos, K.A. Jenkins, D.B. Farmer, H.-Y. Chiu, A. Grill and P. Avouris, *Science*, **327**, 662 (2010).

[3] L. Liao, Y.-C. Lin, M. Bao, R. Cheng, J. Bai, Y. Liu, Y. Qu, K.L. Wang, Y. Huang and X. Duan, *Nature*, **467**, 305 (2010).

[4] Y. Wu, Y.-M. Lin, A.A. Bol, K.A. Jenkins, F. Xia, D.B. Farmer, Y. Zhu and P. Avouris, *Nature*, **472**, 74 (2011).

[5] H. Wang, D. Nezich, J. Kong and T. Palacios, *IEEE Electron Device Lett.,* **30**, 547 (2009).

[6] S.J. Han, K.A. Jenkins, A. Valdes-Garcia, A.D. Franklin, A.A. Bol and W. Haensch, *Nano Lett*., **11**, 3690 (2011).

[7] X. Yang, G. Liu, A.A. Balandin and K. Mohanram, *ACS Nano*, **4**, 5532 (2010)

[8] X. Yang, G. Liu, M. Rostami, A.A. Balandin and K. Mohanram, *IEEE Electron Device Lett.,* **32**, 1328 (2011).

[9] Z. Wang, Z. Zhang, H. Xu, L. Ding, S. Wang and L.-M. Peng, *Appl. Phys. Lett.*, **96**, 73104 (2010).

[10] Z. Wang, L. Ding, T. Pei, Z. Zhang, S. Wang, T. Yu, X. Ye, F. Peng, Y. Li and L.M. Peng, *Nano Lett.*,10, 3648 (2010).

[11] R. Sordan, F. Traversi and V. Russo, *Appl. Phys. Lett.*, **94**, 073305 (2009).

[12] N. Harada, K. Yagi, S. Sato, N. Yokoyama, *Appl. Phys. Lett.*, **96**, 012102 (2010).

[13] A.S. Sedra and K.C. Smith, In Microelectronic Circuits, Oxford University Press: Oxford, 2004, 290-291.

[14] F. Xiong, In Digital Modulation Techniques; Artech House Publishers: Boston, MA, 2006, 99-205.

[15] S.-M. Koo, Q. Li, M.D. Edelstein, C.A. Richter and E.M.Vogel, *Nano Lett.*, **5**, 2519 (2005).

[16] A. Dodabalapur, H.E. Katz, L. Torsi and R.C. Haddon, *Science*, **269**, 1560 (1995).

[17] S. Heinze, M. Radosavljevic, J. Tersoff and P. Avouris. *Phys. Rev. B*, **68**, 235418 (2003).

[18] J. A. Crawford, Advanced Phase-Lock Techniques. Norwood, MA: Artech House, 2008.

[19] P.R. Gray, P.J. Hurst, S.H. Lewis and R.G. Meyer, Analysis and Design of Analog Integrated Circuits. Hoboken, NJ: Wiley, 2001.

Chapter 5

Low-Frequency Noise in Graphene

5.1 Introduction of Low-Frequency Noise

The noise in electronic device is a random, spontaneous perturbation that inherent to the physics of the device. Noise in an electronic system could originate from external source and internal source. The external noise can be eliminated or reduced by proper shielding, filtering and layout design of the circuits. However, the internal source, cannot be eliminated, but is possible to reduce by modification of the devices structure and design. This chapter deals with the internal noise, which is originated from the physics point of view of the devices.

The noise of the device is essentially the fluctuation of the resistance of the device, so that if a constant voltage is applied to the device, the current passing through will be fluctuating. Since this fluctuation is a time varied signal, to be more accurately, a random process, it is more convenient to express the noise in frequency dominant. Hence, the mathematic analysis of noise is done by studying its power spectrum density as a function of frequency *f*, for example current referenced noise spectrum density S_I, with unit of I^2/Hz. Usually the noise is not a function of current I, so the normalized unit S_I/I^2 (Hz^{-1}) is more often used as the characteristics of the noise. Similarly, if we consider a constant current flow through the device, the voltage drop across the device will be fluctuating. The power spectrum density will be expressed as

voltage referenced noise spectrum density S_V, with unit of V^2/Hz. The normalized the voltage noise is S_V/V^2 with unit of Hz^{-1}. Note that in reality the normalized current spectrum density is equal to the normalized voltage spectrum density $S_I/I^2 = S_V/V^2$. Also, noise is often expressed with resistance as subscript, S_R, and $S_R/R^2 = S_I/I^2 = S_V/V^2$ [1].

In modern semiconductor devices, there are several type of noises which is due to different physics mechanisms. The most common one is thermal noise, where the noise is independent on the frequency, and only depend on temperature and resistance $S_V=4kTR$ or $S_I=4kT/R$, where k is Boltzmann constant, T is temperature in Kelvin, and R is resistance. This noise is discovered by J. B. Johnson and explained by H. Nyquist [2, 3]. Shot noise, occurs when the current flow across a potential barrier, such as ph-junction, is expressed as $S_I=2qI$, where q is the elementary charge, I is the current. Generation-recombination noise is a noise in semiconductor which originates from the traps that randomly capture and emit carriers. 1/*f* noise, also called flicker noise, is the noise with spectrum density inversely proportional to frequency f^{γ}, where γ is often close to 1. This 1/*f* noise exists in many materials such as metal and semiconductors, and it is a low-frequency noise that happens below 100 kHz. A large number traps with generation-recombination noise can produce 1/*f* noise. Despite been studied for more than half-a-century, the physical mechanism of the origin 1/f noise is still under debate. The two major schools are carrier number fluctuation

(McWhorter model) and mobility fluctuation (Hooge model), and each of them has experimental results to support their theories.

Graphene is a promising material for high-frequency analog applications due to its excellent physical properties [4,5], such as huge electron mobility of graphene up to 22,000 cm2/Vs [6], large charge carrier saturation velocity of 4.5×10^7 cm/s [7, 8], and outstanding thermal conductivity of above 3000 W/mK [9, 10], exceeding that of diamond. Important components of the analog systems such as phase detectors have already been implemented with the triple-mode graphene transistors [11, 12]. In RF and analog applications, the reduction of the low-frequency noise is important because this type of noise will be up-converted due to the nonlinearity of the system and contribute to the phase noise of the systems [1]. The low-frequency noise in graphene field-effect transistors (FETs) has the drain-current noise spectral density $S_I \sim 1/f$ for the frequency f below 100 kHz [11–18]. Some graphene devices also exhibit the generation-recombination (GR) noise bulges with the time constants $\tau=1/(2\pi f_0)$ of ~0.3–1.1s (f_0 is the corner frequency) [13].

5.2 Noise Measurement Setup

The noise is actually a very small AC signal, especially in good conductors. It is well know that graphene itself is a good conductor, and the Ti/Au electrodes in contact with graphene forms an Ohmic contact. The noise measurement has to be set

up very carefully to eliminate the external and environmental noise so that the physical noise from the device itself can be measured.

The schematic of the noise measurement system is shown as in Fig. 5.1. DC voltage is applied on the source/drain electrodes and gate electrodes of graphene transistor. The voltage drop across the source/drain is magnified by the low-noise amplifier (Stanford Research 560). The amplified voltage fluctuation signal is processed with the dynamic signal analyzer (Stanford Research 780) by converting from time domain to frequency domain using Fourier Transform. The voltage sources V_{DD} and V_{GG} used here for noise measurement are quiet batteries rather than the conventional voltage supply. The reason is that the voltage supply that powered by electrical main is operating at 60 Hz, so the output voltage is inevitably affect by the 60 Hz, although very small, but big enough to influence the noise measurement. Hence we use potential meters R_{PD} and R_{PG} to split the voltages from the batteries. The potential meters used here are multi-loop wirewound type, so that we can split the voltage with high precision and also low noise. The load resistor R_D and gate protection resistor R_G used here are all metallic resistor with very low noise (only has thermal noise). A probe station is used to connect the graphene device with the biasing circuits and amplifier. The whole measurement circuits, amplifier and probe stations are enclosed by a big metal shielding box to protect from environment electro-magnetic waves. The inner walls of the shielding box are coated with sound proof foam to reduce the sound noise coming into the measurement systems.

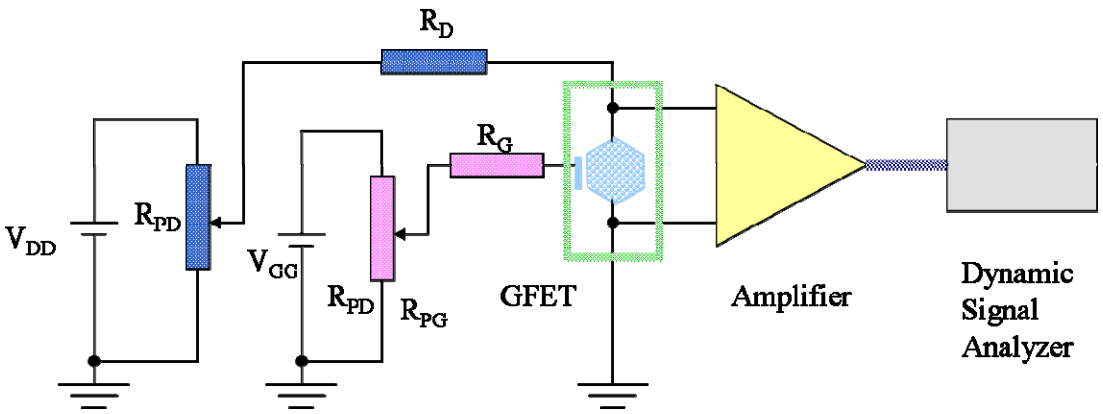

Fig. 5.1. Schematic of the graphene device noise measurement of Graphene FET (GFET) is biased with quiet battery and potential meter circuit. The voltage noise across the graphene is amplified by the low-noise amplifier and then process with dynamic signal analyzer.

Fig. 5.2. Noise measurement setup inside the shielding box. The quiet batteries and potential meter biasing circuits, probe station and low-noise amplifier are all inside the shielding box. Note here the inner walls of the shielding box are coated with sound proof foam.

As we measured the voltage noise spectrum S_V by the dynamic signal analyzer, we convert it to current noise spectrum S_I by $S_I=S_V\times((R_D+R_{Graphene})/ R_D\times R_{Graphene})^2$, where R_D is the load resistance and $R_{Graphene}$ is the resistance from graphene device.

5.3 Low-Frequency Noise in Back-Gate Graphene Devices

The low-frequency noise was measured in a frequency range from 1 Hz to 50 kHz at room tempearture. The graphene transistors were biased in a common source mode at source-drain bias V_{DS} = 50 mV. The voltage-referred electrical current fluctuations S_V from the load resistor R_L connected in series with the drain were analyzed by a SR780 FFT dynamic signal analyzer. Fig. 5.3 shows an example of the noise spectra measured at different gate-bias voltages for one of the graphene transistors. For all examined devices the noise spectra were close to the $1/f^{\gamma}$ with γ=1.0-1.1 depending on the gate voltage and a specific device. When the current was changed by the drain voltage the noise spectral density of the short circuit current fluctuations, S_I, was always proportional to the square of the drain current, i.e $S_I \sim I_D^2$. In this sense, the measured spectra were similar to the low-frequency noise in devices made from other materials [14].

The analysis of this gate voltage dependence of noise spectral density yields valuable information about the noise sources and mechanisms because the gate voltage changes carrier concentration and Fermi level position. In conventional semiconductor FETs the low-frequency noise is usually analyzed in the framework of

the McWhorter model [15]. In this model, the low-frequency noise is caused by the tunneling of the carriers from the channel to the traps in the oxide. Therefore the trap concentration in the oxide is a natural figure-of-merit for the noise amplitude in MOSFETs. The McWhorter model predicts that the normalized noise spectral density, S_I/I_D^2, decreases in the strong inversion regime as $\sim 1/n_s^2$ (where n_s is the channel carriers concentration). Any deviation from this law might indicate the influence of the contacts, non-homogeneous trap distribution in energy or space, or contributions of the mobility fluctuations to the current noise [15-18].

Fig. 5.4 shows the gate voltage dependence of noise spectral density, S_I/I_D^2, for all studied devices. One can see dispersion in the data for the noise spectra density of the examined devices. This is due to the different devices channel size ranging from 1.5-80 μm^2, and also results from the difference between SLG and BLG.

As seen, some device shows noise S_I/I^2 decreases with an increase of the gate voltage, while others exhibits the opposites or no gate dependence. For the examined graphene FETs we found a whole variety of gate voltage dependences of the noise spectral density: the noise level either increased or decreased with deviation from the charge neutrality point (see also [19] for the gate voltage dependence of noise in graphene).

The noise spectral density of metals and semiconductors are inversely proportional to the device area [20]. This relation can also be extended to graphene devices if the noise contribution is mainly from the device channel. Fig. 5.5 shows the

results of area normalized noise spectral density of SLG and BLG devices. The different data points in same shape and color represent the noise level for the same device under different gate bias within $|V_{BG}-V_{CNP}|$=30V. It shows that in BLG cases, the noise inversely scales with area by A^{-1}, however, very week area dependence in SLG cases. This difference indicates that the noise source in BLG case is mainly from channel, and in SLG, the contact noise can not be ignored although the contact between graphene and Ti/Au is Ohmic. Also, it can be seen that the noise in BLG is smaller than in SLG, consistent with reported by other groups [19, 21]. The detail reasons will be discussed in section 5.5.

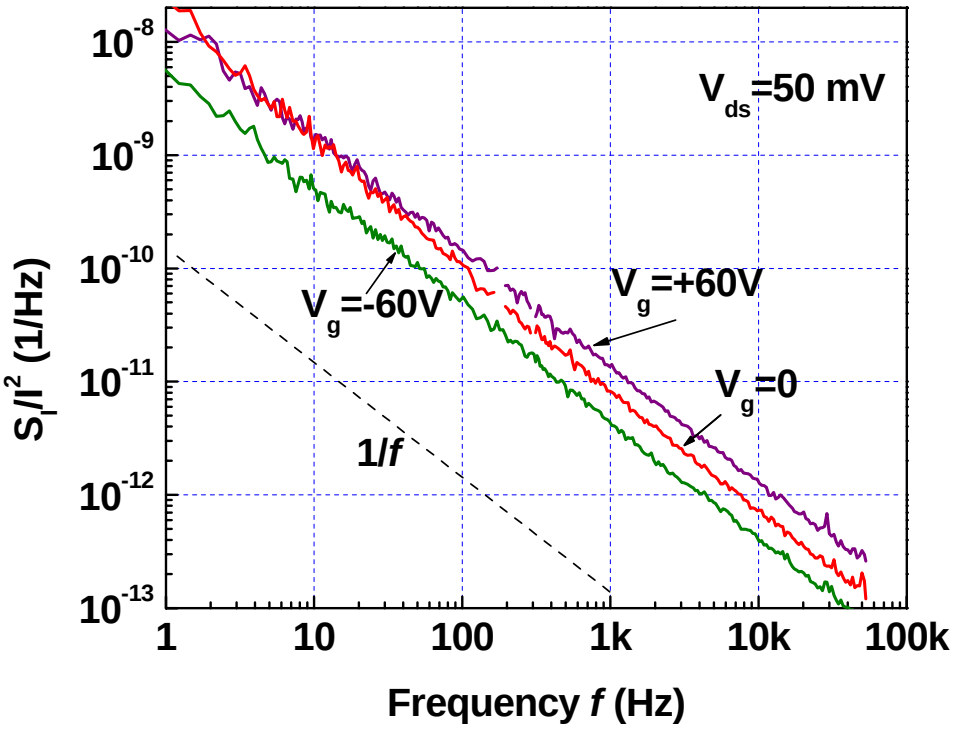

Fig. 5.3. Normalized spectrum density of graphene back-gate transistors under different gate bias. The V_{DS} used for noise measurement is 50 mV. The spectrum exhibit 1/*f* dependency in between 1 Hz to 50 kHz.

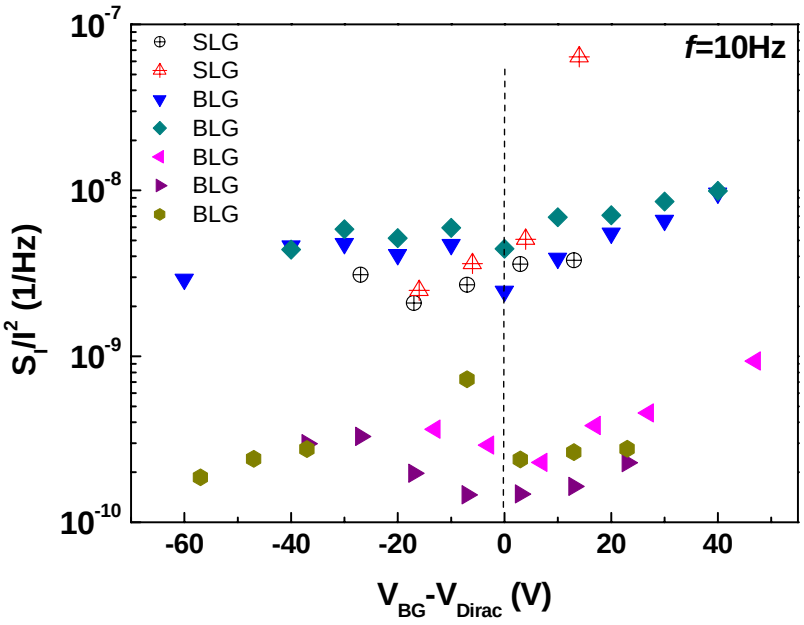

Fig. 5.4. Normalized noise spectral density S_I/I^2 for several devices as functions of the gate bias. The data are picked at 10Hz from the noise spectrum of each device. Note here both SLG and BLG are presented, and there is no collation between the noise dependence on the number of layers.

The Hooge parameter α is usually used as a figure-of-merit of the 1/f noise. Hooge formula is an empirical relation of the noise spectral density with the numbers of carrier N, $\frac{S_I}{I^2} = \frac{\alpha}{Nf}$. Although Hooge's theory supports the mobility fluctuation, the parameter α is to evaluate the magnitude of the noise for devices regardless what type of fluctuation they are. The Hooge parameter for graphene device is on the order of 10^{-3}-10^{-4}, which is pretty low. It is 1-2 orders better than that of carbon nanotube devices, and comparable to the silicon MOSFET. Considering graphene is a essentially a surface material, the entire channel is exposed to the environment, it should be very susceptible to the fluctuation from the outside. The reason is probably the high mobility of graphene.

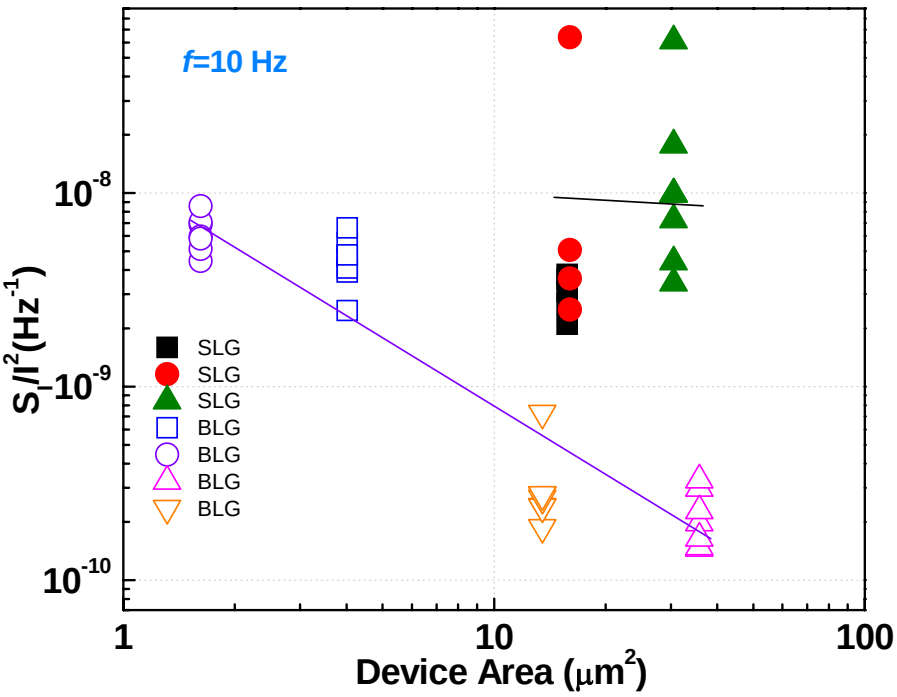

Fig. 5.5. The noise spectral density as a function of device area size. The different data points in same shape and color represent the noise level for the same device under different gate bias within $|V_{BG}-V_{CNP}|$=30V. It shows that in BLG cases, the noise inversely scales with area by A^{-1}, however, very week area dependence in SLG cases. This difference indicates that the noise source in BLG case is mainly from channel, and in SLG, the contact noise is substantial. Also, it can be seen that the noise in BLG is smaller than in SLG.

5.4 Low-Frequency Noise in Top-Gate Graphene Devices

The noise properties are also studied in the top-gate structure. Fig. 5.6(a) shows the noise spectral density of a top-gate BLG graphene device under different gate bias. As seen, the spectra are also of 1/f dependence. The inset shows the optical image of this top-gate device. Fig. 5.6(b) shows the gate dependence of noise together with the I_{DS}-V_{GS} characteristics. In this particular device, the maximum noise happens close to the CNP.

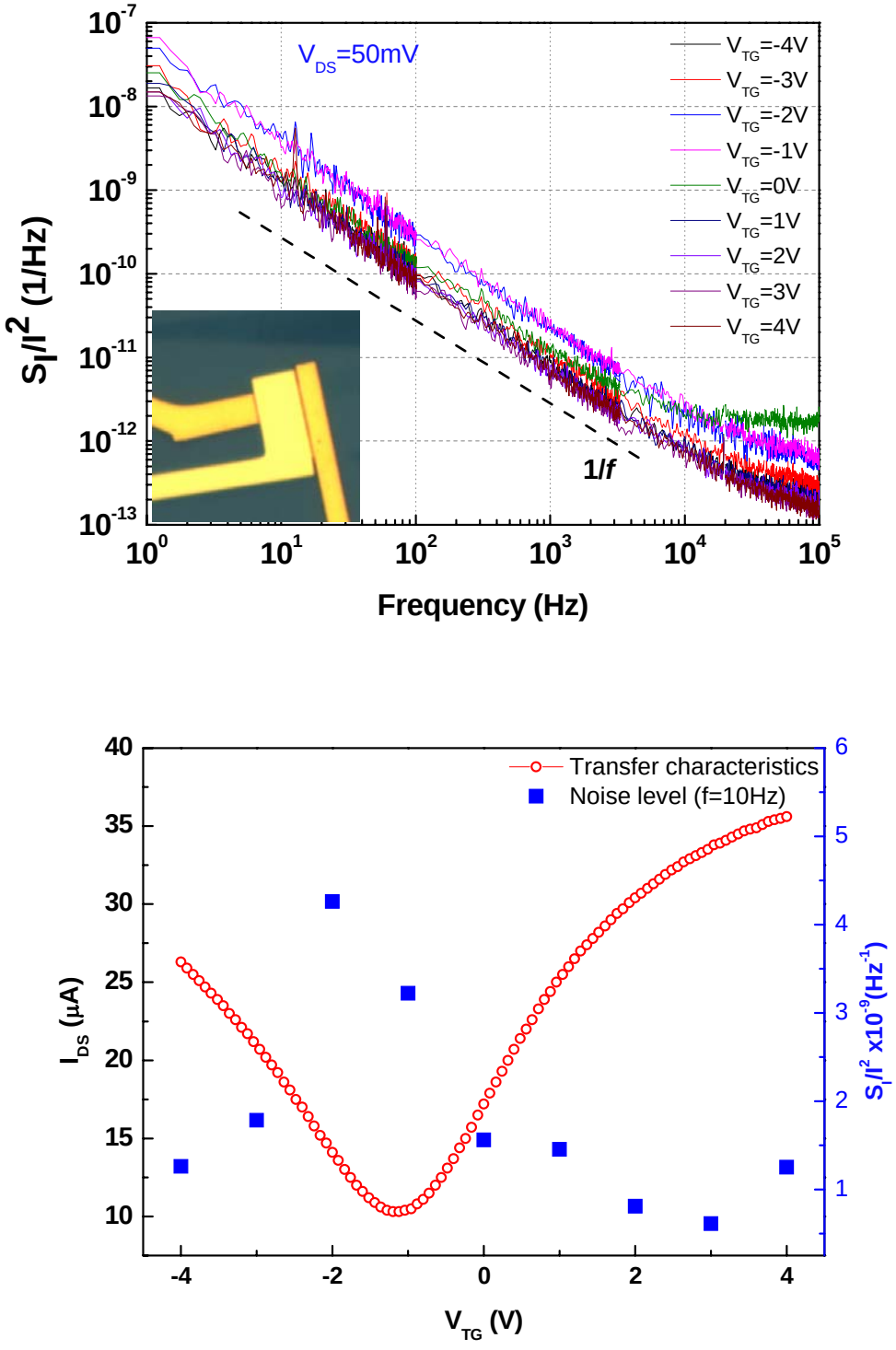

Fig. 5.6. (a) Noise spectral density of a top-gate BLG graphene device under different gate bias. As seen, the spectra are also of 1/f dependence. The inset shows the optical image of this top-gate device. (b) The gate dependence of noise (blue) and the I_{DS}-V_{GS} characteristics (red). In this particular device, the maximum noise happens close to the CNP.

5.5 Noise Reduction in Graded Thickness Graphene

We noticed in our experiment the difference noise behaviors of BLG and SLG, shown in Fig. 5.5. The noise scales with devices channel area in BLG, but not scales well in SLG. Also, the noise level is higher in SLG than in BLG. This brought the question about the noise contribution from contacts and channel. If the noise is dominant by the channel, it should scales with channel size. However, if the contact noise is substantial, the noise will not change that much as the channel size varies. From other side, we know that SLG has larger carrier mobility than in BLG, for high speed electronics, high mobility is favorable. A more important question would be how to reduce the noise in SLG graphene devices. In order to study this issue in more detail, we adopted a new type of graphene device structure which will help to elucidate this question.

The proposed new type of the graphene device is of graded thickness in the direction from the contacts toward the middle. In these devices, the main part of the channel – between the source and drain – has the thickness of one atomic plane (n=1), while the regions closer to the metal contacts have the thickness of two atomic planes (n=2) or more. We refer to this type of FETs as graphene thickness-graded (GTG) transistors. In GTG FETs, the metal contacts are made intentionally on the BLG or few layer graphene (FLG) parts avoiding any contact with the SLG channel (see Fig. 5.7). The conventional exfoliation method to produce graphene also yields such GTG flakes which make this structure available.

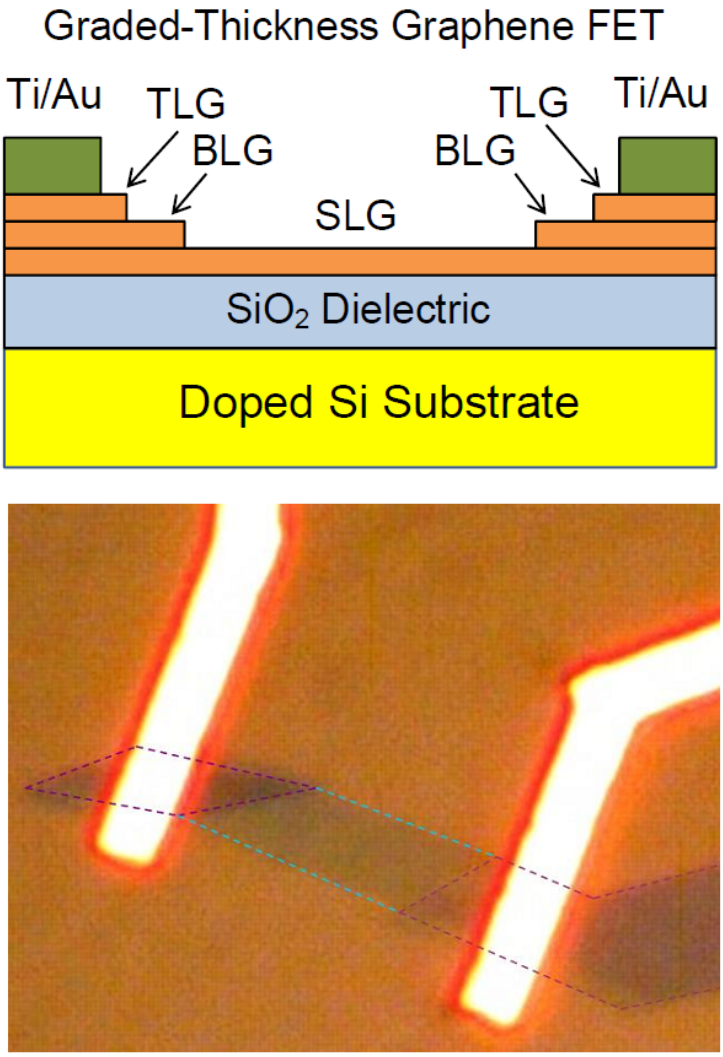

Fig. 5.7. Schematic of the proposed graphene graded-thickness field-effect transistors (upper panel) and an optical microscopy image showing one of such devices (lower panel). The graphene flakes used as the graded-thickness channel is indicated with the dash lines. The darker regions correspond to the few-layer graphene (n=3 in this case). The bright white bars are metal electrodes connected to the source and drain regions. Reprinted with permission from G. Liu, S. Rumyantsev, M. Shur and A.A. Balandin, Appl. Phys. Lett., 100, 033103 (2012). Copyright (2012) APS.

For the proof-of-concept demonstration, we produced the GTG layers by the standard exfoliation method [22] but used the flakes of the ribbon-like shape with the thickness varying from n=1 in the middle to n=3 at the both ends. Initially, the

suitable GTG flakes were identified under the optical microscope. The gradation in the flake thickness was then verified with the micro-Raman spectroscopy utilizing the comparison the 2D/G peak intensity ratio and deconvolution of 2D (G') band [23, 24]. All Raman spectra were measured under 633-nm laser excitation in the backscattering configuration at RT. Details of our Raman microscopy protocols were reported elsewhere [25]. Fig.5.8 shows the Raman spectra from different locations of the same GTG flake on Si/SiO_2 substrate. One can see the signatures of SLG in the middle, BLG in the transition region and FLG at the end of the flake.

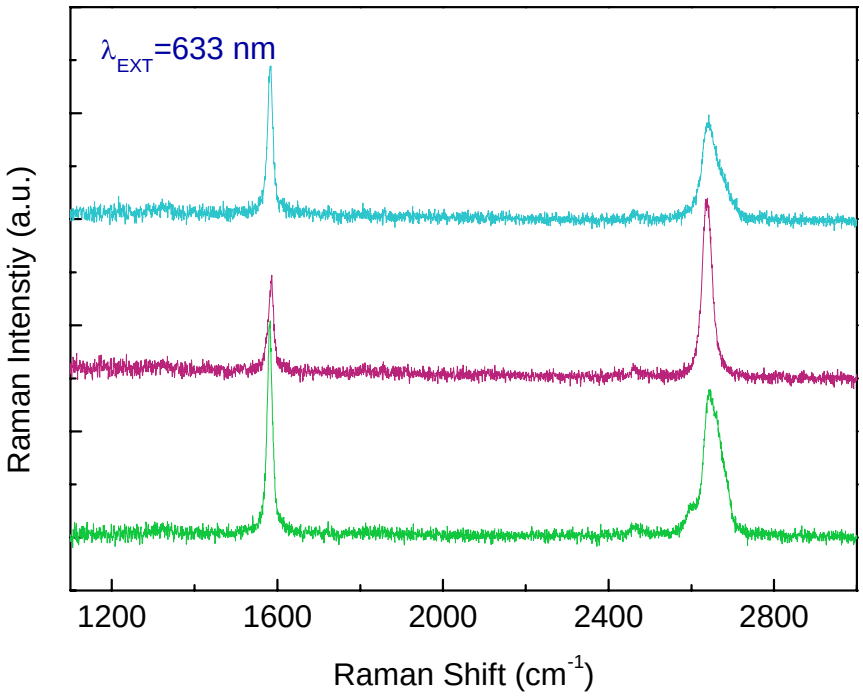

Fig. 5.8. Raman spectra from different regions of the same flake used for fabrication of the channel of the graphene graded-thickness transistor. The middle spectrum displaying clear signatures of the single-layer graphene was recorded from the central region of the channel. The bottom and top spectra characteristic for the few-layer graphene was recorded close to the contact region.

The source and drain electrodes were fabricated by the electron beam lithography (EBL) followed by the electron beam evaporation (EBE), same as described in Chapter 2. The electrode metals were Ti/Au with the thickness of 8-nm/80-nm, respectively. The degenerately doped p-type Si substrate acted as the back gate for tuning the electrical conductivity of the graphene channel. We have also fabricated a large number of SLG and BLG FETs (>15) to be used as references devices for comparison with the GTG FETs.

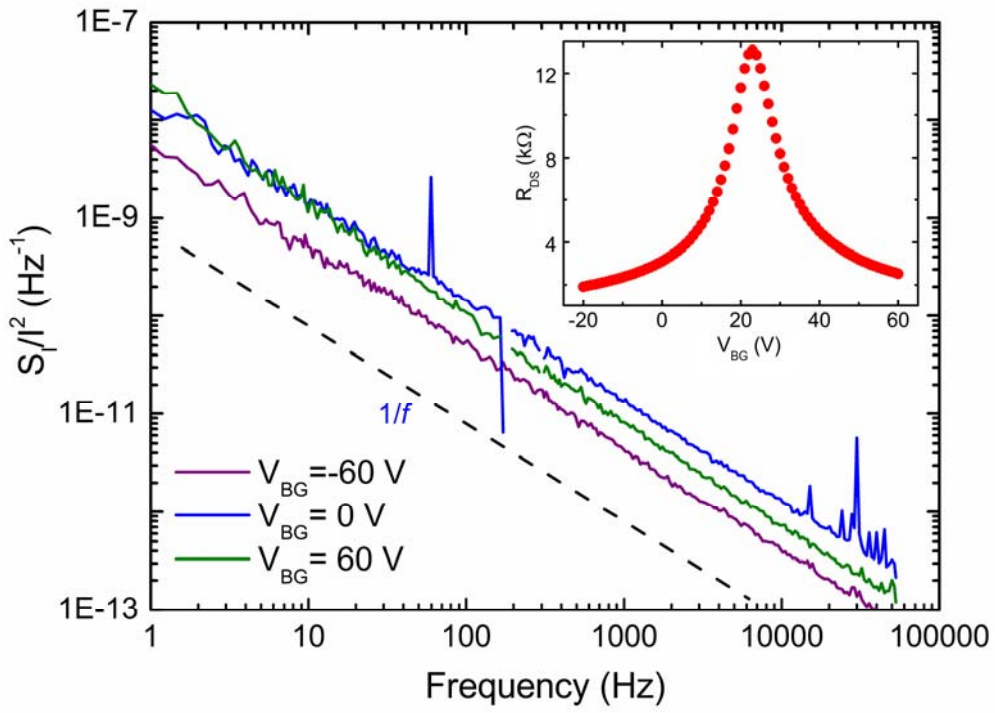

Fig. 5.9. Normalized noise spectrum density as a function of frequency f for several values of the back-gate bias. The 1/f spectrum is added for comparison. The inset shows a typical drain-source resistance characteristic of the graphene thickness-graded transistor near the Dirac point. Reprinted with permission from G. Liu, S. Rumyantsev, M. Shur and A.A. Balandin, Appl. Phys. Lett., 100, 033103 (2012). Copyright (2012) APS.

Fig. 5.9 inset shows the drain-source resistance R_{DS} as a function of the back-gate voltage V_{BG} of the GTG FET measured at ambient conditions. The $R_{DS}(V_{BG})$

dependence is similar to that in conventional SLG FETs. The fabricated devices were robust and retained their current-voltage (I-V) over the testing period of several weeks at ambient. The SLG, GTG and BLG FETs, fabricated using the same process, had the RT electron mobility μ values in the ranges ~5000 – 7000 cm^2/Vs, ~4000 – 5000 cm^2/Vs and ~1000 – 2000 cm^2/Vs, respectively. GTG FETs retained the high mobility values close to those characteristic for SLG devices.

Following the I-V characterization, the low-frequency noise was measured with a spectrum analyzer. Fig. 5.9 shows representative low-frequency noise spectra in GTG FETs. The spectra reveal 1/*f* noise spectral density in the frequency range from 1 Hz to 100 kHz similar to that observed in SLG and BLG FETs. No G-R bulges were observed in the tested GTG FETs. We have examined the normalized noise spectral density S_I/I^2 dependence on the area of the device channels A. As seen in Fig. 5.10, S_I/I^2 in the reference BLG devices decreases with the increasing channel area, A, while the 1/*f* noise in the SLG devices shows only weak area dependence. The strong dependence of the noise spectral density in BLG FETs on A (noise level scales with the area of two-dimensional channel) indicates that the main contribution to the 1/*f* noise comes from the graphene channel. The weak A dependence in SLG FETs suggests that the contribution of the contact noise is substantial. As seen in Fig. 5.10, GTG FETs produce less noise than SLG FETs and have the S_I/I^2 dependence on the channel area. This means that by using the specially designed device structure, which is SLG in middle but has FLG thickness at the contact regions, we were able to reduce

the metal-graphene contact contribution to the low-frequency noise. This result also provides additional evidence that the contacts in conventional SLG devices can substantially contribute to the noise level.

We now offer a physical model, which explains the noise reduction in GTG FETs by the lower potential fluctuations at the metal – FLG interface as compared to those at the metal – SLG interface. Fabrication of the metal contacts to graphene leads to the metal doping of graphene via the charge transfer to reach the equilibrium conditions, and, correspondingly, results in the local shift of the Fermi level position in graphene. Theory suggests that metals with the work functions different from graphene, can dope graphene both n-type and p-type [26]. The electron density of states (DOS) in SLG in the vicinity of the charge neutrality point is low owing to the Dirac-cone linear dispersion. For this reason, even a small amount of the charge transfer from or to the metal can strongly affect the Fermi energy of graphene. The values of ΔE_F=-0.23 eV and ΔE_F=0.25 eV were reported for Ti and Au contacts to graphene, respectively [27]. The scanning photocurrent studies confirmed the strong non-uniform potential variations at the metal-graphene contact edge [27, 28]. These non-uniform variations are also gate bias dependent [28]. The quadratic energy dispersion of BLG results in DOS, which is different from that in SLG. Thus, with the same amount of charge transfer between the metal and graphene – determined by the work function difference – will lead to the smaller Fermi level shifts in BLG than in SLG owing to the larger DOS in BGL (see inset to Fig. 5.10). Although there should

also be non-uniform potential between the metal and bi-layer graphene edge, the magnitude of the potential barrier fluctuations will be smaller than in the metal-SLG interface.

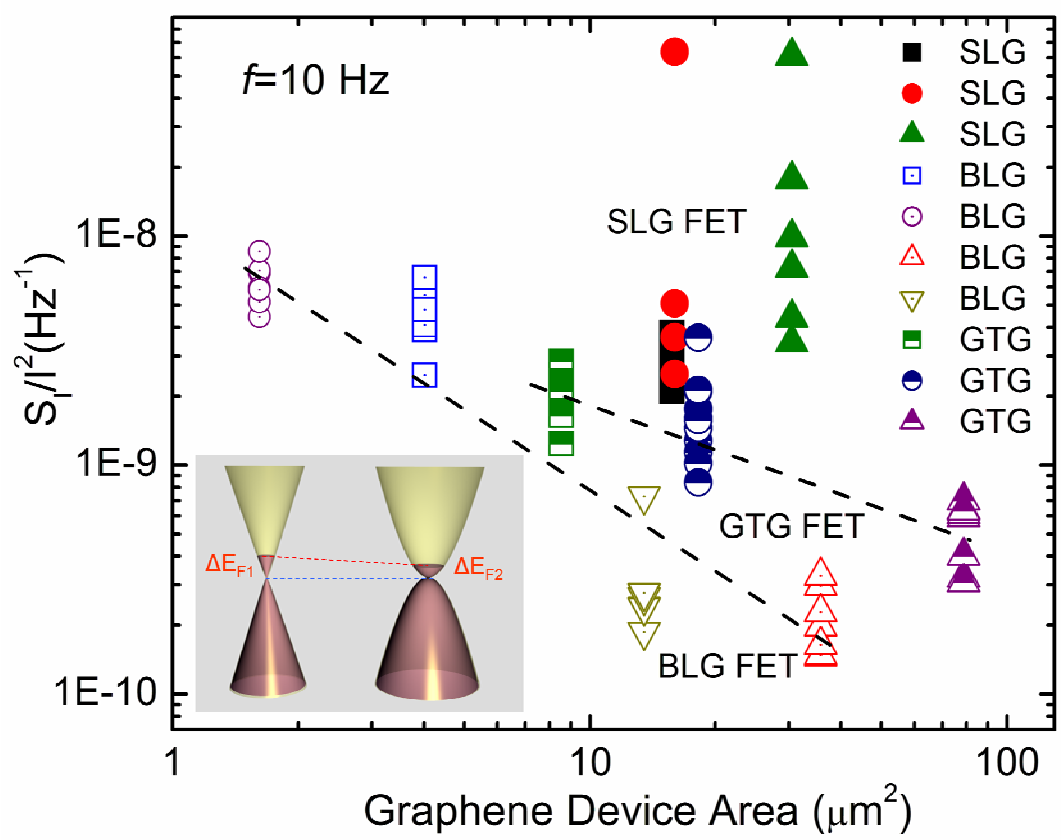

Fig. 5.10. Normalized noise spectral density of the GTG FETs and the reference SLG and BLG FETs as the function of the graphene channel area. The filled symbols represent SLG, the open symbols—BLG while the half-filled symbols indicate the data-points for GTG FETs. For each device the data are shown at several biasing points within the $|V_{BG}-V_{CNP}|$ =30V range from the charge neutrality point VCNP. Note that GTG FETs have the reduced noise level, close to that the in BLG FETs, while revealing the electron mobilities almost as high as in SLG FETs. The inset shows the band structure of SLG and BLG in vicinity of the charge neutrality point. The same amount of the charge, transferred owing to the metal contact doping, leads the smaller local Fermi level shift in BLG devices than in SLG devices. Reprinted with permission from G. Liu, S. Rumyantsev, M. Shur and A.A. Balandin, Appl. Phys. Lett., 100, 033103 (2012). Copyright (2012) APS.

The potential fluctuations due to the traps at interface between Si/SiO_2 were

identified as the origin of 1/*f* noise in the Si metal-oxide-semiconductor field-effect transistors (MOSFETs) [29]. The local potential fluctuations can contribute to the low-frequency noise via both mobility-fluctuation and carrier number fluctuation mechanisms [14]. It follows from the above discussion that the contact between the metal and SGL will have stronger potential in-homogeneities than that between the same metal and FLG not only for the technological but also for fundamental reasons related to the electron DOS. The latter explains the observed reduction of the 1/*f* noise level in our GTG FETs. It has been previously stated that the resistivity of the metal-graphene contacts will be the performance-limiting characteristic in graphene devices [30]. The present results suggest that the metal-graphene contacts are also the important factor for the 1/*f* noise level in graphene devices.

In conclusion, this new type of graphene devices structure, graphene thickness-graded transistors, which combines the high electron mobility of a single-layer graphene and the low 1/*f* noise of the bilayer graphene devices. The investigation of the noise spectra in this new device revealed the contribution of the metal-graphene contact to the overall noise level and shed light on the origin of the low-frequency fluctuations in graphene devices.

5.6 Summary

Graphene devices exhibit 1/f noise in the low-frequency range from 1 Hz to 100 kHz. Considering graphene is only a surface material, the resistance fluctuation is

expected to be very strong as it entirely exposes to the environment. However, as we measured the noise, it shows rather low level of noise, with Hooge parameter on the order of 10^{-3}-10^{-4}. This is probably due to the very high mobility of graphene.

The contact between metal and single layer graphene generates substantial noise which can not be ignored. It is due to the very low density of state at the CNP of graphene. By using GTG structure, one can see the significant reduced noise from the contact, while preserving the high carrier mobility of SLG.

Reference

[1] M. von Haartman and M. Ostling, Low-Frequency Noise in Advanced MOS Devices. Dordrecht, The Netherlands: Springer, 2004.

[2] J.B. Johnson, *Phys. Rev.*, **32**, 97 (1928).

[3] H. Nyquist, *Phys. Rev.*, **32**, 110 (1928).

[4] F. Schwierz, *Nat. Nanotechnol.*, **5**, 487 (2010).

[5] Y.-M. Lin, C. Dimitrakopoulos, K.A. Jenkins, D.B. Farmer, H.-Y. Chiu, A. Grill and P. Avouris, *Science*, **5**, 662 (2010).

[6] K.I. Bolotina, K.J. Sikes, Z. Jianga, M. Klima, G. Fudenberg, J. Hone, P. Kim and H. L. Stormer, *Solid State Commun.*, **146**, 351 (2008).

[7] A. Akturk and N. Goldsman, *J. Appl. Phys.*, **103**, 053702 (2008).

[8] R.S. Shishir and D.K. Ferry, *J. Phys. Condens. Matter*, **21**, 344201 (2009).

[9] A.A. Balandin, S. Ghosh, W. Bao, I. Calizo, D. Teweldebrhan, F. Miao and C.N. Lau, *Nano Lett.*, **8**, 902 (2008).

[10] A.A. Balandin, *Nat. Mater.*, **10**, 569 (2011).

[11] X. Yang, G. Liu, A.A. Balandin and K. Mohanram, *ACS Nano*, **4**, 5532 (2010).

[12] X. Yang, G. Liu, M. Rostami, A.A. Balandin and K. Mohanram, *IEEE Electron Device Lett.*, 32, 1328 (2011).

[13] Q. Shao, G. Liu, D. Teweldebrhan, A.A. Balandin, S. Rumyantsev, M. Shur and D. Yan, *IEEE Electron Device Lett.*, **30**, 288 (2009).

[14] A.A. Balandin, Noise and Fluctuation Control in Electronic Devices. Los

Angeles, CA: American Scientific Publishers, 2002.

[15] A.L. McWhorter, Semiconductor Surface Physics. Philadelphia, PA: University of Pennsylvania Press, 1957, p 207.

[16] C. Surya and T.Y. Hsiang, *Phys. Rev. B* , **33**, 4898 (1986).

[17] S. Christensson, I. Lundstrom and C. Svensson, *Solid-State Electron.*, **11**, 797 (1968).

[18] A.P. Dmitriev, E. Borovitskaya, M.E. Levinshtein, S.L. Rumyantsev and M.S. Shur, *J. Appl. Phys.*, **90**, 301 (2001).

[19] Y.- M. Lin and P. Avouris, *Nano Lett.*, **8**, 2119 (2008).

[20] F.N. Hooge and A.M.H. Hoppenbrouwers, *Physica*, **45**, 386 (1969).

[21] A.N. Pal, S. Ghatak, V. Kochat, E.S. Sneha, A. Sampathkumar, S. Raghavan and A. Ghosh, *ACS Nano*, **5**, 2075 (2011).

[22] K.S. Novoselov, A.K. Geim, S.V. Morozov, D. Jiang, Y. Zhang, S.V. Dubonos, I.V. Grigorieva and A.A. Firsov, *Science*, **306**, 666 (2004).

[23] A.C. Ferrari, J.C. Meyer, V. Scardaci, C. Casiraghi, M. Lazzeri, F. Mauri, S. Piscanec, D. Jiang, K.S. Novoselov, S. Roth and A.K. Geim, *Phys. Rev. Lett.*, **97**, 187401 (2006).

[24] I. Calizo, F. Miao, W. Bao, C.N. Lau and A.A. Balandin, *Appl. Phys. Lett.*, **91**, 071913 (2007).

[25] I. Calizo, I. Bejenari, M. Rahman, G. Liu and A.A. Balandin, *J. Appl. Phys.*, **106**, 043509 (2009).

[26] G. Giovannetti, P.A. Khomyakov, G. Brocks, V.M. Karpan, J. van den Brink and P.J. Kelly, *Phys. Rev. Lett.*, **101**, 026803 (2008).

[27] E.J.H. Lee, K. Balasubramanian, R.T. Weitz, M. Burghard and K. Kern, *Nat. Nanotechnol.*, **3**, 486 (2008).

[28] X. Xu, N.M. Gabor, J.S. Alden, A.M. van der Zande and P.L. McEuen, *Nano Lett.*, **10**, 562 (2010).

[29] E.H. Nicollian and H. Melchior, *Bell Syst. Tech. J.*, **46**, 2019 (1967).

[30] K. Nagashio, T. Nishimura, K. Kita and A. Toriumi, *Appl. Phys. Lett.*, **97**, 143514 (2010).

Chapter 6

Modification of Graphene through E-Beam Irradiation

The controllable property modification method of material is very important for the semiconductor industry. For example, n-type and p-type silicon are obtained by doping the intrinsic silicon by As, P and B. The doping level affects the Fermi level, conductivity, mobility and many other properties. Hence, more functionality can be achieved by combining different types of devices together, such as complementary metal-oxide-semiconductor field-effect transistor (CMOS). It would be necessary to find method to modify the properties of graphene in a similar fashion.

6.1 Introduction of Quality control through Raman Spectroscopy

An important method of examine the material property is by the Raman spectroscopy. Raman spectroscopy is a technique used to study vibration, rotation, and other low-frequency modes in a system by shining a mono-frequency laser on the sample. The interaction between the laser and the molecular vibrations, phonons will result in the energy change of the reflected laser light. This shift of the energy can provide the information of the vibration modes in the studied material. Another advantage of Raman spectroscopy is its efficiency. Usually, it only takes few seconds to collect one spectrum and no particular sample preparation is needed.

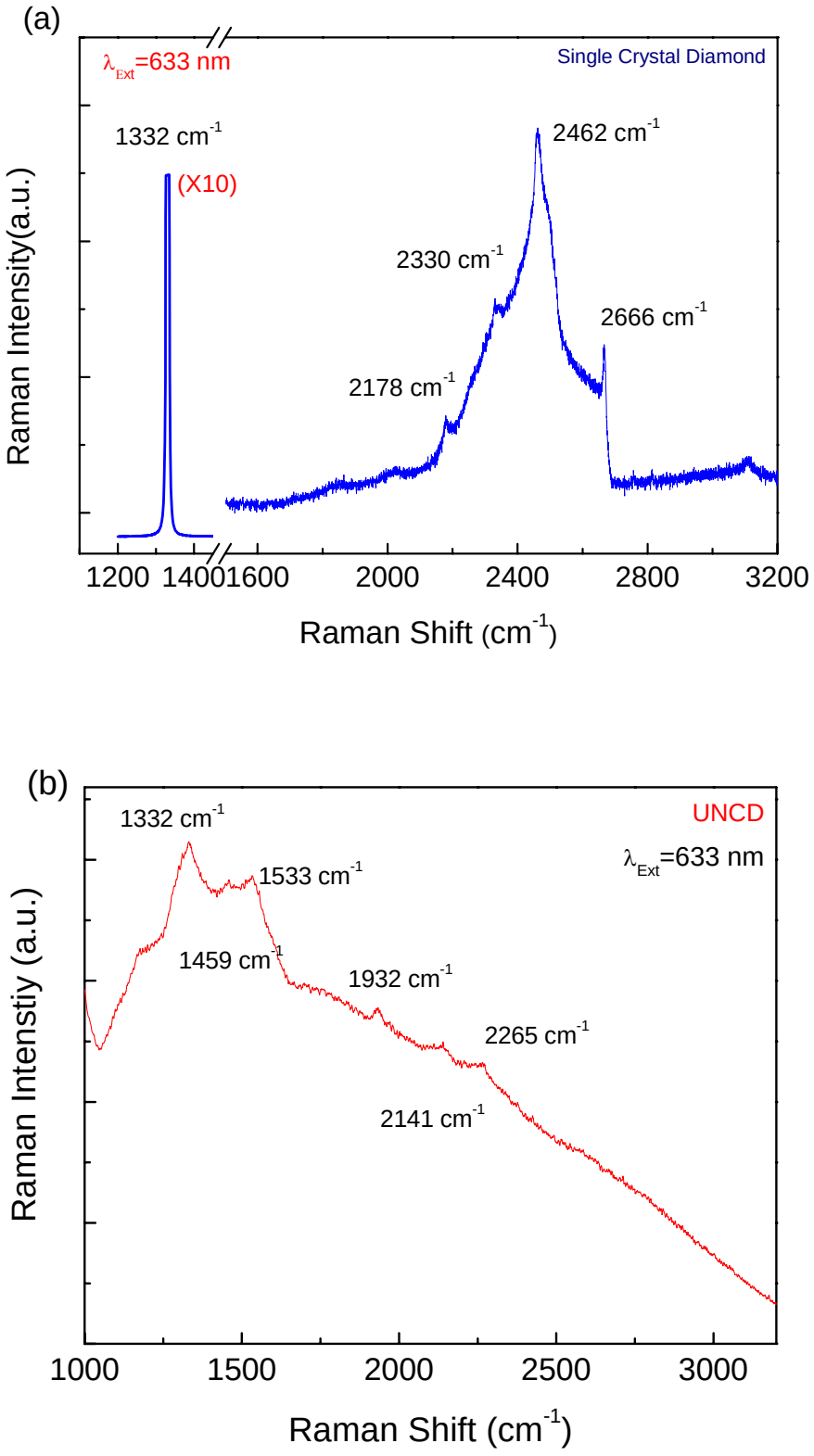

Fig. 6.1. Raman spectrum of (a) synthetic single crystal diamond and (b) ultra nano crystalline diamond (UNCD). The numbers indicates the positions of the peaks.

The Raman spectroscopy has been widely used for carbon material studies, such as carbon nanotubes [1], synthetic diamonds [2], and graphene [3, 4]. Fig. 6.1 shows the Raman spectrum of synthetic single crystal diamond and ultra-nano-crystalline diamond. The peaks and bands in the spectrum are related to the different vibration modes in the material. Table 6.1 lists the assignment of the peaks and bands [5].

Measured (cm^{-1})	Explanation	Combinations (cm^{-1})	Total (cm^{-1})
1332	Zone center optical phonon	1332±0.5	1332±0.5
2462	TO ($L^{(3-)}$)+LO($L^{(2-)}$)	1210±37,1242±37	2452±72
2178	L($W^{(2)}$)+TO($W^{(1)}$)	1168±53, 993±53	2161±106
2666	Second order of zone center optical phonon	1332±0.5	2665±1

Table 6.1. The Raman peak assignment of single crystal diamond shown in Fig. 6.1 (a)

Measured (cm^{-1})	Explanation	Combinations (cm^{-1})	Total (cm^{-1})
1170	Nanocrystalline hexagonal diamond [6]	N/A	N/A
1332	Zone center optical phonon	1332±0.5	1332±0.5
1459	A weak feature observed in diamonds implanted with ions of energy in the MeV range [6]	N/A	N/A
1533	amorphous carbon [7]	N/A	N/A
2265	L($X^{(1)}$)+TO($X^{(4)}$) [5]	1184±21, 1072±26	2256±47

Table 6.2. The Raman peak assignment of ultra nano crystalline diamond shown in Fig. 6.1 (b).

The Raman spectroscopy has been successfully applied in material characterization of graphene [4]. The number of layers can be counted by using the shape of second order 2D band at 2700 cm^{-2}. The defects in graphene can be characterized with the D peak at around 1350cm^{-1}.

6.2 Electron-Beam Irradiation Effects on Graphene

Electron-beam irradiation effects on nano-carbon material, such as single wall and multi-wall carbon nanotube have been studied by using high energy TEM [8, 9]. The high energy electron-beam is able to knock-off carbon atoms from the nanotubes. Considering tuning graphene properties rather than greatly damage its lattice structure, we use moderate energy electron-beam (20 kV) to irradiate the SiO_2 supported graphene.

The electron-beam irradiation is conducted by using electron-beam lithography (EBL) system, which allows for accurate control of the exposed area and irradiation dose. Special precautions have been taken to avoid additional unintentional e-beam irradiation. The alignment program in the utilized EBL system offers a way to scan only the alignment marks without exposing other locations. We used the gold alignment marks located more than 30 μm away from the graphene device to avoid unintentional irradiation during the scanning steps. For our experiments we selected the accelerating voltage of 20 kV and the working distance of 6 mm (the same as in EBL process). The area dosage was calculated and controlled by the nanometer pattern generation system (NPGS). NPGS allowed us to control the scanning distance from point to point and set the dwelling time on each point. The beam current, used in calculation of the irradiation dose, was measured using a Faraday cup. The beam current for all the irradiation experiments in this work was 30.8 pA. The experiments

were conducted in a following sequence. First, the back gated graphene devices were irradiated with a certain dose of electrons. Second, the irradiated graphene devices were examined using micro-Raman spectroscopy to detect any changes with the Raman signatures of graphene. Third, the current-voltage (I-V) characteristics were measured to examine the changes of electrical properties. After I-V data were collected, the irradiation dose was increased and all steps repeated.

The electron-beam irradiation was performed inside the SEM vacuum chamber with a low pressure (10^{-7} Torr), and the Raman spectroscopy and electrical measurements were carried out at ambient conditions. We used a Reinshaw InVia micro-Raman spectrometer system with the laser wavelength of 488 nm. The electrical measurements were performed with an Agilent 4142B instrument. Fig. 6.2 (a) shows an optical image of a typical SLG graphene device. In Fig. 6.2(b) illustrates the irradiation process showing the exposed and shielded regions of the device under test. The devices and irradiation process were intentionally designed in such a way that only graphene channel is exposed to the e-beam while the metal contacts are not irradiated. The latter allowed us to avoid any possible changes in metal contact resistance after the irradiation.

We started by measuring the electrical resistance between the source and drain as a function of the applied gate bias. Fig. 6.3 (a) shows the evolution of the electrical characteristics of SLG device after each irradiation step. The electron irradiation dose for each step is indicated in the figure's legend. As one can see, the ambipolar

property of graphene is preserved after irradiation within the examined dosage range. The observed up shift of the curves indicates increasing resistivity of graphene over a wide range of carrier concentration. The increase is especially pronounced after the 4th step with a higher irradiation dose (1280 μC/cm^2).

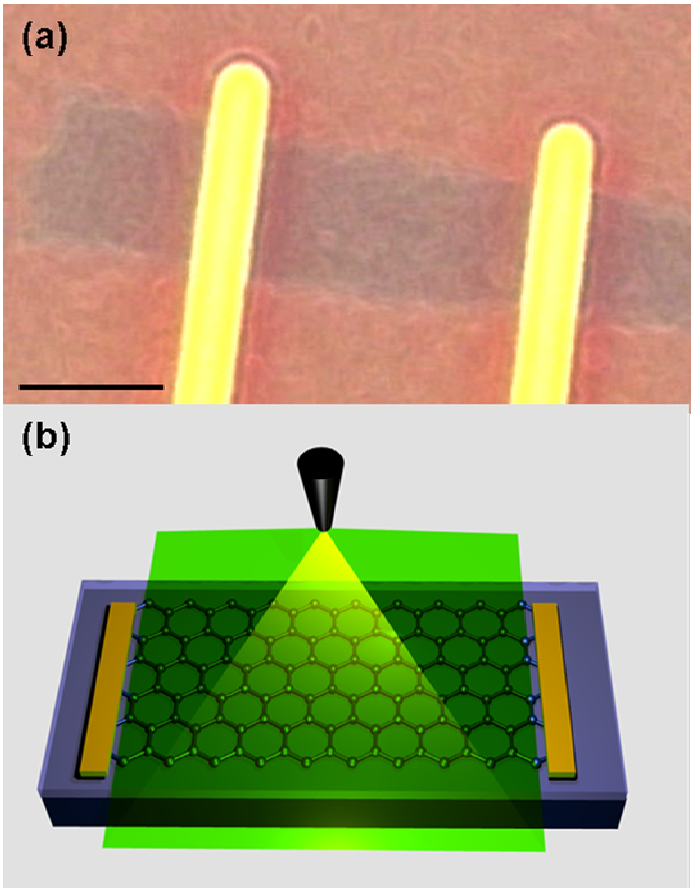

Fig. 6.2. (a) Optical image of a typical graphene device used in this work. The contrast is enhanced. The dark blue region is graphene. The metal electrodes are source and drain contacts, and heavily doped silicon wafer is used as a back gate. The scale bar is 2 μm. (b) Schematic of the irradiation by the electrion beam. The green rectangular region is the irradiation area, which covers graphene between the source and drain while excludes two electrodes to avoid possible changes of the contact resistance due to irradiation. Reprinted with permission from G. Liu, D. Teweldebrhan and A.A. Balandin, IEEE Trans. Nanotechnol., 10, 865 (2011). Copyright (2011) IEEE.

The inset to Fig. 6.3 (b) shows the fitting result based on the mobility extraction method described in Chapter 3. Note that the fitting dose not cover the interval close

to the charge neutrality point because this region is characterized by a large uncertainty in the data. The fitting was conducted separately for the negative and positive gate bias regions. For simplicity, we consider the fitting results from the p-type branch. The estimated contact resistance of 446 Ω, the initial mobility μ=5075 cm^2/Vs, and the charge impurity concentration of $2.13\times10^{11}cm^{-2}$, which are very close to the typical values for clean graphene samples [10]. During the experiments the irradiated regions excluded the contacts. For this reason, the contact resistance should not change during the measurements and we can estimate the resistance of the irradiated graphene channels by subtracting the contact resistance from the total resistance.

We noticed that the total resistance increased as the irradiation, hence we introduce this irradiation induced resistance, $R_{Ird}=(L/W)\rho_{Ird}$, which is the resistance increment induced by e-beam irradiation. Fig. 6.3 (b) shows the evolution of the mobility as a function of e-beam irradiation dosage for three SLG devices. We note that the mobility decreases monotonically and drops from 4000-5000 cm^2/Vs to 2000 cm^2/Vs (50~60%) in the first 4 steps. The mobility reduction starts to stop after the 4^{th} step of irradiation. This evolution coincides with the abrupt change of the total resistance of the device. Moreover, it also coincides with the induced D peak with irradiation, which will be shown as we examine the Raman spectra.

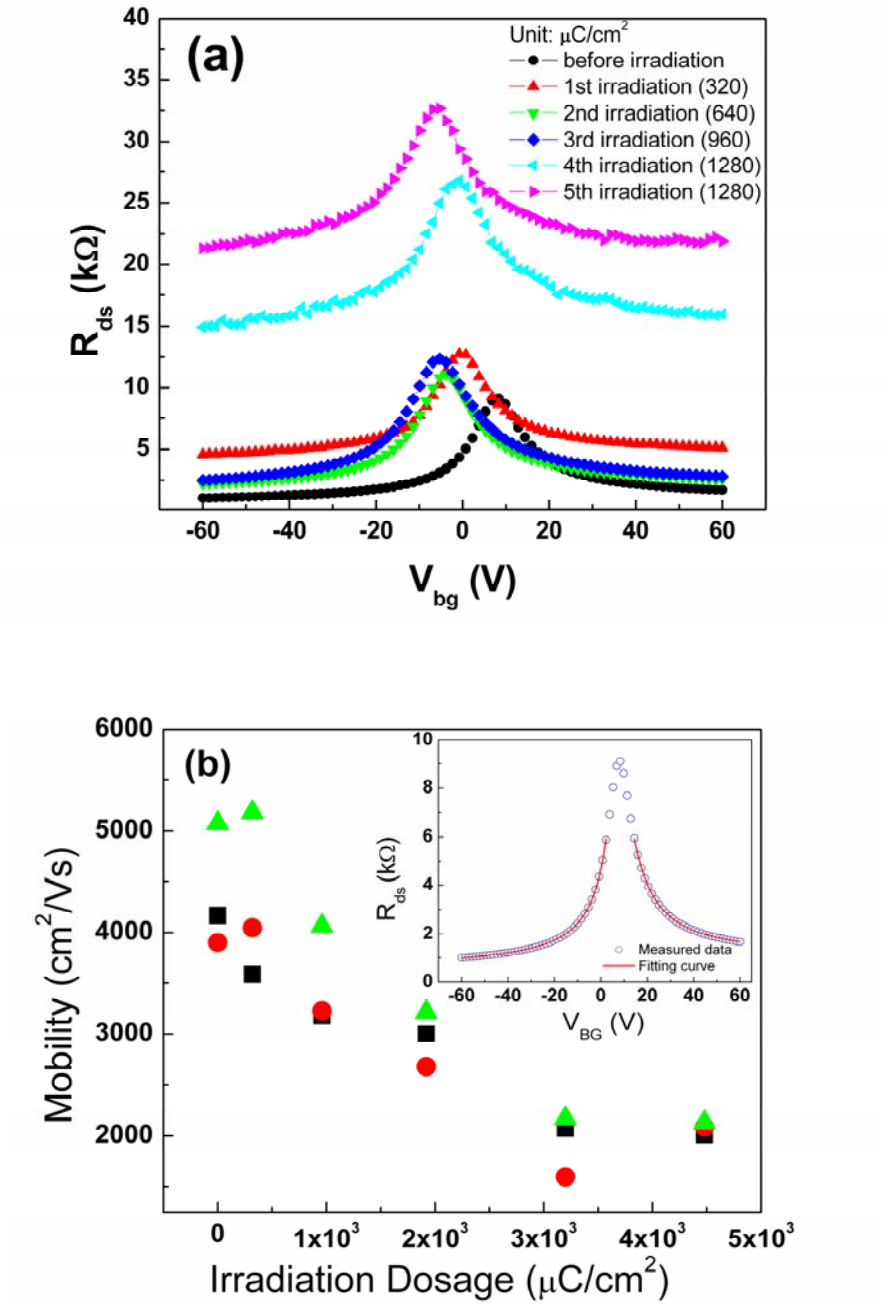

Fig. 6.3. (a) Evolution of the transfer characteristics of SLG with increasing irradiation dose. The electrical resistance of SLG devices was measured after each irradiation step. The irradiation dose is indicated in the legend. (b) Charge carrier mobility as a function of the irradiation dose for three SLG devices, represents by red, green and black data points, respectively. Note a nearly linear decrease of the mobility with the irradiation dose. The inset shows the measured and fitted electrical resistance as a function of the back gate for one of the devices. Reprinted with permission from G. Liu, D. Teweldebrhan and A.A. Balandin, IEEE Trans. Nanotechnol., 10, 865 (2011). Copyright (2011) IEEE.

We carefully examined the Raman spectra of the graphene devices after each irradiation step. One can see from Fig. 6.4 (a) that the pristine graphene has typical signatures of SLG: symmetric and sharp 2D band (~2700 cm^{-1}) and large I(2D)/I(G) ratio. The absent or undetectably small D peak at 1350 cm^{-1} indicates the defect-free high-quality graphene. The disorder D peak appears after the first step of electron beam irradiation. Initially the intensity of the D grows with increasing dosage after each irradiation step. However, it is not a monatomic phenomenon. This trend starts to reverse after the irradiation dose reaches a certain level. We used the intensity ratio I(D)/I(G) to characterize the relative strength of the D peak [3, 11]. The ratio I(D)/I(G) reveals a clear and reproducible non-monotonic dependence on the irradiation dose (see Fig. 6.4 (b)). This behavior was observed in all devices in our experiments. It is consistent with our earlier studies [11]. A similar trend was also reported on graphite that the ratio I(D)/I(G) was increasing and then decreasing with the irradiation dose. Such dependence was attributed to the crystal structure change from crystalline to nanocrystalline and then to amorphous form [3]. The bond breaking in such cases is likely chemically induced since the electron energy is not sufficient for the ballistic knock out of the carbon atoms.

Other factors contributing to the growth of the disorder D peak can be the contaminant molecules or water vapor, which dissolve under irradiation and may form bonds with the carbon atoms of the graphene lattice.

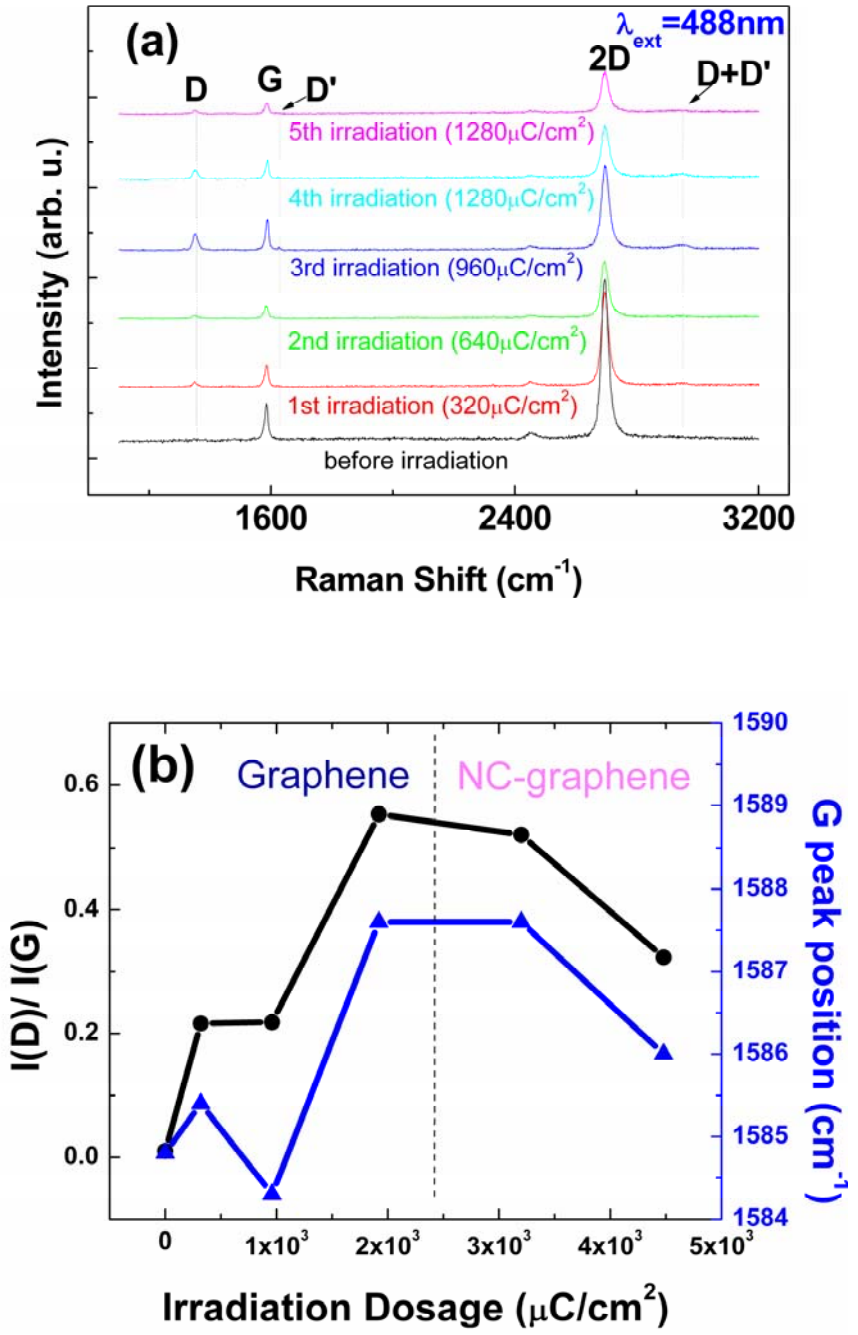

Fig. 6.4. (a) Evolution of Raman spectrum of SLG with increasing irradiation dose. The spectrum of pristine graphene before irradiation does not reveal the disorder band. A pronounced disorder D peak near ~1350 cm^{-1} appears after irradiation. Another D' peak (~1620 cm^{-1}) and higher order harmonic D+D' (~2950 cm^{-1}) are also induced by irradiation. (b) The ratio I(D)/I(G) initially increases with the irradiation dose but starts to decrease after the 3rd irradiation step (black curve). The G peak position also reveals a non-monotonic dependence with the irradiation dose following a similar trend as the I(D)/I(G) ratio. Reprinted with permission from G. Liu, D. Teweldebrhan and A.A. Balandin, IEEE Trans. Nanotechnol., 10, 865 (2011). Copyright (2011) IEEE.

The change in the G peak position under the electron beam irradiation is shown in Fig. 6.4 (b). The G peak position shifts to higher wave numbers with increasing irradiation dose (with exception for the 2nd step). But after certain dose (step four) the peak position starts to move to the lower wave numbers. A similar trend was also observed in graphite [3]. It is reasonable to believe that e-beam irradiation leads to disorder in graphene's crystal lattice via formation of defects.

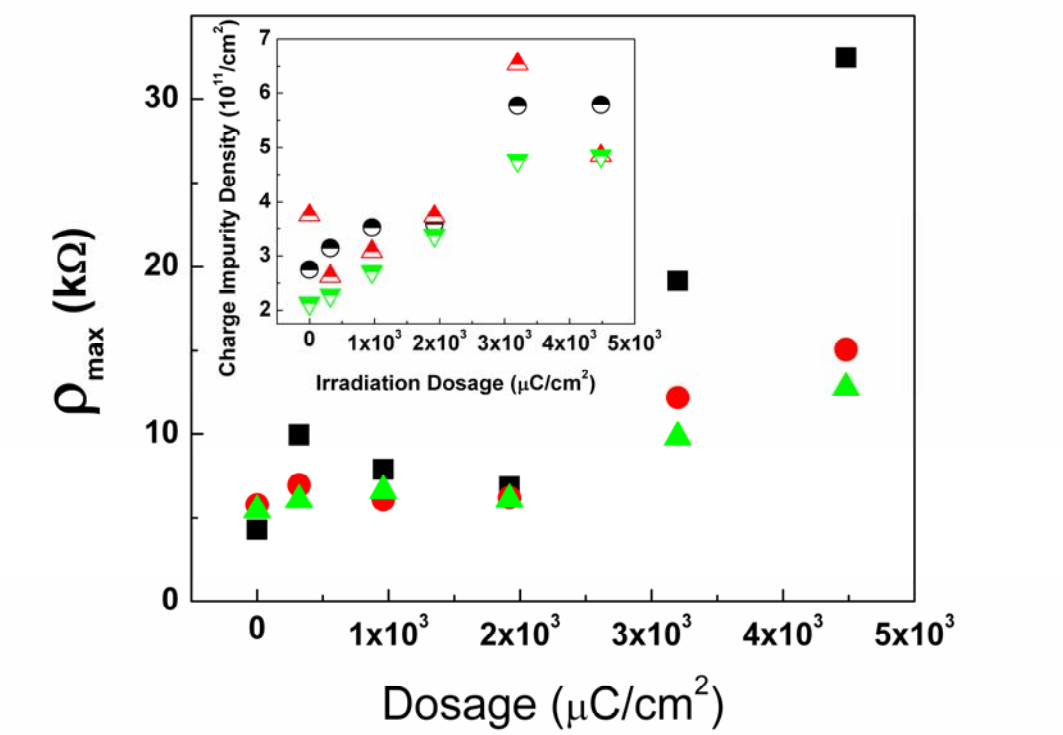

Fig. 6.5. Evolution of SLG resistivity with irradiation dose. The inset shows the effect of e-beam irradiation on the charge density for three SLG devices, represents by red, green and black data points, respectively. Reprinted with permission from G. Liu, D. Teweldebrhan and A.A. Balandin, IEEE Trans. Nanotechnol., 10, 865 (2011). Copyright (2011) IEEE.

In addition to D peak we also observed the appearance of other peaks in Raman spectrum of irradiated graphene. The peak at ~1620 cm^{-1}, referred to as D', was

detected after the second step of irradiation. This peak was attributed to the intra-valley double-resonance process in the presence of defects [12]. The electron-beam irradiation also activates the peak denoted as D+D' at around 2950 cm^{-1}. This peak, unlike the 2D and 2D' bands, is due to a combination of two phonons with different momentum and requires defects for its activation. A slight broadening of 2D band and decrease of the I(2D)/I(G) ratio were also observed. The decrease of the I(2D)/I(G) ratio was previously attributed to increasing concentration of charged defects or impurities [13]. Our electrical measurements are consistent with this interpretation indicating a growing density of the charged impurities with increasing irradiation dose (see inset to Fig. 6.5).

Fig. 6.5 shows evolution of the resistivity (sheet resistance) near the charge neutrality point with the irradiation dose. One can see a clear trend of increasing ρ_{max} with the irradiation dose. Since the contacts were not irradiated during the experiment, the overall increase of device resistance is due to the increasing resistivity of the irradiated graphene. This can be understood by the induced defects that create an increasing number of scattering centers in the graphene lattice. Note that the ρ_{max} increases by a factor of ~ 3 to 7 for SLG devices.

6.3 E-Beam Irradiation Effects on Bilayer Graphene

In order to compare SLG with BLG under e-beam irradiation we conducted the same experiments with the back gated BLG devices. The only difference was a higher

dose of irradiation for BLG than for SLG. The first step was 1600 μC/cm^2 compared to 320 μC/cm^2 in the first step for SLG. We expected that a larger dose would be required for BLG from the analogy with the multi-wall carbon nanotubes (CNTs), which were found to be less susceptible to e-beam irradiation than the single-wall CNTs [14].

We again used Raman spectroscopy to monitor the evolution of the material properties revealed by I-V measurements. We observed substantially different irradiation induced effects in BLG as compared to SLG devices. Fig. 6.6 (a) shows evolution of the transfer characteristics for a typical BLG device with increasing irradiation dose. The total electron irradiation dose shown for BLG is 27200μC/cm^2 while that for SLG is only 4480 μC/cm^2. In Fig. 6.6 (b) we present the effect of irradiation on the charge carrier drift mobility in BLG devices. One can see that the overall trend is similar to the SLG case but the mobility decrease rate is quite different. Our data indicate that the BLG is much less susceptible to e-beam irradiation than SLG. Indeed, if we look at the irradiation dose below 4480 μC/cm^2 we see that the mobility drop is smaller than 25% for BLG compared with ~50-60% drop for SLG. At the irradiation dose above 12000 μC/cm^2, the mobility decrease rate also reduces for the two high mobility devices but for low-mobility devices the mobility decrease rate is roughly constant within the examined range. This is a similar behavior to the one reveled by SLG devices but requires much higher irradiation doses to be observed.

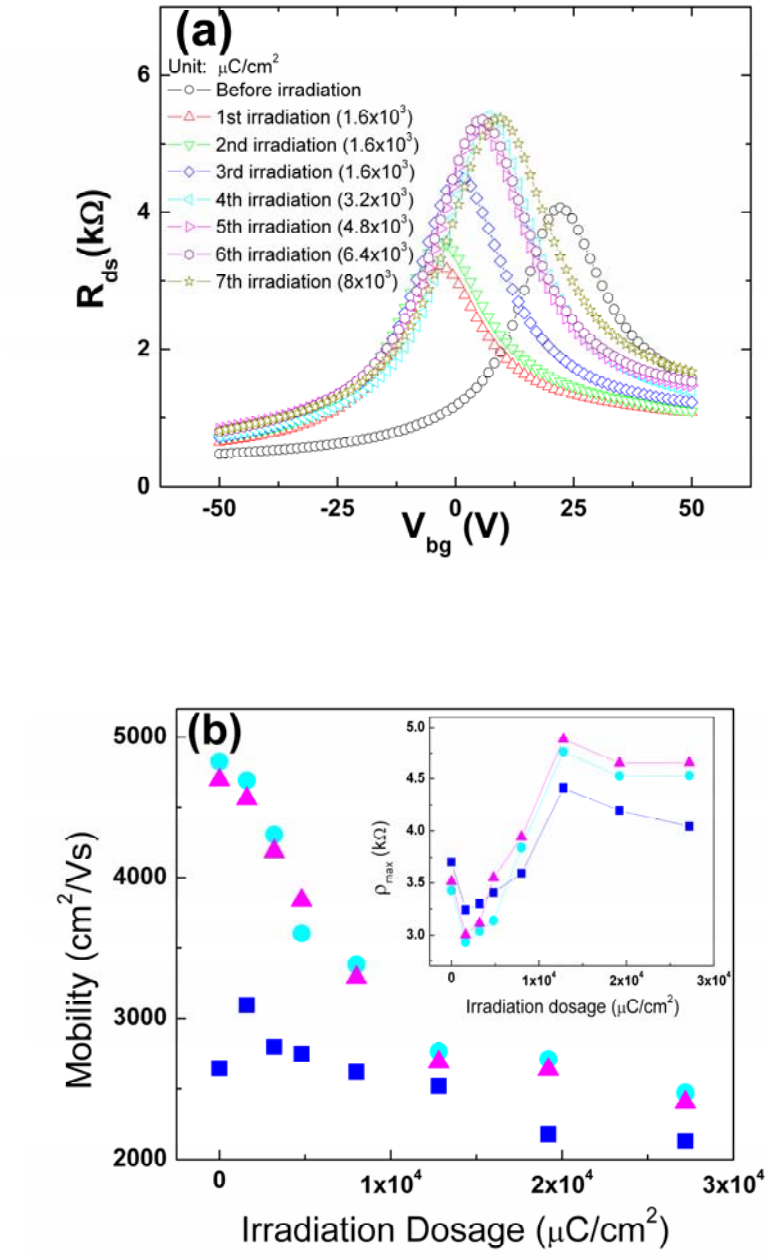

Fig. 6.6. (a) Evolution of the transfer characteristics of BLG with increasing irradiation dose. The irradiation dose after each step is indicated in the legend. (b) Carrier mobility of BLG devices as a function of the irradiation dose for three BLG devices, shown by pink, cyan and blue data points, respectively. Note that the for two devices with higher mobility the dependence has a turning point at the dose of about 12000 μC/cm^2 but for the device with lower mobility the decrease is approximately linear. The inset shows the electrical resistivity as a function of the irradiation dose. Reprinted with permission from G. Liu, D. Teweldebrhan and A.A. Balandin, IEEE Trans. Nanotechnol., 10, 865 (2011). Copyright (2011) IEEE.

The resistivity ρ_{max} increases by a factor of ~1.6 over the entire range for BLG devices as seen in the inset to Fig. 6.6 (b). Up to the dose of ~4480 μC/cm^2, ρ_{max} of BLG changes only by ~14% compared to ~300-700% in the case of SLG. This difference is reflected by the I(D)/I(G) ratio in the Raman spectra for SLG and BLG.

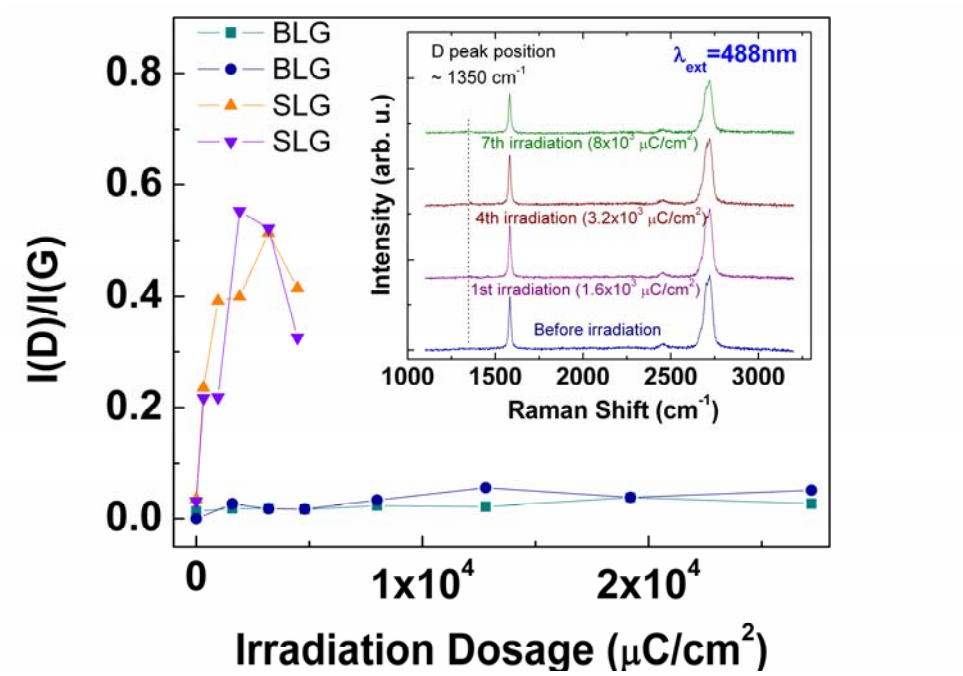

Fig. 6.7. Evolution of Raman spectrum of BLG with increasing irradiation dose. The examined BLG samples do not reveal either a prominent disorder D peak, or D'. The I(D)/I(G) intensity ratio is very small as compared with that in SLG. The data suggest that BLG graphene is much less susceptible to the electron beam irradiation than SLG. Reprinted with permission from G. Liu, D. Teweldebrhan and A.A. Balandin, IEEE Trans. Nanotechnol.., 10, 865 (2011). Copyright (2011) IEEE.

The inset to Fig. 6.7 shows the Raman spectrum of a typical BLG device after several e-beam irradiation steps. Unlike in SLG the disorder induced Raman D peak in BGL does not reveal a pronounced growth with irradiation dose even over a much larger dose range. No detectable D' or D+D' peaks appear in the Raman spectrum of

BLG. The absence of these peaks suggests e-beam irradiation over the examined dose range create limited amount of defects in BLG. Fig. 6.7 shows a comparison of the I(D)/I(G) ratio for two BLG with two SLG devices. The pristine BLG and SLG before irradiation have very small and comparable value of I(D)/I(G). The I(D)/I(G) ratio grows very fast in SLG devices with each irradiation step while it increases very slowly in BLG even over a wider irradiation dose range. This difference of I(D)/I(G) behavior in BLG and SLG is consistent with the different behavior of ρ_{max} in BLG and SLG devices. Similar conclusions were made about the D peak induced by hydrogenation [12, 14]. The authors concluded that it is much harder to induce the disorder D peak in BLG than in SLG [12, 14]. A pronounced D peak in the Raman spectrum of BLG can be induced only using higher dose of e-beam irradiation [11].

Our results suggest that BLG devices can perform better than SLG devices in applications which require radiation hardness. It has to be taken into account that irradiation may not only decrease the carrier mobility and electrical conductivity but also affect the excess noise level in such devices. The low level of 1/*f* noise is essential for the proposed graphene applications in communication systems [15]. It was recently shown that graphene devices reveal a rather low level of 1/*f* noise, but can degrade as a result of aging and environmental exposure, as mentioned in the Chapter 5. The e-beam irradiation may lead to further increase in the noise level in graphene devices. For this reason, special protective cap layers may be required for communication and radiation-hard applications.

From the other side, the e-beam irradiation may lead to a new method of defect engineering of graphene physical properties. The controlled exposure of graphene layers to electron beams can be used to convert certain regions to the highly resistive or electrically insulating areas needed for fabrication of graphene circuits. Irradiation can also be used to reduce the intrinsically high thermal conductivity [16] to the very low values required for the proposed thermoelectric applications of graphene [17]. It is known from the theory of heat conduction in graphene that the lattice thermal conductivity can be strongly reduced by the defects and disorder [18]. The small-dose irradiation can become an effective tool for shifting the position of the minimum conduction point or inducing the carrier "transport gap."

6.3 Summary

We carried out detail investigation of the electrical and Raman spectroscopic characteristics of graphene and bilayer graphene under the e-beam irradiation. It was shown that the SLG is much more susceptible to e-beam irradiation than its bilayer. The appearance of the disorder induced D peak in graphene Raman spectrum suggests that e-beam irradiation induce defects in graphene lattice. The mobility and electrical resistivity of graphene can be varied by the e-beam irradiation over a wide range of values. The obtained results may lead to a new method of defect engineering of graphene properties.

Reference

[1] M.S. Dresselhaus, A. Jorio, A.G. Souza Filho and R. Saito, *Phil. Trans. R. Soc. A*, **368**, 5355 (2010).

[2] A.C. Ferrari and J. Robertson, Saito, *Phil. Trans. R. Soc. A*, **362**, 2477 (2004).

[3] A.C. Ferrari, J.C. Meyer, V. Scardaci, C. Casiraghi, M. Lazzeri, F. Mauri, S. Piscanec, D. Jiang, K.S. Novoselov, S. Roth and A.K. Geim, *Phys. Rev. Lett.*, **97**, 187401 (2006).

[4] I. Calizo, F. Miao, W. Bao, C.N. Lau and A.A. Balandin, *Appl. Phys. Lett.*, **91**, 071913 (2007).

[5] S.A. Solin and A.K. Ramdas, *Phys. Rev. B*, **1**, 1687 (1970).

[6] S.R.P. Silva, G.A.J. Amaratunga, E.K.H. Salje and K.M.Knowles, *J. Mater. Sci.*, **29**, 4962 (1994).

[7] V.Yu. Osipov, A.V. Baranov, V.A. Ermakov, T.L. Makarova, L.F. Chungong, A.I. Shames, K. Takai, T. Enoki, Y. Kaburagi, M. Endo and A.Ya. Vul, *Diam. Relat. Mater.*, **20**, 205 (2011).

[8] Brian W. Smith and David E. Luzzi, *J. of Appl. Phys.*, **90**, 3509 (2001)

[9] K. Mølhave, S. B. Gudnason, A.T. Pedersen, C.H. Clausen, A. Horsewell and P. Bøggild, *Ultramicroscopy*, **108**, 52, (2007).

[10] S. Adam, E.H.Hwang, V.M. Galitski and S.D. Sarma, *Proc. Natl. Acad. Sci.*, vol. **104**, 18392 (2007).

[11] D. Teweldebrhan and A.A. Balandin, *Appl. Phys. Lett.*, **94**, 013101 (2009).

[12] D.C. Elias, R.R. Nair, T.M.G. Mohiuddin, S.V. Morozov, P. Blake, M.P. Halsall, A.C. Ferrari, D.W. Boukhvalov, M.I. Katsnelson, A.K. Geim and K.S. Novoselov, *Science*, **323**, 610 (2009).

[13] Z. Ni, T. Yu, Z. Luo, Y. Wang, L. Liu, C. Wong, J. Miao, W. Huang and Z. Shen, *ACS Nano*, **3**, 569 (2009).

[14] S. Ryu, M.Y. Han, J. Maultzsch, T.F. Heinz, P. Kim, M.L. Steigerwald and L.E. Brus, *Nano Lett.*, **8,** 4597 (2008).

[15] X. Yang, G. Liu, A.A. Balandin and K.Mohanram, *ACS Nano*, **4**, 5532 (2010).

[16] A.A. Balandin, S. Ghosh, W. Bao, I. Calizo, D. Teweldebrhan, F. Miao and C.N. Lau, *Nano Lett.*, **8**, 902 (2008).

[17] P. Wei, W. Bao, Y. Pu, C.N. Lau and J. Shi, *Phys. Rev. Lett.*, **102**, 166808 (2009).

[18] D.L. Nika, E.P. Pokatilov, A.S. Askerov and A.A. Balandin, *Phys. Rev. B*, **79**, 155413 (2009).

Chapter 7

Summary

Graphene, with its extraordinary electrical and thermal properties, attracts tremendous amount of attention among academia and industry ever since its experimental demonstration in 2004. It received physics Nobel Prize in 2010 due to the unique contributions to the understanding of physics in two-dimension world. Moreover, the material itself can be used for practical applications in various aspects, such as high speed electronics, thermal interface material, transparent electrodes, display panel, and so on. The fast development and exploration of the applications of graphene is in part due to its easy material production. Whether from exfoliation from high quality bulk graphite or from simple CVD growth, the good quality of graphene guaranties the electrical properties. Comparing with its sister material, carbon nanotube whose growth method is much complicated yet not providing controllable chirality, graphene can be obtained more uniformly with a better controlled method. However, the history of carbon nanotube since 1990's gives researchers many ideas and inspirations to deal with graphene due to the similarity between them.

The absence of band gap seems to be the biggest obstacle that prevents graphene from being used in digital applications. Although there are several methods of creating band gap such as quantum confinement and using E-field in bilayer graphene, both of them suffer practical problems. The quantum confinement requires graphene

to be cut into nanoribbons with width below 30 nm. However, there is still no crystallography cutting technique can be used to treat graphene. Commonly used oxygen plasma method will leave defective edges that harm the electrical performance of graphene devices. The E-field induced band gap in bilayer graphene is below 100 meV, which is too small if comparing with that of Si, 1.12 eV. Without an appreciable band gap, the graphene device can not be turn off, thus limits its application in digital scenario.

However, for the analog applications, the devices do not necessarily have to be turn off, large transconductance g_m is the key. This is exactly what graphene can offer. Also, the ambipolar transport properties of graphene open up possibilities of simplify the circuitry. We demonstrated the circuit built by a single graphene transistor and a resistor can achieve the functionalities of phase shift keying and frequency shift keying and phase detectors. These modulation and de-modulation functions are widely used in modern communication systems. An important question for analog applications is the low-frequency noise which will inevitably be up-converted to high frequency noise due to the nonlinearity of the circuits and systems. We measured the low-frequency noise in graphene transistors, and found a pretty decent value of noise level with Hooge parameter on the order of 10^{-4} to 10^{-3}. With graded-thickness graphene structure, we are able to reduce the noise contribution from the contact of graphene/metal in single layer graphene device.

Tuning graphene electrical properties such as moving the charge neutrality point is as important as doping effect in silicon technology. With moderate energy electron-beam irradiation, we can shift the charge neutrality point without break the electrical properties of graphene.

Graphene is a promising material for analog electronics, owing to its high carrier mobility and ambipolarity. Considering it has only been studied for less than 10 years, graphene is still in its beginning stage of development. Technical issues such as metal/graphene contact resistance and good saturation are need to be solved in the future research.