Title
An Interleaved 6-Level GaN Bidirectional Converter for Level II Electric Vehicle Charging

ISBN
9781538683309

Authors
Chou, Derek
Fernandez, Kelly
Pilawa-Podgurski, Robert CN

Publication Date
2019-03-21

DOI
10.1109/apec.2019.8721971

Peer reviewed

2019 IEEE Applied Power Electronics Conference and Exposition (APEC), Anaheim, CA, USA

An Interleaved 6-Level GaN Bidirectional Converter for Level II Electric Vehicle Charging

D. Chou
K. Fernandez
R. C. N. Pilawa-Podgurski

Design and Implementation of an Interleaved 6-Level GaN Bidirectional Converter for Level II Electric Vehicle Charging

Derek Chou, Kelly Fernandez, and Robert C. N. Pilawa-Podgurski
Department of Electrical Engineering and Computer Sciences
University of California, Berkeley
Berkeley, CA 94720
derek_chou@berkeley.edu, kefernandez@berkeley.edu, pilawa@berkeley.edu

***Abstract*—On-board battery chargers are a key component of electric vehicles of all types. Conventionally, they may be used to recharge a vehicle's battery pack, but as they are connected to the grid, they can be used to provide ancillary grid services, such as reactive power support and longer-term battery-to-grid backup. On-board chargers also represent a potentially significant portion of a vehicle's weight and can take up considerable volume. This paper discusses the design and implementation of a high power density Level II charger converting between 400 V_{DC} and 240 V_{AC}, utilizing two interleaved flying-capacitor multilevel converter stages combined with a full H-bridge unfolder or active rectifier. Experimental results show a peak system efficiency of 98.9%, a power output of 6.6 kW, and an effective switching frequency at the inductor switch nodes of 720 kHz.**

I. Introduction

MARKET penetration of electric vehicles has increased markedly in the past decade. However, battery electric vehicles continue to face such challenges as range anxiety from the public, combined with long charging times. Improving such metrics requires infrastructure upgrades as well as more powerful battery charging management systems [**?**]. Electric vehicle charging requires hours of time to recover used range, compared with conventional gasoline-powered vehicles, which require minutes of time to refuel [**?**], [**?**], [**?**], [**?**]. Therefore, it is desirable for electric vehicle chargers to handle higher charging power levels, to minimize battery charge times. This must be balanced with keeping charging hardware volume and weight to a minimum, as such energy conversion systems interfacing between grid ac and battery dc voltages are carried on-board for Level I or Level II charging power levels. Electric vehicle batteries may additionally be viewed as a mobile battery backup source for the grid [**?**], [**?**], [**?**].

Conventional approaches to constructing the ac–dc stage for power conversion between grid ac and battery dc voltages encounter the problem of requiring large filter inductors and capacitors for the power factor correction (PFC), for ac–dc conversion, or inverter stage, for dc–ac conversion. A possible solution to this issue involves increasing the switching frequency of the active devices in the converter to reduce passive component sizes, but this reduces overall system efficiency and increases thermal management requirements. It has been shown that the flying capacitor multilevel (FCML) topology has the potential to dramatically reduce passive component volume and weight in inverter applications [**?**], [**?**], [**?**]. This work utilizes a system-level design approach to improve gravimetric and volumetric power density figures of a Level II bidirectional electric vehicle charger. We note that for single-phase ac-dc converters, twice-line frequency energy buffering is another important consideration, but is not the focus of this work. Likewise, power factor correction (PFC) control, grid synchronization, and other high-level control considerations are not the focus of this work, but may be implemented on the hardware developed here. Table I details sample design criteria generated for the purposes of this system platform design.

The remainder of this paper is organized as follows: Section II presents the overall system topology design and operational principles. Section III describes the hardware design and implementation of the system described in the previous section and Section IV discusses experimental results taken from the hardware prototype. Section V provides concluding remarks.

TABLE I: Level II charger design specifications.

Parameter	Notes	Value
DC Voltage	Nominal	400 V_{DC}
AC Voltage	Nominal	240 V_{AC}
Power Processed	Max	6.6 kW
Ambient Temperature	Max	60°C
Physical Location		Under passenger seat

II. Principles of Operation

The hardware platform presented in this work is an interleaved implementation of the FCML converter topology, connected to a full H-bridge active rectifier or unfolder stage. Fig. 1 is a schematic of the core power conversion stage design. To operate the system as an inverter, the FCML dc–dc conversion stage generates a rectified sine wave at the switch node, which is filtered by the inductors, and then converted to a full sine wave by the full H-bridge unfolder. The interleaving operation of the FCML converter portion reduces voltage ripple at the rectified sine wave node, V_{rec}. To operate the system as a rectifier, the H-bridge acts as an active rectifier, and the FCML dc–dc conversion stage steps up the rectified sine wave voltage to the dc bus voltage.

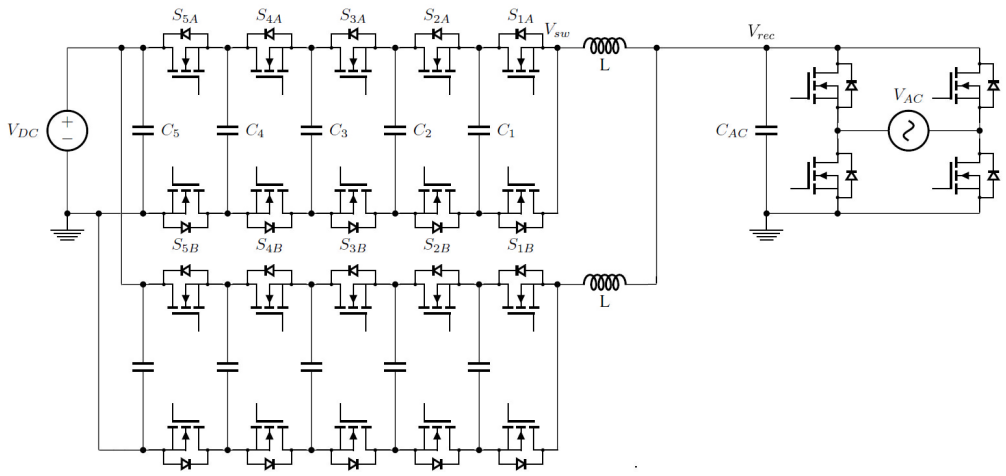

Fig. 1: 6-level interleaved FCML schematic with unfolder / active rectifier.

A. Multilevel DC-DC Conversion

The flying capacitor multilevel topology uses a combination of capacitors and inductors to transfer energy. A major advantage of this topology leveraged in this work is its ability to generate high effective switching frequency waveforms at the filter inductor switch-node (V_{sw}, Fig. 1). Detailed operational principles for the FCML converter topology can be found in [**?**], [**?**], and [**?**].

This work utilizes two interleaved 6-level FCML power stages. To illustrate the operation of a single FCML power stage, switching signals and voltage nodes of interest are shown in Fig. 2, for an example single 6-level FCML converter operating at 70% duty ratio. Switch control and capacitor balancing are achieved through usage of the PSPWM method as described in [**?**], [**?**] and [**?**]. The 6-level topology was chosen for its inherent natural capacitor voltage balancing effect [**?**]. Of note is the frequency multiplication effect inherent to the FCML topology, where the frequency, f_{ind}, seen by the inductor switch-node, V_{sw}, is:

$$f_{ind} = f_{sw} \cdot (N-1) \tag{1}$$

where N is the number of voltage levels in the FCML converter and f_{sw} is the individual switch switching frequency. In a 6-level FCML converter, the frequency seen by the inductor is 5× the base switching frequency. Moreover, the inductors experience a maximum ripple voltage of the smallest voltage across the flying capacitors, $V_{DC}/(N-1)$. This results in an overall $(N-1)^2$ reduction in filtering inductor size, as compared to a conventional two-switch non-isolated converter design ($N = 2$) [**?**]. For a 6-level FCML converter, this is a 25× decrease in the filter inductor size requirement for the same base switching frequency.

To achieve interleaving operations, the switching signals for each of the FCML stages are phase-shifted by 180 degrees, such that the output current waveforms of the two inductors in the system are largely equal and opposing, resulting in a current waveform at the H-bridge section (V_{rec}, Fig. 1) with very low ripple. Even though the interleaved stages may not be perfectly matched for current sharing, since they are constructed with the same components, the benefits of lower current ripple due to interleaved operation are still generally achieved. In this work, only the effects of natural current sharing between stages are explored; interleaved stage balancing, load shedding at light-load operating points, and other more advanced techniques may be implemented in software.

The FCML topology utilizes capacitors to block dc voltages, and the switches see only a fraction of the input voltage:

$$V_{switch} = \frac{V_{DC}}{N-1} \tag{2}$$

Since lower-voltage switching devices tend to have a more favorable figure of merit, the product of gate charge by on-state resistance, the overall efficiency of the system can be improved through selection of such devices. The combination of frequency multiplication effects and increased design space for switching devices allows for some design versatility: the more-favorable figure-of-merit may be leveraged in the way of extreme reduction of filtering capacitors and inductors through high-frequency switching [**?**], or it may be optimized to provide a balance between switching and conduction losses. In this work, EPC2033 GaN devices are selected to provide a balance between switching and conduction losses [**?**].

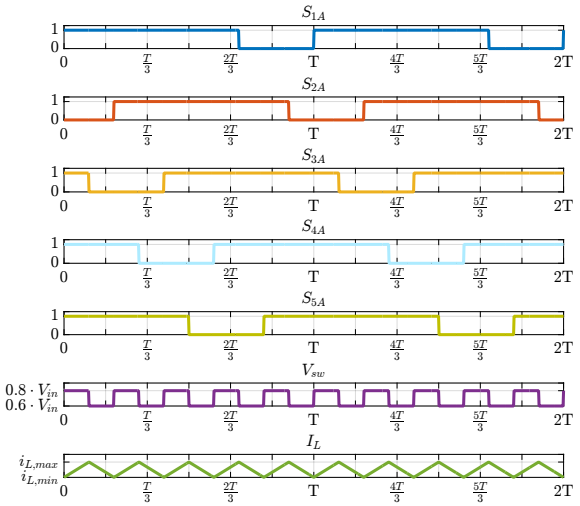

Fig. 2: 6-level FCML control waveforms

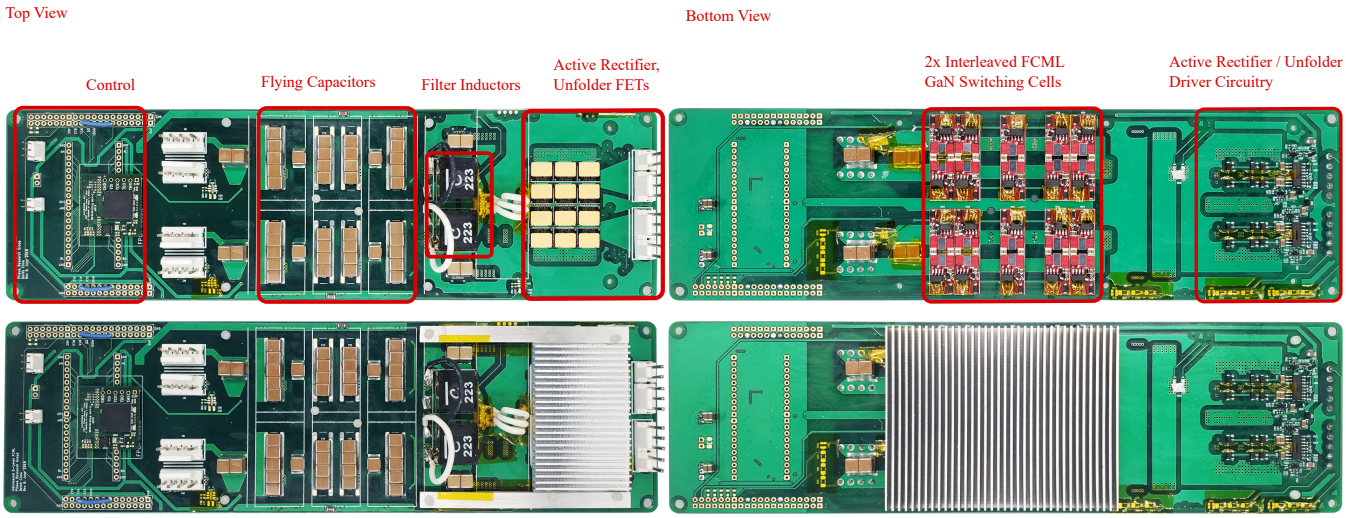

Fig. 3: Converter prototype photograph

III. Hardware Design and Implementation

The hardware prototype has been designed, constructed and tested, using the guidelines set forth in Table I. Figure 3 shows the converter as built, including the control, interleaved FCML, and active rectifier / unfolder stages. Table II shows the major components selected for usage in the converter prototype.

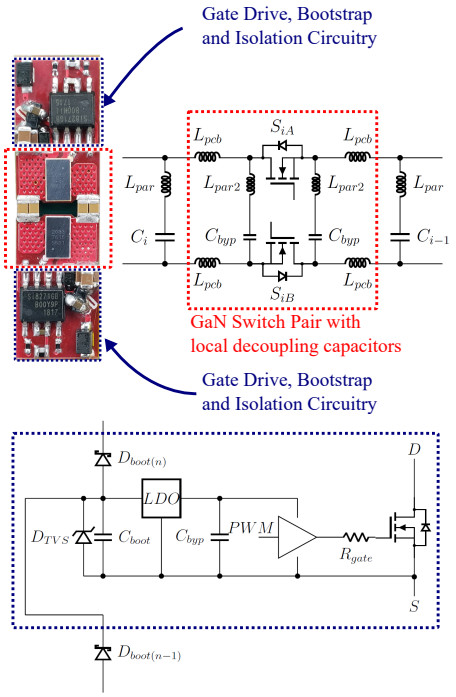

Fig. 4: GaN switching cell daughterboard pair design and schematics.

The main power devices in the FCML stage are EPC 2033 GaN FETs, driven by Silicon Labs Si8271 single-channel isolated gate drivers. To address the challenge of supplying a floating gate drive voltage to each GaN FET, several solutions may be used. In this work, individual gate drive power supplies are achieved through cascaded bootstrap stages with low-dropout (LDO) regulators attached to each bootstrap capacitor to provide a stable drive voltage to each FET (Fig. 4). Reverse conduction of the GaN devices can cause the bootstrap capacitors to be charged to a voltage higher than the input logic voltage. An ESD protection diode rated for 12 V standoff voltage and 13.5 V breakdown voltage is placed in parallel with the bootstrap capacitors of each stage, to protect the LDOs from any overvoltage conditions during higher-current operations of the converter. To ensure that the highest-side FET gets at least 5 V of gate drive voltage, the lowest-side gate driver bootstrap capacitor is fed 12 V of gate drive voltage, which is then regulated down to the 5 V gate drive voltage via an LDO. For each cascaded bootstrap stage, there is a small diode drop from the bootstrap diode, resulting in a voltage of about 6.1 V at the highest-side bootstrap capacitor. The method outlined here achieves a 40+% gate drive supply efficiency, which outperforms a similar solution using small isolated dc-dc converters, the ADuM5010, which would achieve less than 27% gate drive supply efficiency [**?**]. Reducing the gate drive voltage margin, or using small step-down switching converters can improve the gate drive supply efficiency, but is not explored further in this work.

The FCML portion of the converter is two individual 6-level FCML converters, interleaved to reduce ripple at the converter rectified sine wave node. In the FCML converter topology, there are many repeating switch pairs. Therefore, the gate driving, isolation, and bootstrap circuitry are built on a GaN "switching cell" daughterboard (Fig. 4), containing a switch unit, local bypass capacitors, and bootstrap capacitors. This has the advantage of breaking up a large converter into a construction of many smaller switch units, with the additional benefit of reducing parasitic ringing effects through the local bypass capacitors. These smaller capacitors are connected in parallel with the larger flying capacitors on the opposite side of the larger circuit board. Since the local bypass capacitors are physically very close to the switch pairs, the value of L_{par2} is less than the combination of L_{par} and L_{pcb}, reducing switch voltage overshoot during commutation [**?**], [**?**].

In the active rectifier / unfolder H-bridge stage, each of the switches is three GaN Systems GS66516T GaN FETs in parallel, designed to handle the high currents that are switched by the active rectifier / unfolder stage. Compared to a conventional silicon MOSFET implementation, the GaN Systems GS66516T 650 V, 25 mΩ GaN FETs have a significantly lower $R_{DS,on}$ for the same volume, and therefore increases the power density of this stage. For comparison, an Infineon IPT65R033G7 650 V, 33 mΩ silicon MOSFET is over 5× the volume of the GaN Systems FET [**?**], [**?**]. Gate driving power requirements are also reduced, as the gate charge of the GaN FETs is only 12.1 nC per device, compared to 110 nC per device for the silicon device. Silicon Labs Si8274 dual-channel complementary isolated gate drivers are used to drive the power switches, and a conventional bootstrap stage is used to power the high-side gate drivers and FETs. Deadtime between the H-bridge legs is generated by the Si8274 gate driver chip.

The frequency multiplication and voltage division effect of the FCML topology is evident in the size of the passive components selected for use in the system. The GaN FETs in the FCML power stage are switched at 144 kHz, resulting in a 720 kHz ripple frequency at the filter inductor. Each flying capacitor is five 2.2 μF capacitors in parallel, and a single 22 μH inductor per FCML stage is used.

Due to the expected losses of the main FCML power stage – over 5 W per device – custom heatsinks were designed for the power stage components. Simulations were done with SolidWorks thermal and flow simulation tools, as well as ANSYS, to calibrate heatsink performance. To stay within the manufacturer recommended pressure of 30 PSI per EPC GaN device [**?**], heatsink standoffs were milled to precise tolerances such that a gap filler material (Alphacool Eisschicht 17 W/mK, 1 mm thickness) would be compressed by ∼15% when fully interfaced [**?**]. Figure 5 shows the stackup of the thermal interfaces between the FCML GaN devices and heatsink. The unfolder stage utilizes GaN Systems GS66516T top-cooled GaN FETs, and has a similar stackup, but the devices are

soldered directly to the main PCB, and so do not require a daughterboard PCB.

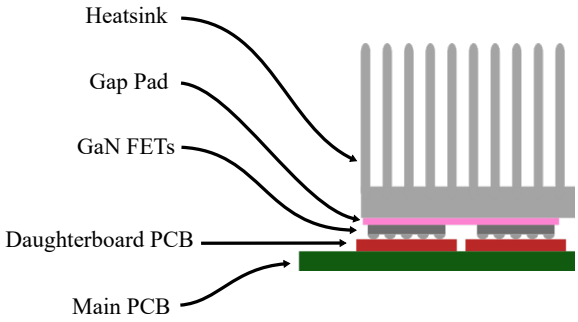

Fig. 5: Diagram of stackup for heatsink interface.

Control of this converter is achieved with an Altera MAX10 series FPGA, which generates all of the interleaved complementary FCML PSPWM control signals with deadtime, as well as the unfolder / active rectifier H-bridge control signals. The PSPWM method combined with the 6-level FCML architecture achieves good natural flying capacitor voltage balancing [**?**], [**?**], [**?**]. To verify power stage operations, this work utilizes the system as an inverter, converting from 400 V_{DC} to 240 V_{AC}. The board design also includes provisions for attaching further control systems, such as a microcontroller, to interface with the FPGA.

TABLE II: Component listing

Component	Part No.	Parameters
Interleaved 6-Level FCML		
GaN FETs	EPC 2033	150 V, 7 $m\Omega$
Isolated Gate Drivers	Si8271GB-IS	Silicon Labs Si827x Series
Flying Capacitors	TDK C5750X6S225K250KA	2.2 μF $\times$ 5 (parallel)
Inductors	Coilcraft XAL1510-223	22 μH
Active Rectifier / Unfolder		
GaN FETs	GaN Systems GS66516T	650 V, 25 $m\Omega\times$ 3 (parallel)
Isolated Gate Drivers	Si8274GB1-IS1	Silicon Labs Si827x Series
Control		
FPGA	Altera 10M16SCU169C8G	MAX10 Series

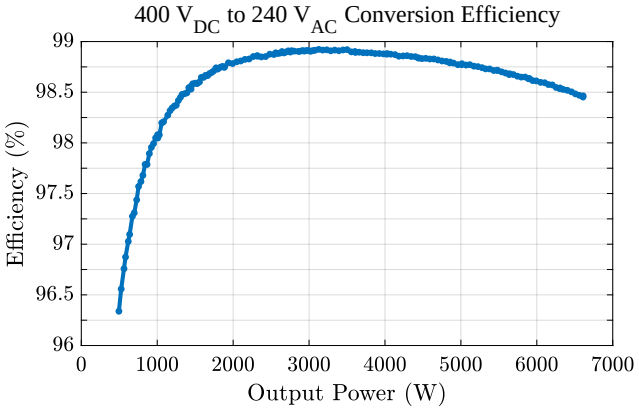

Fig. 6: Converter efficiency plot, with heatsink, up to 6.6 kW, including all control and gate driving losses.

IV. Experimental Results

The full system has been tested to a power processing capability of 6.6 kW, converting from 400 V_{DC} to 240 V_{AC}. Table III details the performance of the converter as measured. The converter achieves a volumetric power stage density of 739 W/in^3 and a gravimetric power density of 23.5 kW/kg. Since the maximum height of the converter is dictated by the heatsinks and the inductors, and the component volume is much smaller than the volume bounded by the maximum component dimensions in each direction, the power density figure is calculated using the composite volume of a prism bounding the FCML stage, a prism bounding the inductors, and a prism bounding the unfolder stage. Figure 6 shows the efficiency of the system; with liberal airflow ($\sim$150 CFM) and with heatsinks on the main power devices. The system achieves a peak efficiency of 98.9%, including all control and gate driving losses. During testing, the heatsinks remained below 85 °C, which is within the rated temperature of most commercial electronic parts.

Figure 7 shows the multi-level voltage output at the switch-node, V_{sw} in Fig. 1. The output THD is less than 1%: the inductors see a ripple frequency of 720 kHz with stepped voltages a fraction of the input voltage, and the ripple currents are interleaved to reduce output current and voltage ripple harmonics. Figure 8 shows the measured interleaving operations of the converter system. Note that the output currents between phases are not perfectly balanced, but are roughly equivalent and thus largely cancel out, as seen in Fig. 9. Further control may be applied to balance the loads between phases, but most of the benefits of interleaving are achieved from the naïve control method of simply applying the same control signals to each of the phase legs, phase-shifted by 180 degrees.

TABLE III: Key Performance Specifications

Parameter	Value	Notes
DC Voltage	400 V_{DC}	Tested
AC Voltage	240 V_{AC}	Tested
AC Current	28 A	Tested
AC Power	6.6 kW	Tested
Efficiency	98.9%	Peak Efficiency
	98.5%	Full Power
THD	$\leq$ 1%	Tested
Switching Frequency	144 kHz	Per Switch
Effective Frequency	720 kHz	At Inductor
Weight	280 g	Incl. heatsink
Dimensions	10.3" x 3.05" x 0.535" (26.16 cm x 7.75 cm x 1.36 cm)	Excl. heatsink
Volume	16.8 in^3 (275.42 cm^3)	Excl. heatsink
Volume	27.5 in^3 (450.64 cm^3)	Incl. heatsink
Power Stage Volume	8.93 in^3 (146.4 cm^3)	Incl. heatsink
Volumetric Power Density	739 W/in^3 (45.1 W/cm^3)	Power stage & heatsink
Gravimetric Power Density	23.5 kW/kg	Incl. heatsink

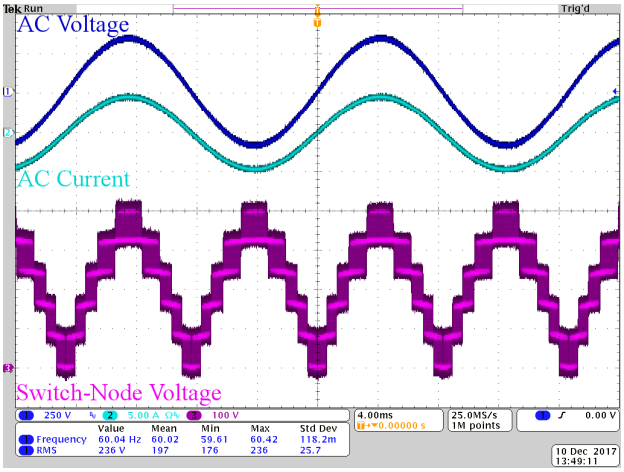

Fig. 7: Typical oscilloscope traces of AC voltage and current as related to the FCML switch-node voltage waveform.

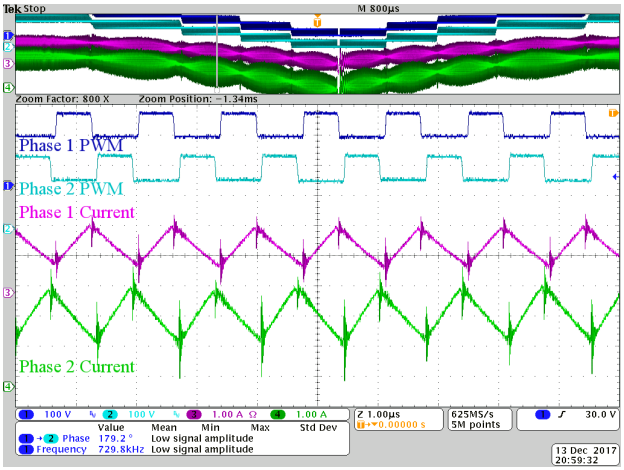

Fig. 8: FCML interleaving operations, showing interleaved signals.

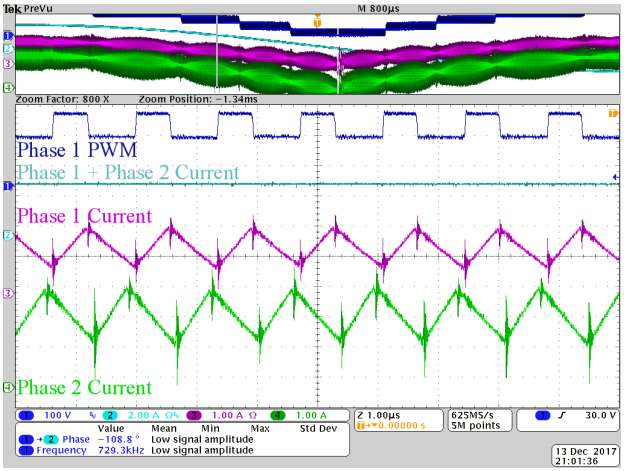

Fig. 9: FCML interleaving operations, showing current waveform canceling.

V. Conclusions and Future Work

This work demonstrates the power stage for a Level II charger converter platform with excellent power density figures, realized through an interleaved FCML power stage connected to an active rectifier / unfolder stage, both utilizing GaN technology. Control is achieved with an FPGA which generates all of the phase-shifted PWM (PSPWM) and H-bridge output signals. A hardware prototype has been implemented, achieving a full system efficiency of 98.9%, a power processing capability of 6.6 kW, and an effective inductor frequency of 720 kHz. A gravimetric power density of 23.5 kW/kg is achieved, and a volumetric power density of 739 W/in^3 is achieved.