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Bonding of Si chips to low carbon steel boards using electroplated Sn solder

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Abstract

Purpose – The purpose of this research was to develop a new process to bond silicon (Si) chips to low carbon steel substrates using pure tin (Sn) without any flux.

Design/methodology/approach – Iron (Fe) substrates were first electroplated with a Sn layer, followed by a thin silver (Ag) layer that inhibits Sn oxidation thereafter. It is this Ag capping layer that makes the fluxless feature possible. Fluxless processes are more environmentally friendly and more likely to produce joints without voids. The Si chips were deposited with Cr/Au dual layer structure. The bonding process was performed at 240°C in vacuum. The Sn joint thickness was controlled by spacers during the bonding. Scanning electron microscopy images on cross sections exhibited quality joints without visible voids. Energy dispersive X-ray spectroscopy analysis was used to detect joint compositions.

Findings – It was revealed that the Sn layer was bonded to a Si chip at the Cr–Sn interface and to the Fe substrate by forming an FeSn₂ intermetallic compound (IMC). The IMC is only 1.1 to 1.5 μm in thickness. Thin IMC is highly preferred because IMC deforms a little in accommodating the coefficient of thermal expansion (CTE) mismatch between Si and Fe. Shear test results showed that the fracture forces of the samples passed the military criteria by a wide margin.

Originality/value – This new fluxless bonding process on Fe should make Fe or low carbon steel a more likely choice of materials in optical modules and electronic packages.

Keywords Solder, Carbon steel

Paper type Research paper

1. Introduction

Ferrous metals are widely used for various applications in optical modules and electronic packaging. For example, iron (Fe) substrates or platforms are important, in particular, in optical applications as a mini-bench to mount small optical components. In addition, the Invar alloy (Fe–36Ni) noted for its uniquely low coefficient of thermal expansion (CTE) of around 0.8 to 1.6 ppm/°C has been utilized in manufacturing precision instruments where high dimensional stability is required. Alloy 42 (Fe–42Ni) and Kovar (Fe–29Ni–17Co) are controlled expansion alloys with CTE of 4.0–4.7 ppm/°C and 5.1–5.5 ppm/°C, respectively (Alam and Chan, 2005; ASM Handbook, 1990a). These controlled expansion alloys have been used as lead-frames of plastic packages and headers of transistors because their CTEs are close to that of Si (3 ppm/°C) and lead-sealing glass. But, one disadvantage of these alloys is their relatively low thermal conductivity (10–17 W/m-K) (ASM Handbook, 1990b).

We, therefore, searched for ferrous metals that have higher thermal conductivity and relatively low CTE for electronic and optical packaging applications. After a thorough research, AISI

1018 low carbon steel (Fe) was selected for study. The thermal conductivity is 51.9 W/m-K and CTE is 11.5 ppm/°C (Briand *et al.*, 2004). It also has very high tensile strength (635–696 MPa) and high melting point (1450–1540°C). In our previous research, we have shown that silicon (Si) chips can be bonded to low carbon steel substrates coated with nickel (Ni) as a buffer layer (Edfagan, 2018). The choice of Ni stems from the fact that Ni has been shown to have a slow rate of reaction with tin (Sn) (Frankenthal and Loginow, 1960; Hall, 1991; Hida and Kajihara, 2012). In that study, Ni₃Sn₄ intermetallic compound (IMC) was observed, and its thickness ranges from 5.1 to 8.5 μm as reflow time went from 200 to 300 s. The rate of Ni₃Sn₄ growth in the Ni/Sn binary system is not as slow as expected (Hsu and Lee, 2013). We, thus, embarked on finding an alternative design and came up with an idea of utilizing an Sn/Fe binary system for bonding without adding the Ni buffer layer. Based on the Sn-Fe binary phase diagram (Hsu *et al.*, 2014), FeSn and FeSn₂ are two stable IMCs at room temperature. However, studies on interfacial reactions between Fe and Sn-based alloys have shown that FeSn₂ is the only IMC observed at the interface (Kim *et al.*, 1999; Shen *et al.*, 2009). We, therefore, decided to study the feasibility of using an Sn/Fe binary system for bonding Si chips to Fe substrates to reduce the IMC thickness.

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At present, nearly all solders used in electronics are Sn-based with a few percentages of silver (Ag) and copper (Cu). They are referred to as lead-free solders. Other die-attach materials include lead-tin solders, gold-tin eutectic alloy and Ag epoxies. In this paper, we report the results of bonding Si chips to Fe substrates using pure Sn solder. In the initial study, to make the reactions more straightforward to analyze, pure Sn solder instead of Sn-based lead-free solders was chosen. The bonding process developed was entirely fluxless; that is, no flux was ever used. The fluxless process eliminates voids in the joints, thus improving joint quality and heat conduction. After the samples were bonded, the quality and microstructure of the joints were examined using scanning electron microscopy (SEM). The composition of the joints was studied with energy dispersive X-ray spectroscopy (EDX). The joint strength was measured by a shear test. In what follows, we first present the experimental design and procedures. Experimental results are then reported and discussed. Finally, a short summary is given.

2. Experimental design and procedures

Substrates of $15 \times 13 \times 3.3$ mm (width \times length \times thickness) were cut from AISI 1018 low carbon steel sheet. Substrates were ground using 800 and 1,200 grit SiC-coated papers to smooth the surface out and cleaned with acetone and deionized water before electroplating. Next, 70- or 50- μ m Sn was electroplated on the Fe substrates in a stannous bath under the condition of 43°C and pH 1 with current density of 30 mA/cm², followed by the electroplating of thin layer Ag of 100 nm in thickness over Sn as a capping layer to prevent Sn from oxidation. To make the Si chips ready for bonding, two-inch n-type (100) orientation Si wafers were deposited with 30 nm chromium (Cr) followed by 100 nm gold (Au) layers using E-beam evaporation. The Cr layer acts as an adhesion layer, and the Au layer acts as the capping layer that protects the Cr layer from oxidation when exposed to air. The wafers were then diced into 5×10 mm chips.

Figure 1(a) depicts the structure design of the bonding system. The Si chip and Fe substrate were held together with 50- or 30- μ m-thick spacers placed between them. To make room for the spacers, only 5×5 mm area on the Fe substrate was plated with Sn. The assembly was mounted on a heater graphite platform in a chamber with a 16 psi pressure applied on the Si chip to ensure contact. The chamber was pumped down to 80 millitorrs, and the graphite platform was then heated. The bonding process was conducted at 240°C with reflow time of 300 s. After bonding, the heater was turned off, and the assembly was allowed to cool down naturally to room temperature in vacuum environment. For SEM examination, the samples were mounted in epoxy, sectioned using a slow speed diamond saw, ground with 800 and 1,200 grit SiC paper

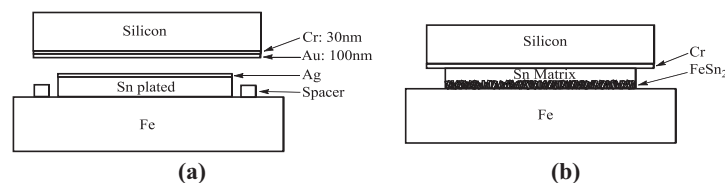


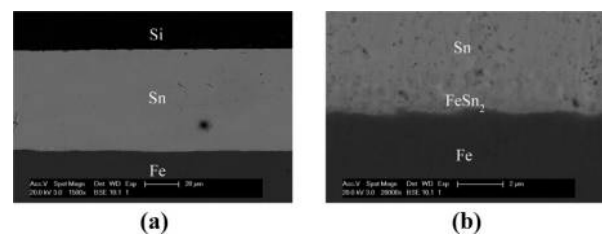
Figure 1 Schematics illustrating (a) bonding structure and configuration and (b) layer structure after bonding

and polished with alumina suspension solution. The microstructures were examined by an SEM equipped with a back-scattered electron image detector. The chemical compositions were analyzed using EDX spectroscopy. A Nordson Dage 4000 shear tester was used for the shear test with a shear speed of 500 μ m/s, and a shear height of 100 μ m was used to evaluate the shear strength of five bonded samples. Fracture modes were studied following the shear test.

3. Experimental results and discussion

The fluidic nature of molten Sn during the bonding process makes the consistent control of joint thickness difficult. Uneven application of pressure in the bonding process could make the Si chip to incline toward an arbitrary direction, resulting in joint thicknesses variation within the sample. To control the joint thickness, spacers of 50- and 30- μ m thicknesses were used. Figure 1(b) displays the layer structure after bonding. The thin Au layer on Si/Cr and thin Ag layer on Sn were both dissolved at 240°C and eventually distributed in the Sn matrix after cooling down to an ambient temperature. Figure 2 shows the cross-section SEM images of the bonded sample using a 50- μ m spacer. The Si chip is well bonded to the Fe substrate. No visible voids are seen across the entire joint cross section because of absence of flux. The Si/Cr–Sn interface is free from IMC formation. The interfacial bond is achieved between Sn and the Cr layer on the Si chip. On the other hand, it is observed that the IMC layer of around 1.5- μ m thickness was formed at the Sn–Fe interface. EDX analysis identified the chemical composition of IMC as FeSn₂, which is similar to the results in the studies on interfacial reactions between Fe and Sn-based alloys (Kim *et al.*, 1999; Shen *et al.*, 2009). This FeSn₂ layer is much thinner than the 8.5- μ m Ni₃Sn₄ formed between Sn and Ni under the same bonding conditions (Edfagan, 2018). Sn thickness is about 60 μ m, which is larger than the spacer thickness. This may be ascribed to the improper setting during the bonding process.

Figure 2 Cross-section SEM images of the sample using 50- μ m spacers at (a) lower magnification (1,500 \times) and (b) higher magnification (20,000 \times) showing the Sn–Fe interface



Theoretically, the possibility of solder joint breakage caused by CTE mismatch could be evaluated by the maximum shear strain. In this model, both Si chip and Fe substrate are assumed to be able to be free to contract during cooling down. This maximum shear strain is calculated by the well-known equation (White and Okamoto, 1992):

$$\gamma = \frac{(\alpha_1 - \alpha_2)(T_2 - T_1)L}{2h} \quad (1)$$

where α_1 and α_2 are the CTE of silicon chip and low carbon steel, respectively, T_2 is the solidifying or the bonding temperature, T_1 is the room temperature, L is the diagonal length of the Si chip and h is the thickness of the joint. For a joint thickness of $60 \mu\text{m}$, the maximum shear strain is 0.10. Figure 2 shows that the joint has no cracks at the bonding interfaces. The samples did not break despite the large CTE mismatch. These observations indicate that the bonded structure is strong enough to sustain the stress developed due to the CTE mismatch.

Exhibited in Figure 3 are the cross-section SEM images of the bonded sample using a $30\text{-}\mu\text{m}$ spacer. The Si chip is also well bonded to the Fe substrate. The Sn thickness is about $30 \mu\text{m}$, close to the thickness of the spacer. The IMC thickness is only about $1.1 \mu\text{m}$. The chemical composition of the IMC was also confirmed as FeSn_2 by EDX. The calculated maximum shear strain is 0.21. This means that the $30\text{-}\mu\text{m}$ joint can also accommodate the thermal stress caused by the CTE mismatch, although the calculated maximum shear strain is twice that of the $60\text{-}\mu\text{m}$ joint.

Shear tests were performed using a Nordson Dage 4000 shear tester on five samples bonded with $30\text{-}\mu\text{m}$ spacers. The measured fracture force ranges from 5.0 to 23.5 kg, as listed in Table I. Even though the chip size is $5 \times 10 \text{ mm}$, only $5 \times 5 \text{ mm}$ of area was bonded, as explained in Section 2. For a bonding area of 0.25 cm^2 , according to MIL-STD-883H method 2019.8, the passing fracture force is 2.5 kg. Thus, all five samples tested passed this military criterion with a wide margin. Sample 2 shows the lowest fracture force (5 kg), and Sample 4 exhibits the highest fracture force (23.5 kg). Next, the fracture modes were evaluated. Figure 4 displays SEM micrographs on the Fe substrate of Samples 2 and 4. The EDX results are provided in Tables II and III. In Figure 4(a), it is seen that the compositions on five locations shown in Table II are all 100 per cent Sn. This means that the joint broke at the Cr–Sn interface, as portrayed in Figure 5. The morphology revealed on the Cr–Sn interface suggests that this interface is only partly bonded because of contaminations on the Si chip

Figure 3 Cross-section SEM images of the sample using $30 \mu\text{m}$ spacers at (a) lower magnification ($3,500\times$) and (b) higher magnification ($20,000\times$) showing the Sn–Fe interface

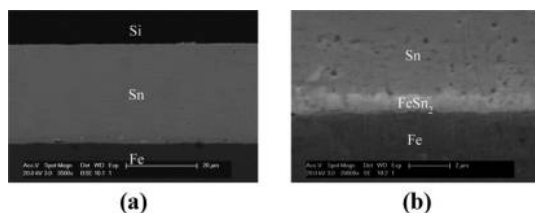


Table I Fracture forces and shear strengths of the six samples bonded using a $30\text{-}\mu\text{m}$ spacer after the shear tests

Sample	Fracture force (kg)	Shear strength	
		(MPa)	(psi)
1	8.6	3.4	496
2	5.0	2.0	285
3	10.7	4.3	682
4	23.5	9.4	1,362
5	8.0	3.2	461

Figure 4 SEM images on the Fe substrate of (a) Sample 2 and (b) Sample 4 after the Si chip was sheared off during the shear test. The chemical compositions of the marked regions are shown in Tables II and III, respectively

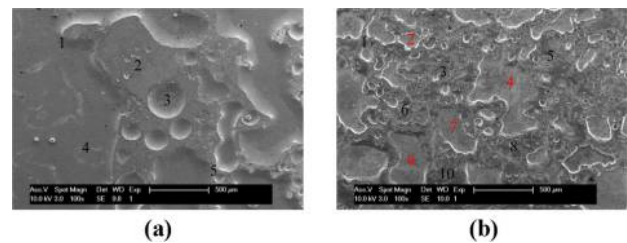


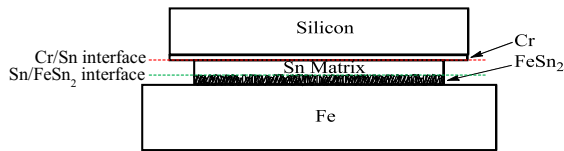
Table II EDX analysis data of five regions marked as 1, 2, 3, 4 and 5, as shown in Figure 4(a)

Region	Composition (At.%)	
	Fe	Sn
1	0	100
2	0	100
3	0	100
4	0	100
5	0	100

Table III EDX analysis data of ten regions marked from 1 to 10, as shown in Figure 4(b)

Region	Composition (At.%)	
	Fe	Sn
1	0	100
2	23	77
3	0	100
4	25	75
5	0	100
6	0	100
7	28	72
8	0	100
9	28	72
10	0	100

Figure 5 Schematics illustrating two fracture interfaces: Cr–Sn and Sn–FeSn₂



prior to bonding. We wish to point out that these samples were made in a typical laboratory environment, and thus, contaminations are likely. On Figure 4(b) of Sample 4, the compositions on six of the ten EDX locations are 100 per cent Sn. The four other locations show compositions of 25 per cent Fe and 75 per cent Sn in average. Each location is within a flat-bottom cavity. We can, thus, confer that on the cavity-like regions, the joint broke on the Sn/FeSn₂, as depicted in Figure 5. On the other regions, the joint broke on the Cr–Sn interface. The fracture mode of Sample 4 is thus mixed and results in the largest fracture force. In production environment, the contaminations can be reduced well. The fracture force of samples produced should exceed that of Sample 4, i.e. 23.5 kg.

4. Summary

In this research, we developed a fluxless process to bond Si chips to low carbon steel, or Fe, substrates, using electroplated Sn solder. The process is entirely fluxless; that is, no flux was ever used. Fe substrates were electroplated with 70 μm Sn, followed by 100 nm layer of Ag. This capping Ag layer protects the Sn layer from oxidation, making fluxless possible. Fluxless feature is important in preventing voids in the joints, particularly for bonding large chips. It is also more environmentally friendly. Si chips were deposited with 30 nm Cr and 100 nm Au layers using E-beam evaporation in a high vacuum environment. The Si chip was placed over the Fe substrate and bonded at 240°C using 50- μm -thick spacers to control joint thickness. In another design, 30- μm spacers were used. SEM images on the joint cross sections exhibit uniform thickness without visible voids. A thin IMC layer between the Sn and Fe substrate was observed. EDX results confirmed the IMC to be FeSn₂. The FeSn₂ layer is very thin, that is, 1.1–1.5 μm . Thin IMC is highly preferred in solder joints because IMCs are mostly brittle. Shear test results certified that the fracture forces of the samples exceeded the criterion in MIL-STD-883H, method 2019.8, by a wide margin. This process presents a new process to bond Si chips to Fe substrates without using any flux, thus expanding the choice of electronic and optical packaging and substrate materials to Fe which has

many advantages including low cost, high strength, relatively high thermal conductivity, low CTE among metals and ease for machining, forging and heat treatment.

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