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Influence of plasma-based *in-situ* surface cleaning procedures on HfO₂/In_{0.53}Ga_{0.47}As gate stack properties

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We report on the influence of variations in the process parameters of an *in-situ* surface cleaning procedure, consisting of alternating cycles of nitrogen plasma and trimethylaluminum dosing, on the interface trap density of highly scaled HfO₂ gate dielectrics deposited on *n*-In_{0.53}Ga_{0.47}As by atomic layer deposition. We discuss the interface chemistry of stacks resulting from the pre-deposition exposure to nitrogen plasma/trimethylaluminum cycles. Measurements of interface trap densities, interface chemistry, and surface morphology show that variations in the cleaning process have a large effect on nucleation and surface coverage, which in turn are crucial for achieving low interface state densities. © 2013 AIP Publishing LLC. [<http://dx.doi.org/10.1063/1.4825259>]

INTRODUCTION

In_{0.53}Ga_{0.47}As is currently being investigated as a channel material for III-V metal-oxide-semiconductor field effect transistors for post-Si complementary metal-oxide-semiconductor (CMOS) applications. To reduce the large trap densities at interfaces between In_{0.53}Ga_{0.47}As and the gate dielectric (typically Al₂O₃ or HfO₂), various surface preparation and passivation methods are currently being investigated.^{1–9} Interface trap densities (D_{it}), at least around midgap, are relatively straight-forward to detect for In_{0.53}Ga_{0.47}As, because of its narrow band gap (0.75 eV (Ref. 10)); they cause, for example, a frequency-dependent hump in the depletion region of capacitance-voltage (CV) characteristics,^{11,12} and peaks in normalized conductance maps.¹³ Recently, we have reported on an *in-situ*, cyclic nitrogen plasma/trimethylaluminum (TMA) surface treatment prior to atomic layer deposition (ALD) of gate dielectrics on In_{0.53}Ga_{0.47}As. We showed that this process results in significantly reduced D_{it} of metal-oxide-semiconductor capacitors (MOSCAPs), while at the same time allowing for scaling of accumulation capacitance densities to greater than 2 μF/cm² for both HfO₂ and HfO₂/Al₂O₃ gate stacks.¹⁴ For further scaling and D_{it} reduction, it is important to understand the mechanisms by which surface treatments control the gate stack properties. Towards this goal, we report here on comparisons of different implementations of this surface treatment process, and how these correlate with D_{it} , interface chemistry and surface morphology. We show that details of the surface treatment critically influence uniformity and surface coverage.

EXPERIMENTAL

MOSCAPs were fabricated on 300-nm-thick, *n*-type In_{0.53}Ga_{0.47}As (Si: 1 × 10¹⁷ cm⁻³) grown by molecular beam epitaxy on (001) *n*⁺-InP (IntelliEpi, Richardson, Texas). After a 3 min clean in buffered HF, samples were transferred to an ALD reactor (Oxford Instruments FlexAL ALD), where they

were exposed to the *in-situ* nitrogen plasma/TMA surface clean immediately prior to HfO₂ growth. Two slightly different surface cleaning procedures are compared here. The first (recipe A) consisted of 7 cycles of nitrogen plasma/TMA pulses/nitrogen plasma, as described in detail elsewhere.¹⁴ The second (recipe B) is a modified version of recipe A. For recipe B, each cycle consisted of a nitrogen gas set-up step (5 s at 20 mTorr), a nitrogen plasma pulse [inductively coupled plasma (ICP) power of 100 W at 20 mTorr for 2 s], a pump step (5 s), a short TMA pulse (40 ms), followed by an Ar gas draw/purge step (7 s). After 9 of these cycles, a final nitrogen plasma pulse was added (100 W ICP power at 20 mTorr for 2 s), followed by 4 s of a N₂ stabilization step. The valve between the plasma and main reaction chambers was opened only during the nitrogen plasma pulse to avoid precursor contamination to the plasma chamber. The main differences between the two recipes are the additional pump and Ar purging steps after the nitrogen plasma and TMA pulse steps, respectively, in recipe B, as well as the shorter total time that the sample was exposed to nitrogen plasma in recipe B.

The substrate temperature was 300 °C for both cleaning and HfO₂ deposition. The chamber reactor was held at 200 mTorr during oxide deposition. The deposition cycle used was as follows: a TEMAH (tetrakis[ethylmethylamino]hafnium) pulse for 1 s (flowing 250 sccm Ar gas through a bubbler held at 60 °C) followed by an Ar gas purge step (7 s) then a short pulse of deionized water (500 ms) followed by pump (7 s) and Ar gas purge (5 s) steps. The oxide thicknesses were determined *ex-situ* (immediately after growth) using variable angle spectroscopic ellipsometry. The growth rate was ~1.3 Å/cycle. After dielectric deposition, the samples were annealed in a tube furnace at 400 °C for 15 min in forming gas (95% of N₂ and 5% of H₂) at atmospheric pressure. 85-nm-thick Ni gate electrodes were deposited by thermal evaporation through a shadow mask. The back Ohmic contact, consisting of Cr (20 nm)/Au (100 nm), was deposited using thermal evaporation. Frequency-dependent CV and conductance-voltage measurements were carried out in the dark from 1 kHz to 1 MHz at room temperature using an impedance analyzer (Agilent

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4294A). Surfaces were characterized using atomic force microscopy (AFM) and field emission scanning electron microscopy (SEM). X-ray photoelectron spectroscopy (XPS) and secondary ion mass spectrometry (SIMS) were used to investigate the interface composition.

RESULTS AND DISCUSSION

Figure 1 compares the CV curves and conductance maps measured for the ~ 4 nm $\text{HfO}_2/\text{InGaAs}$ MOSCAPs that were cleaned with recipe A [Figs. 1(a) and 1(c)] and with recipe B [Figs. 1(b) and 1(d)], respectively. In both cases, the CV characteristics are steep, and accumulation capacitance densities of greater than $2.5 \mu\text{F}/\text{cm}^2$ at 1 MHz are achieved, which corresponds to sub-nm equivalent oxide thickness (EOT). The large frequency dispersion in accumulation is typical for highly scaled MOSCAPs, for reasons that currently not fully understood.^{15–17} The measured accumulation capacitances at low frequencies suffer from leakage artifacts; however, leakage is not expected to be an issue for transistors with gate dimensions much smaller than the MOSCAPs investigated here. In particular, the current density was measured to be less than $2 \text{ mA}/\text{cm}^2$ at 2 V. At frequencies not affected by leakage, the measured accumulation capacitance dispersion is slightly smaller in the sample cleaned using recipe B than that cleaned using recipe A, indicating a reduced (interface) trap density.¹⁷ More importantly, the much smaller frequency dispersion (hump) at negative biases measured for recipe B [Fig. 1(b)] is a clear evidence of a significantly reduced D_{it} .¹¹ These qualitative observations are confirmed in the measured conductance maps [Figs. 1(c) and

1(d)], which show the normalized conductance peaks, $(G_p/A\omega q)_{\text{max}}$, where G_p is the parallel conductance, A is the capacitor area, ω is the modulation frequency, and q is the elemental charge, as a function of gate voltage and ω . The $(G_p/A\omega q)_{\text{max}}$ values (see vertical axes and scale bar on the right of each graph) can be used to estimate the D_{it} by multiplication with a factor of ~ 2.5 .¹⁸ Recipe B results in a D_{it} that is ~ 4 times lower than for recipe A (values are in the mid- $10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ range). The maps also indicate how efficient the Fermi level moves around midgap as a function of gate bias.¹⁹ For both samples, the peaks shift more than two orders of magnitude in frequency as the gate bias is changed between 0 and -1 V. For the recipe B sample, the narrower trace additionally suggests larger band bending in response to a change in gate bias.

We note that there are great inconsistencies (amounting to several orders of magnitude) in the reported D_{it} in the dielectric/III-V MOSCAP literature. Several sources of error exist for all D_{it} quantification methods, in particular, near the conduction band/valence band edges, as discussed in the recent literature (see Refs. 11 and 20, and references cited therein). One source of error in conductance maps are incorrect estimates of the oxide capacitance, which cannot be directly obtained from the CV of MOSCAPs.^{11,21} To reduce this error, the dielectric capacitance used here ($3.8 \mu\text{F}/\text{cm}^2$) was estimated from a thickness series (measurement of $C_{\text{acc}}^{-1}(t)$, where C_{acc}^{-1} is the inverse of the accumulation capacitance density and t is the thickness measured by transmission electron microscopy). This value includes the interfacial layer capacitance, C_{IL} (see below). In particular, the intercept of $C_{\text{acc}}^{-1}(t)$ gives $(C_{IL})^{-1} + (C_S)^{-1}$, where $(C_S)^{-1}$ is the semiconductor capacitance at 2 V, which was calculated as described previously.²² Because of the low density of conduction band states typical for III-V semiconductors, the C_{acc} is lower than the dielectric capacitance. The slope of $C_{\text{acc}}^{-1}(t)$ can be used to extract the dielectric constant of HfO_2 , which was determined to be 17 ± 2 , which is close to the expected value. Thus, the conduction maps reported here are expected to give realistic values for the D_{it} , at least around midgap.

To investigate the origins of the different electrical properties resulting from the different cleaning recipes, Fig. 2 shows AFM and SEM images of the HfO_2 film surfaces after the postdeposition anneal (images taken of as-deposited films show qualitatively similar features). The surface of the recipe A sample [Fig. 2(a)] is rougher, and shows features that are up to 10 nm in height. The sample also exhibits regions of poor coverage, as seen in SEM [darker areas in Fig. 2(c)]. In contrast, the dielectric film of the recipe B sample is completely coalesced and exhibits a much more uniform surface, with lower roughness. The latter may be caused by shorter total plasma time, because long plasma exposures are known to result in surface roughening.²³ Occasional surface features still exist but are only about 2 nm in height. Since a main difference between recipes A and B is the additional pumping/purging steps in B, we may conclude that these steps result in improved nucleation. Improved nucleation and growth of HfO_2 on III-V surfaces using small amounts of TMA either before or during

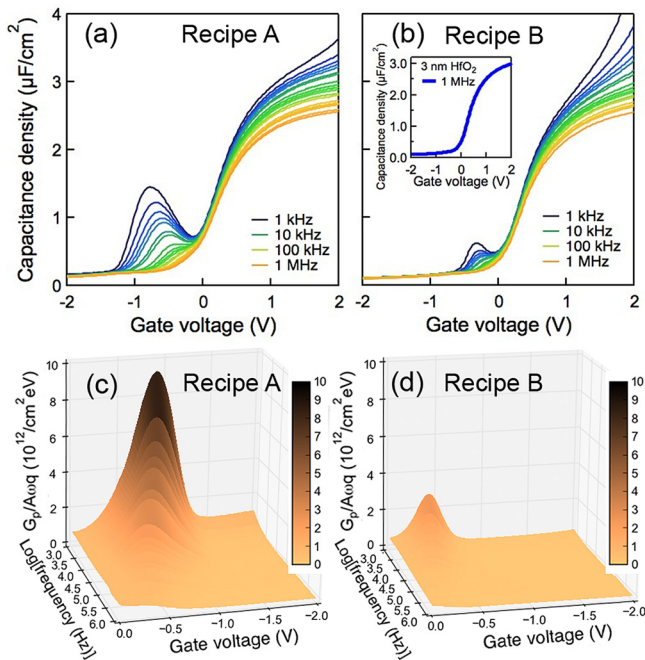


FIG. 1. Electrical characteristics of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOSCAPs with ~ 4 nm HfO_2 subjected to pre-deposition surface cleaning recipes A and B, respectively. (a) and (b) CV characteristics as a function of frequency; (c) and (d) normalized parallel conductance maps, showing $(G_p/A\omega q)_{\text{max}}$ as a function of gate voltage and frequency. The MOSCAP size is $8.2 \times 10^{-5} \text{ cm}^2$ and $1.8 \times 10^{-4} \text{ cm}^2$ for the samples in ((a) and (c)) and ((b) and (d)), respectively. The inset in (b) shows CV curve at 1 MHz of MOSCAPs with ~ 3 nm HfO_2 subjected to pre-deposition surface cleaning recipe B.

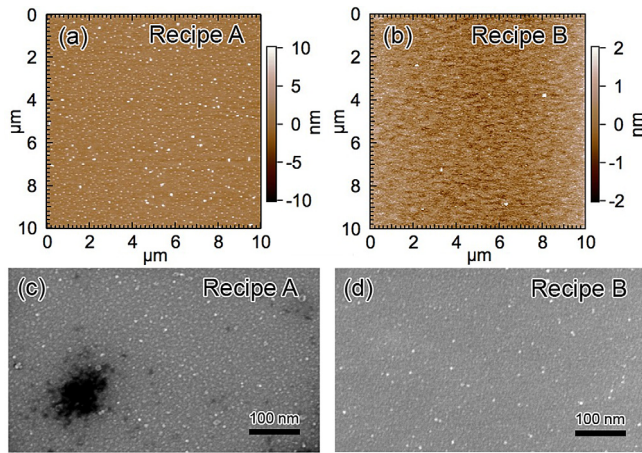


FIG. 2. Surface morphologies of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOSCAPs with ~ 4 nm HfO_2 subjected to pre-deposition surface cleaning recipes A and B, respectively. (a) and (b) AFM images; (c) and (d) SEM images.

deposition has been shown previously;^{24–26} hence the additional pumping/purging steps likely result in a more uniform distribution of the nucleation centers generated by TMA-exposure of the surface, due to the additional time for surface diffusion.

The improved nucleation also allows for further scaling. Specifically, if improved nucleation allows for complete coverage of the III-V surface at lower physical thicknesses, HfO_2 films with higher capacitance densities and good electrical properties should be achievable. Recipe B allows for MOSCAPs with capacitance densities of $3 \mu\text{F}/\text{cm}^2$ at 1 MHz for HfO_2 films with a 3 nm thickness, as shown in the inset of Fig. 1(b). This capacitance density is higher than values in the literature,^{27–29} while a very low D_{it} is maintained. Attempts to scale films grown on recipe A-cleaned surfaces to comparable thicknesses resulted in higher D_{it} , as exhibited by large frequency dispersion at negative biases.

If the nucleation is indeed facilitated by the TMA step, residual Al may be present at the interface. To investigate this, XPS was performed on thinner (~ 1.5 nm) HfO_2 films to allow signals from the interface to be detected. Figure 3 shows the measured XPS spectra from these samples. The binding energy scales were calibrated by setting the surface aliphatic hydrocarbon peak to 285.0 eV. Quantification of survey scans indicates that both samples have an As-rich surface. They also showed that Al was present in both samples at approximately 0.2 at. %. Figures 3(a) and 3(b) show the Al 2p peak, deconvoluted into two components, namely, $\text{Al } 2p^{1/2}$ and $\text{Al } 2p^{3/2}$, which are separated by 0.6 eV.³⁰ The peaks have a full width at half maximum (FWHM) of ~ 1.2 eV. A very weak nitrogen signal was also detected. Figures 3(c) and 3(d) show the As 3d and Hf 5p peaks. The $\text{As } 3d^{3/2}$ and $3d^{5/2}$ peaks have a FWHM of 0.65 eV. Because $\Delta_{\text{As } 3d} = 0.7$ eV,³⁰ we conclude that no detectable arsenic oxides are present in the interfacial layer. The $\text{Hf } 5p^{1/2}$ and $\text{Hf } 5p^{3/2}$ peaks have a FWHM of 2 eV and 1.6 eV, respectively, with $\Delta_{\text{Hf } 5p} = 7.2$ eV.³¹ SIMS (not shown) with a 3 kV Cs beam detected a negatively charged fragment at mass 41 at the oxide-arsenide interface, identified as AlN^- . This mass was not ascribed to AlCH_2^- because other masses (at

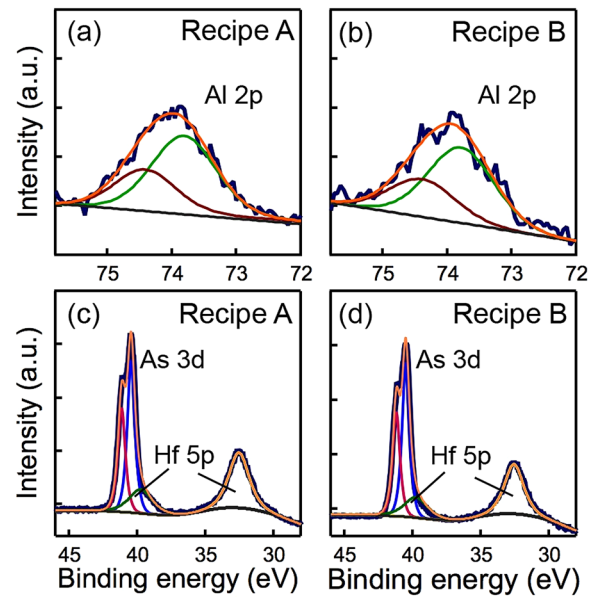


FIG. 3. XPS analysis of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOSCAPs with ~ 1.5 nm HfO_2 subjected to pre-deposition surface cleaning recipes A and B, respectively. (a) and (b) Al 2p peaks; (c) and (d) As 3d and Hf 5p peaks. The thin lines are fitted peaks.

12, 13, and 14 Da) clearly associated with hydrocarbon followed a different depth profile than mass 41, decreasing monotonically from the top surface. Additional SIMS analysis with a 2 kV oxygen beam revealed a positively charged mass at 27 peaks at the $\text{HfO}_2/\text{InGaAs}$ interface region on both samples, which we identify as Al. The small N signal in XPS and the $\text{Al } 2p^{3/2}$ peak position at 73.8 eV are consistent with an oxygen-rich AlO_xN_y interfacial layer.

The notable absence of As-(sub)-oxides at these interfaces provides evidence of the efficiency of the cleaning procedures (both recipe A and B) in native oxide removal, good coverage, and passivation of the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ surface early in the ALD process, and that even ~ 1.5 nm thin HfO_2 provides protection from subcutaneous oxidation. The results support theoretical studies that indicate that avoiding As-(sub)-oxides is critical for achieving low D_{it} .^{32–34} In particular, even for recipe A, the D_{it} is already significantly lower than for other cleaning methods,¹⁴ and this is likely due to combination of the absence of As-(sub)-oxides and the passivation properties of the AlO_xN_y interfacial layer.

Within the detection limit of XPS and SIMS, we find no difference in the interfacial chemistry between recipe A and B. This shows that these methods are not sufficiently sensitive to the atomic scale origins that are responsible for the differences in surface morphology, coverage and D_{it} between the two recipes. While this may simply be a detection limit issue, it is more likely that a reduction of defects, such as dangling bonds and subtle atomic rearrangements, which have been implicated as giving rise to D_{it} for III-V semiconductors,^{34–36} are responsible for the improvement in D_{it} with recipe B. This is in keeping with prior results that show that avoiding or reducing damage to the III-V surface results in improvements in the D_{it} .³⁷ Such defects cannot be detected by XPS or SIMS and will require the development of experimental methods, such as electron spin resonance,

which is, however, substantially more difficult for III-V semiconductors than for Si.³⁶ However, the results reported here provide indirect evidence that complete surface coverage as early as possible in the ALD process, as facilitated by optimizing the cleaning process, reduces these defects through early passivation of the surface. Conversely, nucleation issues that may result in prolonged exposure of the surface after cleaning increase the D_{it} .

CONCLUSIONS

In summary, we have shown that modifications to a pre-deposition *in-situ* cleaning using alternating cycles of remote nitrogen plasma and TMA can further substantially reduce the D_{it} of $\text{HfO}_2/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ gate stacks into the mid- $10^{12}\text{-cm}^{-2}\text{eV}^{-1}$ for sub-nm-EOT gate stacks. Comparison of different implementations of the cleaning procedure showed that improving surface coverage is critical for significant D_{it} reduction and EOT scaling. Both TMA and N are essential for providing nucleation sites that facilitate the growth of HfO_2 on $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ surfaces,^{14,24–26} and both species were detected at the interface in XPS and SIMS. The present study shows that optimization of the pre-deposition cleaning procedure, such as sequences and exposure times, are needed for a high density of these nucleation sites, and can enable very low- D_{it} and highly scaled gate stacks.

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¹A. Callegari, P. D. Hoh, D. A. Buchanan, and D. Lacey, *Appl. Phys. Lett.* **54**, 332 (1989).

²A. D. Carter, W. J. Mitchell, B. J. Thibeault, J. J. M. Law, and M. J. W. Rodwell, *Appl. Phys. Express* **4**, 091102 (2011).

³É. O'Connor, B. Brennan, V. Djara, K. Cherkaoui, S. Monaghan, S. B. Newcomb, R. Contreras, M. Milojevic, G. Hughes, M. E. Pemble *et al.*, *J. Appl. Phys.* **109**, 024101 (2011).

⁴E. J. Kim, E. Chagarov, J. Cagnon, Y. Yuan, A. C. Kummel, P. M. Asbeck, S. Stemmer, K. C. Saraswat, and P. C. McIntyre, *J. Appl. Phys.* **106**, 124508 (2009).

⁵I. Krylov, A. Gavrilov, D. Ritter, and M. Eizenberg, *Appl. Phys. Lett.* **99**, 203504 (2011).

⁶W. Melitz, J. Shen, T. Kent, A. C. Kummel, and R. Droopad, *J. Appl. Phys.* **110**, 013713 (2011).

⁷B. Brennan, R. V. Galatage, K. Thomas, E. Pelucchi, P. K. Hurley, J. Kim, C. L. Hinkle, E. M. Vogel, and R. M. Wallace, *J. Appl. Phys.* **114**, 104103 (2013).

⁸C. Weiland, A. K. Rumaiz, J. Price, P. Lysaght, and J. C. Woick, *J. Appl. Phys.* **114**, 034107 (2013).

⁹W. Melitz, T. Kent, A. C. Kummel, R. Droopad, M. Holland, and I. Thayne, *J. Chem. Phys.* **136**, 154706 (2012).

¹⁰Y. Takeda, A. Sasaki, Y. Imamura, and T. Takagi, *J. Appl. Phys.* **47**, 5405 (1976).

¹¹R. Engel-Herbert, Y. Hwang, and S. Stemmer, *J. Appl. Phys.* **108**, 124101 (2010).

¹²I. Krylov, L. Kornblum, A. Gavrilov, D. Ritter, and M. Eizenberg, *Appl. Phys. Lett.* **100**, 173508 (2012).

¹³K. Martens, C. O. Chui, G. Brammertz, B. De Jaeger, D. Kuzum, M. Meuris, M. M. Heyns, T. Krishnamohan, K. Saraswat, H. E. Maes *et al.*, *IEEE Trans. Electron Devices* **55**, 547 (2008).

¹⁴V. Chobpattana, J. Son, J. J. M. Law, R. Engel-Herbert, C. Y. Huang, and S. Stemmer, *Appl. Phys. Lett.* **102**, 022907 (2013).

¹⁵S. Stemmer, V. Chobpattana, and S. Rajan, *Appl. Phys. Lett.* **100**, 233510 (2012).

¹⁶A. Ali, H. Madan, S. Koveshnikov, S. Oktyabrsky, R. Kambhampati, T. Heeg, D. Schlom, and S. Datta, *IEEE Trans. Electron Devices* **57**, 742 (2010).

¹⁷A. M. Sonnet, C. L. Hinkle, D. Heh, G. Bersuker, and E. M. Vogel, *IEEE Trans. Electron Devices* **57**, 2599 (2010).

¹⁸E. H. Nicollian and J. R. Brews, *MOS (Metal Oxide Semiconductor) Physics and Technology* (John Wiley & Sons, New York, 1982).

¹⁹H. C. Lin, G. Brammertz, K. Martens, G. de Valicourt, L. Negre, W. E. Wang, W. Tsai, M. Meuris, and M. Heyns, *Appl. Phys. Lett.* **94**, 153508 (2009).

²⁰A. J. Grede and S. L. Rommel, *J. Appl. Phys.* **114**, 114510 (2013).

²¹D. Veksler, P. Nagaiah, T. Chidambaram, R. Cammarere, V. Tokranov, M. Yakimov, Y. T. Chen, J. Huang, N. Goel, J. Oh *et al.*, *J. Appl. Phys.* **112**, 054504 (2012).

²²R. Engel-Herbert, Y. Hwang, and S. Stemmer, *Appl. Phys. Lett.* **97**, 062905 (2010).

²³J. S. Herman and F. L. Terry, *J. Vac. Sci. Technol. A* **11**, 1094 (1993).

²⁴Y. Hwang, V. Chobpattana, J. Y. Zhang, J. M. LeBeau, R. Engel-Herbert, and S. Stemmer, *Appl. Phys. Lett.* **98**, 142901 (2011).

²⁵Y. Hwang, R. Engel-Herbert, and S. Stemmer, *Appl. Phys. Lett.* **98**, 052911 (2011).

²⁶J. B. Clemens, E. A. Chagarov, M. Holland, R. Droopad, J. Shen, and A. C. Kummel, *J. Chem. Phys.* **133**, 154704 (2010).

²⁷S. Koveshnikov, N. Goel, P. Majhi, H. Wen, M. B. Santos, S. Oktyabrsky, V. Tokranov, R. Kambhampati, R. Moore, F. Zhu *et al.*, *Appl. Phys. Lett.* **92**, 222904 (2008).

²⁸R. Suzuki, N. Taoka, M. Yokoyama, S. Lee, S. H. Kim, T. Hoshii, T. Yasuda, W. Jevasuwan, T. Maeda, O. Ichikawa *et al.*, *Appl. Phys. Lett.* **100**, 132906 (2012).

²⁹M. El Kazzi, L. Czornomaz, C. Rossel, C. Gerl, D. Caimi, H. Siegwart, J. Fompeyrine, and C. Marchiori, *Appl. Phys. Lett.* **100**, 063505 (2012).

³⁰C. D. Wagner, W. M. Riggs, I. E. Davis, J. F. Moulder, and G. E. Muilenberg, *Handbook of X-ray Photoelectron Spectroscopy* (Perkin-Elmer Corp., Minnesota, 1979).

³¹M. Engelhard, J. Herman, R. Wallace, and D. Baer, *Surf. Sci. Spectra* **18**, 46 (2011).

³²W. Wang, K. Xiong, R. M. Wallace, and K. Cho, *J. Phys. Chem. C* **114**, 22610 (2010).

³³L. Lin and J. Robertson, *J. Vac. Sci. Technol. B* **30**, 04E101 (2012).

³⁴H. P. Komsa and A. Pasquarello, *Physica B* **407**, 2833 (2012).

³⁵W. E. Spicer, I. Lindau, P. Skeath, and C. Y. Su, *J. Vac. Sci. Technol.* **17**, 1019 (1980).

³⁶V. Djara, T. P. O'Regan, K. Cherkaoui, M. Schmidt, S. Monaghan, É. O'Connor, I. M. Povey, D. O'Connell, M. E. Pemble, and P. K. Hurley, *Microelectron. Eng.* **109**, 182 (2013).

³⁷G. J. Burek, Y. Hwang, A. D. Carter, V. Chobpattana, J. J. M. Law, W. J. Mitchell, B. Thibeault, S. Stemmer, and M. J. W. Rodwell, *J. Vac. Sci. Technol. B* **29**, 040603 (2011).