Spatial Correlation Extraction via Random Field Simulation and Production Chip Performance Regression

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Abstract

Statistical timing analysis is based on *a priori* knowledge of process variations. The lack of such *a priori* knowledge of process variations prevents accurate statistical timing analysis and has been largely blamed for foundry confidentiality policy. In this paper, we show that a significant part of process variations are specific to the design, and can only be achieved based on production chip performance variabilities. We adopt the homogeneous isotropic random field model for intra-die random variations, apply fast Fourier transform (FFT) to simulate a homogeneous isotropic random field, obtain corners for Monte Carlo SPICE simulation of timing critical paths in a VLSI circuit, and apply regression to match production chip performance variability. Our experimental results based on a timing critical path in an industry design with 70*nm* Berkeley Predictive Technology Models reveal *constant mean, increased standard deviation, and decreased skewness of a signal propagation path delay as spatial correlation increases*. Our proposed spatial correlation extraction technique can be applied in a chip tapeout process, where process variations extracted from an early tapeout help to improve statistical timing analysis accuracy and guide engineering change order for subsequent tapeouts.

1 Introduction

VLSI designs experience increased variabilities as technology scales. Reduced layout feature sizes lead to increased geometric, lithography, chemical, and dopant variabilities in the manufacturing process, which result in increased circuit performance variability. Such circuit performance variability is increasingly significant in the latest technologies, and has be to captured by statistical timing analysis for parametric yield estimation.

Statistical timing analysis needs *a priori* knowledge of process variabilities, e.g., in terms of standard deviations and correlations of various process parameters. The lack of such *a priori* knowledge of process variabilities has formed a fundamental gap to achieve accurate parametric yield estimation. This has been largely blamed for foundry confidentiality policy. However, in this paper, we show that a significant part of process parameter variabilities differ for each design, and can be achieved only *after* a VLSI design is manufactured and measured. Extracting process variabilities can be achieved based on production chip performance variability, even without access to foundry confidentiality data. Of particular interest is spatial correlation extraction, which is vitally important to achieve accurate statistical timing analysis [13], and can only be extracted based on production chip performance variability as we present as follows.

Test chips and test structures help foundry process development and provide design guidelines in SPICE models, technology file parameters, and design rules. However, they provide only limited capability for production monitoring and yield analysis [12]. This is because process parameters in a test chip may not have the same variabilities as in the production chip. Most interconnects in a test chip look nothing like in a production chip. Lateral layout feature dimensions, e.g., wire width and transistor channel length, are given by lithography process and affected by nearby features [3]. Vertical layout feature dimensions, e.g., wire thickness and gate oxide thickness, are given by chemical mechanical polishing (CMP) process and depend on local layout density [14]. As a result, accurate production monitoring and yield analysis can only be achieved via production chip based process variation extraction.

Process parameter spatial correlation has received increased attention recently. A conventional technique partitions the layout plane by a grid, assuming perfect correlation for all random variables (e.g., transistor threshold voltage or channel length) in the same grid cell, and computes a correlation matrix for the grid cells [1]. The number of correlated random variables can be further reduced by (1) clustering the grid cells into perfect correlation circles [11], (2) applying principle component analysis (PCA) [1, 16], or (3) applying Kahuna-Loève expansion [2]. These techniques are based on a discrete random field (represented by the grid cells). A continuous (homogeneous isotropic) random field is the simplest model for intra-die variation (consisting of a single parameter), which greatly facilitates spatial correlation extraction, with reasonable accuracy (a homogeneous isotropic random field has a constant mean and a spatial correlation which depends only on distance) [20]. However, in [20], spatial correlations are extracted based on

direct measurement at sampling sites across a chip, which is unlikely to be available in a production chip. To the best of our knowledge, no practical spatial correlation extraction method is available, except a recent publication [10] which proposes to refine spatial correlation bounds by rejection sampling based on statistical static timing analysis (SSTA) results.

In this paper, we model process parameter variations across a chip in homogeneous isotropic random fields, and propose a spatial correlation extraction technique based on production chip performance statistics. We simulate a homogeneous isotropic random field by fast Fourier transform (FFT), generate corners for Monte Carlo SPICE simulation, and apply regression to match production chip performance variability. Our proposed technique can be applied to a chip tapeout process, where process variation extraction based on an early tapeout improves statistical timing analysis accuracy and guides engineering change order for subsequent tapeouts.

We organize the rest of the paper as follows. We briefly introduce process variations in Section 2, and give our problem formulation in Section 3. We present our proposed spatial correlation extraction technique in Section 4, and give our experimental results in Section 5 before we conclude in Section 6.

2 Background

Variabilities in various VLSI manufacturing processes, e.g., lithography, chemical mechanical polishing (CMP), chemical vapor deposition (CVD), ion implantation, etc., give rise to different physical process parameter variations, including:

1. lateral layout feature dimension variations, such as (1) transistor channel length, and (2) metal wire width variations, which are given by lithography processes,

2. vertical layout feature dimension variations, such as (1) transistor gate oxide thickness, and (2) metal wire thickness variations, which are given by mechanical polishing (CMP) processes, and

3. ion implantation dopant fluctuation and chemical vapor deposition (CVD) variation, which affect (1) transistor threshold voltage and (2) via resistance, respectively.

Such physical process variations result in electrical parameter and performance variations in a VLSI circuit. Based on the scales of the variation components, these variations are decomposed into (1) inter-die variations, (2) systematic intra-die variations, and (3) residual intra-die random variations [18].

1. Inter-die variations are generally caused by additional equipment nonuniformity and other physical effects such as thermal gradients and loading phenomena, and are slowly varying and smooth at a large scale. They are independent on the chip under manufacturing, and can be filtered out from the production chip performance measurement by averaging over the dies [18].

2. Intra-die variations are often caused by layout and topography interaction with the process, such as pattern planarization in chemical mechanical polishing (CMP), and lithography effects in determining transistor channel lengths and metal line widths. Lithography [3] and CMP [14] simulations provide accurate prediction of systematic intra-die variations.

3. The residual intra-die random variations can be filtered to have zero means. Their autocorrelation functions approximately depend only on the distance between the two components on a chip [4, 13, 15, 20].

Among the variation components, VLSI performance variation is mainly affected by spatial correlation between components on a chip [13], including (1) the slow varying inter-die variations and (3) the residual intra-die random variations, since (2) the systematic intra-die variations are given by layout features in local areas, hence are uncorrelated and their effects on a signal propagation path delay largely cancel each other.

3 Problem Formulation

In this paper, we study the problem of process variation extraction. We show that any accurate process variation extraction can only be achieved based on production ship performance variabilities. Of particular interest is spatial correlation extraction, which is critical in achieving accurate statistical timing analysis, and can only be achieved by extracting intra-die random variations, given lithograph and CMP simulation results for systematic variations. We formulate our problem as follows.

Problem 1 (Production Chip Process Variation Extraction) *Given*

1. *a (SPICE netlist) circuit,*

2. *(SPICE transistor) performance models, and*

3. *(critical path delay) performance variabilities from production chip measurement,*

find dominant parameter variations in the performance models such that minimum mismatch is achieved between the model prediction and the production chip performance variability measurement.

Given systematic variation prediction results (e.g., by lithography and CMP simulations and correspondent parasitics extraction which translate geometries to electrical parameters), we model the residual random variations by homogeneous isotropic random fields, and apply regression to extract spatial correlations of the random fields which best fit the production chip performance variability measurement. For the most accurate statistical performance analysis, we simulate homogeneous isotropic random fields to generate corners, and apply Monte Carlo SPICE simulation for the timing critical paths

in the design. For efficiency, we establish functional relationships between performance variations and process parameter spatial correlations, and apply regression based on the established functional relationships. Algorithm 1 summarizes our proposed process variation extraction method.

Algorithm 1: Process Variation Extraction via Performance Variations

Input: VLSI circuit, SPICE models, performance variations
Output: Dominant process parameter spatial correlations

1. Select dominant process parameter variations to extract
2. Predict systematic variations
3. For each set of process parameter spatial correlations
3. Simulate homogeneous isotropic random fields
4. Perform Monte Carlo SPICE simulation
5. Find functional relationships between perf. var. and spatial corr.
7. Perform regression
8. Find best fit process parameter spatial correlations

4 Modeling and Extraction of Spatial Correlations

4.1 Homogeneous Isotropic Random Field

We model intra-die random variations by homogeneous isotropic random fields [20], i.e., they have identical means at every location on the chip, and their spatial correlations depend only on the distance between the two locations. Most intra-die random variations closely resemble homogeneous isotropic random fields, e.g., transistor channel doping concentration fluctuation results from ion implantation atmosphere pressure variation and has identical means and zero spatial correlations across a chip. Furthermore, we can enhance the accuracy of a homogeneous isotropic random field model as follows.

1. We can separate systematic intra-die variations and inter-die variations such that the remaining intra-die random variations have identical (zero) means over the layout plane. This is because systematic variation prediction includes a minimum deviation regression process which tunes model parameters and achieves mean variation predictions.

2. We can scale the vertical and horizontal dimensions to remove any orientation preference which may be present in a manufacturing process, e.g., lens aberration takes place only in the stepper scan direction (which, however, is not significant, and only leads to within 5% transistor channel length variation [6]).

A homogeneous isotropic random field model for intra-die random variations achieves not only accuracy but also efficiency in spatial correlation extraction. We present the formal definition of a homogeneous isotropic random field as follows.

Definition 1 *A random function $\xi(x)(x \in R^n)$ is a homogeneous isotropic random field if $E[\xi(x)] = const$ (e.g. 0), $E[\xi^2(x)] < \infty$, and its autocovariance function $E[\xi(x)\xi(y)] = R_{\xi\xi}(r)$ depends only on the distance $r = |x-y|$ between the two locations x and y [17].*[1]

A homogeneous isotropic random field has specific autocovariance functions, e.g., as follows [20]:

$$R_{\xi\xi}(r) = e^{-\alpha r} \tag{1}$$

where α is a parameter that regulates the decaying rate of the correlation function with respect to distance r.

The simplicity of this model (with a single parameter a) greatly facilitates spatial correlation extraction. We adopt this spatial correlation function for homogeneous isotropic random field extraction in this paper, while our method is independent on the spatial correlation function that we adopt, any other possible spatial correlation functions can also be applied or found by regression techniques [20].

4.2 Fast Fourier Transform Based Simulation

We simulate the random fields of process parameters to generate corners for Monte Carlo SPICE simulation.

A homogeneous isotropic random field $\xi(x)$ is completely described by its autocovariance function $R_{\xi\xi}(r)$ or its autospectral density function $G_{\xi\xi}(\omega)$, which form a Fourier transform pair [19]:

$$\begin{aligned} R_{\xi\xi}(r) &= \int_R e^{i\omega r} G_{\xi\xi}(\omega) d\omega \\ G_{\xi\xi}(\omega) &= \int_R e^{-i\omega r} R_{\xi\xi}(r) dr \end{aligned} \tag{2}$$

where $\omega = 2\pi\lambda^{-1}$ is frequency, λ^{-1} is wavenumber, λ is wavelength. For a real-valued random field, $G_{\xi\xi}(\omega) = G_{\xi\xi}(-\omega)$, we denote the one-sided spectral density function as $S_{\xi\xi}(\omega)$.

Let ω_u be the upper cutoff frequency, above which the values of the frequency spectrum are insignificant for practical purposes. We divide the interval $[0, \omega_u]$ into N equal parts, each having length $\Delta\omega = \omega_u/N$. To apply the FFT in the simulations, we choose ω_k such that for any $k \geq 1$, $\omega_{k+1} - \omega_k = \Delta\omega$. Let (r, φ) be the polar coordinates in a 2-D random field. The simulation result $\xi'(r, \varphi)$ is given in the form of Riemann integral sum as follows [7].

$$\begin{aligned} \xi'(r,\varphi) &= \sqrt{2\pi\Delta\omega} \sum_{l=-L}^{L} \sum_{k=1}^{N} \sqrt{\omega_k S_{\xi\xi}(\omega_k)} J_l(\omega_k r) \\ &\quad (cos(l\varphi)\eta_{lk1} + sin(l\varphi)\eta_{lk2}) \end{aligned} \tag{3}$$

where $J_l(.)$ is Bessel function of l-th order, $\eta_{lkm}, m = 1, 2$ are independent Gaussian random variables with zero mean and unit variance.

The algorithm for simulating a homogeneous isotropic random field using FFT consists of two steps as follow.

[1] A random field's autocovariance function $E[\xi(x)\xi(y)] = R_{\xi\xi}(r)$ is equivalent to its spatial correlation function $E[\Delta\xi(x)\Delta\xi(y)]$ if $E[\xi(x)] = 0$.

1. Define two arrays for $1 \le k \le N$ and $-L \le l \le L$:

$$a_{lk} = \sqrt{2\pi\Delta\omega\omega_k S_{\xi\xi}(\omega_k)}\eta_{lk1}$$
$$b_{lk} = \sqrt{2\pi\Delta\omega\omega_k S_{\xi\xi}(\omega_k)}\eta_{lk2} \quad (4)$$

2. Calculate approximated random field value at any location (r,φ):

$$\varepsilon'(r,\varphi) = \sum_{l=-L}^{L}\sum_{k=1}^{N} J_l(\omega_k r)(cos(l\varphi)a_{lk} + sin(l\varphi)b_{lk}) \quad (5)$$

We have $S_{\xi\xi}(\omega)$ as follows by substituting (1) into (2).

$$S_{\xi\xi}(\omega) = \int_0^\infty e^{-(\alpha+i\omega)r}dr = \frac{1}{\alpha+i\omega} \quad (6)$$

The simulated random field is isotropic and asymptotically homogeneous (as $L \to \infty$) Gaussian with zero mean and unit standard deviation. A similar homogeneous isotropic random field simulation method is available in [7].

4.3 Regression

Having the corners generated by simulating the random fields of process parameters, we can apply Monte Carlo SPICE simulation and find the mean square mismatch between our model and the measured data. The tentative random fields are then perturbed to minimize the mean square mismatch.

For example, we can formulate the regression problem for spatial correlation decaying rate extraction as follows.

Problem 2 (Spatial Correlation Decaying Rate Extraction) Given

1. *a group of timing path* $\{p_i\}$,
2. *statistical moments* $\{m_i\}$ *(standard deviations, skewness, etc.) and/or correlations of signal propagation delays* $\{d_i\}$ *of timing paths* $\{p_i\}$ *from production chip measurement,*
3. *a set of dominant process parameter variations* $\{v_i\}$ *in homogeneous isotropic random fields with their autocovariance functions in the form of* $R_{\xi\xi}(r) = e^{-\alpha r}$,
4. *functional relationships between spatial correlation decaying rates* $\{\alpha_i\}$ *and the measured path delay statistical moments* $\{m_i\}$ *which are obtained by homogeneous isotropic random field simulation and SPICE simulation,*

find *the spatial correlation decaying rates* $\{\alpha_i\}$ *which best fit the process parameter variations* $\{v_i\}$.

For efficiency, we establish functional relationships between path delay statistical moments and process parameter spatial correlation decaying rates, such that we do not need to apply Monte Carlo SPICE simulation during regression. For a straightforward implementation, we adopt a greedy steepest descent algorithm for nonlinear optimization. More powerful methods, e.g., Levenbert-Marquis algorithm for least mean square regression, can be applied for improved efficiency and solution quality.

5 Experiment

We validate our proposed spatial correlation extraction method in the following experiments.

Assuming we are given inter-die variations and systematic intra-die variations (which are predictable by lithography and CMP simulations and correctable by OPC and dummy fill insertion techniques, and their effects usually cancel each other without the presence of correlation), we simulate the effect of spatial correlation on timing critical path delay as follows.

1. We perform timing analysis by Synopsis PrimeTime and find a timing critical path.
2. We find the locations of the cell instances in the timing critical path, simulate a homogeneous isotropic random field according to an assumed spatial correlation delaying rate α, and find the variations for each cell instance in the critical path.
3. We modify the netlist and the device models for the cell instances in the timing critical path, and perform SPICE simulation for the critical path delay statistical distribution.

We study signal propagation delay variation of a timing critical path of 30 combinational logic gates in an industry design of 109,000 components. The logic gates in the path include inverters, buffers, NAND, OR, XOR, and AOI gates, which are placed in a $165.2\mu m \times 554.4\mu m$ layout region. We simulate homogeneous isotropic random fields for gate channel length L_{gate}, transistor threshold voltage V_{th}, and interconnect width w_{int} variations,[2] and perform SPICE simulation for the gates based on $70nm$ technology Berkeley Predictive Technology Models (BPTM). The interconnects are obtained from parasitics extraction results in SPEF files.

We assume near zero spatial correlation for the transistor threshold voltage V_{th} variation (which results from ion implantation) by setting a large spatial correlation decaying rate $\alpha = 1$. The spatial correlation decaying rate α ranges from 1, 0.1, to 0.01 for gate length L_{gate} and interconnect width w_{int}, such that cell instances several hundreds or thousands μm apart would have virtually no correlation. We have a $1\mu m$ cutoff wavelength $\lambda_u = 1\mu m$, and partition the correlation frequency spectrum $[0,\omega_u]$ into 100 equal parts $N = 100$. We compute Bessel functions of order ranging from -50 to 50, i.e., $L = 50$. The simulated homogeneous isotropic random fields have an approximately unit standard deviation $\sigma = 1$. We scale the simulated random field according to different standard deviations of the parameters, e.g., gate length L_{gate} and interconnect width w_{int} have $3\sigma = 15\%$, transistor threshold voltage has $3\sigma = 30\%$.

Fig. 1 gives probability density functions (pdf's) for the critical path delay with different spatial correlation decaying rate α. Each pdf is achieved by SPICE simulation based on 1000 samples of random field variation corners. Table 1 gives the means

[2] A more detailed analysis of process parameter variations would separate PMOS and NMOS transistor channel lengths and threshold voltages, and interconnect widths on different routing layers.

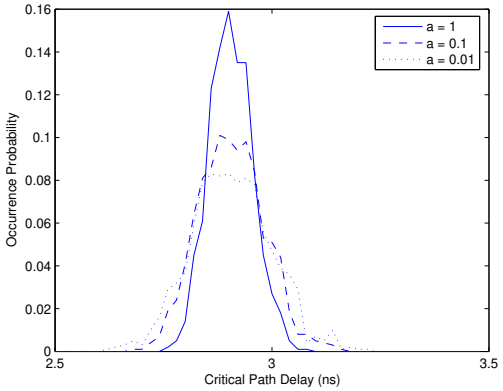

Figure 1: Probability density function (pdf) of a critical path delay with spatial correlation decaying rate $\alpha = 1, 0.1$, or 0.01 for gate channel length L_{gate} and interconnect width w_{int} variations, and $\alpha = 1$ for transistor threshold voltage V_{th} variations.

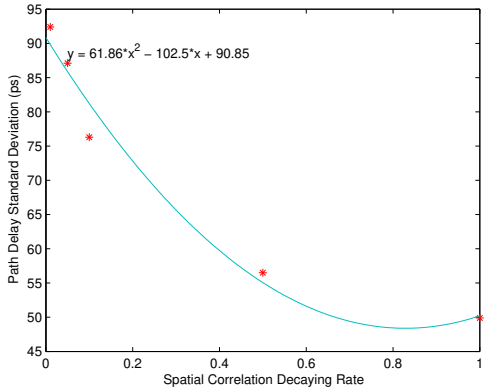

Figure 2: Path delay standard deviation σ (ps) approximated as a quadratic function of spatial correlation decaying rate α.

Table 1: The means μ, the standard deviations σ, and the skewness γ_1 of a critical path delay of 30 combinational logic gates in a 109,000 component industry design with 70nm Berkeley Predictive Technology Models.

α	1	0.5	0.1	0.05	0.01
μ (ns)	2.92	2.92	2.92	2.92	2.92
σ (ps)	49.90	56.49	76.27	87.05	92.45
γ_1	0.18	0.19	0.16	0.13	0.12

and the standard deviations of the critical path delay variations for different spatial correlations. We have the following observations.

The mean critical path delay is constant for different spatial correlation decaying rate α, while the standard deviation of the critical path delay increases as the spatial correlation decaying rate decreases. A decreased spatial correlation decaying rate gives increased spatial correlation. The two extreme cases $\alpha = \infty$ and $\alpha = 0$ corresponds to zero and 100% spatial correlation, respectively. In the presence of zero spatial correlation, delay variations for the components in a timing path would cancel each other and result in smaller path delay deviation. A larger spatial correlation results in a larger path delay variation.

The critical path delays have a positive skewness γ_1, i.e., their distributions have a longer right tail than a left tail. The skewness γ_1 of the critical path delay decreases as the spatial correlation decaying rate decreases, i.e., an increased spatial correlation results in an increasingly symmetric path delay distribution.

We observe *constant mean, increased standard deviation and decreased skewness of a signal propagation path delay for a decreased spatial correlation decaying rate*. Delay variations for other signal propagation paths are similar, i.e., the absolute locations and the orientations of the gates in the paths do not affect random variations in a homogeneous isotropic field, while the scale of the distances between the gates in a timing path can be translated to the scale of the spatial correlation decaying rate α, i.e., placing the gates in a path closer to each other is equivalent to scaling down α, which implies a larger path delay variation.

For efficiency, we find approximated functional relationships between path delay deviations and spatial correlation decaying rates, e.g., by least mean square regression based on SPICE simulation results for sampled spatial correlation decaying rates. For example, we approximate the standard deviation for the path delay of 30 combinational logic gates in our experiment as follows (Fig. 2).

$$\sigma = 61.86\alpha^2 - 102.5\alpha + 90.85 \tag{7}$$

where α is the spatial correlation decaying rate for gate channel length L_{gate} and interconnect width w_{int} ($\alpha = 0$ for transistor threshold voltage V_{th}).

Based on the functional relationships between path delay deviations and spatial correlation decaying rates, we can apply regression techniques and find process parameter spatial correlation decaying rates which best fit the path delay distributions obtained from production chip performance measurement. The achieved spatial correlations can then be taken into account in statistical performance analysis for improved accuracy, and guide statistical physical design optimization techniques, e.g., placement and gate sizing, in a successive chip tapeout process.

The proposed spatial correlation extraction technique is quite efficient. It takes $0.61s$ to simulate a homogeneous isotropic random field and generate a set of corners for 30 locations, and $2.05s$ for SPICE simulation to conduct transient analysis across a $5000ps$ time frame with $1ps$ time step, on an $i686$ Linus system with a $2.8GHz$ processor and $512MB$ memory. Finding an approximated quadratic function for path delay standard deviation σ of spatial correlation decaying rate α takes linear time of the number of samples. The runtime of regression for best fit spatial correlation decaying rates α is given by the number of path delays and the number of process parameter variations, which can be bounded for accuracy-efficiency tradeoff.

6 Conclusion

Spatial correlation is critical to VLSI timing critical path delay variation. We propose spatial correlation extraction based on production chip performance statistics. We adopt the homogeneous isotropic random field model for the on-chip variations, and propose a fast Fourier transform (FFT) based random field simulation technique to generate variation corners for Monte Carlo SPICE simulation of a timing critical path delay. We apply our proposed technique to a timing critical path in an industry design with 70*nm* Berkeley Predictive Technology Model, and observe constant mean, increased standard deviation and decreased skewness of the path delay variation. We propose to apply regression techniques to match a production chip performance statistics, and extract spatial correlations for more accurate statistical timing analysis and subsequent statistical physical design optimization, e.g., in a successive chip tapeout process.

References

[1] A. Agarwal, David Blaauw, and V. Zolotov, "Statistical Timing Analysis for Intro-Die Process Variations with Spatial Correlations," *Proc. International Conference on Computer Aided Design*, 2003.

[2] S. Bhardwaj, S. Vrudhula, P. Ghanta, and Y. Cao, "Modeling of Intra-die Process Variations for Accurate Analysis and Optimization of Nano-scale Circuits," in Proc. *Proc. Design Automation Conference*, 2006, pp. 791-796.

[3] Calibre WORKbench User's Manual, Mentor Graphics, Inc., 2006.

[4] P. Friedberg, Y. Cao, J. Cain, R. Wang, J. Rabaey, and C. Spanos, "Modeling Within-Die Spatial Correlation Effects for Process-Design Co-Optimization," *Proc. International Symposium on Quality Electronic Design*, pp. 516-521, 2005.

[5] A. Genz, "Numerical Computation of Multivariate Normal Probabilities," *Journal of Computational and Graphical Statistics,* Vol. 1, 1992, pp. 141-149.

[6] A. B. Kahng, C.-H. Park, P. Sharma and Q. Wang, "Lens Aberration-Aware Timing-Driven Placement," *Proc. Design Automation and Testing in Europe*, Mar. 2006, pp. 890-895.

[7] L. S. Katafygiotis, A. Zerva and A. A. Malyarenko, "Simulation of Homogeneous and Partially Isotropic Random Fields," *Journal of Engineering Mechanics*, Oct., 1999, pp. 1180-1189.

[8] P. R. Kramer, O. Kurbanmuradov, and K. Sabelfeld, "Comparative Analysis of Multiscale Gaussian Random Field Simulation Algorithms," *Journal of Computational Physics*, 2005.

[9] B. Lee, D. S. Boning and L. Economikos, "A Fixed Abrasive CMP Model," *Proc. International Conference on Chemical-Mechanical Polish (CMP) Planarization for ULSI Multilevel Interconnection (CMP-MIC)* , Mar. 2001, pp. 395-402.

[10] B. N. Lee, L.-C. Wang and M. S. Abadir, "Refined Statistical Static Timing Analysis Through Learning Spatial Delay Correlations," *Proc. Design Automation Conference*, 2006, pp. 149-154.

[11] J. Luo, S. Sinha, Q. Su, J. Kawa, and C. Chiang, "An IC Manufacturing Yield Model Considering Intra-Die Variations," *Proc. Design Automation Conference*, 2006, pp. 749-754.

[12] M. Smayling, "Test Structures, Test Chips, In-Line Metrology and Inspection", *Design Automation Conference DFM Tutorial*, 2006.

[13] M. Orshansky, L. Milor, P. Chen, K. Keutzer, C. Hu, "Impact of spatial intrachip gate length variability on the performance of high-speed digital circuits," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, 2002, pp. 544-553.

[14] D. O. Ouma, D. S. Boning, J. E. Chung, W. G. Easter, V. Saxena, S. Misra and A. Crevasse, "Characterization and Modeling of Oxide Chemical-Mechanical Polishing Using Planarization Length and Pattern Density Concepts," *IEEE Trans. on Semiconductor Manufacturing*, 15(2), 2002.

[15] M. J. M. Pelgrom, A. C. J. Diunmijer, and A. P. G. Welbers, "Matching Properties of MOS Transistor," *IEEE Journal of Solid-State Circuits,* Vol SC-24, pp. 1433-1440, 1989.

[16] G. Seber, *Multivariate Observations*, Wiley Series, 1984.

[17] N. V. Semenovs'ka and M. I. Yadrenko, "Explicit Extrapolation Formulas for Correlation Models of Homogeneous Isotropic Random Fields," *Theoretical Probability and Mathematical Statistics*, 69, 2004, pp. 175-185.

[18] B. E. Stine, D. S. Boning and J. E. Chung, "Analysis and Decomposition of Spatial Variation in Integrated Circuit Processes and Devices," *IEEE Trans. on Semiconductor Manufacturing*, 10(1), Feb., 1997, pp. 24-41.

[19] L. Sun, W. Kenis and W. Wang, "Stochastic Spatial Excitation Induced by a Distributed Contact on Homogeneous Gaussian Random Fields," *Journal of Engineering Mechanics*, Jul., 2006, pp. 714-722.

[20] J. Xiong, V. Zolotov, and L. He, "Robust Extraction of Spatial Correlation," *Proc. International Symposium on Physical Design*, 2006, pp. 2-9.