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Payload-Envelope Detection and Label-Detection Integrated Photonic Circuit for Asynchronous Variable-Length Optical-Packet Switching With 40-Gb/s RZ Payloads and 10-Gb/s NRZ Labels

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***Abstract*—A photonic integrated circuit that performs 40-Gb/s payload-envelope detection (PED) and 10-Gb/s label detection for asynchronous variable-length optical-packet switching is demonstrated. The circuit consists of an InP photonic integrated device combined with electronic GaAs and InP devices on a carrier. Asynchronous variable-length optical packets with 40-Gb/s return-to-zero (RZ) payloads and 10-Gb/s non-RZ (NRZ) labels are processed by the circuit. The circuit outputs a PED electrical signal that represents the temporal location of the payload and a 10-Gb/s electrical signal representing the optical label. The optical label is detected error free. The PED signal has a rise/fall time of 3-ns and 150-ps jitter. The PED signal was also used to erase and rewrite the optical labels error free.**

***Index Terms*—Optical-label swapping (OLS), payload-envelope detection (PED), photonic integrated circuit, traveling-wave photodetector (TWPD).**

I. Introduction

OPTICAL-PACKET-SWITCHED networks are a promising approach to deal with the ever-increasing traffic on the Internet. Optical-label swapping (OLS) is a technique that allows optical-packet-switched networks to scale to a large number of nodes [1]–[5]. In OLS, each optical packet consists of a payload and a label. The payload is forwarded through each node without optical–electrical–optical (OEO) conversion. The label is used to compute to which node output the payload must be switched. Two key-label-oriented tasks occur while the payload is forwarded in optics: 1) label erase/rewrite and 2) label detection. The detected label is processed electronically, and a new label is generated in the exact location of the original.

The quality of label erase/rewrite and detection will affect the signal quality, correct packet forwarding, and cascadability of nodes. In the serial labeling technique for the OLS, the label is located serially in time before its associated payload. For serial labeling, the payload-envelope detection (PED) function is used in the label-erase/rewrite process to precisely locate the associated payload [6]. Label detection requires error-free conversion of the incoming optical label to an electrical signal for an electronic-label lookup and packet forwarding. Both of these functions must operate asynchronously where the arrival time of the optical packet is not known in advance. These functions must also work for the variable-length-packet characteristics of the Internet traffic.

Fig. 1 shows an optical-packet switch based on fast tunable wavelength conversion that forwards asynchronous variable-length optical packets. Packets are labeled by $\lambda_{x,y}$, where x is the wavelength, and y is the input port number. The PED and optical-label-detection (OLD) circuits are located at the input ports where the incoming packets can be at any wavelength on the input fiber grid. Fig. 2 is a timing diagram showing the incoming packets along with the other optical and electrical signals described in the following text. The payload, label, and guard-band durations are given later in the experimental sections. The packet switch requires that the PED output signal provide the timing control for label erasure and rewriting. By directly driving an optical gate with the PED signal, as shown in Fig. 1(b), the label (and any noise between packets) can be erased without affecting the payload. In an actual system, the PED signal may be first processed by an electronic-routing controller for packet timing control and then sent to a label eraser, as shown in Fig. 1(a). The functions, which are performed in the dashed box in Fig. 1(a), are equivalent to the functions in Fig. 1(b). The system also requires an electrical version of the optical label to be processed by an electronic forwarding lookup table, where a new label and a new wavelength for the corresponding packet are determined. The packets are sent through a fixed optical delay to allow time for the electronic processing of the label. The original label is erased; next, a label-rewrite modulator driven by the electronic-routing table writes a new optical label, and the packet is wavelength converted for routing.

In this paper, we describe and characterize the integration of the PED and OLD functions together and demonstrate their operation for the implementation with the packet switch shown in Fig. 1. Fitting more components in a single package avoids additional power supplies, circuitry, and fiber coupling and loss. Thus, size, cost, and power can be saved. The combination

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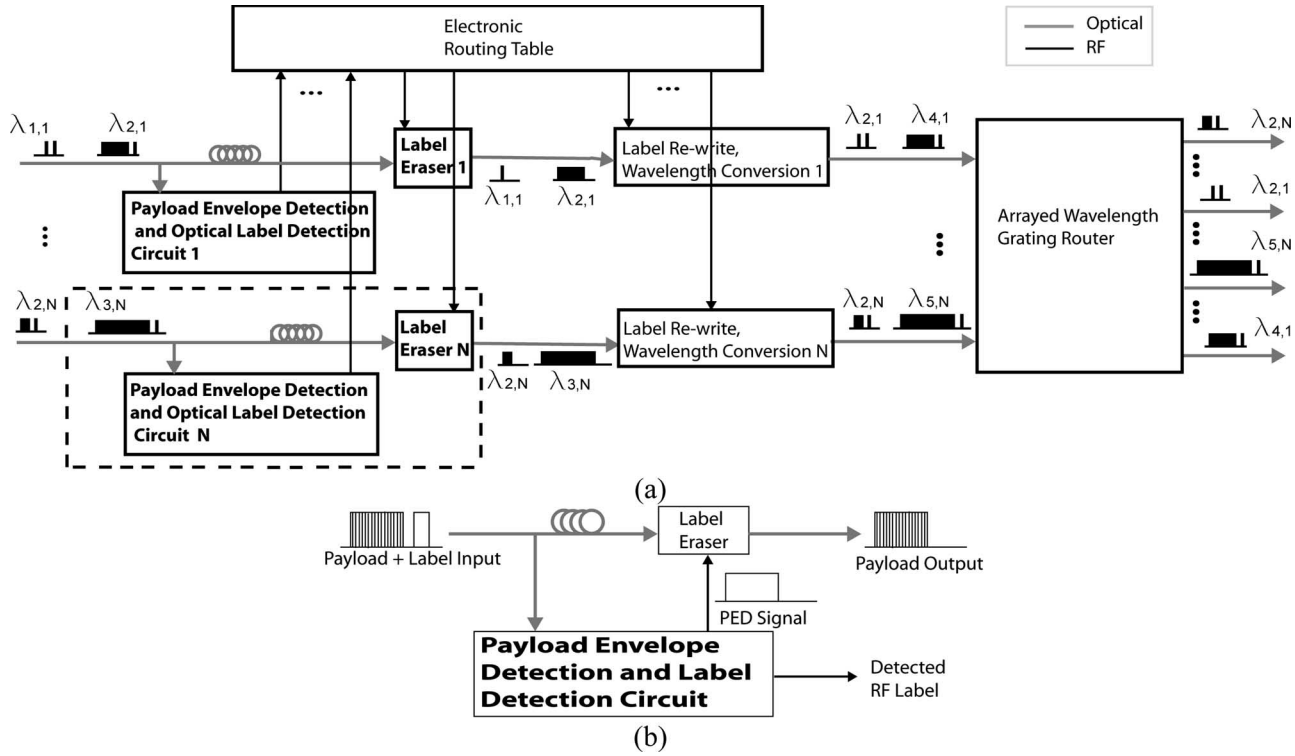

Fig. 1. (a) Schematic of the PED and OLD application in a packet-switching-network node with the wavelength-conversion-based packet forwarding. Packets are labeled with $\lambda_{x,y}$, where x is the wavelength, and y is the input port number. (b) Functions performed in the boxed area in (a) can be performed equivalently in our experiments without an electronic-routing table by using the PED signal directly from our circuit to drive the label eraser.

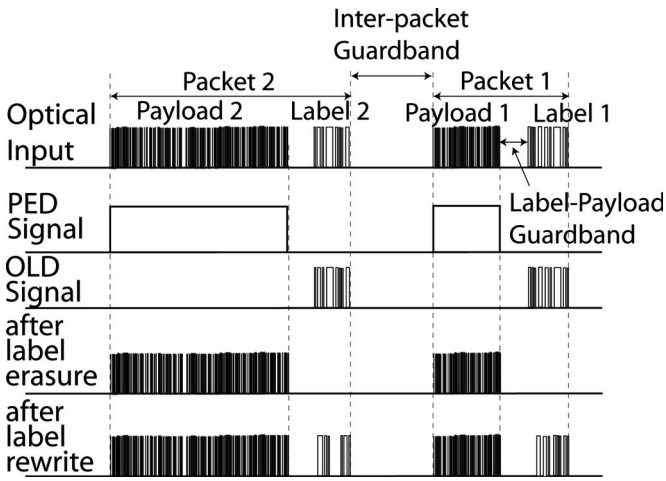

Fig. 2. Timing diagram showing the optical and electrical signals at various points in the optical-packet switch.

of different devices on a chip also proves the potential for integration with even more components involved in the packet switch. For the packets used in this paper, the labels are 128 bits long in a 10-Gb/s nonreturn-to-zero (NRZ) format and are located serially before the payloads in time. The payloads are in a 40-Gb/s RZ format and have varying length. The label-payload guard bands are fixed, and the interpacket guard bands are variable. The circuit receives packets of the format described above and simultaneously outputs an electrical PED signal and an electrical label, as shown in Fig. 1(b).

The PED signal generated by the device is characterized and then used to demonstrate error-free label erasure and rewriting. The label-detection signal generated by the integrated device is error free. Section II of this paper describes the operation principle and requirements of the PED and OLD integrated circuit. Section III discusses the design and fabrication of the photonic device made on the InP. Section IV discusses the testing of the components on the InP optoelectronic device. In Section V, the details of the carrier design are given. The PED and OLD test results are given in Section VI. Section VII gives the details of a label-erase and label-rewrite experiment performed using the PED circuit.

II. PED and OLD Circuit

A. PED and OLD Operation Principle

The PED and OLD circuit is created by combining an InP integrated optoelectronic device with GaAs and InP electronic devices on a single AlN carrier, as shown in Fig. 3. Details of the devices and carrier will be discussed in later sections.

The PED signal is generated by using a traveling-wave photodetector (TWPD—also referred to as a traveling-wave electroabsorption modulator in the references)-based optical-clock recovery (OCR) on the carrier [6]–[9]. The TWPD is part of an optoelectronic injection-locked loop formed on the carrier, as shown in Fig. 3. The TWPD generates a photocurrent when the packets enter the device. This photocurrent is injected to a 40-GHz narrowband electrical amplifier on the carrier. Next, the amplified signal passes through a power divider on the carrier that couples some of the signal out as the 40-GHz packet clock. The remaining part of the signal passes through a Q filter on the carrier for an increased frequency filtering. The signal then returns to the TWPD to complete the loop, where it combines in phase with the newly generated photocurrent. If the

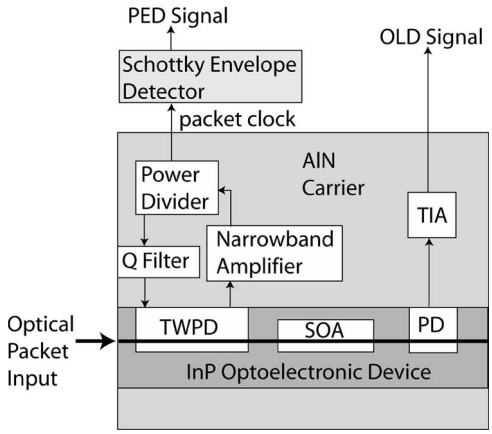

Fig. 3. PED and OLD operation principles.

input optical signal contains a clock frequency within the ring oscillator's locking range, the ring oscillator can be injection locked through the photocurrent detected by the TWPD. Thus, the 40-Gb/s RZ payload locks the oscillator, and the 10-Gb/s NRZ label has no effect. The phase of the loop can be controlled by tuning the bias of the TWPD and the gain of the narrowband amplifier. The recovered packet-clock signal can be converted to a PED signal using a Schottky envelope detector, which rectifies and self-mixes the 40-GHz packet clock. In practice, the Schottky envelope detector could be placed on the carrier by using a commercially available surface mount device, but this was avoided to allow us to test the clock-recovery capabilities of the device as well [10].

The original packets pass through the TWPD on the InP device with some fixed loss that can be compensated by a semiconductor optical amplifier (SOA). Thus, the label in the packet can be detected using a burst-mode PD on the same chip, which is located serially after the TWPD. The label-detection PD is connected to a transimpedance amplifier (TIA) on the carrier, which amplifies the electrical-label signal to drive the external clock and the data-recovery circuits.

B. System Requirements

The PED signal should have a low jitter and a relatively fast rise time. The low jitter in the PED signal is needed to avoid the unwanted erasure of the payload bits during the erase process. The fast rise time is desired so that the PED process does not increase the system latency. The rise and fall times must be shorter than the guard bands between the labels and the payloads such that none of the payload is erased during the label erasure. The fall time of the PED signal should be slightly greater than or equal to the rise time, so that none of the payload bits will be erased (assuming a low jitter). All the noise between payloads should be erased in addition to the labels.

For label detection, a receiver cannot saturate for the asynchronously arriving packets of data, i.e., bursts of data after potentially long intervals of no data. For example, any receiver with a variable gain will not work for label detection because the signal will spike for a data sequence after an extended period of zeros. Both the PED and OLD signals have a 50-Ω impedance to match the external components.

III. Optoelectronic Device Design and Fabrication

The InP device was fabricated on a semi-insulating InP substrate. It is consists of a TWPD, an SOA, and a PD on the same straight optical waveguide, as shown in Fig. 4. The material consists of offset quantum wells and centered shallow quantum wells. The details of this material can be found in [11]. The TWPD and the PD use the shallow quantum wells that have a fast optoelectronic response, and the SOA uses the additional offset quantum wells that provide an increased gain. The offset quantum wells are etched away everywhere, except in the SOA waveguide. The centered shallow quantum wells remain everywhere. A p-type material is then regrown, and the ridge is defined. Top-side n-contacts are made and isolated from each other, which is followed by several steps involving deposition and etching of photo-bis-benzocyclobutene (BCB) dielectric required for the high-speed electrical lines. Finally, p-contacts are made, and hydrogen is implanted into the passive waveguide regions for a decreased propagation loss.

The active waveguide of the TWPD is 400-μm long. As shown in Fig. 4, both ends of the TWPD's coplanar waveguide (CPW) curve away from the optical waveguide to the same side of the device, allowing for the connection to the electrical ring oscillator for clock recovery. The TWPD and the PD are both of a traveling-wave CPW design, meaning that the electrical signal will propagate along the electrical waveguide at the same speed as the optical signal in the optical waveguide, allowing for a higher frequency operation [12], [13].

To do this, the electrical waveguide above the optical propagation region should have the same impedance as the optical waveguide, which is around 20 Ω. The CPW impedance is determined predominantly by the signal (center) conductor width and the gap between the signal conductor and the ground (outer) conductors. A wider signal with narrower gaps leads to a lower impedance.

Due to the narrowness of the optical waveguide, the CPW signal and the gap width are limited, unless a dielectric layer is used to allow the signal width to increase, as shown in Fig. 4. For example, without the dielectric in place, the signal linewidth is limited to 3 μm, which is the width of the optical-waveguide ridge. A thick layer of a BCB dielectric was used to achieve this function, allowing the signal width to be 6 μm for impedance matching. At the electrical output of the devices, the impedance of the CPW line is designed to be 50 Ω to match the carrier CPW line and the external circuitry. The CPW lines are also wider at the output to allow for easier testing and wire bonding.

The SOA design and a length of 600 μm were chosen based on the characterized results given in [14]. Several PD designs were tested, as shown in Figs. 5 and 6. In general, the bandwidth of the shallow-quantum-well designs was higher than that of the offset-quantum-well designs, and the quantum efficiency (QE) increased with the device's length. Ultimately, the 150-μm PD using the shallow quantum wells was chosen for its high photocurrent generation (QE) and bandwidth.

Some precautions were taken in the device design to avoid an unwanted interaction between the integrated optoelectronic devices. In order to electrically isolate the TWPD, SOA, and PD from each other, a dry etch down to the substrate was

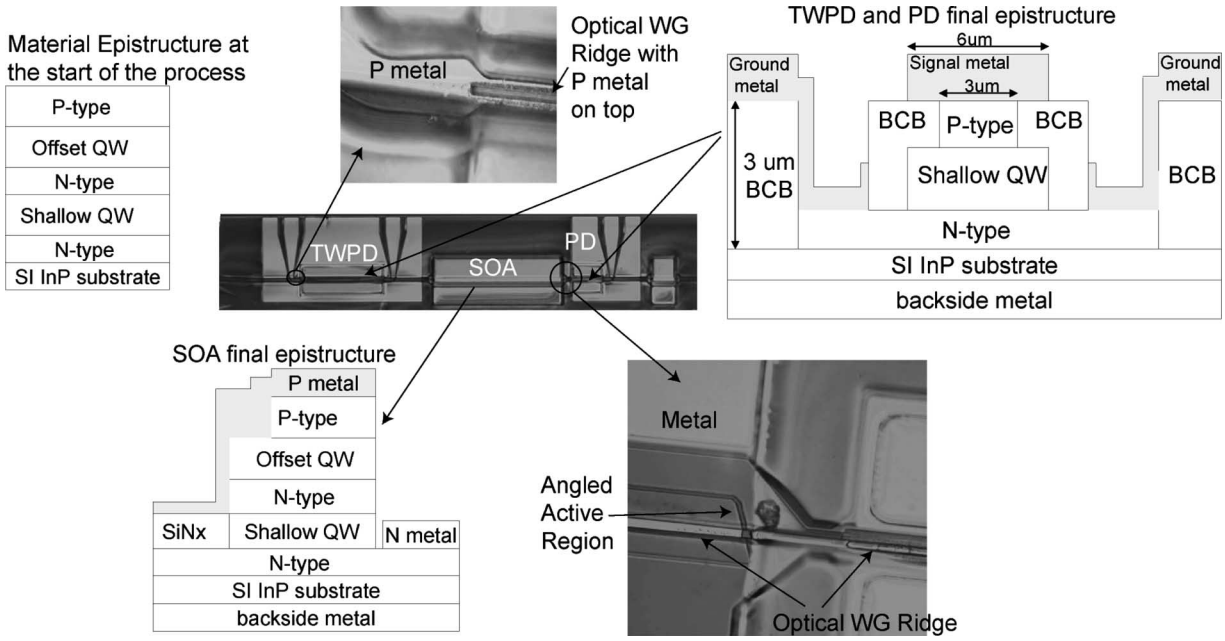

Fig. 4. Integrated-optoelectronic-device layout showing the material epistructure at the start of the process (left) and end of the process in the SOA and TWPD/PD regions. Also shown are the photographs of the electrical waveguide over the optical waveguide of the TWPD and the interface between the SOA and the PD.

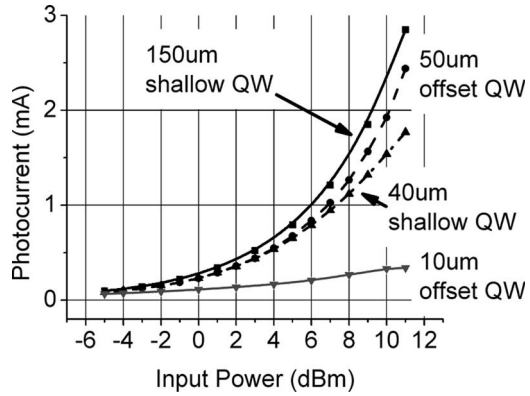

Fig. 5. Photocurrent generation versus the input power for the several PD designs.

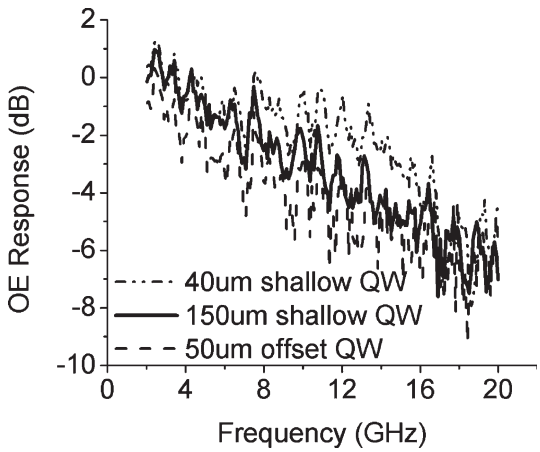

Fig. 6. Comparison of the OE response for three different PD designs.

performed. To minimize the optical reflections, the gain region of the SOA was angled with respect to the waveguide, and an absorber was placed after the PD. The offset-quantum-well material design inherently minimizes the optical reflections because of the low refractive-index contrast waveguides and continuous quaternary waveguide layer throughout the device [15]. The input and output facets of the integrated-device optical waveguide are also curved and flared to reduce the reflections and to improve the coupling efficiency. The waveguide facets are also antireflection coated. The device has a coupling loss of approximately 4 dB. Due to the compressively strained quantum wells [11], the device is polarization sensitive. This effect is more prominent for the offset quantum wells (used in the SOAs) due to their higher strain.

IV. Device-Component Testing

Before implementing the function of the integrated circuit, the components of the optoelectronic device were tested for performance individually and then together. First, the TWPD was tested. We are concerned primarily with the detection characteristics at 40 GHz, since the purpose of the TWPD is only to recover the 40-GHz clock tone. This tone will be used for the clock-recovery circuit to obtain the PED signal. The 40-Gb/s optical packets were transmitted to the TWPD (without connection to the ring oscillator), and the electrical output of the TWPD was sent to an RF spectrum analyzer. The results in Fig. 7 show that the 40-GHz clock tone is detected, as expected from a detector with a sufficient response at 40 GHz.

The optical-transmission characteristics of the TWPD were measured as a function of the reverse bias. Fig. 8 shows the TWPD optical transmission and photocurrent generated versus the reverse bias. This is an important measurement because of the serial design of the integrated device. If too much extinction occurs in the TWPD, no optical signal will pass to the PD for label detection. The TWPD is normally biased at around -3 V for our purposes, at which its extinction is near 15 dB. This is less than most PDs or modulators because of the shallow quantum

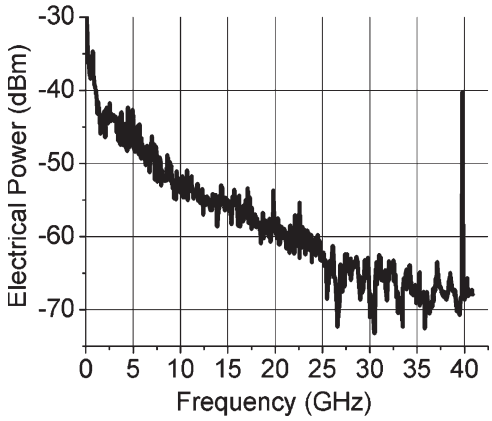

Fig. 7. TWPD response to the 40-Gb/s input signal with a −2-V applied bias.

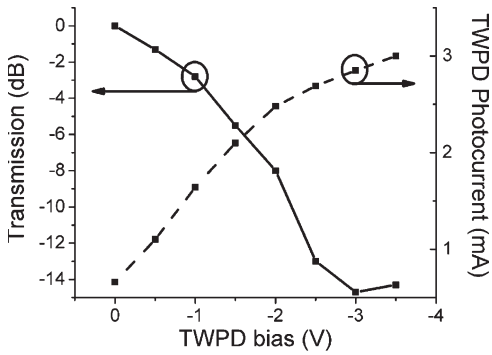

Fig. 8. TWPD transmission and photocurrent versus the reverse bias.

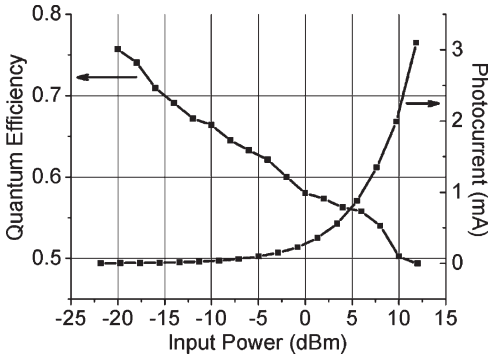

Fig. 9. PD QE and photocurrent versus the input power at −3-V bias.

wells used. For our application, this is desirable as long as the absorption is sufficient for a 40-GHz clock-tone detection.

Next, the PD was tested for several properties. We determined the QE of a stand-alone PD, with the same design as in the integrated device, by measuring the photocurrent as a function of the input optical power. The generated photocurrent is also shown. The results are shown in Fig. 9. For the reverse bias voltages greater than −3 V, there is a very little improvement in the photocurrent generated. The OE response of the PD was also measured, and the 3-dB bandwidth was measured to be around 8 GHz, as can be seen in Fig. 6, which is sufficient for the 10-Gb/s NRZ data.

Finally, all the devices were tested together in the integrated device. 10-Gb/s data was sent into the device. The TWPD bias was varied, and the SOA current was turned on and off. The PD was used to detect the data, and the electrical power generated

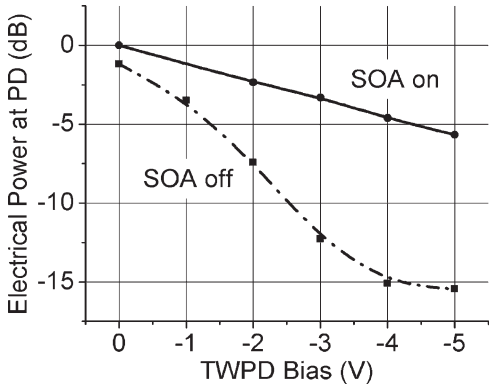

Fig. 10. PD-detected power versus the TWPD bias with the SOA either on or off.

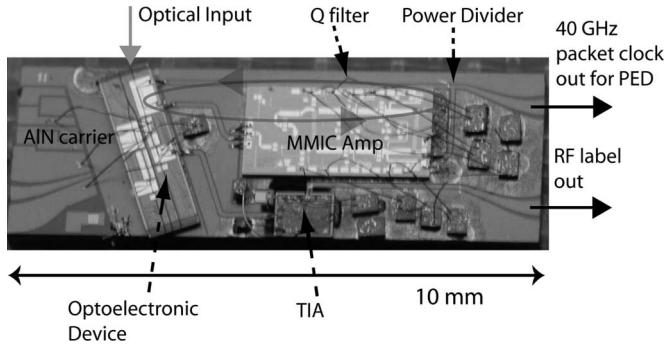

Fig. 11. Photograph of the carrier with the optoelectronic InP device and GaAs and InP electronic chips connected via the CPW lines on the carrier.

was recorded. The results are shown in Fig. 10. From Fig. 10, we also can see that when the TWPD has a high applied bias, the SOA is required in order to detect more electrical power at the PD. With the SOA on, the electrical power generated into the integrated device by the detector is several hundred millivolts for the input powers above 0 dBm.

V. Carrier Design

The InP optoelectronic device is die bonded to the AlN carrier and ribbon bonded to the CPW lines on the carrier connecting to the electronic devices, as shown in Fig. 11. All of the CPW lines are designed to have a 50-Ω impedance to minimize the reflections. The carrier has a ring-oscillator CPW line to connect to the TWPD for the 40-GHz clock recovery for the PED function. Part of this CPW line ring leaves room for the narrowband 36–43 GHz MMIC amplifier chip (XP1005; Mimix Broadband Co.) made out of GaAs, which is also die bonded to the carrier. The chip is consists of multiple transistors, and the gain can be adjusted by tuning the gate voltages. The amplifier can give up to 26 dB of gain. The amplifier output goes through a CPW-based power divider. The part remaining in the loop passes through a CPW-based Q filter that uses a capacitively coupled resonant section in the inner conductor. The Q filter was designed to have a Q factor of 50, which is chosen for a fast locking time, while still maintaining a relatively low jitter.

For the label-detection function, the PD is connected to a TIA on the carrier. The PD-output CPW line is ribbon bonded to the carrier CPW line, which leads to the TIA input. The TIA input and output are also bonded to the carrier CPW lines. The

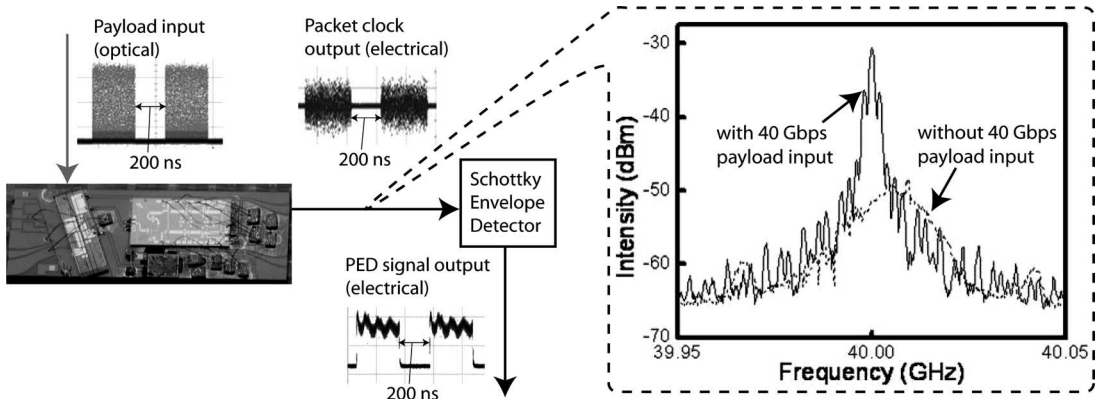

Fig. 12. Transmitted optical payloads at 40 Gb/s (upper left), electrical-recovered 40-Gb/s payload-clock output (upper middle), and PED-signal output after passing through the off-chip Schottky envelope detector (lower middle). At the far right is a graph showing the RF spectra of the ring oscillator's free-running signal output near the oscillation threshold (dashed line) and the injection-locked-recovered optical clock (solid line).

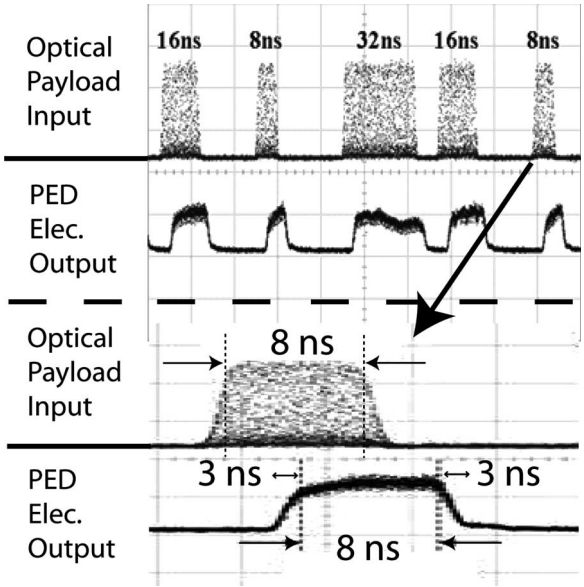

Fig. 13. Payload input and the corresponding PED-signal output for the varied-length payloads, with a zoom of an 8-ns long payload and a PED signal.

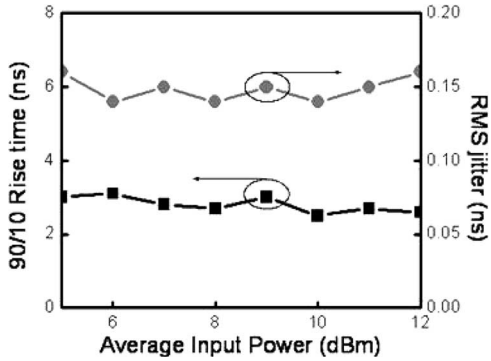

Fig. 14. Plot of the 90/10 rise time and the RMS jitter versus the input power.

label-detection output is located at the bottom right of the carrier. Space is also reserved on the carrier for the capacitors and pads needed for the electrical contact to the various devices on the carrier. The CPW lines run to the side of the carrier, where the ground-signal ground probes can retrieve the 40-GHz electrical clock signal for the PED and the label-detection signal.

To detect the payload envelope, the recovered clock must quickly appear at the beginning of the payloads and then quickly vanish at the end of the payloads. To do this, the MMIC amplifier's gain can be tuned to make the OCR run near the oscillation threshold. The output from the ring oscillator was connected to an RF spectrum analyzer for the characterization of the signal. The condition near the oscillation threshold is shown as the dashed curve in the graph on the right side in Fig. 12. Then, the 40-Gb/s optical payloads are transmitted, which are shown in the upper left inset. After tuning the oscillator's phase by changing the MMIC amplifier's gain and reverse-bias voltage of the TWPD [9], the 40-GHz payload clock was recovered, which is shown as the solid curve in the graph in Fig. 12. Its corresponding oscilloscope trace is the upper middle waveform. The recovered clock corresponds to the payload, and the zero level corresponds to the guard bands, respectively.

To obtain a PED signal, this payload-clock signal is passed through an off-chip Schottky envelope detector, which rectifies and self-mixes the signal. The result is the electrical signal shown in the lower middle in Fig. 12. The high level of the PED signal corresponds to the payload, and the zero level corresponds to the guard bands.

VI. OLD AND PED TEST RESULTS

A. PED Results

The PED signal was tested for variable-length payloads between 8 and 32 ns, which are separated by variable-length guard bands between 8 and 32 ns. The oscilloscope traces are shown in Fig. 13. A close-up of the 8-ns-long payload and the PED signal are shown at the bottom of the figure, showing the approximate rise and fall times of the PED signal and the input payloads. The payloads were generated by gating a 40-Gb/s pseudorandom bit stream (PRBS) using a lithium-niobate ($LiNbO_3$) modulator driven by an electrical-signal generator. This method of gating results in a 2-ns rise and fall time of the payload input signal. As shown in the figure, the 8-ns flat top of the PED signal corresponds well to the 8-ns flat top of the input payload.

The 90/10 rise time and RMS jitter of the PED signal were measured directly from an oscilloscope and are shown in Fig. 14. The 90/10 rise and fall times are both 3 ns. However, as

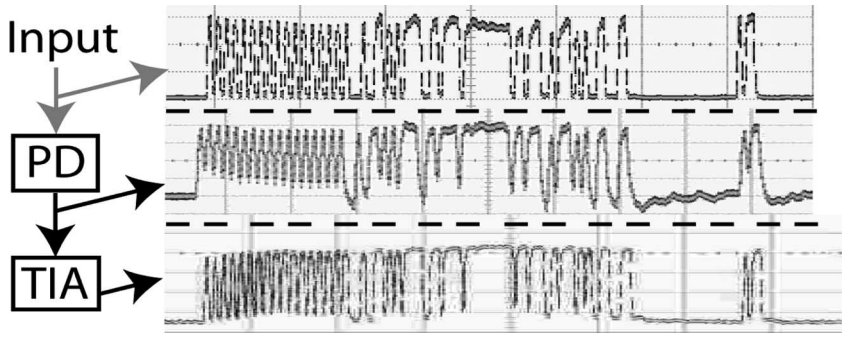

Fig. 15. Input optical label, detected electrical label from the PD, and detected label from the TIA.

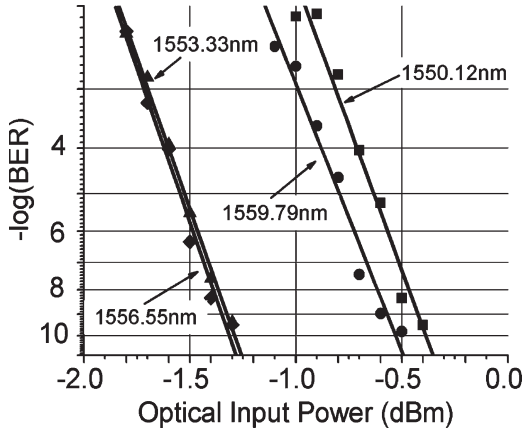

Fig. 16. BER measurements of the detected labels from the PD on the integrated device for four wavelengths.

can be seen in the figure, the rise/fall time of the input payload is 2 ns, meaning that the actual PED rise/fall time is actually less than 3 ns. The RMS jitter was measured to be 150 ps, but this measurement is limited by the precision of the oscilloscope. The actual jitter is estimated to be much less than this, which is near 1 ps. An RF spectrum analyzer was used to measure the jitter of the 40-GHz recovered clock from the device. By integrating the noise spectrum from 200 Hz to 10 MHz, the jitter was found to be 643 fs [10]. The PED-signal jitter should be close to this value.

B. Label-Detection Results

To test the PD for label detection, the 128-bit (12.8 ns) 10-Gb/s-NRZ optical labels with 190-ns guard bands were transmitted to the integrated device, and the RF output of the PD was analyzed. An optical-label input is shown at the top in Fig. 15. The label sequence has a series of 1 and 0 s at the beginning, which is required for the label's clock- and data-recovery circuits connected to the PD output in the system. In these measurements, the TWPD was unbiased, and the SOA was not used for amplification. The use of the offset quantum wells in the SOA means that much of the light can pass through the unbiased SOA without being drastically attenuated. Also, the shallow quantum wells in the modulator do not absorb as much light as the normal quantum wells in a TWPD. A typical electronic-label output by the PD is shown in the middle of Fig. 15. The figure shows that the detector does not saturate in burst mode.

The bit-error-rate (BER) measurements on the detected labels are shown in Fig. 16. To measure the BERs, a 10-Gb/s BER tester (BERT) was programmed with the labels and guard bands described above. Label detection was error free for the optical input powers greater than 0 dBm. Note that this is the power sent into the integrated device (TWPD, SOA, and PD) and that the electrical signal was sent directly from the PD to the BERT without amplification or decision circuits. With an appropriate amplifier, we believe the sensitivity would improve to -20 or -30 dBm.

The TIA used was found to be incompatible with the burst-mode output of the PD. Due to a limiting amplifier with a feedback loop inside the TIA, the amplifier saturates for the labels with either long payloads or long guard bands. An output of the TIA is shown at the bottom in Fig. 15. This is a problem that can be avoided in the future by using a more linear amplifier that will not saturate in burst mode.

VII. Label Erase and Rewrite Experiment Using the PED Signal

The experimental setup used to perform the label-swapping experiment is shown in Fig. 17. The optical input shown in the upper left of the figure consists of 10-Gb/s NRZ labels, which are 128-bits (12.8 ns) long, and 40-Gb/s RZ payloads, which are 290-ns long. The payloads and the labels are generated separately on the same wavelength and then optically combined in the proper temporal positions by using an optical-fiber delay for the label input. In this paper, the guard bands between the labels and the payloads are 30 and 75 ns. Whenever the labels and payloads are combined, a polarization controller and a variable optical attenuator are used at one of these inputs, so that the labels the and payloads have the same polarization and power level.

The input signal is split: half goes to the integrated PED circuit, while the other half passes through a fixed optical delay and goes to a label-eraser SOA board. The PED circuit recovers the 40-GHz payload clock, which then passes through a Schottky envelope detector to get the payload envelope. This passes to an amplifier and then to a voltage-to-current converter circuit. This conversion is necessary because the SOA needs to be driven by a current instead of a voltage. The spiking of the payload seen after the SOA is due to the limited bandwidth of the voltage-to-current conversion electronics, which can be avoided in the future by using better electronics.

The optical delay before the SOA is designed such that the PED signal arrives at the SOA at the same time as the optical

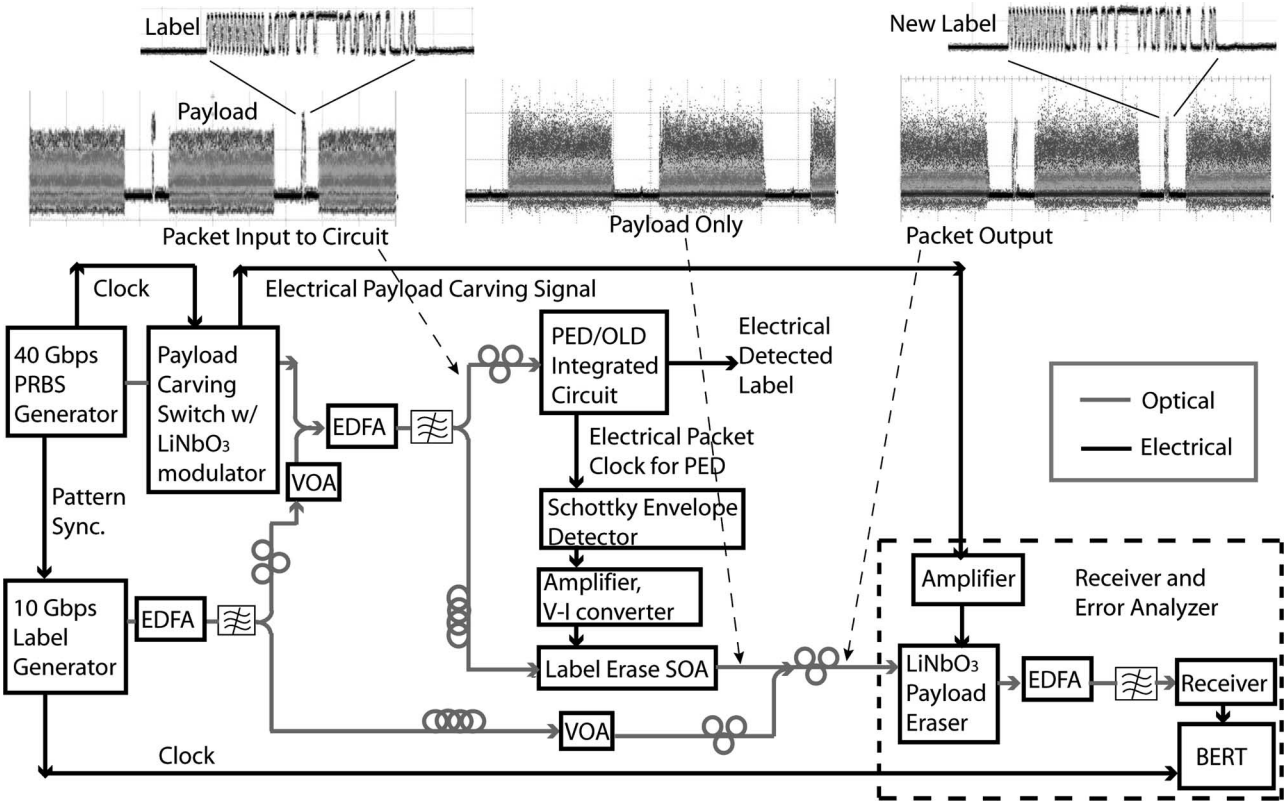

Fig. 17. Optical-label erasure and rewrite experimental setup with oscilloscope traces at the input to the PED circuit, after erasure of the original label, and at the output of the label-swapping system.

packets. Thus, the SOA will turn on and off just at the right time to erase the label and allow the payloads to pass through (with amplification). Once this timing is established, it will be the same for all the variable-length asynchronously arriving packets. The optical signal consisting of only payloads is then combined with the new labels for the final output. For simplicity, the new label comes from the same generator as the original label.

The PED-signal duration was measured on an oscilloscope to be 290 ns, which exactly matches the duration of the payload. Label erasure and rewrite was performed error free with a power penalty less than 1 dB. This small power penalty is due to the imperfect erasure of the original label by the label-eraser SOA and the added amplified spontaneous emission noise from that SOA, which was not present in the back-to-back measurement. The BER curves, which are taken for the rewritten label, are shown in Fig. 18. The experiment described here is simpler than an actual network node, as shown in Fig. 1, but the results indicate that the device can work well in such a node.

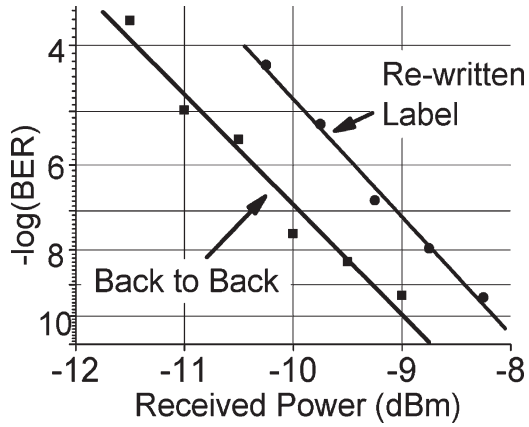

Fig. 18. Back to back and rewritten label BERs from the OLS experiment.

VIII. Conclusion

A photonic integrated circuit has been designed and demonstrated to perform optical PED and OLD for asynchronous variable-length packets consisting of 40-Gb/s RZ payloads and 10-Gb/s NRZ labels. These are two essential functions required for OLS. The circuit combines the integrated InP optoelectronic devices with GaAs and InP electronics on a single carrier. We measured the characteristics of the PED signal, and it has a 3-ns rise time and a 150-ps RMS jitter. The error-free OLD was demonstrated, and an error-free optical-label erasure and rewriting was demonstrated by combining the device in a system with other devices. The material platform, processing techniques, multiple chips on carrier integration, and the process compatible components used in our system-level experiment all indicate the potential for a fully integrated OLS.

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