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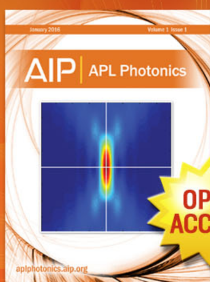

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APPLIED PHYSICS LETTERS **108**, 153103 (2016)

The electro-mechanical responses of suspended graphene ribbons for electrostatic discharge applications

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This work presents a suspended graphene ribbon device for electrostatic discharge (ESD) applications. The device structure was proposed and fabricated after careful design considerations. Compared to the conventional ESD devices such as diodes, bipolar junction transistors, and metal-oxide-semiconductor field effect transistors, the proposed device structure is believed to render several advantages including zero leakage, low parasitic effects, fast response, and high critical current density. A process flow was developed for higher yield and reliability of the suspended graphene ribbons. Direct current (DC) and transmission-line pulse (TLP) measurements were carried out to investigate the switching behavior of the device, which is crucial for ESD operation. DC measurements with a different configuration were used to assess the mechanical shape evolution of the graphene ribbon upon biasing. Finite Element Simulations were conducted and agreed well with the experimental results. Furthermore, the current carrying capability of non-suspended graphene ribbons was tested using TLP. It was found that the critical current density of graphene is higher than that of copper wires widely used as interconnects in integrated circuits (ICs). *Published by AIP Publishing.*
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While traditional ESD protection solutions using diodes, bipolar junction transistors (BJTs), and metal-oxide-semiconductor field effect transistors (MOSFETs) still dominate in current integrated circuit (IC) designs,[1–4] as scaling down of IC technologies continues according to Moore's Law, the requirements for ESD devices become more stringent.[1–6] The challenges of existing ESD solutions include:[1,2] (1) Traditional PN junction based ESD devices are inherently very leaky. For example, the typical leakage current for a 2.5 kV classic grounded-gate n-channel MOSFET (ggNMOS) ESD device can be $\sim$100 nA, which is intolerable to advanced integrated circuits (ICs) at sub-45 nm nodes. (2) ESD events involve significant heating due to very high current surges, which require ESD protection structures to be superior in electrical and thermal conduction. (3) Advanced ESD protection requires the fast response time (t_1) of ESD devices to be in the range of 10^{-10}–10^{-9} s. (4) ESD-induced parasitic capacitance (C_{ESD}) and noises become more severe for advanced mixed-signal and RF ICs. The demand for high performance ESD solutions with low parasitic effects hence calls for other ESD protection structures.

Graphene, as a two-dimensional material with superior electrical[7] and thermal conductivity,[8] as well as mechanical strength,[9] is an excellent candidate to build ESD devices from. The high electrical conductivity of graphene promises a high current carrying capability and low heating effects. Combined with graphene's excellent thermal conductivity, the heat dissipation problem can be resolved. Moreover, graphene is known as the strongest material, which guarantees the robustness of ESD device. In this work, an electro-mechanical graphene ribbon (GR) ESD protection structure was demonstrated. In principle, zero leakage and fast response time can be achieved by using the proposed device structure. While some studies of suspended graphene devices have been previously studied,[10–13] there is little information on transient characterization of suspended graphene devices for ESD protection which is different from any direct current (DC) switch phenomena. Most of the previously reported suspended graphene devices were fabricated using mechanically exfoliated graphene which is impractical for wafer-scale fabrication. The fabrication process is usually delicate and involves the use of critical point drier. The process flow developed in this study uses large-area CVD grown graphene. Si_3N_4 hard mask and a HF vapor etching technique were used to release the suspended GR rendering higher yield and device reliability.

Figure 1(a) illustrates the suspended GR ESD structure for ICs. When GR is in its original suspended position, the device is in the "OFF" state with no conduction. When a bias is applied to the device, GR will be pulled down towards the bottom by the electrostatic force. If the mechanical restoring force is strong enough to balance the electrostatic force, the GR can bend and remain in a stable equilibrium position. If the bias is large enough, the GR will touch the heavily doped Si substrate, forming a conducting path. This puts the device in the "ON" state to discharge ESD surges. The voltage at which the GR is pulled down to the bottom is the trigger voltage (V_{t1}) of the ESD device. Ideally, the on-resistance (R_{on}) should be small for efficient ESD discharging. Since there is no conducting path when the device is in the OFF state, in principle, zero leakage can be realized.

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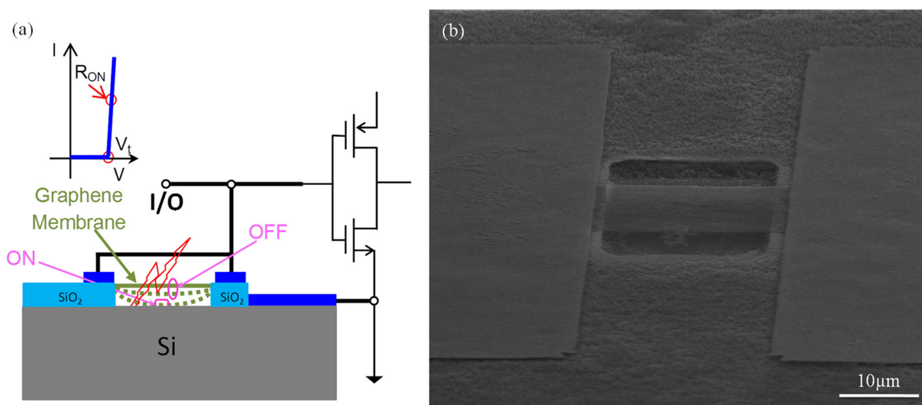

FIG. 1. Suspended GR ESD device structure. (a) Device structure and its I-V curve. (b) SEM image of an as-fabricated device.

The process flow for the fabrication of the suspended GR device is as follows: First, thermal SiO_2 (wet oxidation) with desired thickness was grown at 1000 °C on heavily doped Si substrate. Second, thin layer of LPCVD Si_3N_4 (~50 nm) was grown on top of SiO_2 to form a hard mask for the final HF vapor etching. This was followed by thermal annealing at 1100 °C in air for 1 h to release the residual strain at the interface. This step is crucial because in the final HF vapor etching step, the residual strain will cause fast etching of SiO_2 at interface, leading to the Si_3N_4 layer being peeled off. Third, photolithography and reactive-ion etching were used to etch away the Si_3N_4 in the area where the chambers will be formed in the end. AZ5214 photoresist was used in the photolithography and CHF_3 and O_2 gases were used for the plasma etching. Then, CVD grown graphene was transferred onto the trenched substrate and patterned into individual GRs by photolithography and O_2 plasma etching. Next, the metal pads consisting of Ti/Pd/Au (0.5/30/50 nm) were deposited by e-beam evaporation and lift-off processes. Finally, HF vapor etching was used to etch away the exposed SiO_2 layer to release the suspended GR structure. Figure 1(b) shows a scanning electron microscopy (SEM) image of the as-fabricated device.

Two-terminal DC measurements were carried out by applying a bias between top and bottom contacts. A current compliance of 0.1 mA was set to avoid device breakdown. Measurements were conducted on devices with different dimensions, i.e., the length (L) and the device trench depth (d), to characterize the turn-on behaviors. Figure 2(a) depicts the sharp turn-on of the devices affected by L with a fixed d. The measured V_{t1} are about 3.9, 7.2, 15.2, and 30 V for L = 7/10/15/20 μm, respectively. It seems to follow the $V_{t1} \propto 1/L^2$ relationship.[10,11] Similarly, Figure 2(b) shows the turn-on behavior of the devices with different d for a fixed L. The measured V_{t1} are about 3.9, 7.8, and 16 V for d = 350/550/850 nm, respectively, following a relationship of $V_{t1} \propto d^{3/2}$.[11] The observed DC switching behaviors lay the foundation for potential ESD discharging function of the proposed suspended GR ESD device.

Another three-terminal DC measurement set-up was used to study the mechanical shape evolution of GR as the applied bias increased. The purpose of this measurement is to measure the resistance (R) change of the GR as the bottom contact bias (V) increases, from which the bias induced charge (ΔQ), the capacitance (C) change, and the bending information of GR can be calculated and extracted. The capacitance of the device cannot be directly measured because majority of the total capacitance comes from metal contacts, whereas the capacitance from GR is negligibly small (on the order of 0.1 fF). As opposed to the device for two-terminal measurement, a thin layer of SiO_2 (50 nm) was intentionally left at the bottom of the chamber in order to prevent direct contact between the GR and the Si substrate, so that R of the GR can still be measured even after it has collapsed. The measurements were conducted by simultaneously applying lateral "top-top" and vertical "top-bottom" biases. The top-top bias was kept at 5 mV to measure the resistance of GR while sweeping the top-bottom bias. The intentionally left-behind SiO_2 would not affect the device performance much except for a slight decrease in the trigger voltage. Finite Element Simulations using COMSOL Multiphysics

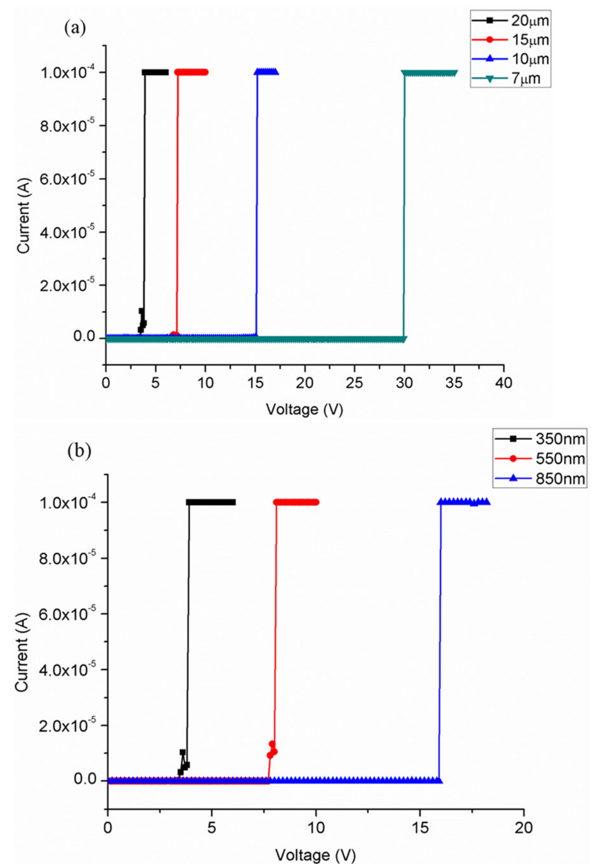

FIG. 2. Two-terminal DC measurement results show ideal switching effect. (a) Devices of L = 7/10/15/20 μm with fixed d = 350 nm. (b) Devices of d = 350/550/850 nm with fixed L = 20 μm. Width of GR is 5 μm.

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Modeling software package were conducted to compare with the experimental results. Three built-in models were used to simulate the device behavior including Solid Mechanics, Electrostatic, and Moving Mesh. Suspended GR is viewed as an equal potential entity and the effect of quantum capacitance is assumed to be negligible.

Figure 3(a) shows the change of R as V increases (for positive bottom contact bias) for a sample device with $L = 20\,\mu m$ and $d = 300\,nm$. Because the GRs used in the experiments are p-type doped, as the positive bias on Si substrate increases, the Fermi level of GR goes up and R increases slowly. At a certain voltage, R increases abruptly, corresponding to the pull-in of the GR.[14] The trigger voltage is slightly smaller than that measured by the two-terminal testing due to the smaller trench depth. The bias induced excess charge per GR width (ΔQ) and capacitance per GR width (C) of GR can be calculated by

$$Q = L^2/WR\mu, \quad (1)$$

$$C = \Delta Q/\Delta V, \quad (2)$$

where Q is the total number of charges per GR width, W is the width of GR, and μ is the mobility of GR. The calculated and simulated results of ΔQ and C as a function of V are shown in Figures 3(b) and 3(c). Similar to the change of R, ΔQ and C increase slowly at small voltage values and then increase abruptly at the pull-in voltage. When the GR is pulled in and collapsed at trench bottom, the gap between the GR and the Si substrate reaches its minimum at 50 nm; thus, the capacitance reaches its peak value and remains constant thereafter. The maximum calculated and simulated capacitance are consistent with the value calculated from the geometry of the device. The experimental and simulation results fit very well with each other. Devices with dimensions of $L = 20\,\mu m$ and $d = 2\,\mu m$ were also tested using the same measurement method. It is worth noting that the GR breaks at pull-in due to the very deep trench of the sample devices and R increases dramatically. But before breaking, the calculations are still valid, and the results are similar. Assuming that the GR fully collapses on the trench bottom and sidewalls, the tensile strain on GR is ~20%, which is smaller than the theoretical maximum strain (25%) that the graphene can sustain.[15] This can be explained by the non-uniform strain distribution on the GR.[16]

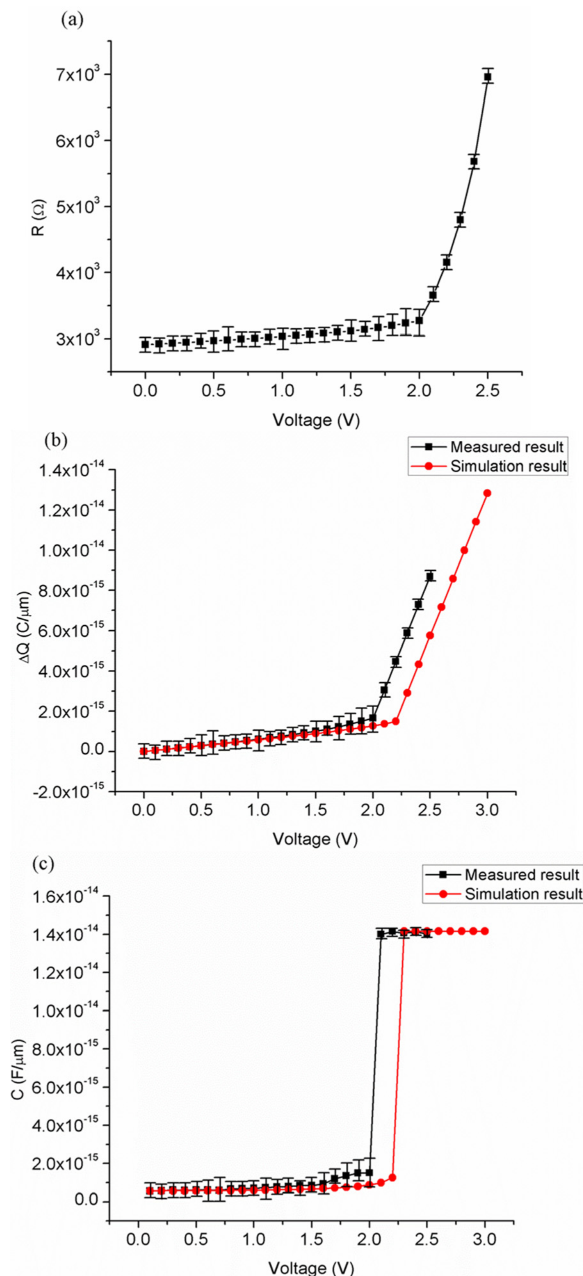

FIG. 3. Three-terminal DC measurement and simulation results for sample devices ($L = 20\,\mu m$, $W = 5\,\mu m$, $d = 300\,nm$) show the change of (a) R, (b) ΔQ, and (c) C with V (positive bottom contact bias) and pull-in phenomena.

Next, transient transmission-line pulse (TLP) measurements, specific for human body model (HBM) ESD discharging testing, were conducted using a BARTH Model 4002 HBM TLP tester to characterize the fast switching behavior and reliability of the suspended GR ESD protection device. The measurements were conducted by applying a fast TLP pulse between top and bottom contacts. A rise time of 10 ns and duration time of 100 ns were used per HBM ESD testing standard. A current compliance of 2 mA was set to avoid the breakdown of the device. Similar to the two-terminal DC measurement results, sharp turn-on behavior was clearly observed as shown in Figure 4 with a $V_{t1} \sim 19\,V$ for the sample device of $L = 10\,\mu m$. Unlike DC biasing, transient TLP testing is very fast, which confirms that the new GR device can switch at ns speed, critical for ESD protection. For device reliability study, repeated TLP stresses were applied to the same device over 30 times and the transient switching behavior remains. A slight change in V_{t1}, decreasing from 19 V to 18 V after 30-time repeats of the test, was observed for the sample device, which may be due to the slight sliding of the GR caused by repetitive pulling.[17] Further studies need to be carried out to improve the device reliability, mainly in the device fabrication.

Trigger voltage (V_{t1}) and response time (t_1) are two key parameters of ESD devices. As has been discussed previously, V_{t1} can be tuned by modifying the device dimensions to meet specific design requirements of ICs. On the other hand, t_1 of the device can be calculated as follows:[18]

$$t_1 = 3.67V_{t1}/(V_{op}f_0), \quad (3)$$

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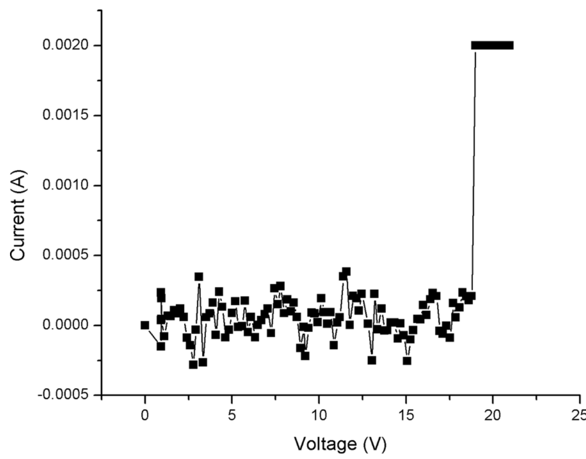

FIG. 4. TLP testing shows fast turn-on behavior of a suspended GR ESD device (L = 10 μm). TLP pulse rise time is 10 ns and duration is 100 ns.

$$f_0 = 1.03\sqrt{\frac{E}{\rho}\frac{h}{L^2}}, \quad (4)$$

where V_{op} is the operation voltage, f_0 is the resonance frequency of GR, E is the Young's modulus of graphene, ρ is the density of graphene, h is the thickness of graphene, and L is the length of GR. Due to the large E and small ρ of graphene, it is a perfect fit for making fast response ESD protection devices. Theoretically, for monolayer graphene, a GR of L = 300 nm could have a $t_1 \sim 10^{-9}$ s. Multilayer graphene may be used to provide a faster response.

Moreover, design trade-offs for ESD protection devices always exist among the ESD protection level, parasitic capacitance, and leakage current. Usually, higher ESD robustness means larger ESD device size, meaning more ESD-induced parasitic effects which are undesired for mixed-signal and RF ICs.[2–7] Therefore, two figures of merit (FOM) are often used to evaluate the overall performance of ESD devices

$$FOM_1 = I_{t2}/C_{ESD}, \quad (5)$$

$$FOM_2 = I_{t2}/I_{leakage}, \quad (6)$$

where I_{t2}, C_{ESD}, and $I_{leakage}$ are the second breakdown current, ESD-induced parasitic capacitance, and leakage current, respectively. For the suspended GR device, I_{t2} is the breakdown current of the GR, i.e., the current carrying capability of an ESD device. I_{t2} was tested by TLP for both monolayer and bilayer graphene devices. The measured I_{t2} are about 5.5 mA and 7.5 mA for monolayer and bilayer GR devices (L = 9 μm and W = 5 μm), respectively, as depicted in Figure 5. The breakdown of the devices was caused by Joule heating at high current densities and the corresponding breakdown voltages (V_{t2}) were both about 12 V for monolayer and bilayer GR devices. Bilayer graphene devices show higher I_{t2} because both graphene layers contribute to the current conduction. For practical ESD device design in the future, design optimization to maximize I_{t2} will be a key challenge in future research.[2] C_{ESD} is the capacitance between the GR and the Si substrate and can be calculated from the device geometry. Zero OFF-state leakage current could be possible. The measured leakage was ~1 pA, presumably due to non-perfect dielectrics or surface leakage. Therefore, the FOMs of the suspended GR

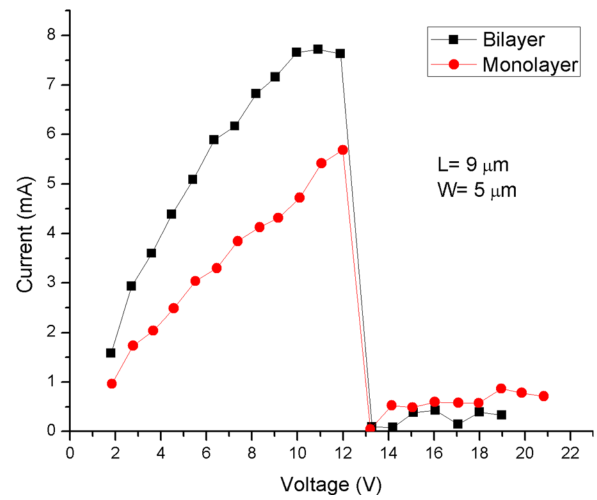

FIG. 5. TLP testing shows breakdown characteristics for monolayer and bilayer GR devices (L = 9 μm, W = 5 μm).

device samples have achieved ~14 mA/fF and ~5.5 $\times$ 10^9, which are comparable or superior to the best achievable FOMs for traditional ESD devices. We believe that I_{t2} of the suspended GR device can be much improved by using multilayer graphene, appropriate doping of graphene, and device encapsulation technique to provide an oxygen deficient working environment.[19,20] Device encapsulation could also prevent possible oxidation of the heavily doped Si surface and provide more stable atmospheric conditions, which are crucial for the device reliability. It is also worth noting that the device may render faster response times and higher current carrying capabilities by using multilayer graphene. However, the electrical and mechanical properties of graphene vary with film thickness and trigger voltage will increase with the increase of graphene number of layers. Therefore, there should be an optimum film thickness per design requirements. Further research is needed on this matter.

In summary, a suspended GR ESD device is reported and a fabrication process flow was developed. Both the DC and transient TLP measurements were carried out for the sample devices, showing the desired sharp and fast switching behaviors critical for ESD discharging operations. Measurement and simulation results match each other very well. FOMs for the sample devices achieved ~14 mA/fF (I_{t2}/C_{ESD}) and ~5.5 $\times$ 10^9 ($I_{t2}/I_{leakage}$), respectively. While more research is needed to further understand the ESD switching details and to improve the performance, the initial work clearly demonstrated that the suspended GR ESD device shall be a promising future ESD protection solution with advantages over traditional PN junction based ESD protection structures, including zero leakage, fast response, and superior FOMs.

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