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Thermal Transport in Graphene Multilayers and Nanoribbons

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Samia Subrina

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Dedicated

to

my parents

ABSTRACT OF THE DISSERTATION

Thermal Transport in Graphene Multilayers and Nanoribbons

by

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Doctor of Philosophy, Graduate Program in Electrical Engineering
University of California, Riverside, March 2011
Dr. Alexander A. Balandin, Chairperson

As the electronic industry aggressively moves towards nanometer designs thermal issues are becoming increasingly important for the high-end electronic chips. One of the approaches to mitigate the self-heating problems is the high-heat-flux hot-spot removal via incorporation into the chip designs of materials with the high thermal conductivity. Graphene is found to be one of the best known heat conductors, thus it can be used in nanoelectronic and optoelectronic devices as a heat spreader component. Graphene, the latest isolated allotrope of carbon made of individual atomic sheets bound in two dimensions, shows many remarkable properties. A non-contact method of measuring G peak position of the Raman spectrum as a function of both the temperature of the

graphene sample and the power of the heat source was used to measure the thermal conductivity of graphene. The samples in the experiment had approximately rectangle geometry and the assumption about the plane heat wave was used for the data extraction. In this dissertation research we propose to develop a model and numerical procedure for the (i) accurate modeling-based data extraction for the thermal conductivity measurements; and (ii) simulate heat propagation in semiconductor device structures with graphene layers incorporated as heat spreaders. To achieve the goals of this dissertation research we simulated the heat transport in graphene using the finite element method (FEM) with the help of COMSOL software package, which solves numerically the partial differential equations. The modeling based data extraction was necessary to determine thermal conductivity of the graphene flakes of arbitrary shape. It also substantially improved the accuracy of the measurements. The simulation of heat propagation in device structures with graphene heat spreaders allows one to assess the feasibility of the graphene high-heat-flux thermal management. We focused on understanding how thermal transport is influenced by a surface geometry of the sample and geometries of the heat sources. The simulation results showed that the size, shape and heat source geometry impact heat propagation in different ways and have to be included in the experimental data extraction. The simulation procedure provided a necessary input for next experiments on heat conduction in graphene structures e.g., graphene multi-layers and graphene–heat sink structures and other device-level thermal management applications. It was found that the incorporation of graphene or few-layer graphene (FLG) layers with proper heat sinks can substantially lower the temperature of the localized hot spots. The developed model and obtained results are important for the design of graphene heat spreaders and interconnects and lead to a new method of heat removal from nanoelectronic and 3-D chips.

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Chapter 1

Introduction

1.1 THERMAL CONDUCTIVITY

The rate of heat transfer, within a material, depends upon the temperature gradient and the thermal conductivity of that material. According to Fourier's Law of heat conduction, thermal conductivity is the time rate of heat flow, under steady state condition, through a unit area per unit temperature gradient in the direction perpendicular to the area. The heat transfer rate across the element of area A is given by

$$\dot{Q} = -KA\,\Delta T \tag{1.1}$$

where ΔT is the temperature gradient and K is the material thermal conductivity [1] .

1.1.1 Thermal conductivity: metals and non-metallic crystals

The total thermal conductivity of materials can be expressed as a sum of two components

$$K = K_e + K_L \tag{1.2}$$

where K is the total thermal conductivity, K_e is the component due to electrical charge carriers and K_L is the component due to lattice vibrations. In metals almost all the heat is carried by electrons. The lattice part of the thermal conductivity is usually negligible in a metal, firstly because of the scattering of phonons by the electrons, and secondly the electron component K_e is very high. According to Wiedemann-Franz law, at a given temperature, T the electronic polar contribution to thermal conductivity of metal with electrical conductivity, σ is given by

$$K_e = L\sigma T \tag{1.3}$$

where the constant of proportionality L is called the Lorenz number. On the other hand, in insulators, the lattice component of thermal conductivity is appreciable. In a solid, since atoms are held in their positions in the lattice by interatomic forces, any displacement or vibration given to a particular atom does not remain localized, instead it travels through the lattice giving rise to lattice wave or displacement wave and causes the propagation of thermal energy through the crystal. Phonons are the quanta of excitation of normal modes of vibration which are quasi-particles of the energy $\hbar\omega$ and quasi-momentum, $p = \hbar q$ which obeys Bose-Einstein statistics. Phonons normally propagate through a perfectly elastic crystal without interfering with one another, but at high temperature due to Umklapp process, momentum is not conserved in the phonon- phonon interaction and this introduces thermal resistance. The thermal conductivity is limited and varies as $1/T$. Lattice thermal conductivity, associating a mean-free path l with phonons can be expressed as

$$K_L = \frac{1}{3} C v_S l \tag{1.4}$$

where C is the specific heat per unit volume and v_S is the sound (phonon) velocity. At moderate temperatures, the thermal transport behavior of a pure (intrinsic) semiconductor is similar to that of an insulator with heat conduction due to lattice waves [1, 2]. Even in heavily doped semiconductors, the electronic contribution to the thermal conductivity is only on the order of one percent [3]; the conduction of heat is mostly due to lattice vibrations.

1.1.2 Thermal transport at nanoscale

Due to advancement in the synthesis and processing of structures in the nanometer length scale, understanding of thermal transport in nanostructured materials is crucial for high performance devices. We are mostly concerned about semiconductors in which thermal transport is dominated by phonons having large wave vector and at room temperature, the mean free path (MFP) varies from 1nm to 100 nm. Phonon transport in nanostructures is often markedly different than it is in bulk materials. As the size of a structure decreases, its surface area to volume ratio increases, thereby increasing the importance of boundaries and interfaces. Additionally, at nanoscale the characteristic length of the structure approaches the phonon wavelength, and other phenomena such as dispersion relation modification and quantum confinement may arise and further alter the thermal transport. Table 1.1 shows different phonon dispersions and scattering processes that

Table 1.1: Phonon transport regimes-Length scale consideration and Scattering processes

Length Scale	Phonon Dispersion	Dominant Scattering Process
$L >> \mathrm{MFP}$	Bulk dispersion	Three-phonon Umklapp, Point defect
$\lambda << L \leq \mathrm{MFP}$	Bulk dispersion	Three-phonon Umklapp, Point defect, Boundary scattering
$\lambda \leq L << \mathrm{MFP}$	Modified dispersion with many phonon branches populated	Three-phonon Umklapp, Point defect, Boundary scattering
$L < \lambda$	Modified dispersion with only lowest branches populated	Ballistic transport

have dominant effects in various scales of length, L [4]. The phonon thermal wavelength is symbolized as λ.

According to Cahill *et al*. [5], the definition of temperature becomes very important in the scale of phonon mean free path and wavelength. Phonons in two regions of space have different distributions since they have difference in temperature. Scattering of phonons changes their distributions. The anharmonic scattering process occurs on the length of mean free path. Therefore a local region with a particular temperature should be larger than the phonon scattering distance. Low frequency phonons have long mean free path and vice versa for high frequency phonons. Hence for phonons that carry major portion of the heat, can be considered to have an average mean free path. It is quite difficult to define temperature within the scale of average phonon mean free path. But similar phenomenon might not happen across grain boundaries as the boundary provides a natural limit to the temperature region. There cannot be a temperature change within a grain or within a superlattice layer. Wave interference is also significant in nanostructures. At room temperature, all the phonon states in the Brillouin zone are engaged in the transport mechanism. But since the phonon thermal wavelength becomes comparable to length scale of nanostructures, Boltzmann equation cannot explain the phenomenon. Other theoretical approaches have to be considered at this point.

Thermal conductivity in the plane of thin films or along the length of nanowires is influenced by the increased phonon-rough boundary scattering [6] and this effect becomes pronounced when the structure dimension is on the order of phonon MFP. This phonon boundary scattering contributes to the structure thermal resistance, and thus is always detrimental to heat removal. In case of very thin films, phonon interference [7], alteration of phonon dispersion relation [8] and anharmonic interaction rates [9-11] as well as structural imperfections and impurities influence the thermal properties.

The spatial confinement of charge carriers and the resultant change in carrier density of states causes significant change in thermal properties of quantum well structures [12-14]. The quantum well structures that have boundaries with similar elastic and crystalline properties as those of the structures themselves, the phonon modes would extend through the boundaries and would behave like bulk materials. But, if the quantum well structures are free standing or embedded in rigid materials with markedly different elastic properties, then they would have phonon confinement effect. This effect has strong influence on phonon relaxation rates and in turn modifies the group velocity [15]. Thus the thermal transport in quantum well is different from that in bulk sample. Spatial confinement of phonons in nanostructures and thin films can strongly affect the phonon dispersion, modify phonon properties such as phonon group velocity, polarization etc. and influence the interaction of phonons with other particles.

Superlattice is periodically alternating layers of lattice matched crystalline materials that forms mini-brillouin zone in the direction of layering. The mini reciprocal lattice vectors associated with these mini zones give rise to mini Umklapp scattering. This contributes to the thermal resistance and influences the phonon transport and hence the lattice thermal conductivity of superlattice [9]. In the case of Si-Ge superlattice, a dramatic suppression of thermal transport is predicted in the perpendicular direction [16]. Total internal reflection confines the phonon modes in the superlattice and reduces the group velocity of phonons significantly. As a result of this acoustic mismatch, thermal conductivity is reduced at high temperature.

1.2 HIGH HEAT FLUX THERMAL MANAGEMENT

For decades, electronic industries have been shrinking transistor size in integrated circuits in order to achieve the yearly increases in speed and performance described by Moore's Law - chip performance will double every two years [17]. This device miniaturization trend has led to the evolution of new era of digital application and has yielded enormous gains in performance-cost ratio, computing power, portability and integration density. However, continuous scaling raises severe design challenges and concerns due to excessive power consumption and associated thermal problems. Elevated temperature as a result of high power density is a major contributor to reduced semiconductor reliability. If heat is not transferred at a rate equal to or greater than its rate of generation, junction temperature will rise and reduce mean time to failure (MTTF) for the devices. Device reliability has a direct impact on overall system reliability. At present the chip level power density has reached the order of 100 W/cm^2. This value may rise even further if the rates of integration and miniaturization continue to follow the International Technology Roadmap for Semiconductors (ITRS) guidelines [18]. Furthermore, nonuniform power density, resulting in localized hot spots is becoming more prevalent in integrated circuits. The temperature of hot-spots can exceed 100ºC [19]. While this is an issue with chip level circuit designers, device designers are now encountering the thermal problem at nanometer-length scales within individual transistors [20]. When the device feature size approaches the phonon mean free path, phonon boundary/rough interface scattering starts to dominate the Umklapp 3-phonon scattering and Rayleigh scattering. In bulk silicon, room temperature phonon MFP is around 43~300 nm according to different estimates and the transistor gate length is ~30-60 nm [21, 22]. When this length becomes significantly smaller than the dominant phonon wavelength, acoustic phonon confinement occurs [23] and modification of phonon spectrum splits acoustic phonon branches into quasi-optic phonon branches. Optical phonons have small group velocity and contribute little to the thermal conductivity. This might reduce the thermal

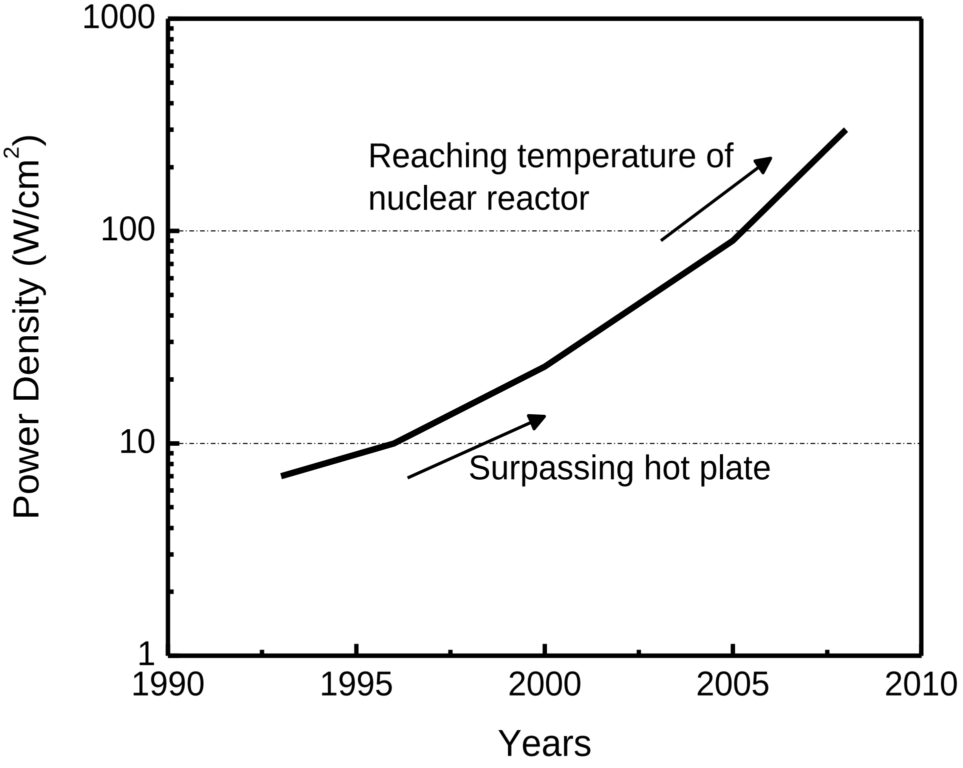


Figure 1.1: On-chip power density over the past twenty years [The data is after Ref [18]]

conductivity leading to higher operating temperature. The interaction of carrier electrons with the lattice vibrations can cause self-heating during operation of the devices. Integration of new materials with low thermal conductivity such as low-κ inter-layer dielectrics (ILD) and silicide, high thermal resistance due to increased number of interconnects together with the thermal boundary resistance in advanced device structures result in increased temperature rise within the devices. New technology of circuit fabrication like vertical integration of integrated circuits [three- dimensional (3-D) ICs] has enhanced chip performance, functionality and device packing density. But thermal effects are expected to be more pronounced because of high power densities and greater thermal resistance along heat dissipation paths in this technology [24-27]. Thermal management is thus of critical importance for 3-D designs. Excessive heating severely impacts the operations of a wide range of devices, like complementary metal-oxide silicon CMOS, high electron mobility transistors and photonic devices. In a CMOS device, the total power dissipation constitutes of three major sources:

$$P_{total} = P_{dynamic} + P_{short-circuit} + P_{static} \tag{1.5}$$

$P_{dynamic}$ denotes the dynamic or switching power component of the total power dissipation. It occurs during the transition of output signal of a logic cell. This component is the most dominant and expressed as $P_{dynamic} = 0.5 C_{load} V_d^2 f_{clock}\, \alpha$, where f_{clock} is the clock frequency, α is the expected number of output transitions in a clock period and C_{load} is the load capacitance. Short-circuit power, $P_{short\text{-}circuit}$ $(I_{short\text{-}circuit} \times V_d)$ is due to short-circuit current flow from the power supply to the ground and $I_{short\text{-}circuit}$ flows only briefly during the switching of gates. P_{static} is the static power or device leakage power. It is caused by the static current, also referred to as leakage current, drawn from the power supply. This current is mainly due to the direct gate current and the subthreshold conduction current [28]. Maintaining the clock frequency and same gate numbers, attempt has to be taken to reduce all three terms. Several techniques like transistor gating, power gating and sleep transistor insertion have been used to reduce the leakage power and the clock power dissipation [29, 30]. Reduction of the supply voltage reduces the chip total power consumption, which in turn reduces the chip temperature. But scaling of the supply voltage has limited applicability in case of current and future device technology since V_d cannot go below $4k_BT/q$ because of thermal fluctuations [4]. Here k_B is Boltzmann constant, T is temperature and q is electronic charge. So development of new technologies is required to solve this issue. The new advanced materials where we can engineer thermal properties provide us such opportunity. We also need to look into new physical design paradigms and tools to elevate the thermal problem.

Another source of heat generation is the power dissipation results from Joule heating (self-heating) due to the flow of current through the interconnects. Interconnect Joule heating can cause significantly high temperature rise even though it might be a small percentage of the total power dissipation in the chip. Because interconnects are located away from silicon substrate and heat sink by several layers of electrically insulating materials which have low thermal conductivity. The materials with low thermal conductivity help in reducing the noise in form of crosstalk to improve the performance of the circuits but give rise to considerable amount of thermal effects. Again, as the advanced integrated circuits (ICs) have evolved to deep sub-micron generations, the interconnect density is increased by decreasing the metal pitch and increasing the number of interconnect metal layers. The decrease in metal pitch causes the increase of both interconnect wiring resistance and capacitance, which lead to increased interconnect RC delay time and power dissipation. Temperature rise due to self-heating is given by

$$\Delta T_{self} = R_e I_{rms}^2 R_\theta \qquad (1.6)$$

where ΔT_{self} is the temperature rise of interconnect due to flow of current, R_e is the electrical resistance of interconnect and R_θ is the thermal impedance of the interconnect line to the substrate [28]. According to the International Technology Roadmap for Semiconductors (ITRS) projections, the volumetric heat generation rates approach to the limit of $P = j^2\rho \sim 3.3\times10^4$ W/mm^3 within interconnects assuming a current density, j=3.9 MA/cm^2 and a resistivity, ρ = 2.2 μΩ-cm [31-35]. Another phenomena called "electro-migration" occurs when the current density in metal interconnects becomes too high. This limits the maximum current density that can flow through the interconnect and severely degrades the reliability of the circuit. According to ITRS, at present, about fifty percent of microprocessor power is consumed by interconnects, with a projection that it will go up even further without changes in design philosophy [33]. That is why efficient thermal management becomes important not only for reliable and high performance conventional electronics but also for magnetic memory, logic elements with alternative state variables, three-dimensional and reconfigurable architectures and optoelectronic devices.

Chapter 2

Graphene and Thermal Conductivity Measurement

2.1 THERMAL CONDUCTION IN CARBON BASED MATERIALS

Aggressive scaling and complex device design cause increase of dissipation power density, switching speed and thermal resistance of the multi-layer structures; also formation of the local hot spots inside the chips. Thus, thermal management in electronic circuits is becoming an increasingly important issue. The thermal conduction of nanometer materials plays a fundamentally critical role that controls the performance and stability of nano/micro devices. Understanding of the thermal properties in novel materials and materials at nanometer scale are thus essential for thermal management of CMOS and beyond-CMOS heterogeneous and hybrid type devices. A wide variety of carbon materials like diamond, diamond-like carbon, polycrystalline diamond, tetrahedral amorphous carbon, graphite, carbon nanotubes, graphene etc. are possible candidates in this regard since they cover a large range of thermal conductivity. The thermal conductivity of carbon materials depends on the sp^3/sp^2 content, structural disorder, grain structure and size, thickness of the films and dimensionality of the material systems. The bulk of heat in carbon materials is carried by lattice vibrations, i.e. acoustic phonons.

The three dimensional form of carbon, diamond has remarkably high Young's modulus, record high thermal conductivity, chemical inertness, high mobility of charge carriers and high electron emission at low fields [36-38]. Crystalline diamond is known to have the highest thermal conductivity among all bulk solids. At room temperature, it varies between 1000 - 2200 $Wm^{-1}K^{-1}$ [39, 40] depending on the quality. These properties make diamond a preferable candidate for heat removal application. However, diamond's scarcity and hence cost makes this unappealing. Graphite is a layered material formed by stacks of two dimensional sheets of carbon atoms. It has one of the highest in plane thermal conductivity (2000 $Wm^{-1}K^{-1}$) [41]. But the thermal conductivity along c-axis is smaller compared to that along graphite basal plane [42, 43]. Again carbon nanotube (CNT) is a unique one dimensional form of carbon [44] which has high thermal conductivity (ballistic conduction) along the tube. It is predicted that experimentally determined room temperature value of thermal conductivity for an individual multiwall carbon nanotube (MW-CNT) is 3000 $Wm^{-1}K^{-1}$ [45] and 3500 $Wm^{-1}K^{-1}$ for an individual single-wall carbon nanotube (SW-CNT) [46]. Theoretical calculations of the thermal conductivity of CNTs mostly support the experimental results for individual CNTs, although some discrepancy exists. These values exceed those of the best bulk crystalline thermal conductor, diamond. Despite the high thermal conductivity, these materials are not well suited for integration with CMOS, instead newly discovered material graphene can be considered in this regard. The extracted near-room temperature thermal conductivity is on the high end of the values reported for CNTs or exceeds and was recently measured to be between (4.84±0.44) $\times 10^3$ to (5.30±0.48) $\times 10^3$ $Wm^{-1}K^{-1}$ [47]. This extremely high thermal conduction property of graphene allows it to be used for heat removal. The planer geometry of graphene provides more exposed contact to heat sink and much lower contact thermal resistance as compared to CNT. Such excellent properties allow graphene for better thermal management in the nanoelectronic devices and circuits.

2.2 UNIQUE CHARACTERISTICS OF GRAPHENE

New material systems must be investigated for possible applications in electronics in order to sustain the rapid progress in integrated circuits (ICs) and information technology as projected by Moore’s law. Such discovery gives a new era to solve old problems as well as new ones. Graphene is a two-dimensional lattice of sp^2 bonded carbon atoms arranged in a hexagonal sheet structure [48, 49] as shown in Figure 2.1. The dashed rhombus in Figure 2.1 (a) represents the unit cell of graphene in real space. This is constructed by the primitive vectors $\mathbf{a_1}$ and $\mathbf{a_2}$. Each unit cell consists of two atoms **A** and **B**, indicated by red and blue colors. The shaded hexagon represents the Wigner Seitz cell of the extended rhombus lattice which through translation encloses two atoms per unit cell. This represents the Brillouin zone of graphene in reciprocal space. The nearest neighbor *C-C* distance is 1.421 Å where as the length between the lattice spacing is 2.46 Å. This creates a strong in-plane bonding. Figure 2.1 (b) represents the reciprocal

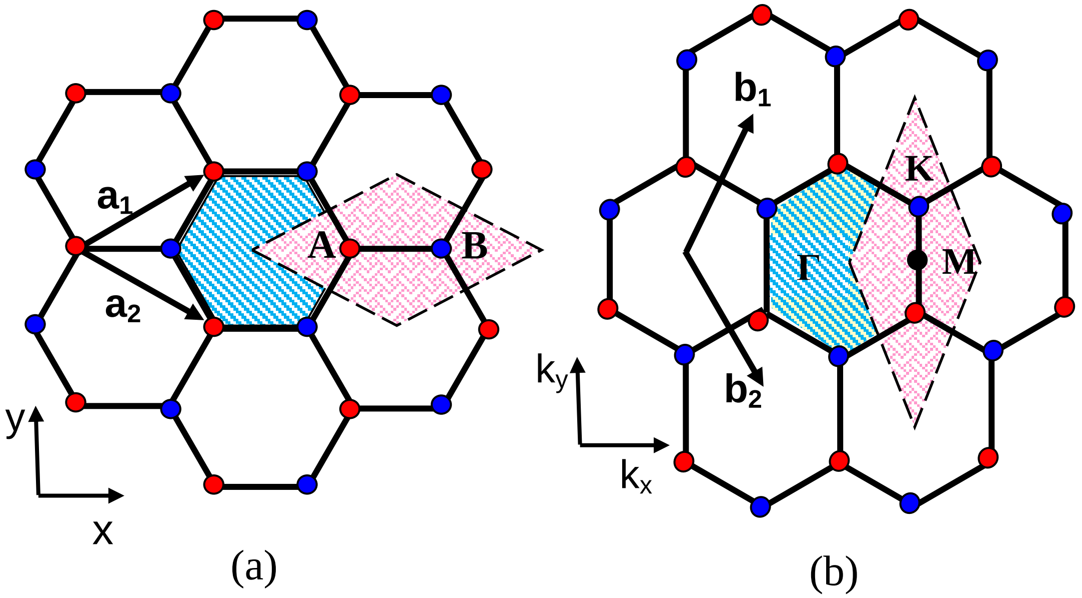


Figure 2.1: Unit cell of graphene lattice in (a) Real space and (b) Reciprocal space. High symmetry points, **Γ**, **K**, and **M** are all shown in the figure.

lattice vectors $\mathbf{b_1}$ and $\mathbf{b_2}$ constructing the unit cell of graphene in reciprocal space. The high symmetry points **Γ**, **K** and **M** are marked in the figure and the phonon dispersions are obtained along the lines connecting these points [50, 51]. Such structure is a building element for any graphitic material; it can be enfolded into 0-D large fullerenes, rolled into 1-D carbon nanotubes or can also be stacked up to form 3-D bulk graphite. Graphene possesses several unique properties that make it a very promising material for electronic devices and circuits:

A) In most conductors and semiconductors electron transport can be described by non-relativistic quantum equations. But in graphene electrons and holes behave like relativistic particles [52]. The E-k relation is linear at low energies near six corners of the

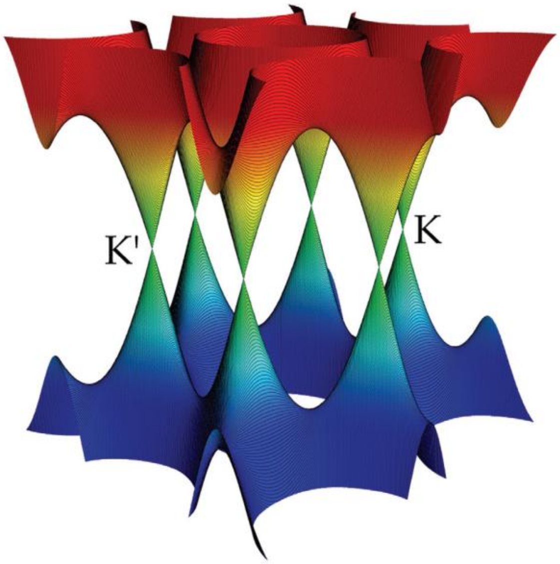


Figure 2.2: Band structure of graphene. The conductance band touches the valence band at the **K** and **K'** points [Figure is adapted from Ref [53]]

two-dimensional hexagonal Brillouin zone. That leads to zero effective masses for electrons and holes that can be described by the Dirac equation for spin 1/2 particles.

B) Experimental results and simulations suggest that graphene has very high values of electron mobility at room temperature. Intrinsic mobility can reach the value as high as 2 x 10^5 $cm^2V^{-1}s^{-1}$ at a carrier density of 10^{12} cm^{-2} [54]. For such a case, the corresponding resistivity of the graphene sheet would be 10^{-6} Ohm-cm, which is slightly less than the resistivity of silver (1.6 x 10^{-6} Ohm-cm), the least resistive metal. The magnitude of an electron mobility of graphene exceeds that of InSb (7.7 x 10^4 $cm^2V^{-1}s^{-1}$) and is comparable to an electron mobility of carbon nanotubes (1 x 10^5 $cm^2V^{-1}s^{-1}$).

C) A single layer graphene has an opacity which is unexpectedly high for just one atomic layer. The white light absorption is

$$\pi\alpha = 2.3\ \%, \tag{2.1}$$

where, α is the fine-structure constant [55, 56].

D) Graphene is a very strong and rigid material. If several layers of graphene are suspended over cavities, graphene sheets are held together by Vander Waals forces and one can measure mechanical properties of the suspended sheet using an atomic force microscope [57]. The spring constant and Young's modulus of graphene were found to be 1 – 5 N/m and 0.5 TPa, correspondingly. Such remarkable elastic properties could lead to utilization of graphene as a material for sensors and resonators.

E) Graphene might be the first observed two-dimensional crystal. However, it is still debated whether such a statement is true. Mermin-Wagner theorem states that continuous symmetries cannot be spontaneously broken at finite temperature in one- or two-dimensional theories [58-60]. In other words, a two-dimensional crystal cannot remain ordered in a three-dimensional environment, because of long wavelength fluctuations. The theorem leads to an assumption that a large two-dimensional structure will eventually fold or collapse into a more stable three-dimensional crystal. Graphene has a tendency to ripple [61], if suspended. Such tendency, in part, supports the Mermin-Wagner theory. Proponents for a truly two-dimensional structure of graphene argue that the Mermin-Wagner theorem is applicable for infinite structures, or, at least, for layers with very large sizes, but finite-size graphene layers can remain stable as two-dimensional crystals.

F) In the presence of a magnetic field graphene shows an anomalous quantum Hall effect [49]. The Hall conductivity of a single layer graphene is

$$\sigma_{xy} = \mp \frac{4e^2(N + \frac{1}{2})}{h}, \tag{2.2}$$

where h is the Plank constant, e is the elementary charge, and N is the Landau index level. The factor 4 comes from double valley and double spin degeneracies. Above equation shows that the sequence is shifted by 1/2 from the standard.

Contrary to single layer graphene, bilayer graphene displays the quantum Hall effect but the sequence is standard:

$$\sigma_{xy} = \mp \frac{4e^2 N}{h} \tag{2.3}$$

G) In presence of very intense, time varying magnetic fields the conductivity of graphene oscillates. This is so-called Shubnikov-de Hass effect. The longitudinal resistance of graphene is at maximum [62] for every Landau index value N. This is an opposite to many metals, since they show the minimum of resistance for the integral Landau values N. A possible explanation of such phenomenon could be Berry phase that occurs due to zero effective masses of the carriers near Dirac points [63]. Although E-k relation manifests zero carrier masses, studies of Shubnikov-de Hass oscillations as a function of temperature reveals that the carriers in graphene have non-zero cyclotron masses [62].

Unique mechanical and electromagnetic properties make graphene a very promising material for a variety of high-tech applications. Particularly, due to a very high conductivity, graphene can be used to fabricate ballistic field-effect transistors and integrated circuits. Graphene can be utilized in single molecule gas sensors; absorption of just one molecule drastically changes a local electrical resistance. Nanoribbons with specific electrical properties can be made of graphene to be used in interconnects. High optical transparency, mechanical strength and flexibility allow use of graphene in transparent conducting electrodes such as liquid crystal displays, organic photovoltaic cells and touch screens.

2.3 PREPARATION OF GRAPHENE

Since graphene is only a single layer of carbon atoms, it was predicted that it could not be existed at finite temperature. In 2004, this thinnest material was developed by peeling off graphite using adhesive tape by researchers in Britain [48]. This method is called micro-mechanical exfoliation. This method is much easier than other methods as it does not require any sophisticated equipment and more importantly it yields high quality graphene flakes. Another way of synthesis graphene is by epitaxial growth on SiC substrate which was invented by researchers of USA [64].

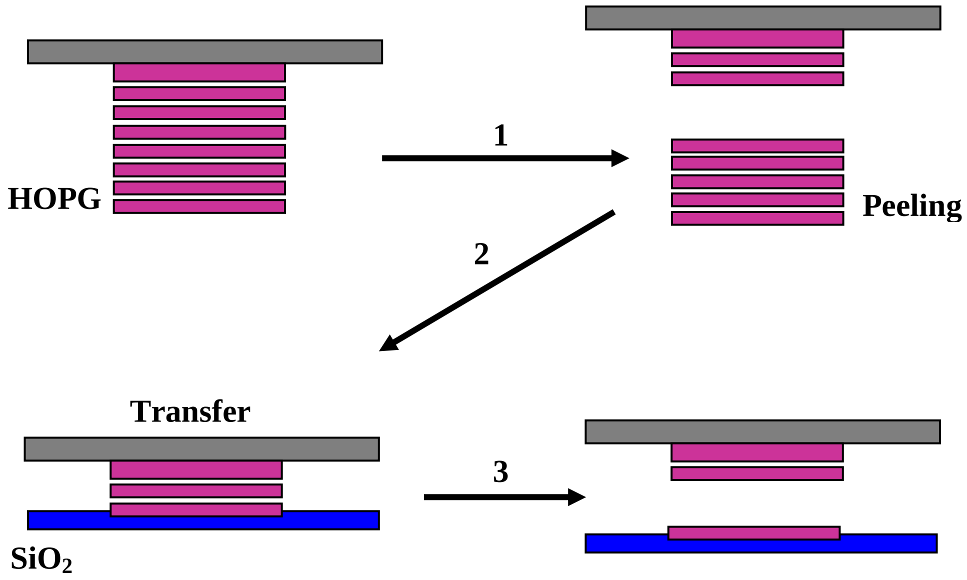


Figure 2.3: Micro-mechanical exfoliation method to prepare single layer graphene from bulk graphite.

Simplified method of making graphene starts from bulk graphite like HOPG, Kish, HPHT. Figure 2.3 shows the steps involved in micro-mechanical exfoliation method to prepare single layer graphene from bulk graphite. Clean environment during production process is important for good quality of graphene. Attach a HOPG flake to about six inches of adhesive tape with tweezers and press it down carefully and peel the tape apart slowly enough so that graphite cleaving smoothly in two. Repeat the step above for several minutes until the graphite flakes spread a larger area on the tape. Then, carefully lay the tape with graphite flakes onto a small silicon dice and press the tape gently for a few minutes. This silicon has silicon dioxide layer of 300 nm on the top, which helps to find graphene under white light optical microscope. The final step is to

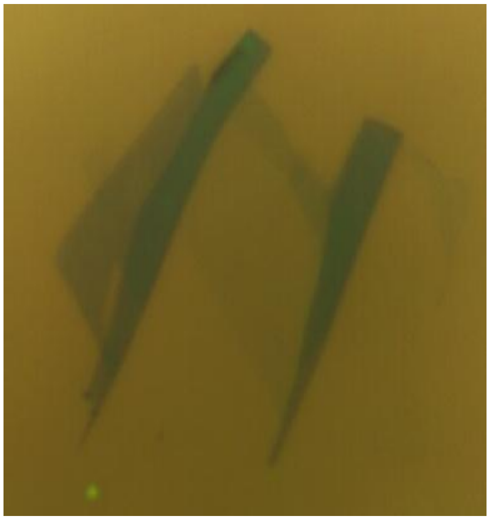


Figure 2.4: Optical microscopy image of exfoliated graphene flake on Si/SiO_2 substrate (The image is courtesy of M. Z. Hossain)

peel off from silicon dice. Then it is ready to find graphene under optical microscope. Figure 2.4 shows the image of graphene flake on Si/SiO_2 substrate under optical microscope.

2.4 METHODS OF THERMAL CONDUCTIVITY MEASUREMENTS

Determination of the thermal conductivity is of great interest because it contributes to the performance of thermoelectric materials and thermal management in electronic circuits and contains information about the microstructure of the material being studied. Thermal conductivity depends on material type as well as many properties like structure, density, porosity, electrical conductivity etc. of the material. This property also exhibits strong dependence on temperature and pressure. Because of these large variations in thermal transport properties, a number of different experimental techniques have been developed for different materials. The broad division lies in whether the mode of measurement is steady state or non-steady-state. The signal analysis in steady state method is straight forward since the temperature of the material that is measured does not change with time but it takes a well-engineered experimental setup. On the other hand, non-steady-state method can be performed more quickly; since it does not require the signal to obtain a constant value but the mathematical analysis of the data is in general more difficult. These two classes include a number of measurement techniques and depending on the materials to be tested - metal, non metal and composite, size of samples, conductivity range, temperature range, test environment, accuracy; method of thermal conductivity measurement is chosen.

One example of the steady state methods is the Guarded Heat Flow Meter technique, which is mostly used for the poorly conducting materials like glass, ceramic coated metals and composite ceramics. In this operation, a small piece of test specimen is sandwiched under a uniform load between two heated surfaces controlled at different temperatures. Temperature sensors fixed directly in the surfaces are used to measure the surface temperatures. As heat flows from the upper surface through the sample to the lower surface, an axial temperature gradient is established in the stack. A guard furnace, maintained at mean temperature of the plates, surrounds the test stack in order to reduce the effect of heat transfer across the edges of the sample. By measuring the temperature difference across the sample along with the output from the heat flux transducer, thermal conductivity of a sample of known thickness can be determined [65-67].

Thermal contact resistance usually causes an inherent error in steady state methods. Because of the interface influence between a thermo couple and a sample surface, a negative systematic error occurs during the measurement which cannot be compensated by the method itself. On the contrary, transient or non-steady-state methods like Transient Plane Source (TPS) technique can circumvent such errors caused by the influence of thermal contact resistance. TPS technique can be used for measuring various kinds of materials, such as solids, powder, liquid, paste and film etc. and it covers a thermal conductivity range of 4-5 orders of magnitude [68-70].

The general theory of transient plane source technique is followed by proposed approximations for arrangements, which can be referred to as “hot square” and “hot disk”. A nickel wire which also functions as a resistance thermometer is supplied power through an electric circuit. The voltage drop across the wire is used to determine the temperature rise. The slope of temperature increase versus time gives an estimate of the thermal conductivity of the medium [71]. The measurement of thermal conductivity using TPS method utilizes a thin disk-shaped temperature dependent resistor simultaneously as the temperature sensor and as the heat source. The sensor is sandwiched between two specimen halves and a sufficiently large direct current is passed through the sensor to increase the sensor temperature by about 1-2K [69]. Due to the temperature increment, the resistance of the sensor will change and there will be a corresponding detention in

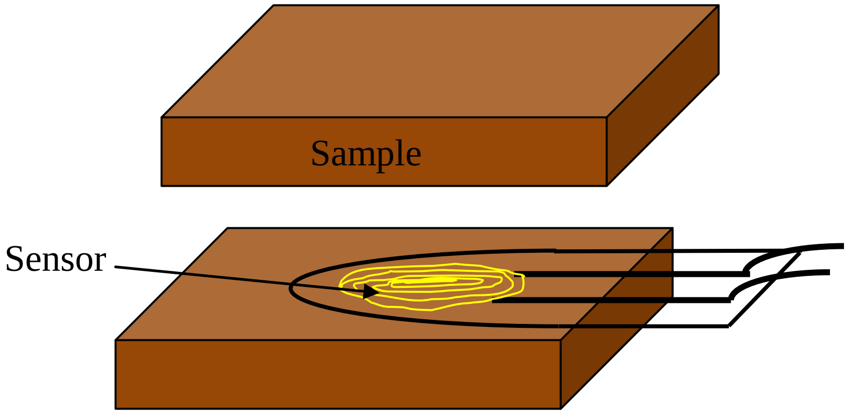


Figure 2.5: Schematic of Transient Plane Source (TPS) technique for measuring thermal conductivity.

voltage drop over the sensor. By recording the voltage variation and the current variation over a certain time period from the onset of the heating current, it is possible to obtain precise information on the heat flow between the sensor and the test specimen.

3ω (3-omega) method uses a narrow-band detection technique and therefore gives a relatively better signal-to-noise ratio. This is basically an ac technique like transient plane source technique. However, the main difference is that TPS functions in the time domain, where as the 3ω method moves the measurement to the excitation frequency domain. Earlier there were other frequency domain techniques like the a.c. calorimetry method [72] which used separate heaters and thermometers. However, Cahill *et al*. [73], for the first time discussed the 3ω technique for amorphous materials and elimination of

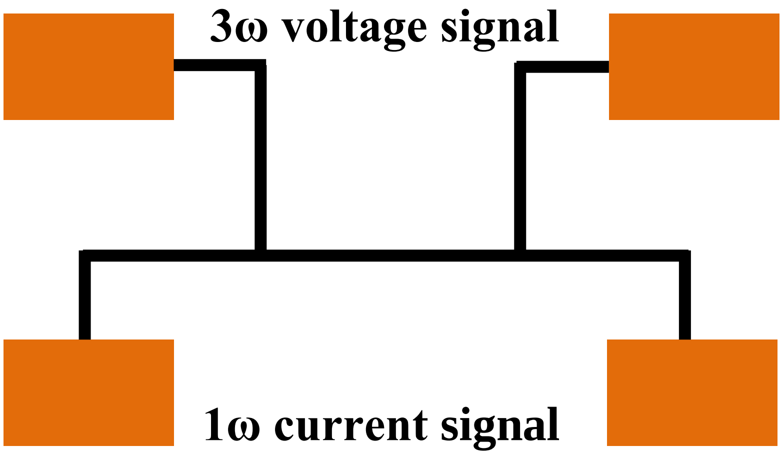


Figure 2.6: Schematic of the 3ω heater/thermometer element patterned on top of the sample.

blackbody radiation error thereof. Later, Cahill used this technique for measuring thermal conductivity of dielectric solids [74]. This is achieved through the lock-in amplifier technology. A frequency synthesizer supplies the driving current of angular frequency ω to an amplifier that heats the sample at 2ω. The heating produces the temperature oscillation. The metal line serves as a thermometer and resistance of the line is a function of temperature. The resistance oscillation at 2ω multiplied by the excitation current at ω produces a voltage oscillation at 3ω. The amplitude of this oscillation is measured by the lock-in amplifier. A frequency tripler provides a reference signal at 3ω. By measuring the third harmonic signal at two different frequencies, f_1 and $f2$, we obtain the thermal conductivity, K [73].

The flash method is another well-known transient technique for measurement of the thermophysical properties of various kinds of solids, powders and liquids. Easy sample preparation, fast measurement times and high accuracy are only some of the advantages of this non-contact, non-destructive testing technique.

The Laser Flash technique is based on the measurement of the thermal transient of the rear surface of the sample when a pulsed laser illuminates the front and it avoids interferences between the thermal sensor and the heat source [75, 76]. The physical model of the Laser Flash measurement supposes to have a single pulsed heat source

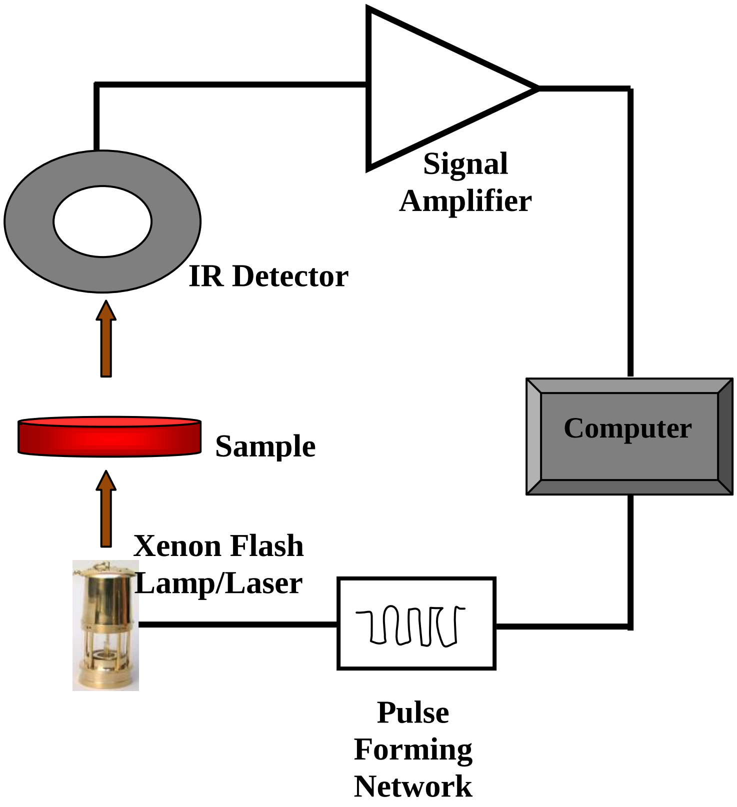


Figure 2.7: Schematic of “Laser Flash” technique for measuring thermal diffusivity.

(delta like), for example a laser shot, on the sample front surface. The study of the thermal transient of the rear surface provides the desired thermal information. The temperature of the rear face is measured with an infrared detector and it can be expressed mathematically as a function of several variables that are grouped into dimensionless parameters. These variables include sample geometry, thermal diffusivity and heat loss from the sample. Thermal diffusivity can be determined by comparing the measured data with the appropriate mathematical model which was first developed by Parker *at el* [75].

Specific heat is measured by comparing the actual temperature rise of the sample to the temperature rise of a reference sample with a known specific heat under the same conditions. Measurement of the thermal diffusivity and specific heat allows the calculation of the thermal conductivity, with an additional measurement or knowledge of the bulk density of the sample material [77].

But such conventional techniques for measuring the thermal conductivity are not well suited for single layer graphene (SLG). For instance, the 3ω method is good for But such conventional techniques for measuring the thermal conductivity are not well suited for single layer graphene (SLG). For instance, the 3ω method is good for measuring the cross-plane thermal conductivity and requires a substantial temperature drop over the thickness of the examined film. Since graphene is of one atomic layer thick and the expected thermal conductivity is very high, it does not satisfy such a requirement. Also, TPS technique and laser flash are suitable for samples of thickness around few microns. The direct thermal-bridge measurements of graphene are possible in principle but the

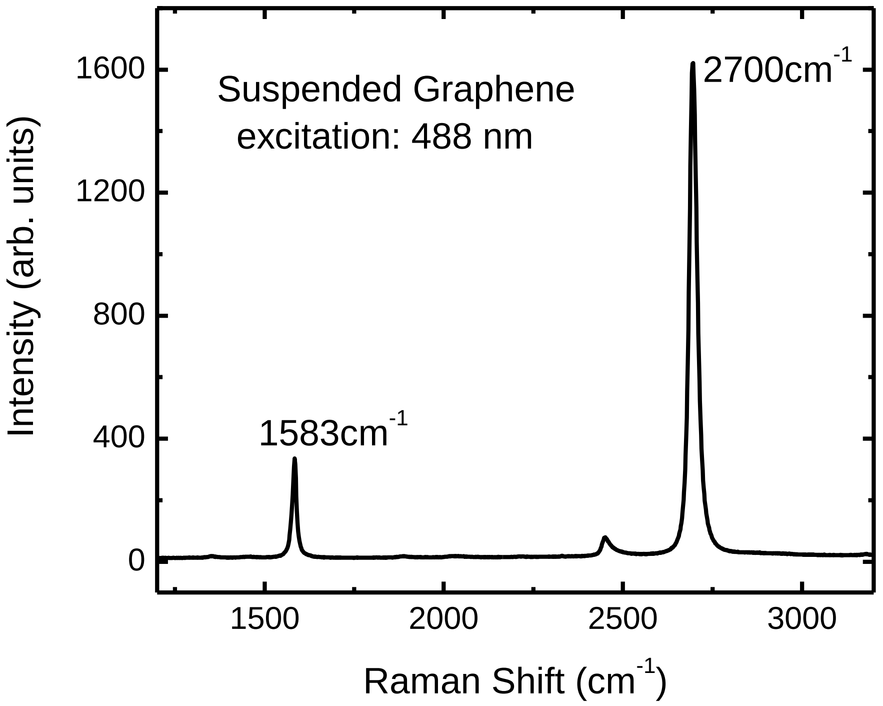


Figure 2.8: Raman spectrum of suspended single layer graphene showing the *G* peak and 2D band features characteristic for single layer graphene.

technology is very challenging. For these reasons, an unconventional technique was developed on the basis of confocal micro-Raman spectroscopy [47]. Graphene has clear signatures in Raman spectra. The SLG flakes connected to multilayer graphenes were selected using the Raman spectroscopy and 2D band deconvolution. Figure 2.8 shows that the suspended graphene flake has the Stokes *G* peak at 1583 cm^{-1} and a symmetric 2D band around 2700 cm^{-1}, which is consistent with the reported SLG spectra [78-82].

2.5 EXPERIMENTAL APPROACH FROM MEASURING THERMAL CONDUCTIVITY OF GRAPHENE

In the experiment a single layer graphene was exfoliated from bulk graphite [47, 83]. Using Raman spectrometer the graphene layer, placed on a silicon substrate covered with a film of SiO_2, was excited with visible (488 nm) laser light and the backscattering data were collected [82]. A cold-hot cell operated using liquid nitrogen was able to control the temperature of the sample, which was varied from -190^0C to 100^0C. The position of the *G* peak in the spectrum was measured and found to be changing from ~1584 cm^{-1} to ~1578 cm^{-1}. The resulting *G* peak position distribution was fitted with the user-defined linear function

$$\omega = \omega_0 - \chi T \, , \qquad (2.4)$$

where the temperature coefficient $\chi = 0.016\ cm^{-1}K^{-1}$.

The very fact that the *G* peak position depends on temperature allowed designing and carrying out the experiment during which the thermal conductivity of graphene was measured for the first time (see Figure 2.9). In that experiment a trench with the width of ~2 – 5 μm was made on the Si/SiO_2 substrate by reactive ion etching. The thickness of SiO_2 layer (the depth of the trench) was ~300 nm. A single layer graphene flake was placed across the trench. Then the laser light from Raman spectrometer was focused in the middle of the suspended flake with the spot size of about 0.5 – 1.0 μm. Large graphitic pieces were placed on top of the graphene flake at the distance of 10 μm from

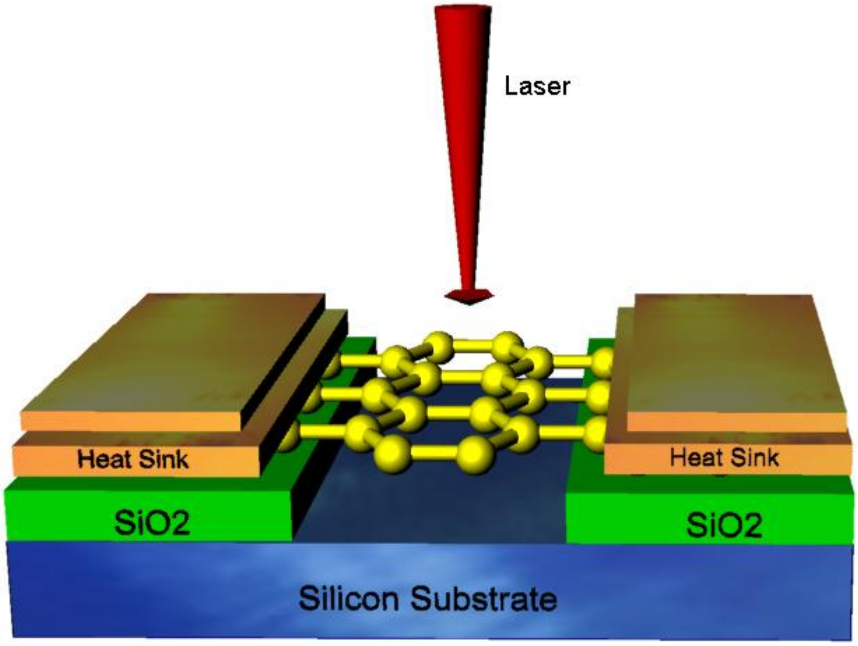


Figure 2.9: Experimental setup for measurement of thermal conductivity of graphene.

the trench edges. Those graphitic pieces acted as heat sinks. The temperature of the heat sinks was constant and equal to ambient room temperature. Power from the laser light was dissipated in the flake. Due to low thermal conductivities of air and SiO_2 it was reasonable to assume that the heat dissipation into the air and SiO_2 was negligible, so the heat was propagating laterally within the flake from the laser spot toward the heat sinks. Excitation power was controlled and varied, and the *G* peak position of the Raman spectrum was measured in regard to a particular value of the power. Thus the *G* peak position was extracted as a function of the power dissipated in graphene.

Heat transfer in graphene occurs through conduction. Conduction is defined as a spontaneous transfer of thermal energy from a region with high temperature to a region with low temperature. Direct molecular (or atomic) interactions are involved in the heat conduction either within the same medium or between different media if they are in physical contact. The heat transfer in graphene is mostly due to acoustic phonons (atomic vibrations).

The law of heat conduction, also known as a Fourier's law, defines the time rate of heat transfer as

$$\frac{\partial Q}{\partial t} = -K \oint \overrightarrow{\nabla T} . \overrightarrow{dS} \ , \tag{2.5}$$

where $\frac{\partial Q}{\partial t}$ is the heat transfer rate, i.e. amount of heat transferred per unit time [W], T is the temperature [K], S is the surface through which the heat is flowing [m^2], and K is the thermal conductivity [$Wm^{-1}K^{-1}$].

The Fourier's equation means that the heat transfer rate is proportional to the negative gradient in the temperature and to the area of the surface through which the heat is flowing. That surface is normal to the temperature gradient.

This allows us to write the heat conduction equation as

$$\frac{\partial Q}{\partial t} = -K \ \frac{dT}{dx} \vec{x}.\vec{x} \oint dS \ , \tag{2.6}$$

where x is the magnitude of the unit vector normal to the surface through which the heat is flowing. The minus sign in the equation indicates that the temperature drops along the direction of the heat flow. We drop the minus sign from further equation transformations.

To extract the thermal conductivity of single layer graphene the flake was thought to be a rectangle. The axes of Cartesian coordinate system are orthogonal to the surfaces of the flake. Thus

$$\frac{\partial Q}{\partial t} = K \frac{dT}{dx} \int_0^W dy \int_0^h dz \quad , \tag{2.7}$$

or

$$P = K \frac{dT}{dx} Wh \quad , \tag{2.8}$$

where $P = \frac{\partial Q}{\partial t}$, which is equal to the heat power dissipated in the flake (or the heat transfer rate), W is the width of the flake [m], h is the thickness of the flake [m], and Wh is the cross-sectional area of the flake [m^2].

If the diameter of the laser sport is comparable to the width of the graphene flake, to simplify the solution one can approximate the shape of the heat source into an infinitesimally thin line, the length of which equals the width of the modeled flake. A graphene layer has a thickness of one carbon atom plane (~0.35 nm). Since it is rather thin, heating the top plane of the flake with the hot line can be seen as resulting in creating within the flake a uniformly hot surface normal to the flake's plane. The length of this hot surface is equal to W and the width of this surface is equal to 0.35 nm.

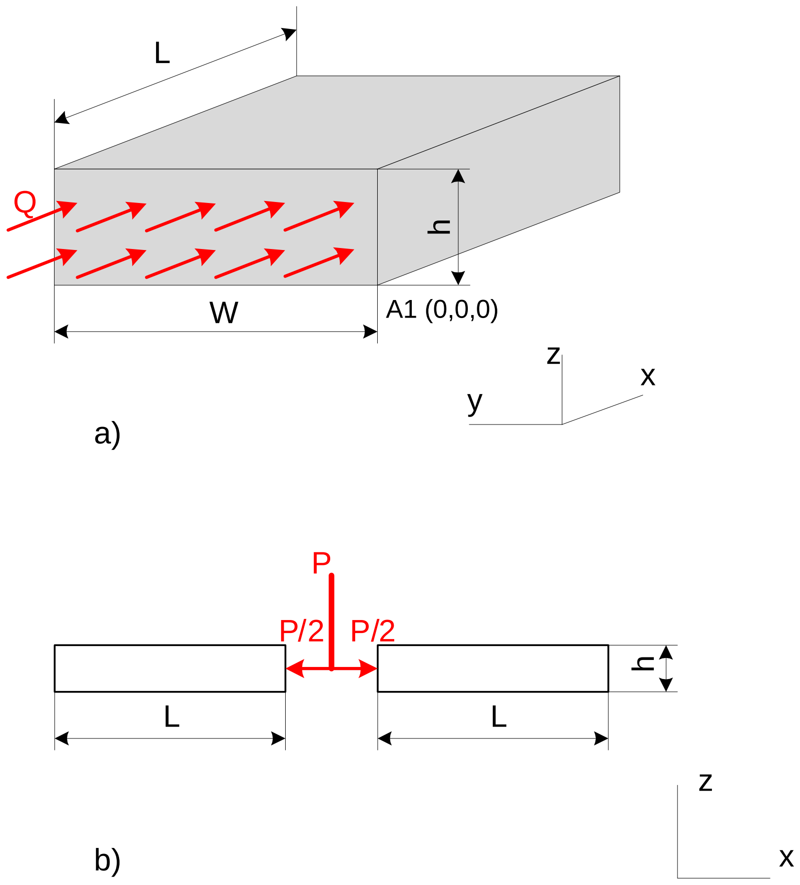


Figure 2.10: a) Half-flake of single layer graphene. b) Representation of the heat flow in graphene as heating two adjacent identical half-flakes.

If one cuts imaginarily the rectangular flake along the line of the heat source into two pieces (half-flakes), for each piece the heat can be seen as flowing into the half-flake through surfaces (intake surfaces). These surfaces both pass through three points: $A_1 = (0, 0, 0)$, $A_2 = (0, W, 0)$ and $A_3 = (0, 0, h)$ (see Figure 2.10). The plane that passes through the points $A_4 = (L, 0, 0)$, $A_5 = (L, W, 0)$ and $A_6 = (L, 0, h)$ for one half-flake and the plane that passes through the points $A_7 = (-L, 0, 0)$, $A_8 = (-L, W, 0)$ and $A_9 = (-L, 0, h)$ for the other half-flake are connected to heat sinks, so the temperatures of those planes (sink planes) are constant (note that $2L$ is the length of the flake). All other surfaces of the half-flakes are assumed to be perfectly insulated from the surroundings.

If one considers the half-flake, the fact that

1) the half-flake has a rectangular shape,

2) one of the surfaces is thermally connected to a heat sink, and

3) all surfaces, except for the intake and sink planes, are thermally insulated leads to considering the temperature in the half-flake as linearly changing, thus we can replace the derivative $\frac{dT}{dx}$ with $\frac{\Delta T}{\Delta x}$ and write

$$\frac{P}{2} = K \frac{\Delta T}{\Delta x} Wh \tag{2.9}$$

In the equation (2.9) the dissipated power P is divided by 2, since the suspended graphene flake was heated in the middle and we considered the heat transfer as two equal and opposite flows going through the identical adjacent half-flakes (note that $\Delta x = L$). Changes in the dissipated power result in changes in the temperature of the intake surface. The temperature of the sink surface remains constant at 300 K. Thus for a particular value of the dissipated power there is one unique temperature of the intake surface:

$$\frac{P_1}{2} = K \frac{\Delta T_1}{\Delta x_1} Wh = K \frac{T_1 - T_s}{L} Wh \ , \tag{2.10}$$

$$\frac{P_2}{2} = K \frac{\Delta T_2}{\Delta x_2} Wh = K \frac{T_2 - T_s}{L} Wh \ , \tag{2.11}$$

where T_s is the temperature of the heat sink.

We can express the change in the power as

$$P_2 - P_1 = K \frac{2(T_2 - T_1)}{L} Wh \quad , \tag{2.12}$$

and the thermal conductivity as

$$K = \frac{L(P_2 - P_1)}{2Wh\,(T_2 - T_1)}, \tag{2.13}$$

The G peak position of Raman spectrum was found to be linearly dependent on temperature

$$\partial T = \frac{\partial \omega}{\chi} \quad , \tag{2.14}$$

where $\delta\omega$ is the shift in G peak position in Raman spectrum [m^{-1}], χ is the temperature coefficient [$\mathrm{m}^{-1}\mathrm{K}^{-1}$].

This allows us to write the thermal conductivity of the rectangular shape graphene flake as

$$K = \left(\frac{L}{2Wh} \right) \bullet \chi \left(\frac{\partial \omega}{\partial P} \right)^{-1} , \tag{2.15}$$

During the experiment the power variations δP were relatively small. The G-peak position in the Raman spectrum was shifted linearly depending on how the dissipated power was changing. For the Raman spectrum with the excitation wavelength of 488 nm, the spectrometer power was varied from 0.5 mW to 4 mW. The *G*-peak position was found to be

$$\omega = \omega_0 - \theta P_D\,, \tag{2.16}$$

where $\theta = 1.226$ cm^{-1}(mW)$^{-1}$ and P_D is the power of the spectrometer (detector).

Only a fraction of P_D can be dissipated in graphene:

$$P = \eta P_D, \tag{2.17}$$

where $\eta = 0.11 - 0.13$. This was found through spectrometer calibrations.

Finally the thermal conductivity of the rectangular shaped single layer graphene flake can be expressed as

$$K = \left(\frac{\eta L}{2Wh}\right) \bullet \chi \left(\frac{\partial \omega}{\partial P_D}\right)^{-1}, \tag{2.18}$$

or

$$K = \left(\frac{\eta L}{2Wh}\right) \bullet \chi \theta^{-1}, \tag{2.19}$$

Equation (2.19) defines the thermal conductivity of the flake which has a shape of a rectangle. In reality, of course, it is hard to make such a sheet of graphene. Measurements on several samples, whose shapes resembled to rectangles, were done. Both parameters $\chi = 0.016$ cm^{-1}K^{-1} and $\theta = 1.226$ cm^{-1}(mW)$^{-1}$ are constant, so *L*, *W* and *h* could be varied. The single layer graphene thermal conductivity was found to be in the range of 3080 $Wm^{-1}K^{-1}$ to 5300 $Wm^{-1}K^{-1}$. From these results the average temperature of a graphene flake was estimated to be ~370 – 400 K.

Chapter 3

Finite Element Analysis

3.1 THE NEED FOR NUMERICAL SOLUTIONS

Under assumptions of diffusive thermal transport in the flake, flake with rectangular shape and comparable sizes of the laser spot and the width of the flake, the thermal conductivity of single layer graphene was determined to be in the range from 3080 $Wm^{-1}K^{-1}$ to 5300 $Wm^{-1}K^{-1}$. But it is not always possible to mechanically exfoliate graphene flake of rectangular shape. It might deviate from a perfect rectangle. Different cutting tools can be used to serve this purpose but these might damage or degrade the quality of the sample. And also for experimental purpose, graphene flake with any shape and size can be required. Again the intensity of laser beam is distributed according to Gaussian distribution. That is why numerical solution of heat diffusion equation is necessary in order to extract thermal conductivity of suspended graphene flake of arbitrary shape and size. The thermal conduction in graphene flake was simulated using the finite element method. It helps to investigate how the thermal transport is influenced by different parameters and provides a necessary input for next experiments on heat conduction in graphene structures. Moreover the simulation of heat propagation in graphene electronic devices and in conventional semiconductor device structures with graphene heat spreaders allows us to study the feasibility of the graphene application for high-heat-flux thermal management.

3.2 SOFTWARE USED IN SIMULATIONS

We simulated the heat transfer in graphene using COMSOL Multiphysics software package [84]. COMSOL package is a finite element analysis tool and it has application-specific modules for various physics phenomena: AC/DC Module, Acoustic Module, Structural Mechanics Module, Heat Transfer Module and others. The finite element analysis technique is a numerical method for finding approximate solutions of partial differential equations. The solutions are mostly based on dividing the simulated object into a large set of very small components and linearizing the differential equations within each of the components.

The finite element method is a numerical procedure for obtaining solutions to boundary-value problems, for finding approximate solutions of partial differential equations (PDE) as well as of integral equations. The principle of the finite element method is to replace an entire continuous domain by a number of subdomains in which the unknown function is represented by simple interpolation functions with unknown coefficients Thus, the original boundary-value problem with an infinite number of degrees of freedom is converted into a problem with a finite number of degrees of freedom, or in other words, the solution of the whole system is approximated by a finite number of unknown coefficients. Then a set of algebraic equations or a system of equations is obtained by applying the Ritz variational or Galerkin procedure, and finally, solution of the boundary-value problem is achieved by solving the system of equations. Therefore, a finite element analysis of a boundary-value problem should include the following basic steps:

1. Subdivision of the domain or domain discretization
2. Selection of the interpolation functions
3. Formulation of the system of equations
4. Solution of the system of equations

1. Domain discretization

The discretization of the domain, say **Ω**, is the first and perhaps the most important step in any finite element analysis because the manner in which the domain is discretized will affect the computer storage requirements, the computation time, and the accuracy of the numerical results. In this step, the entire domain is subdivided into a number of small domains, denoted as $(e = 1,2,3,...,M)$, with M denoting the total number of subdomains. These subdomains are usually referred to as the elements. For a one-dimensional domain which is actually a straight or curved line, the elements are often short line segments interconnected to form the original line [Figure 3.1 (a)]. For a two-dimensional domain, the elements are usually small triangles andrectangles [Figure 3.1 (b)]. The rectangular elements are, of course, best suited for

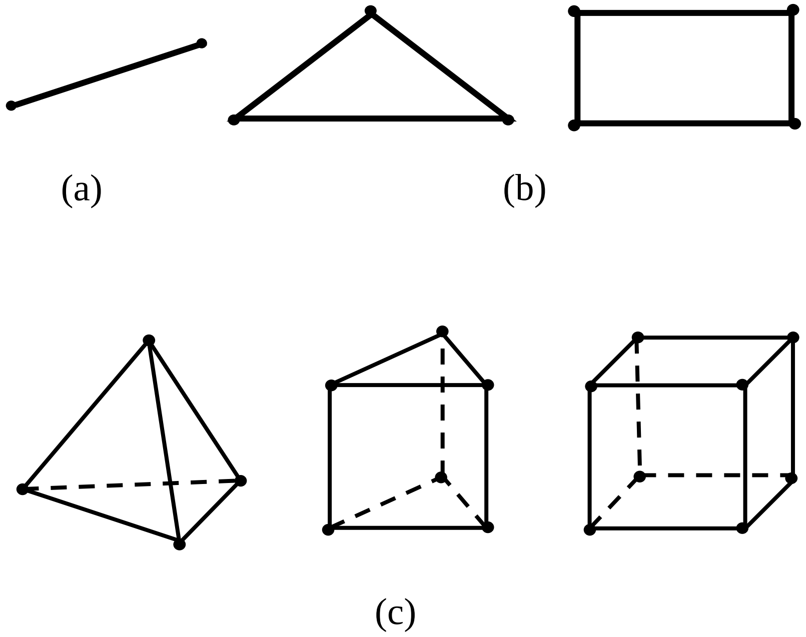
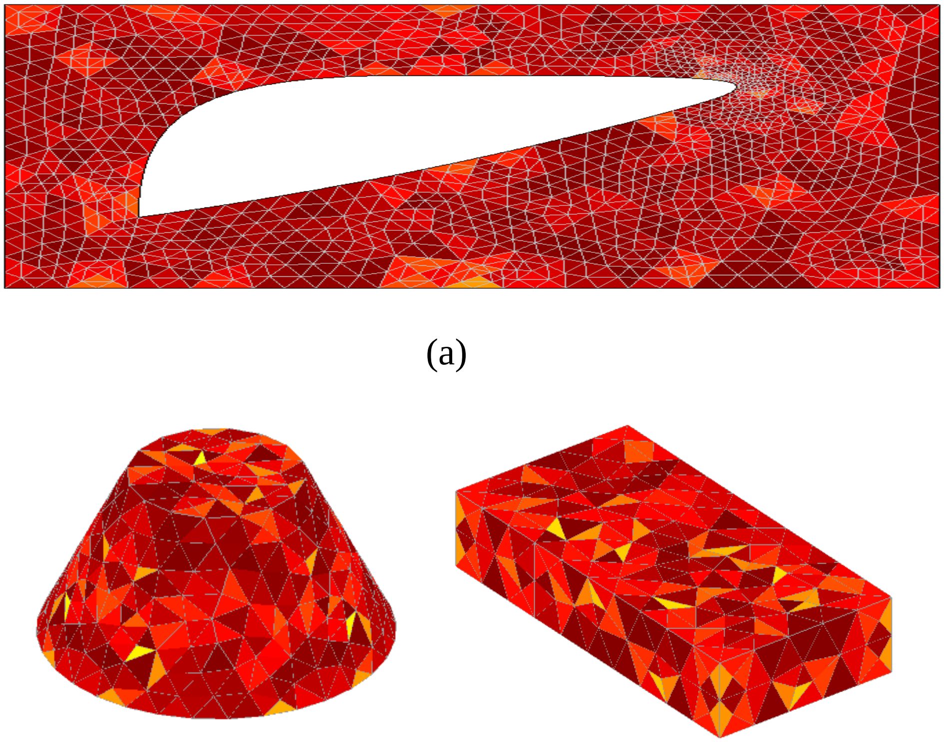


Figure 3.1: Basic finite elements (a) One-dimensional, (b) Two-dimensional, (c) Three dimensional.

discretizing rectangular regions, while the triangular ones can be used for irregular regions. In a three-dimensional solution, the domain may be subdivided into tetrahedra, triangular prisms, or rectangular bricks [Figure 3.1 (c)], among which the tetrahedra are the simplest and best suited for arbitrary-volume domains. We note that the linear line segments, triangles, and tetrahedra are the basic one-, two-, and three-dimensional elements which model curved lines or surfaces by straight line segments or planar patches. In Figure 3.2, we give two examples showing the finite element discretization of a two- and a three- dimensional domain.



(a)

(b)

Figure 3.2: Examples of finite element discritization (a) Two-dimension with triangle (b) Three-dimension with tetrahedral.

In most finite element solutions, the problem is formulated in terms of the unknown function Ø at nodes associated with the elements. For example, a linear line element has two nodes, one at each endpoint. A linear triangular element has three nodes, located at its three vertices, whereas a linear tetrahedron has four nodes, located at its four corners. For implementation purposes, it is necessary to describe these nodes. A complete description of a node contains its coordinate values, local number, and global number. The local number of the node indicates its position in the element, whereas global number specifies its position in the entire system.

2. Selection of interpolation functions

Let us again consider a typical boundary-value problem defined as

$$\Gamma \phi = f \tag{3.1}$$

where Γ is a differential operator, *f* is the excitation or forcing function, and *Ø* is the unknown quantity and it is assumed that the problem is real valued. The second step of a finite element analysis is to select an interpolation function that provides an approximation of the unknown solution within an element. The interpolation is usually selected to be a polynomial of first (linear), second (quadratic), or higher order. Higher-order polynomials, although more accurate, usually result in a more complicated formulation. Hence, the simple and basic linear interpolation is still widely used. Once the order of the polynomial is selected, we can derive an expression for the unknown solution in an element, say element *e*, in the following form:

$$\tilde{\phi}^{e} = \sum_{j=1}^{n} N_j^e \phi_j^e = \{N^e\}^T \{\phi^e\} = \{\phi^e\}^T \{N^e\} \tag{3.2}$$

where n is the number of nodes in the element, $Ø_j^e$ the value of at node j of the element, and N_j^e the interpolation function, which is also known as the expansion or basis function. The highest order of N_j^e is referred to as the order of the element; for example, if N_j^e is a linear function, the element *e* is a linear element. An important feature of the functions N_j^e is that they are nonzero only within element *e*, and outside this element they vanish.

3. Formulation of the System of Equations

The third step, also a major step in a finite element analysis, is to formulate the system of equations. Both the Ritz variational and Galerkin methods can be used for this purpose. Here we shall consider the Ritz variational formulation. The functional *F* can be expressed as

$$F\left(\tilde{\phi}\right) = \sum_{e=1}^{M} F^{e}\left(\tilde{\phi}^{e}\right) \tag{3.3}$$

where *M* is the number of the elements comprising the entire domain and

$$F^{e}\left(\tilde{\phi}^{e}\right) = \frac{1}{2}\int_{\Omega^{e}} \tilde{\phi}^{e}\,\Gamma\,\tilde{\phi}^{e}\,d\Omega - \int_{\Omega^{e}} f\tilde{\phi}^{e}\,d\Omega \tag{3.4}$$

Substituting (3.2) into (3.4), we obtain

$$F^{e} = \frac{1}{2}\left\{\phi^{e}\right\}^{T} \int_{\Omega^{e}} \left\{N^{e}\right\}\Gamma\left\{N^{e}\right\}^{T} d\Omega\left\{\phi^{e}\right\} - \left\{\phi^{e}\right\}^{T} \int_{\Omega^{e}} f\left\{N^{e}\right\} d\Omega \tag{3.5}$$

which can be written in matrix form as

$$F^e = \frac{1}{2}\{\phi^e\}^T[W^e]\{\phi^e\} - \{\phi^e\}^T\{b^e\} \tag{3.6}$$

where $[W^e]$ is an $n \times n$ matrix and $\{b^e\}$ an $n \times 1$ column vector with their elements given by

$$W_{ij}^e = \int_{\Omega^e} N_i^e \Gamma N_j^e \, d\Omega$$

and $$b_i^e = \int_{\Omega^e} f N_i^e \, d\Omega$$

The elemental matrix $[W^e]$ is symmetric since Γ is self-adjoint. Substituting (3.6) into (3.3), we obtain

$$F(\tilde{\phi}) = \sum_{e=1}^{M}\left(\frac{1}{2}\{\phi^e\}^T[W^e]\{\phi^e\} - \{\phi^e\}^T\{b^e\}\right) \tag{3.7}$$

and by performing the summation and adopting the global node numbers, this can be written as ,

$$F = \frac{1}{2}\{\phi\}^T[W]\{\phi\} - \{\phi^e\}^T\{b\} \tag{3.8}$$

where $[W]$ is an $N \times N$ symmetric matrix with N being the total number of unknowns or nodes, $\{Ø\}$ an $N \times 1$ unknown vector whose elements are the unknown expansion coefficients, and $\{b\}$ an $N \times 1$ known vector. The system of equations is then obtained by imposing the stationarity requirement δ*F*=0, or equivalently, by setting the partial derivative of *F* with respect to $Ø_i$ to zero:

$$\frac{\partial F}{\partial \phi_i} = \frac{1}{2}\sum_{j=1}^{N} (W_{ij} + W_{ji})\phi_j - b_i = 0 \qquad i=1,2,3,\ldots\ldots,N. \qquad (3.9)$$

Since [*K*] is symmetric, $W_{ij}=W_{ji}$, and therefore (2.9) becomes

$$\frac{\partial F}{\partial \phi_i} = \sum_{j=1}^{N} W_{ij}\phi_j - b_i = 0 \qquad i=1,2,3,\ldots\ldots,N. \qquad (3.10)$$

Or, $[W]\{\phi\} = \{b\}$ (3.11)

An equivalent, but slightly different derivation of (3.11), is first to take the derivative of $\boldsymbol{F}^{e}$ with respect to $Ø_i^e$

$$\frac{\partial F^{e}}{\partial \phi_i^{e}} = \int_{\Omega^{e}} N_i^{e}\Gamma\{N^{e}\}^{T} d\Omega\{\phi^{e}\} - \int_{\Omega^{e}} fN_i^{e} d\Omega \qquad i=1,2,3,\ldots\ldots,n \qquad (3.12)$$

which can be written in matrix form as

$$\left\{\frac{\partial F^{e}}{\partial \phi^{e}}\right\} = [W^{e}]\{\phi^{e}\} - \{b^{e}\} \qquad (3.13)$$

where $$\left\{\frac{\partial F^{e}}{\partial \phi^{e}}\right\} = \left[\frac{\partial F^{e}}{\partial \phi_1^{e}}, \frac{\partial F^{e}}{\partial \phi_2^{e}}, \frac{\partial F^{e}}{\partial \phi_3^{e}}, \ldots\ldots\ldots.., \frac{\partial F^{e}}{\partial \phi_n^{e}}\right]^{T}$$

to obtain the system of equations, it is necessary to first find $\partial F/\partial \phi$, where

$$\left\{\frac{\partial F}{\partial \phi}\right\} = \left[\frac{\partial F}{\partial \phi_1}, \frac{\partial F}{\partial \phi_2}, \frac{\partial F}{\partial \phi_3}, \ldots\ldots\ldots, \frac{\partial F}{\partial \phi_n}\right]^T$$

Since only the elements that are directly connected to node i contribute to $\partial F / \partial \phi_i$, $\{\partial F / \partial \phi\}$ may be obtained by expanding $\{\partial F^e / \partial \phi^e\}$ into an $N \times 1$ column vector for each element using the relation between the local and global node numbers and then adding them together:

$$\left\{\frac{\partial F}{\partial \phi}\right\} = \sum_{e=1}^{M} \left\{\overline{\frac{\partial F^e}{\partial \phi^e}}\right\} \tag{3.14}$$

The system of equations is then obtained by imposing the stationarity requirement

$$\left\{\frac{\partial F}{\partial \phi}\right\} = \sum_{e=1}^{M} \left(\left[\overline{W}^e\right]\left\{\overline{\phi}^e\right\} - \left\{\overline{b}^e\right\}\right) = \{0\} \tag{3.15}$$

where all the vectors and matrices following the summation signs have been expanded or augmented. To be more specific, $\left[\overline{W}^e\right]$ is expanded or augmented (by zero filling) from $\left[\overline{W}^e\right]$ to an $N \times N$ matrix using the relation between the local node numbers and global node numbers. Similarly $\left\{\overline{\phi}^e\right\}$ and $\left\{\overline{b}^e\right\}$ are augmented to $N \times 1$ column vectors. As a result, (3.15) can also be written as (3.11).

4. Simulation of the System of Equations

Solving the system of equations is the final step in a finite element analysis. The resultant system has one of the following two forms:

$$[W]\{\phi\} = \{b\} \tag{3.16}$$

$$[A]\{\phi\} = \lambda[B]\{\phi\} \tag{3.17}$$

Equation (3.16) is of the deterministic type, resulting from either an inhomogeneous differential equation or inhomogeneous boundary conditions or both. In electromagnetics, deterministic systems are usually associated with scattering, radiation, and other deterministic problems where there exists a source or excitation. To the contrary, (3.17) is of the eigenvalue type, resulting from a homogeneous governing differential equation and homogeneous boundary conditions. In electromagnetics, eigen value systems are usually associated with source-free problems such as wave propagation in waveguides and resonances in cavities. In this case, the known vector $\{b\}$ vanishes and the matrix $[W]$ can be written as $[A]$-$\lambda[B]$, where λ denotes the unknown eigen values.

Once we have solved the system of equations for $\{\emptyset\}$, we can then compute the desired parameters, such as capacitance, inductance, input impedance, and scattering or radiation patterns and display the result in form of curves, plots, or color pictures, which are more meaningful and interpretable [85]. This final stage, often referred to as post-processing, can also be separated completely from the other steps.

Chapter 4

Simulation of Heat Transfer in Graphene

4.1 MODELING OF HEAT TRANSFER IN SINGLE LAYER GRAPHENE

The experiment measured the thermal conductivity of single layer graphene to be within a relatively wide range. The upper estimated limit of the value is larger than the lower limit by 72%. During the derivation of the thermal conductivity two major assumptions were made among others:

- the shape of the flake was thought to be of a rectangle,

- the size of the laser spot was comparable to the width of the flake, so the spot was approximated to be seen as a line heat source producing a plane front of the heat.

It is obvious that new experiments on the thermal conductivity of graphene should be carried out. Some of those studies can look at how the shape and the thickness of the flake, together with the geometry of the heat source, affect the measured value of the thermal conductivity. Such systematic studies might not only improve an accuracy of the thermal conductivity magnitude, but also help understand a picture of the heat transfer in graphene in overall.

Simulations can be performed to study the abovementioned affects. Thus we simulated the heat transfer in single layer graphene and studied various shapes and heat sources. The main objective of the simulation was to model the heat transfer in graphene for different geometries of the flake and the heat source and to see whether the simulated values of the thermal conductivity fall within the experimental range. Also, simulating different geometries of the flake and the heat source allows us to study how they can affect calculations of the thermal conductivity. This eventually helps plan future experiments.

To simulate the heat transfer in graphene we created three models which differ from each other primarily by types of the heat sources:

- the model of the line heat source,
- the model of the disk heat source, and
- the model of the Gaussian heat source.

In COMSOL the design of the model involves several steps that include

1) object's geometry specification,
2) division of the object into subdomains,
3) description of every subdomain,
4) specification of subdomains' boundaries.

During the model design a COMSOL software user can specify the power of the heat source and the thermal conductivity of graphene. The temperature distribution in the flake is a result of the simulation runs. Thus any dependencies of the thermal conductivity can be studied only indirectly, since the thermal conductivity itself is the input for simulations. The simulation itself includes dividing (meshing) the modeled flake into an ensemble of flake's structural components and solving heat conduction equations for each component.

4.1.1. Modeling of heat transfer from a line heat source

If the diameter of the laser sport is comparable to the width of the graphene flake, to simplify the solution one can approximate the shape of the heat source into an infinitesimally thin line, the length of which equals the width of the modeled flake. A graphene layer has a thickness of one carbon atom plane (~0.35 nm). Since it is rather thin, heating the top surface of the flake with the hot line can be seen as resulting in creating within the flake a uniformly hot surface normal to the flake's top or bottom surfaces.

The heated flake, which in COMSOL is called "the domain", is represented as a set of two identical subdomains, 1 and 2 (see Figure 4.1). Each subdomain is a rectangular sheet with dimensions $W \times 2L \times h$. One subdomain is put into contact with another along one of its surfaces. This contact surface is a boundary with a heat flux

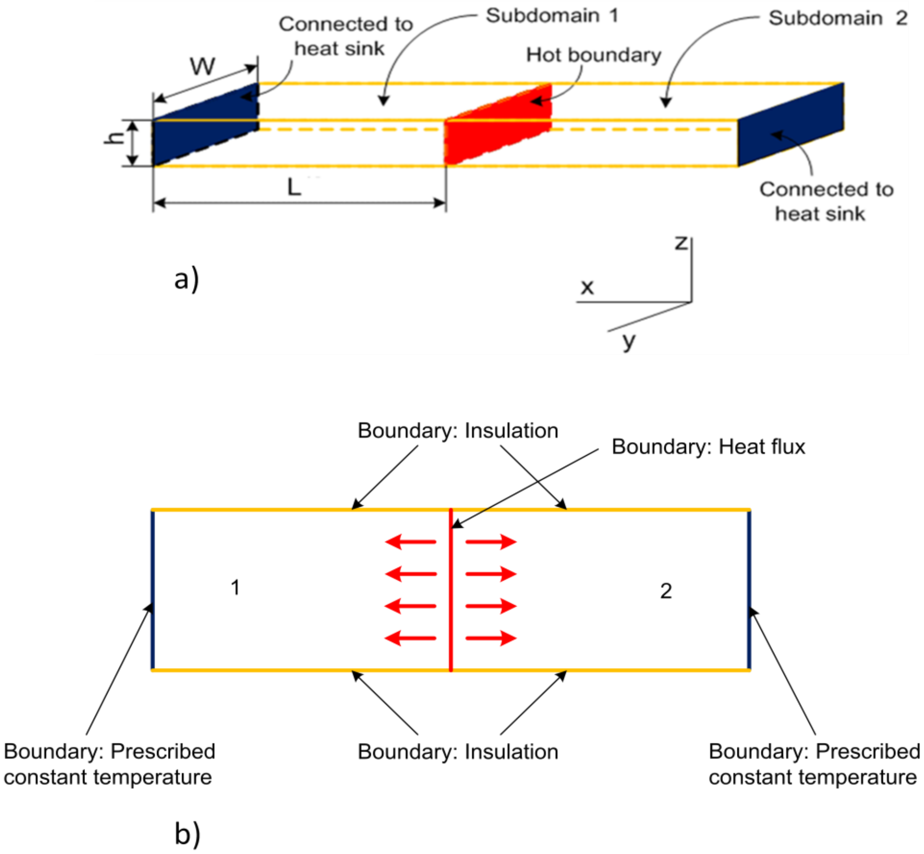


Figure 4.1: Model of the flake heated by a hot line source: a) Axonometric view; b) View from top. This image is after S. Subrina and D. Kotchetkov, "Simulation of Heat Conduction in Suspended Graphene Flakes of Variable Shapes," *J. Nanoelectronics and OptoelectronicsC*, 3, 1 (2008). The image is reprinted with the permission from ASP.

directed inward normally to the sheet. The area of the contact surface is equal to *Wh* which is a product of the width of the sheet and its thickness. The boundary condition of the contact surface is specified using Fourier's law of heat conduction written in the form

$$\vec{n} \cdot (K \nabla T) = q_0 \,, \tag{4.1}$$

where n is the magnitude of the unit vector normal to the contact surface of the subdomain, q_0 is the heat flux that enters the subdomain, [W/m^2].

In each subdomain the boundary that is opposite to the contact surface is specified as being kept at a constant prescribed temperature

$$T = T_0, \tag{4.2}$$

where T_0 = 300 K is the room temperature.

All other four subdomain's boundaries are defined as being completely insulated from the surrounding environment:

$$\vec{n} \cdot (K \nabla T) = 0, \tag{4.3}$$

i.e. the temperature gradient across the boundary is zero.

This assumption simplifies the model but is reasonable. Graphene flake, besides being in contact with the heat sinks and being heated by the laser, can only interact with either air or silicon dioxide. Both air and silicon dioxide have thermal conductivities (0.024 Wm^{-1}K^{-1} and 1.28 W/m^{-1}K^{-1}, respectively) negligible if they are compared with the thermal conductivity of graphene, thus the heat transfer from graphene to either air or silicon dioxide can be ignored.

The heat transfer is modeled as two-dimensional. Due to the fact that the flake has just one atomic layer of arranged carbon atoms, and there are no interactions between graphene and air or silicon dioxide, the heat propagates entirely within the plane. In this model we can vary the power by assigning different values of the hot boundary heat flux (the cross-sectional area *Wh* is constant). Also, we can vary the thermal conductivity. The result of the simulation is a two-dimensional distribution of the temperature in the flake.

4.1.2 Modeling of heat transfer from a disk heat source

During heating, the laser makes a sport on the graphene surface. The spot has a shape of a disk. The heat transfer in the graphene flake can be simulated considering this more realistic heat source. The areas within the laser spot are generally illuminated with different intensities. Also, there is no sharp edge between the spot and non-illuminated areas of the flake. Thus it is necessary to simulate the heat transfer with different radii of the spot to see how reduction of the size of the spot affects the heat conduction and whether the line source is indeed a good approximation for the laser spot. Since the flake is thin, heating the top plane of the flake with the hot disk can be seen as resulting in creating a uniformly hot cylinder embedded in the flake.

For the hot disk source model the flake is described as a set of two subdomains, 1 and 2 (see Figure 4.2). Subdomain 1 is a rectangle with dimensions $W \times 2L \times h$. Subdomain 2 is a cylinder that is embedded in the rectangle and has a specific diameter. The height of the cylinder equals the thickness *h* of the rectangle. The axis of the cylinder is normal to the surface of the rectangle with sides *W* and 2*L* and passes through the

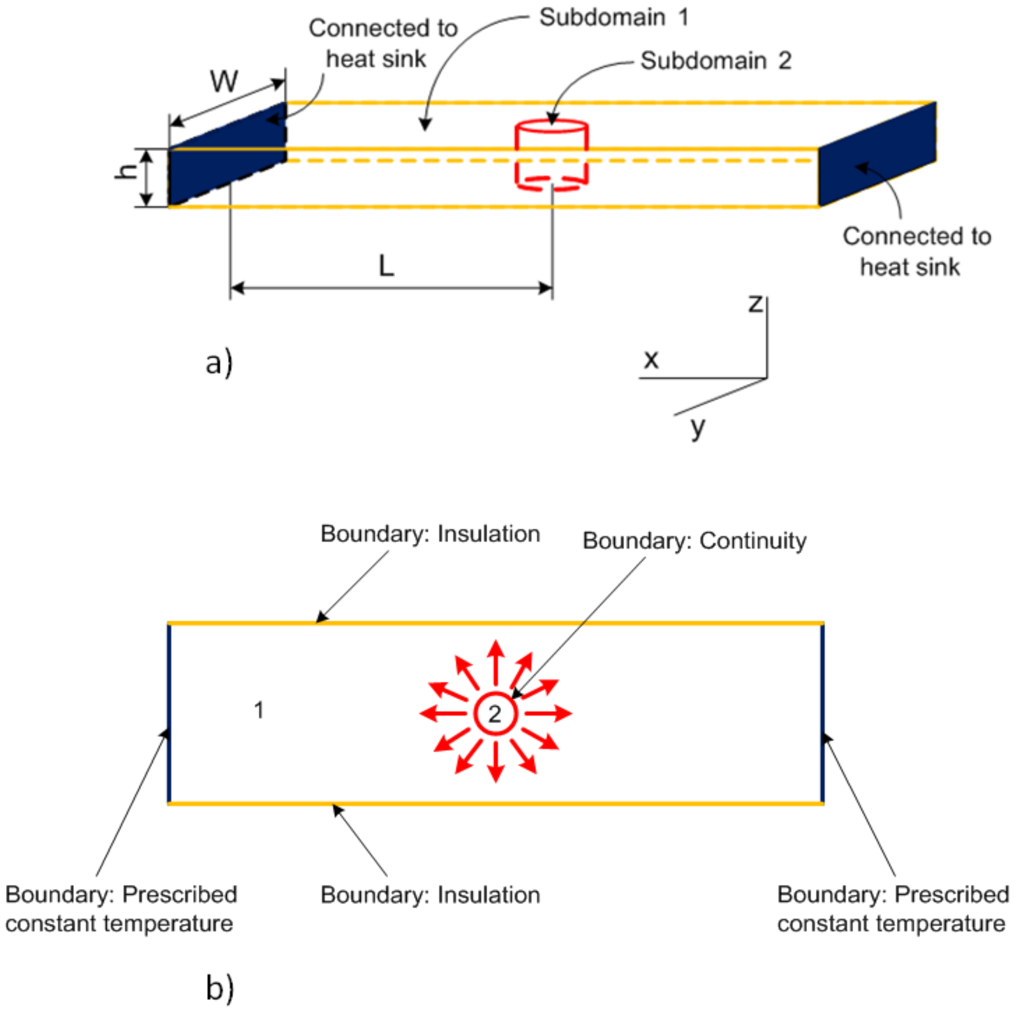


Figure 4.2: Model of the flake heated by a disk source: a) Axonometric view; b) View from top. This image is after S. Subrina and D. Kotchetkov, "Simulation of Heat Conduction in Suspended Graphene Flakes of Variable Shapes *J. Nanoelectronics and OptoelectronicsC*, 3, 1 (2008). The image is reprinted with the permission from ASP.

geometrical center of the rectangle. The difference between this model and the model of the line heat source is that one of the subdomains, namely the subdomain 2, plays the role of a heat generator. In other words, the subdomain 2 contains a heat source within.

The heat conduction in this model is described by the heat equation derived from Fourier’s law:

$$-\nabla \cdot (K \nabla T) = Q \, , \tag{4.4}$$

where Q is the heat source, [W/m^3], which is defined as a heat energy generated within a unit volume per unit time.

The boundary between the subdomains 1 and 2, which is a “barrel” surface of the hot cylinder, is defined as a boundary with the continuous heat flux through it:

$$-\vec{n} \cdot (\overrightarrow{q_1} - \overrightarrow{q_2}) = 0 \, , \tag{4.5}$$

where n is the magnitude of the unit vector normal to the boundary between subdomains, q_1 is the magnitude of the flux of heat flowing out of the subdomain 1, q_2 is the magnitude of the flux of heat flowing into the subdomain 2.

The heat flux is normal to the “barrel” surface of the hot cylinder and is continuous across the boundary: the amount of the heat leaving the subdomain 2 per unit time per unit area equals the amount of the heat flowing into the subdomain 1 per unit time per unit area.

The opposite end surfaces of the subdomain 1 are connected to heat sinks. These boundaries of the subdomain1 are prescribed to be kept at a constant temperature

$$T = T_0 \, , \tag{4.6}$$

where T_0 = 300 K is the room temperature, like for the model of the line heat source.

All other four boundaries of the subdomain 1 and “endcap” surfaces of the subdomain 2 are defined as being completely insulated from the surrounding environment:

$$\vec{n} \cdot (K\nabla T) = 0, \tag{4.7}$$

Like in the case of the line heat source, for the model of the hot disk source the heat transfer is assumed to be two-dimensional.

The heat source equals

$$Q = P/V\ , \tag{4.8}$$

where P is the dissipated power, V is the volume of the subdomain 2.

We can vary the power P (the volume V of the subdomain 2 is constant) and the thermal conductivity. The result of the simulation is a two-dimensional distribution of the temperature in the flake.

4.1.3. Modeling of heat transfer from Gaussian heat source

The third considered heat source is Gaussian. It is interesting to investigate the case when the laser light intensity and the dissipated power follow the normal distribution. Due to a continuous nature of the Gaussian distribution, the heat source in this model cannot be

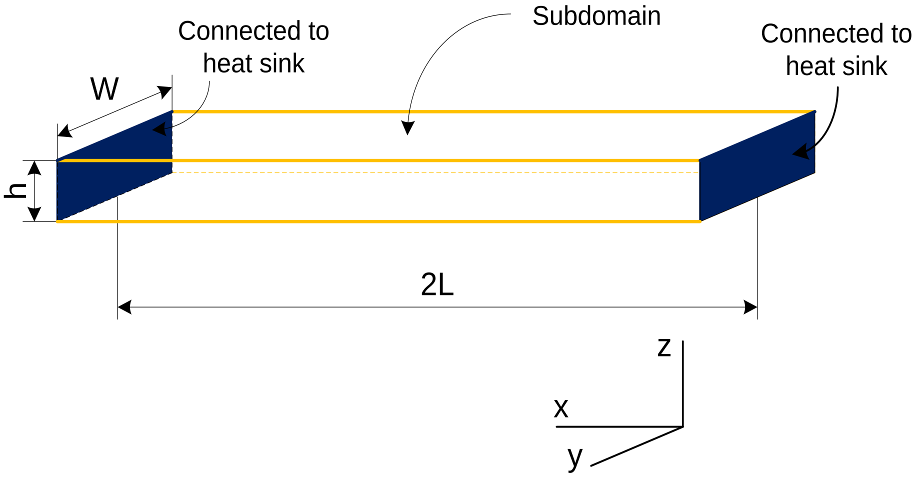


Figure 4.3: Model of the flake heated by Gaussian heat source. This image is after S. Subrina and D. Kotchetkov, "Simulation of Heat Conduction in Suspended Graphene Flakes of Variable Shapes," *J. Nanoelectronics and OptoelectronicsC*, 3, 1 (2008). Reprinted with the permission from ASP.

isolated by boundaries. Neither the Gaussian source itself can be some boundary. Thus in this case, the flake is described as a single subdomain with a heat source within (see Figure 4.3).

Like in the case for the disk source, the heat conduction in this model is described by the heat equation:

$$-\nabla \cdot (K\nabla T) = Q, \tag{4.9}$$

Here the heat source is defined as

$$Q = P/V = P_u, \tag{4.10}$$

where V is the volume of the subdomain. The dissipated power P follows the two-dimensional Gaussian distribution

$$P_u(x,y) = P_{peak} \cdot e^{-\left(\frac{x^2}{2\sigma_x^2}+\frac{y^2}{2\sigma_y^2}\right)}, \qquad (4.11)$$

where P_{peak} is the peak power. Sigmas can be varied but, for simplicity of the model, are assumed to be equal $\sigma = \sigma_x = \sigma_y$.

The volume of the subdomain has a constant value. The Gaussian distribution reaches its peak at the geometrical center of the flake. Like in the case of the line or disk heat sources, the heat transfer is assumed to be two-dimensional, thus the dissipated power is a function of x and y coordinates, but not of z.

The opposite end surfaces of the subdomain are connected to heat sinks. These boundaries of the subdomain are modeled to be kept at a constant prescribed temperature

$$T = T_0 \qquad (4.12)$$

where T_0 = 300 K is the room temperature, like for the models of the line and disk heat sources.

All other four boundaries of the subdomain are defined as being completely insulated from the surrounding environment:

$$\vec{n} \cdot (K\nabla T) = 0 \qquad (4.13)$$

In this model the peak power P_{peak}, the sigma σ and the thermal conductivity can be varied. The result of the simulation is a two-dimensional distribution of the temperature in the flake.

4.2 SIMULATION RESULTS

4.2.1. Effects of the shape of a flake: a line heat source

First simulation runs were dedicated to the studies how much the deviation of the shape from that of a rectangle changes the heat conduction in the flake. We considered the line heat source. The following values were used as inputs for the simulation runs:

- the power of the detector (spectrometer) P_D: 0.5 mW, 1.0 mW, 1.5 mW, 2.0 mW, and 2.7 mW,

- the thermal conductivity of graphene: 3000 $Wm^{-1}K^{-1}$, 3500 $Wm^{-1}K^{-1}$, 4000 $Wm^{-1}K^{-1}$, 4500 $Wm^{-1}K^{-1}$, 5000 $Wm^{-1}K^{-1}$, and 5500 $Wm^{-1}K^{-1}$.

Six shapes were analyzed. Figures 4.4-4.5 show views from top of each shape. Shape 1 viewed from top represents a rectangle with the length $2L = 23$ μm and the width $W = 5$ μm. The excitation line from the heat source passes along the symmetry axis and divides the rectangle into two identical rectangles each with the length of 11.5 μm. Shape 2 viewed from top is a "butterfly"-type shape which is two identical isosceles trapezoids connected along their small sides. The width of each trapezoid is $W = 5$ μm and the height is 11.5 μm. Shape 3 viewed from top is also a "butterfly"- type shape

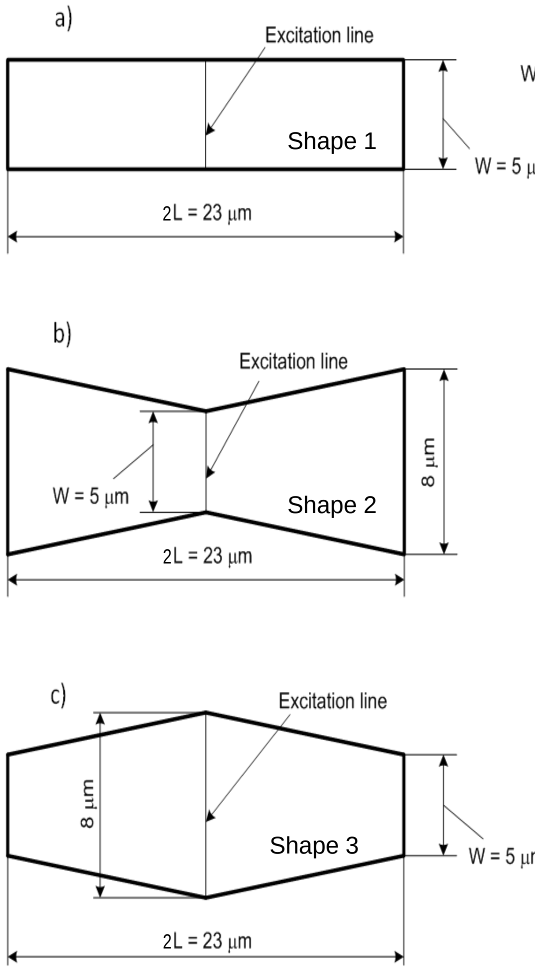


Figure 4.4: a) Shape 1, b) Shape 2, c) Shape 3.

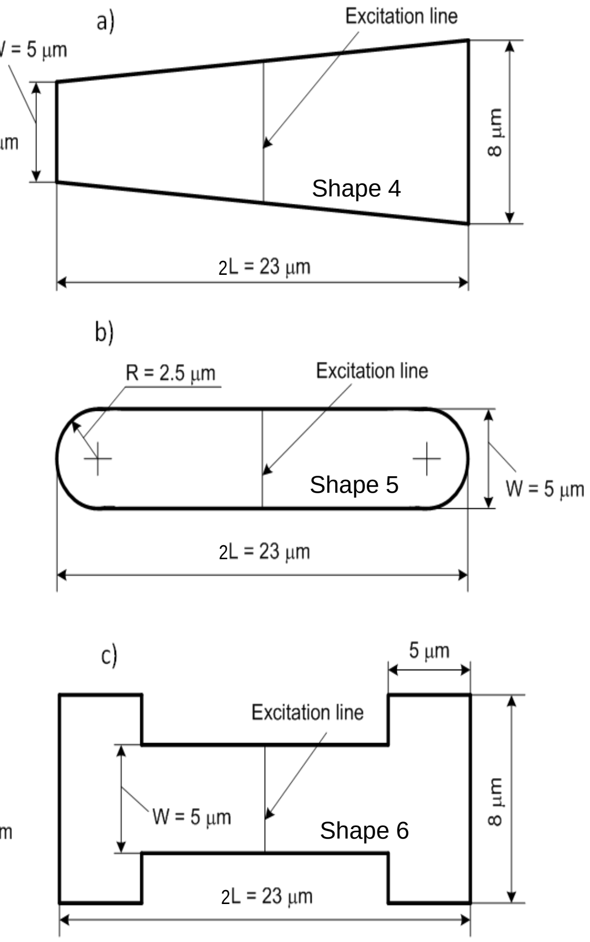


Figure 4.5: a) Shape 4, b) Shape 5, c) Shape 6.

which is two identical isosceles trapezoids but connected along their large sides which have the widths of 8 µm. For both the Shape 2 and Shape 3 the excitation lines go along the connection lines. Shape 4 viewed from top is a trapezoid with the height $2L = 23$ µm and widths W = 5 µm and 8 µm. The excitation line is parallel to both 5 µm and 8 µm sides and crosses the trapezoid at 11.5 µm from either 5 µm or 8 µm side. Shape 5 viewed from top represents a rectangle with the width *W* = 5 μm and the length 18 μm connected at its small sides to two half-disks. The radius of each half-disk is equal to 2.5 μm. The excitation line is perpendicular to both straight lines of the rectangle and passes at 9 μm from either of two small sides of the rectangle. Shape 6 viewed from top is “H”- type shape made of three rectangles. One rectangle has the width *W* = 5 μm and the length of 13 μm. Two identical rectangles with the widths of 5 μm and the lengths of 8 μm are connected to the large rectangle in such a way that the large line of symmetry of the 5 μm x 13 μm rectangle coincides with the small lines of symmetry of the 5 μm x 8 μm rectangles.

By varying the input power and thermal conductivity we were able to extract a temperature profile for each shape. Simulated temperature profiles are shown in Figures 4.6 – 4.7. The linearity of the heat source defines the linear front of the heat wave. Subsequently, linear temperature drop was observed in the Shape 1 flake from the excitation line to the surfaces connected to the heat sinks. It was found that only the Shape 6 mostly preserves the linearity of the temperature drop along the flake. Rounded ends of the Shape 5 result in non-linear behavior of the temperature. Also, in the Shapes 2, 3 and 4 temperature decreases non-linearly from the excitation line to the ends. This is due to a constant change in the width of the flake; the width is not equal to the length of the excitation line everywhere but exactly at the excitation line. The plane heat front gets disturbed in the Shapes 2, 3 and 4, because the cross-section of the flake changes along the large symmetry axis, thus the area, through which the heat flows, changes from its original value (measured under the excitation line).

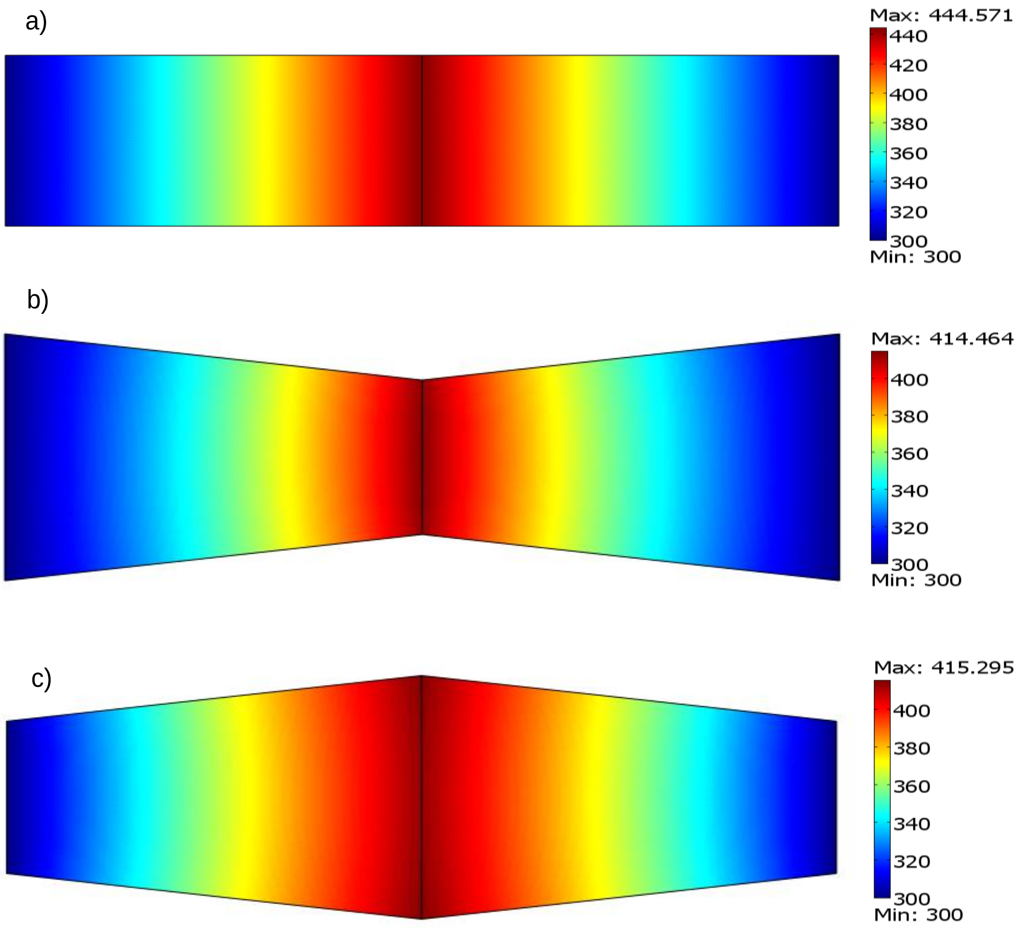


Figure 4.6: Temperature profile of the flake heated with the line source: a) Shape 1, b) Shape 2, c) Shape 3. The excitation power is P_D = 2 mW and the thermal conductivity is K = 5000 $Wm^{-1}K^{-1}$. This figure is after S. Subrina and D. Kotchetkov, "Simulation of Heat Conduction in Suspended Graphene Flakes of Variable Shapes," *J. Nanoelectronics and OptoelectronicsC*, 3, 1 (2008). The figure is reprinted with the permission from ASP.

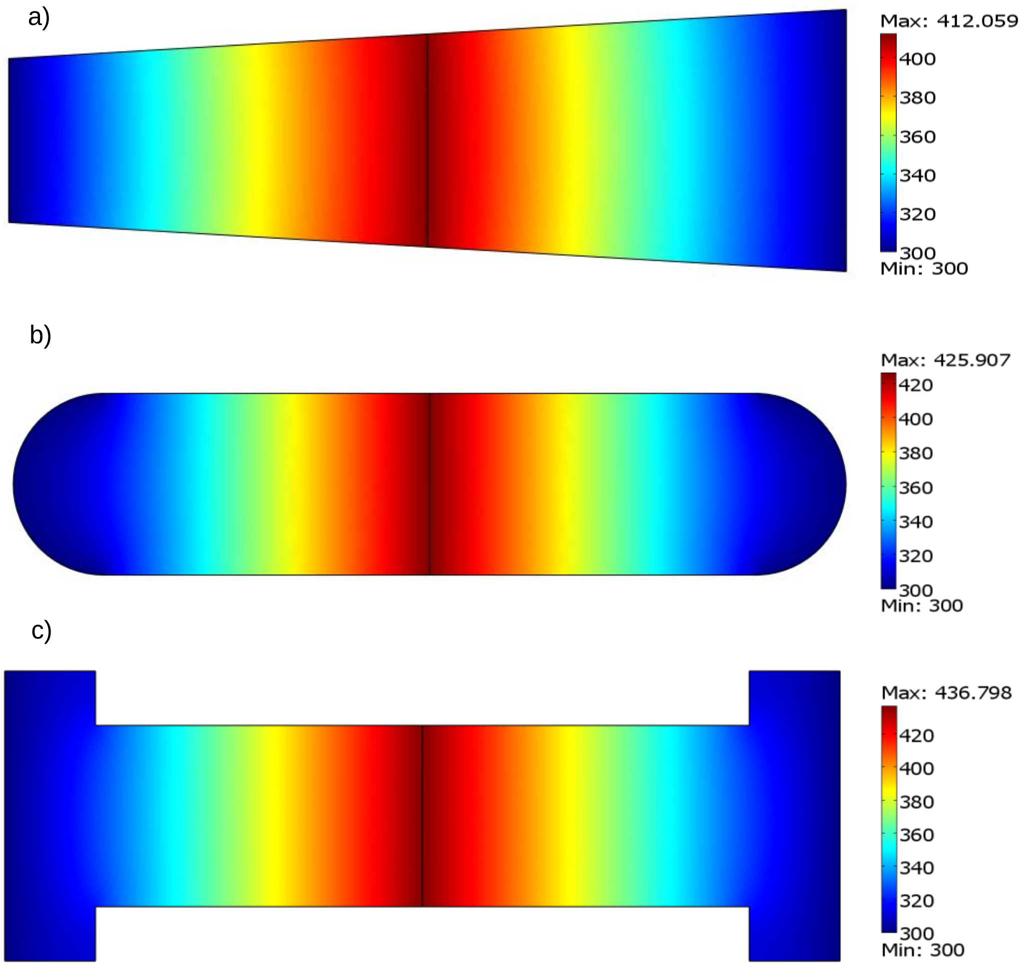


Figure 4.7: Temperature profile of the flake heated with the line source: a) Shape 4, b) Shape 5, c) Shape 6. The excitation power is $P_D = 2$ mW and the thermal conductivity is $K = 5000$ $Wm^{-1}K^{-1}$. This figure is after S. Subrina and D. Kotchetkov, "Simulation of Heat Conduction in Suspended Graphene Flakes of Variable Shapes," *J. Nanoelectronics and OptoelectronicsC*, 3, 1 (2008). The figure is reprinted with the permission from ASP.

By studying a temperature profile for each shape one can analyze how the temperature at the excitation line (the maximum temperature) depends on the power of the detector for each studied shape. Figure 4.8 plots such functions. From the analysis of those plots we can conclude that

1) higher thermal conductivity of graphene results in lower maximum temperature,
2) when the power of the detector is small (0.5 mW) the maximum temperature is approximately same for all shapes,
3) an increase in the power of the detector corresponds to an increase of the maximum temperature; such increase of the temperature is more pronounced for flakes with lower thermal conductivities.

We can also compare different shapes by analyzing their maximum temperatures for certain thermal conductivities. Figure 4.9 shows such analysis for flakes with the thermal conductivities K = 3500 $\mathrm{Wm^{-1}K^{-1}}$ and K = 5000 $\mathrm{Wm^{-1}K^{-1}}$. For both cases, the highest temperatures at the excitation lines are reached when the flakes have geometries of the Shape 1, i.e. rectangular (viewed from top) shapes. Second to the highest value of the temperature is observed for the Shape 6. The lowest temperatures correspond to the "butterfly" Shapes 2 and 3 and the trapezoid Shape 4.

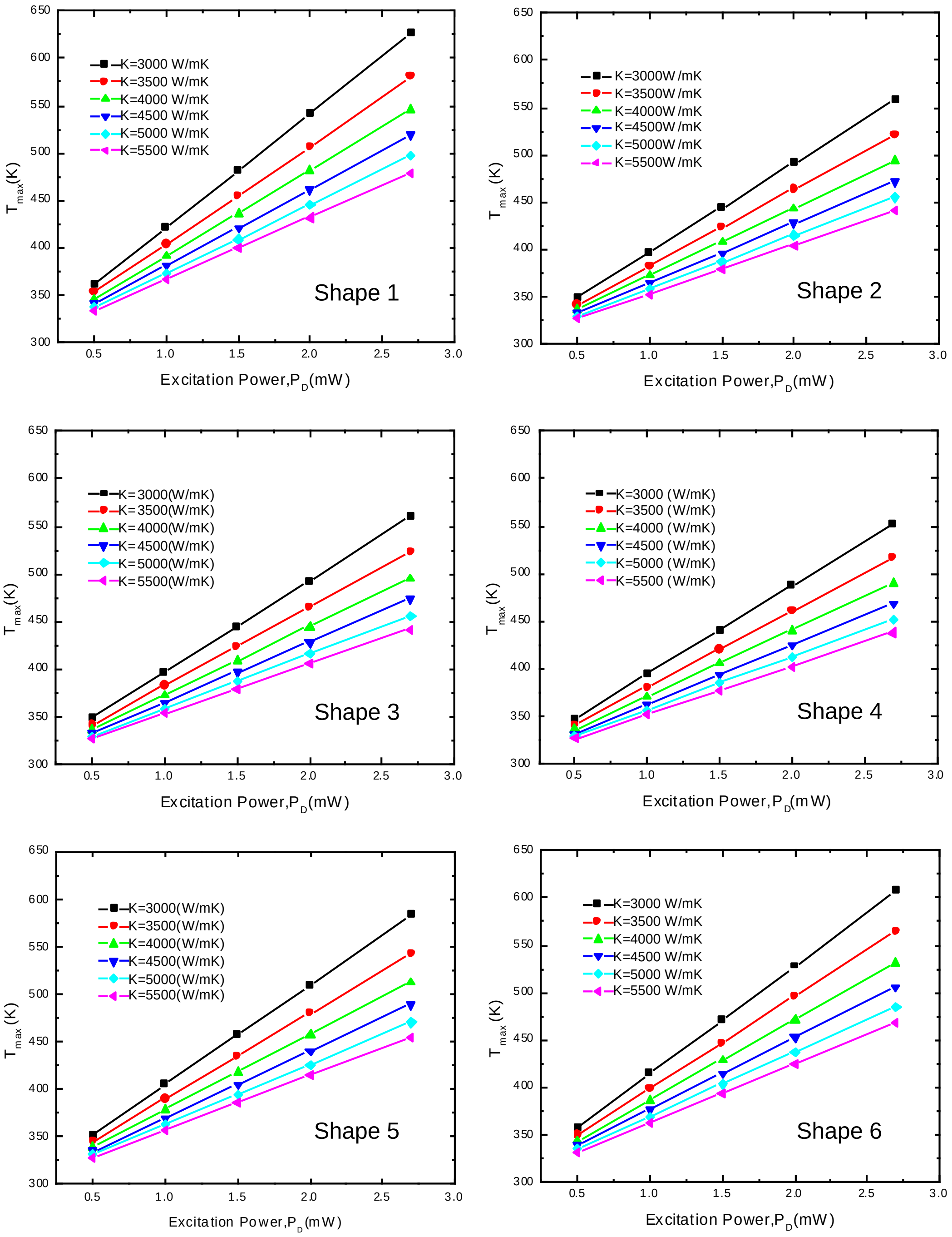


Figure 4.8: Temperature at the center of the excitation line as a function of the detector power for different values of thermal conductivity of graphene and for different shapes.

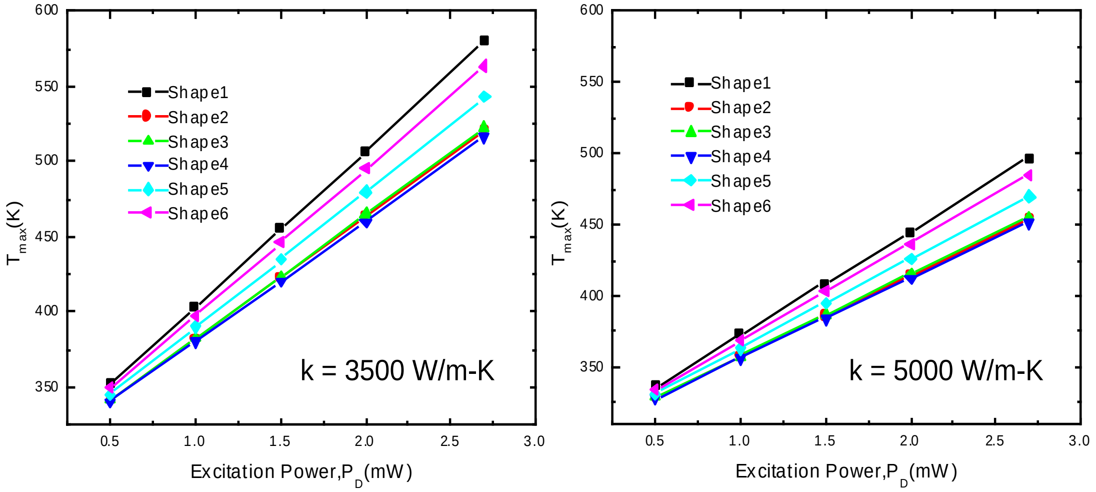


Figure 4.9: Maximum temperatures in the graphene flake for different shapes when the thermal conductivity is equal to K = 3500 $Wm^{-1}K^{-1}$ or K = 5000 $Wm^{-1}K^{-1}$. The results are after S. Subrina and D. Kotchetkov, "Simulation of Heat Conduction in Suspended Graphene Flakes of Variable Shapes," *J. Nanoelectronics and OptoelectronicsC*, 3, 1 (2008). Reprinted with the permission from ASP.

The thermal conductivity of single layer graphene was measured as

$$K = \left(\frac{\eta L}{2Wh}\right) \cdot \chi\theta^{-1} = \left(\frac{\eta L}{2\beta Wh}\right) \cdot \left(\frac{\partial \omega}{\partial T}\right) \cdot \left(\frac{\partial P}{\partial \omega}\right) , \tag{4.14}$$

taking in consideration that the flake had a rectangular shape and the heat was transferring from a line laser source. The measurements were done without actually measuring the temperature at the excitation line, and both coefficients

$$\chi = \delta\omega/\delta T = 0.016 \text{ cm}^{-1}\text{K}^{-1} \tag{4.15}$$

and

$$\theta = \delta\omega/\delta P = 1.226 \text{ cm}^{-1}(\text{mW})^{-1} \tag{4.16}$$

were set to be constant.

In simulations both the power and thermal conductivity are input parameters, and the temperature at the excitation line has to be computed. We can study the function

$$K = f\left(\theta^{-1}\right) , \tag{4.17}$$

where

$$\theta^{-1} = \left(\frac{\partial P}{\partial \omega}\right) = \left(\frac{\partial P}{\chi \partial T}\right) , \tag{4.18}$$

assuming that the temperature coefficient χ remains constant. The example of the simulated $K = f(\theta^{-1})$ spectrum for the Shape 1 is shown in Figure 4.10. Such spectrum gives an insight how a shape irregularity from a perfect rectangle and an actual difference of the heat source from a line affect the measured thermal conductivity. In the experiments both functions of the *G* peak position versus the temperature and the *G* peak position versus the power were independent from the shapes of the flake and source. The shapes of the flake and source were taken into consideration when the thermal conductivity was derived. We can do an opposite task and use simulation results, together with the calculated spectrum $K = f(\theta^{-1})$, to find an extracted value of thermal conductivity for each type of shapes and sources. For example, referring to Figure 4.10,

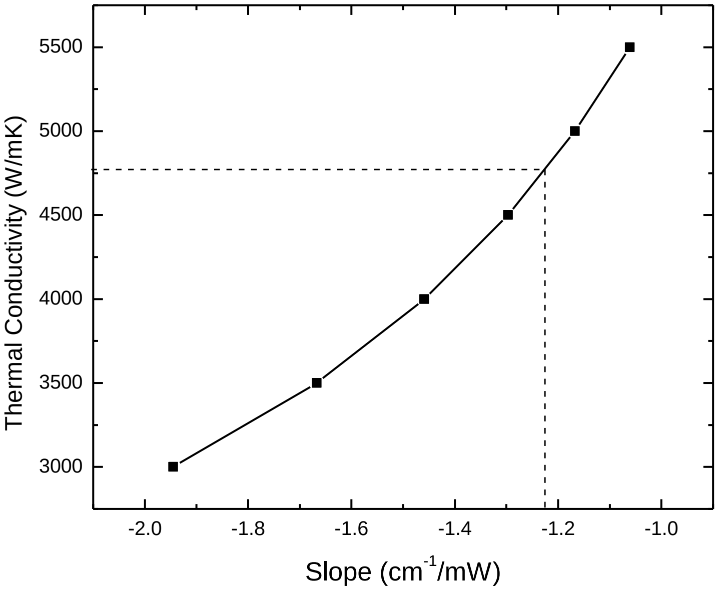


Figure 4.10: Thermal conductivity of the rectangular shaped graphene flake as a function of the parameter $\theta = \delta\omega / \delta P$ (slope) when the line laser source is used. This figure is after S. Subrina and D. Kotchetkov, "Simulation of Heat Conduction in Suspended Graphene Flakes of Variable Shapes," *J. Nanoelectronics and OptoelectronicsC,* 3, 1 (2008). The figure is reprinted with the permission from ASP.

having $K = f(\theta^{-1})$ spectrum, we can choose the point $\theta = 1.226$ cm^{-1}(mW)$^{-1}$ and find the extracted value of the thermal conductivity for the rectangle shape to be $K = 4766$ Wm^{-1}K^{-1}.

Table 4.1 summarizes the simulation results of the heat conduction through the flakes of different shapes when the line source is used. Both the length $2L$ and minimum width W of the flake are kept constant. A is the surface area of the flake; A_0 is the surface area of the Shape 1 flake; T_{max} is the maximum temperature when the excitation

Table 4.1: Effects of different geometries on the temperature and extracted thermal conductivity when the line source is applied. Both the length and minimum width of the flake are kept constant.

Geometry	A x 10^{-10} (m^2)	A/A_0 (%)	T_{max} (K)	T_{max}/T_{0_max} (%)	K ($Wm^{-1}K^{-1}$)	K/K_0 (%)
Shape1	1.15	100 %	444.57	100 %	4766.20	100 %
Shape 2	1.84	160.87 %	414.46	93.23 %	3758.53	78.86 %
Shape 3	1.84	160.87 %	415.30	93.42 %	3782.40	79.36 %
Shape 4	1.84	160.87 %	412.06	92.69 %	3676.68	77.14 %
Shape 5	1.10	95.65 %	425.91	95.80 %	4124.25	86.53 %
Shape 6	1.30	113.04 %	436.80	98.25 %	4477.20	93.94 %

power is P_D = 2 mW and the thermal conductivity of graphene is K= 5000 $Wm^{-1}K^{-1}$; T_{0_max} is the maximum temperature when the excitation power is P_D = 2 mW, the thermal conductivity of graphene is K = 5000 $Wm^{-1}K^{-1}$, and the flake has Shape 1 geometry; K is the extracted thermal conductivity of graphene when θ = 1.226 $cm^{-1}(mW)^{-1}$; K_0 is the extracted thermal conductivity of graphene when θ= 1.226 $cm^{-1}(mW)^{-1}$ and the flake has Shape 1 geometry.

The table compares the surface areas of all shapes, the temperatures at the excitation lines (T_{max}) when the power of the detector equals 2 mW, and when the simulated thermal conductivity of the flake equals 5000 $Wm^{-1}K^{-1}$. Also, the extracted thermal conductivities for different flakes are compared for a chosen parameter $\theta = 1.226$ $cm^{-1}(mW)^{-1}$. From the presented data we can conclude that the heat conduction in the Shape 6 flake resembles the heat conduction in the Shape 1 flake. Both the maximum temperature and extracted thermal conductivity for the Shape 6 are similar to those that correspond to the Shape 1. We might speculate that for the line source, when the heat waves form a plane front within the flake, the nature of the heat propagation is defined by the ratio of the flake's width to the flake's length and rectangularity of the flake. Viewing both the Shape 1 and Shape 6 from top, each of these shapes is essentially rectangular for a substantial distance from the excitation line, and the width of the rectangle is small compared to the length of the rectangle. Only at the "ends" of the rectangle, the Shape 1 is "modified" into the Shape 6 by increasing the width of the rectangle. Since those enlarged ends are connected to the heat sinks which are kept under an ambient temperature, the picture of the heat propagation is not changed much, thus the extracted thermal conductivity and temperature at the excitation line are almost the same as for the case of an "unmodified" rectangle. Partially the abovementioned argument is supported by the fact that the Shape 5 also shows the maximum temperature and extracted thermal conductivity to be close to those of the Shape 1. They are lower than for either the Shape 1 or the Shape 6, because the total area of the flake is reduced. Moreover, the width of the Shape 5 flake reduces fast at the ends of the flake, thus reducing the surface of the heat front that approaches the heat sinks.

We can argue that both the Shape 5 and Shape 6 to some extent resemble the rectangle shapes in areas of the flake which are near the excitation line, thus such flakes display the thermal characteristics similar to those of the “perfect” Shape 1 rectangle. The Shapes 2, 3, and 4 represent opposite phenomena when the shapes are substantially different from a rectangle, particularly in the area near the excitation line. In our specific example, the areas of the Shapes 2, 3, and 4 are larger by 1.6 compared to that of the Shape 1. But both the maximum temperature and extracted thermal conductivity are lower (the temperature is approximately 93% and the extracted thermal conductivity is approximately 80% of the temperature and extracted thermal conductivity, correspondingly, of the Shape 1 flake). An increase of the flake’s width (in average, and in some areas), and a constant change of the width along the large symmetry axis produce such an effect.

The described simulations were done considering all shapes having the same lengths $2L$ and minimum widths W. Thus the surface areas of the flakes were different for different shapes. We also performed similar studies, considering all shapes having the same surface areas and minimum widths W. For such simulation runs we varied the length $2L$ to adjust the surface area of any particular shape to that of the Shape 1. Figure 4.11 shows an example of the simulated maximum temperature as a function of the detector power for the flake that has the Shape 2 type, and which thermal conductivity is 5000 $\mathrm{Wm^{-1}K^{-1}}$. With the reduced length, the temperature rises with the power not as fast as in the case of the original dimension $2L = 23$ µm.

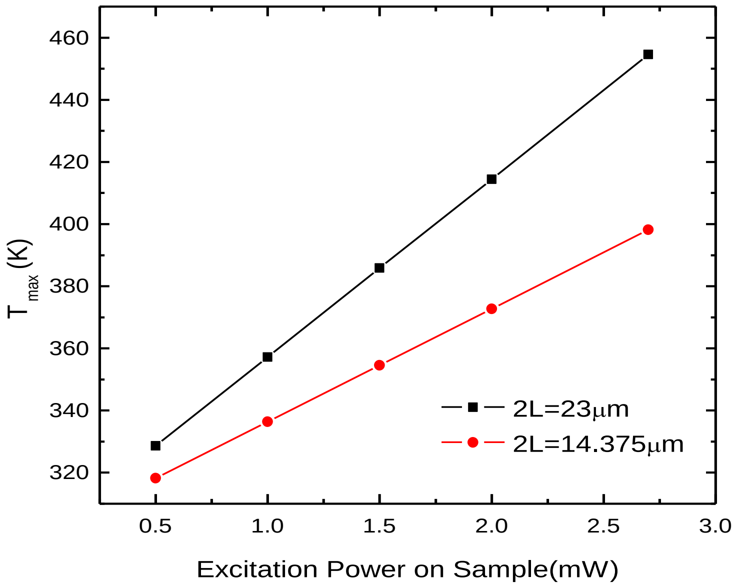


Figure 4.11: Maximum temperature as a function of the detector power in Shape 2 when either the length or the surface area matches that of the Shape 1. The thermal conductivity is 5000 $Wm^{-1}K^{-1}$. This figure is after S. Subrina and D. Kotchetkov, “Simulation of Heat Conduction in Suspended Graphene Flakes of Variable Shapes,” *J. Nanoelectronics and OptoelectronicsC*, 3, 1 (2008). The figure is reprinted with the permission from ASP.

Table 4.2 summarizes the simulations of the heat conduction through the flakes of different shapes when the line source is used and when the surface areas and the minimum widths are fixed. $2L$ is the length of the flake; $2L_0$ is the length of the Shape 1 flake; The detector power is assumed to be 2 mW and the thermal conductivity of the flake is assigned to be 5000 $Wm^{-1}K^{-1}$. Only the flake of the Shape 5 has the length increased by 1.05 if compared with the Shape 1 (rectangle). For all shapes both the maximum temperature and extracted thermal conductivity are dropped. But such drop

Table 4.2: Effects of different geometries on the temperature and extracted thermal conductivity when the line source is applied. Both the surface area and minimum width of the flake are kept constant.

Geometry	$2L$ (μm)	$2L/2L_0$ (%)	T_{max} (K)	T_{max}/T_{0_max} (%)	K ($W/m^{-1}K^{-1}$)	K / K_0 (%)
Shape 1	23.000	100 %	444.57	100 %	4766.20	100 %
Shape 2	14.375	62.50 %	372.74	83.84 %	2386.44	50.07 %
Shape 3	14.375	62.50 %	374.21	84.17 %	2429.93	50.98 %
Shape 4	14.375	62.50 %	369.92	83.21 %	2314.81	48.57 %
Shape 5	24.072	104.66 %	431.70	97.11 %	4319.07	90.62 %
Shape 6	15.000	65.22 %	418.17	94.06 %	3870.72	81.21 %

is minimal for the Shape 5, largely because the length is increased. The flakes that have geometries of the Shapes 2, 3, 4, and 6 have their lengths reduced to 63-65% of the original 23 μm. The Shape 6 does not show significant reductions in the temperature and extracted thermal conductivity due to rectangularity of this shape and still a small fraction width to length ratio. However, the extracted thermal conductivity drops as much as twice in the “butterfly” and trapezoid flakes (the maximum temperatures are 83-84% of the maximum temperature in the Shape 1 flake).

4.2.2. Effects of the shape of a flake: a disk heat source

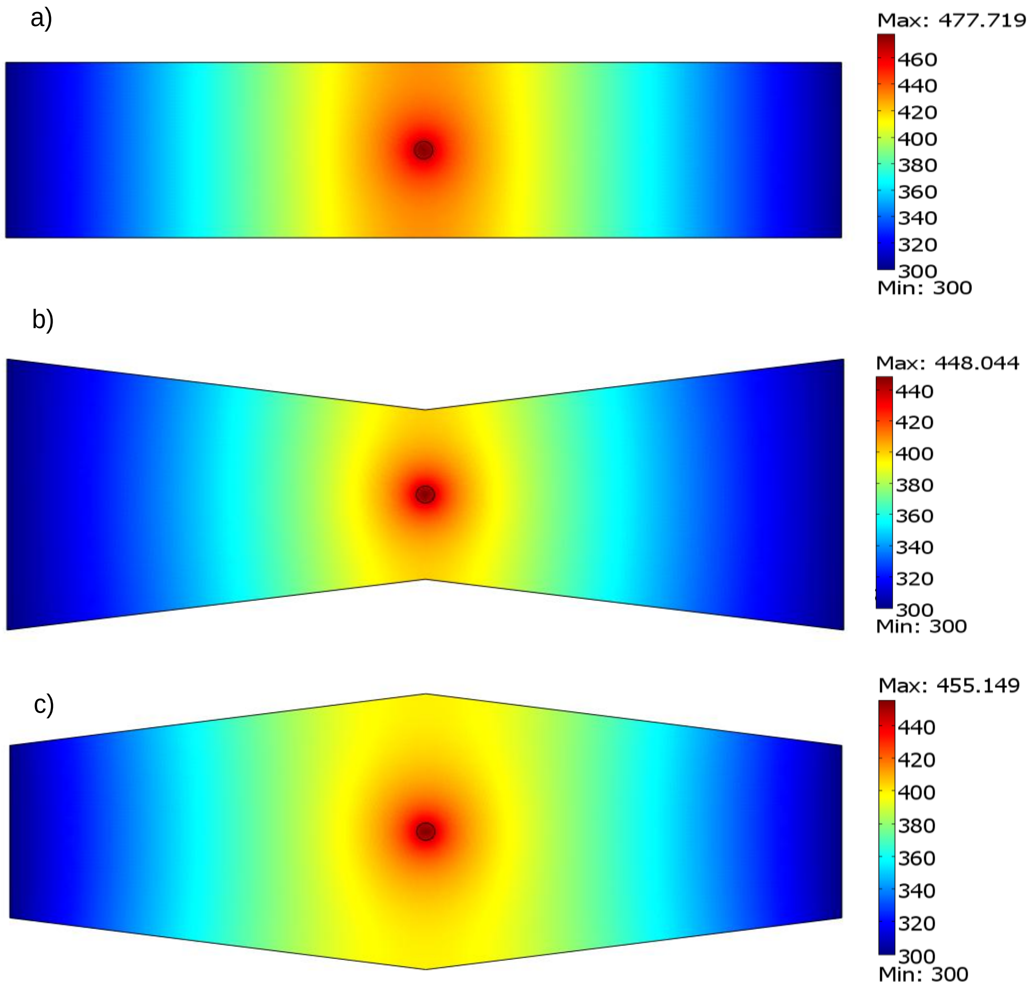


Figure 4.12: Temperature profile of the flake heated with the disk source: a) Shape 1, b) Shape 2, c) Shape 3. The excitation power is P_D = 2 mW and the thermal conductivity is K = 5000 $\mathrm{Wm^{-1}K^{-1}}$. The diameter of the laser spot is 0.5 µm. This figure is after S. Subrina and D. Kotchetkov, ‘Simulation of Heat Conduction in Suspended Graphene Flakes of Variable Shapes,” *J. Nanoelectronics and OptoelectronicsC*, 3, 1 (2008). The figure is reprinted with the permission from ASP.

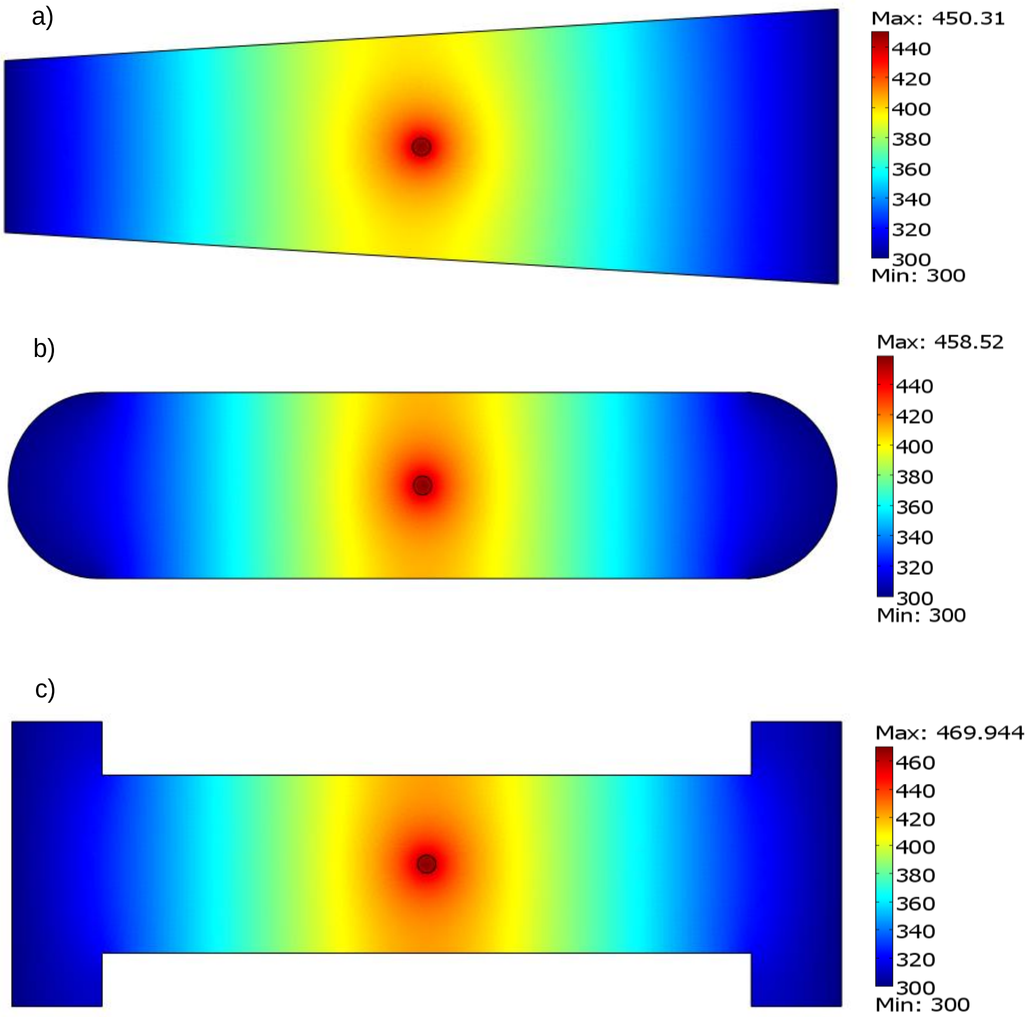


Figure 4.13: Temperature profile of the flake heated with the disk source: a) Shape 4, b) Shape 5, c) Shape 6. The excitation power is P_D = 2 mW and the thermal conductivity is K = 5000 $Wm^{-1}K^{-1}$. The diameter of the laser spot is 0.5 µm. This figure is after S. Subrina and D. Kotchetkov, "Simulation of Heat Conduction in Suspended Graphene Flakes of Variable Shapes," *J. Nanoelectronics and OptoelectronicsC*, 3, 1 (2008). Reprinted with the permission from ASP.

During the measurement of the thermal conductivity of graphene, the heat source was approximated to be the line source. It is interesting to investigate how good such an approximation was. In simulations we replaced the line heat source with a disk heat source. The diameter of the heated disk is taken as 0.5 μm which is close to the diameter of the laser spot during the experiment. We considered the same six shapes of the flake and run simulations again varying the detector power from 0.5 to 2.7 mW and the thermal conductivity from 3000 to 5500 $Wm^{-1}K^{-1}$. As a result, temperature profiles and functions T_{max} vs. P_D were extracted for each shape and the assigned value of the thermal conductivity Figures 4.12 – 4.13 present the temperature profiles for each shape when the heat source has disk geometry. Figure 4.14 shows the maximum temperatures as functions of the detector power for particular values of the thermal conductivity. Inspection of the plots in Figure 4.14 allows us to state that the increase of the temperature, as the detector power increases, shows the trends very similar to those observed in the cases of the line sources. But, when the disk heat source is used, the maximum temperature rises faster, as the power increases.

Table 4.3 summarizes the simulations of the heat conduction through the flakes of different shapes when the disk heat source is used. Both the length $2L$ and minimum width W of the flake are kept constant. The detector power is assumed to be 2 mW and the thermal conductivity of the flake is assigned to be 5000 $Wm^{-1}K^{-1}$. The flakes of different shapes have different surface areas, but the same lengths and minimum widths. If compared with the data in Table 4.1, these results show that, when the hot disk source is used, the geometry of the flake influences changes in the maximum temperature in a

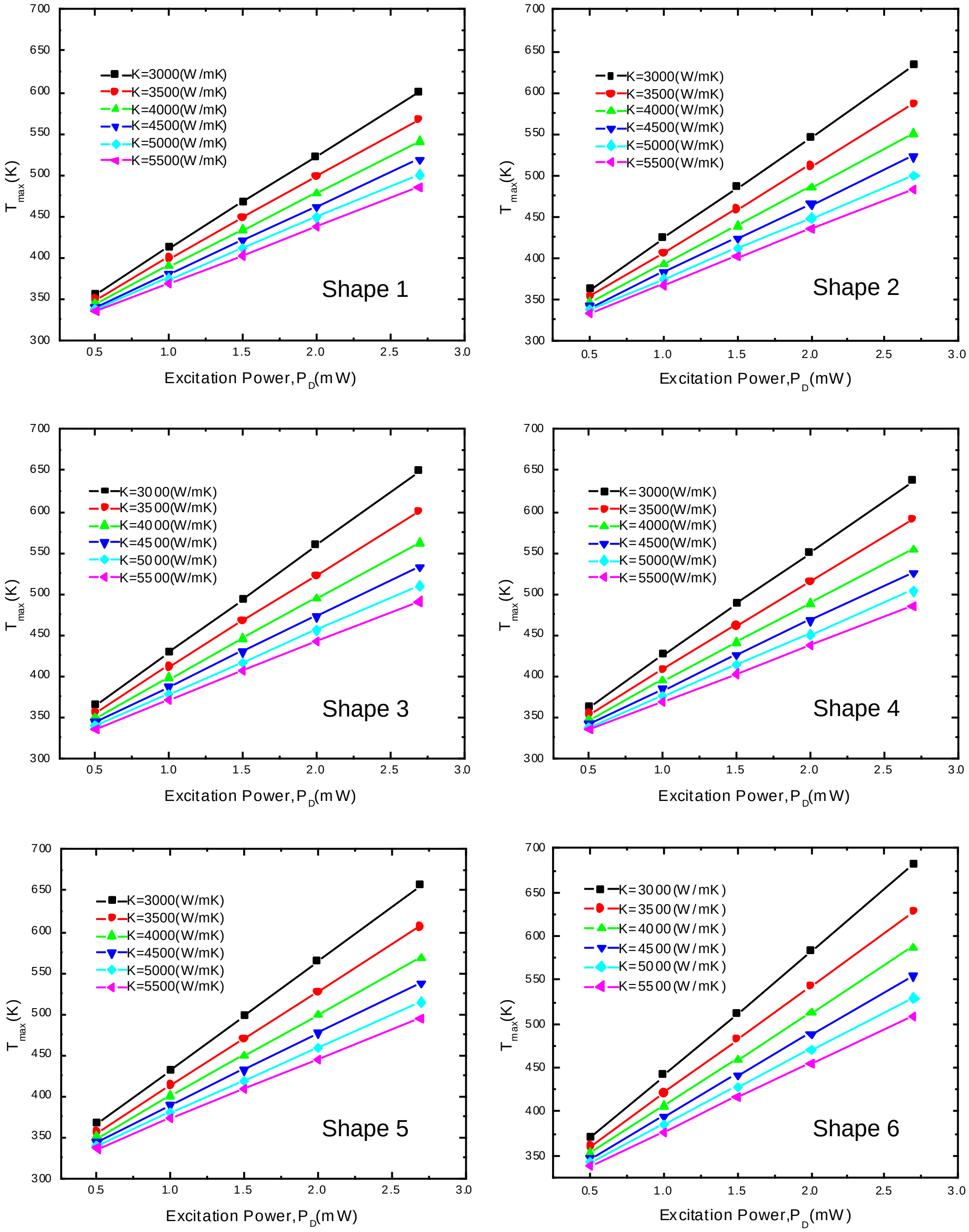


Figure 4.14: Temperature at the center of the laser spot (disk source) as a function of the detector power for different values of graphene's thermal conductivity and different shapes. The results are after S. Subrina and D. Kotchetkov, "Simulation of Heat Conduction in Suspended Graphene Flakes of Variable Shapes," *J. Nanoelectronics and OptoelectronicsC*, 3, 1 (2008). Reprinted with the permission from ASP.

Table 4.3. Effects of different geometries on the temperature and extracted thermal conductivity when the disk heat source is used.

Geometry	A x 10^{-10} (m^2)	A/A_0 (%)	T_{max} (K)	T_{max}/T_{0_max} (%)	K ($Wm^{-1}K^{-1}$)	K / K_0 (%)
Shape 1	1.15	100 %	477.72	100 %	5816.80	100 %
Shape 2	1.84	160.87 %	447.99	93.78 %	4843.52	83.27 %
Shape 3	1.84	160.87 %	455.15	95.28 %	5067.79	87.12 %
Shape 4	1.84	160.87 %	450.31	94.26 %	4914.30	84.48 %
Shape 5	1.10	95.65 %	458.52	95.98 %	5185.47	89.15 %
Shape 6	1.30	113.04 %	469.94	98.37 %	5578.88	95.91 %

very similar way, as when the heat source is a line. But the “butterfly” and trapezoid geometries of the Shapes 2, 3 and 4 have lesser effects on the extracted thermal conductivity compared to the situation with the line source. As in the case of the line source, the heat conduction in the Shape 6 flake most closely resembles the heat conduction in the rectangle Shape 1 flake.

4.2.3 Effects of a geometry of a source: a disk and Gaussian heat sources

It is interesting to see how the geometry of the heat spot affects the simulated heat conduction. To investigate this we can directly compare the heat conduction profiles for the line and the disk sources, vary the sizes of the disk spots or replace the disk laser spot with Gaussian heat source.

Table 4.4 provides a direct reference-comparison of the maximum temperatures and extracted thermal conductivities for different shapes (P_D = 2 mW and K = 5000 $Wm^{-1}K^{-1}$). As it was mentioned, the maximum temperature slightly drops in all

Table 4.4. Maximum temperatures and extracted thermal conductivities for the cases of the line and disk heat sources.

Geometry	T_{max}/T_{0_max} (%) line source	T_{max}/T_{0_max} (%) disk source	K / K_0 (%) line source	K / K_0 (%), disk source
Shape 1	100 %	100 %	100 %	100 %
Shape 2	93.23 %	93.78 %	78.86 %	83.27 %
Shape 3	93.42 %	95.28 %	79.36 %	87.12 %
Shape 4	92.69 %	94.26 %	77.14 %	84.48 %
Shape 5	95.80 %	95.98 %	86.53 %	89.15 %
Shape 6	98.25 %	98.37 %	93.94 %	95.91 %

shapes when the geometry changes from a perfect rectangle. The percentage of the drop in the temperature in the case of the line heat source is almost identical to the percentage of such drop when the hot disk source is used. However, with the disk source the extracted thermal conductivity is less dependent on the shapes than when the heat source is a line. Obviously, variation of the shape from a rectangle has a stronger effect when the heat waves travel in a line (plane) front. When the heat travels along the longer side of the flake, the propagation of the front is affected by how the width of the flake changes. But, when the source has disk geometry, the heat waves form a circular front, thus, at least in the areas near the source, the heat propagates independently of the shape of the flake. The data in the table supports the fact that in the cases of the line source and the "butterfly" or trapezoid shapes the heat propagation is strongly affected by the geometry of the flake.

Table 4.5 directly compares the maximum temperatures and the extracted thermal conductivities extracted under the same conditions (P_D = 2 mW and K = 5000 $\mathrm{Wm^{-1}K^{-1}}$) for the line and the disk heat sources. The very fact that the heat source has a disk shape results in increases in both the temperature and thermal conductivity. The temperature is increased by 7-10% and the thermal conductivity is increased by 22-34% when we change the model of the heat source from the line to the disk. It is interesting to see that the flakes that resemble rectangles better (the Shapes 5 and 6) show less dependence on the geometry of the source. This effect is especially seen in the values of the extracted thermal conductivity. While the disk heat source models for the Shapes 5 and 6 show 25-26% increases compared to the line source models, the extracted thermal conductivity

Table 4.5. Direct comparison of the maximum temperatures and extracted thermal conductivities for the cases of the line and disk heat sources.

Geometry	T_{max_line} (K)	T_{max_disk} (K)	$T_{max\_disk}/T_{max\_line}$ (%)	$K_{\_line}$ ($Wm^{-1}K^{-1}$)	$K_{\_disk}$ ($Wm^{-1}K^{-1}$)	$K_{\_disk}/K_{\_line}$ (%)
Shape1	444.57	477.72	107.47 %	4766.20	5816.80	122.04 %
Shape 2	414.46	447.99	108.09 %	3758.53	4843.52	128.87 %
Shape 3	415.30	455.15	109.60 %	3782.40	5067.79	133.98 %
Shape 4	412.06	450.31	109.28 %	3676.68	4914.30	133.66 %
Shape 5	425.91	458.52	107.66 %	4124.25	5185.47	125.73 %
Shape 6	436.80	469.94	107.59 %	4477.20	5578.88	124.61 %

is increased by 29-34% in the “butterfly” and trapezoid flakes. The difference between the line and the disk heat sources is not so obvious if the flake resembles a rectangle and when the width W is small compared to the length $2L$.

According to Table 4.5, the extracted thermal conductivities of the rectangle Shape 1 and the H-type Shape 6 are both higher than the thermal conductivity reported by the experiment. If during the experiment the dimensions of the flake were evaluated correctly, approximation of the disk source by the line source results in underestimation of the thermal conductivity during calculations. Moreover, such a simulation result hints

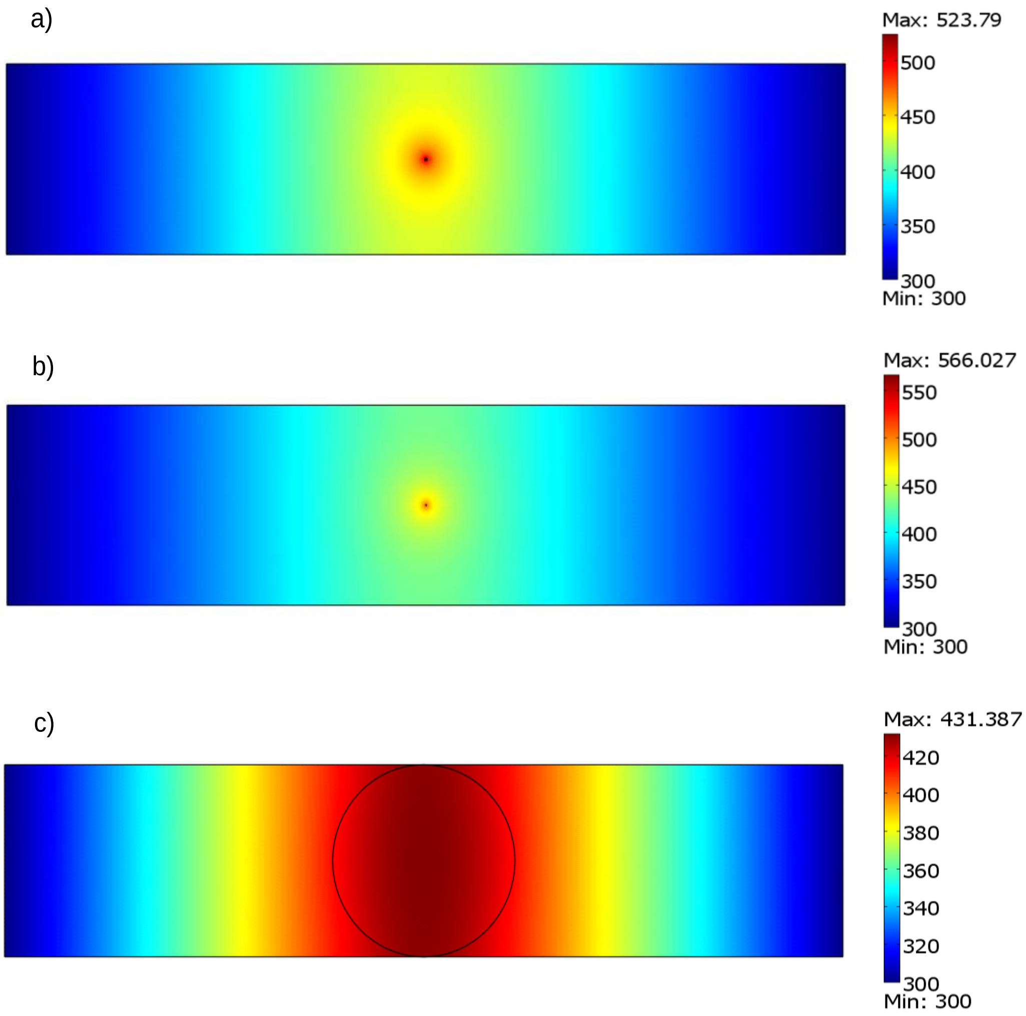


Figure 4.15: Temperature profile of the flake heated with the disk source. The excitation power is P_D = 2 mW and the thermal conductivity is K = 5000 Wm^{-1}K^{-1}. The diameter of the laser spot is a) 0.05 μm, b) 0.005 μm, and c) 5 μm. This figure is after S. Subrina and D. Kotchetkov, "Simulation of Heat Conduction in Suspended Graphene Flakes of Variable Shapes," *J. Nanoelectronics and OptoelectronicsC*, 3, 1 (2008). Reprinted with the permission from ASP.

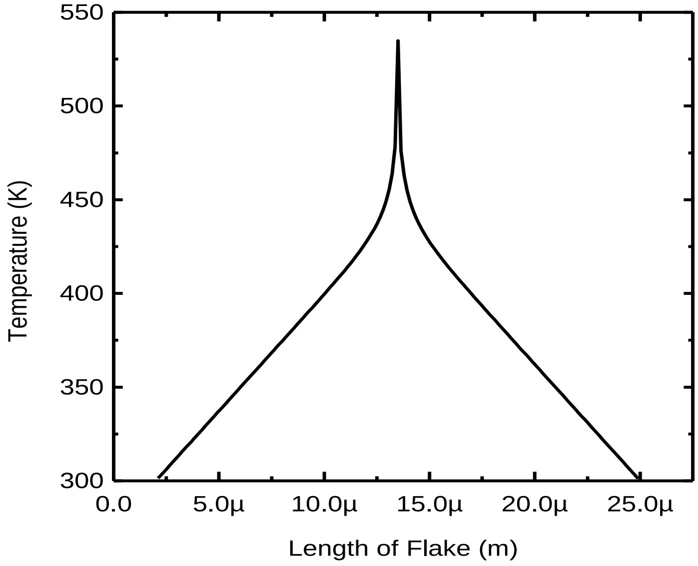


Figure 4.16: Local temperature as a function of the coordinate along the large symmetry axis. Disk heat source with a diameter of 0.05 µm.

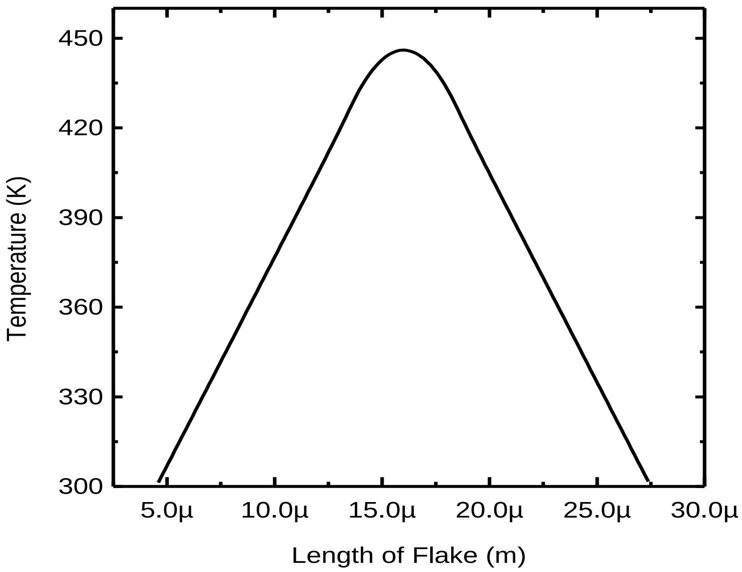


Figure 4.17: Local temperature as a function of the coordinate along the large symmetry axis. Disk heat source with a diameter of 5 µm.

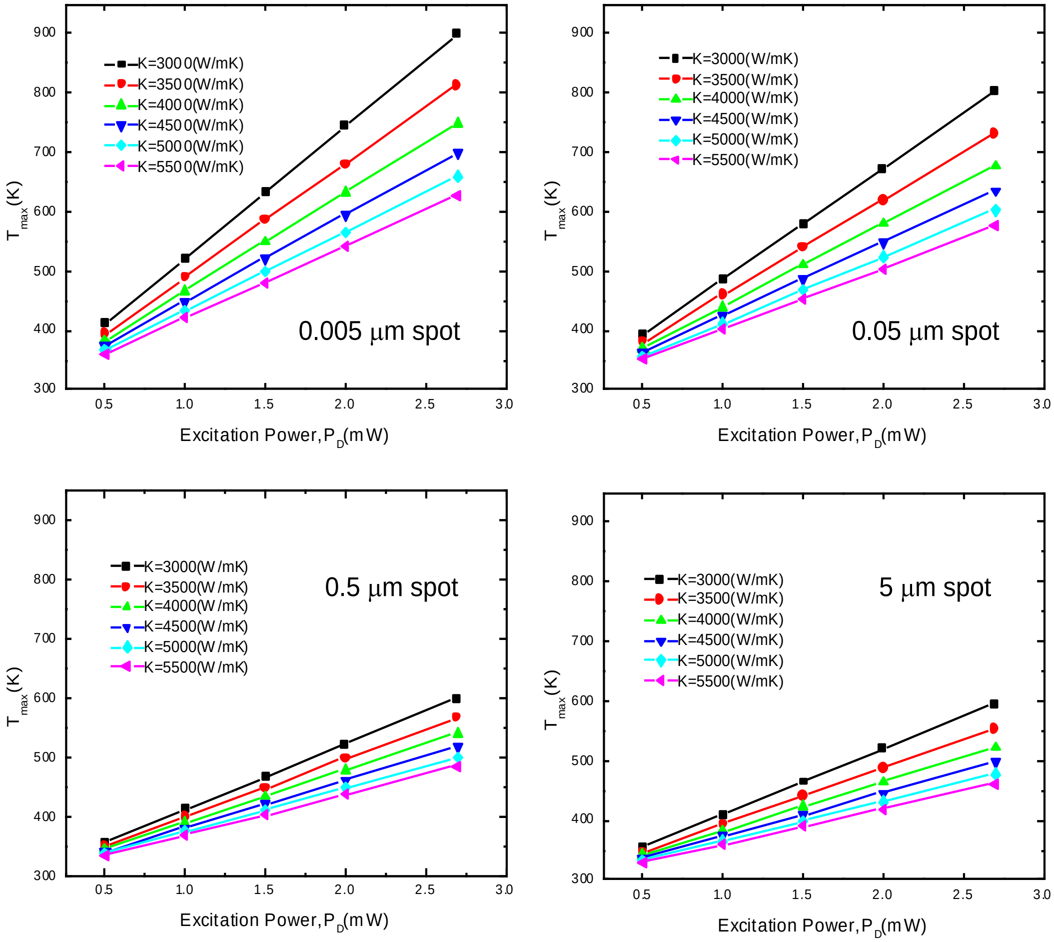


Figure 4.18: Temperature at the center of the laser spot (disk source) as a function of the detector power for different values of graphene’s thermal conductivity and different diameters of the laser spots. This figure is after S. Subrina and D. Kotchetkov, “Simulation of Heat Conduction in Suspended Graphene Flakes of Variable Shapes,” *J. Nanoelectronics and OptoelectronicsC*, 3, 1 (2008). Reprinted with the permission from ASP.

that the true value of the single layer graphene thermal conductivity is closer to its upper reported bound (5300 $Wm^{-1}K^{-1}$) rather than to its lower bound (3080 $Wm^{-1}K^{-1}$).

We can also investigate how the sizes of the laser spots affect the simulated temperature and extracted thermal conductivity. Figure 4.15 presents the temperature profiles for the Shape 1 flakes when the heat sources are disks and the diameters of the disks are 0.005 µm, 0.05 µm and 5 µm. The local temperatures as functions of the coordinates along the large symmetry axis of the Shape 1 are shown in Figure 4.16 for the 0.05 µm and in Figure 4.17 for the 5 µm disk sources. Both plots suggest that this function is highly non-linear in the areas close to the center of the laser spot, but linearizes as the distance from the center of the spot increases. Figure 4.18 shows the maximum temperatures as functions of the detector power for chosen values of the thermal conductivity. The temperature increases very rapidly with the power in cases of small laser spots, 0.005 µm and 0.05 µm.

Table 4.6 illustrates the results of the simulated maximum temperature (P_D = 2 mW and K = 5000 Wm^{-1}K^{-1}) and extracted thermal conductivity for different disk diameters. The Shape 1 was considered. It is seen that the reduction of the size of the spot leads to an increased maximum temperature and an increased extracted thermal conductivity, but such increases are functionally weaker compared to the size modification. Reducing the size by a factor of 10 results in just 10% increase in the temperature and 26% increase in the extracted thermal conductivity. Reducing the size by a factor of 100 leads to 18% increase in the temperature and 50% increase in the thermal conductivity. Increase of the size of the spot by 100 makes the temperature drop by 10% and the thermal conductivity drop by 26%.

Table 4.6. Maximum temperatures and extracted thermal conductivities for different sizes of the hot disk source. Shape 1 is considered.

Spot diameter (μm)	T_{max} (K)	$T_{max}/T_{0.5\_max}$ (%)	K ($Wm^{-1}K^{-1}$)	$K/K_{0.5}$ (%)
0.5	477.72	100 %	5816.80	100 %
0.005	566.03	118.49%	8697.63	149.53 %
0.05	523.79	109.64 %	7310.93	125.69 %
5	431.39	90.30 %	4303.94	73.99 %

According to the table the extracted thermal conductivities for the 0.05 μm and 0.005 μm laser spots are unrealistically high. We might conclude that it is unlikely that the laser spots can be modeled as the spots with such small diameters. The model of the 5 μm spot shows the extracted thermal conductivity to be within the range reported by the experiment. Thus the large disk spot is not in contradiction with observations. Also, since the diameter of such a big spot equals the width of the flake, the front of the propagating heat in the flake will be predominantly linear, thus the 5 μm disk source can surely be approximated as a line heat source.

It is not clear what kind of distribution the laser beam follows. We investigated whether the model of the heat source as a disk with a distinct boundary can be replaced by the model of the heat source where the power follows Gaussian distribution. We considered laser source of diameter 1 μm as a source of excitation which had FWHM power at the radius of the laser source. Volume integral of the power distribution, equals the power dissipated by the laser source. The heat dissipation to the air as well as the thermal coupling between the flake and substrate was considered to be negligible. The temperature of the graphene flake was locally increased in the middle with a laser source that follows Gaussian distribution and the peak of this distribution was located at the geometrical center of the trench zone. During the experiment, the laser power was set to approximately 2 mW. Figure 4.19 presents the temperature profile of the flake heated with the Gaussian heat source. The maximum temperature (measured under the condition that the thermal conductivity of graphene equals K = 5000 $Wm^{-1}K^{-1}$) at 2mW and the extracted thermal conductivity of the flake are equal to 455.93 K and 5073 $Wm^{-1}K^{-1}$, correspondingly. As it is seen, in this model the extracted thermal conductivity is closer to the upper experimental bound.

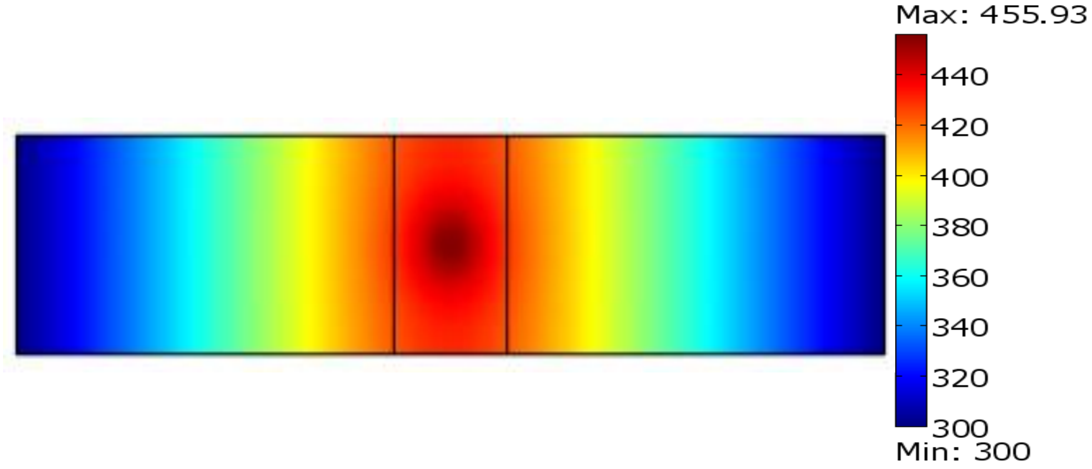


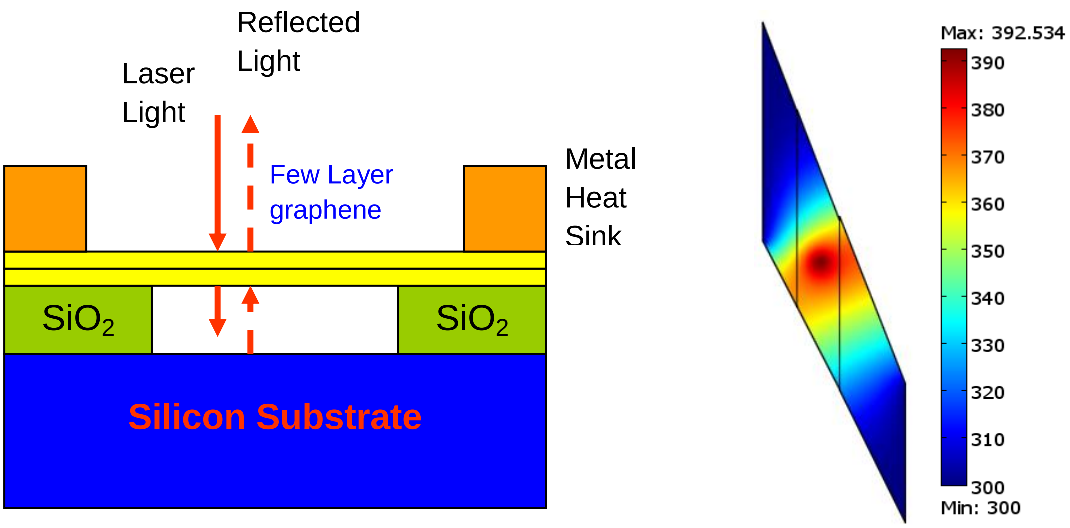
Figure 4.19: Temperature profile of the flake heated with the Gaussian heat source. The excitation power is P_D = 2 mW and the thermal conductivity is K = 5000 W/mK. The diameter of the laser spot is 1 μm.

4.3 HEAT CONDUCTION IN FEW GRAPHENE

The investigation of heat conduction from 2D graphene to 3D bulk is of great interest for both fundamental science and practical applications [86, 87]. We considered this issue by determining the thermal conductivity of few layer graphene (FLG) as the number of atomic planes increases. Detailed experimental studies on the thermal conductivity of graphene were performed, in which flakes with multiple sp^2 carbon layers were measured. It is quite difficult to mechanically exfoliate FLG of the same geometry and dimensions. We intentionally did not pattern the exfoliated FLG flakes into the same shape to avoid any possible damage into the flakes. Balandin's *et al.* [47] considered plane heat front as the size of the laser spot was comparable to the width of the flake and relatively low width to length ratio. However, these assumptions are no longer valid in the obtained few layer graphene samples. Again the intensity of laser beam follows Gaussian distribution. That is why numerical solution of heat diffusion equation is necessary to extract thermal conductivity of suspended FLG flakes of arbitrary geometries. We developed a model of heat conduction in two, three and four layer graphene flakes using the finite element method. The model allowed us to simulate temperature profiles and extract thermal conductivity of irregular shaped suspended few layer graphene.

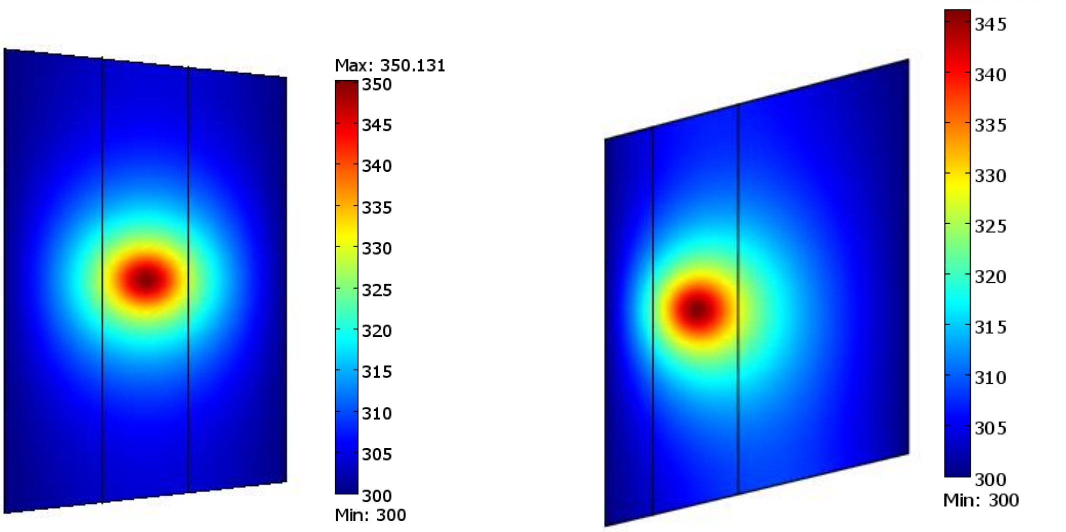
A number of FLG samples were prepared by standard mechanical exfoliation of bulk graphite and suspended across trenches in Si/SiO_2 wafers to minimize heat interactions of graphene with the environment and to simplify the calibration procedure for estimation of the absorption coefficients. The width of the suspended flakes varied from 5 µm to 16 µm. The number of atomic layers in the graphene flakes was determined with micro-Raman spectroscopy through deconvolution of the 2D/*G* band in the spectrum of graphene [78]. The measurements of thermal conductivity were carried out with the help of steady-state non-contact optical technique using micro-Raman spectroscopy [47]. The Raman spectra of graphene were studied as functions of temperature [82] and power of the detector [47, 83]. Both functions, the shift of the *G*-peak position versus the temperature of the flake (temperature coefficient) and the shift of the *G*-peak position versus the power of the detector (power coefficient), were linear. The temperature coefficients χ were measured to be -0.016 $cm^{-1}K^{-1}$ for single-layer graphene and -0.011 $cm^{-1}K^{-1}$ for seven-layer graphene. Assuming a linear dependence of the temperature coefficients on the number of layers, we extrapolated the values of χ for few layer graphene samples. The power coefficients were uniquely found from Raman analysis and estimated values for two-, three- and four-layer graphene were -0.7 x 10^3, -0.31 x 10^3, -0.5 x 10^3 $cm^{-1}W^{-1}$ respectively. Absorption coefficient characterizes what fraction of the total laser power gets absorbed in the flake. Through calibration studies the absorption coefficients η for flakes with two, three or four layers were estimated as 0.054*N*, where *N* is the number of layers. It was found, however, that the coefficient η for single-layer graphene is not significantly different from that for two-layer graphene, and it is equal to 0.11. The thickness of multilayer graphene is considered to be integer multiple of the thickness of single layer graphene.

The thermal conductivity of few layer graphene was extracted from the power dissipated in the sample, the resulting temperature rise and the flake geometry through the numerical solution of the heat diffusion equation. We developed the model by specifying the geometry of the object, internal properties and boundary conditions. By solving numerically the Fourier's Law of heat conduction, an overall picture of heat propagation in the flake can be created (Figure 4.20). The graphene flakes were simulated as three-dimensional objects with finite thicknesses. However, it was assumed that the heat propagates isotropically only in two dimensions, in plane parallel to the largest surfaces of the 3-D object. Figure 4.20 depicts the schematic of the thermal conductivity measurement of suspended FLG flakes with excitation laser light. Away from the trenches, large graphitic or metallic pieces were placed on top of the flakes. Those pieces served as heat sinks which were kept at a constant ambient temperature T_0 = 300 K. Other surfaces were isolated from interactions with the environment. We considered that the excitation laser light followed Gaussian distribution and the peak of this distribution was located at the geometrical center of the trench zone. The power of the laser during the experiment was set to be approximately equal to 2 mW and we estimated that the spot was contained within the circle of 1μm diameter with FWHM power at the radius of the laser source. Volume integral of the power distribution, equals the power dissipated by the laser source. To describe the Gaussian heat source within the flake per unit volume we considered that $Q = P(x, y) = P_0 \exp\left(-\frac{x^2 + y^2}{2\sigma^2}\right)$, where P_0 is the maximum power and σ = 0.425 μm is the sigma of the Gaussian distribution.



(a)

(b) 2-layer



(c) 3-Layer

(d) 4-Layer

Figure 4.20: (a) Schematic of the experimental setup of thermal conductivity measurement of suspended FLG flakes with excitation laser light. (b), (c), (d) Temperature profile of the flakes heated with the Gaussian source. The excitation power is P_D = 2 mW and the thermal conductivity is K = 2500 $\mathrm{Wm^{-1}K^{-1}}$. Shapes of the flakes were taken from SEM images. Figure 4.20 (b), (c), (d) are after S. Ghosh, W. Bao, D. L. Nika, S. Subrina, E. P. Pokatilov, C. N. Lau and A. A. Balandin, "Dimensional crossover of thermal transport in few-layer graphene," *Nature Materials*, 9, 555 (2010)

The result of the simulation run is a two-dimensional temperature profile of the flake. For every simulated flake we studied the function $K = f\ (\theta^1)$ assuming that the temperature coefficient, χ is constant. Since $\theta^1 = \delta P/\delta\omega = \delta P/\chi\delta T,$ one can input different values of the simulated K and obtain the corresponding power coefficient, θ. For each flake a unique function $K = f\ (\theta^1)$ was obtained. Using this function for every flake we could extract the thermal conductivity of few layer graphene flakes when the value of θ is assigned from the experimental data [88].

Figure 4.21 presents the extracted thermal conductivity as a function of the number of atomic planes, n in FLG. The maximum and average K values for SLG are also shown. As the thermal conductivity of graphene depends on the width of the flakes [89, 90] the data for FLG are normalized to the width 5 µm to allow for direct comparison. The extracted thermal conductivity of few layer graphene at room temperature is lower than that of single layer graphene and changes from K~2800 $Wm^{-1}K^{-1}$ to ~1300 $Wm^{-1}K^{-1}$ as the number of atomic planes increases from n=2 to n =4. As the number of atomic planes increases, the thermal conductivity of FLG decreases all the way to the in-plane bulk graphite limit. The errors associated with the laser spot size and intensity variation were ~8%, i.e. smaller than the error associated with the local temperature measurement by Raman spectrometer (~10-13%). The results were also cross checked with the assumption of a disk shaped source to take into account local hot spots which might be formed. At fixed W, the changes in the value of K with n mostly result from modification of the three-phonon Umklapp scattering. The thermal

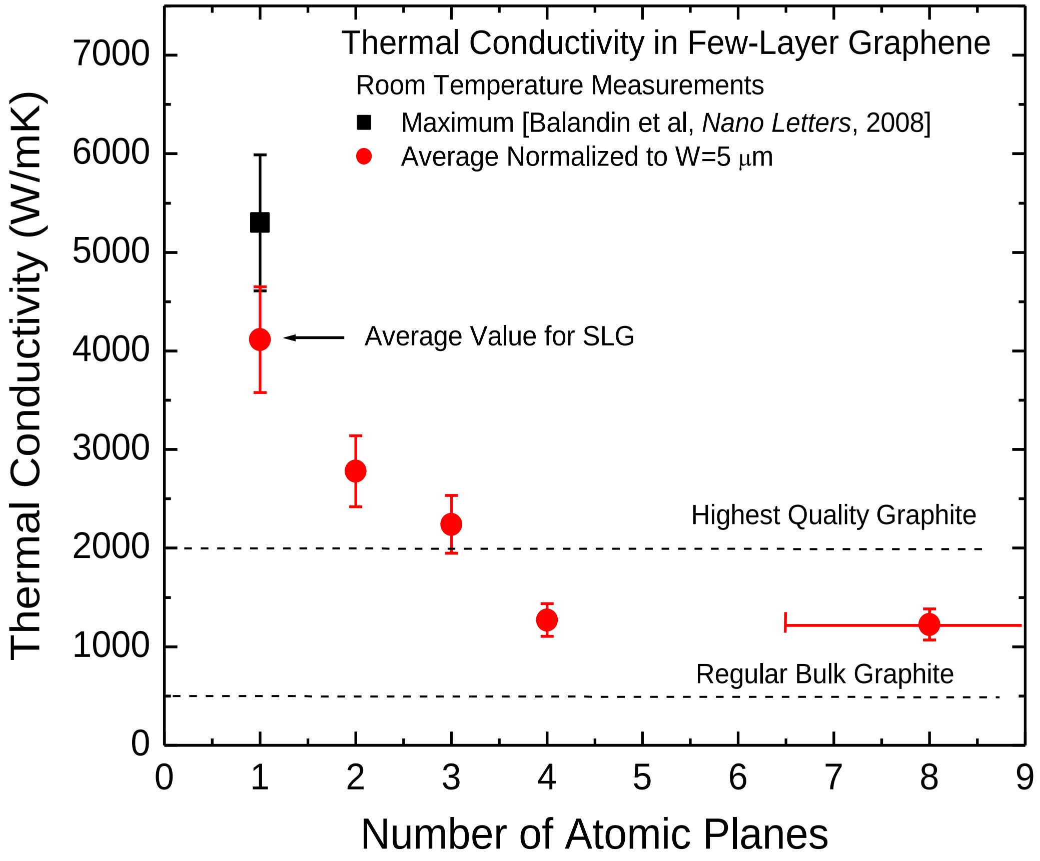
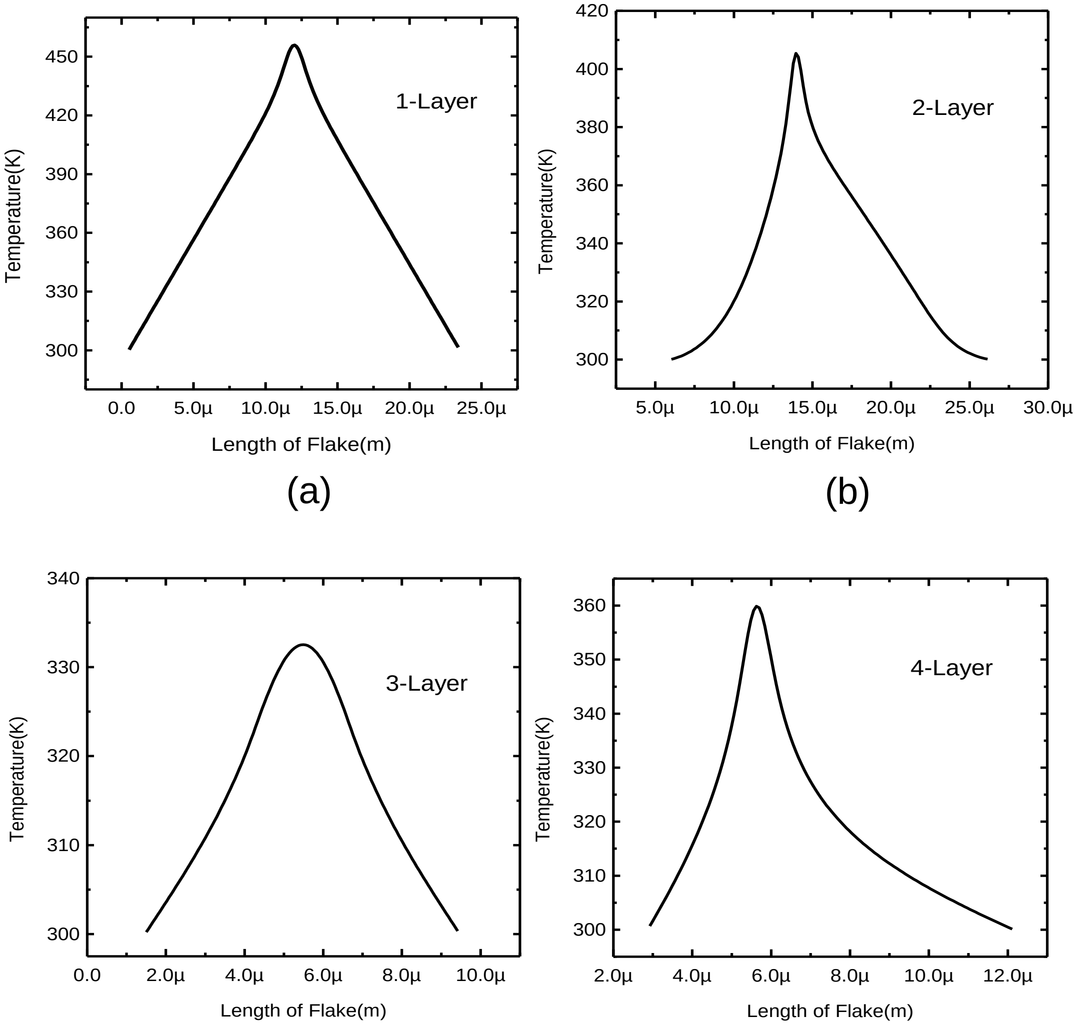


Figure 4.21: Extracted thermal conductivity as a function of the number of atomic planes in FLG. The dashed straight lines indicate the range of bulk graphite thermal conductivities.

transport in our experiment is in the diffusive regime because L is larger than the phonon MFP in graphene, which was measured [83] and calculated [91] to be around ~800nm near room temperature. Thus, we explicitly observed heat conduction crossover from 2D graphene to 3D graphite as the number of atomic planes changes from 2 to ~8. It is illustrative that the measured K dependence on FLG thickness $h \times n$ (h = 0.35 nm) is opposite from what is observed for conventional thin films with thicknesses in the range of a few nanometres to micrometres. In conventional films with thickness smaller than the phonon MFP, thermal transport is dominated by phonon-rough-boundary scattering. The thermal conductivity can be estimated from $K = (1/3)C_V v^2 \tau$, where C_V is the specific heat and v and τ are the average phonon velocity and lifetime. When the phonon lifetime is limited by the boundary scattering, $\tau = \tau_B$, one can use the Ziman formula, $\left(\frac{1}{\tau_B}\right) = \left(\frac{v}{H}\right)((1-p)/(1+p))$, which shows that K scales down with decreasing thickness (here p is a parameter defined by the surface roughness). In FLG with 2 or 3 atomic layer thickness there is essentially no scattering from the top and back surfaces (only the edge scattering is present [90]). Indeed, FLG is too thin for any cross-plane velocity component and for random thickness fluctuations, that is, $p \approx 1$ for FLG. To understand the thermal crossover one needs to examine the changes in the intrinsic scattering mechanisms limiting K: Umklapp scattering resulting from crystal anharmonicity. The trend of thermal conductivity quenching of few layer graphene with the addition of number of layers is in agreement with the theoretical work of Berber *et al*. [92]. We also performed the simulation for a disk shaped source to take into account local hot spots which might be formed in nanoscale devices. The result shows similar trend of decreasing thermal conductivity with the increase of *n* but with little higher values.

Figure 4.22 represents the one-dimensional temperature profiles along the flakes. For each flake the profiling line is drawn through the geometrical center of the trench zone (the point of the P_{peak}) and the middle of the left side of the flake. Clearly, the dimensions and the geometries of the flakes define the temperature profiles. If the heat sinks are closer to the center of the Gaussian heat source, the fall of the temperature along the flake is steeper, and the maximum temperature is lower in overall.



(a) (b)

(c) (d)

Figure 4.22: Simulated temperature profile along the length of the flake: (a) single-layer, (b) two-layer, (c) three-layer and (d) four- layer.

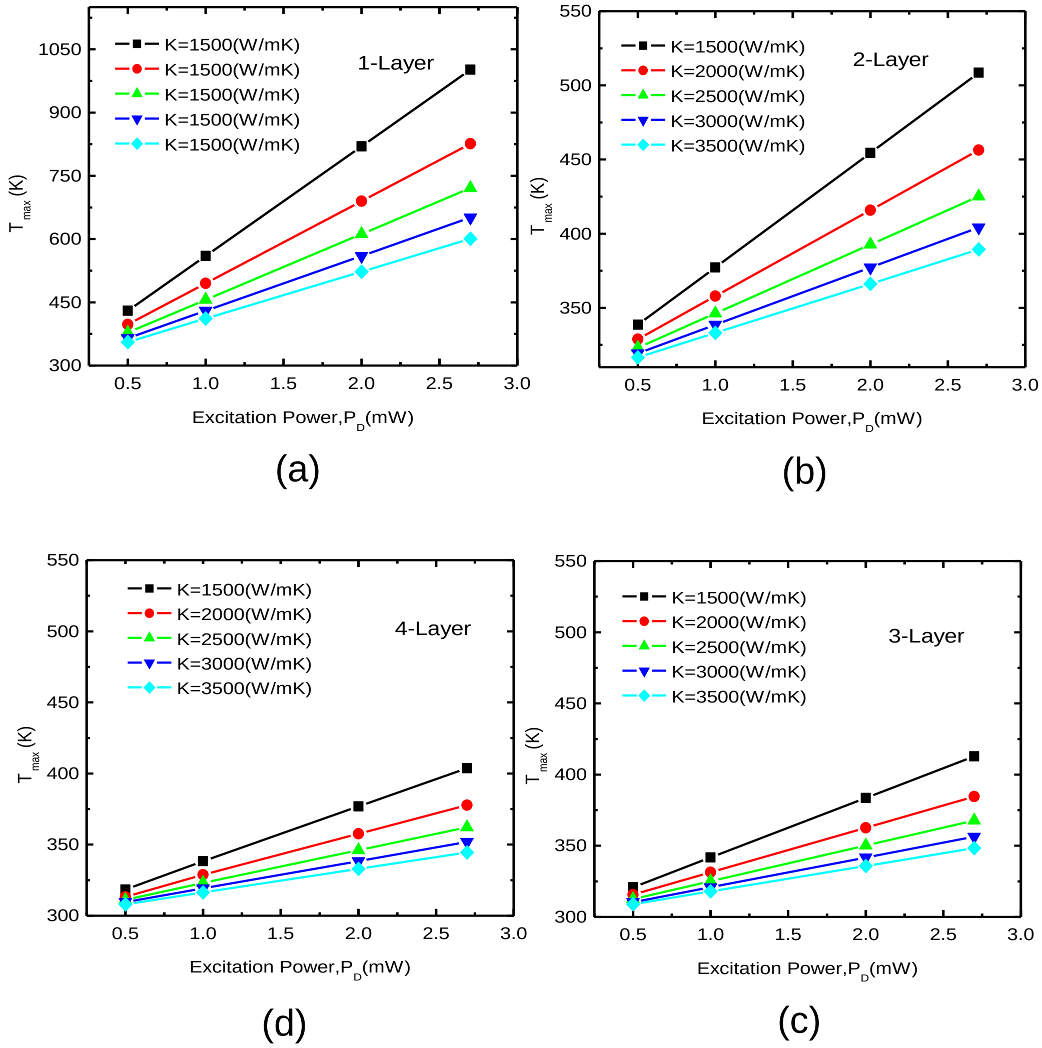


Figure 4.23: Temperature at the center of the laser spot (Gaussian source) as a function of the detector power for different values of thermal conductivity of few layer graphene.

Figure 4.23 shows the maximum temperatures as functions of the detector power for particular values of the thermal conductivity. Inspection of the plots in Figure 4.23 allows us to state that the temperature increases with the increase of the detector power. We observe similar trend in case of single layer graphene. But the maximum temperature rises faster in single layer graphene than that in few layer graphene as the power increases. The higher thermal conductivity of graphene results in lower maximum temperature for all samples of few layer graphene flakes.

Chapter 5

Modeling and Simulation Study of Graphene Application for Electronic Chips Cooling

5.1 GRAPHENE HEAT SPEAREDS IN SOI INTEGRATED CIRCUITS

Silicon technology continues to advance exponentially in both performance and productivity over the past few decades. Silicon-on-Insulator (SOI) technology offers several advantages over traditional silicon device structure such as improved electrical isolation, reduced parasitic capacitances, improved radiation hardness, higher packing density. But the buried insulator in SOI metal-oxide-semiconductor field-effect transistor (MOSFET) structure provides electrical as well as thermal isolation of the active channel from the substrate. As a result, the temperature rise in SOI MOSFETs can become excessive leading to performance degradation and early thermal breakdowns [93-95]. In addition, the down-scaling and higher circuit speeds lead to even high power densities, increased heat generation and temperature rises [18, 96]. So efficient thermal management becomes an integral part of device design for long-term reliability and optimum performance. Traditional means of heat removal (liquid cooling, air blowing, and external heat sinks) still remain ineffective for hot-spot removal in the region near drain-source current or new interconnect wiring. One of the possible approaches to mitigate the self-heating problems is the high-heat-flux hot-spot removal via incorporation into the chip designs of materials with the high thermal conductivity. Single layer graphene is a superior heat conductor with the room temperature (RT) thermal conductivity in the range of 3080 – 5300 $Wm^{-1}K^{-1}$ [47, 83]. Moreover, the flat

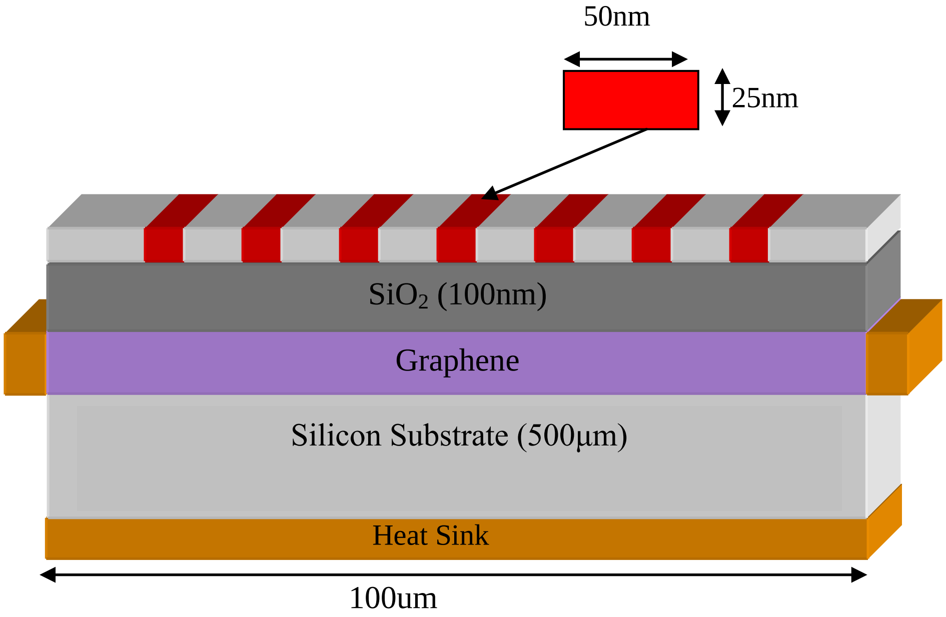


Figure 5.1: Schematic of the MOSFET-based circuit on SOI with the graphene lateral heat spreader attached to side heat sinks. The thicknesses are not to scale. This image is after S. Subrina, D. Kotchetkov and A. A. Balandin "Heat removal in silicon-on-insulator integrated circuits with graphene lateral heat spreaders," *IEEE Electron Device Letters*, 30, 1281 (2009). The image is reprinted with permission from *IEEE*.

geometry of graphene allows it to be readily incorporated into the device structure. The heat propagates laterally within the graphene plane, which results in an increase in the area of heat dissipation, reduction of the heat flux and more efficient thermal management.

In order to evaluate the feasibility of the use of graphene for thermal management we simulate heat propagation in SOI structures with and without graphene layers. In our model we approximate several MOSFETs as rectangular channels generating heat (see Figure 5.1). Each channel, formed between the source and drain, has the width and thickness of 50 nm and 25 nm, respectively. The heat source in each channel is expressed as power normalized by unit length (W/mm units). The heat sources are separated from each other by 10 μm. The thicknesses of the silicon substrate, the buried oxide layer and the surface silicon film are 500 μm, 100 nm and 25 nm, respectively, while their thermal conductivities are assigned to be 155 $Wm^{-1}K^{-1}$, 1.38 $Wm^{-1}K^{-1}$ and 155 $Wm^{-1}K^{-1}$, respectively [97]. A heat sink is attached to the device structure at the bottom. A graphene heat spreader layer, when used, is sandwiched between the oxide layer and the silicon substrate. The two ends of the graphene layer are attached to the side heat sinks, thus forming the lateral channel for heat escape.

The simulations of the heat propagation were carried out with the help of the finite element method using COMSOL software. The heat conduction was modeled by solving numerically the Fourier's law

$$-\nabla \cdot (K \nabla T) = Q, \tag{5.1}$$

where Q is the heat source, which is defined as the heat energy generated within a unit volume per unit time [W/m^3], T is the absolute temperature [K] and K is the thermal conductivity [W/mK]. The internal boundaries between the components of the chip were assumed to be thermally continuous and were described as:

$$n \cdot (K_1 \nabla T_1 - K_2 \nabla T_2) = 0, \tag{5.2}$$

where n is the magnitude of the unit vector normal to the contact surface of the components. The bottom surface of the substrate and the two opposite ends of the graphene heat spreader were kept at a constant temperature T_0 = 300 K. The external surfaces were modeled as insulated from environment, i.e. the temperature gradients across these surfaces were set to zero. This assumption simplifies the model but is reasonable since air has negligible thermal conductivity (0.024 Wm^{-1}K^{-1}), thus the heat transfer from device to air can be ignored.

5.1.1 Chip with and without graphene lateral heat spreader

Simulation runs allowed us to study temperature profiles of the SOI MOSFET-based circuit with and without the embedded graphene heat removal component. The maximum temperatures in the circuit were computed for different circuit configurations and simulation conditions. In these simulations the thermal conductivity of graphene or FLG was assumed to be within the range from 1000 Wm^{-1}K^{-1} to 5000 Wm^{-1}K^{-1}. The decrease in the value of graphene thermal conductivity from the maximum reported for the large

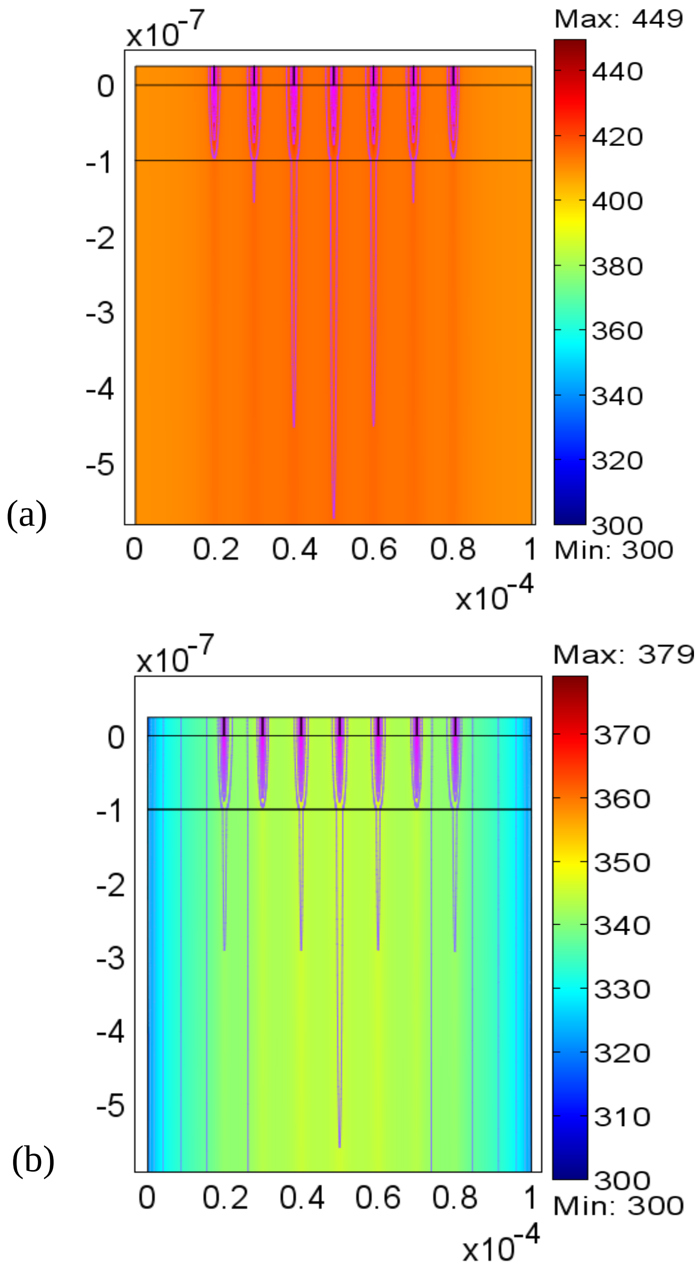


Figure 5.2 Temperature distribution across SOI-based circuit with seven active transistors (a) without and (b) with graphene heat spreaders attached to the heat sinks. The spreaders are embedded between SiO_2 layer and the substrate. The thermal conductivity of graphene is assumed to be 5000 $Wm^{-1}K^{-1}$. The results are after S. Subrina, D. Kotchetkov and A. A. Balandin "Heat removal in silicon-on-insulator integrated circuits with graphene lateral heat spreaders," *IEEE Electron Device Letters*, 30, 1281 (2009). Reprinted with permission from *IEEE*.

suspended flakes can come up as a result of the flake size dependence (phonon – edge scattering), temperature rise and the interface effect [89, 90]. Figure 5.2 shows the calculated temperature profiles for the SOI circuit (a) without the lateral heat spreader and (b) with the graphene heat spreader. The linear power density of each active channel was set to 0.5 W/mm. For a given parameters of the structure and a number of transistors the maximum temperature in the hot spots decreases by 70 K when graphene layers are embedded in the chip.

5.1.2. Heat removal from chips with different active devices

The effect of the graphene lateral heat spreaders is more pronounced when the number of transistors increases. In Figure 5.3 we show for comparison the temperature rise in the SOI-based chip with seven MOSFETs and in a chip with just one MOSFET. The temperature drop owing to incorporation of the single-layer graphene heat spreader is about ~ 23 % in the seven finger chip while in the structure with one device it is ~ 11 %. The overall cooling of the device structures with the lateral heat spreaders also depends on the distance between the heat generating devices, their geometry, thickness of the substrate, overall size of the chip and power dissipated in each device.

The thickness of the substrate has a profound effect on the maximum temperature in the circuit, since the bottom of the substrate is attached to the heat sink, and the substrate complements a heat removal function of the graphene layer. Figure 5.4 shows

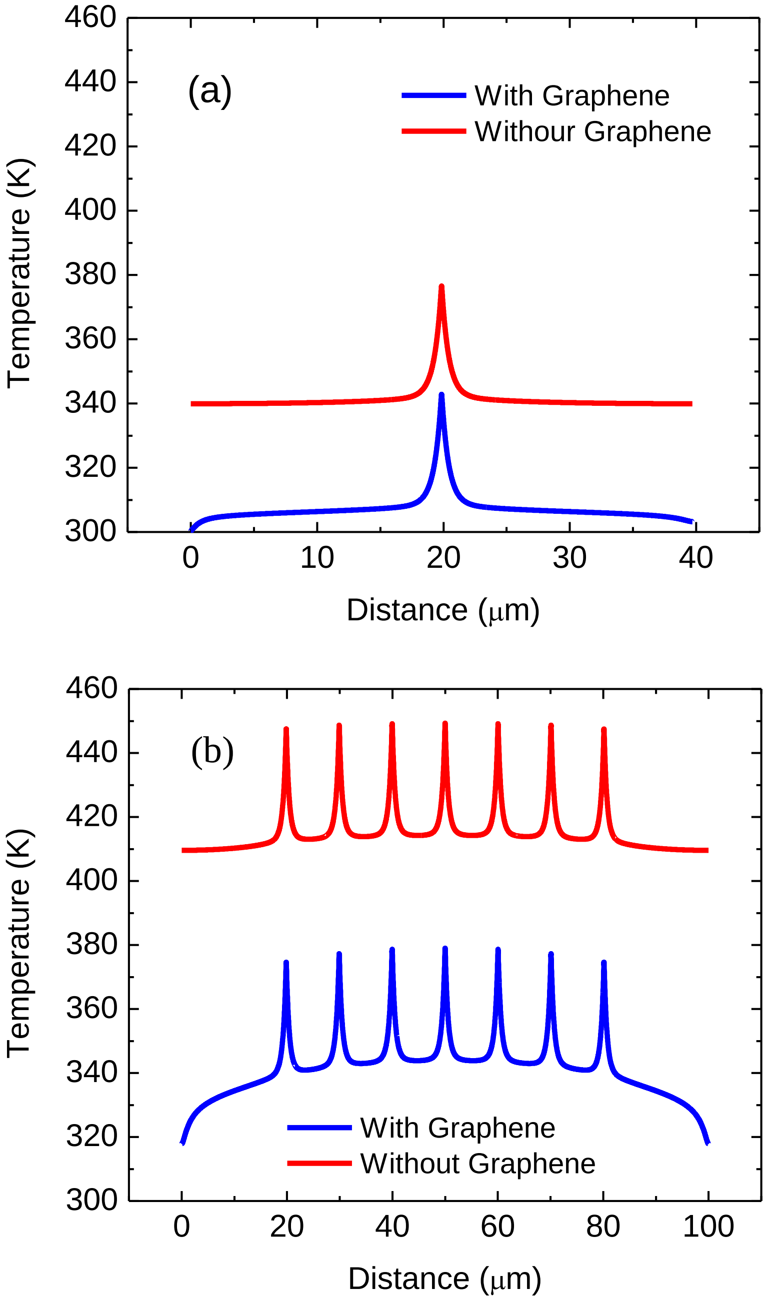


Figure 5.3: Temperature profile along the top surface of the SOI-based MOSFET with (black) and without (red) graphene heat spreaders for chips with (a) single and (b) seven active devices (fingers). The power dissipated in each device is 0.5 W/mm.

that the maximum temperature in the circuit is a weak function of the graphene thermal conductivity (when this thermal conductivity is considered over a substantially wide range of values from 1000 $Wm^{-1}K^{-1}$ to 5000 $Wm^{-1}K^{-1}$). Such dependence becomes weaker when the thickness of the substrate increases. Expectedly, since the substrate is attached to the heat sink, the increase of the substrate thickness leads to the reduction in the maximum temperature.

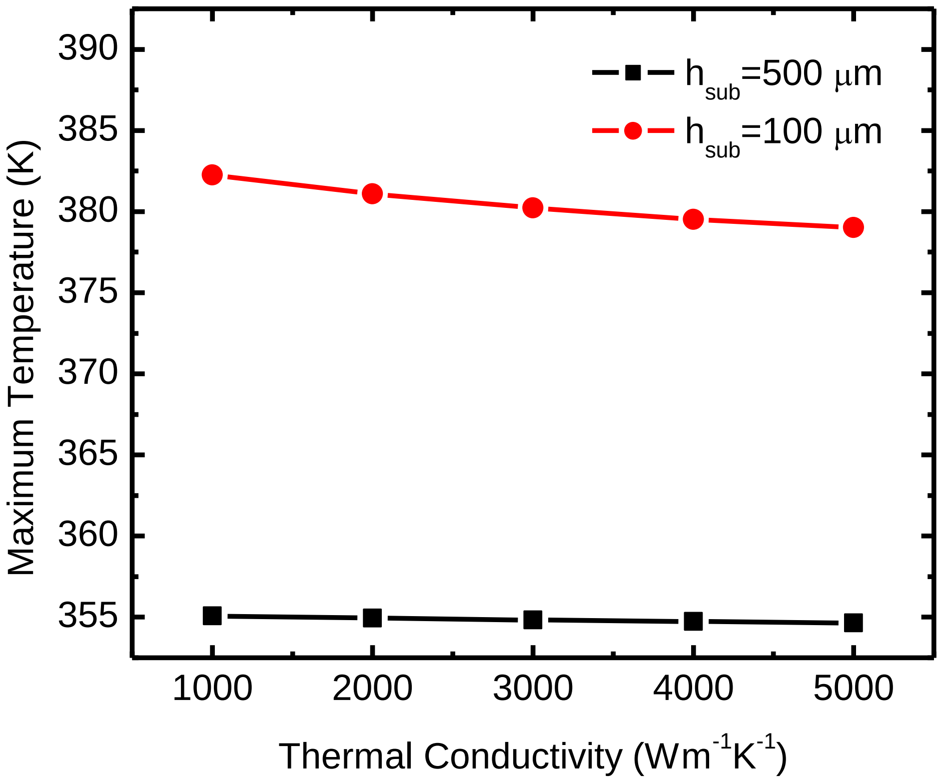


Figure 5.4: Maximum temperature in the circuit as a function of the graphene thermal conductivity for two simulated thicknesses of the substrate.

5.1.3. Use of few layer graphene heat spreaders

It is important to understand how the heat spreading ability of graphene or FLG layer depends on its thickness and the value of the thermal conductivity. The chip cooling with graphene under-layers is within the general approach referred to as high-heat flux thermal management. It might be more beneficial and technologically feasible to use FLG instead of single layer graphene. The thermal conductivity of FLG is extracted to be lower approaching that of bulk graphite (around ~2000 $Wm^{-1}K^{-1}$ at room temperature along the basal plane) [98]. At the same time, the mechanical and thermal properties of FLG are expected to be less subject to degradation when the layer is embedded between the oxide and the substrate. Figure 5.5 shows the simulated maximum temperature of the SOI chip as the function of the values of the thermal conductivity and thicknesses of the heat spreader. The general trend is that the cooling becomes more efficient with the increasing thermal conductivity and thickness of the spreader owing to the increasing heat flux directed to the side heat sinks. Our results suggest that the lateral heat spreaders with the number of atomic planes between three and ten would be efficient. This is encouraging news for practical applications that allows for greater flexibility with the sample preparation. The continuing progress in epitaxial growth of FLG may allow in the future for convenient fabrication of the lateral FLG heat spreaders.

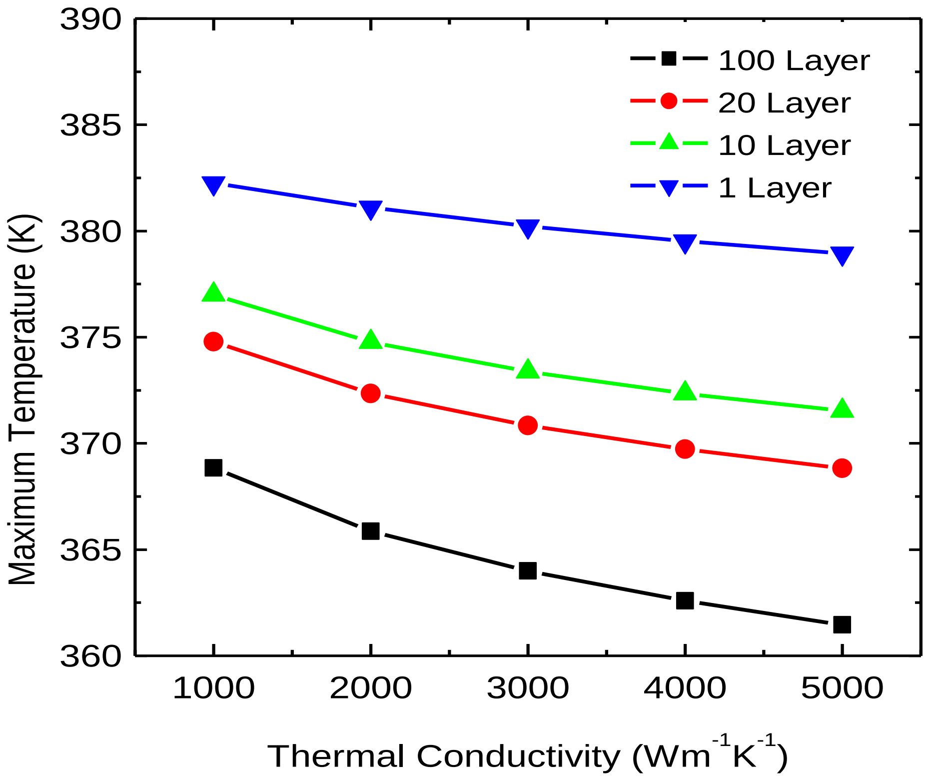


Figure 5.5: Maximum temperature in the SOI chip as a function of the thermal conductivity of the lateral heat spreader. The number of graphene atomic planes in the layers was varied from 1 to 100. The thickness of each atomic plane is 0.35 nm. The figure is after S. Subrina, D. Kotchetkov and A. A. Balandin "Heat removal in silicon-on-insulator integrated circuits with graphene lateral heat spreaders," *IEEE Electron Device Letters*, 30, 1281 (2009). The figure is reprinted with permission from *IEEE*.

Due to its strong sp^2 bonds it is preferable to use FLG for in-plane heat conduction. That was reflected in our heat spreader design. Analogously, bulk graphite is a much better conductor of heat in the in-plane direction than in the cross-plane direction: the difference in thermal conductivity values is two orders of magnitude at RT. At the same time the heat conduction through the plane of the graphene or FLG heat spreaders

Table 5.1: Maximum chip temperature for different cross-plane thermal conductivities.

Cross-Plane K_z ($Wm^{-1}K^{-1}$)	Maximum Temperature (K)
0.001	426
1	379
10	379

still exists. We model the effect of the cross-plane thermal coupling by assuming some cross-plane thermal conductivity K_z values. This thermal conductivity should be viewed as an effective value, which describes heat conduction through FLG and oxide layer to the substrate. It includes possible effect of the thermal boundary resistances. Table 5.1 shows simulated maximum temperatures in the circuit with a single-layered graphene heat spreader. The in-plane thermal conductivity is assumed to be equal to 5000 $Wm^{-1}K^{-1}$ and the heat source of each active channel is set to 0.5 W/mm.

The simulation results show even a small value of the cross-plane thermal coupling give reasonable temperature rise. The variation of the cross - plane thermal conductivity in the physically reasonable range $K_z > 1$ $Wm^{-1}K^{-1}$ do not produce string effect on the maximum chip temperature. The latter is explained by the fact that in our design the lateral heat spreaders are attached to the side heat sinks creating a path for heat escape. At the same time, the effect of the cross-plane thermal conductivity on the temperature rise depends on the specifics of the layered structure and overall power dissipation in each device.

5.2 COPPER INTERCONNECTS EMBEDDED WITH GRAPHENE HEAT SPEADERS

Power dissipation results from self-heating across interconnect network is another source heat generation and temperature rise within electronic circuits. We did thermal modeling to show the effect of graphene heat spreaders within interconnect hierarchy for the purpose of heat removal. In our model, we assume that heat is generated by self-heating in several MOSFET active regions between source and drain and also in circuit interconnects. The width and thickness of each device are assigned to be 40 nm and 30 nm, respectively and these are separated from each other by 10 μm. We model several copper interconnect layers with thicknesses of 236 nm, 200 nm and 170 nm. Thermal conductivity of copper interconnect is assigned to be 400 $Wm^{-1}K^{-1}$. The thickness of oxide layer between the interconnects and interconnect and heat spreader are 2.9 μm and 100 nm, correspondingly and the value of thermal conductivity is 1.38 $Wm^{-1}K^{-1}$. Figure 5.6 shows the cross sectional view of the simulated circuit. The heat source is expressed as power normalized by unit length (W/mm units). The thicknesses of the silicon substrate, the buried oxide layer and the device layer are 500 μm, 100 nm and 30 nm, respectively, while their thermal conductivities are assigned to be 155 $Wm^{-1}K^{-1}$, 1.38 $Wm^{-1}K^{-1}$ and 155 $Wm^{-1}K^{-1}$, respectively. A reference temperature is maintained at the bottom of the device. Graphene, when used as a heat spreader, is embedded underneath the device layer and metal layers with two side heat sinks in order to form lateral channel for heat escape.

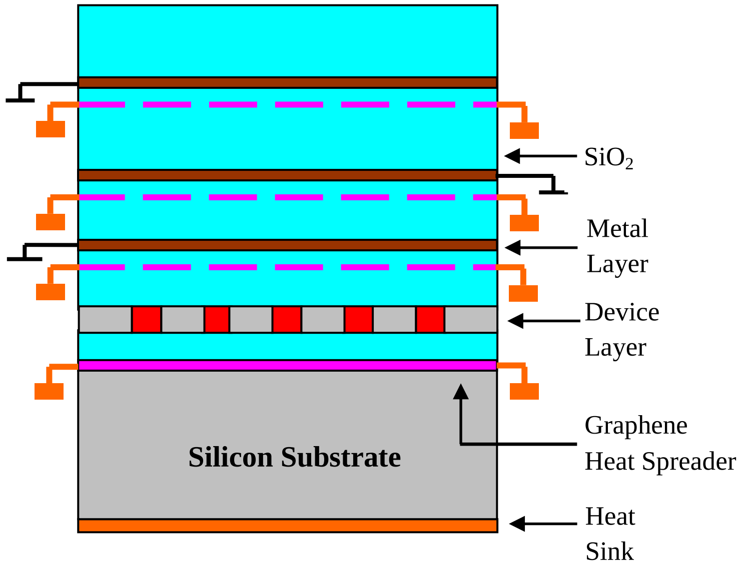
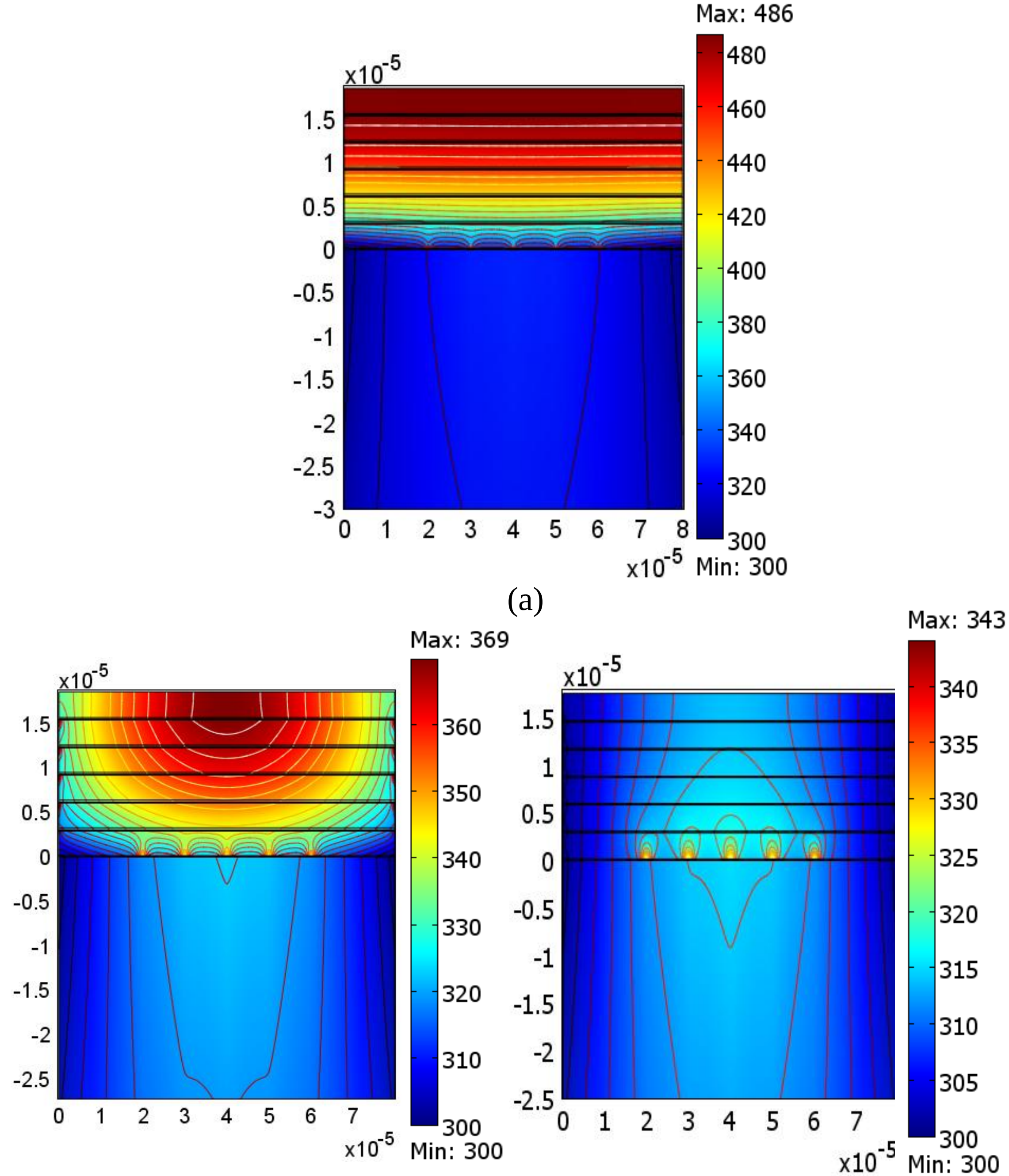


Figure 5.6: Schematic cross-section of a circuit on SOI substrate with graphene lateral heat spreaders for heat removal from localized hot spots and interconnects. Heat sinks are attached to the graphene heat spreaders at the sides and a main heat sink at the bottom.

We simulate heat propagation in SOI structures with and without graphene layers underneath the interconnects. Finite element analysis was performed to solve Fourier's law of heat conduction. The internal boundaries among the components of the circuit were assumed to be thermally continuous i.e., the heat flux was continuous across the boundary. The bottom of the substrate and the ends of graphene heat spreaders were kept at constant temperature, T_0 = 300 K. The external boundaries were adiabatic and were defined as, $n \cdot (K \nabla T) = 0$ i.e., the temperature gradients across these boundaries were zero.



(a)

(b) (c)

Figure 5.7: Temperature distribution across SOI-based circuit consisting of active transistors and (a) copper interconnects without heat spreaders (b) copper interconnects embedded with graphene heat spreaders (c) graphene that performs the dual function of interconnects and lateral heat spreaders. The thermal conductivity of graphene is assumed to be 5000 $Wm^{-1}K^{-1}$.

Figure 5.7 shows the temperature profiles for the circuit (a) without and (b) with the graphene heat spreaders embedded underneath the interconnects. The linear power density of each active device and interconnect was set to 0.5 W/mm. The graphene component was thought to be single-layered (the thickness of single-layered graphene is ~0.35 nm) and the value of thermal conductivity was 5000 $Wm^{-1}K^{-1}$. It is seen that the maximum temperature in the chip with specific configurations is dropped by 117 K with graphene heat spreaders. The temperature of the circuit continues to increase with the increase of interconnect layers as well as with the increase of the dissipated power across each interconnect as shown in Figure 5.8. It is also noticeable that the reduction in maximum temperature with graphene heat spreaders is larger when the circuit is hotter. With five metal layers, the maximum temperature drops by 26% while in the circuit with three metal layers it drops by 11% with the incorporation of heat spreaders at 0.5 W/mm.

5.3 GRAPHENE LAYERS AS INTERCONNECTS AND LATERAL HEAT SPREADERS

Graphene has very high RT carrier mobility and very low resistivity with the value of ~ 2×10^5 $cm^2V^{-1}s^{-1}$ and 10^{-8} ohm-m respectively [54, 99]. The resistivity of graphene is approximately twice less than that of copper and copper is most widely used material to form interconnect metal wires. Using the interconnect material that has a low value of resistivity and a high value of thermal conductivity is very efficient for designing novel integrated circuits. Such a material serves to reduce the signal propagation time and at the same time, removes heat from the semiconductor devices at a high rate. The very high

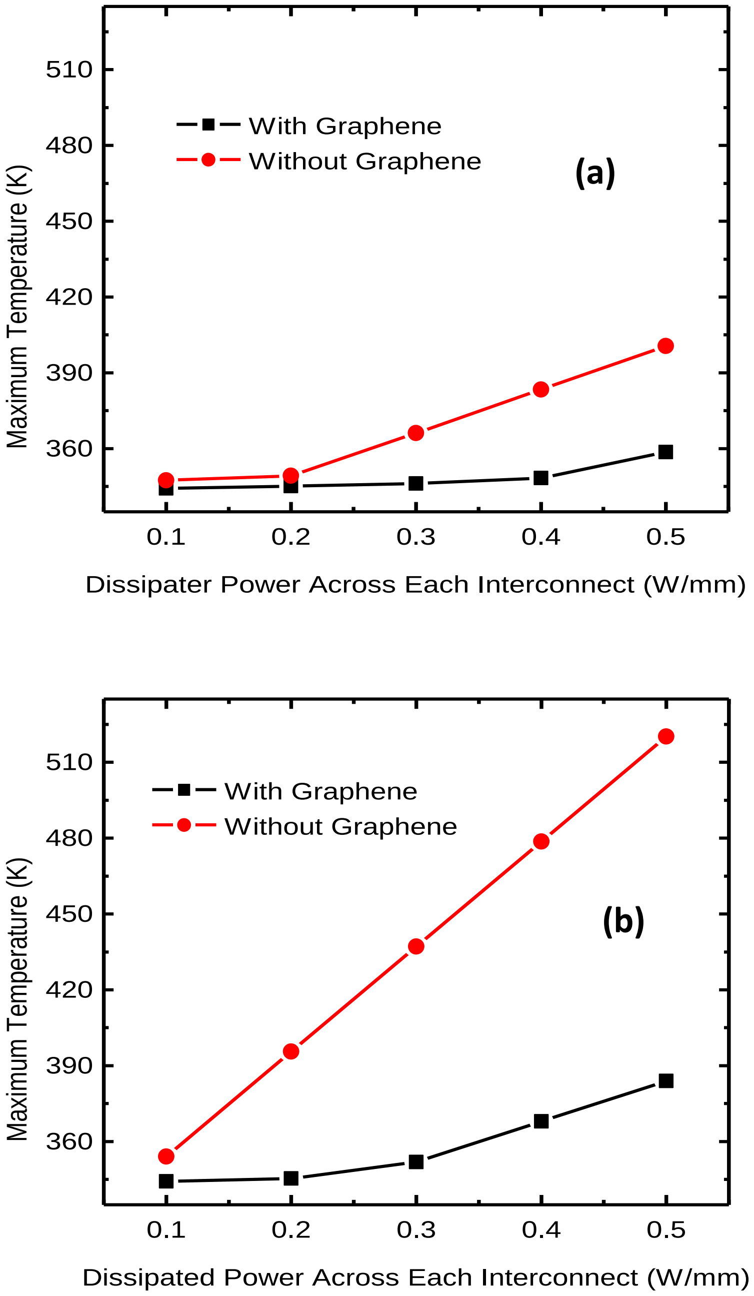


Figure 5.8: Maximum temperature as a function dissipated power across each interconnect layer with (a) three and (b) five interconnects within the circuit. The power dissipated in each device is 0.5 W/mm.

thermal conductivity coupled with its very low resistivity makes graphene as a new core in interconnect technologies. Recent breakthrough in fabrication of large area graphene has stirred up a major interest in potential applications of graphene in electronic systems particularly as transistors and interconnects. We are now interested to observe how graphene performs a dual function of interconnects and, simultaneously, lateral heat spreaders.

As the next step, we assume that the film copper interconnects are replaced by single layer graphene and graphene plays the roles of both interconnects as well as heat spreaders. Figure 5.7 (c) shows the calculated temperature profile for the circuit with graphene interconnects and heat spreaders. The maximum temperature drops by 26 K as compared to that in the chip with copper interconnects and graphene heat spreaders [Figure 5.7 (b)]. This is encouraging since the temperature drop improves the device lifetime. Moreover a high current capacity is critical for interconnect applications and reliability. The current carrying capacity of graphene ribbon is as much as thousand times of the copper. The breakdown current density of graphene ribbon is on the order of ~ 10^{12} A/m^2 [100]. This will resist the electromigration up to a great extends and fulfill the ITRS projections for interconnects.

We also looked into in-plane direct current propagation through the graphene. The current, through the interconnect, flows in one direction from one side to another and the same sides of graphene heat spreader are thermally connected to heat sinks. The direct current conduction in interconnect is described by Ohm’s law as

$$-\nabla \cdot d\,(\sigma\nabla V - J^{e}) = 0, \tag{5.3}$$

where d is the thickness of the interconnect, σ is the electric conductivity [S/m], V is the potential along the interconnect [V] and J^{e} is the external current density [A/m^2]. The electric field is tangential to the xy-plane, the electric potential varies in the x and y directions and is constant in the z direction. The inward flow of current goes through one surface and is given by:

$$-n \cdot J = J_{n}, \tag{5.4}$$

where J_n is the normal current density [A/m^2] and n is the unit vector normal to the surface under consideration while the another surface is grounded to $V = 0$. For simplicity, the other external boundaries are set to be electrically insulated. The direct current creates a heat source Q in the interconnect. The heat conduction in the circuit is solved by using time dependent Fourier's law:

$$\delta_{ts}\rho C_P \, {}^{\delta T}/_{\delta t} - \nabla \cdot (K\nabla T) = Q \tag{5.5}$$

where ρ is the density [kg/m^3] and C_P is the specific capacity at constant pressure [J/(kg.K)]. δ_{ts} is the time-scaling coefficient and the value is assigned to be 1. The external boundaries are considered to be thermally insulated, except the bottom surface of the substrate and the two ends of graphene heat spreaders are connected to heat sinks. Thus, by changing the normal current density and the thermal conductivity, we obtain the effects of these parameters on the temperature profile of the circuit.

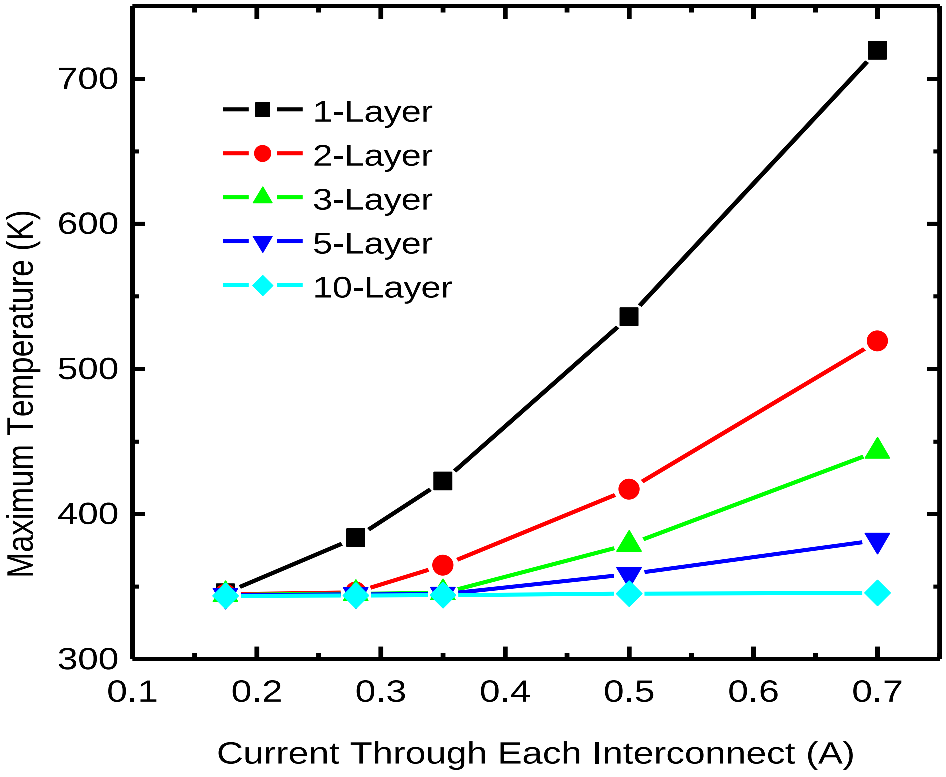


Figure 5.9: Maximum temperature in the SOI chip as a function of current through the graphene interconnects. The thermal conductivity of graphene is assumed to be 5000 $Wm^{-1}K^{-1}$.

In the simulation, electrical conductivities of silicon, oxide layer, copper and graphene are assigned to be 1.23 x 10^{-3} S/m, 5.99 x 10^{-10} S/m, 59.66 x 10^{6} S/m and 1x 10^{8} S/m, respectively while density and specific capacity at constant pressure are 2.3 x 10^{3} kg/m^{3}, 2.6 x 10^{3} kg/m^{3}, 8.7 x 10^{3} kg/m^{3}, 2 x 10^{3} kg/m^{3} and 0.71 x 10^{3} J/(kg.K), 1 x 10^{3} J/(kg.K), 0.385 x 10^{3} J/(kg.K), 0.71 x 10^{3} J/(kg.K), correspondingly. During each simulation run, the current density along the interconnect was assigned to be constant.

The current passing through the interconnect causes heating and rises temperature of the interconnects as well as the entire structure. This effect is expectedly more pronounced as the current through the interconnect increases as shown in Figure 5.9. It is also seen that for constant current through the interconnects, the maximum temperature decreases as the number of atomic planes of few layer graphene increases. This effect is due the decreased current density through the interconnects and increased heat flux towards the heat sink. The linear power density of each active channel was set to 0.5 W/mm.

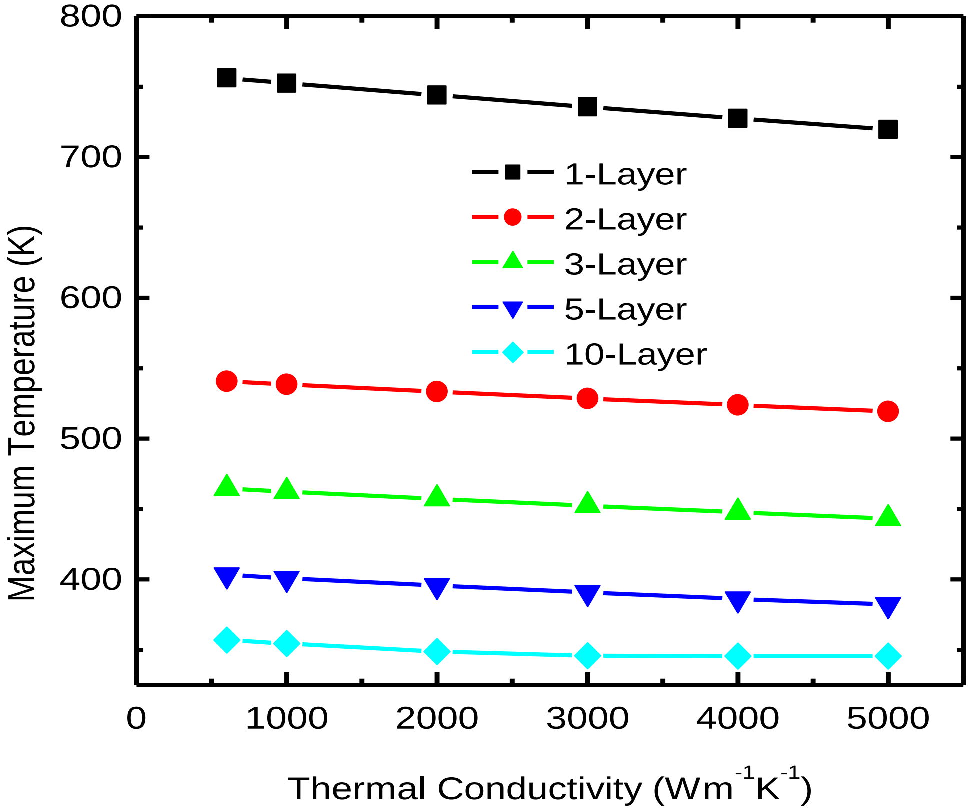


Figure 5.10: Maximum temperature in the SOI circuit as a function of the thermal conductivity of the lateral heat spreaders underneath the interconnect layers. The number of graphene atomic planes in the layers was varied from 1 to 10.

During the simulation runs, the thermal conductivity of graphene or few layer graphene (FLG) was modeled to be temperature independent and to have values within the range from 1000 $Wm^{-1}K^{-1}$ to 5000 $Wm^{-1}K^{-1}$. Figure 5.10 shows how the values of the thermal conductivity and thicknesses of the graphene heat spreaders placed underneath the interconnects layers affect the temperature of the circuit. The current through each interconnect was set to 0.7 A. The trends are very similar to those observed in the cases of the hot spot removal [101]. It shows more efficient cooling as the thermal conductivity as well as the thickness of the heat spreader increases. The thermal conductivity of single layer graphene heat spreader, placed underneath the device layer, was assigned to be 5000 $Wm^{-1}K^{-1}$.

Chapter 6

Design of 3-D ICs with Graphene Heat Spreaders

6.1 GRAPHENE HEAT SPREADERS FOR 3-D INTEGRATED CIRCUITS

With the progress of technological nodes, device dimension is getting smaller and smaller. As more number of devices is accumulated into a single chip, wire length is getting larger and larger which in turn cause increased power dissipation, temperature and interconnect delays. For submicron technology, interconnect delay becomes a dominant factor. These might result serious implications on system performance and reliability. Innovative circuit designs, new interconnect materials and architectures are required to meet the projected chip and system performance. The new interconnect materials such as copper, low-k dielectric offer only a limited improvement in system performance and the interconnect delay is expected to be substantial below 130 nm technology node [102, 103]. Some fundamental changes are needed in system architectures, designs and fabrication technologies in order to achieve significant and scalable solutions to interconnect delay problem and increased device density in future VLSI applications. One emerging solution is three dimensional (3-D) integration.

The 3-D integrated circuits stack multiple layers of active devices into a monolithic structure. They have the potential to enhance chip performance, functionality and power efficiency [104]. By expanding vertically rather than spreading out over a larger area, interconnect lengths are decreased and since propagation delay is proportional to the square of the wire length, overall performance is increased. The shorter wire length can reduce the power consumption by factor of ten to hundred times [105]. In 3-D chip, not only is the total wire length reduced, but also the length of the longest wire. The chip space is better utilized, and device packing densities are increased which extends Moore's law and enables a new generation of tiny but powerful devices. Moreover, large numbers of vertical vias between the layers in 3-D integration allow wider bandwidth buses between functional blocks in different layers. The layers of circuit can be built with different processes, or even on different types of wafers. This gives much larger degree of freedom to optimize circuit components compared to those on a single wafer and more flexibility to heterogeneous integration [106].

Despite the expected advantages of three-dimensional ICs over two-dimensional (2-D) ICs, this new technology faces challenges also. One major challenge of 3-D technology is thermal problem. Thermal effects are expected to be more pronounced because of higher power densities and greater thermal resistance along heat dissipation paths to the heat sinks. Even though the power dissipation per transistor is smaller in 3-D chip, high packing densities cause high power densities [25]. Moreover, due to the poor thermal conductivity of the inter-layer dielectric (ILD) layers, the heat generated by the active devices and interconnects cannot be effectively dissipated towards the heat sinks [107]. These result in higher temperature rise and larger temperature gradient and can cause variations in the performance across the chip and reliability issues. New materials and physical design paradigms are essential to alleviate this thermal issue.

The final goal of this research is the development of the graphene heat spreaders incorporated in 3-D integrated circuits. We carry out steady state thermal simulation within the chip that includes interconnects, active device structures and vertical vias (Figure 6.1). In order to investigate the effects of graphene, it is incorporated in the circuit for the purposes of heat removal. The developed models and simulation tools also allow us to address the architecture and optimum design issues. The studied integration is a two-stratum face-to-face stacking using wafer-to-wafer SiO_2 direct bonding. The first stratum is bulk and the second one is thinned silicon-on-insulator. Each stratum consists of a device layer with several metal – oxide – semiconductor field – effect transistors (MOSFETs) and a number of interconnect metal layers located above the device layer. Heat is produced within the channel of active MOSFETs and also within the interconnect layers due to Joule heating. Each channel, formed between the source and drain, has the length and thickness of 40 nm and 30 nm, respectively and are separated from each other by 10 μm. We model several copper interconnect layers with thickness of 236 nm and thermal conductivity of 400 $Wm^{-1}K^{-1}$. The thickness of oxide layer between the interconnects is 2.9 μm with thermal conductivity of 1.38 $Wm^{-1}K^{-1}$. The thicknesses of

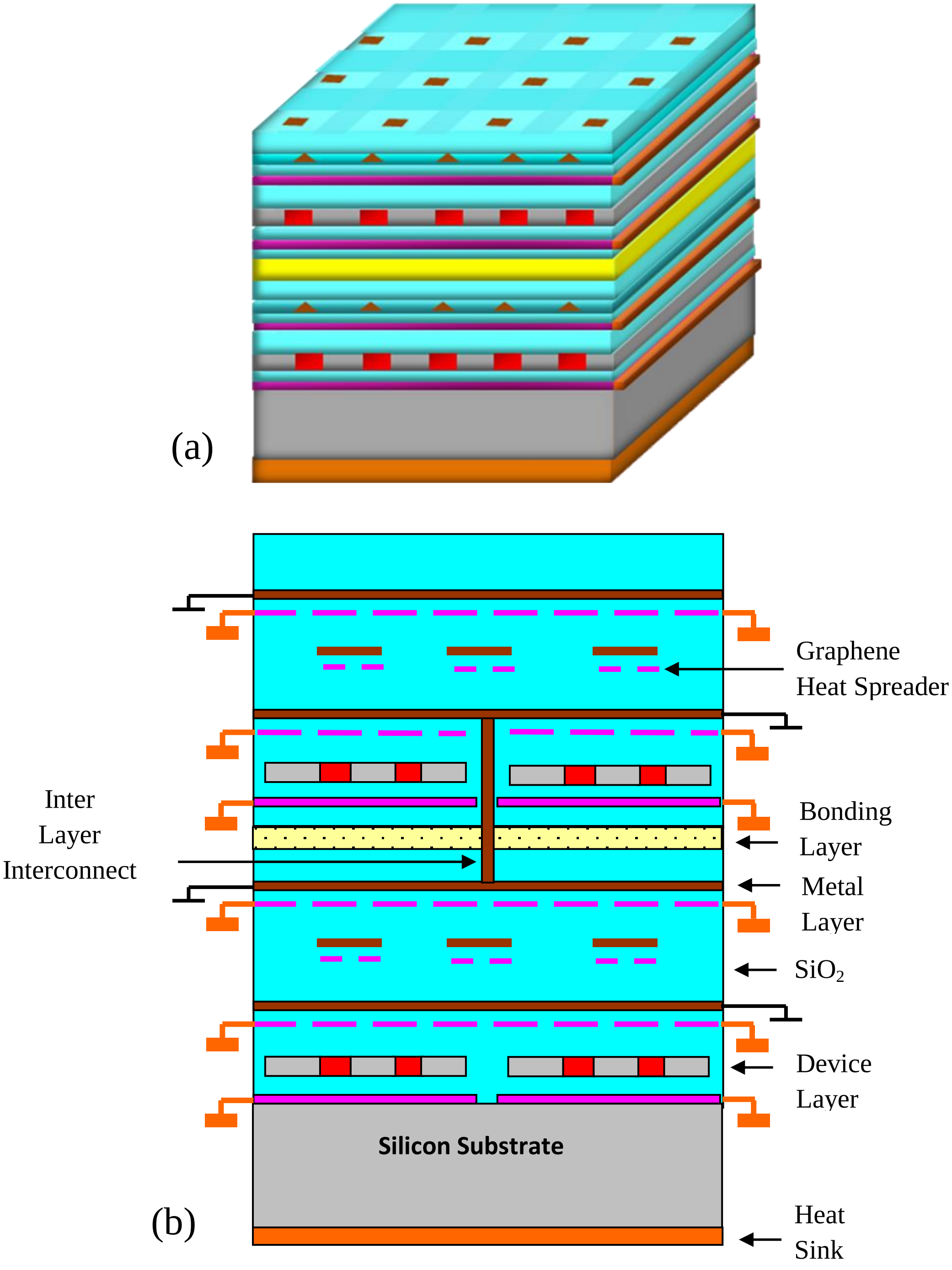


Figure 6.1: Schematic diagram of the 3-D chip with graphene heat spreaders (a) 3D view and (b) Detailed cross-section of Design-1. Graphene heat spreader is used for heat removal from localized hot spots and interconnects. Heat Sink is connected to the bottom of the substrate and two ends of the graphene heat spreaders.

the silicon substrate, the buried oxide layer and the device layer are 500 µm, 100 nm and 30 nm, respectively, while their thermal conductivities are 155 $Wm^{-1}K^{-1}$, 1.38 $Wm^{-1}K^{-1}$ and 155 $Wm^{-1}K^{-1}$, respectively [97]. The two strata are bonded by SiO_2 layer with thermal conductivity of 1.38 $Wm^{-1}K^{-1}$ and thickness of 10 µm. Inter layer interconnect, “super via” is designed to connect the two strata internally. This interlayer via electrically connects vertically adjacent areas and thus reduces wirelengths. The width of this copper via is 500 nm. Graphene heat spreaders are embedded underneath the device layers and interconnect layers. Two side heat sinks are connected to heat spreader for lateral heat escape. A conventional heat sink is attached to the device structure at the bottom of the first stratum.

We performed COMSOL simulations within this two-stratum architecture. A reference temperature was maintained at the bottom of the substrate and the ends of graphene heat spreaders. The internal boundaries among the components of the circuit were thermally continuous and the external boundaries were set to adiabatic. Heat transfer through the external surfaces to the air was ignored. We solved Fourier’s law of heat conduction with the help of the finite element analysis.

$$-\nabla \cdot (K \nabla T) = Q, \tag{6.1}$$

where Q is the heat source, which is defined as the heat energy generated within a unit volume per unit time, T is the absolute temperature and K is the thermal conductivity.

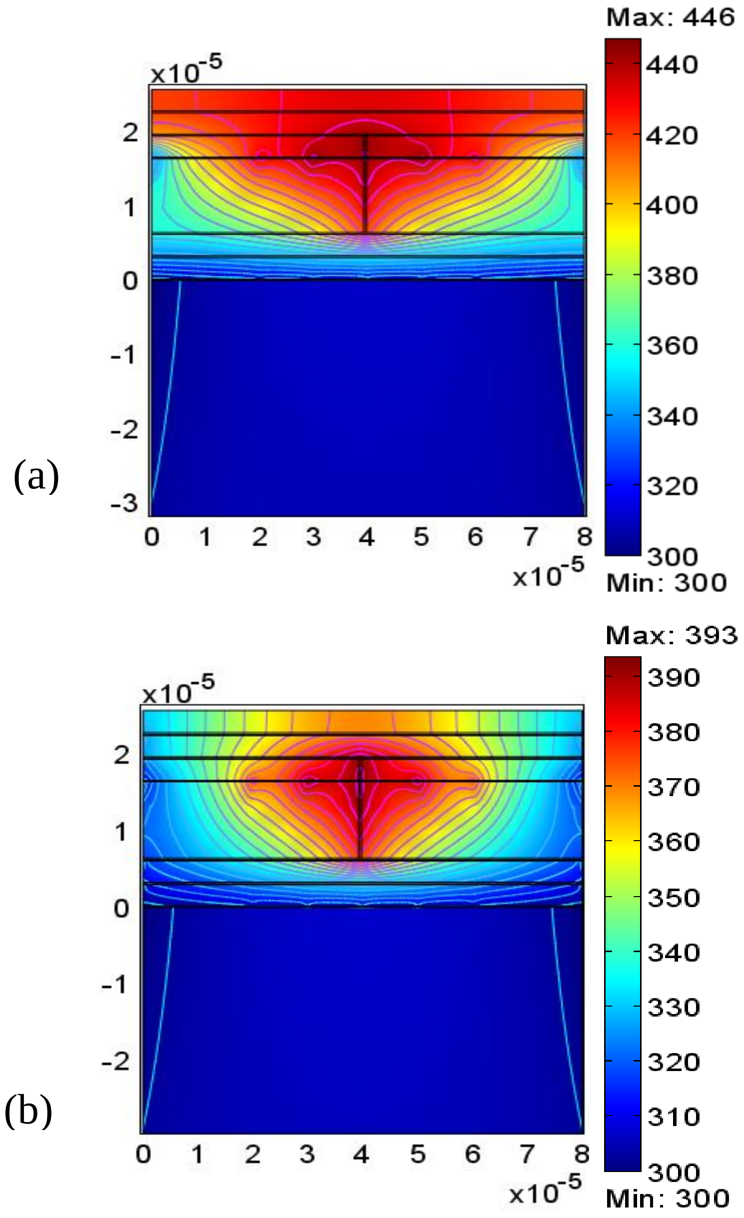


Figure 6.2: Temperature distribution across the 3-D chip with two stratums consisting of one device layer and two interconnect layers per stratum (a) without and (b) with graphene heat spreaders attached to the side heat sinks. The heat spreaders are embedded underneath the device layers and interconnect layers. The thermal conductivity of graphene is set to 5000 $Wm^{-1}K^{-1}$. This figure is after S. Subrina, "Modeling Based Design of Graphene Heat Spreaders and Interconnects in 3-D Integrated Circuits," *J. Nanoelectronics and OptoelectronicsC,* 5, 1 (2010). The figure is reprinted with the permission from ASP.

Figure 6.2 shows the calculated temperature profiles for the 3-D chip without [Figure 6.2 (a)] and with [Figure 6.2 (b)] the graphene lateral heat spreaders embedded within the interconnect hierarchy. The linear power density of each active channel and interconnect were set to 0.10 W/mm and 0.15 W/mm, respectively. The thermal conductivity of single graphene layer heat spreader was assumed to be 5000 $Wm^{-1}K^{-1}$ (the thickness of single-layered graphene is ~0.35 nm) and the value was independent of temperature. For given parameters of the structure, the maximum temperature in the chip with graphene lateral heat spreaders is dropped by 53 K. The reduction in maximum temperature with graphene heat spreader is larger within the chip with more active devices and interconnects.

The use of few layer graphene instead of single layer graphene might be more advantageous since FLG gives greater flexibility with the sample preparation and convenient fabrication. In order to understand the heat spreading ability of graphene or FLG, we calculated maximum temperatures as functions of the values of thermal conductivity and thicknesses of the heat spreaders underneath the interconnect layers. It is seen in Figure 6.3 that cooling is higher within the chip with increased thermal conductivity and thickness of the spreader because of high heat flow towards the heat sinks. During the simulation runs, the thermal conductivity of graphene or few layer graphene were assumed to be within the range from 1000 $Wm^{-1}K^{-1}$ to 5000 $Wm^{-1}K^{-1}$ and to be temperature independent. It is known that the thermal conductivity is a strong function of lateral dimensions [89, 90] and the cross-plane coupling with the changes in

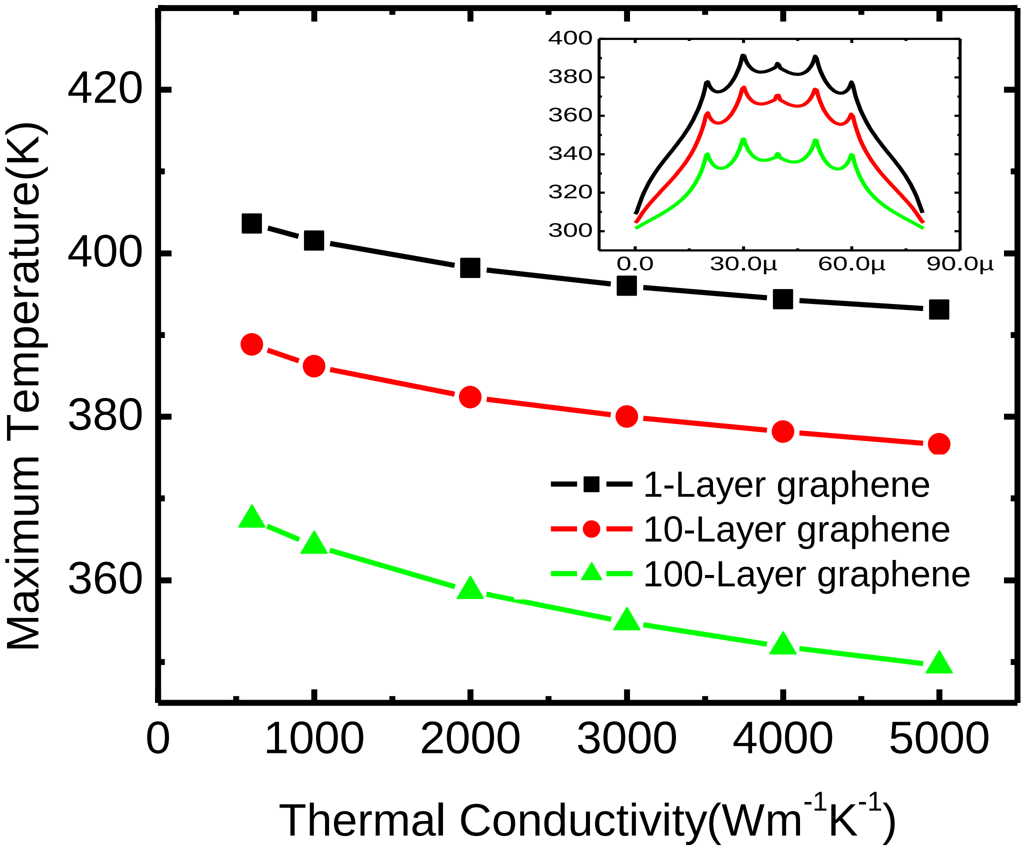


Figure 6.3: Maximum temperature in the 3-D chip as a function of the thermal conductivity of the lateral heat spreader. The number of graphene atomic planes in the layers was varied from 1 to 100 and thickness of each atomic plane is 0.35 nm. The inset shows the temperature profiles along the length of the chip. This figure is after S. Subrina, "Modeling Based Design of Graphene Heat Spreaders and Interconnects in 3-D Integrated Circuits," *J. Nanoelectronics and OptoelectronicsC,* 5, 1 (2010). The figure is reprinted with the permission from ASP.

leads to FLG [98]. The thermal conductivity of single layer graphene heat spreader, place the phonon thermal conductivity decrease to the bulk graphite value Umklapp scattering d underneath the device layer, was assigned to be 5000 Wm^{-1}K^{-1}.

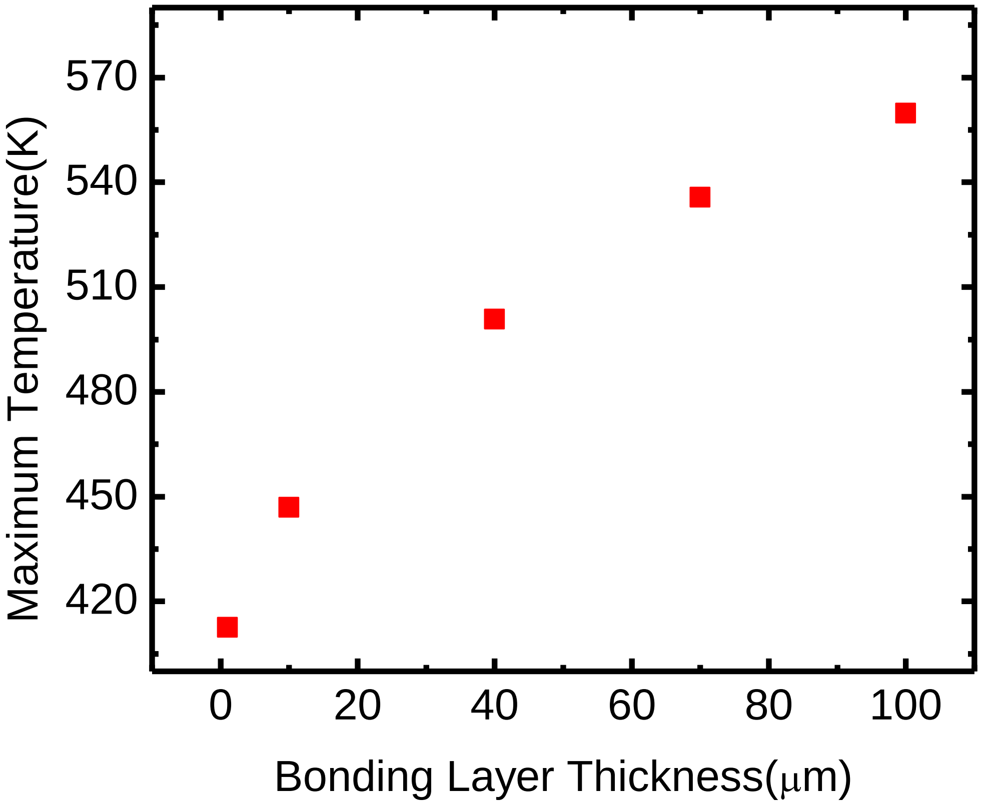


Figure 6.4: Maximum temperature in the chip as a function of the thicknesses of the bonding layer without graphene heat spreaders underneath the interconnect layers. This figure is after S. Subrina, "Modeling Based Design of Graphene Heat Spreaders and Interconnects in 3-D Integrated Circuits," *J. Nanoelectronics and OptoelectronicsC*, 5, 1 (2010). The figure is reprinted with the permission from ASP.

One of the challenges of 3-D integration is the study of wafer-to-wafer bonding quality. Although wafer-bonding techniques vary in their process flow, there are some common 3-D specific manufacturing stages that need to be followed like 1) silicon substrate thinning, 2) wafer alignment, 3) bonding, and 4) vertical interconnect [108]. Individual wafers are bonded following the thinning and polishing of the surface for better bonding quality. Subsequently, wafers are bonded to each other by using a metal-to-metal thermocompression process or by using polymeric or dielectric layers. We varied the thickness of SiO_2 bonding layer from 1µm to 100 µm and calculated the maximum temperature within the chip. Figure 6.4 shows the maximum temperature as a function of bonding layer thickness. We find the thickness of the bonding layer has a profound effect on the temperature rise. The incorporation of graphene heat spreaders reduces maximum temperature but follows similar temperature profile with different bonding layer thickness. Increasing thickness of the bonding layer leads to an overall increase in the maximum temperature in the chip. This is reasonable as the thermal resistance increases with the increase of bonding layer thickness.

6.2 STUDY OF DIFFERENT ARCHITECTURES

We also explore three different architectures of 3-D integration as shown in Figure 6.1, Figure 6.5 and Figure 6.7. In each design, the chip consists of two stratums with one device layer and two interconnect layers per stratum. But the location and design of inter-layer-interconnect via is different. It connects the two stratums in the middle in Design-1 where in Design-2, it connects at the side. In Design-3, two vertical side vias are connected to a common metal layer at the top of the chip. Figure 6.2, Figure 6.6 and Figure 6.8 present the calculated temperature profiles without and with graphene heat spreaders within the 3-D chip of Design-1, Design-2 and Design-3, correspondingly. The power density of each active channel and interconnect were 0.10 W/mm and 0.15 W/mm,

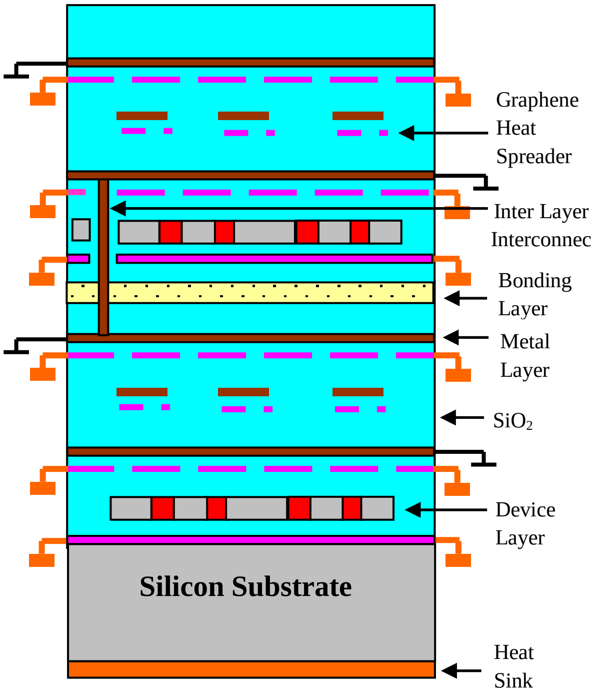
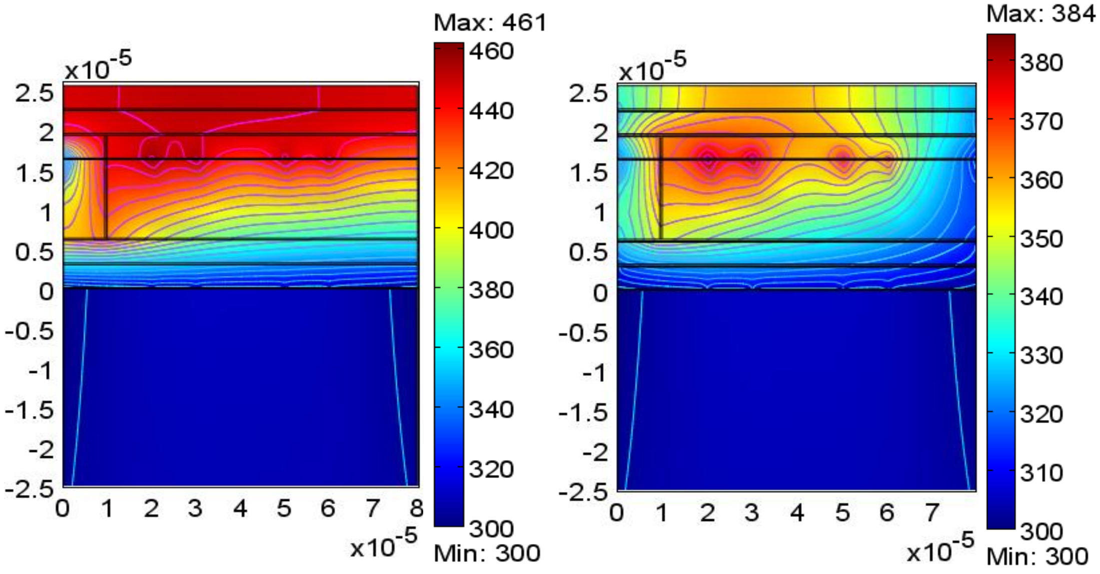


Figure 6.5: Schematic cross-section of the 3-D chip with graphene heat spreaders: Design-2.



(a) (b)

Figure 6.6: Temperature distribution across the 3-D chip (Design-2) with two stratums consisting of one device layer and two interconnect layers per stratum (a) without and (b) with graphene heat spreaders attached to the side heat sinks.

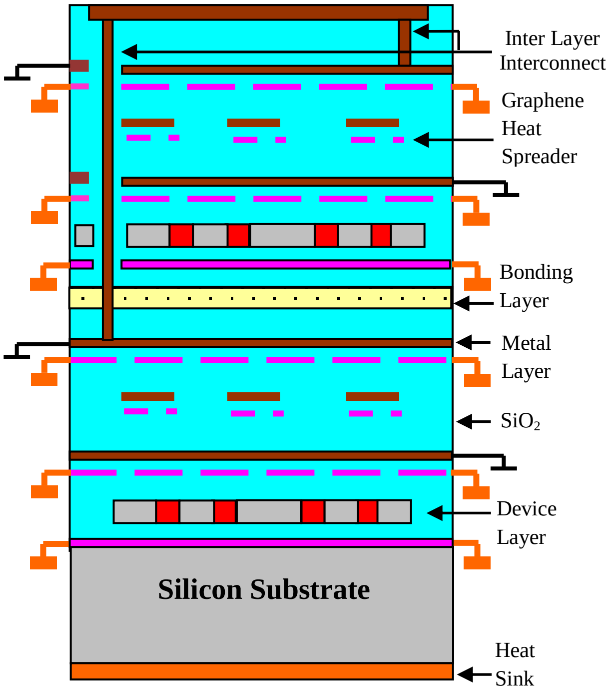
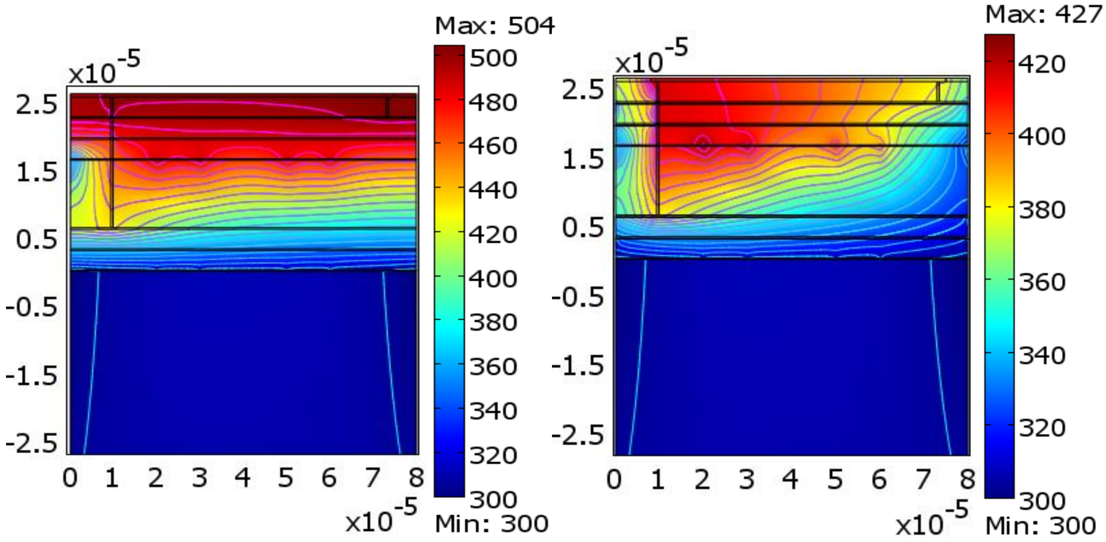


Figure 6.7: Schematic cross-section of the 3-D chip with graphene heat spreaders: Design-3.



(a) (b)

Figure 6.8: Temperature distribution across the 3-D chip (Design-3) with two stratums consisting of one device layer and two interconnect layers per stratum (a) without and (b) with graphene heat spreaders attached to the side heat sinks.

respectively. It is seen that the drop in temperature with graphene heat spreaders is various in different design paradigms. The simulation results suggest that the optimum design and proper placement of the interconnects and vertical vias can help to lower the temperature rise in the chip.

Chapter 7

Conclusions

Thermal management considerations in nanometer-size devices became an integral part of the design. The increasing power density is one of the critical issues, which resulted from downscaling of the device feature size and increasing integration density. One possible approach to alleviate the thermal problem is finding materials with extremely high thermal conductivity and integrating them with Si complementary metal-oxide semiconductor (CMOS) technology. Graphene is an excellent conductor of heat with the room-temperature intrinsic thermal conductivity comparable to or exceeding those of carbon nanotubes.

In this dissertation, we developed physical models and simulated heat propagation in graphene layers of different shape. The finite-element analysis method was used as a tool for solving the steady-state and continuous problems. The data extraction in the first measurements of the thermal conductivity of single-layer graphene was performed under the assumption of the plane wave heat front propagating in rectangular flake. The first goal of the computer simulation was verifying the validity of such an assumption. The second goal of this study was the understanding of the effects of the flake geometry and laser spot on the heat propagation in graphene. The obtained results of the simulations gave insights for planning of the future thermal experiments with graphene. The developed numerical procedure was used for the data extraction in the experiments with few-layer graphene.

The multilayer graphene is more robust, mechanically stable and technologically more feasible for practical applications. These considerations motivated our study of heat propagation in few-layer graphene. We analyzed graphene flakes with 2 to 4 atomic planes. Due to the difficulty of mechanical exfoliation of flakes with exactly the same geometry, we solved the heat diffusion equation numerically for each shape of the sample. The data analysis was accomplished through an original iteration procedure with an assumption of the Gaussian-distributed laser intensity on the surface of graphene flake. The obtained values of the intrinsic thermal conductivity of the few-layer graphene were in the range between the maximum for the single-layer graphene and the value for the basal plane of the high-quality graphite. The intrinsic thermal conductivity decreases as the number of atomic planes increases and approaches the in-plane bulk graphite limit. The obtained results are important for the proposed applications of few-layer graphene in the lateral heat spreaders.

In order to evaluate the feasibility of the hot spot removal with graphene or FLG, we simulated heat propagation in a prototype SOI-based chip with and without graphene heat spreaders. Numerical solutions of the heat propagation equations were obtained using the finite element method. The analysis was focused on the prototype SOI circuits with the metal – oxide -semiconductor field-effect transistors. It was found that the incorporation of graphene or few-layer graphene (FLG) layers when sandwiched between buried oxide layer and the substrate can lead to substantial reduction of the temperature of hot spots. The effective cooling can only be achieved if graphene layers are connected to the side heat sinks. The maximum temperature in the transistor channels was studied as function of thermal conductivity of graphene, thickness of the substrate and thickness of FLG.

As the next step, we also simulated the heat propagation in SOI chip with active devices, which also included the effects of Joule heating within the interconnect network. This results in higher temperature rise within the chip. Our developed models include structures where SLG or FLG (i) act just as heat spreaders incorporated within interconnect hierarchy; or (ii) perform a dual function of interconnects and, simultaneously, lateral heat spreaders. We also investigated heat conduction in 3-D chips with graphene lateral heat spreaders. The developed models and simulation tools allowed us to address the architecture and optimum design issues. Our numerical results show that incorporation of graphene layers with proper heat sinks and architecture lower the temperature of localized hot spots. The efficiency of the hot spot removal with graphene depends on the specifics of the device structure and geometry. Numerical experiments suggest that few-layer graphene heat spreaders can be more technologically feasible than single-layer graphene. The obtained results may lead to a new type of the high-heat-flux thermal management. Due to the increasing dissipation power density, switching speed and thermal resistance of the multi-layer structures, the device-level thermal management becomes important not only for conventional electronics but also for magnetic memory logic elements with alternative state variables three-dimensional and reconfigurable architectures and optoelectronic devices.

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