UNIVERSITY OF CALIFORNIA SAN DIEGO

Low Power Biomedical Signal Acquisition using Frequency Modulation and Frequency Domain Multiplexing

A dissertation submitted in partial satisfaction of the requirements for the degree
Doctor of Philosophy

in

Electrical Engineering (Electronic Circuits and Systems)

by

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2019

The dissertation of Julian Alexander Warchall is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

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University of California San Diego

2019

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ACKNOWLEDGEMENTS

Since my arrival at UC San Diego, Professor Mercier has had an enormous positive effect on my development as an academic and professional. I'd like to thank him first for his patience, wisdom, and guidance during my degree program because without him this work would never have been done.

The members of my thesis committee – Professors Cauwenberghs, Coleman, Hall, Kahng, and Doctor Garudadri – provided guidance throughout the course of my research and I thank them profusely for their time and effort on my behalf.

I am grateful to all my colleagues at UC San Diego for the stimulating technical duscussions we have had over the years, including but not limited to (and in no particular order): Loai Salem, Hui Wang, Dhon Lee, Cooper Levy, Jiwoong Park, Somayeh Imani, Sally Amin, Po-Han Wang, Bao Lam, Xiaoyang Wang, Abdullah Abdulslam, Jason Huang, Ali Nikoofard, Hossein Rahmanian, Nader Fathy, Hongsen Yang, Dukju Ahn, Nidhi Jayapalan, Giri Nayak, Shiva Kaleru, Qing Qin, Aishwarya Balakrishnan, Yuan Cao, and Omar Mirza.

My friends and roommates have been a big part of my life throughout the degree process and instrumental in the preservation of my mental health, especially Doctor Ali Ebrahim, Doctor Kelvin Fang, Doctor Robert Kaspar, Master Steven Okai, Master John Louie, A.B.D. Paolo Gabriel, Bachelor Brandon Robinson, and Comrade Aleksandr Arzamasov.

I am forever indebted to my mother and father, Nora Kronenthal and Doctor

Henry A. Warchall Jr., who instilled in me at a young age an interest in building things, testing theories, and science and technology in general. Countless times in my life they have helped me to understand the value of thorough research, clear prose, and a job well done; this has had a profound effect on my life, both academic and otherwise. My sister, Iris Warchall, DPT, is always full of aid and advice, especially recently when I have injured myself exercising. My fiancée, Yukari Otsuka, has been a source of inspiration and support from the moment we met and I am truly lucky to have her in my life.

Thank you all.

Julian Alexander Warchall

June 10th, 2019

Material in this dissertation is based on the following published papers.

Chapter 2 is based on and mostly a reprint of the following publication:

- J. Warchall, S. Kaleru, N. Jayapalan, B. Nayak, H. Garudadri, and P.P. Mercier, "A 678-uW Frequency-Modulation-Based ADC With 104-dB Dynamic Range in 44-kHz Bandwidth," *IEEE Transactions on Circuits and Systems II: Express Briefs*, 65 (10), 2018, 1370-1374.

Chapter 3 expands upon the following publication:

- J. Warchall, P. Theilmann, Y. Ouyang, H. Garudadri, P.P. Mercier, "22.2 A Rugged Wearable Modular ExG Platform Employing a Distributed Scalable Multi-Channel FM-ADC Achieving 101dB Input Dynamic Range and Motion-Artifact Resilience," *2019 IEEE International Solid- State Circuits Conference - (ISSCC)*, San Francisco, CA, 2019, pp. 362-363.

The dissertation author is the primary investigator and author of the work in these papers.

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ABSTRACT OF THE DISSERTATION

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Patrick P. Mercier, Chair

A scheme for the sampling and quantization of voltages over time in an integrated circuit chip is presented based on first frequency modulating the signal of interest and then sampling and quantizing its frequency modulated representation. When a single input signal is considered and demodulation to recover the original signal is performed on the same chip as modulation, the resulting structure is an FM-ADC as discussed in Chapter 2. The recording of multiple input signals using multiple frequency modulating chips and frequency domain multiplexing combined with demodulation off-chip is referred to as a distributed multi-channel FM-ADC with demodulation

offloading, and is discussed in Chapter 3 as applied to biopotential signal acquisition as it offers unique advantages in that application space. Chapter 4 deals with theoretical optimization of the FM-ADC in both its single-channel and multi-channel forms.

Chapter 1

Foreword

The contents of this thesis deal with a type of voltage-controlled oscillator (VCO) based analog to digital converter (ADC) which we will come to call the FM-ADC. The FM-ADC is different from traditional VCO-based ADCs as it uses a sinusoidal-output VCO and multi-bit quantization of its output as opposed to the traditional square-wave-output VCO with single bit output quantization. The use of a sinusoidal-output VCO affords the FM-ADC two advantages: First, it can achieve higher input dynamic range than traditional VCO ADCs for the same levels of power consumption, as will be shown in Chapter 2. Second, it can be used in a scheme with multiple input signals all recorded simultaneously, a scheme we call the distributed multi-channel FM-ADC. It turns out that this multiple-input scheme affords some unique advantages in the realm of biopotential signal acquisition, or sensing of the human body's electrical activity at the skin, and we will exposit both the technique and its application-related advantages in Chapter 3. In Chapter 4 we will briefly touch on ways to optimize the design choices made when implementing an FM-ADC system, regardless of whether it has a single channel of input signal or multiple channels.

Chapter 2

A 678 Microwatt Frequency-Modulation-Based ADC With 104 Decibel Dynamic Range in 44 Kilohertz Bandwidth

2.1 Abstract

This work presents a frequency-modulation-based analog-to-digital converter (FM-ADC) that takes advantage of the coding gain resulting from bandwidth expansion in the analog domain of FM systems to achieve high dynamic range and incorporates a highly digital demodulation approach for power efficiency. The novel architecture employs a sinusoidal output voltage-controlled oscillator (VCO), a relatively low-resolution successive approximation register (SAR) ADC to sample signals in the FM domain, and then a digital signal processing (DSP) FM demodulator to recover high-resolution samples of the VCO's original analog input. The proposed ADC is im-

plemented in 0.5mm2 of 65nm CMOS; it achieves 104dB DR, 99dB SNR, and 71dB SNDR in a 44kHz bandwidth while dissipating 678μW of power. The architecture of the FM-ADC leverages analog domain processing for system performance and digital domain processing for lower power. This novel approach presents a viable alternative to delta-sigma converters for high dynamic range conversion in advanced process nodes.

2.2 Introduction

Smartphones and emerging Internet of Things (IoT) devices feature multitudes of sensors that capture information from a variety of analog sources such as sound, light, motion, pressure, magnetic fields, humidity, and more. These sensors require analog to digital conversion over wide dynamic ranges and must meet the stringent power demands of portable and wearable devices. For size and cost purposes, this is preferably achieved in the same CMOS technology as the primary system-on-chip (SoC). Delta-sigma ($\Delta\Sigma$) converters are popular for these applications because of their high dynamic range (DR) due to oversampling and noise shaping, but the precision analog operational amplifiers required for their difference amplifiers do not scale well to smaller CMOS processes.

VCO-based ADCs have been proposed as an alternative to traditional $\Delta\Sigma$ converters, as they inherit first-order noise-shaping properties while being inherently better suited to process scaling [1]; however, to date, low achievable DR makes these VCO ADC architectures better suited for communication applications than for high-DR sen-

sor applications. The low DR of state-of-the-art VCO ADCs [2] can be traced to the use of square-wave VCOs, as square-wave VCOs limit the amount of information represented, as discussed further in Section 2.3.2.

This work proposes a novel ADC architecture in which a sine wave VCO is used for frequency modulation, followed by multi-bit carrier quantization and digital FM demodulation. A higher DR than previously reported VCO ADCs and an SNR figure-of-merit (FOM) comparable with $\Delta\Sigma$ architectures is thus demonstrated in a more scaling-compatible and synthesis-friendly architecture.

2.3 FM-ADC System Design

2.3.1 Motivation for Analog Domain FM Processing

The SNR of an FM system in dB can be expressed as

$$SNR_{FM} = 10log_{10}(3D^2(D+1)) + CNR \qquad (1)$$

where CNR is the Carrier to Noise Ratio in dB [3]. Here, D is the bandwidth expansion ratio, Δf / W, where Δf is the maximum frequency deviation of the FM carrier and W is the message signal's bandwidth. The first term in this expression is known in FM broadcasting literature as FM coding gain.

Figure 2.1 depicts the proposed FM-ADC. The input signal is frequency modulated, resulting in bandwidth expansion. The FM signal is then sampled and quantized with a conventional medium-resolution ADC. The discretized signal is demodulated to recover the input signal with a high DR, due to the inherent coding gain of frequency modulation.

For a 60dB SNR internal medium-resolution ADC with 2MHz sampling frequency, the CNR is 60 dB, with a bandwidth expansion D = 22.7 for audio band signals. This is a 45.6 dB FM coding gain and a theoretical 105.6 dB of dynamic range from Equation 1, comparable to a 17.2-bit effective-number-of-bits (ENOB) ADC.

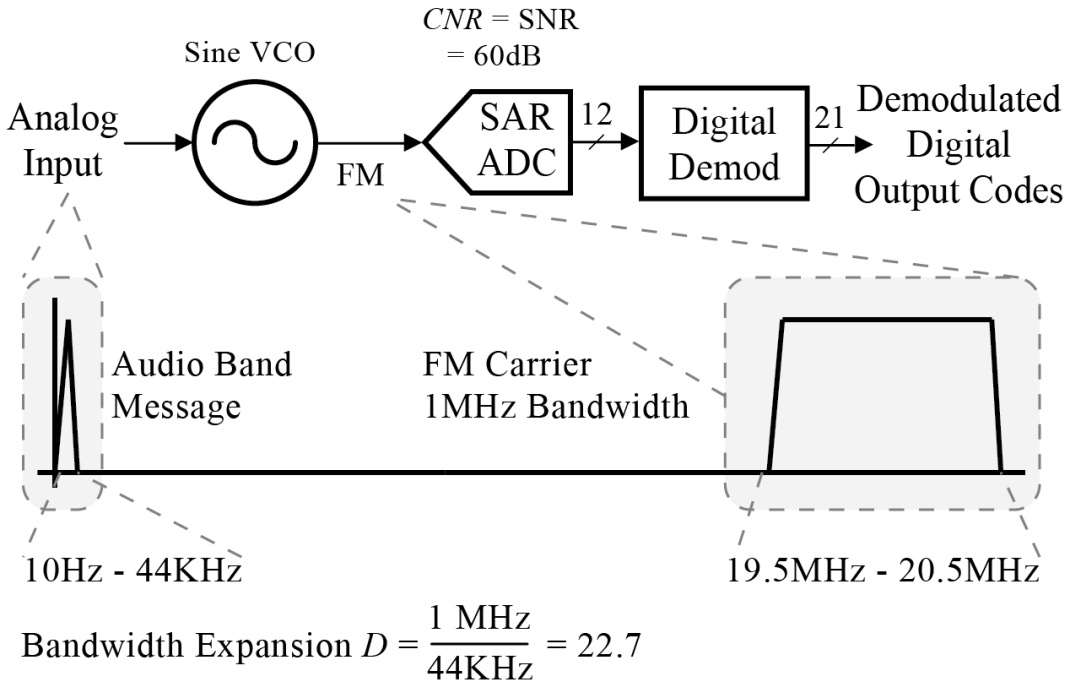

Figure 2.1: Block diagram of proposed FM-ADC.

2.3.2 Differences from Prior Work

Prior VCO ADCs have opted for square-wave VCOs, typically based on digital ring oscillators, thanks to their low-power, synthesizability, and process scaling compatibility. However, a square wave can only encode instantaneous frequency information at its zero crossings this means that the resolution in time with which one can determine the frequency of a square wave is limited by the wave's frequency itself, as illustrated in Figure 2.2. In the case of a sine wave, instantaneous frequency, in principle, can be determined from inter-period samples to arbitrarily high resolution.

Another way to think of this is that a sine wave's observed frequency is continuous, while a square wave's known frequency is discrete and unchanging until the next

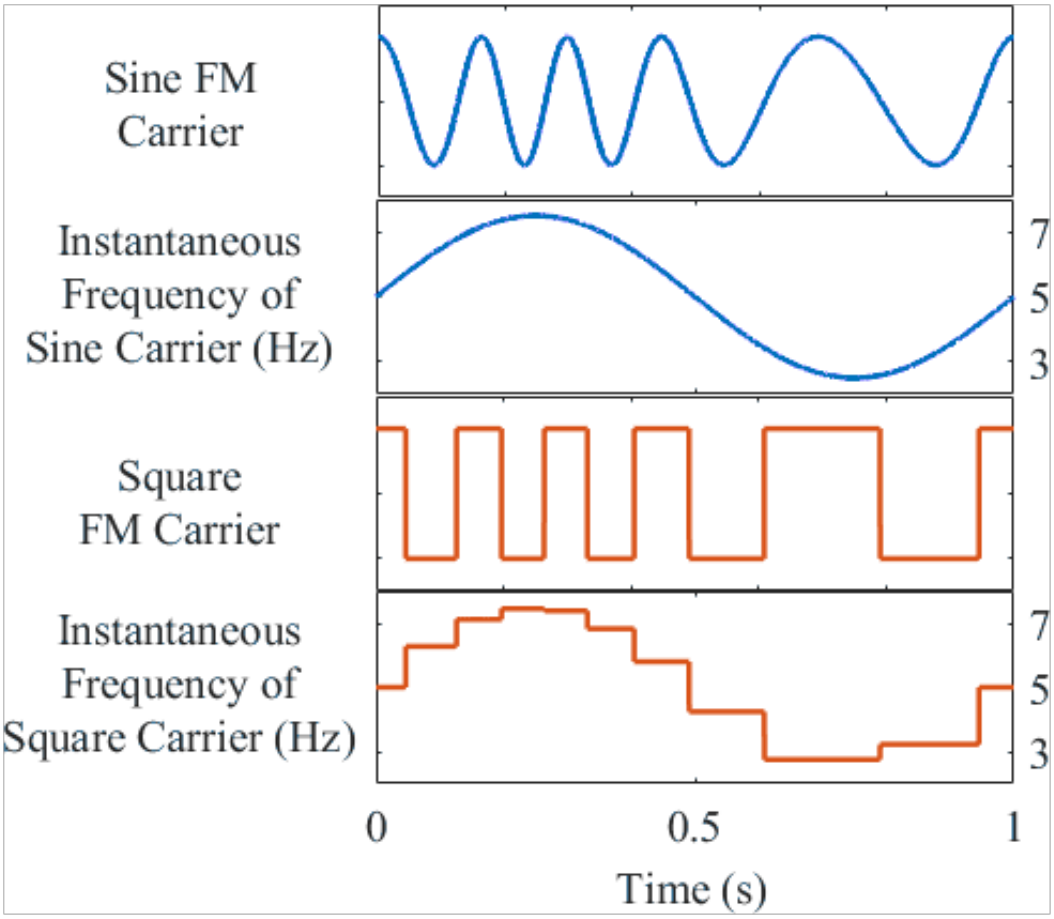

Figure 2.2: Instantaneous known frequencies of FM carriers.

zero crossing. At the same frequency, a sine wave carrier can encode more message information than its square wave counterpart, potentially saving absolute VCO power since, in general, the power of a VCO is directly proportional to the VCO oscillation frequency.

Recently-reported VCO based ADCs have circumvented this limitation by tapping a ring oscillator in multiple locations to acquire sub-period frequency information using the multiple phases of output square wave [4]. In this case, more stages must be added to increase accuracy at the same VCO frequency, but additional stages may con-

sume more power or introduce jitter or phase noise, both of which can be detrimental to the overall converter's FOM. Consequently, VCO-based ADCs achieve an SNR FOM of about 10dB lower than comparable $\Delta\Sigma$ ADCs, as seen later in Table 2.2.

2.3.3 System Design Considerations

The chip described in this paper targets a high-fidelity audio bandwidth (44kHz) as a sample application of an FM-ADC, with a bandwidth expansion of 22.7 (to 1MHz) to achieve high dynamic range. The key system-level questions to address are as follows: What type of VCO should be used, and at what frequency should it operate?

To practically achieve the targeted system dynamic range, the VCO must have a low enough phase noise [5]. While RC-based VCOs, such as the Wien bridge topology, can produce sinusoidal outputs while consuming low power, the phase noise and frequency drift of such oscillators are too high to achieve $>$100dB DR. LC VCOs, on the other hand, are known to have excellent phase noise, particularly if a high-Q resonant tank can be used, and thus an LC VCO is chosen for this work.

The choice of the VCO's center frequency in this work is motivated by two competing factors: keeping the frequency low reduces power expenditure in the oscillator, and yet, higher frequencies allow for increased linearity in the VCO's tuning curve because its varactor diodes can be swept over a smaller, more linear, capacitance range for the same FM bandwidth. High oscillation frequencies also allow for a smaller VCO footprint since the LC tank scales down with higher frequency. Simulations show that

by going from a 2MHz oscillator to a 20MHz oscillator, spur-free DR can be increased by 20dB for a roughly 10x increase in VCO power. As VCO frequencies continue to increase past 20MHz, however, there are diminishing returns in added linearity with the employed VCO and 20MHz was settled on to balance linearity and power expenditure and provide a competitive FOM.

If the SAR ADC were to quantize the FM carrier in the most obvious way by sampling at the Nyquist frequency of the carrier (41MHz in this case) the power consumption of the SAR ADC would be quite large and would thus suggest selection of a smaller carrier frequency to reduce overall ADC power. Fortunately, this trade-off can be decoupled, as signal power is only located in a small portion of this overall bandwidth 1MHz in this design. Like in FM (and most other RF) systems, the signal of interest can be mixed-down to baseband prior to digitization to reduce the ADC requirements.

Rather than build an explicit mixer, in this work bandpass sampling, which is a careful form of subsampling, is utilized, as there are no interfering signals between the VCO and on-chip SAR ADC, and thus down-conversion can be accomplished with zero power overhead [6]. Specifically, the SAR ADC samples at the Nyquist rate of the bandwidth of the FM-modulated signal (2MHz), such that the 1MHz spectrum of interest is represented in aliased form near baseband, ready for demodulation, at an ADC power $\sim$20x lower than if sampled at the Nyquist frequency of the carrier.

Interestingly, this technique would be difficult, if not impossible, to employ with a square-wave VCO, as aliases of the square wave's very high amplitude harmonic content would fold onto the primary FM band in the subsampling operation. In the sine-

wave VCO case, the harmonic content of the carrier is made to be lower than the level of quantization noise in the SAR.

2.4 FM-ADC Circuit Design

2.4.1 VCO

To achieve low phase noise and power consumption, a current reuse LC VCO, shown in Figure 2.3, is used in this design [7]. To further increase phase noise performance of the oscillator, the switching active core technique is utilized, in which a larger width MN2 and MP2 are used to start up the oscillator but are disconnected during normal operation [8]. The tank inductance is realized by a 3.3μH off-chip 0603 inductor. The tuning elements employed are on-chip silicon varactor diodes, which introduce a nonlinear voltage-to-frequency response in the VCO. This nonlinear relationship is primarily responsible for the nonlinearity of the FM-ADC's output. The allowable bias range of the varactor diodes also limits the input full scale range of the FM-ADC to the 0.8V - 1.2V range. The VCO as implemented consumes 113μW from a 1.2V supply.

2.4.2 SAR ADC

The internal SAR ADC design is based on a 12-bit metal-oxide-metal (MOM) capacitor conventional binary weighted DAC and is illustrated in Figure 2.4. A 12-bit design is chosen to target at least 60dB SNR and achieve the CNR target elaborated

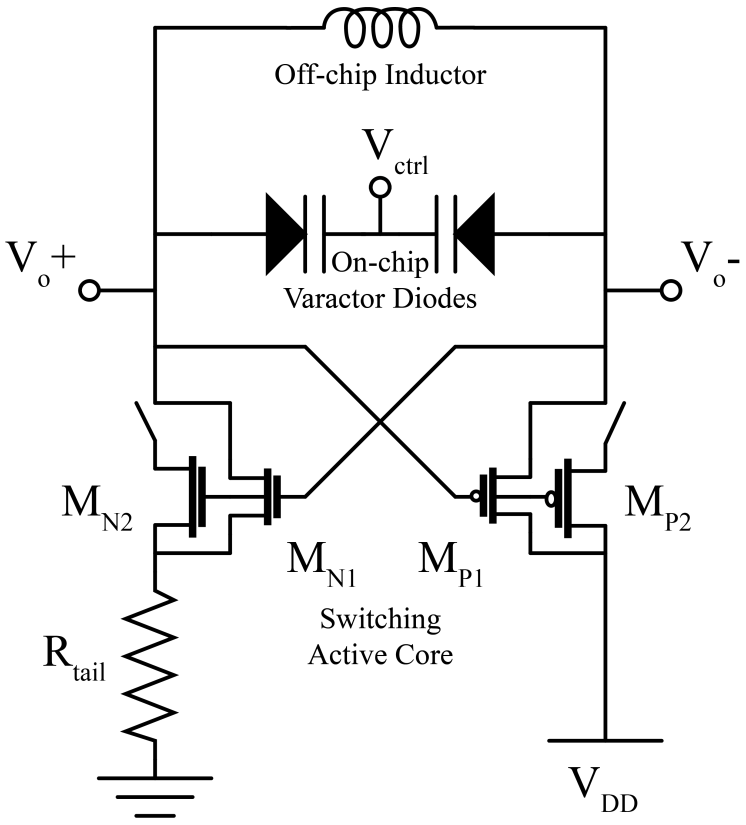

Figure 2.3: Current reuse voltage-controlled oscillator.

previously.

A unit capacitance of 3fF is chosen for the capacitive DAC. Removal of the dummy unit capacitor on the LSB side of the capacitor bank allows the use of a unit capacitor as the bridge capacitance between the least-significant-bit (LSB) and most-significant-bit (MSB) sides of the capacitor banks. For input sampling, a bootstrapped switch configuration is used to reduce the input-dependent on-resistance of the switch which leads to distortion [9].

The comparator used in the SAR consists of a pre-amplifier stage and a latching stage. The pre-amplifier is isolated in latch mode to reduce kickback from the latching

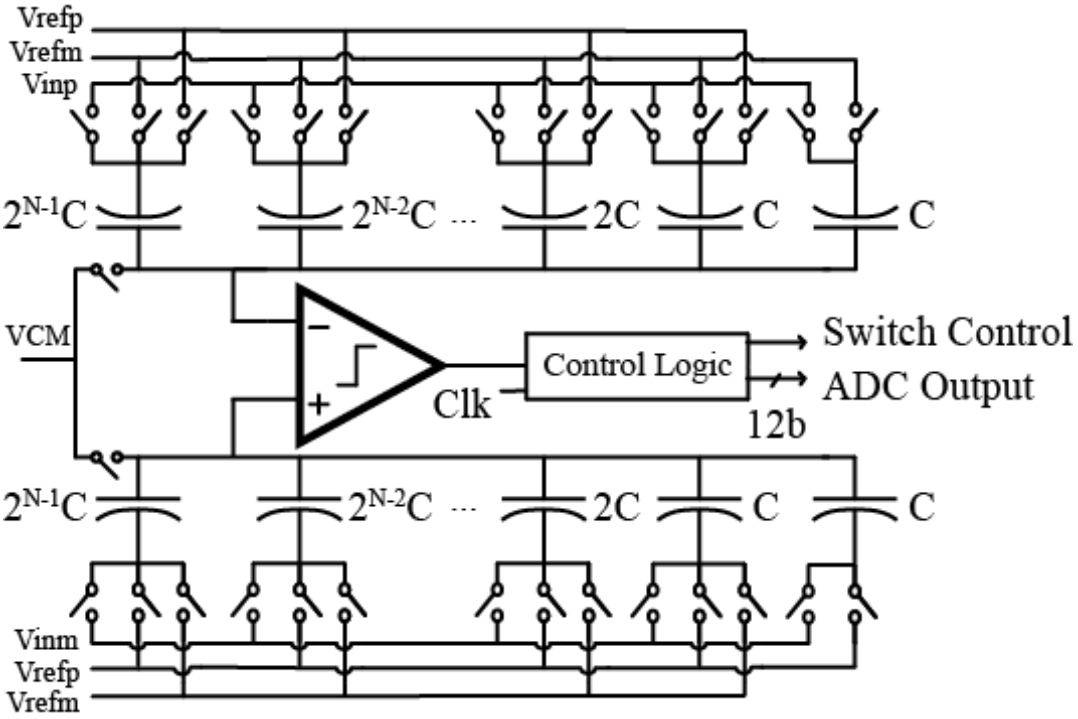

Figure 2.4: FM-ADC internal SAR ADC diagram.

stage and utilizes positive feedback to increase gain. The pre-amplifier's low output common mode resistance helps to reduce kickback from charge injection of the switches to the input nodes. Dummy transistors are used in both stages to reduce offset and charge injection. The internal SAR consumes 148μW from a 1.2V supply and takes 16 cycles per conversion and is thus clocked 16x faster than the demodulation DSP block.

2.4.3 Digital Demodulation

The block diagram in Figure 2.5 illustrates the top-level logic blocks in the on-chip FM demodulation DSP. The 12-bit sampled FM carrier is first put through a Hilbert transform to generate 12-bit in-phase (I) and quadrature (Q) versions of the signal needed for demodulation. Then, I and Q are mixed to baseband by multiplying

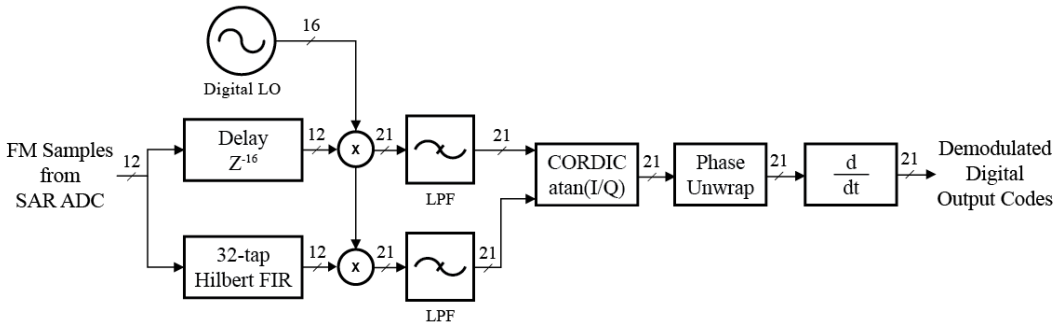

Figure 2.5: FM-ADC demodulation digital signal processing block diagram.

sample-by-sample with 16-bit tabulated sine wave samples at the carrier frequency and low pass filtering. The results of this mixing are a 21-bit baseband I and Q which are fed into a 16-iteration coordinate rotation digital computation (CORDIC) arctangent. 16 iterations are chosen so that the CORDIC is clocked from the same 16x clock source as the internal SAR.

After phase unwrapping to remove discontinuities in the resultant phase samples and a difference operation to recover frequency from phase, the result of the entire DSP chain is a 21-bit demodulated signal a digital representation of the original input to the VCO.

This DSP is implemented in a straightforward fashion without pipelining so that there is minimal latency in the ADC. The Hilbert and low-pass filters are implemented as finite impulse response (FIR) filters to ensure accurate representation of the carrier's phase. In total, the digital demodulator consists of approximately 200,000 gates and consumes 417μW from a 0.66V supply.

2.5 Measurement Results

2.5.1 Testing Apparatus and Methods

The chip is fabricated in 0.5mm^2 of core area in a low-power 65nm CMOS process. Test signals are applied to the chip using a Stanford Research Systems DS360 Low Distortion Function Generator. The chip's digital outputs are recorded using an Opal Kelly XEM6310 FPGA Integration Module and then saved to MATLAB for post-processing and analysis.

2.5.2 nonlinearity Correction

To combat the nonlinearity discussed in Section 2.4.1, some nonlinearity correction (NLC) is required in practice. Note that the NLC specifications depend on the specific varactors chosen for VCO tuning. To demonstrate the FM-ADC's practically achievable DR, NLC is implemented in MATLAB post-processing and its power consumption simulated. Using a ramp waveform stimulus at the FM-ADC's input, a 1-to-1 mapping is determined based on a fifth-order polynomial fit that calibrates the output codes to form a linear ramp. This time-independent amplitude mapping is then applied to the ADC's output in all experiments as offline calibration. Vector-input post-placement post-routing power simulations from the Cadence Innovus suite of tools indicate that with this NLC implemented on-chip, digital power would increase by approximately 7 percent and the digital floorplan utilization would increase from 88 percent to

91 percent so no additional chip area would be required. To further increase the ADC's linearity, more linear tuning varactors would be required in the VCO, or a new more linear tuning paradigm could be considered.

2.5.3 Test Results

The measured power spectral density of the FM-ADC's output for a 100Hz sinusoidal full scale (0.4Vpp) input is shown in Figure 2.6a, achieving a maximum SNR of 99dB. Noise shaping due to the integrative nature of the VCO is exhibited in the output codes as the noise floor rises on the right-hand side of Figure 2.6a. Figure 2.6b illustrates the peak in-band spur-free dynamic range (SFDR) to be 81dB, measured by attenuating the input amplitude until spurious tones are hidden below the noise floor (0.04 Vpp).

Figure 2.6c illustrates measured SNDR and SNR of the output for varying input amplitudes. As the input amplitude goes above 0.04V, the locally linear but globally nonlinear V-to-C nature of the VCO varactor diodes limits the system SNDR and causes it to fall off with increasing amplitude of input signal. Figure 2.6d demonstrates that SNR and SNDR are virtually unchanged with test input frequency, except for the SNDR of the high-amplitude input, which increases at high frequencies as the signal distortion falls out of band.

Interestingly, these results are achieved despite poorer than expected performance from the internal SAR ADC due to higher than expected comparator noise and DAC nonlinearity. Specifically, the internal SAR achieves an SNR of 60.5dB (ENOB =

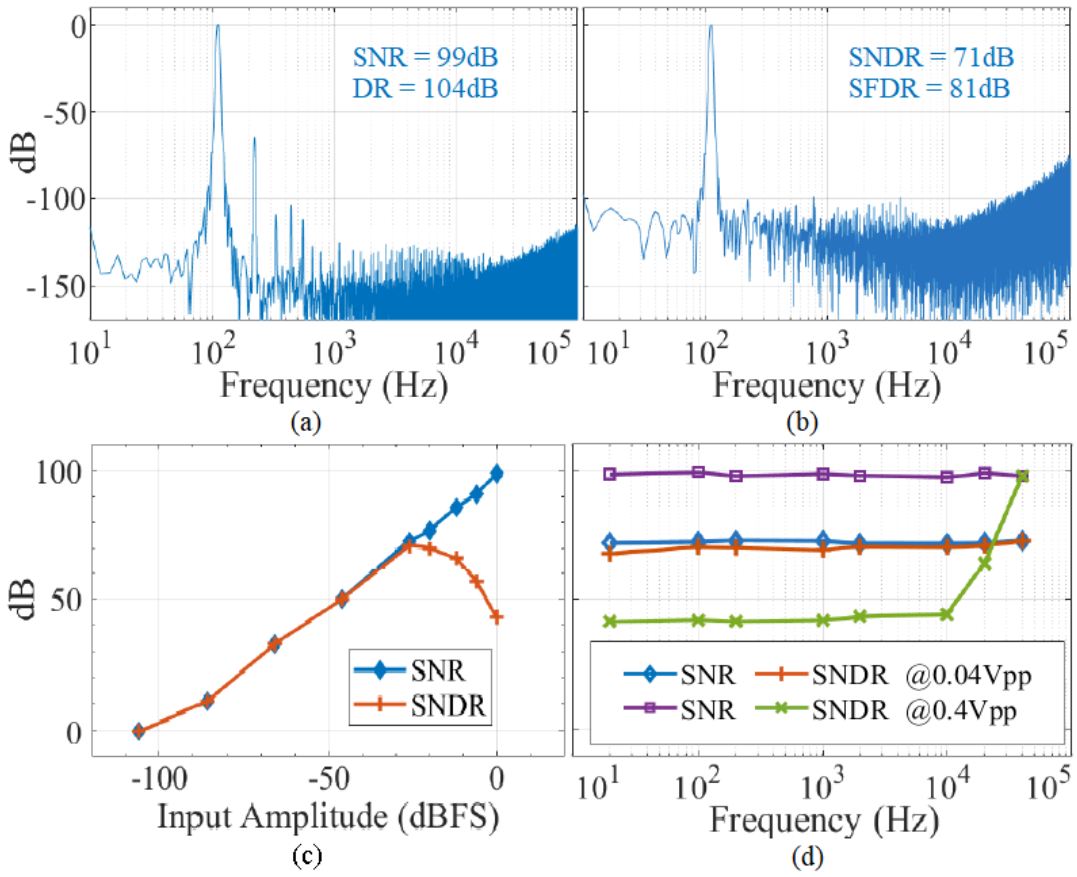

Figure 2.6: Collected measurement results from FM-ADC.

9.76-bits when ignoring distortion) and SNDR of 33.5dB (ENOB = 5.27-bits including distortion) over its 1MHz bandwidth. This prompted the authors to investigate the overall effects of quantizer nonlinearity on the FM-ADC signal chain's overall performance.

2.5.4 Supplemental Simulation Results

MATLAB simulations of the whole FM-ADC signal chain with a variably nonlinear 12-bit internal SAR ADC yield the results illustrated in Figure 2.7. In this simulation, intrinsic nonlinearity is removed from the VCO's tuning profile so that purely the effects of the FM carrier quantizer can be studied. The SAR is modeled as an ideal

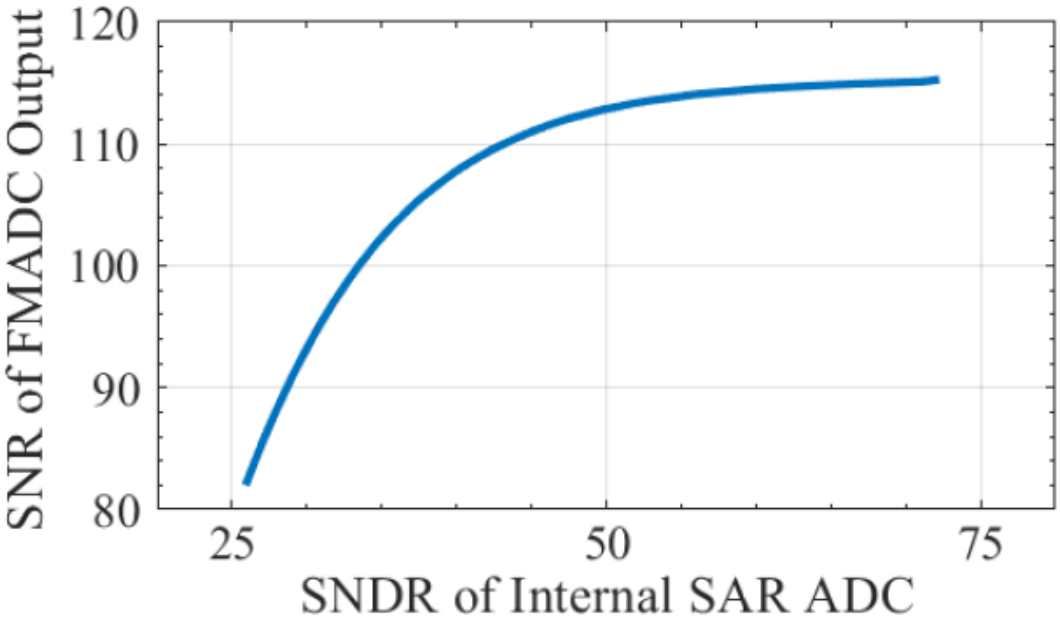

Figure 2.7: Simulated effect of SAR SNDR on FM-ADC output SNDR.

12-bit quantizer and sampler with a variable amplitude arctangent profile, which is a strategy often used to model memoryless nonlinearities [10].

It is observed that the FM-ADC signal chain tolerates relatively high amounts of nonlinearity in the ADC used to quantize the FM carrier before a detrimental effect is seen at the overall ADC's output. This result also suggests that, had the SAR in our chip shown better SNDR, measured SNR/DR in our tests may have improved by roughly 10dB. The achievement of high system SNR and SNDR despite poorer than expected quantizer performance cements the advantage of the proposed FM process and shows that the FM-ADC technique can indeed utilize a low-power rough quantizer and still achieve high resolution analog-to-digital conversion.

Table 2.1 summarizes simulations investigating the effect on process, voltage, and temperature variation on the performance of the FM-ADC. We see that across vari-

Table 2.1: Process, voltage, and temperature simulation results for FM-ADC.

PVT Simulation Type	**TT** 20 C 1.2V	**FF** 20 C 1.2V	**SS** 20 C 1.2V	**FS** 20 C 1.2V	**SF** 20C 1.2V	TT 20 C **1.1V**	TT 20 C **1.3V**	TT **0 C** 1.2V	TT **40 C** 1.2V
SNR [dB]	106	107	100	104	103	104	108	109	101
SNDR [dB]	85	86	82	84	85	83	86	87	79
Power [mW]	0.573	0.616	0.539	0.575	0.562	0.511	0.642	0.505	0.625

ation types the proposed architecture maintains SNR and SNDR performance within 6 dB of the typical case.

2.5.5 Comparison with Prior Work

The FM-ADC consumes 678μW of total power including clock power (estimated from post-route simulations to be 707μW with on-chip digital nonlinearity correction) with a SAR/CORDIC clock rate of 32MHz and demodulation DSP clock rate of 2MHz. Of this power, 417μW is consumed in the digital demodulator, 148μW in the SAR, and 113μW in the VCO. A comparison of the FM-ADC with other state-of-the-art VCO-based (right-hand side) and $\Delta\Sigma$-based (left-hand side) ADCs is given in Table 2.2. It is seen that the achievable DR, SNR, and SNR FOM of the FM-ADC architecture are comparable with that of $\Delta\Sigma$ ADCs and greater than that of VCO ADCs.

The FM-ADC has a reliance on an off-chip inductor for the sinusoidal VCO, which is not included in the tabulated active area and would increase real-world implementation cost. We believe, however, that the architecture has useful application to save power in the multiplexed acquisition of multiple signal channels (see our related

Table 2.2: Comparison of FM-ADC with prior work.

Design	Karmakar, ISSCC 2018	Gonen, JSSC 2017	Park, TCAS-II 2017	This Work	Zhu, TCAS-II 2015	Babaie-Fishani, JSSC 2017	Dey, CICC 2017
Process	160nm	160nm	65nm	**65nm**	40nm	65nm	65nm
Active area [mm^2]	0.25	0.16	0.38	**0.5**	0.16	0.01	0.35
ADC Type	$\Delta\sum$/Zoom	$\Delta\sum$/Zoom	$\Delta\sum$	**FM**	VCO	VCO	VCO
DR [dB]	120.3	109	70.1	**104**	78	71	76.1
SNR [dB]	119.1	106	65.3	**99**	68.7	66.2	76.1
SNDR [dB]	118.1	103	60.8	**71**	66.8	62.5	73.5
Bandwidth [KHz]	1	20	7.5	**44**	40000	10000	50000
Output Sample Frequency [MHz]	2	11.29	0.4	**2**	1600	1600	1500
Power Consumption [mW]	0.280	1.12	0.0127	0.678 **0.707***	5.48	3.7	51.8
FOM 1 = SNR + 10log(BW/P)	184.6	178.5	153	177 **176.9***	167.3	161	166
FOM 2 = SNDR + 10log(BW/P)	183.6	175.5	148.5	149 **148.9***	165.4	156.8	163

* Includes digital nonlinearity correction power addition from post-route simulations

work [5]). Future work will focus on demonstrating such multi-channel signal acquisition, improving the VCO's tuning linearity to improve overall SNDR, and moving to a smaller process node. Importantly, since 61 percent of the ADC power is consumed by the digital demodulator, the FOMs of the FM-ADC will improve dramatically with process scaling. Using a smaller process node would also allow the active area to be reduced significantly, as 77 percent of the chip area consists of digital circuitry. A die photo is shown in Figure 2.8.

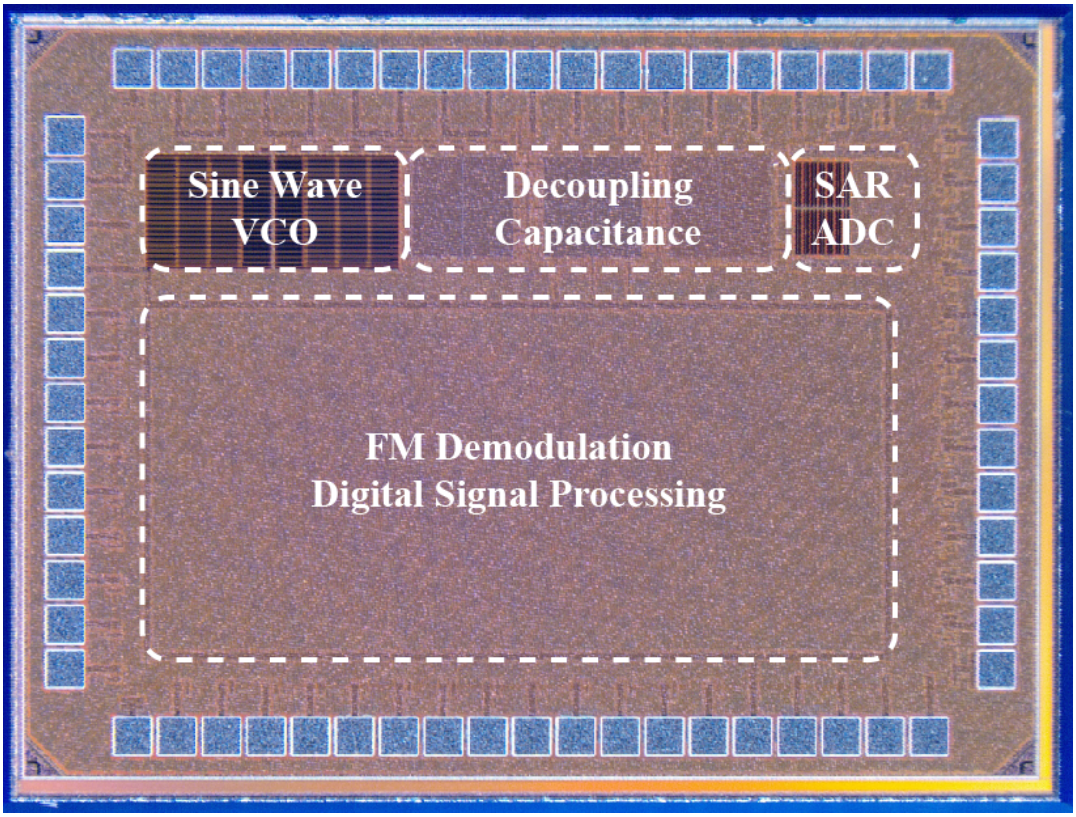

Figure 2.8: FM-ADC die photograph. Total die size 1.5mm^2.

Chapter 2 is based on and mostly a reprint of the following publication: J. Warchall, S. Kaleru, N. Jayapalan, B. Nayak, H. Garudadri, and P.P. Mercier, "A 678-uW Frequency-Modulation-Based ADC With 104-dB Dynamic Range in 44-kHz Bandwidth," *IEEE Transactions on Circuits and Systems II: Express Briefs*, 65 (10), 2018, 1370-1374. The dissertation author is the primary investigator and author of the work in these papers.

Chapter 3

A Rugged Wearable Modular ExG Platform Employing a Distributed Scalable Multi-Channel FM-ADC Achieving 101 Decibel Input Dynamic Range and Motion-Artifact Resilience

3.1 Abstract

This paper presents an active electrode system for biopotential acquisition using a distributed multi-channel FM-modulated analog front-end and ADC. The system is comprised of two integrated circuits: First, an FM-modulating front-end active electrode integrated circuit replicated N times for N channels, and second, a single gateway integrated circuit used to digitize and transmit the aggregate FM spectrum of all front-end channels off of the body using a UWB transmitter. After off-body demodulation,

the system has 27dB better dynamic range and 25dB better FoM than other state of the art active electrode designs, and is the first such system to demonstrate quantifiable motion resilience. Compared to other integrated AFE arrays used in non-active electrode applications, the proposed design achieves 18dB better dynamic range and 5dB better FoM.

3.2 Introduction

Biopotential signals are voltages measured from an organism caused by the flow of ions in its body. These voltages may be the result of a number of physiological processes and their recordings over time are given a different name depending on their source: Muscle activity generates an electromyogram (EMG), heart activity leads to an electrocardiogram (ECG), eye activity creates an electrooculogram (EOG), and the brain produces an electroencephalogram (EEG), just to name a few.

While invasive measurement techniques which pierce the body do exist for acquisition of all of these signals, this paper will consider them as non-invasively recorded from an electrode placed on the subject's skin, and we refer to this type of biopotential measurement, in general and without regard to source, as ExG.

ExG allows us to indirectly observe the physiology of an organism by recording its electrical activity. These recordings have diagnostic use in medical clinical settings for the diagnosis, monitoring, and subsequent treatment of disease. The usefulness of ExG, however, is not limited to the diagnostic case. ExG as employed in research set-

tings allows us to further understand humans and other organisms at a fundamental level by observing their body's response to external stimuli. In addition, these recorded responses can be used in greater systems, such as brain-computer-interfaces (BCI), prosthetic applications, and others.

This work introduces a system design focused on two goals: First, to reduce the power of ExG acquisition so that biopotential measurement systems can be made with smaller batteries and longer battery lives in smaller, more easily wearable, form factors. Second, to use electronic techniques to reduce cabling overhead and the severity of motion artifacts inherent in biopotential acquisition systems, enabling robust and rugged systems that can be applied in new and interesting ways. The following subsections of introduction will provide additional background on ExG, further motivate the work, and introduce the proposed system.

3.2.1 ExG Signal Properties

Biopotential signals sensed at the skin vary in amplitude based on organism, signal source, and the specific activity that the organism is undertaking. In modern human ExG applications, the smallest relevant signals are on the order of microvolts and vary over time periods ranging from tens of seconds to milliseconds, resulting in a signal bandwidth ranging approximately from 0.1Hz to 500Hz [11].

In applications where, for ease of use or to deal with thick hair covering skin, dry electrodes are employed, the electrode can shift on the subject's skin and generate static

charge which is sensed at the electrode. These motion artifacts can reach up to one volt and potentially saturate input electronics and cause the microvolt-level ExG signal to be momentarily lost. To combat this problem, a number of schemes have been employed, including electrode impedance based motion artifact measurement and feedback [12,13] and filter-based feedback techniques [14]. The only surefire way to ensure all relevant ExG is not lost for any length of time, however, is to fully quantize the voltage present at the electrode, including both the motion artifact and the signal of interest, and remove the motion artifact later in post-processing using digital filters [15, 16] or by subtracting stored measurements of motion from an accelerometer [17, 18]. In such a case, the system requires an input dynamic range of over 100dB to ensure tracking of both 1 microvolt ExG and 1 volt motion-induced signals.

In clinical and research settings, EEG brain-wave recording devices have the highest density of recording electrodes placed on the skin, which can reach 256 electrodes per subject in some applications [19]. Thus, a system of use in clinical and research application must achieve recording of 256 ExG signals with 500Hz bandwidth and over 100dB of dynamic range.

3.2.2 Ambulatory ExG Acquisition

Recording of ExG from subjects in motion guarantees the presence of motion artifacts. Such artifacts from electrode motion on the skin are aggravated when the mass of the equipment used for recording contributes inertia to the system and causes the elec-

trodes to move further during a shift of subject position than they would on their own. In addition, an additional type of interference caused by the motion of electrode cabling is introduced known as cable sway electromagnetic interference (EMI). This type of interference occurs due to the movement of the cables through ambient electromagnetic fields during subject movement and can reach 200 millivolts in amplitude [20]. Prior work has demonstrated that EMI can be mitigated via ensuring matched electrode contact impedances [20], shielding the device, electrodes, and cabling [21], and postprocess filtering [22]. We will show in Section 3.3.3 that the approach presented in this paper also virtually eliminates this type of interference in ExG acquisition.

3.2.3 Traditional ExG Acquisition Approaches

In a traditional biopotential acquisition system, depicted in Figure 3.1, N channels of ExG are acquired by N analog-to-digital converters (ADCs) via N wires which carry the ExG voltage from the electrode to the ADC. The ADCs may [23] or may not be preceded by active electrodes designed to mitigate cable sway EMI. These active electrodes contain a low output impedance amplifier designed to robustly drive the cable to the ExG voltage, since it is the high impedance nature of the electrode signal source which leaves the cable vulnerable to EMI. The power consumption of such traditional biopotential acquisition systems is dominated by their many ADCs. Typical power consumption per channel in such systems targeting wearable application is around 100 microwatts per channel with around 80dB of dynamic range [24–27]. This

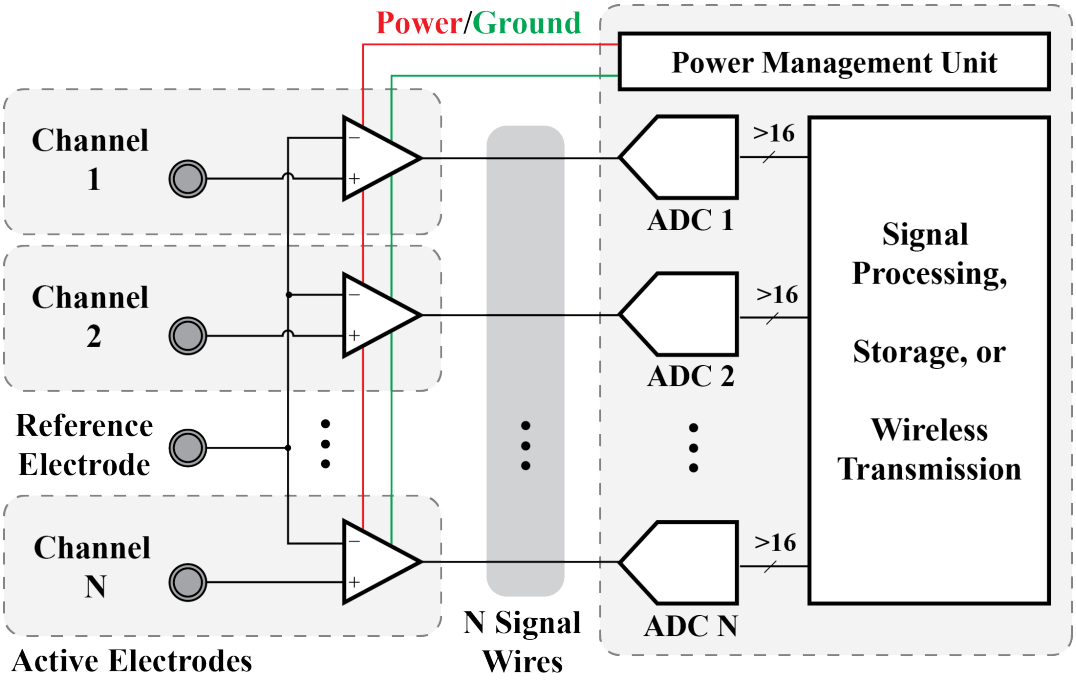

Figure 3.1: Block diagram of traditional N-channel biopotential recording system.

power consumption level is workable for all-day system wear with a reasonably sized battery, but this dynamic range is just shy of being clinically useful in settings with artifacts and EMI caused by subject motion.

3.2.4 Proposed ExG Acquisition Approach

The approach taken for biopotential acquisition in this work was previously discussed in [28]. This paper expands upon that publication, discussing further system-level considerations, expounding on circuit-level design details, and presenting additional measurement results.

In the proposed approach, depicted in Figure 3.2, N channels of ExG are aggregated together onto a single wire prior to being acquired by a single ADC. This aggre-

gation technique is based on frequency modulation (FM) and frequency division multiplexing (FDM) and has the advantage of reducing cable count and ADC count in such a signal acquisition system [5]. Cable count reduction reduces system cost and weight in portable systems, and has the added benefit of reducing system inertia, therefore potentially lessening the severity of motion artifacts. ADC count reduction has advantages in systems based on off-the-shelf microprocessor-based boards where only one or a few ADCs are available for use. When employed for a single channel as a monolithic ADC in silicon, the FM method employed is known as an FM-ADC and demonstrates comparable energy efficiency with state-of-the-art delta-sigma ADCs [29]. In a single channel FM-ADC, the FM demodulation of the single channel is implemented on-chip to directly recover samples of the input analog waveform in real time. In this work, multiple channels are recorded simultaneously in the FM quantizer and FM demodulation is offloaded to another energy-rich device to save power in the acquisition system; we call this a distributed multi-channel FM-ADC with demodulation offloading.

Other multiplexing strategies could have been adopted in lieu of FM-FDM; the possibilities are depicted in Table 3.1.

Table 3.1: Comparison of multiplexing strategies as applied to biopotential measurement.

Strategy	Requirements in N-Channel System		
	Wire Count	ADC Count	ADC Resolution
Traditional System	N	N	>100dB
Serial Digital (TDM, I2C, SPI)	1	N	>100dB
Digital FDM (OOK, PSK, etc)	1	N	>100dB
AM FDM	1	1	>100dB
FM FDM	1	1	>70dB

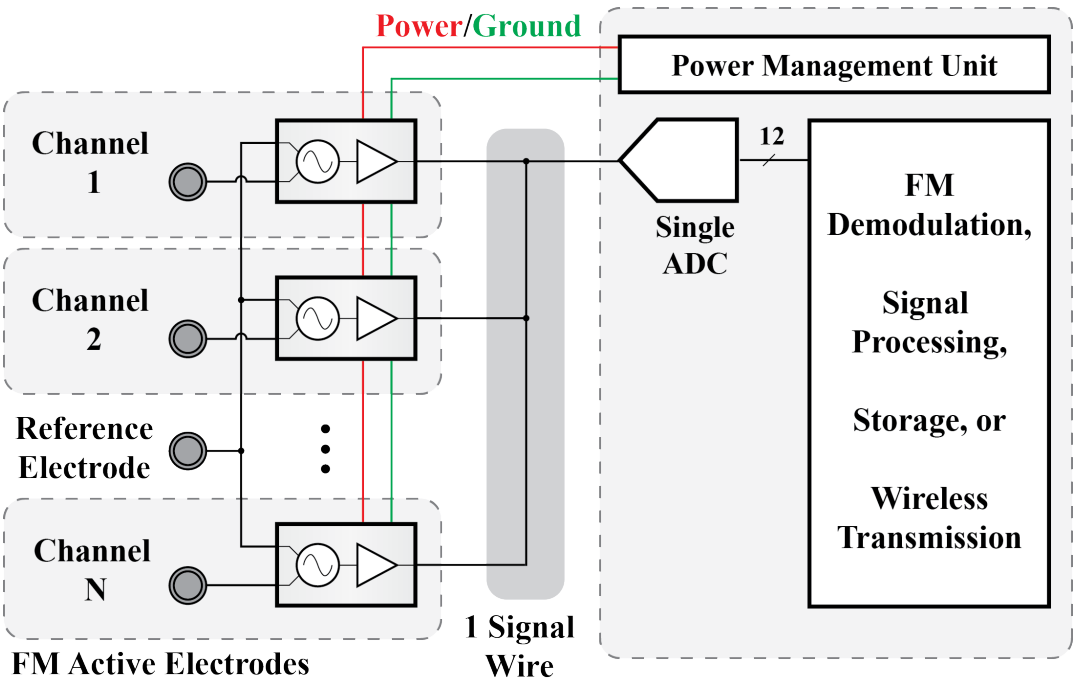

Figure 3.2: Block diagram of distibuted FM-ADC biopotential recording system.

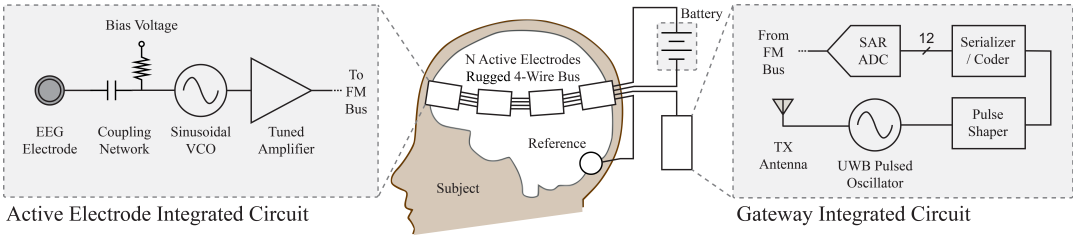

Figure 3.3: Block diagram of the implemented robust biopotential recording system using distributed multi-channel FM-ADC and offloaded demodulation.

While all multiplexing approaches reduce wire count, digital multiplexing does not have the aforementioned advantage of reducing ADC count. Amplitude modulation (AM) FDM could be used, but the single ADC employed for quantization of the aggregate FDM signal would be required to maintain at least 100dB of dynamic range in amplitude resolution since AM represents the message signal's amplitude in amplitude of the carrier. Due to N-channel voltage-domain carrier summation, well over 100dB of

dynamic range would be required, and the sample rate of this single ADC would need to be fast enough to capture the entire AM-FDM spectrum bandwidth. In practice, according to a survey of state-of-the-art ADCs [30], this would mean expending around 10 to the 6th picojoules per sample and, assuming the AM carriers were well above ExG frequencies in the 1-10kHz range, using a 20 kilosample per second ADC resulting in a total ADC power expenditure of approximately 20 milliwatts. This is well above the feasible system power for our target application of a wearable multi-channel ExG system. FM-FDM does not require a very high dynamic range quantizer, as the message signals are represented in the frequencies of the carriers, not their amplitude. Because of this distinct advantage, FM-FDM was adopted as the multiplexing strategy of choice for this work.

Section 3.3 details the design and measurement of the distributed multi-channel FM-ADC responsible for acquisition of the aggregate FM-FDM carrier signal which contains the signal information of all channels simultaneously. As mentioned previously, this carrier signal is offloaded to an energy-rich device for demodulation of the individual channels, and this is achieved by transmitting the quantized carrier to another device via a low-power ultra-wide-band (UWB) transmitter, whose design and measurement is discussed in Section 3.4. Section 3.5 compares the system with previously published works and Section 3.6 presents conclusions and possible future work.

3.3 Distributed Multi-Channel FM-ADC

3.3.1 System Considerations

The distributed multi-channel FM-ADC is depicted in Figure 3.3. Its inputs are N analog voltage waveforms to be recorded, and its output is a single stream of samples which contain the FM-FDM carrier spectrum with N distinct FM channels which is present on the FM-FDM bus wire. This stream of samples of the FM-FDM bus contains the analog voltage information present at all N inputs simultaneously and individual channels can be filtered out and demodulated at a later time as discussed later in Section 3.3.3.

The conversion of each input channel into an FM carrier is achieved by employing one voltage-controlled oscillator (VCO) per channel. A tuned drive amplifier follows each VCO to achieve the desired FM-FDM bus. Were the outputs of the VCOs employed for this work directly connected together, they would load each other strongly; hence, this drive amplifier is necessary to isolate them from each other. In addition, each tuned drive amplifier has a bandpass response which ensures the carrier driven onto the bus in highly sinusoidal. This is important for many channels to share a bus without interfering with one another. The combination of VCO and tuned drive amplifier is referred to in this work as the FM active electrode and is implemented as a single integrated circuit per channel.

The FM-FDM bus wire is tied to the output of all active electrodes in the system

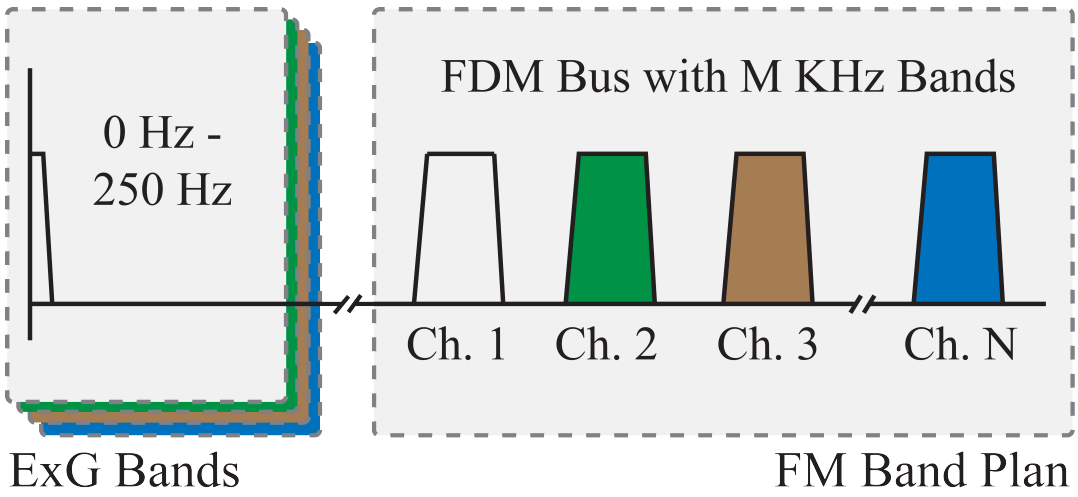

Figure 3.4: Frequency domain representation of ExG message signals and their mapping to the system's FM-FDM bus.

and connects to the input of a single 12-bit successive approximation register (SAR) ADC which acts as the quantizer for the FM-FDM signal. In our system this SAR ADC is integrated along with the UWB transmitter which offloads the aggregate FM-FDM signal on a single integrated circuit called the gateway IC.

Figure 3.4 depicts a frequency-domain representation of the system's FM-FDM bus. The width, or occupied bandwidth M, of each channel in this frequency-domain bandplan is an important design parameter of the system and can be controlled by selecting the VCO gain KVCO, which has units of Hz/V. Selection of M is dictated in an FM system by

$$SNR_{FM} = 10log_{10}(3D^2(D+1)) + CNR \qquad (1)$$

where the bandwidth expansion ratio D is defined as the occupied channel band-

width M divided by the message bandwidth. The first term of Equation 1 is known as FM Coding Gain and represents the increase in system SNR achievable over the SNR of the channel over which an FM signal is transmitted. The second term, carrier-to-noise ratio or CNR, is set in our system by the SNR of the gateway SAR ADC.

It is important to note that, with a fixed bit depth ADC, this CNR is dependent upon the number of channels in the system since carrier waves sum in voltage at the ADC's input and the sum of all the carriers must not exceed the input range of the ADC. Figure 3.5 shows the results of MATLAB simulations in which a variable number of carriers are summed and peak amplitude out to three standard deviations is reported. From this data, we see that 64 summed carriers of amplitude 1 show a peak-to-peak amplitude less than 8 but more than 4; thus, in a 64-channel system, the effective ENOB of the ADC used to sample the FM-FDM bus is reduced by 3 bits.

Referring back to Equation 1 and using a CNR of 55dB to represent a system with a 12-bit ADC sampling a 64-channel FM-FDM bus, we find that for 100dB of system SNR a bandwidth expansion of approximately D = 25 should be selected. If ExG signals with a bandwidth of 500Hz are considered, this would require FM-FDM bands width a width of around 12.5KHz.

Analysis until this point has considered a noiseless FM source, however, and when noise is introduced in the VCO the FM-FDM bandplan must be adjusted to maintain system performance. Specifically, since the input signal's voltage is represented in the frequency/phase of the carrier generated by the VCO, phase noise of the VCO itself appears as noise in the demodulated system output. MATLAB simulations of an FM

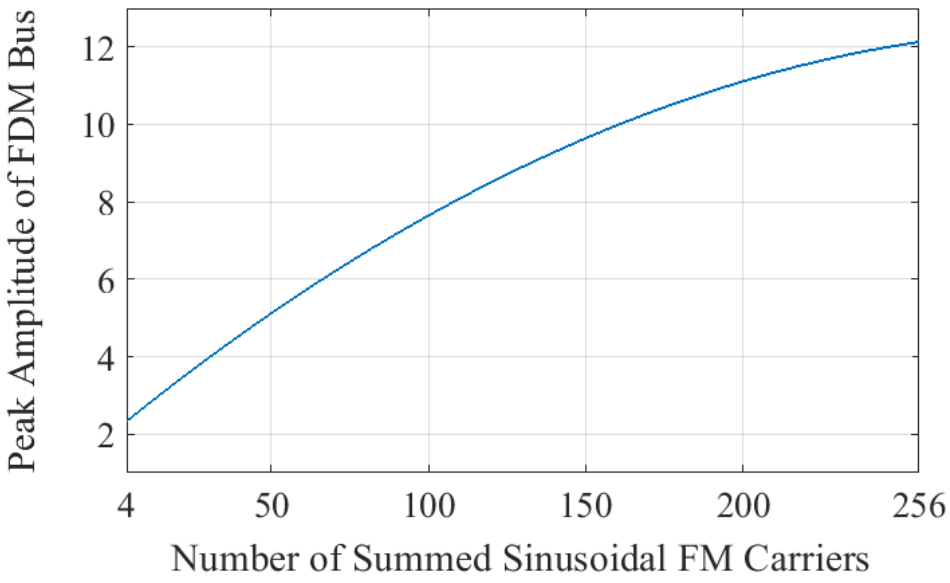

Figure 3.5: MATLAB simulation results of the three-sigma peak amplitude of summed sinusoidal FM carrier waves.

system with variable VCO gain (and therefore variable FM bandwidth) are shown in Figure 3.6. To maintain high system SNR, either the FM bandwidth can be increased to push and pull the carrier farther in frequency and reduce the effect of phase noise, or the phase noise of the VCO itself can be reduced. In our system, therefore, phase noise was minimized in the VCO given power and area constraints, and then VCO gain was selected to compensate and maintain over 100dB system SNR to meet the ExG signal acquisition application requirements laid out previously.

Besides the bandwidth occupied per channel, the other important designer-selectable parameter in this FM-FDM system is FM carrier frequency. By keeping the carrier frequency low, power is saved in the VCO used for FM, since oscillator power is proportional to oscillation frequency when other oscillator properties are held constant. A

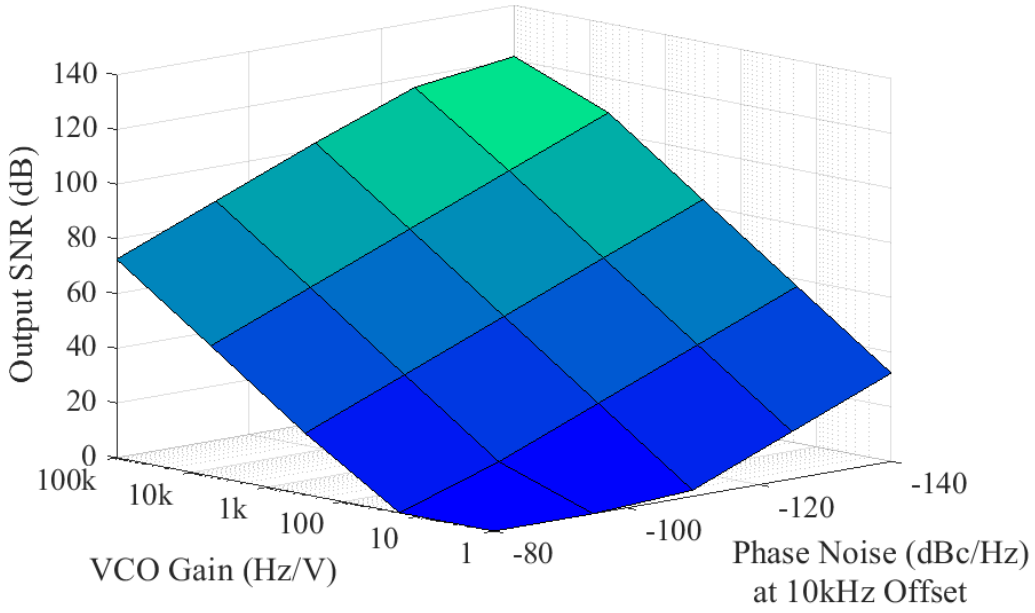

Figure 3.6: MATLAB simulation results demonstrating the effect of VCO gain and phase noise on system SNR.

lower carrier frequency would also enable a lower sampling rate in the gateway SAR ADC, were it sampling the carriers while satisfying the Nyquist Criterion. As we will explain later in further detail, however, our system is able to employ bandpass sampling in the SAR ADC to sample at the Nyquist rate for the aggregate FM spectrum bandwidth, not the Nyquist rate for the carriers' absolute frequencies. The trade-off between gateway SAR ADC power and carrier frequency is therefore decoupled and is not of primary concern in selection of carrier frequency. Practical considerations concerning the circuit implementation of the VCO used for FM prevent system carrier frequency from being selected arbitrarily low; this will be discussed in the next section.

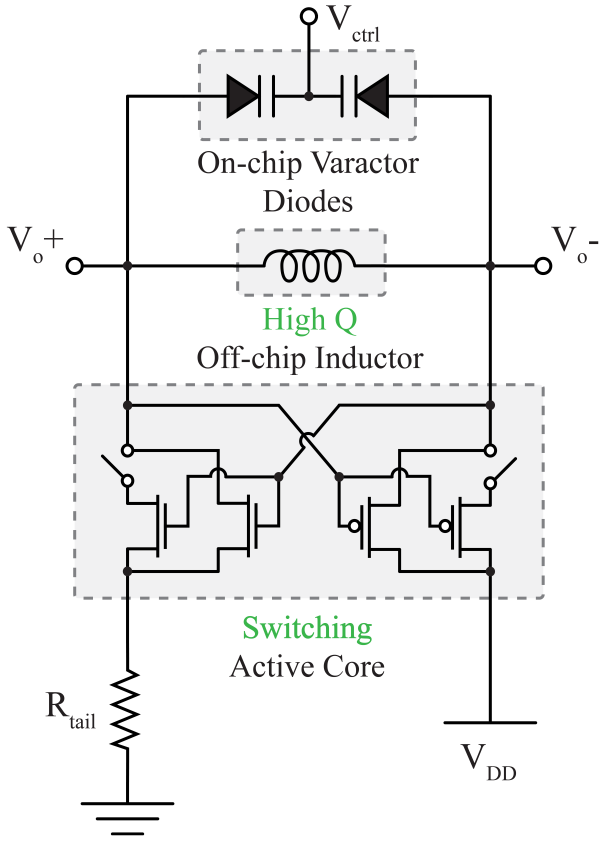

Figure 3.7: The voltage-controlled oscillator implemented on the active electrode integrated circuit.

3.3.2 Circuit Implementation

The VCO used for this work, pictured in Figure 3.7, is a cross-coupled LC tank current-reuse voltage-controlled oscillator [7]. It was chosen for its ability to achieve low enough phase noise at reasonable power consumption. Other VCO topologies evaluated for this work based on ring oscillators, op-amps, and RC tanks proved in simulation to have phase noise performance too poor to meet system SNR and power constraints simultaneously.

The VCO features a switching active core topology [8], which starts up oscilla-

tion at system power-up via large transistors which are switched out once oscillation is achieved to save power in the oscillator during normal system operation. The center frequency of oscillation, referred to as the FM carrier frequency in the previous section, is set via selection of the tank's inductor size and the sizing of the on-chip varactor diodes. If the inductor is made smaller and the varactors bigger in equal proportions, the oscillation frequency will remain constant but KVCO will increase. Conversely, if the inductor is made larger and the varactors smaller, KVCO will decrease. Thus, changing the inductor value in the VCO relative to the amount of capacitance employed while keeping the center frequency the same enables selection of KVCO to fit the system bandplan as explained in the section prior.

The capacitance versus control voltage relationship of the on-chip varactor diodes used for this work's VCO frequency control is quite nonlinear; this nonlinearity appears directly as system output nonlinearity after demodulation, since the control voltage is the message signal to be measured and the capacitance of the tank dictates FM carrier frequency which is ultimately demodulated to recover the message signal. It is this nonlinear property of the varactor diodes used for VCO tuning which influences our selection of system carrier frequency. At lower VCO frequencies, to cover the same FM bandwidth, the VCO must be pulled over a larger range relative to to its oscillation frequency. This means that a larger percentage of the employed capacitance must be changed, and therefore the varactor control voltage must cover a larger operating range to realize this. By going to higher and higher carrier frequencies, an equal FM bandwidth can be covered by a smaller percentage change in the tank's capacitance, so a smaller and more

locally linear region of C-to-V curve is employed. A VCO oscillation frequency of around 15 MHz was selected for this work to achieve an application-workable tradeoff between VCO power consumption and system linearity.

Figure 3.8 depicts the tuned drive amplifier which follows each VCO's output and drives the VCO's FM carrier wave onto the shared FM-FDM bus. This amplifier, based on the design in [31], serves two purposes: First and foremost, it isolates the VCO tanks from each other, effectively providing a favorable impedance transformation so that all the FM carrier signals can reside on the FM-FDM bus wire without loading the outputs of any of the VCOs. A second important function of the tuned amplifier results from its frequency response; since it functions as a sharp bandpass filter it ensures a low total-harmonic-distortion (THD) sinusoidal carrier is driven from each VCO onto the FM-FDM bus. The low harmonic content of the carriers enables bandpass sampling in the gateway's SAR ADC - were the carriers not so purely sinusoidal, their harmonics would fold back into the first Nyquist zone and interfere with one another, corrupting the message signals and reducing post-demodulation system performance. As our carriers reside at 15MHz but the aggregate FM spectrum for 64 channels is only 1.28MHz, we are able to reduce ADC power from approximately 5.7 milliwatts to 190 microwatts thanks to bandpass sampling enabled by the use of the tuned drive amplifier.

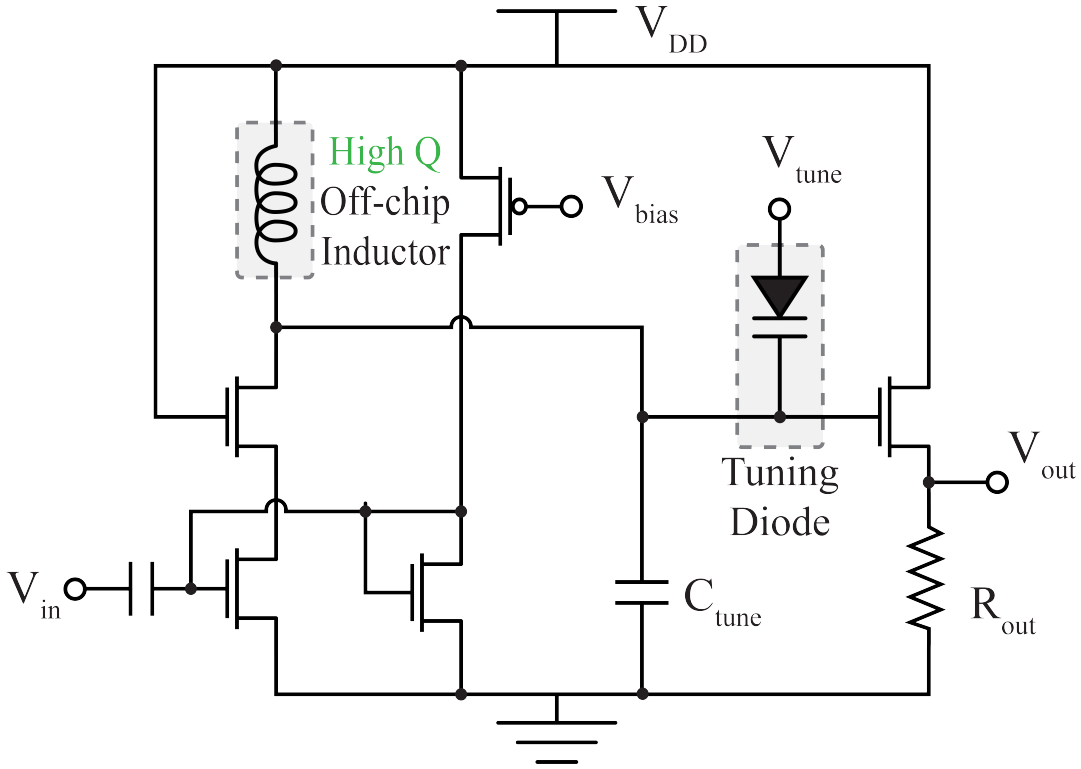

Figure 3.8: The bandpass tuned amplifier implemented on the active electrode integrated circuit.

3.3.3 Measurement Results

A series of experiments were conducted to characterize the performance of the active electrode integrated circuit alone. For these tests, stimulus was provided to the chip's VCO control voltage from a Stanford Research Systems DS360 low distortion function generator. The FM output of the chip's tuned drive amplifier was sampled at

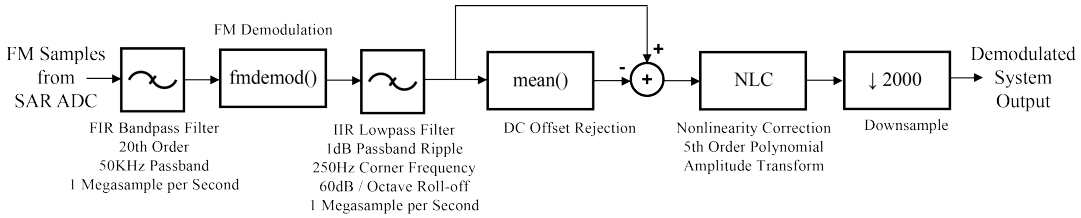

Figure 3.9: The demodulation scheme implemented in MATLAB that was used for all analog performance measurements.

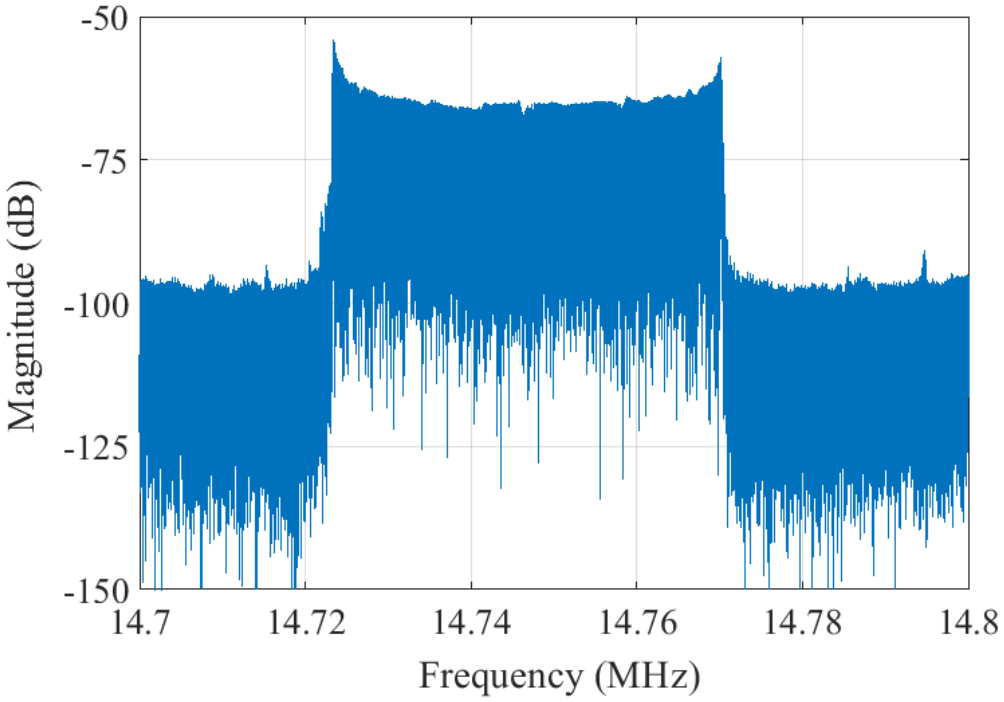

Figure 3.10: A single active electrode's FM output in the frequency domain.

1.28 megasamples/second using a Measurement Computing USB-2020 data acquisition system to mimic the bandpass sampling functionality of the gateway chip's SAR ADC. Demodulation of the chip's FM output was achieved in MATLAB using the approach illustrated in Figure 3.9. The nonlinearity correction (NLC) block consists of a fifth order polynomial transform that is fit to the system's measured nonlinearity during a one-time calibration in which a linear ramp signal is used as chip stimulus. This NLC, based on the scheme presented in [32], cannot achieve perfect system linearity, but does provide approximately 20dB improvement in SNDR over the demodulated system output to which NLC is not applied.

Figure 3.10 depicts a single active electrode's FM output in the frequency domain for a full-scale 10 millivolt amplitude 10 hertz sinusoidal input signal. A wideband

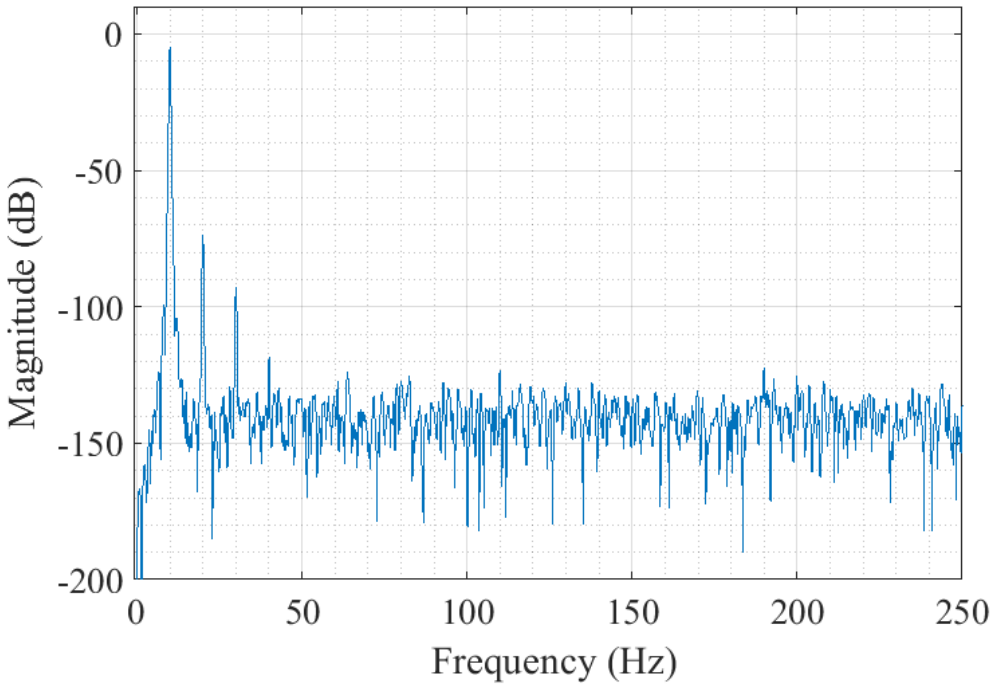

Figure 3.11: A single active electrode's demodulated output as recorded by the whole system.

FM spectrum is observed occupying approximately 50 kilohertz of bandwidth. After FM demodulation to recover the sinusoidal message, the recovered signal's frequency domain representation is seen in Figure 3.11, achieving 101 decibels of signal-to-noise ratio. Note the harmonic content present at 20 hertz and 30 hertz; this reflects the system nonlinearity introduced by the active electrode VCO's varactor diodes, whose nonlinear V-to-C relationship cannot be entirely compensated for by the system's NLC. Figure 3.12 plots SNR and SNDR of the demodulated system output for varying input amplitudes - it can be observed that, as the amplitude approaches full-scale (10 mV), the SNDR is degraded as the transition is made from the locally linear region to the globally nonlinear region of the VCO's varactor diodes' V-to-C response.

The SNR of the demodulated output from the active electrode is, as mentioned

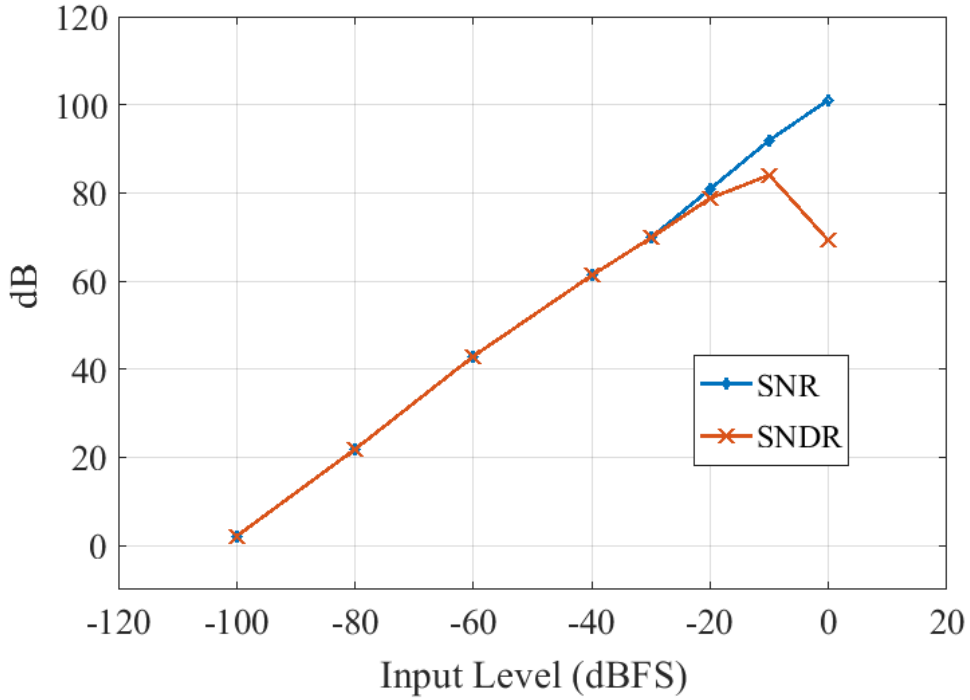

Figure 3.12: Measured SNR and SNDR across input voltage dynamic range.

earlier, limited by the phase noise of the active electrode's VCO. In Figure 3.13 we see the measured phase noise profile of the VCO circuit, gathered using a Keysight N9020A spectrum analyzer. It achieves -111dBc/Hz levels of phase noise at 10KHz offset, which, referring back to the simulation results presented in Figure X, are sufficient for over 100dB demodulated system SNR.

The active electrode IC does not use a gain amplifier prior to the VCO's input, and instead directly couples the electrode's baseband signal to the VCO's frequency tuning control voltage. This provides direct up-conversion to the FM domain in which the electrode signal is represented by carrier frequency, not voltage. Therefore, there is not a voltage rail up against which the signal can saturate like in a traditional amplifier. This non-saturating input feature of the system provides resilience to large motion artifacts

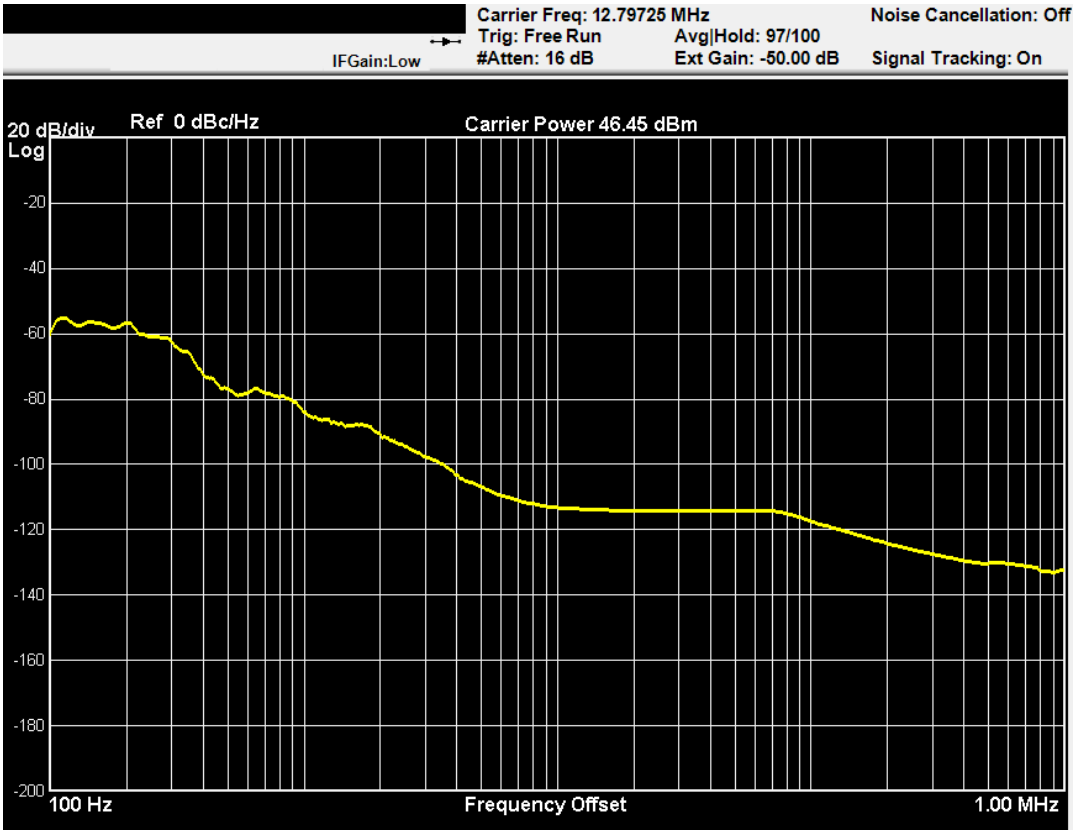

Figure 3.13: Measured phase noise of VCO employed for FM modulation.

at the electrode, provided sufficient guard band exists adjacent to each FM carrier on the FM bus wire. To test this feature, a 100 mV DC step voltage (10 the previously stated full-scale range of the VCO's input) is applied at the electrode in summation with a 10mV message sinusoid both with and without an input coupling capacitor. The demodulated output is shown in Figure 3.14 and is seen to track the 10mV sinusoid throughout the step disturbance. Hence, if larger than full-scale artifacts are expected at the electrode, the system can be reconfigured by spreading the FM carrier frequencies apart in the frequency domain, ensuring sufficient guard band such that large steps will not cause the FM channels to collide and the system will tolerate them without loss of

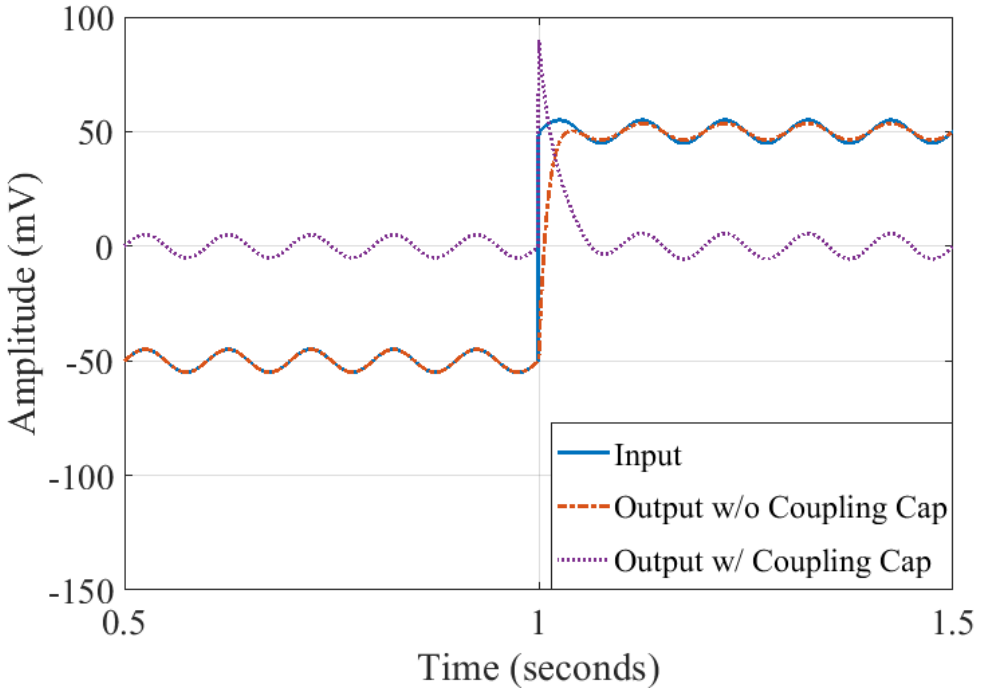

Figure 3.14: Demodulated system output for 100mV step voltage at active electrode input.

signal.

To demonstrate multi-channel FM-FDM bus operation, six active electrode integrated circuits had their tuned amplifier outputs tied together to achieve current-mode summation, and the six chips were driven with six different 1mV input sinusoids at 10, 50, 90, 130, 170, and 210Hz. We see six wideband spectra residing side-by-side in the frequency domain spectrum of the FM-FDM bus in this experiment, depicted in Figure 3.15. The six test sinusoidal signals are individually recognizable without any cross-talk after demodulation at the system output as shown in Figure 3.16. Note that the spur-free input range of the system was exercised here instead of the full-scale input range to minimize spurious content in the graph. An arbitrary number of active electrode ICs can have their outputs chained together to realize massively parallel ExG acquisition.

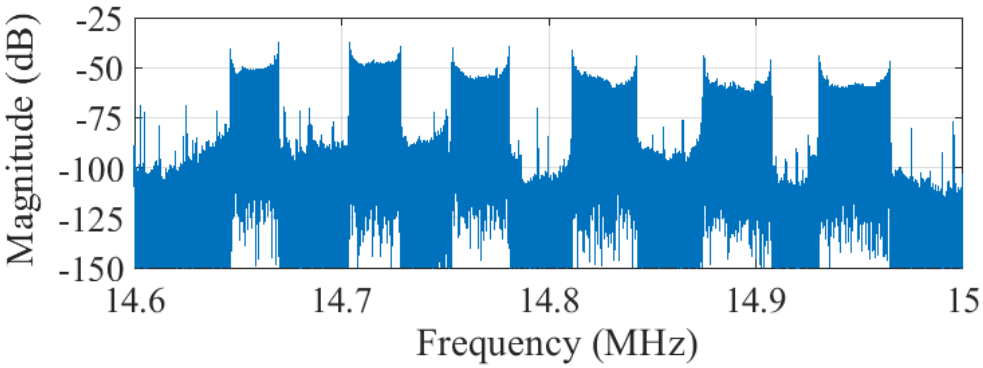

Figure 3.15: Frequency spectrum of FM-FDM bus with 6 channels.

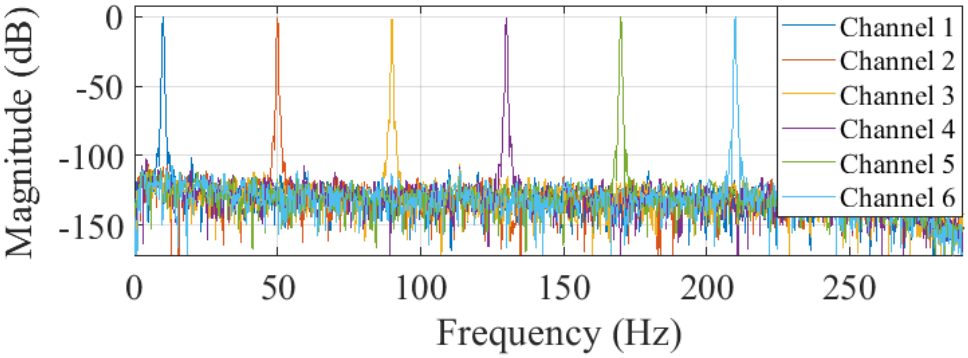

Figure 3.16: Demodulated system output in 6-channel test measurement.

The system designer needs only increase the ADC sampling frequency to accommodate any added FM bandwidth resulting from stacking additional channels in the frequency domain.

In preparation for on-body biopotential measurement in human subjects, the active electrode ICs were integrated into application printed circuit boards (PCBs), a photograph of one of which is depicted in Figure 3.17. The boards, which measure 12 millimeters by 16 millimeters each, are mounted atop standard biopotential electrode snap connectors (diameter 15 mm) for compatibility and ease of use with existing snap-button electrodes used in clinical and research applications. The boards contain a large

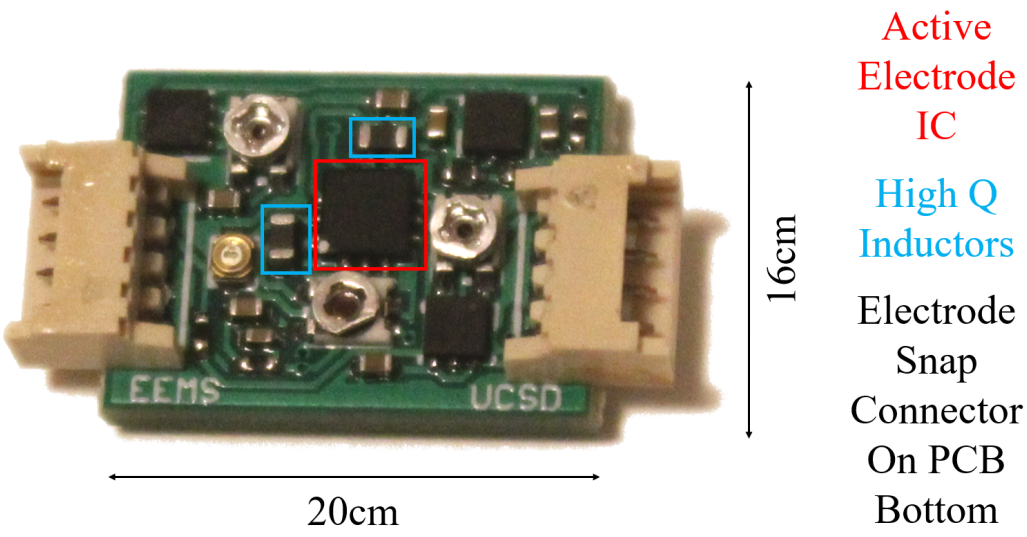

Figure 3.17: Active Electrode IC application printed circuit board.

area dedicated to screw potentiometer adjustment of chip biases and FM center frequency, a feature which could be integrated on-chip and digitally controlled via serial communication in a more ruggedized or commercialized system. Plastic-housed blade connectors on each side of the board allow for daisy-chaining boards together in a modular multi-channel acquisition system.

When multiple active electrode integrated circuits are connected in this way, special care must be taken that the VCOs in each do not interact. VCOs that share a power supply are known to influence each other in frequency by causing slight supply droop every time they instantaneously demand current to fill their tank, a phenomenon known as frequency pushing [33]. Frequency pushing could corrupt the measured signals by intermixing the results of disparate channels and therefore severely degrade system performance if the phenomenon is strong enough. A low drop-out voltage regulator (LDO) is used at each active electrode application PCB to mitigate this effect and ensure that

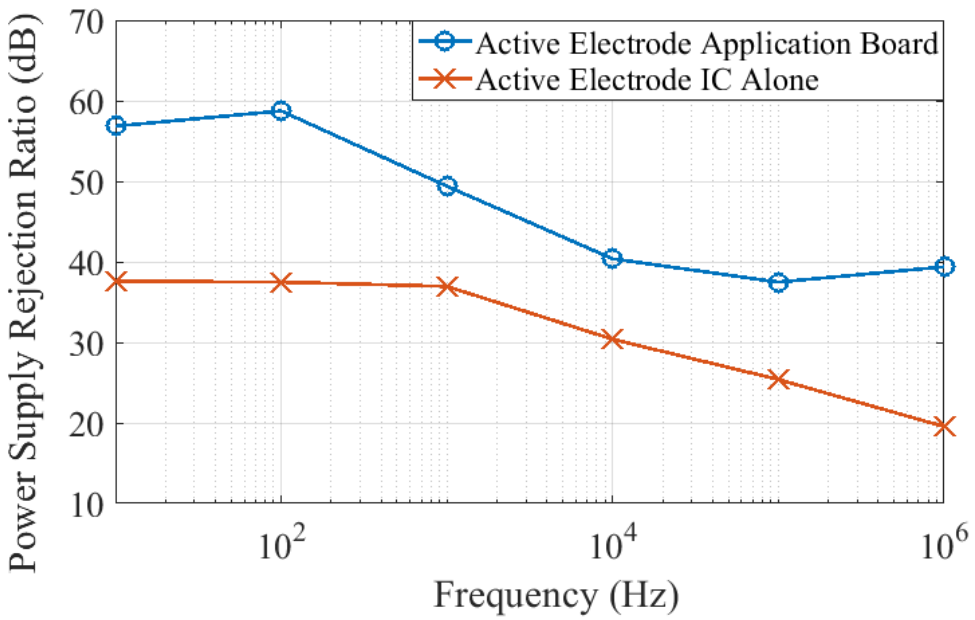

Figure 3.18: Active Electrode IC and application PCB power supply rejection ratio measurements.

the input signals do not corrupt one another. The robustness of the boards to power supply variation (such as that caused by changing load of other boards) can be seen in the power supply rejection ratio (PSRR), which was measured and plotted against frequency in Figure 3.18 for both the active electrode integrated circuits alone and with LDO on the application board. This measurement was conducted by using a Tektronix AFG3022C arbitrary waveform generator to generate a power supply with 100 millivolts of sinusoidal ripple at varying frequencies and observing the ratio of that ripple to ripple in the demodulated system output. We can see that PSRR improves by a factor of more than 20dB in the megahertz range at which the oscillators demand current from the power supply when an LDO is used on the application board.

Common mode rejection ratio (CMRR) is an often-computed metric for data

acquisition circuits; it is defined as the differential-mode output of a system divided by a common-mode perturbation applied into both of the system's differential inputs simultaneously. In our system, it was measured by connecting two active electrode integrated circuits' FM outputs together and driving both of their inputs with an identical 1mV peak-to-peak sine wave at various frequencies. The demodulated outputs of both channels were subtracted from each other and the result was divided into the amplitude of the test sine to calculate CMRR. The results are presented in Figure 3.19 over the system's usable input bandwidth. In theory, since the system's demodulated output amplitude is calibrated by driving a known amplitude as input and observing the result, achievable CMRR should be limited by this calibration. In practice, over time, the voltage-to-frequency response of each VCO used for FM varies due to thermal drift in the oscillator and it is this drift which accounts for the system's finite CMRR.

As indicated previously, due to the reduced cable overhead in the system and long signal wires carrying FM as opposed to baseband signals, the distributed multichannel FM-ADC approach affords some resilience to motion artifacts commonly encountered during biopotential measurement in ambulatory subjects. To demonstrate this advantage, the distributed multichannel FM-based biopotential recording system and a more traditional industry-standard OpenBCI biopotential measurement system were connected in tadem to measure ECG on a variably ambulatory subject. In this test, the subject went through 20 successive trials of standing at rest for two seconds and then jogging in place for two seconds. Successive trials were used to ensure relatively consistent heart rate under exercise conditions; the presented data is from the 20th trial.

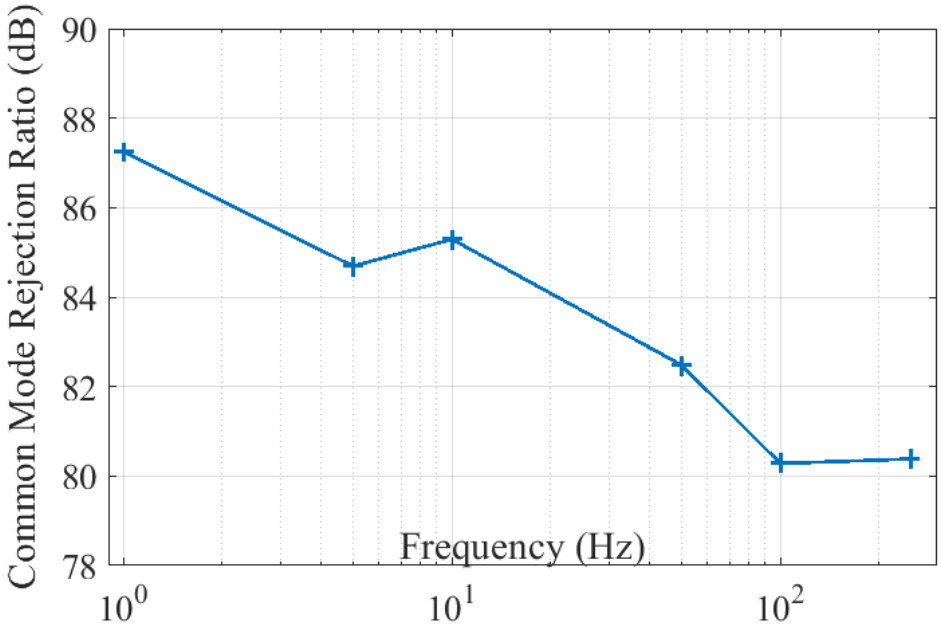

Figure 3.19: Active Electrode IC common mode rejection ratio measurements.

Both systems recorded differential waveforms for the duration of the exercise with six electrodes each placed on the chest. As can be clearly seen in transient recordings from the V2 chest electrode in Figure 3.20, the distributed FM-ADC biopotential recording system tolerated subject motion better, with less jogging-induced oscillation in the transient waveform. In Figure 3.21, the FFTs of the color coded transient waveforms are presented and the motion-induced frequency behavior around 6 Hz and 7 - 14 Hz is seen more strongly in the OpenBCI system's recording during subject motion than any of the other waveforms. According to normalized cross-correlations between still and motion data from each system, the distributed FM-ADC based system performs 2.9x better than the OpenBCI system.

In addition, the reduced cable overhead signal wires carrying FM also affords

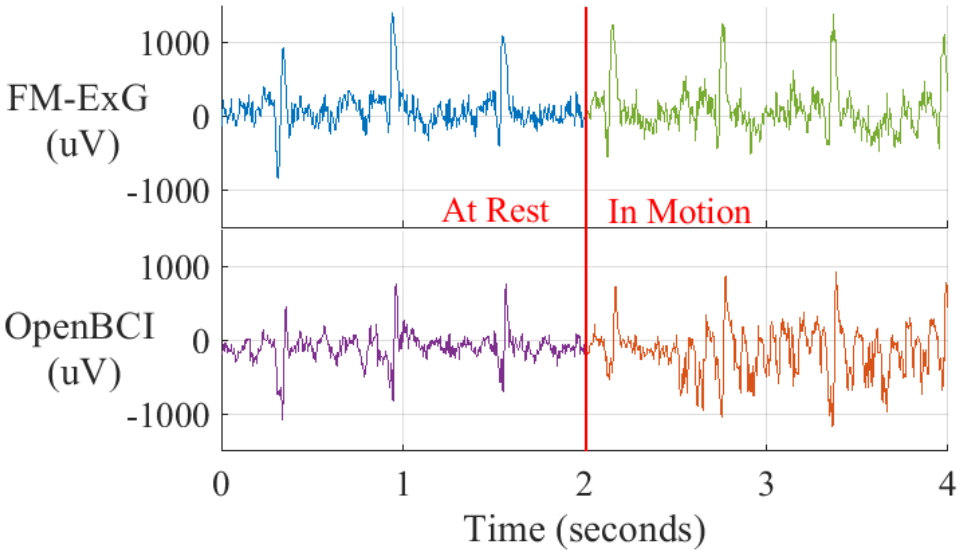

Figure 3.20: Comparison between FM-ExG and OpenBCI transient traces during subject motion.

the system some resilience to power line interference in the signal cables. Again the FM-ExG system was benchmarked against the commonly-used OpenBCI biopotential acquisition system; a two-prong United States power cable was brought within 1 centimeter of both the FM-ExG system's FM-FDM bus wire and the OpenBCI system's electrode lead cables during an ECG measurement on a resting subject. The resulting ECG transient waveforms are depicted in Figure 3.22. In the figure's zoom box, it is easily seen that the 60Hz coupling present in the FM-ExG system is lower than that of the OpenBCI system. This is corroborated by the Fourier transforms of both signals, seen in Figure 3.23 - a stronger peak at 60Hz is seen in the OpenBCI ECG's Fourier transform than that of the FM-ExG system.

The FM-ExG system was also validated in an EEG-based experiment; a steady-

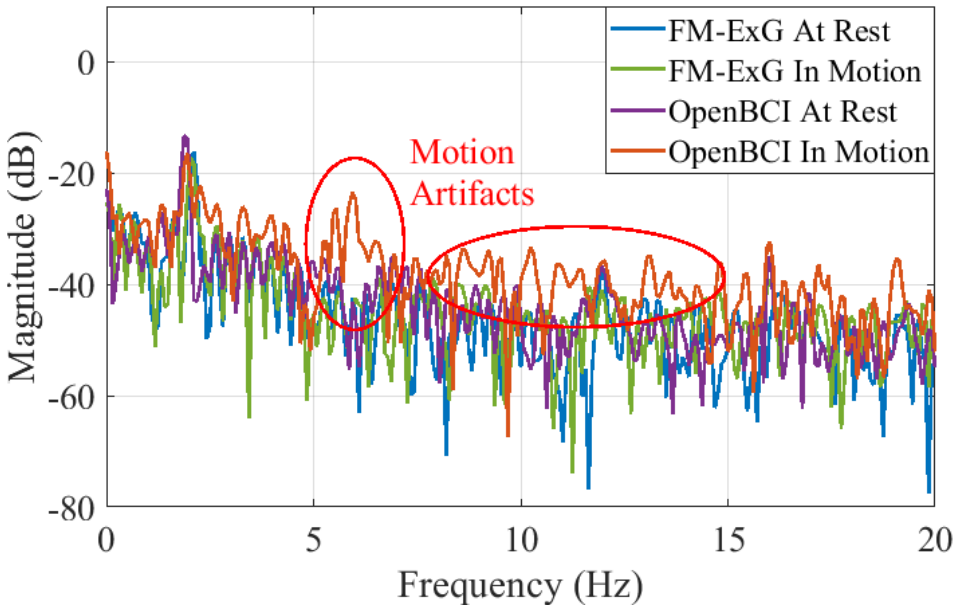

Figure 3.21: Comparison between frequency components in FM-ExG and OpenBCI recordings during subject motion.

state visually evoked potential (SSVEP) experiment was chosen as it is often involved in brain-computer interface systems and is a well-known EEG test [34]. In this test, the subject wore a headband with six active electrode integrated circuits used for EEG across the forehead. The subject viewed a computer monitor flashing between black and white screens 10 times per second - Figure 3.24 shows the frequency domain representation of the right temple EEG measurement (with reference placed behind the left ear) acquired by the distributed FM-ADC biopotential acquisition system. These results indicate more brainwave power at 10Hz, corresponding to the 10Hz flashing of the monitor screen during the SSVEP trial.

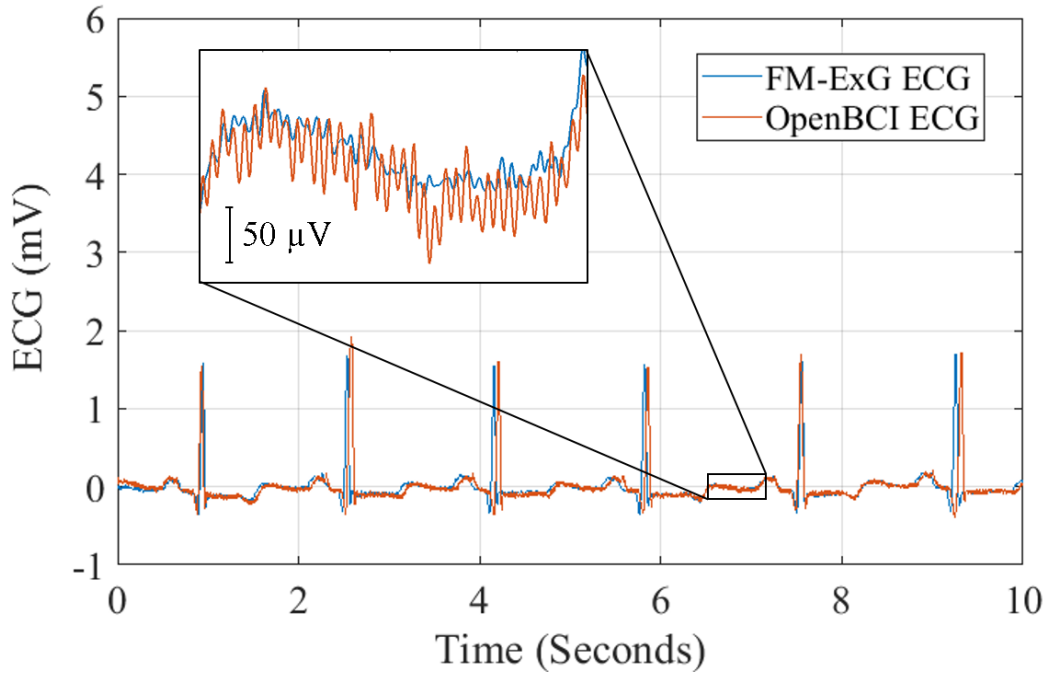

Figure 3.22: Comparison between FM-ExG and OpenBCI transient traces with 60Hz power line interference present.

3.4 UWB Gateway System on Chip

3.4.1 Motivation

Once the FM-ExG active electrode ICs have upconverted the ExG signals of interest into the FM domain, they must be quantized and transmitted off-body for later demodulation. Such is the function of the gateway integrated circuit exposited in this section. A SAR ADC was chosen as the gateway quantizer because SAR ADCs are able to achieve the moderate bit depth of 12 bits required for this application at 1 megasample per second with state-of-the-art efficiency [30]. An ultra-wideband (UWB) radio was designed to meet application requirements; UWB is a low power high data rate radio op-

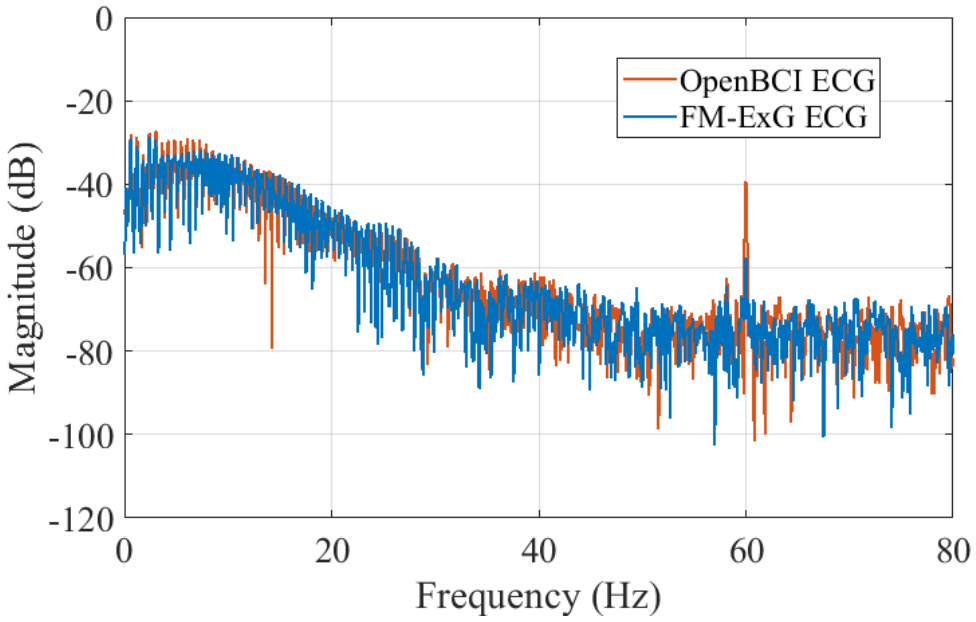

Figure 3.23: Comparison between frequency components in FM-ExG and OpenBCI recordings with 60Hz power line interference present.

tion with some advantages over other radio types, including increased noise resistance, enhanced security, resistance to jamming, multipath immunity, and high object penetration [35]. These advantages, coupled with the fact that it occupies a separate spectrum from the critical Wi-Fi networks in hospitals, make UWB transmission optimal for use in clinical ExG settings where reliability and security are tantamount.

3.4.2 Circuit Implementation

An overall block diagram of the gateway IC is shown in Figure 3.25. The design leverages an IR-UWB based digital transmitter with a low power SAR ADC digitizer. The FM-BUS is received by a 12 bit SAR ADC clocked at 1.28MSPS. The digital output from the SAR is serialized, coded and shaped prior to driving a UWB pulsed oscillator.

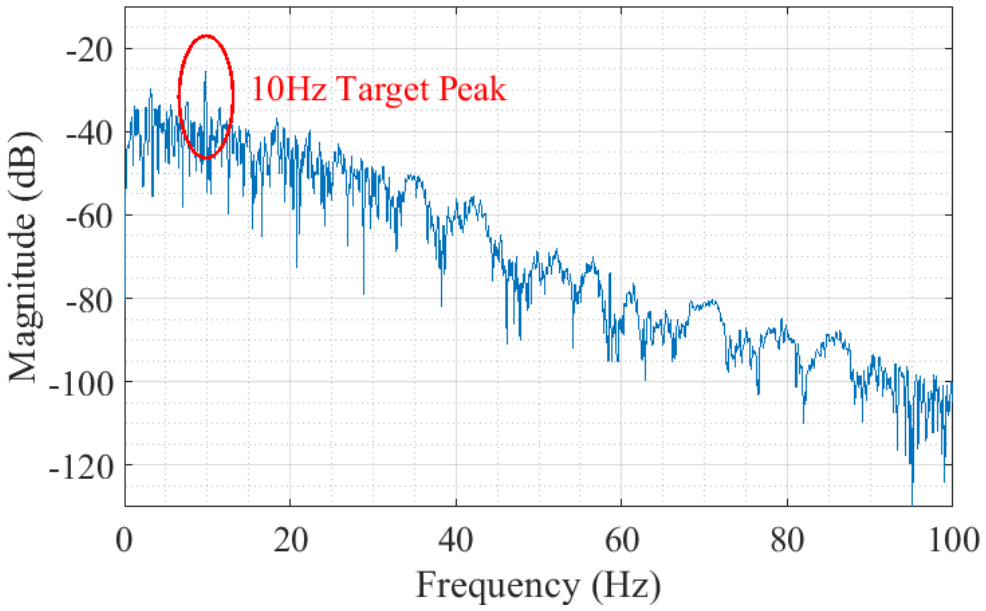

Figure 3.24: Frequency components in FM-ExG recording during SSVEP EEG experiment with 10Hz flashing target.

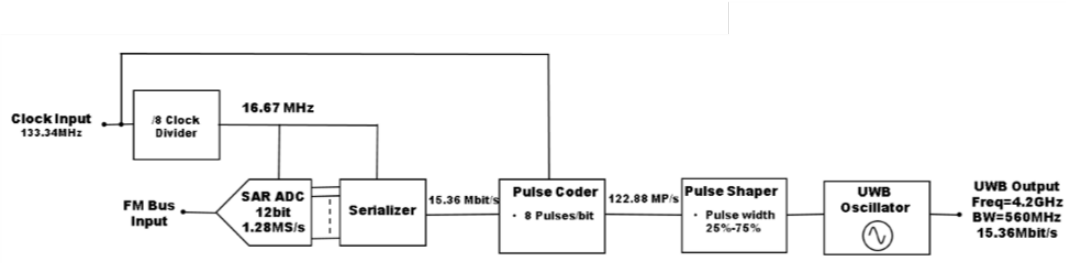

Figure 3.25: Top level block diagram of FM-ExG gateway integrated circuit.

The transmitter is suitable for energy detection (noncoherent) receiver architectures. The design is power efficient and minimally complex. The IC receives a single 133.34MHz off-chip clock which drives timing for the ADC, serializer and pulse coder. A data rate of 15.36Mbit/sec is achieved with each bit represented by a burst of 8 pulses using On-Off Keying (OOK) modulation.

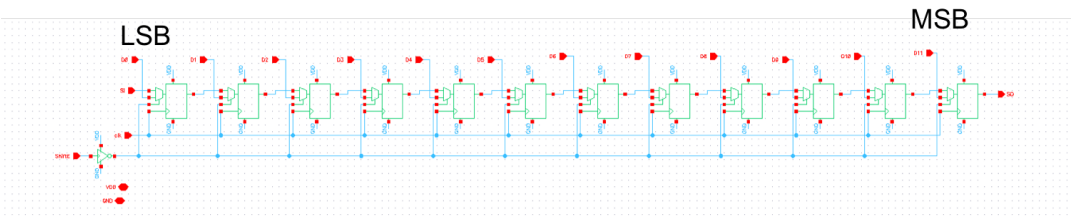

Figure 3.26: Circuit schematic of shift register based PISO used to serialize the output of the FM-ExG gateway SAR ADC prior to coding for UWB.

Serializer and Coder

To convert the parallel digital output of the ADC into a serial data stream for wireless transmission, a serializer is used. Serialization is realized using a Parallel-In Serial-Out (PISO) shift register approach. A schematic diagram of the serializer is shown in Figure 3.26. Each stage consists of a D flip-flop and a 2-1 MUX. The flip-flops are clocked using the same clock as the ADC (16.67MHz) while the MUXs are controlled by a counter which loads a new digital word from the ADC after the previous word cycles through the PISO. The design is oriented in an MSB first configuration.

After serialization the data is encoded for transmission. OOK modulation is adopted to minimize system complexity. The design, shown in Figure 3.27, implements AND logic between the input data stream and a pulse clock which generates an 8 pulse burst for each bit. Thus, a bit is represented by the absence or presence of 8 back-to-back pulses in a fixed time window.

Pulse Shaper

To ensure the transmitter meets FCC specifications at maximum average output power a pulse shaper is employed. Maximizing average output power leads to extended

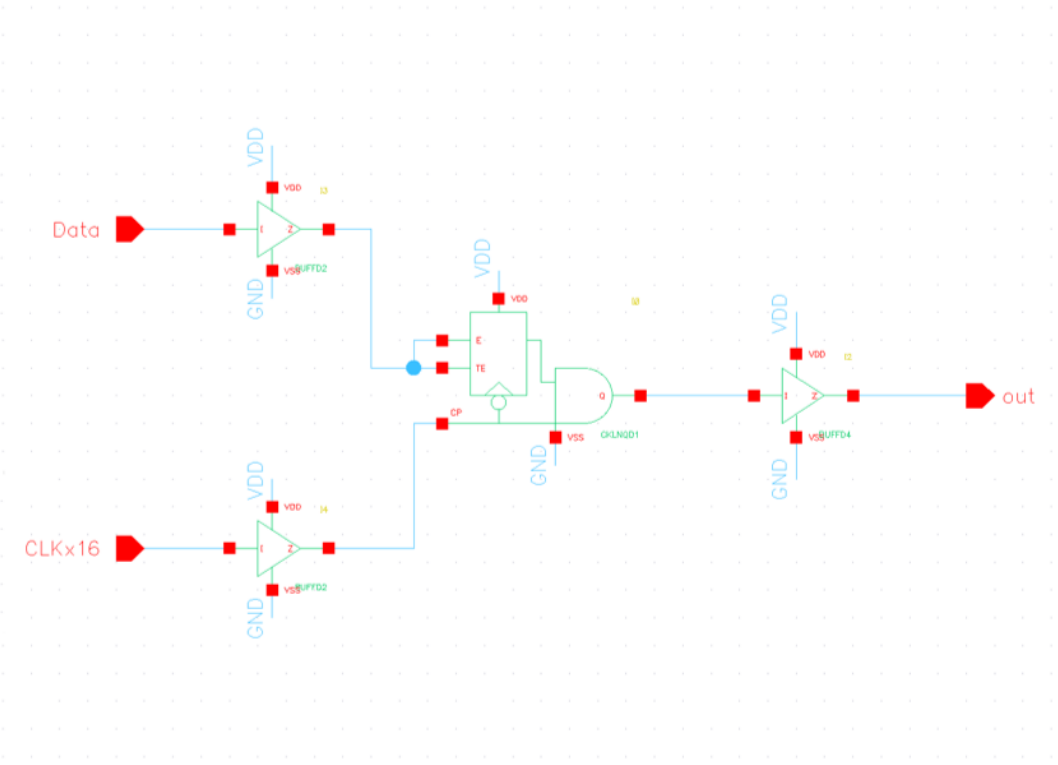

Figure 3.27: OOK coder schematic diagram from FM-ExG gateway integrated circuit.

communication range. The shaper adjusts the duty cycle of each pulse through a switchable RC delay. Binary weighted capacitance values are used with 3 bits of control as shown in Figure 3.28. This implementation allows for the duty cycle of each pulse to be tuned to a value between 25-75 percent. The control bits are brought out to pads to allow for off chip control.

UWB TX Oscillator

The core system block in the IR-UWB transmitter is the pulse generator. An oscillator with sub-band switching was employed in this work [36]. The design exhibits low complexity which allows for straight-forward implementation. Further, power con-

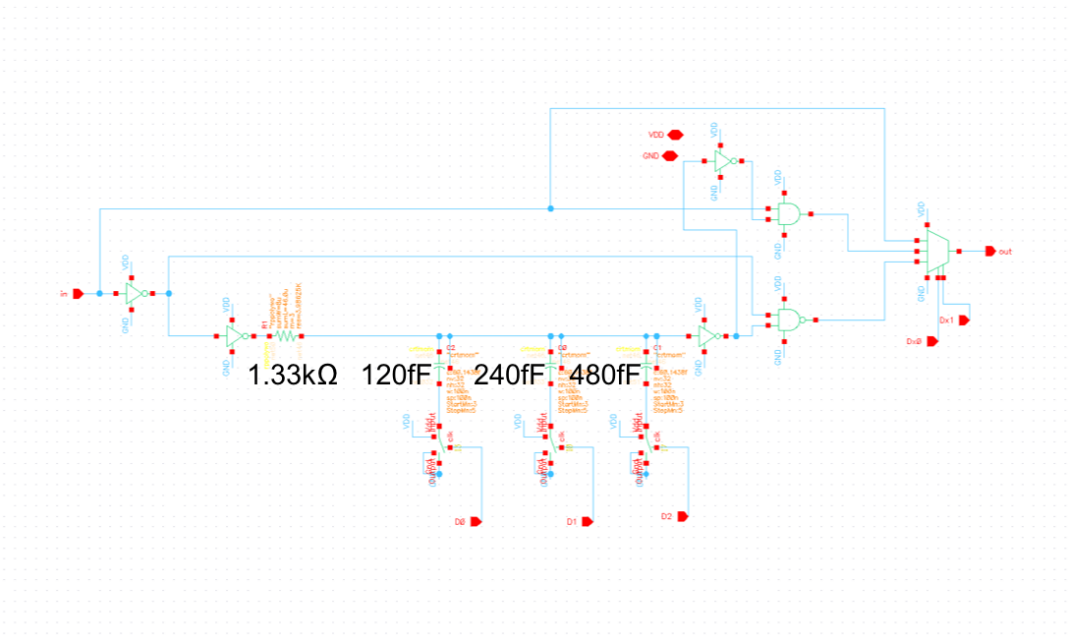

Figure 3.28: Pulse shaper circuit implementation diagram from FM-ExG gateway integrated circuit.

sumption is minimal leading to high system efficiency.

A schematic of the LC voltage-controlled oscillator (VCO) implemented in this work is shown in Figure 3.29. Pulses are generated by switching on and off SW1 and SW2. When SW1 is OFF and SW2 is ON, the LC-VCO powers up and oscillates. When SW1 is ON and SW2 is OFF, current through the oscillator is cutoff and the LC tank is shorted turning off the oscillator. Since this design requires no local oscillator and the circuit is active only during pulse transmission, power consumption is minimized.

The width of each pulse is controlled by the input from the pulse shaper. By setting a pulse width of 3.5ns, a bandwidth of ¿500MHz at 10dB from peak is achieved. The shape of each pulse must be controlled to optimize spectral emissions. A sidelobe rejection of 20dB or greater is required to allow for maximum in-band power while

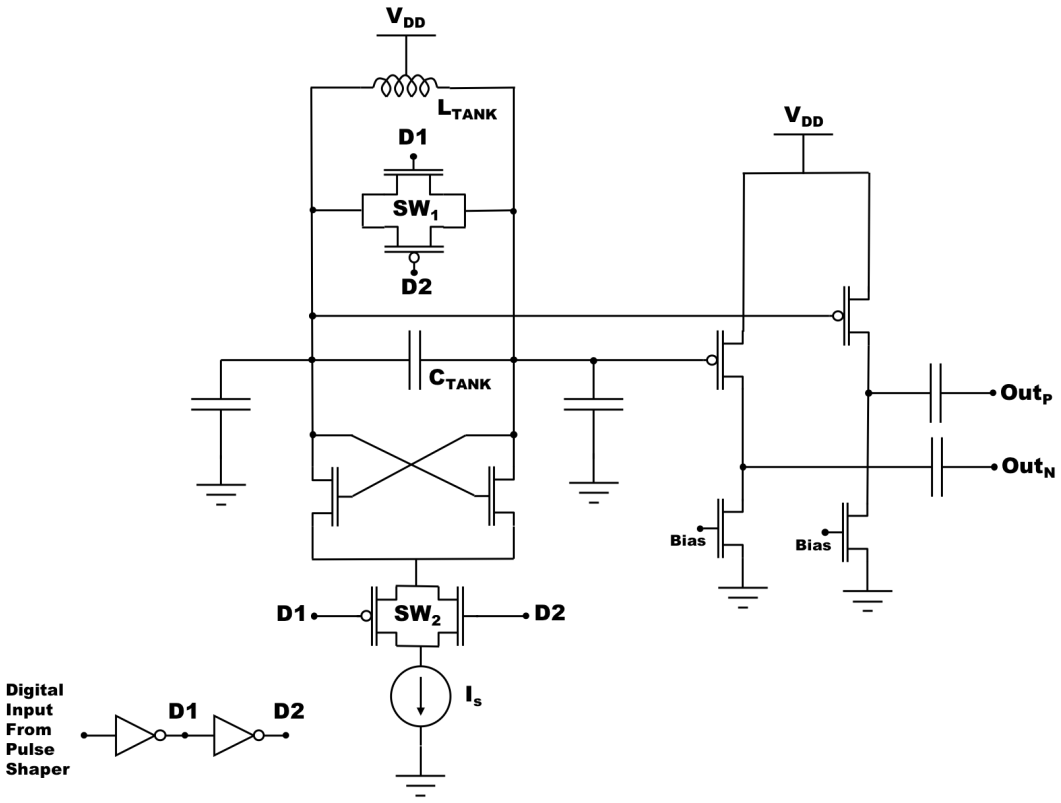

Figure 3.29: Schematic of pulse generator for IR-UWB transmitter on FM-ExG gateway integrated circuit.

still meeting the FCC UWB outdoor spectral mask. A triangle shaped pulse with approximately symmetric rise and fall times will accomplish this goal and is achieved by controlling the rise and fall time of the LC-VCO. As a pulse begins, the oscillation increases in amplitude with a rise time governed by the open loop gain, the tank capacitance including parasitics and the tank loss resistance. A pulse is completed by shutting off the LC-VCO before it reaches steady state and allowing the output to fall back to zero amplitude. The fall time is determined by the tank capacitance and the overall tank equivalent resistance in the off state. The rise time is optimized during the design through selection of I_S which controls the open loop gain. The fall time is independently

controlled through the sizing of SW1 which determines tank resistance in the off state.

Gateway SAR ADC

In this IR-UWB based digital transmitter, we adopt the early reset merged capacitor switching algorithm (EMCS) in our SAR ADC to maximize the energy efficiency while improving the linearity [37]. A EMCS SAR ADC is a ternary SAR ADC essentially except the voltage switching for the current and previous cycle bits will depend on both cycles status. In a EMCS SAR ADC, if the current cycle bit is the same as its previous cycle bit, then the current cycle capacitor voltage will be set to the same as the previous cycle capacitor voltage; If the current cycle bit is complementary to its previous cycle bit, the previous cycle capacitor voltage will be reset to the common mode voltage and the current capacitor voltage will be switched to the opposite polarity. According to [37], the EMCS techniques provide a 12.5 percent switching power efficiency improvement than the MCS technique for a 12b SAR ADC and the worst case code capacitor matching requirement is reduced by a factor of 2 such that the differential nonlinearity(DNL) and integral nonlinearity (INL) is also reduced by a factor of 2 on average. Figure 3.30 is a schematic representation of the EMCS SAR ADC.

3.4.3 Measurement Results

The IR-UWB transmitter was implemented in a 1.2V 65nm CMOS technology and the chip size is 1 mm by 1mm. Figure 3.31 shows the measured output pulse and spectrum. The pulse exhibits a diamond shape (triangular envelope) which results in

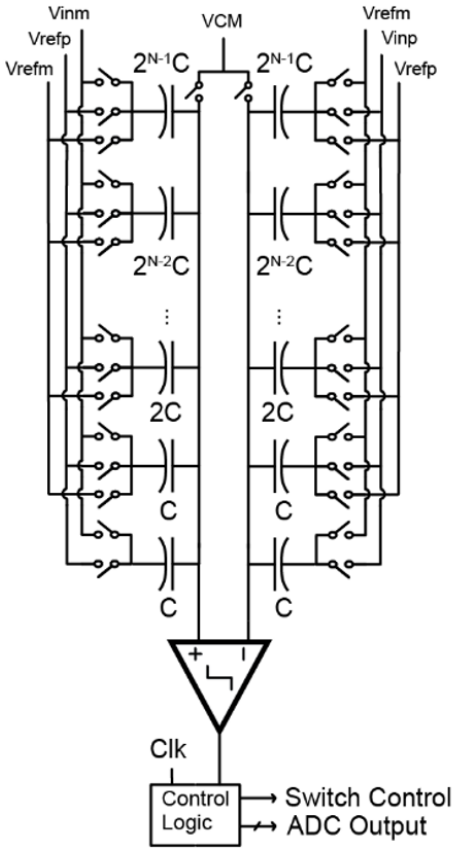

Figure 3.30: Schematic of EMCS SAR ADC on FM-ExG gateway integrated circuit.

more than 20dB of side lobe suppression as indicated in the PSD. This allows the design to meet the FCC outdoor spectral mask with a peak power at the FCC limit of -41.3dBm/MHz. Under these conditions the peak-to-peak pulse amplitude is measured to be 170mV.The pulse width as set by the system clock and pulse shaper is 3.5ns. This results in a -10dB bandwidth of 560MHz.

The transmitter consumes 1.125mA at 1.2V (excluding output buffers) when operating at 15.36Mbit/sec. This translates to a power consumption of 11pJ/pulse or 88pJ/bit (8 pulses per bit). The power consumption of the output buffers range from

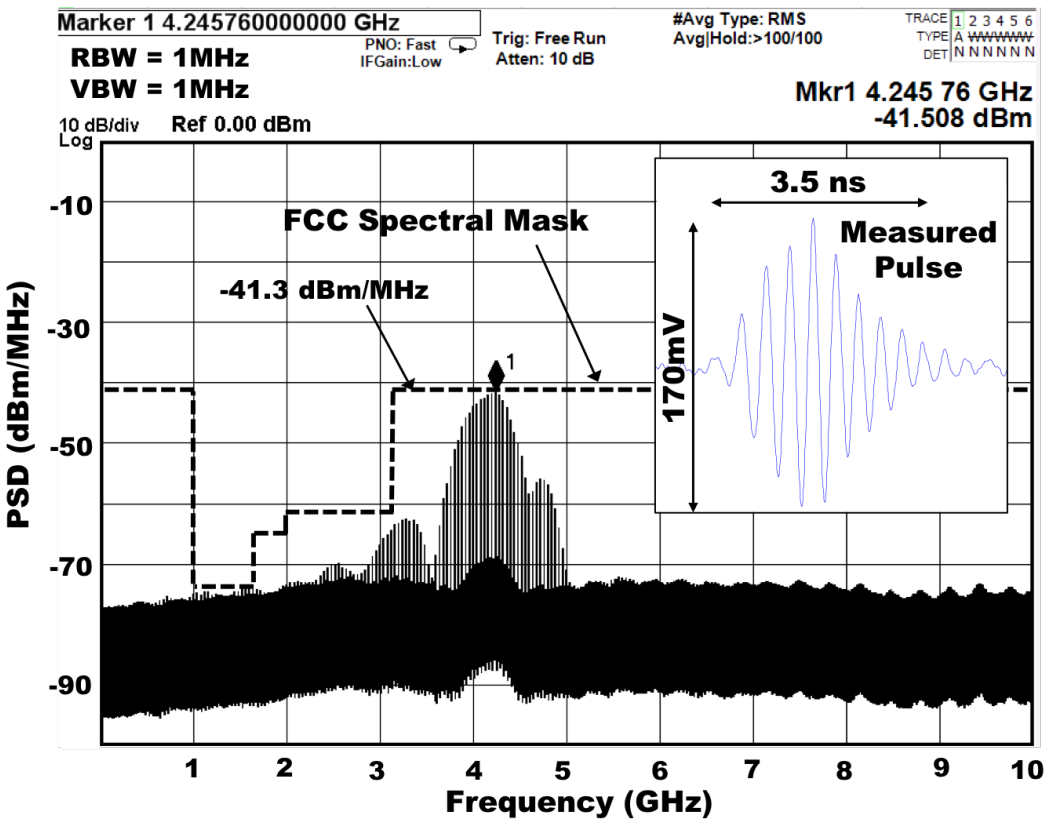

Figure 3.31: Measured FM-ExG Gateway IC UWB PSD showing FCC mask compliance and time domain pulse (inset).

2-20 mA which can be controlled by adjusting the bias via off chip controls. Table 3.2 summarizes the measured performance of the implemented UWB transmitter IC.

3.5 Comparison with Previous Works

The active electrode integrated circuits and gateway integrated circuit were both fabricated in a 65nm process. The active electrodes expend 212μW per channel, and the 12b SAR ADC in the gateway IC consumes 190μW at 1.28MS/s. Both chips operate at 1.2V. The UWB TX consumes 11pJ/pulse, and eight pulses are transmitted per bit

Table 3.2: Measured metrics for the FM-ExG gateway integrated circuit.

Parameters	**Measured Result**
Sub-band Center Frequency	4.2GHz
Bandwidth	560MHz
Peak power spectral density (PSD)	-41.5dBm/MHz
Sidelobe Suppression	> 20dB
Output (Vpp)	170mV
Pulse Duration	3.5ns
Energy Per Pulse	11pJ (excluding output buffers)
Vdd	1.2V
Data Rate	15.36Mbit/sec
Chip Size	1mm x 1mm
Modulation	OOK

for a total energy cost of 88pJ/b. Achieving 101dB SNR operation, each FM channel occupies 50kHz, and with 50kHz of guard band between channels, 12 total channels are supported in the currently developed FM-ExG system. Addition of more channels is possible simply by increasing the system's SAR sampling rate. Refer to Table 3.3 for a direct comparison of the distributed multi-channel FM-ADC biopotential acquisition system with recently published works. Note that in for all references in the table, 88pJ/b energy from the UWB TX is assumed when calculating wireless transmission power. This assumption is made in order to normalize TX performance across references. Die photos of both the active electrode IC and the gateway IC are presented in Figure 3.32.

Table 3.3: Comparison of FM-ExG work with prior biopotential acquisition literature.

Design	Helleputte, JSSC 2015	Rieger, TCAS-I 2018	O'Leary, ISSCC 2018	Schönle, JSSC 2018	Xu, ISSCC 2014	This Work
Active Electrode?	**No**				**Yes**	
Process [nm]	180	180	130	130	180	**65**
IC Active Area [mm^2]	49	0.06	7.6	20.8	15.8	**1**
Electrode Bus Drive Type	-	-	-	-	Digital I2C	**FDM via Tuned Amplifier**
Channels / Chip	5	3	32	9	1	**1**
IRN [uVrms] (BW)	0.61 (150Hz)	0.67 (100Hz)	1.6 (500Hz)	1.21 (150Hz)	0.65 (100Hz)	**0.99 (250Hz) 0.63 (100Hz)**
Acquisition Bandwidth [Hz]	250	7000	500	4000	100	**250**
Usable DR at Input [dB]	~83 (13.5-bit)	~50 (8-bit)	70	~83 (13.5-bit)	~74 (12-bit)	**101**
Output Bit Rate per Channel [Hz]	32000	56000	1000000	112000	2400	**1280000**
Acquisition Power per Channel [µW]	56	96.7	1.26	285	104.4	**228**
Calculated Wireless TX Power* per Channel [µW]	2.82	4.93	88	9.86	0.21	**112.6**
Total Power per Channel [µW]	58.82	101.63	89.26	294.86	104.61	**340.6**
FOM = Usable DR [dB] + 10 log10(BW [Hz] / Total Power per Channel [W])	149.3	128.4	137.5	154.3	133.8	**159.7**

*Calculated using 88 pJ/bit at digital output bit rate

3.6 Conclusion

The digitization of multiple channels via a single low-power SAR ADC cements the power advantage of the proposed system, where each channel achieves 101dB SNR, yet with an aggregate power consumption of only 228µW/channel without the UWB TX, and 340µW/channel with. Despite the increased bit rate per channel due to FM-based oversampling and the corresponding extra energy required from the UWB TX to transmit at a higher data rate, the power efficiency and DR of the system reflected in the Schreier FoM exceeds that of prior-art active electrode systems that include the power of electrode-to-gateway drivers, and also exceeds conventional AFE arrays that do not. The distributed multi-channel FM-ADC approach presented herein is applicable to many different sensing modalities, and particularly useful in application cases that require multiple sensors co-located and low total system power consumption.

Chapter 3 expands upon the following publication: J. Warchall, P. Theilmann, Y.

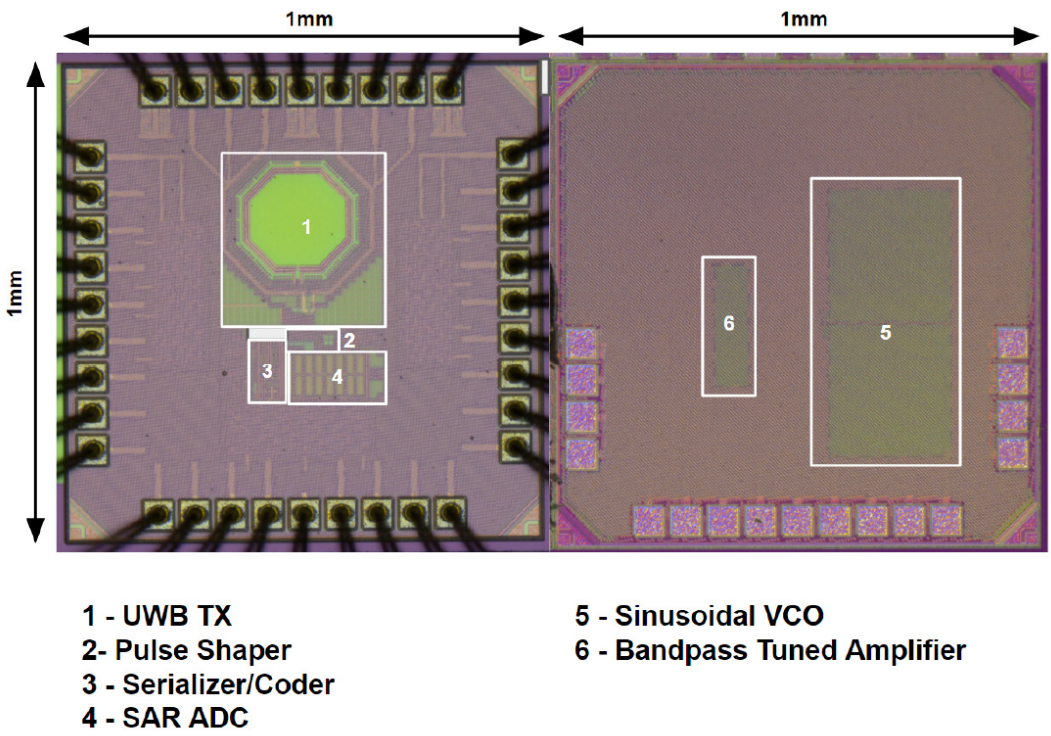

Figure 3.32: Die photographs of the two chips in the FM-ExG system.

Ouyang, H. Garudadri, P.P. Mercier, ”22.2 A Rugged Wearable Modular ExG Platform Employing a Distributed Scalable Multi-Channel FM-ADC Achieving 101dB Input Dynamic Range and Motion-Artifact Resilience,” *2019 IEEE International Solid- State Circuits Conference - (ISSCC)*, San Francisco, CA, 2019, pp. 362-363. The dissertation author is the primary investigator and author of the work in these papers.

Chapter 4

MATLAB Analysis and Optimization of the FM-ADC

4.1 Introduction

The chapters thus far in this thesis have dealt primarily with the design and application of FM-ADC systems to specific tasks, and while many parameters in their design are based on calculation presented in those chapters, a couple were chosen out of convenience at design-time or chosen via trial-and-error processes which settled on near-optimal values for the task at hand.

This section focuses on the two most important designer-selectable parameters in FM-ADC design that the previous chapters did not address how to choose. Namely, these are the FM carrier wave's frequency, also known as the FM center frequency, and the number of bits in the system's quantizer.

In selecting these parameters, we must provide a definition of good system performance. For this, we refer to the Schreier figure of merit (FOM) which is used to

evaluate ADC performance [30]:

$$FOM_{Schreier} = SNR + 10log_{10}(Bandwidth/Power) \qquad (1)$$

This metric not only captures the resolution that an ADC design achieves, but also reflects the power efficiency with which it achieves that resolution over a certain bandwidth. Comparison of various ADC designs via this FOM is considered fair as it accounts for differences in input bandwidth and resolution targets between ADCs made for different tasks while evaluating their relative power efficiency. We will therefore strive in this chapter to replace terms in this equation with their FM-ADC specific counterparts and use it as our system optimization variable.

4.2 System-level Trade-offs

As we detailed in Chapter 2, by keeping the carrier frequency low, power is saved in the VCO used for FM, since oscillator power is proportional to oscillation frequency when other oscillator properties are held constant. A lower carrier frequency would also enable a lower sampling rate in the quantizer, were it sampling the carriers while satisfying the Nyquist Criterion. However, our system employs bandpass sampling in the quantizer to sample at the Nyquist rate for the aggregate FM spectrum bandwidth, not the Nyquist rate for the carriers' absolute frequencies. The direct trade-off between quantizer power and carrier frequency is therefore decoupled.

The capacitance versus control voltage relationship of the on-chip varactor diodes used for VCO frequency control is quite nonlinear; it is ultimately this nonlinear property of the varactor diodes used for VCO tuning which influences our selection of system carrier frequency. At lower VCO frequencies, to cover the same FM bandwidth, the VCO must be pulled over a larger range relative to to its oscillation frequency. This means that a larger percentage of the employed capacitance must be changed, and therefore the varactor control voltage must cover a larger operating range to realize this. By going to higher and higher carrier frequencies, an equal FM bandwidth can be covered by a smaller percentage change in the tank's capacitance, so a smaller and more locally linear region of C-to-V curve is employed.

Put another way, higher FM carrier frequencies must be used to realize larger FM bandwidth for the same linearity. As FM bandwidth gets larger, system SNR increases per

$$SNR_{FM} = 10log_{10}(3D^2(D+1)) + CNR \qquad (2)$$

from [3] where D is the bandwidth expansion ratio, Δf / W, where Δf is the maximum frequency deviation of the FM carrier and W is the message signal's bandwidth (constant in this analysis). Also, the sampling rate requirement of the quantizer increases as FM bandwidth increases because of the nature of subsampling in the system. Power in the quantizer increases linearly with sample rate according to

$$Constant\ \ K_{Thermal} = Power/(2^{2*ENOB} * f_s) \qquad (3)$$

from [30]. Furthermore, according to [38], as the tuning bandwidth of a VCO (also, in our case, the FM bandwidth or quantizer sampling rate) increases and all other parameters of the VCO are held constant, its phase noise will increase logarithmically. Referring back to Figure 3.6 in Chapter 3, we notice a linear relationship between phase noise in dB and system SNR in dB. This means a linear increase in carrier frequency has a logarithmic (dB-linear) effect on phase noise degradation of system SNR.

Therefore, due to the couplings among variables just mentioned, we have the following trade-off: Increase carrier frequency and one term contributing to system SNR (FM coding gain) increases, another term detracting from system SNR (phase noise) increases, and system power increases due to increased VCO tank oscillation rate and increased quantizer bandwidth requirements. We will take this tradeoff into account in Section 4.3.

Furthermore, from (2), increasing the number of bits (ENOB) in the quantizer increases CNR and therefore system SNR directly. From (3), as quantizer ENOB increases, power will increase geometrically. These tradeoffs will be further taken into account in Section 4.3.

4.3 Optimization of FM Carrier Frequency and Number of Bits in System Quantizer

In the previous two sections, the tradeoffs between FM carrier frequency (here called F) and the number of bits in the system quantizer (here called N) were explained verbally. The mathematical combination of these tradeoffs will allow us to inspect visually their effect on FOM. We combine equations (1), (2), and (3) and make the approximations that CNR = 6N, $3D^2(D+1) = 3D^3$ in (2), and FM message bandwidth = 1 to yield the following equation:

$$FOM_{Schreier} = 6N + 10log_{10}(3F^3) + 10log_{10}(1/(K_{THERMAL}F2^{2N})) - K_{PN}F \qquad (4)$$

Here, K_{PN} serves as a constant reflecting the fact that linear increases in carrier frequency cause logarithmic degradation in SNR, which we showed in Section 4.2. It also serves as a scale constant that adjusts for the fact that we used FM carrier frequency as a proxy for FM bandwidth according to the relationships described in Section 4.2. $K_{THERMAL}$ is similarly constant and comes directly from (3).

Plugging in the empirical data in Table 2.2 into (4), we find a reasonable value for K_{PN} to be 10^{-6}. Using this value, we plot the Schreier FOM versus N and F in Figure 4.1.

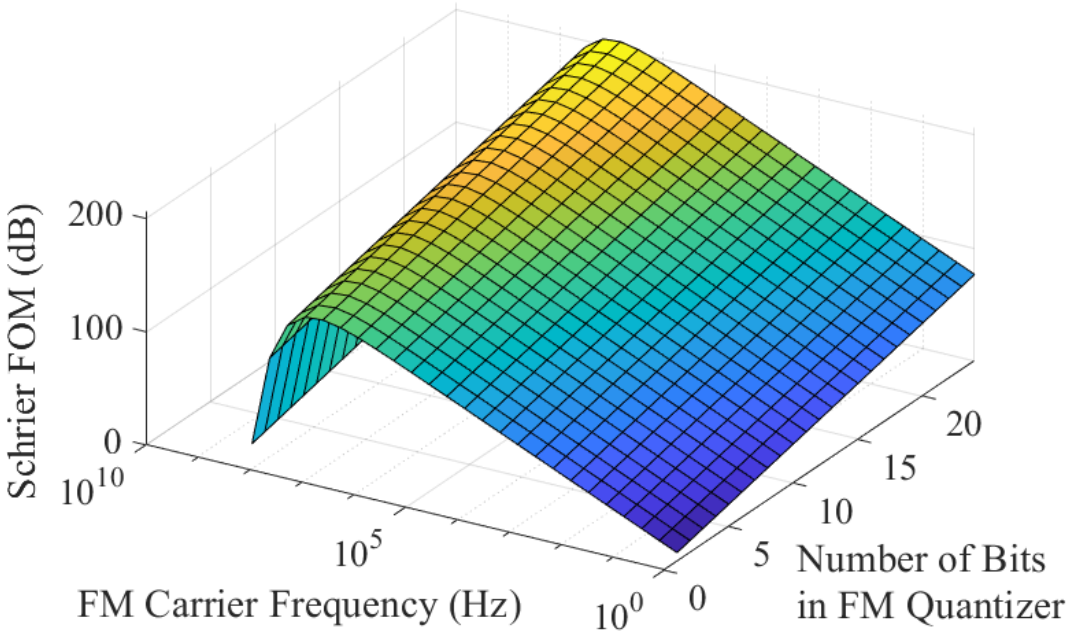

Figure 4.1: FM-ADC system Schreier FOM versus FM carrier frequency and number of bits in FM quantizer.

4.4 Conclusion

We can draw two useful pieces of knowledge from Figure 4.1: First, there exists an optimal FM carrier frequency to use for a specific VCO implementation (provided we would like to maintain a certain level of system linearity); remember, K_{PN} will vary depending on which oscillator is used and was determined from our empirical data. Our design settled at around 15 MHz while the optimal according to this graph is around 6 MHz, so our trial-and-error design process was able to get within an order of magnitude of the optimal value. Second, if absolute maximum figure of merit is your design goal, the internal quantizer in the FM-ADC should be made as high-resolution as possible. Of course, this design goal would rarely fit application requirements, since increases in

quantizer ENOB scale a large fraction of the system power geometrically. In practical use, quantizer ENOB will be chosen to fit application resolution and power consumption requirements. We see that, once a VCO is designed, quantizer ENOB is essentially the only free knob left for the designer to turn since the specific VCO employed will dictate optimal FM carrier frequency and, therefore, quantizer sample rate.

Chapter 5

Conclusion

In this thesis we have described a type of voltage-controlled oscillator (VCO) based analog to digital converter (ADC) called the FM-ADC. We have shown that the use of a sinusoidal-output VCO affords the FM-ADC two advantages: First, it can achieve higher input dynamic range than traditional VCO ADCs for the same levels of power consumption, as was shown in Chapter 2. Second, it can be used in a scheme with multiple input signals all recorded simultaneously, a scheme we call the distributed multi-channel FM-ADC. We showed in Chapter 3 that this multiple-input scheme affords some unique advantages in the realm of biopotential signal acquisition. In Chapter 4 we briefly touched on ways to optimize the design choices made when implementing an FM-ADC system, regardless of whether it has a single channel of input signal or multiple channels.

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