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Status of the CCD development for the Dark Energy Spectroscopic Instrument

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ABSTRACT: We describe improvements in CCD performance that have been achieved on $4k \times 4k$, $(15 \mu\text{m})^2$ -pixel, fully depleted CCDs for the Dark Energy Spectroscopic Instrument (DESI) [1]. With respect to our previous work on CCDs for the Dark Energy Camera and the Baryon Oscillation Spectroscopic Survey, our goals for the DESI CCD development were to improve read noise and quantum efficiency, improve the astrometric precision, and decrease pixel-size variations. We report experimental results on recently fabricated CCDs to be used in DESI.

KEYWORDS: Photon detectors for UV, visible and IR photons (solid-state); Photon detectors for UV, visible and IR photons (solid-state) (PIN diodes, APDs, Si-PMTs, G-APDs, CCDs, EBCCDs, EMCCDs etc); Solid state detectors

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1 Introduction

We previously reported our strategies to improve the performance of fully depleted CCDs for the Dark Energy Spectroscopic Instrument (DESI) [2]. In particular, our desire was to realize CCDs for DESI that exceeded the capabilities of prior generations of fully depleted CCDs developed in our group for the Dark Energy Camera (DECam) [3, 4], and the Baryon Oscillation Spectroscopic Survey (BOSS) [5–7]. At the time of that publication we had not produced actual DESI CCDs, but rather had explored some of the pertinent concepts on smaller, prototype devices [2].

In this work we present experimental results on 250 μm -thick, $4\text{k} \times 4\text{k}$, $(15 \mu\text{m})^2$ -pixel CCDs that have been produced specifically for DESI. The areas targeted for improvement are read noise, quantum efficiency (QE), and low-level effects that impact the use of these CCDs in precision astronomical measurements. The latter include effects due to resistivity variations in the starting silicon material, i.e. “tree rings” [8], and pixel-size variations arising from the methods used to produce the photomasks that are used in the CCD production process.

2 CCD fabrication and packaging

The majority of the CCD fabrication is done at Teledyne DALSA Semiconductor. Figure 1 shows a photograph of a DESI wafer that includes the $4\text{k} \times 4\text{k}$ DESI CCD and two, $4\text{k} \times 2\text{k}$ CCDs that share the same features of the DESI CCD. The CCD fabrication process uses three layers of polycrystalline silicon for the three-phase devices, and requires 13 photomasks. The CCD processing at Teledyne DALSA Semiconductor is performed on standard thickness wafers, i.e. 650–675 μm thick, in order to maintain compatibility with the fabrication equipment in the DALSA foundry.

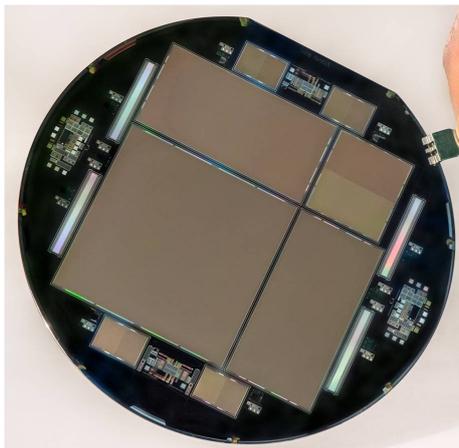


Figure 1. Photograph of a 150 mm diameter DESI wafer. The large CCD on the lower left is the DESI CCD. The format is 4114 columns by 4128 rows. The pixel size is $(15 \mu\text{m})^2$. The wafer layout also contains two CCDs with 4114 columns and 2040 rows with a pixel size of $(15 \mu\text{m})^2$. The CCDs feature 4-corner readout.

Back-illuminated CCDs are produced by terminating the processing at DALSA after ten of the photomask steps are completed. The wafers are then thinned at a commercial vendor to the DESI thickness of $250 \mu\text{m}$, and the remainder of the processing is performed at the Lawrence Berkeley National Laboratory (LBNL) MicroSystems Laboratory [9]. The lot size at DALSA is 24 wafers, and the lots are split into smaller, 5 wafer batches, for processing at LBNL.

Once the wafers are completed at LBNL, the DESI CCDs are tested in a probe station at -65°C to screen out defective devices [9]. To date we have completed the processing of about 70 wafers, and the yield after the screening at -65°C is about 40–45%. The CCDs that pass the initial screening process are then diced, and the die are sent to Fermi National Accelerator Laboratory (FNAL) for packaging and detailed testing. CCD testing is also performed at LBNL on select CCDs. Considering the fabrication and packaging yields, we plan to fabricate a total of approximately 110 DESI wafers in order to provide the 20 CCDs plus spares required for the experiment [1, 2].

3 Read-noise and quantum-efficiency improvements

In the following sections we describe the improvements to the read noise and QE that have been achieved on the DESI CCDs. The latter is due to the addition of an improved anti-reflection (AR) coating material that allows for more degrees of freedom in the optical designs. The noise improvements are due to a smaller floating-diffusion area and output-transistor width, and together these result in lower noise than what was observed with the DECam and BOSS CCDs.

3.1 Read-noise improvements

We have previously reported the development of low-noise amplifier structures [10, 11]. In that work we described efforts at Teledyne DALSA Semiconductor to develop a buried-contact structure that consists of a direct connection between the output-transistor, polycrystalline-silicon gate electrode and the floating diffusion. Figure 2 shows both an optical photograph of a buried-contact amplifier as well as a cross-sectional scanning-electron-microscope (SEM) image taken at EAG

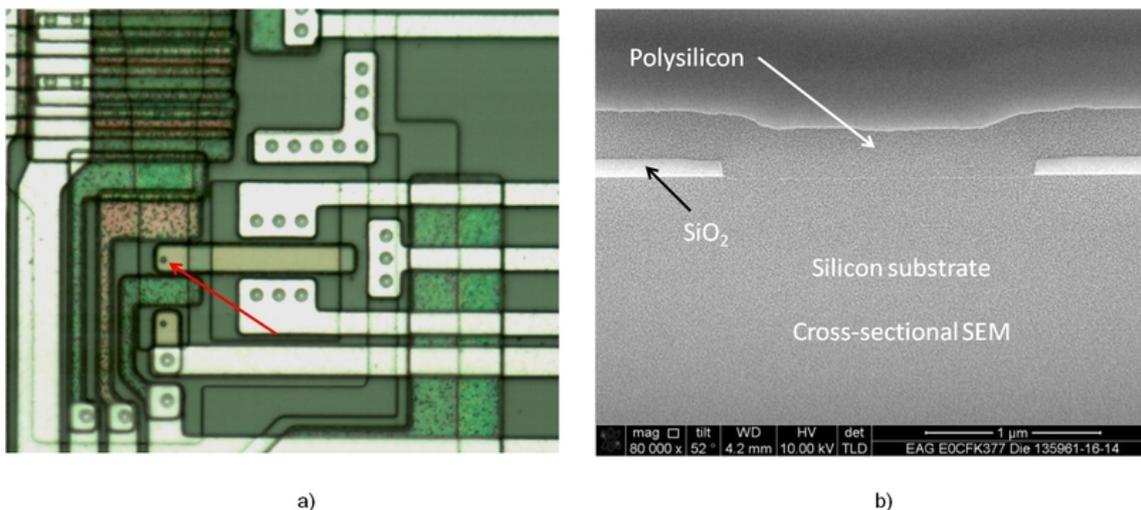


Figure 2. a) Photograph of a buried-contact amplifier. The arrow points to the buried contact where a direct connection is made between the output transistor polycrystalline-silicon gate electrode and the floating diffusion. b) Cross-sectional SEM image of the buried contact region of a). The cross section was taken along a horizontal line passing through the circular feature pointed to by the arrow in a). The ion-implanted, floating-diffusion region is between the SiO₂ edges and in the silicon. The SEM work was done at EAG Laboratories [12].

Laboratories [12]. The direct contact to the floating diffusion allows for a minimum-sized, floating-diffusion area. This is in contrast to the conventional floating-diffusion contact that requires a larger implanted region with the additional area needed to accommodate the metal contact and its spacing to the edge of the implanted region.

The area required for a metal connection to the polycrystalline-silicon gate is also eliminated, and the net effect is a reduction in the capacitance at the floating diffusion with a concurrent reduction in the read noise. We also reported an investigation of the effect of the transistor width on the read noise [10, 11]. Based on this work we were able to reduce the output-transistor width by about a factor of two thus further reducing the capacitance at the floating diffusion.

Prior to the work reported here, we fabricated buried-contact amplifiers on three research and development lots at DALSA in order to gain confidence in the reproducibility of the process. Based on those efforts, we implemented the buried-contact amplifiers on both the 4k × 4k DESI CCD and the 4k × 2k CCDs that are included on the same wafer layout shown in figure 1. Figure 3 a) shows a comparison of the read noise measured on DESI CCDs with those of CCDs for the Mosaic3 camera [13]. The latter CCDs are of the BOSS design with the older-style amplifiers. The Mosaic3 CCDs are unique in that they were fabricated on very high-resistivity silicon substrates. This allows for the fully depleted operation of 500 μm-thick substrates, making these the thickest CCDs presently in use on an astronomical telescope. The median read noise from figure 3 a) measured on these CCDs is 3.3 e⁻ rms with a standard deviation of 0.5 e⁻. The noise was measured at an integration time of 5.2 μs corresponding to a readout rate of 70 kpixels/sec. The operating temperature was -140°C.

Also shown in figure 3 a) is the read noise measured on both 4k × 4k and 4k × 2k CCDs taken from the pre-production lot of DESI wafers. The median read noise in this case is 2.1 e⁻ with a

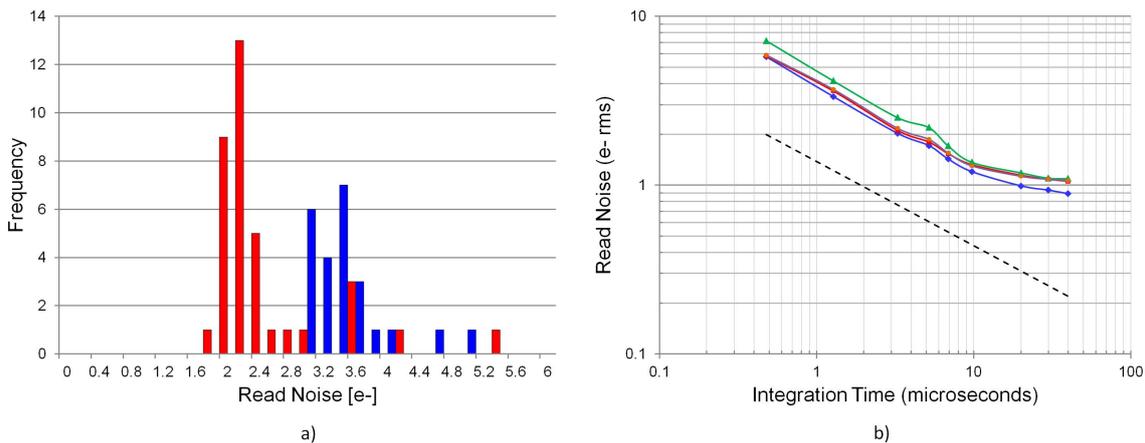


Figure 3. a) Histogram of read noise comparing pre-production DESI CCDs in red versus Mosaic3 CCDs in blue. The DESI results include results from $4k \times 4k$ and $4k \times 2k$ CCDs, and those CCDs were $250 \mu\text{m}$ thick. The Mosaic3 CCDs were $500 \mu\text{m}$ thick. The measurements were done at -140°C and at an integration time of $5.2 \mu\text{s}$ and pixel readout rate of 70 kpixels/sec . b) Read noise for the four amplifiers on a DESI $4k \times 4k$ versus integration time. The dashed line has an inverse square root of time dependence. The measurements were done at -140°C .

standard deviation of $0.7 e^-$, or an improvement of about $1 e^-$ rms for the buried-contact amplifier when compared to the Mosaic3 CCDs at the same integration time. It should be noted that for the case of the DESI CCDs in figure 3 a), the biasing conditions were not consistent in all cases as we had not yet adopted a standard biasing condition during the early phase of the testing. Nonetheless, the noise improvement for the buried-contact amplifiers is evident in figure 3 a). There are outlier amplifiers with higher than desired noise in figure 3 a), and we noticed a systematic issue with the pre-production lot where one amplifier location showed excess noise about half the time and especially at long integration times. We have been unable to ascertain the source of the excess noise, and we have not observed it on CCDs produced in the subsequent three production lots.

Figure 3 b) shows the read noise for the four amplifiers on a DESI $4k \times 4k$ CCD from the first of the production lots. The substrate-bias voltage was 50 V and the operating temperature was -140°C . The noise at $5.2 \mu\text{s}$ is consistent with figure 3 a) from the pre-production lot, and the noise level is about $1 e^-$ rms at long integration times. The full-well capacity measured on DESI CCDs is about $90\text{--}120 \text{ ke}^-$ depending on the output-transistor biasing, with the lower value corresponding to a power supply and reset voltage combination of -25 V and -9 V , respectively. The larger full-well value corresponds to bias conditions of -22 V and -12.5 V . The $-25/-9 \text{ V}$ combination results in more voltage dropped across the transistor, and generally lower noise [10]. This behavior is consistent with a full well limited not by the pixel but by the output-amplifier voltage swing. The results shown in figure 3 were measured on an Astronomical Research Cameras, Inc. controller.

3.2 Quantum-efficiency improvements

The DESI experiment includes three wavelength ranges of interest. The CCDs described here are to be used in the red band from 566 to 772 nm and the near-infrared band from 747 to 980 nm [1]. Our efforts to improve CCD QE have emphasized the investigations of new materials in the AR coating

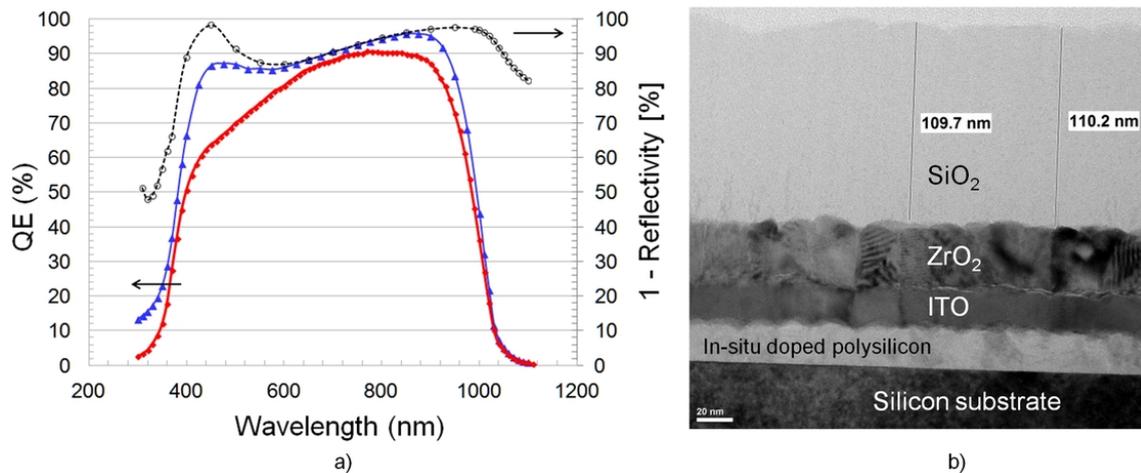


Figure 4. a) Measured QE versus wavelength. The data shown in blue were taken on a preproduction-lot DESI $4k \times 4k$ CCD at an operating temperature of -135°C and with the three-layer AR coating described in the text. The ISDP thickness was nominally 10 nm. The data shown in red are for a CCD at -140°C with the two-layer ITO/SiO₂ AR coating and an ISDP thickness of nominally 25 nm [4]. Both CCDs are $250 \mu\text{m}$ thick. b) A cross-sectional TEM image showing the AR-coating stack consisting of nominally 25 nm of ISDP, 20 nm of ITO, 38 nm of ZrO₂, and 106 nm of SiO₂. The sample used for the TEM study was a DESI CCD from the first production lot. The numerical values shown denote the measured SiO₂ thickness. The TEM work was done at EAG Laboratories [12].

stack. Our previous AR coating consisted of indium tin oxide (ITO) and SiO₂ [4]. This coating suffered from the fact that the ITO was absorptive and had a refractive index that decreased with increasing wavelength [2]. We explored various high-index materials, and determined that ZrO₂ had desirable properties for DESI CCDs that must be sensitive at long wavelengths where much of the DESI science is focused [14]. In particular, we have incorporated a three-layer coating on the DESI CCDs that consists of a thin, i.e. 20 nm thick, ITO layer that is capped with ZrO₂ and SiO₂. The thin ITO layer is included to maintain the same interface to the silicon substrate as has been used in previous CCDs developed at LBNL. This is discussed in more detail below.

Figure 4 a) shows measured QE on a pre-production DESI CCD that has an AR coating stack consisting of nominally 20 nm ITO, 38 nm ZrO₂, and 106 nm of SiO₂. Also shown in figure 4 a) is the measured $1 - R$ where R is the reflectivity. $1 - R$ is a figure of merit for AR coatings in CCDs since that is the maximum QE possible assuming all incident light that is not reflected is absorbed in the active volume of the CCD. Deviations from $1 - R$ indicate absorption in the AR coatings or back-side contact materials, or transparency of the CCD at long wavelengths. The QE of a CCD with the two-layer ITO/SiO₂ coating is also shown in figure 4 a). As can be seen, the QE improvement with the three-layer coating including ZrO₂ is significant.

At blue wavelengths in figure 4 a) the QE is less than $1 - R$ due to absorption primarily in the 10 nm-thick, in-situ doped (phosphorus) polycrystalline-silicon layer (ISDP) that forms the heavily-doped, back-side contact of the CCD [4]. The pre-production CCDs used 10 nm-thick ISDP layers. This has been increased to 25 nm in production devices because of yield concerns regarding back-side defects that could be exacerbated with the thinner ISDP layers [6, 15].

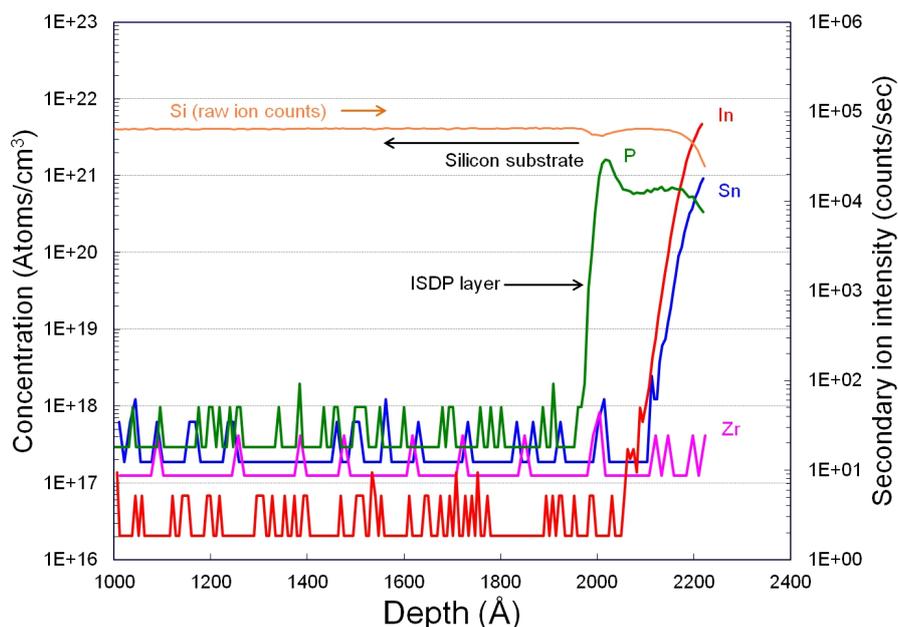


Figure 5. SIMS depth profile of the AR coating stack used in the DESI CCDs. The profile is taken on a sample that is thinned from the side of the CCD containing the CCD circuitry. The region to the left of the phosphorus profile labeled P in the plot is the silicon substrate. Also shown are concentrations for In, Sn, and Zr. The silicon values are in counts/sec. The Zr was not observed above the detection limit in either the ISDP layer or the silicon substrate.

In the mid-band wavelength region of figure 4 a) the QE is nearly equal to $1 - R$, indicating that nearly 100% of the photons that are not reflected from the CCD are detected as useful signal. This demonstrates that the ZrO_2 coating is performing as expected. At the longest wavelengths the absorption length is exceeding the CCD thickness, and the CCD is becoming transparent.

As mentioned previously, the 20 nm-thick ITO layer was included in the AR-coating stack in order to maintain the same AR coating-silicon interface as used previously. In order to study possible reliability problems associated with the introduction of ZrO_2 , we had cross-sectional transmission-electron-microscope (TEM) imaging and secondary ion mass spectroscopy (SIMS) analysis performed at EAG Laboratories [12] in order to verify the integrity of the AR coating. Figure 4 b) shows the cross-sectional TEM image of a portion of the back side of a DESI wafer. No anomalies are present in the TEM image of the AR coating stack, and the film thickness of the various layers is reasonably uniform. The sample used for the TEM images shown in figure 4 b) was a CCD from the first production lot where the ISDP thickness was nominally 25 nm.

Figure 5 shows the SIMS analysis of the AR coating stack. The sample came from the same wafer used for the TEM study shown previously in figure 4 b). The objective of this work was to check for possible diffusion of metal impurities, especially Zr, from the AR coatings into the silicon where the metals could act as dark-current generation centers. For this work, the sample was thinned from the side containing the CCD circuitry. The thinning was stopped just before the back-side layers were encountered. The SIMS analysis proceeded from the thinned silicon substrate, through

the ISDP layer, and partially through the ITO layer. This avoids potentially false readings that could occur if the incident SIMS ion beam were incident from the back side of the wafer. Lateral extension of the sputtered area during the measurement could yield SIMS signals from the metal layers that would mimic diffusion into the substrate.

The phosphorus profile indicates the ISDP layer. Beyond the ISDP, In and Sn from the ITO are detected. Both of these elements drop rapidly below the detection limit as expected based on prior SIMS analysis of our older AR coating stack. There is also no detection of Zr above the detection limit in the ISDP layer or the silicon substrate, as desired. No degradation of the typical dark current of a few $e^-/\text{pixel-hour}$ at -140°C has been observed with the improved AR coating.

4 “Tree rings” and periodic-mask errors

In the following sections we address our efforts to reduce the lateral electric fields resulting from resistivity variations in the starting silicon. This effect results in errors in astrometric measurements, and in the case of DECam it was shown that the astrometric errors have the same radial variation as the “tree rings” that are discussed in more detail below [16]. We also address pixel size variations that arise from the step-and-repeat methods used in the manufacturing of the photomasks that define the CCD pixels.

4.1 “Tree rings” improvements

Radial resistivity variations in the starting silicon have been shown to result in radial patterns in uniformly illuminated imagers including silicon vidicons [17, 18], CCDs [19, 20], and CMOS image sensors [21]. The resistivity variations arise due to impurity segregation at the spherically-shaped, liquid-solid interface that is present during the crystal growth or float-zone refining steps. The spherically-shaped surface translates into a radial resistivity pattern when the silicon ingot is sawn in a direction perpendicular to the growth surface in order to form wafers from the ingot [22]. The term “tree rings” to describe this situation dates back to at least 1997 [23]. The effects can be exacerbated in thick, fully depleted CCDs due to the large aspect ratios of these devices [8].

In our initial work on “tree rings” we described a simple model based on the lateral travel distance of photogenerated carriers during the drift time through the substrate [24]. The lateral motion is due to the electric field in the transverse direction that results from the resistivity variations. Given that the field is due to the ionized dopants in the fully depleted substrate, we anticipated that one method to minimize the lateral motion would be to reduce the transverse electric field by reducing the doping levels in the silicon substrate [24]. Fortuitously, very high-resistivity silicon from Topsil had become available to us, and in fact was used initially for the Mosaic3 CCDs in order to be able to fully deplete those $500\ \mu\text{m}$ -thick CCDs at a reasonable substrate-bias voltage [13].

Our prior work on DECam used Siltronic silicon with a resistivity that was in most cases in the $4\text{--}6\ \text{k}\Omega\text{-cm}$ (n-type) resistivity range. We were able to procure material from Topsil with resistivity exceeding $15\ \text{k}\Omega\text{-cm}$ for the pre-production lot, and values in the $\approx 20\text{--}25\ \text{k}\Omega\text{-cm}$ range in the wafers used to date in the production lots. Figure 6 shows median-filtered images taken under the conditions of uniform illumination at a wavelength of $500\ \text{nm}$ comparing a BOSS CCD fabricated on the Siltronic, $4\text{--}6\ \text{k}\Omega\text{-cm}$ silicon, versus that of a DESI CCD fabricated on the $> 15\ \text{k}\Omega\text{-cm}$, Topsil material. As can be seen qualitatively, the “tree rings” are much less pronounced for the

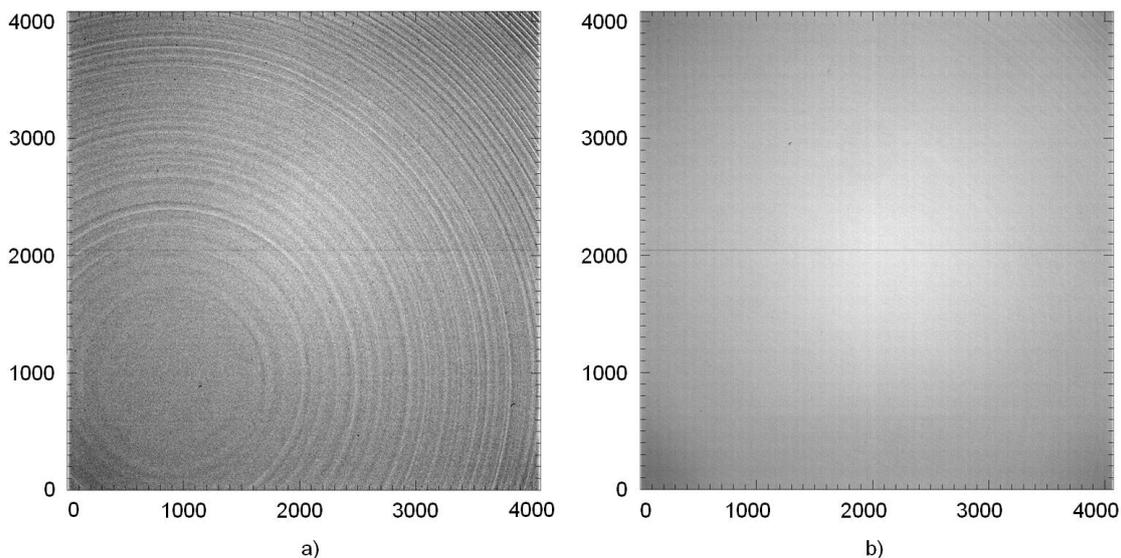


Figure 6. a) Median-filtered image taken with a $250\ \mu\text{m}$ -thick, $4\text{k} \times 4\text{k}$, BOSS CCD at a substrate-bias voltage of 20 V and an operating temperature of -140°C . This CCD was fabricated on $\approx 5\ \text{k}\Omega\text{-cm}$ silicon. b) Median-filtered image taken with a $250\ \mu\text{m}$ -thick, $4\text{k} \times 4\text{k}$, DESI CCD at a substrate-bias voltage of 20 V and an operating temperature of -140°C . This CCD was fabricated on $> 15\ \text{k}\Omega\text{-cm}$ silicon. For both images the illumination wavelength was 500 nm, and 100 images were used to generate the median-filtered versions shown.

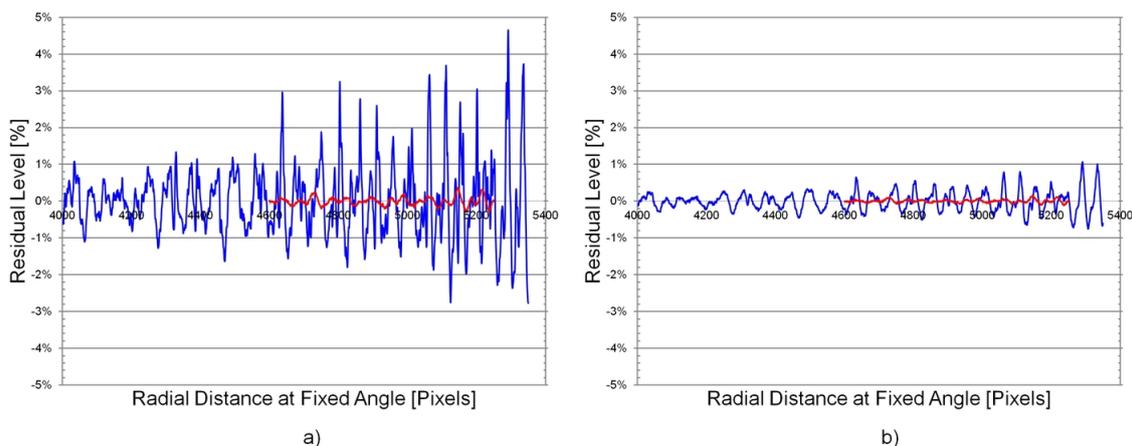


Figure 7. a) Residual-level amplitude versus radial distance calculated from the images shown in figure 6. Data for the $\approx 5\ \text{k}\Omega\text{-cm}$ silicon from figure 6 a) is shown in blue, and the data for the $> 15\ \text{k}\Omega\text{-cm}$ silicon from figure 6 b) is shown in red. The substrate bias voltage was 20 V. b) Residual-level amplitude comparing the same two CCDs as in a) but at a substrate-bias voltage of 50 V.

higher-resistivity silicon. The substrate-bias voltage used to generate the images shown in figure 6 was 20 V in order to enhance the contrast due to the “tree rings”.

Figure 7 shows the calculated “tree-ring” amplitude versus radial distance at substrate-bias voltages of 20 and 50 V for the two CCDs of figure 6. The amplitudes are calculated by averaging 500 rows after the images of figure 6 are converted to polar coordinates [24]. A cubic fit was

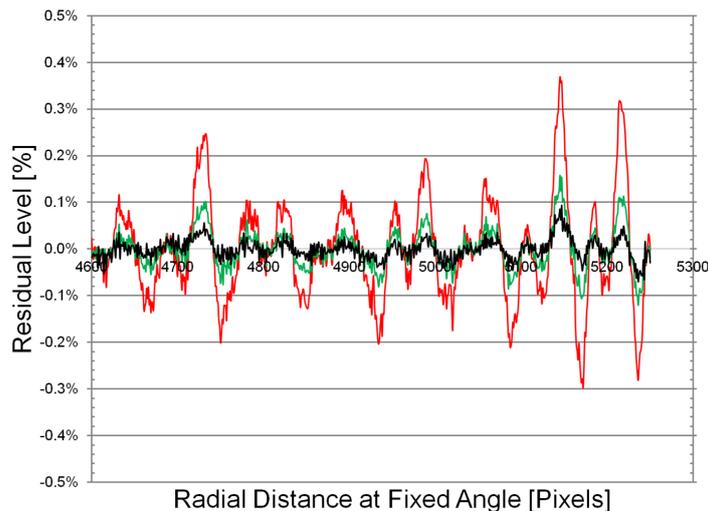


Figure 8. Measured residual-level amplitude versus radial distance calculated for the DESI CCD fabricated on $> 15 \text{ k}\Omega\text{-cm}$ silicon whose image at a substrate-bias voltage of 20 V was shown in figure 6 b). The amplitude is shown for substrate-bias voltages of 20, 50 and 100 V corresponding to the red, green, and black curves, respectively.

subtracted from the averaged, median-filtered flat-field data, and the remaining residual level was normalized by the cubic-fit values. The “tree-ring” amplitudes are as large as a percent for the lower resistivity material at 50 V, and much smaller for the higher-resistivity silicon. The lower amplitudes for the higher-resistivity silicon are shown on an expanded scale in figure 8 that also shows the dependence on substrate-bias voltage. The “tree-ring” amplitude is reduced to approximately 0.1% or less for the CCD fabricated on $> 15 \text{ k}\Omega\text{-cm}$ and operated at a substrate-bias voltage of 50 V or greater. While we attribute the greater than 5-fold reduction in the “tree-ring” amplitude primarily to the use of the much higher-resistivity silicon, it is also likely that improvements in crystal growth and float-zone refining methods also contribute to the improvement [25].

4.2 Pixel-size variations and improvements

Pixel-size variations that are periodic in nature have been reported and attributed to the photomask manufacturing method [26]. We observed a particularly large and periodic variation of about 0.5% in a 16-channel CCD [2], and similar variations were reported for an early prototype CCD for the Large Synoptic Survey Telescope (LSST) [8]. These CCDs had in common that they were both fabricated at Teledyne DALSA Semiconductor. Efforts at DALSA have led to a significant reduction in this effect for both DESI and LSST CCDs, as described below.

Figure 9 a) shows an image taken on the 16-channel CCD referred to above, and figure 9 b) shows an analysis of the periodic patterns. The latter is the average of 500 columns centered at column 250 taken on a median-filtered image that itself was generated from 100 images. The residuals were calculated as described earlier for the “tree-ring” analysis. The period of the large pixel-size excursions is about 39.4 pixels, or about $414 \mu\text{m}$. This agrees well with the $410 \mu\text{m}$ period reported for the early-version LSST CCD [8].

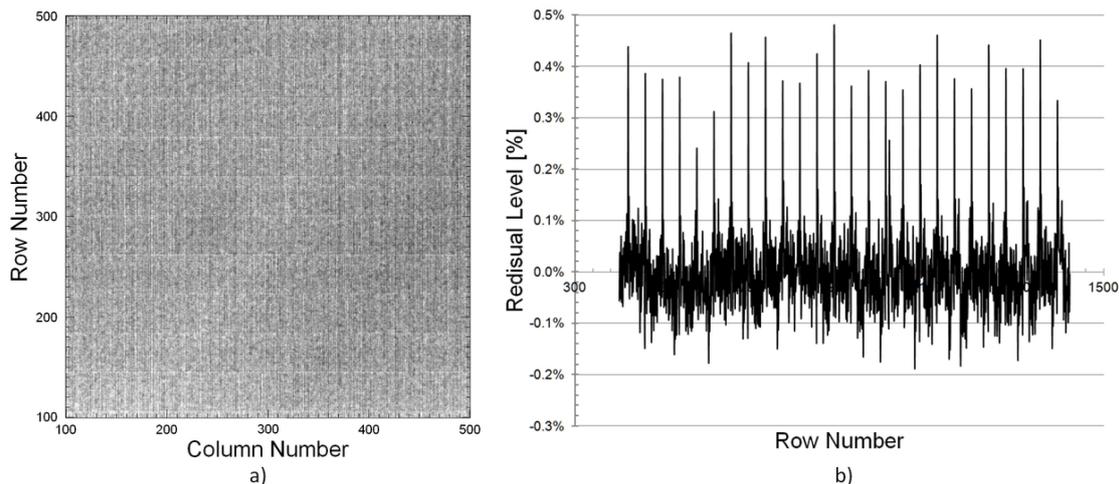


Figure 9. a) Median-filtered image showing significant periodic patterns taken with a 16-channel CCD. For this CCD the photomasks were generated on the Etec CORE-2564. The substrate-bias voltage was 50 V. The median-filtered image was generated from 100 images. b) Residual-level value in % for an average of 500 columns centered about column 250 versus the row number for the CCD in a).

The periodic effect is due to the method employed to manufacture the photomasks used in the CCD process. Commercially available, step-and-repeat systems are used at the vendor that provides the photomasks used in the DALSA CCD process. Multiple, parallel laser beams referred to as a “brush” are modulated to write the pixels, and the beams are incident on a rotating mirror that writes the mask pattern at each step-and-repeat location [27]. The regions where the patterns are butted together result in the periodic pixel-size variations.

The vendor of the equipment that made the step-and-repeat mask making systems, Etec Systems, Inc., made a number of such machines over a period of nearly two decades with increasingly better performance for each generation. It was discovered that the mask-making machine typically used for the DALSA CCD process was an early version, the CORE-2564. Given the relatively large geometries typical in scientific CCDs, this was a reasonable choice save for the periodic errors. The photomask vendor also had more modern versions of the mask-making equipment, and for the DESI CCDs the ALTA-3500 was used for the six masks that define the pixels in our process. The ALTA-3500 is roughly four generations more advanced than the CORE-2564 [28].

We used the same flat-field data that was discussed previously for the “tree-ring” analysis to study the periodic pixel-size variations for the DESI CCD of figure 6 b). Since the “tree rings” for that CCD are only significant at large radii from the center of the wafer, we were able to avoid any area with “tree rings” for this analysis. Figure 10 a) shows the residual level from columns 3150 to 4173 for an average of 500 rows centered at row 1000 at substrate-bias voltages of 50 and 100 V. The residual level is reduced by more than a factor of two when compared to the periodic-peak level seen in the 16-channel CCD in figure 9, and any periodic pattern that might be present in this data is not nearly as obvious as those seen on the 16-channel and LSST CCDs referenced earlier [2, 8]. In order to test for the presence of periodic patterns, a Fourier transform of the data in figure 10 a) was performed, and the results are shown in figure 10 b). We observe periodic peaks corresponding to high-frequency harmonics spaced at an inverse-spatial frequency of about 21.8 pixels, i.e. about

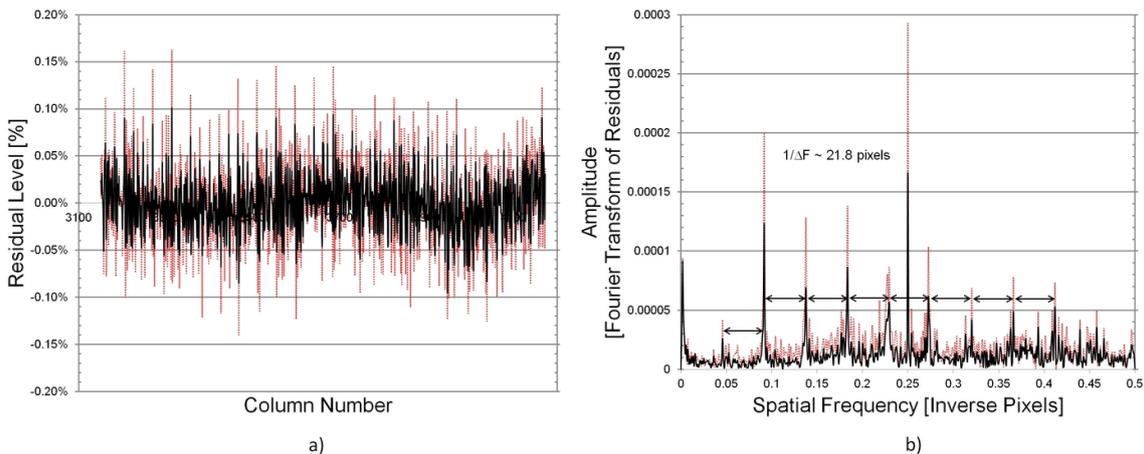


Figure 10. a) Residual-level value in % for an average of 500 rows centered about row 1000 versus column number for the DESI CCD fabricated on $> 15 \text{ k}\Omega\text{-cm}$ silicon whose image at 20 V substrate-bias voltage was shown in figure 6 b). The range of column numbers is 3150–4173. The data shown in the dashed red lines is for a substrate-bias voltage of 50 V, and that in the solid black lines corresponds to 100 V. The Etec ALTA-3500 was used to fabricate the six photomasks that define the pixels. b) The Fourier transform of the data in a) for 50 (dashed red lines) and 100 V (solid black lines) substrate-bias voltage. The arrowed lines are of equal length and denote the high-frequency harmonics of the periodic spatial frequency.

$327 \mu\text{m}$, as well as the peak at the fundamental frequency. The strong peak at a spatial frequency of 0.25 inverse pixels, i.e. a period of 4 pixels, is believed to be an artifact of the method used to calculate the Fourier transform.

Referring to the wafer layout shown in figure 1, we observed the same spatial-frequency component in the column direction of the $4\text{k} \times 2\text{k}$ to the right of the DESI $4\text{k} \times 4\text{k}$ CCD, but in the row direction of the $4\text{k} \times 2\text{k}$ that is above the DESI CCD. In all three cases this is the direction parallel to the wafer flat, and this is consistent with errors due to the mask-making equipment as initially pointed out by Smith and Rahmer [26]. The errors in the orthogonal direction, i.e. perpendicular to the wafer flat, do not show a strong periodicity according to the Fourier-transform analysis in those directions. The residual levels in that case are comparable to those shown in figure 10 a).

5 Summary

We have demonstrated performance improvements for the CCDs to be used in the Dark Energy Spectroscopic Instrument when compared to our prior CCD development for the Dark Energy Camera and the Baryon Oscillation Spectroscopic Survey. Read noise improvements explored earlier have been implemented on the DESI CCDs with good results. The QE is improved through the introduction of the high-index material ZrO_2 , and the physical properties of the anti-reflection coating stack has been analyzed in detail by transmission electron microscopy and secondary ion mass spectroscopy. We have also presented experimental results showing significant reductions in the level of “tree rings” and periodic mask errors that are enabled by the use of very high-resistivity silicon starting material, and the use of advanced photomasks, respectively.

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