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Automation of Serial Dilution using Microfluidic Digital Logic

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Automation of Serial Dilution using Microfluidic Digital Logic

THESIS

submitted in partial satisfaction of the requirements
for the degree of

MASTER OF SCIENCE

in Biomedical Engineering

by

Manasi Madhav Raje

Thesis Committee:
Assistant Professor Elliot E. Hui, Chair
Professor Abraham P. Lee
Assistant Professor Michelle Digman

2015

DEDICATION

To

my parents Aai and Baba, and my brother

my family and my friends

you all made me

Two roads diverged in a yellow wood,
And sorry I could not travel both
And be one traveler, long I stood
And looked down one as far as I could
To where it bent in the undergrowth;

Then took the other, as just as fair,
And having perhaps the better claim
Because it was grassy and wanted wear,
Though as for that the passing there
Had worn them really about the same,

And both that morning equally lay
In leaves no step had trodden black.
Oh, I kept the first for another day!
Yet knowing how way leads on to way
I doubted if I should ever come back.

I shall be telling this with a sigh
Somewhere ages and ages hence:
Two roads diverged in a wood, and I,
I took the one less traveled by,
And that has made all the difference.

- Robert Frost (1916)

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I would like to thank my committee members, Dr. Abraham Lee and Dr. Michelle Digman for their time and support.

I cannot thank my lab mates enough who enriched my lab experience at UC Irvine; a special thanks to Siavash Ahrar for his constant guidance and support towards my work. I genuinely appreciate his helpful attitude towards his colleagues and I admire his industrious approach towards his research.

Last but not the least; I thank the God inside me, for everything.

ABSTRACT OF THE THESIS

Automation of Serial Dilution using Microfluidic Digital Logic

By

Manasi Madhav Raje

Master of Science in Biomedical Engineering

University of California, Irvine, 2015

Assistant Professor Elliot E. Hui, Chair

Fluid handling procedures like serial dilution are common to a number of laboratory protocols. Such procedures are time consuming and require laboratory training to be performed. Thus using microfluidics technology for such procedures is very promising. Whereas there are a number of innovative lab-on-a-chip systems that use microfluidics to miniaturize lab procedures, these devices require heavy off-chip equipments to operate. For example a typical setup consists of a pump, a computer, tons of tubing and more. Such dependency on off-chip machinery limits microfluidic liquid handling devices only to highly-equipped settings. Therefore to exploit the microfluidic technology such that the devices are also useful for limited resource settings and other applications (e.g. point-of-care diagnostics), it is important to minimize or eliminate the dependence of these devices on off-chip control equipments.

Automation of fluid-handling microfluidic devices can be achieved by incorporating the control logic in the chip design. Pneumatic digital logic structures can be built on the chip and can be used to provide timing reference and also control signals for operations such as mixing/diluting, selection, storage and routing of liquid on the chip. This project explores the usefulness of

pneumatic digital logic for the purpose of automation of fluid handling microdevices. Serial dilution, which is a very common laboratory procedure, is automated on-chip such that the chip requires only one constant vacuum source for power and one clock signal to operate. Logic circuits such as the microfluidic oscillator, the finite state machine and, decoding circuits are employed to automate a fluid-handling circuit on the chip. This report discusses how these pneumatic digital logic structures can be integrated and optimized in order to control and operate a fluid-handling structure that carries out on-chip serial dilution.

1 Introduction

Lab-on-a-chip devices for the purpose of performing fluid handling operations have been a prominent topic of research lately since these devices offer advantages such as low fluid volume consumption, faster response time, compactness and better process control. A number of novel design concepts show promise in miniaturization of lab procedures [3]. However these devices are limited to highly equipped laboratories because they require a plethora of off-chip controllers. Even though a few devices work on technologies that provide convenient methods of on-chip liquid handling [2, 4, 6], they require a good amount of external machinery to control the liquid handling structure on-chip (Figure 1). The requirement of external controlling equipment almost defeats the purpose of miniaturizing the lab procedures. The dependency of such devices on off-chip controllers indicates that there is opportunity for further development of lab-on-a-chip devices such that their complete automation is achieved.

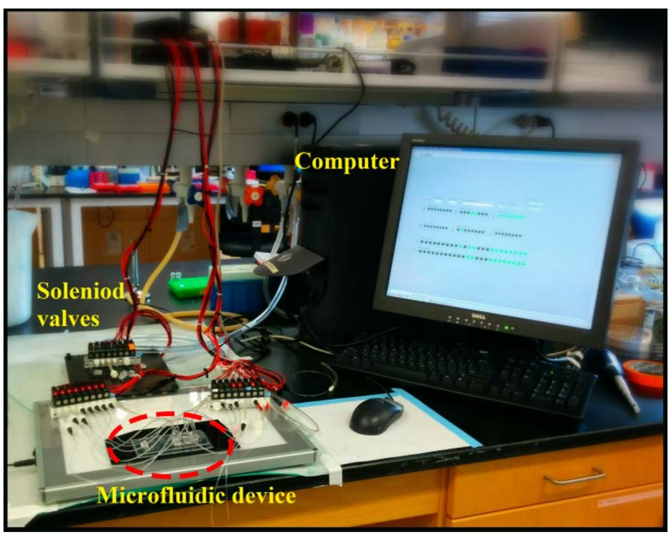


Figure 1: A typical setup to operate microfluidic devices requires a computer, solenoid valves and vacuum source.

The introduction of integrated electronic circuits (IEC) revolutionized the miniaturization of electrical circuits and facilitated the growth of the electronic industry quite massively [3]. While early digital circuits were built by wiring together discreet logic components, integrated circuit technology enabled large numbers of gates to be fabricated in parallel, along with all necessary wiring, on a single microchip. This brought tremendous advantages in manufacturing cost and miniaturization. A similar trend can be synthesized into microfluidics by constructing digital logic on the microfluidic chip itself. Implementation of digital logic in microfluidic devices has the potential to empower the lab-on-a-chip devices such that they can function with minimal or no control equipment [3, 5, 11, 13, 16]. This project chose to apply the pneumatic digital logic for the purpose of automation of a fluid handling chip. Pneumatic digital logic is similar to electronic digital logic with constant vacuum being analogous to constant electrical voltage and atmospheric pressure being analogous to electrical ground. A normally-closed monolithic valve [1] is employed as the basic building block of the logic circuits. Using this basic building block, digital logic circuits can be constructed, and these circuits can be employed to control liquid handling circuits on chip.

Serial dilution, which is a common lab procedure, is the subject of automation in this project. A microfluidic structure that can serially dilute a given sample is built and automated by on-chip pneumatic logic circuits.. Further chapters discuss the details of this technology and the methods used to implement it for the automation of serial dilution.

2 Background

Beginning with a simple pneumatic valve, one can build complex structures like latches, gates, memory elements and clocks. Microfluidic digital logic is quite similar to electronic digital logic and the following section describes various building blocks and examples of fluid-handling devices that can be useful for understanding this technology.

2.1 A Toolkit for microfluidic integration

As discussed in the previous chapter, one needs to identify the appropriate circuit for a specific function to be performed on a microfluidic chip. In this section a few examples of logic circuits that can perform common functions are discussed.

2.1.1 Valve- The basic building block

A valve is the most basic structure on a microfluidic chip. A valve has two states of operation namely open and closed. Thus it can either act as a switch or it can be interwoven into a complex structure with other valves and channels to perform complex operations. Figure 2 shows the cross-section of a normally closed monolithic valve. Since this project utilizes the architecture of only such valves, this report will be limited to the discussion of only normally closed monolithic valves [1, 15].

A typical valve as shown in Figure 2 is made of three layers; a fluidic layer that holds the input and output channel, a control layer that holds the displacement chamber and an elastomeric membrane that is the object of actuation. The control signal is supplied to the control layer and thus the displacement chamber holds vacuum; the vacuum pulls the elastomeric membrane into the displacement chamber and thereby establishes a connection between the input and output channels. Once such a connection is set, the fluid/signal in the input channel can flow to the output channel for further processing. Thus the valve can act as a switch controlled by a vacuum control signal.

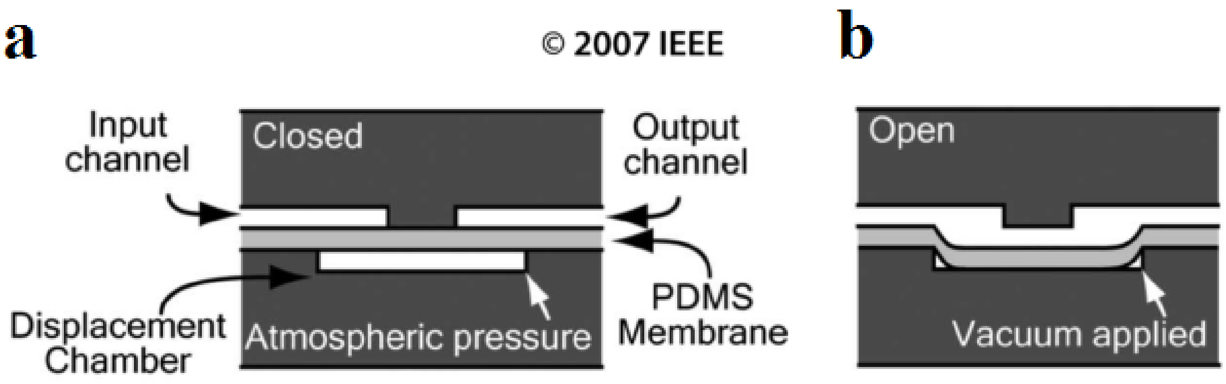


Figure 2: Cross-sectional view of a normally-closed monolithic valve. (a) The normally closed state of the valve when no control vacuum is supplied. (b) Open state of the valve when control vacuum is applied. Figure reprinted from [8]

2.1.2 Inverter

A NOT gate can be constructed out of a valve as shown in the Figure 3. An Inverter, as the name suggests outputs the inverse of a given input signal; it outputs 0 for a 1 and 1 for 0; where 1 denotes constant vacuum and 0 denotes atmosphere. The inverter can be constructed by connecting a valve to a constant vacuum and atmosphere each as shown in the figure. The valve is connected to the vacuum in series with a microfluidic resistor; a microfluidic resistor can be built by using a long channel that provides appropriate fluidic resistance to the signal. The constant vacuum can be supplied to the resistor and the control signal is supplied to the valve. When the control signal is 1, the valve opens up and connects the output to atmosphere (GND) and thus the output is 0. When the control signal is 0, the valve stays shut and the output receives 1 via the resistor’s path.

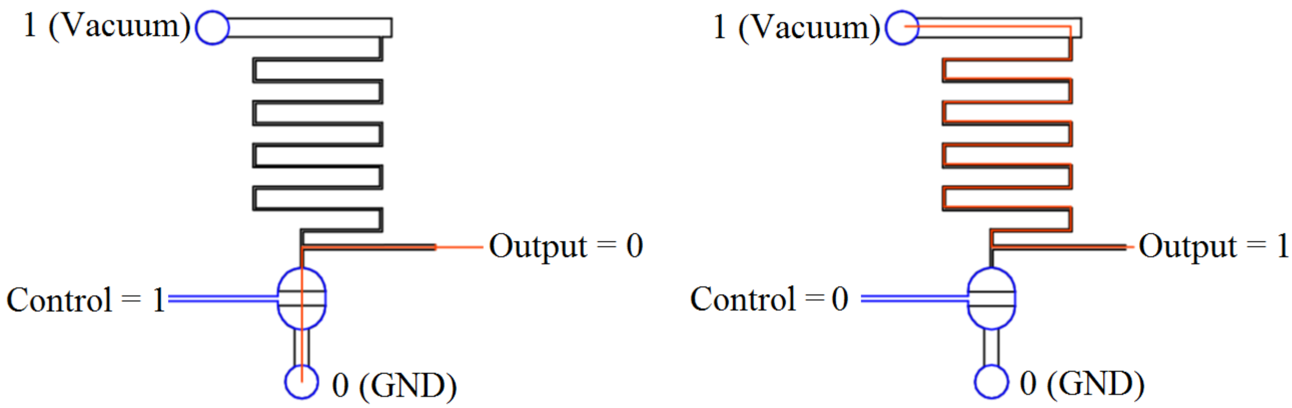


Figure 3: An inverter outputs a 0 for the control input 1 and it outputs a 0 for the control input 0. Black marking denotes the features on fluidic layer (top glass layer), blue marking denotes the features on the control layer (bottom glass layer) and, orange marking shows the path of output signal.

2.1.3 Buffer

A buffer is basically two inverters connected in series. A buffer is an extremely important tool when the circuit is designed to do a lot of signal processing. In such cases, the signals tend to weaken over the length of long channels or aren't strong enough for high frequency operations. Thus a buffer can be implanted in the middle of logic blocks to revive and maintain a signal's strength. Table 2 shows a microfluidic buffer circuit.

2.1.4 NOR gate

Now that a NOT gate is described, it is obvious that other logic gates can also be constructed using a valve. NOR gate is one such example where two or more inputs are fed to the gate to output a value according to the given truth table in Table 1. Such gates can be used to design logic programs or conditional switches or more. Table 2 shows the design of a NOR gate and other gates as well.

Input 1	Input 2	Output
0	0	1
0	1	0
1	0	0
1	1	0

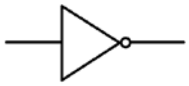
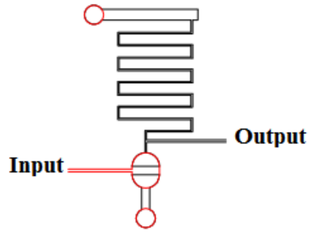
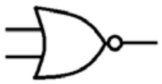
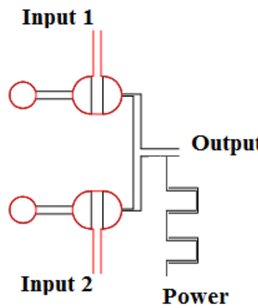
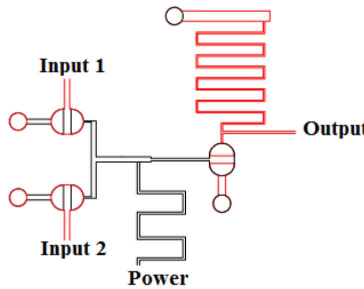
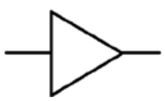
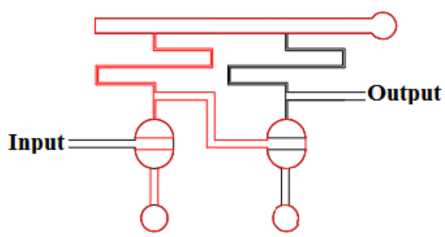
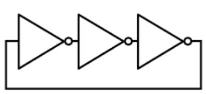
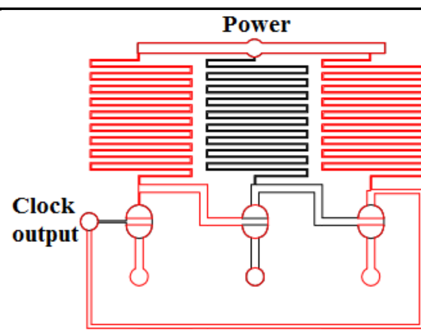
Table 1: The Truth-Table for NOR gate describes its functioning.

2.1.5 Oscillator

A microfluidic oscillator is analogous to a ring oscillator in electronic digital logic. It can be built by connecting an odd number of inverters in series and feeding the most extreme output to the first inverter. An oscillator produces oscillating signals that are very useful for operating on-chip pumps or providing a clock signal to other logic units on the same chip [7]. Since a variety of digital logic designs use a timing reference, an oscillator is a key element of the microfluidic automation toolkit. A schematic diagram and a circuit diagram can be seen in Table 2.

2.1.6 DFF (D Flip-Flop)

A microfluidic clocked D Flip-Flop is illustrated in Table 2. Its function is to shift the input bit by one clock cycle. It consists of two D latches connected in series where the clock pulse is supplied to the gate of the first latch and an inverse clock pulse is supplied to the gate of the second latch. The working of a DFF is briefly as follows; when the clock is 1 the first gate valve opens and the first D latch receives the data and stores it. When the clock turns 0, the gate of the first D latch closes to avoid further transfer of data and the gate of the second D latch opens to allow transfer of the data to the second D latch. Thus for one clock cycle, the data hops from the first D latch to the second D latch. Such microfluidic DFFs have been demonstrated previously by a few groups [5, 9, 11, 2]

Logic element	Logic symbol	Microfluidic circuit	Function
Inverter (NOT)			**Inverts the input**
NOR			**Outputs 1 only if both inputs are 0**
OR			**Outputs 1 when either of the two inputs is 1**
Buffer			**Outputs the same input (Maintains/ strengthens the input strength)**
Oscillator			**Generates oscillating signal**

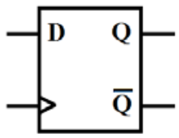
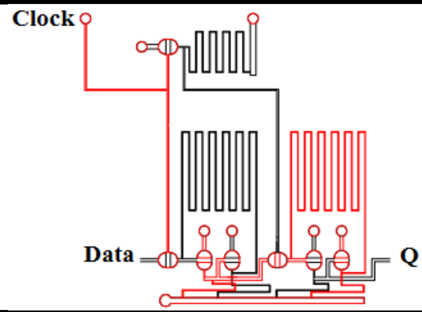
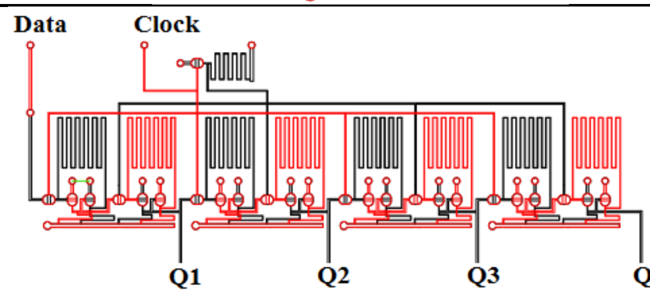
<table>
<tr><th>Logic element</th><th>Logic symbol</th><th>Microfluidic circuit</th><th>Function</th></tr>
<tr><td>DFF</td><td></td><td></td><td>Shifts the input data bit in one clock cycle</td></tr>
<tr><td>Shift Register</td><td>n/a</td><td></td><td>Shifts more than one data bits in one clock cycle</td></tr>
</table>

Table 2: Examples of a few logic elements and their logic symbols, microfluidic circuit diagram and, function.

2.2 A few fluid-handling devices

Till this date various microfluidic fluid handling devices that employ pneumatic digital logic have been demonstrated by a number of research groups. However, there has not been much progress in applying the microfluidic digital logic to control complex liquid handling on chip. This section highlights a few microfluidic fluid handling devices which served as the motivation for this project.

2.2.1 Microfluidic serial dilution circuit

A microfluidic serial dilution circuit was developed by Paegel et al. [4]. This device is capable of serially diluting a sample as small as 400 nanoliter with a minimum mixing time of 22 seconds for the mixing cycle. This is a very good example of how a cumbersome lab procedure can be made very simple to perform by recruiting the microfluidic technology. While the device (Figure

4) is good to conduct serial dilution on chip, it does require a good amount external control machinery.

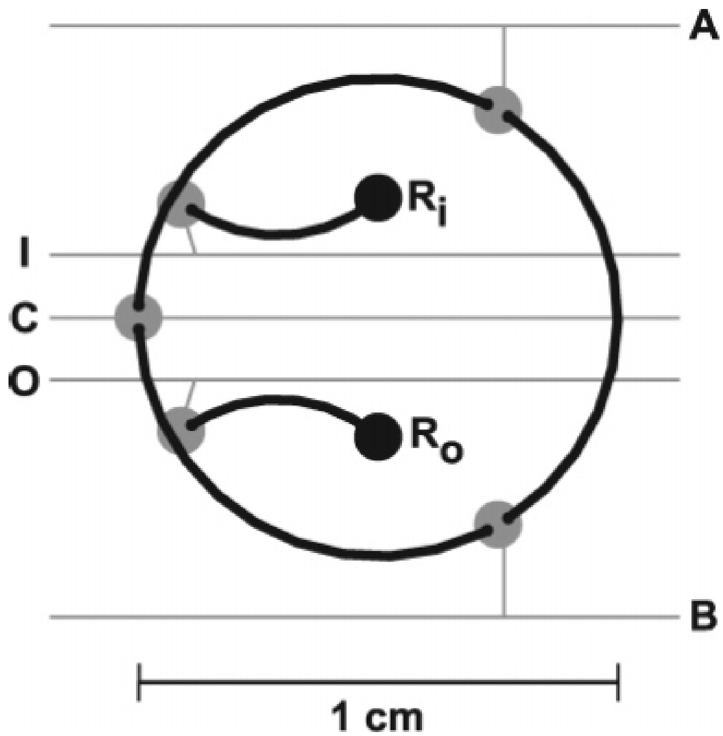


Figure 4: The microfluidic serial dilution circuit by Paegel et al. A, B, I, C, O denote the control lines of the valves on the chip. Figure reprinted by permission from Royal Society of Chemistry, copyright 2006, American Chemical Society [4].

2.2.2 Automaton

The Mathies research group at University of California Berkeley came up with a number of microfluidic fluid handling devices. The Automaton [2, 12] is a 2-D array of interconnected valves that can perform multiple fluidic operations by grouping specific valves (Figure 5). The group fabricated an 8 x 8 valve array which is used to carry out a variety of operations on a single chip. Where this device shows promising usefulness for carrying out complex fluid handling operations on-chip, due to a large number of control inputs it is heavily dependent on external control machinery and not to mention, the presence of multiple valves arranged closely on a single chip generates the requirement of positive pressure to close the valves properly. Thus it is realized that as the fluid handling gets complex, the microfluidics involved also get complex and as a result require more control equipments.

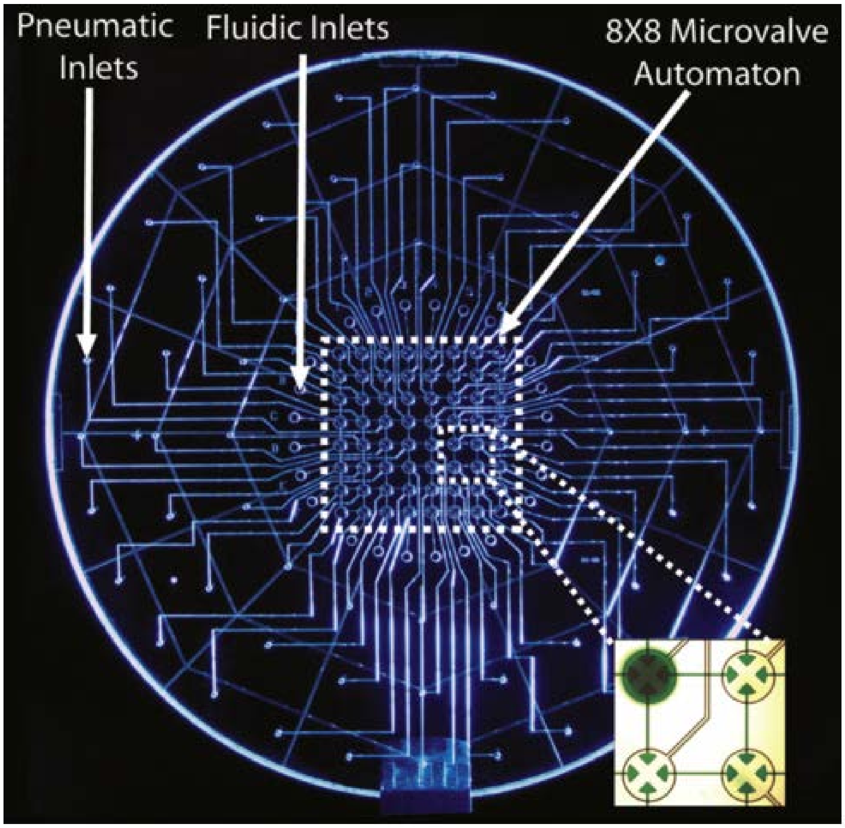


Figure 5: The Automaton by Jensen et al. The inset shows a close-up of the network of valves on-chip. Figure reprinted by permission from SAGE publications: JALA, copyright 2010 [2].

2.2.3 Serial dilution ladder

The serial dilution ladder is an evolution of the serial dilution circuit by Paegel et al. [6]. It consists of seven loops arranged in the form of a ladder as shown in Figure 6. Each loop carries out a 1:1 dilution through circulatory mixing by peristaltic pumping. Every loop is executed to perform 1:1 dilution one by one until an array of serially diluted sample is obtained. The novelty of this device is that it is capable of storing each stage of the dilutions for further use. Despite the compact and effective architecture of this device, it requires a lot of heavy off-chip control circuitry to operate which motivates the application of microfluidic digital logic to such systems.

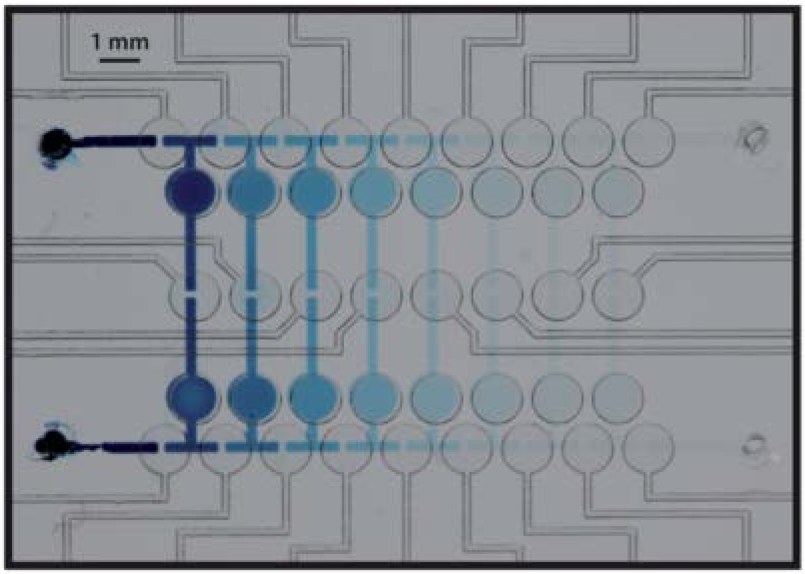


Figure 6: The serial dilution ladder demonstrated by Ahrar et al. Figure reprinted by permission from Royal Society of Chemistry, copyright 2013 [6].

2.2.4 Semi-Autonomous liquid handling device

A semi-autonomous device was engineered by Nguyen et al. [10]. This device was capable of producing on-chip pumping signals for pumping and mixing fluid on-chip. The device required a total of four control inputs and one power line to operate and maintain four states of operation; meter, mix, incubate and flush (Figure 7). While this device is a good example that portrays the usefulness of pneumatic digital logic for a simple lab procedure, a small amount of off-chip machinery is still required to drive the four control inputs.

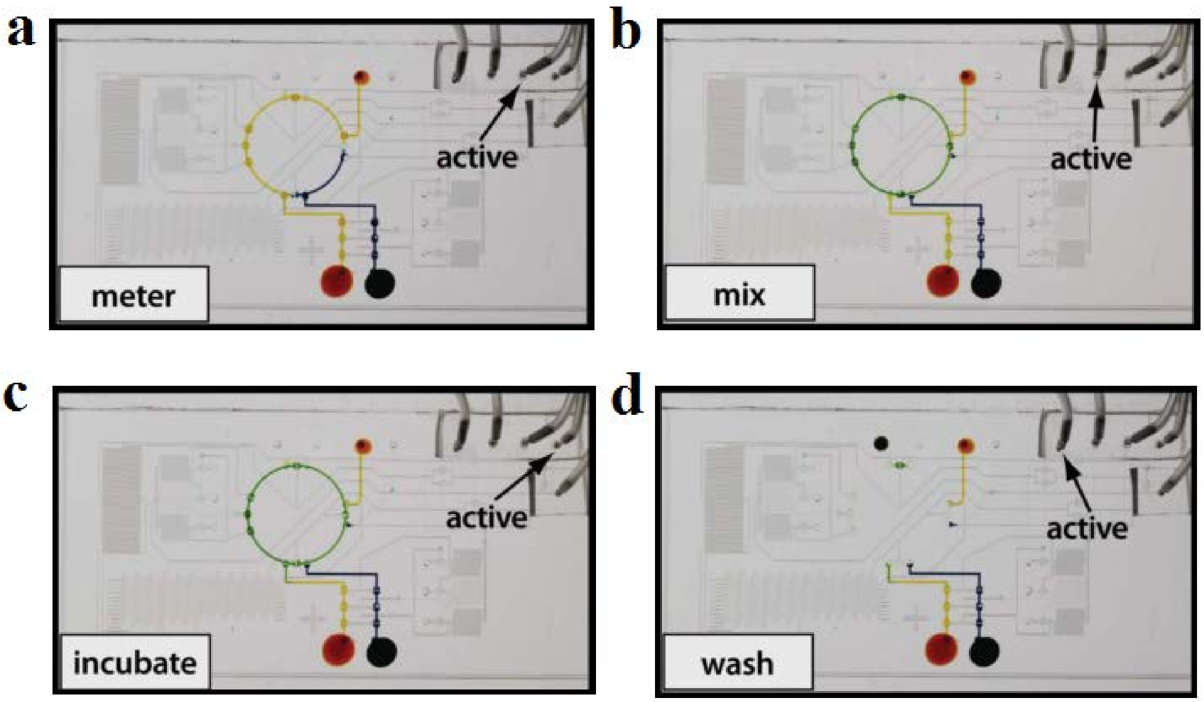


Figure 7: Four states of the semi-autonomous liquid handling device by Nguyen et al. Figure reprinted by permission from Royal Society of Chemistry, copyright 2012 [10].

3 Materials and Methods

Figure 8 shows the dismantled view of a part of the typical device in the discussion. The device is basically two patterned glass wafers and a thin PDMS membrane stacked together. The adhesion forces between glass and PDMS are enough to hold the three layers tight. The features on the glass wafers face each other through the sheet of PDMS. Signal transfer between these two glass wafers is achieved by Via holes, which are made by coring the PDMS membrane using a hollow blunt needle. To access the power ports and make ground ports, the glass wafer was drilled using diamond-tipped grinding bits (McMaster-Carr, Robbinsville, NJ, USA).

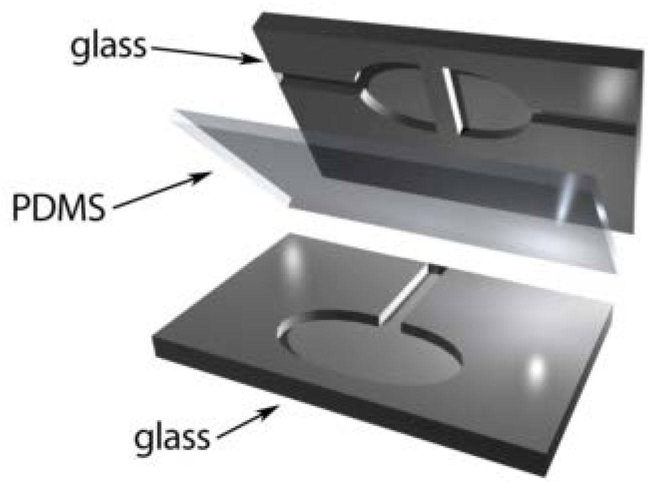


Figure 8: A dismantled view of the normally-closed monolithic valve; showing three layers of the device.

The device fabrication has been described in detail previously [1]. The device fabrication briefly involves a few stages; Designing, Lithography, Glass etching, drilling the access and ground holes and, assembling the device for use. The circuits were designed and drawn on AutoCAD. The design was then patterned on glass using lithography and HF etching of the glass. Further, a thin PDMS membrane was sandwiched between the two layers of glass etched with compatible designs. Via holes in the PDMS layer were bored before assembling all three layers.

Devices were first tested without liquid to visualize the timing of the valves. After this first stage of debugging, the devices were then tested with liquid added. In order to drive the prototype devices during testing, pneumatic input signals were provided by an off-chip vacuum manifold under computer control.

4 The Scheme of Automation

This project employs an approach that is analogous to the digital logic in electronic design. Normally-closed valves and channels are brought together to perform in the way digital logic structures like transistors, flip-flops etc. do. Microfluidic digital logic structures like flip-flops, switches, timing circuits have been developed in previous reports [5, 7, 9, 11]. Whereas previously this technology has been similarly exploited by a few research groups, it has not been yet explored for the automation of a complex liquid handling procedure. This project uses microfluidic digital logic to automate serial dilution on chip. Since the prime aim of this project is to achieve the automation of serial dilution, rather than quantification of the dilution efficiency, the emphasis is given on the integration, reduction of off-chip control and, the compactness of the device.

The proposed autonomous serial dilution ladder consists of four logic blocks; the oscillator, the Finite State Machine (FSM) (See section 7.1 for detailed explanation), the decoder and, the dilution ladder. The heart of the system is a four stage dilution ladder. The first step towards reduction of off-chip control was to build a decoder circuit (see section 5 for detailed explanation). Briefly, the decoder decodes the loop selection signal generated on chip and routes the pumping signal appropriately towards the dilution ladder. The Oscillator provides oscillatory signal used for operating the pump valves in order to mix fluid and the FSM provides the loop selection signal useful for carrying out the mixing in a pre-determined sequence down the architecture of the ladder. Full device integration required buffer gates to be placed along the circuit connections between the different logic blocks in order to avoid signal attenuation.

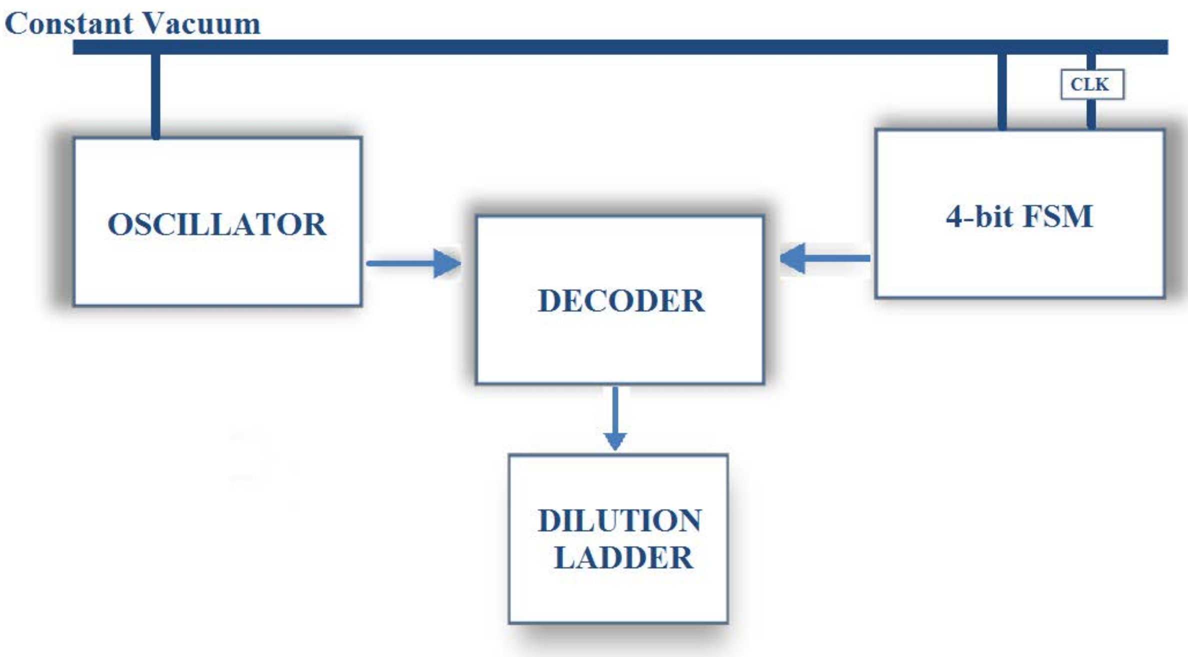


Figure 9: A block diagram of the scheme of automation; Integrating the digital logic elements with the fluid handling system (Serial dilution ladder).

The working of this chip can be explained using the schematic diagram provided (Figure 9) as follows: The FSM generates a 4-bit binary code which is fed to the decoder; the decoder decodes the code and selects the corresponding loop of the dilution ladder. Upon selection by the decoder, the path of the oscillatory signal for that particular loop opens up and the oscillatory signal that is generated by the oscillator is routed to the pump valves of that loop. This oscillatory signal, by the nature of it, establishes circulatory motion of the fluid in the loop and as a result mixes the contents of that loop. In this fashion all the loops are executed in a sequence of the first to the fourth loop and the end result should be an array of serially diluted sample.

5 Design and Integration of the Decoder

5.1 Purpose

The dilution ladder is basically a series of mixing loops that requires two basic steps for operation; 1) selecting a particular loop and then 2) mixing the contents of that loop. Thus it would require two signals that carry out these two activities. Since the dilution ladder is designed as a fluid handling system without any digital logic, it needs a decoding unit that would decode the signals received from the FSM and route the signal from the Oscillator to the specific loop in order to facilitate the dilution ladder to carry out the mixing in that loop. Thus, decoder circuits that sit around the dilution ladder and receive and process the control signals from other logic blocks on the chip were built and tested.

5.2 Decoder designs built and tested

Two designs were tested for the purpose of routing the signals to the dilution ladder. The first design that was tested incorporated columns of microfluidic AND gates for each pump valve of the dilution ladder as shown in Figure 10. Normally-closed-valves when connected serially, perform like an AND logic gate. An eight-stage dilution ladder decoder was built with six inputs and eight outputs. Every output was used to control the pump valves of the dilution ladder. Rigorous testing of this circuit with air and with liquid in the pump channels proved that this circuit is not the best design for the decoder. This design is not easily scalable and it is difficult to shrink the size of the decoder in this design. Further, the design posed difficulty in priming of the ladder. Therefore, a new design was built and tested which consisted of lesser valves, occupied lesser chip area and, is priming-friendly.

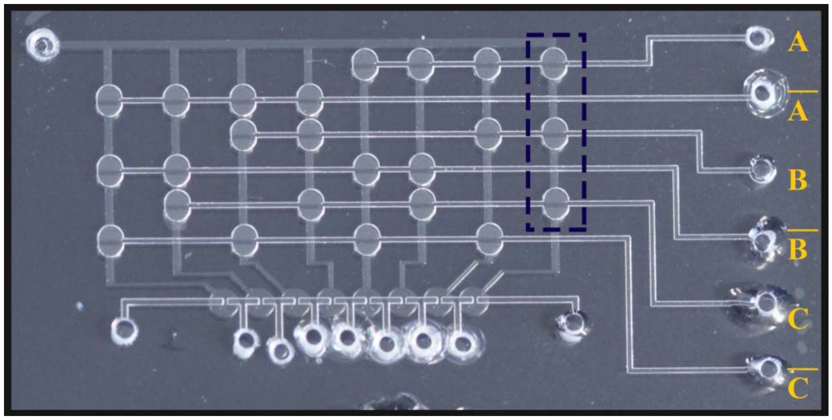


Figure 10: The first design tested for the decoder; boxed section shows one of the AND logic gates on the design, the AND logic gate allows the input to flow into the output channel only when all the three control inputs are 1. (A - inv. C are control inputs.)

A better design for the decoder was built and tested for proper routing of signals and any possible signal or fluid leakage. After several tests it was finalized as the decoder that would be used for the system. Figure 11 shows the schematic diagram of the decoder used in our system. The valves of a decoder are situated in such a fashion that on receiving the signal from the FSM, only a particular set of valves open and route the oscillating signal towards the corresponding loop of the dilution ladder. This circuit requires a four bit signal from the FSM thus the input requirement for the decoder block is four. Figure 11 shows a four-stage decoder circuit and the highlighted path demonstrates the selection and activation of a loop. For example when loop 2 is supposed to be selected, the FSM generates a signal of 0010 and the valve d2 of the decoder opens to route the oscillating signal via the perpendicularly underlying channel. The function of the decoder can also be noted in Table 3.

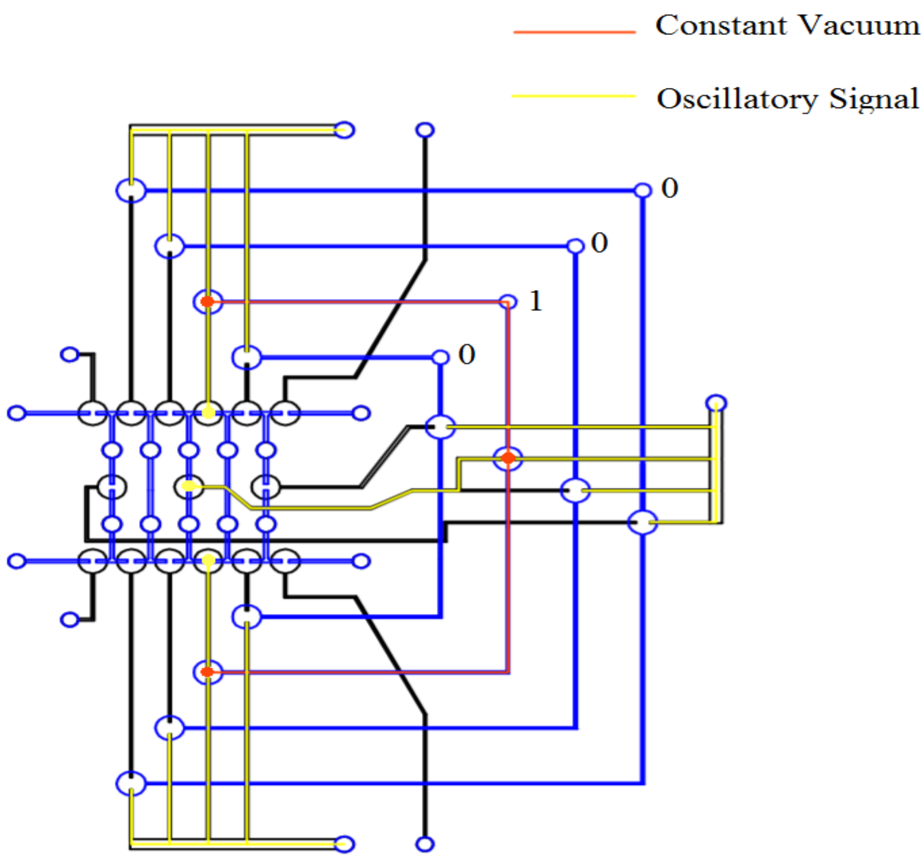


Figure 11: A schematic diagram of the decoder integrated with the dilution ladder; the highlighted orange path shows the path of control signal and the yellow color shows the path of the oscillatory signal that establishes pumping action in the ladder.

Code	Function
0001	Select loop 1
0010	Select loop 2
0100	Select loop 3
1000	Select loop 4

Table 3: Table showing the function of the decoder; the decoder selects the corresponding loop on receiving a 4-bit signal.

The serial dilution ladder is a scalable structure and thus also requires a scalable decoder structure. This decoder design is scalable and can be scaled up to eight stages without increasing the number of input bits. Further scaling requires only two more input bits which is easy to incorporate in bigger circuits. Therefore, the decoder for eight-stage and sixteen-stage ladders were also fabricated and tested. Figure 12 shows the 8-stage and 16-stage decoder circuits.

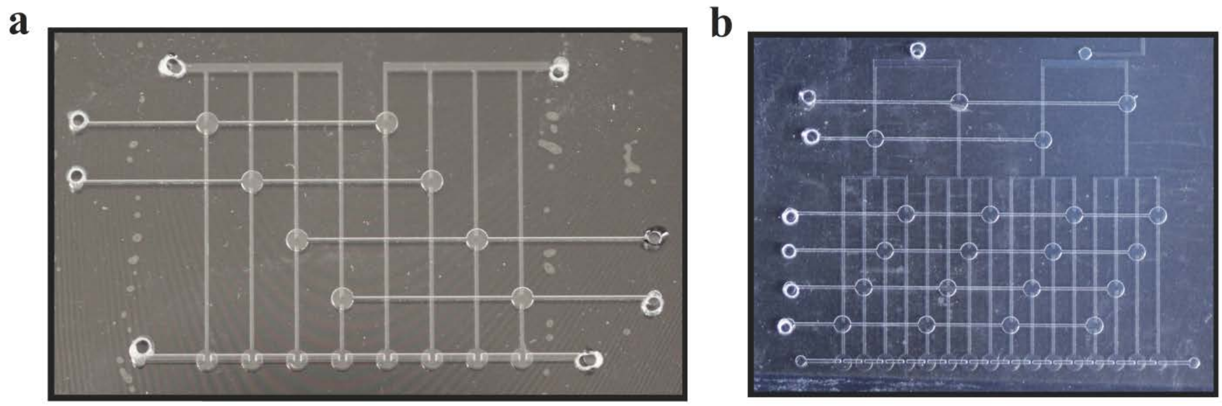


Figure 12: (a) The 8 stage decoder that can decode for an 8 stage dilution ladder and (b) The 16 stage decoder that can decode for a 16 stage dilution ladder.

5.3 Features of the decoder

5.3.1 Leak-proof routing structure

Various circuit parameters such as the width of the channels, the inter-valve distance and the length of the routing channel were tested during the development of the decoder. It was experimentally found that 100 microns is the best width for decoder channels to avoid crossover signals between the two layers. It is important to avoid crossover signals since it can lead to fluid leakage in the adjacent loops. Further, to test the best distance to be maintained in between two valves, various designs were tested and it was found that two valves of this decoder should be spaced by around 1400 microns vertically to avoid signal leakage. Using these designs various decoder heights were tested to ensure that the shortest possible working decoder is used in the final system. The shortest decoder (height 5.4 mm) designed works well but in order to accommodate another feature of the decoder (discussed in section 5.3.2), the height of 7 mm was chosen for the final decoder design. Figure 13 shows the decoder variations that were tested.

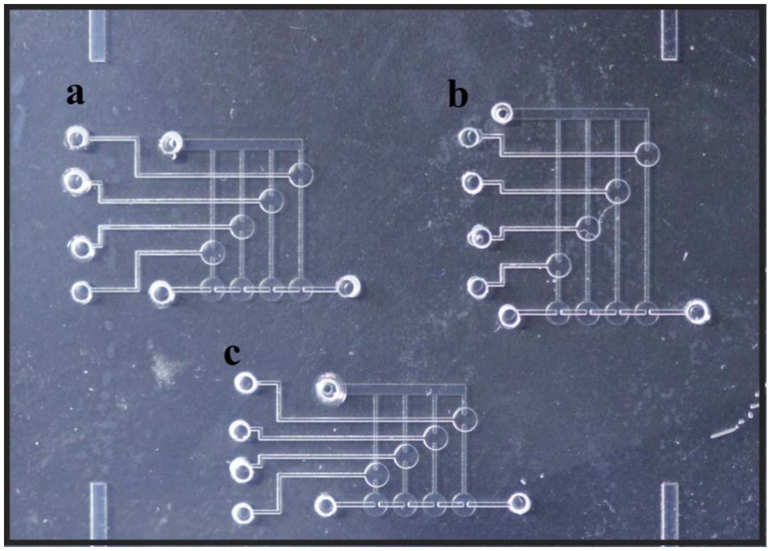


Figure 13: A number of variations in the decoder's features were tested; the height and channel width were changed and tested. (a) The decoder with a height of 7 mm, (b) The decoder with a height of 10 mm, (c) The decoder with a height of 5.4 mm.

5.3.2 Leak-proof pumping using the venting valves

As more components were integrated together, it was observed that pockets of vacuum could become trapped in parts of the decoder circuitry. This trapped vacuum could prevent liquid valves from closing properly, leading to leakage within the dilution ladder.

In order to overcome this limitation, a venting network was incorporated into the decoder circuit. This unique feature makes sure that the valves of the dilution ladder are sealed and closed well after performing the task of mixing so that the dilution is done in a leak-proof way. The venting network is automated in the sense that it doesn't require any manual venting operation; instead this network is designed in such a way that the valves of the decoder operate the venting valves.

The venting network (See Figure 15) consists of a set of valves that when activated, connect the routing channels to the nearest ground (GND). A particular venting valve is activated by the decoder valve that decodes the previous loop. In this way every venting valve vents off the extra vacuum in the routing channel that is connected to the previous loop. This results in efficient sealing of the valves of the previous loop and ensures leak-proof mixing in the running loop. Figure 14 shows the difference in the quality of dilution when the venting network is added to the decoders.

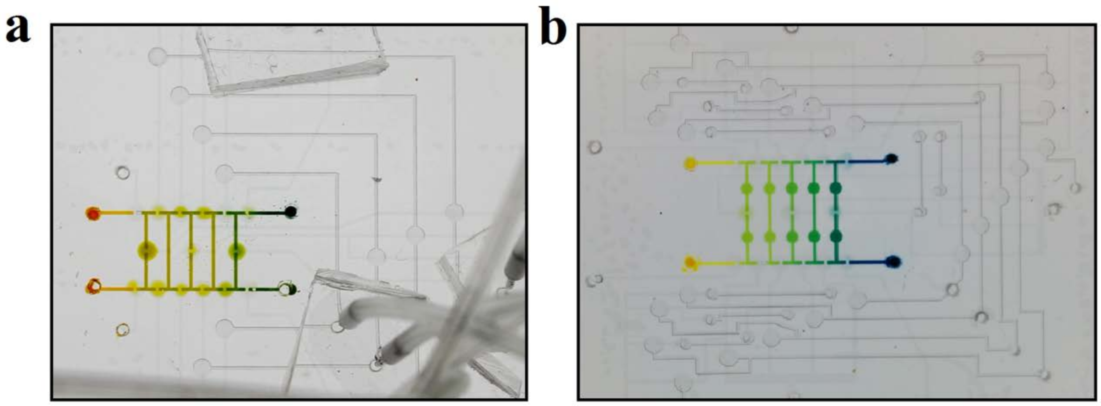


Figure 14: Figure showing the difference in the quality of dilution with and without venting network in the decoders; (a) Leakage of fluid from loop to loop and weak closing of the valves is seen. (b) Venting network helps in sealing the valves close after mixing which prevents leakage.

5.4 Integration of the decoder circuit with the dilution ladder

Considering a particular loop in the dilution ladder which has three pump valves in it, it requires three routing channels in order to route the oscillating signal to each pump valve in the loop. Further, to sequentially select each of the four loops of the dilution ladder, four valves are required on the decoder. Keeping these two requirements in mind, three decoders, each with four control valves were integrated with the dilution ladder. As shown in Figure 15, each decoder addressed the pump valves on the corresponding side of the dilution ladder. This integrated system reduced the number of off-chip connections from eleven to seven off-chip connections: three oscillating signals and four loop selection signals. This reduction of off-chip connections marks the first step of the automation of dilution ladder.

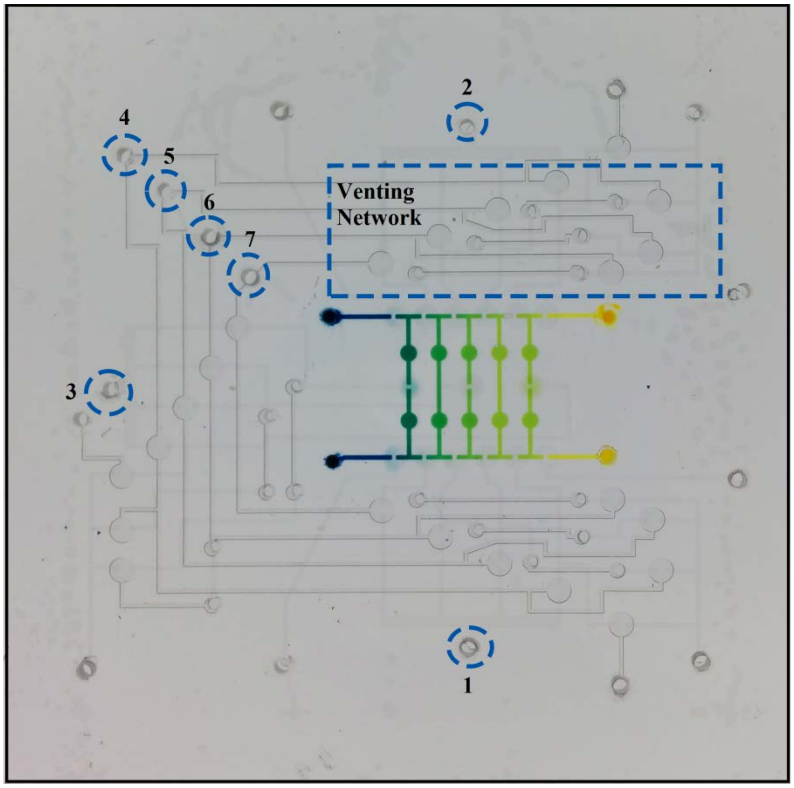


Figure 15: The device image of the integrated decoders with the dilution ladder; The boxed region is an example of one of the venting networks in the device, The circled inlets denote the seven active control inputs of the device.

6 Integration and automation of the on-chip pump

The next step in automation of the dilution ladder would be providing on chip signals for creating circulatory motion of the fluid in each loop of the dilution ladder and for the sequential selection of the loops. This chapter talks about how the automation of circulatory motion was achieved.

The circulatory mixing is done by peristaltic pumping. Peristaltic pumping is established by coordinated opening and closing of the three valves within a loop [6, 13, 14]. To achieve coordinated opening and closing of the valves, each valve should receive an oscillating signal which is shifted by a phase difference with respect to the signal provided to the other valves in the same loop.

Such a pumping pattern can be achieved by using a pneumatic oscillator [7, 10]. The oscillator is a series of odd number of pneumatic inverters connected to one another. The output of the final inverter is fed back to the first inverter so that a continuous oscillating signal is obtained from the output of every inverter. Thus, an oscillator with at least three inverters can be used to provide three phase-shifted oscillating signals to each of the three valves of the loop. As shown in the figure, one of the three output nodes can be connected to the input of each decoder. The decoders then carry out the task of routing the oscillating signal to the appropriate valve of the loop.

The challenges associated with the integration of an oscillator to the decoder depend on the distance between the oscillator's output nodes and the decoder input node, the signal strength and, the frequency of oscillations. The connection between the oscillator and the decoder is required to be that of least resistance so the connecting channels were designed to be 100 microns wide. The length of the channel was governed by the physical distance between the two circuit blocks. Further, two types of oscillators were integrated with the decoder and tested for efficient pumping. The three inverter oscillator provides a higher frequency of oscillations and thus requires a low resistance path for the signal to travel with the high frequency. Its high frequency does not provide enough time for the signal to reach the pump valves and the long connecting channel provides a high volume to overcome in the given short amount of time. Since the physical distance between the two circuits cannot be further reduced, a buffer (an inverter also strengthens the signal) was introduced on each connection in between the two connections to amplify the attenuated signal (Figure 16). The buffer cancelled the effect of the long channel and facilitated the pump valves to open and close efficiently with the provided high frequency of the oscillator. In contrast, the five-inverter oscillator has lower frequency and can pump efficiently without requiring any buffer. Since it is important to integrate these components in a way that the least signal attenuation is observed, the five-inverter oscillator along with the buffering inverters was chosen to provide on-chip pumping for the dilution ladder. This system is tested to be fast enough to provide a four stage serial dilution in approximately one minute.

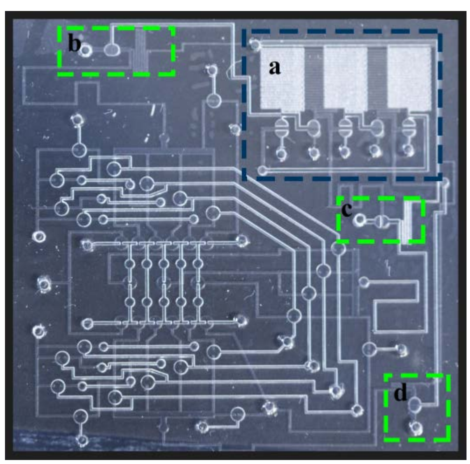


Figure 16: Device image of the integrated oscillator and decoders with the dilution ladder; (a) The five-stage oscillator. (b), (c), (d) the buffers connected in between the oscillator output nodes and the respective decoder inputs.

At this stage the system requires only five off-chip input signals; one constant signal for the oscillator and four constant signals for loop selection. The loop selection is semi-automated at this stage, meaning that off-chip inputs must be provided to select individual loops for mixing.

Manual operation of this activity can lead to differences in between the amount of selection times among the different loops. Such differences in selection times may lead to inaccurate dilution ratios throughout the ladder. Therefore, automation of this activity is essential. The problem can be solved by using a Finite State Machine which generates an accurate sequence of loop activation signals.

7 Integration of the Finite State Machine with the Decoder

At this stage the only inputs to the decoder are the four inputs for loop selection. Every loop must be selected sequentially for a specific amount of time to provide us with serial dilution of the given sample. To achieve this, a logic circuit which produces a 4-bit signal that follows a time varying output such as 1000, 0100, 0010, 0001 is required. This signal can be provided to the decoder network in order to achieve the proper loop selection.

7.1 The finite state machine

To generate such a 4-bit signal, a microfluidic 4-bit Finite State Machine (FSM) as shown in Figure 17 can be used to integrate with the decoder. A 2-bit and a 3-bit FSM have been demonstrated previously [5]. The FSM that is used consists of four D Flip Flops (DFF) connected together such that they can store and transfer one bit at a time and a NOR gate to process the output in order to generate the next bit. The output of the first three DFFs is fed to the NOR gate and thus it produces a 1 only when the last bit also has turned 0. This way loops are selected serially and only loop one is selected at a time.

The schematic diagram for the 4-bit FSM is shown in Figure 17. The building block of this system is a D Flip-Flop (DFF) that receives and stores the signal on the rising edge of the clock and does not change at other times. Thus in this system the DFF receives a value when the clock is 1 and transfers it to the next DFF when the clock is 0. As shown in the figure, the FSM consists of four cascading D Flip Flops, i.e. the output of the first three DFF is connected to the input of the DFF next to it. The output of the first three DFF also feed the NOR gate and the output of the NOR gate acts as the input to the first DFF. The FSM receives a clock input which acts as a timing reference for the DFFs to store and transfer the signal.

Thus, initially the power supplies an input of 1 to the first DFF, which it transfers to the second DFF and receives a 0 from the NOR output. Similarly, the second DFF transfers the 1 to the third DFF and receives a 0 from the first DFF in the next clock cycle. This continues till the last DFF receives a 0 from the third DFF. Once the last DFF turns 0, the NOR gate outputs a 1 to the first DFF. This way all the components form a loop and the machine results in an output of; 1000...0100…0010…0001...1000…0100 and so on. The loop continues till the FSM receives the power and the clock.

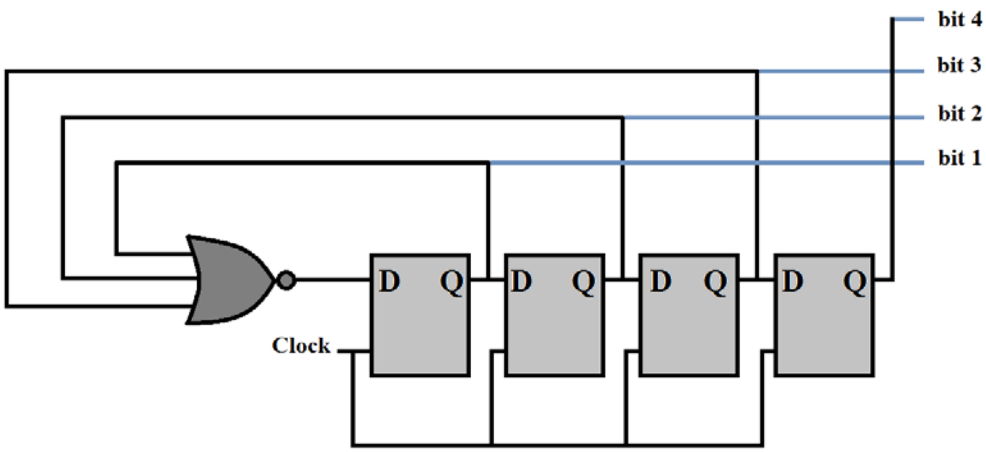


Figure 17: Schematic diagram of the Finite State Machine; four DFFs are cascaded and a NOR logic gate is connected to the first DFF. The outputs of the first three DFFs are fed to the NOR gate.

7.3 Integration of the FSM with the decoder

The challenges involved in the integration of the FSM with the decoder include: the placement of the FSM on a 40x80 chip such that the clock lines to each DFF are of equal length and, the connection channels between the decoder and the FSM offer low enough resistance to avoid signal attenuation. The placement and connections were thus made as shown in Figure 18. The number of off-chip connections at this point is 5: 3 oscillatory signals and one power and one clock signal to the FSM.

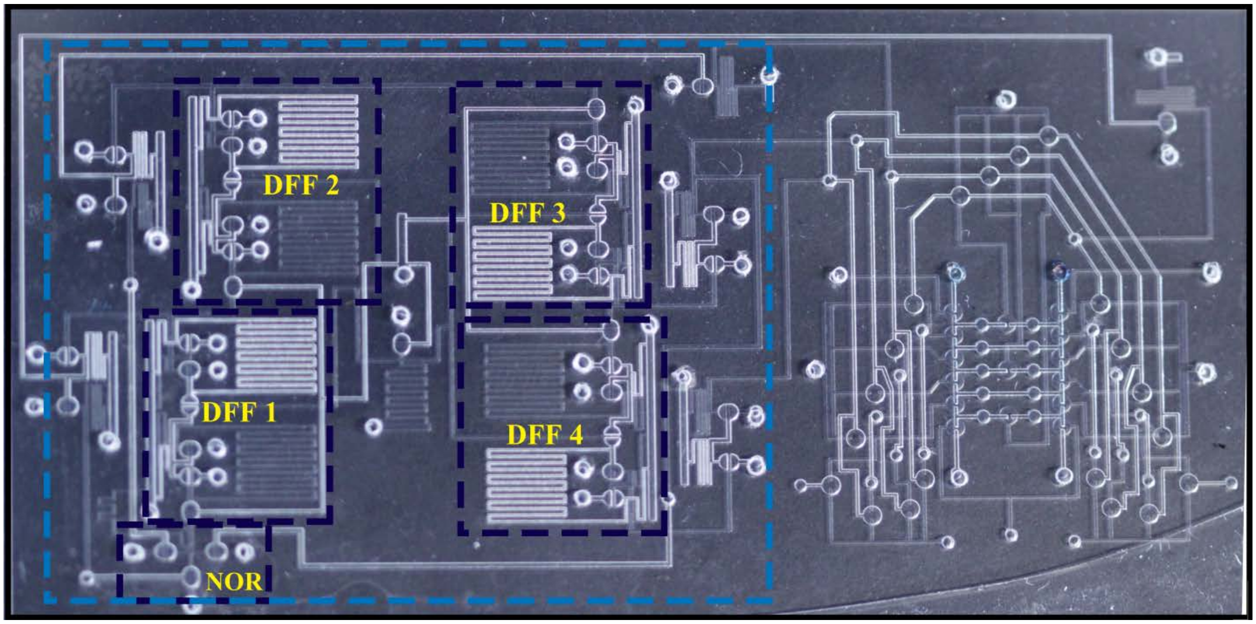


Figure 18: Device image of the integrated FSM and the decoders with the dilution ladder; outermost box denotes the 4-bit FSM block, the NOR logic gate and all the four DFFs have been highlighted and labeled.

At this stage, the decoder had been integrated with the oscillator and the FSM separately. The next step in the process of automation would be to integrate all the components together on one chip and reduce the number of off-chip inputs further.

8 Integration of all the control elements with the fluid handling element

The final step in automation of the dilution ladder involves integrating all the components on chip, (Figure 19) i.e. the dilution ladder, the decoders, the oscillator and, the FSM. All the components are required to be integrated on a small chip estate of 40x80 cm and to function together as a system. The integration was carried out as shown in the Figure. The device was fabricated and tested using one off-chip constant vacuum for power and one off-chip clock signal of desired frequency. Figure 20 shows the four stages of device working to achieve an array of serially diluted sample. Device performance was visualized by diluting food coloring.

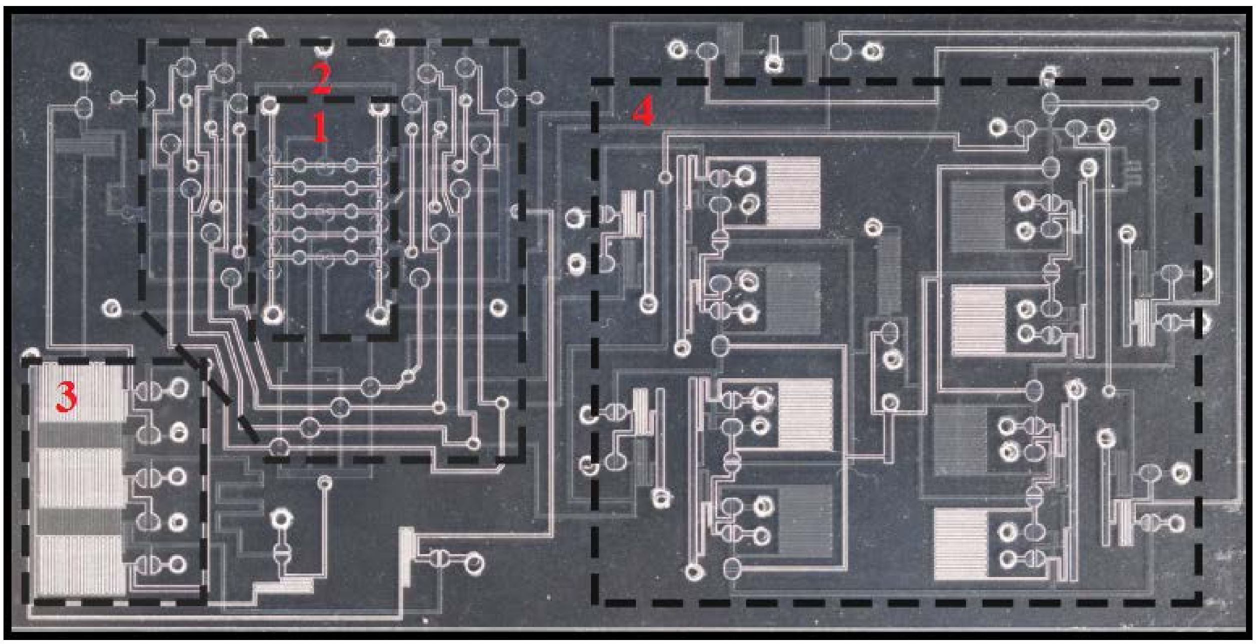


Figure 19: Device image of the final stage of the device which includes every control logic block on the chip; (1) The dilution ladder, (2) The decoders, (3) The oscillator, (4) The 4-bit Finite State Machine.

8.1 Working of this automated chip

The process can be described as follows: the FSM receives an off chip clock and constant vacuum signal as power. It generates and transfers a 4-bit binary signal that is fed to the four input lines in the decoders. The decoder decodes the 4-bit signal and selects a loop for mixing.

As a result the path for the oscillatory signal of the selected loop gets connected and the selected loop receives the oscillatory signal from the oscillator. Once the loop receives the oscillatory signal, the three pump valves of the loop get involved in a peristaltic pumping action and cause circulatory mixing of the contents of the loop. Thus, a 1:1 dilution is obtained in that loop. This process continues till all the four loops are selected and activated sequentially. Finally, an array of dilutions is obtained in the ladder structure**.**

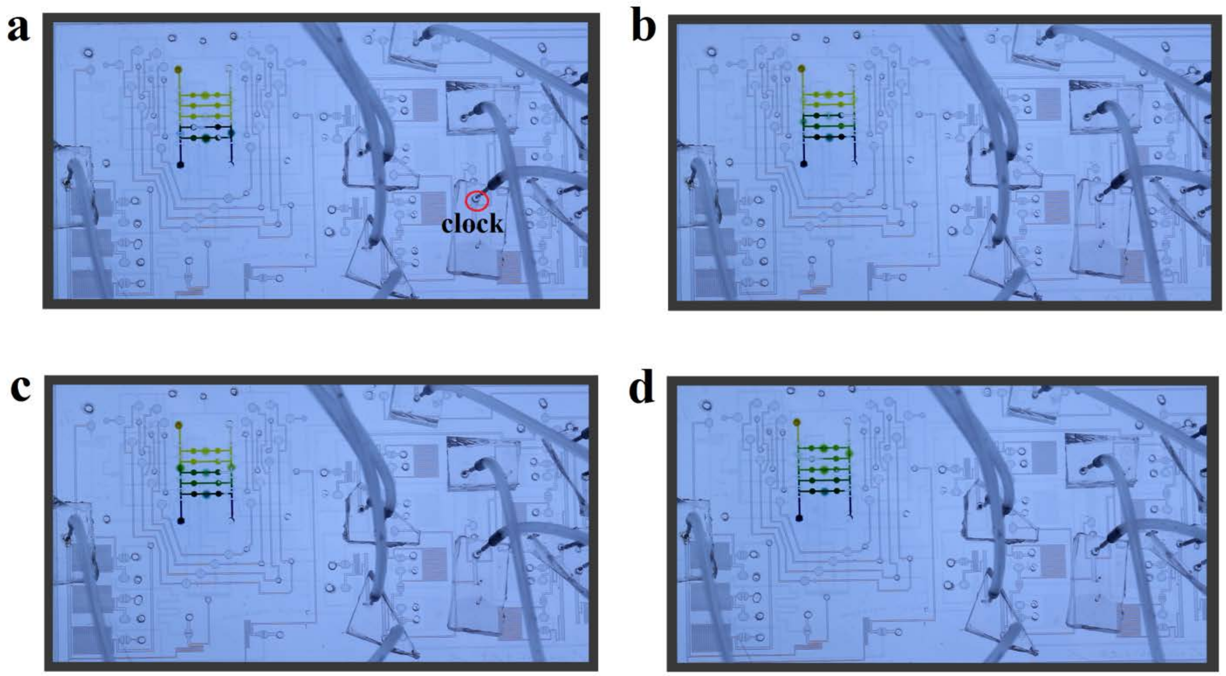


Figure 20: The four stages of the automated diluter; (a) The first loop is being executed, *the encircled input denotes the clock input while the other inputs being static vacuum.* (b) The second loop is being executed. (c) The third loop is being executed. (d) The fourth loop is being executed.

9 Discussion

This report has described the evolution of a complex fluid handling microfluidic device into an intelligent and autonomous device. It was noted that the operations like actuation of the pump, and selection of the loops of the dilution ladder were automated by using on-chip microfluidic digital logic. The progress made from a manually operated device to an automated device is summarized and listed in the following table (Table 4) and depicted in Figure 21.

Characteristics	Manually operated diluter	Automated diluter
Number of control inputs	**11**	**2**
Time required to dilute	**Depends on the user's speed**	**Approx 1 min (dye and water)**
Control equipments required	**Solenoid valves, Computer program, Vacuum source**	**Vacuum source, Clock**
Priming technique	**User dependant**	**Self-priming**

Table 4: Showing comparison between the manually operated serial dilution ladder and the automated serial dilution ladder.

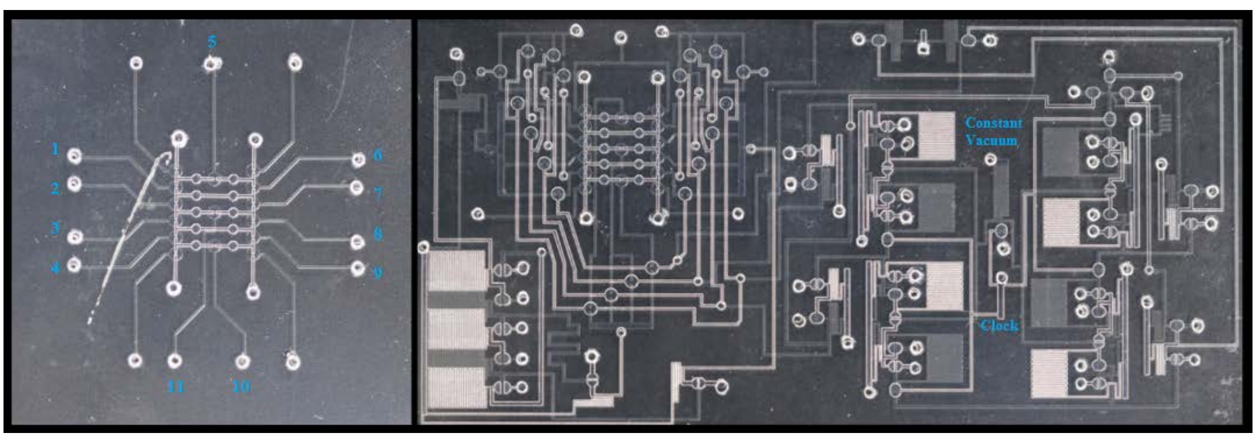


Figure 21: An image showing the difference between the manually operated diluter and the automated diluter with the control logic on-chip; the numbers on the image on left show the number of active control inputs.

This design also shows opportunity for further development in the number of dilutions that can be performed on the chip. The dilution ladder itself is a pretty scalable design and the logic circuitry around it can also be extended to control a longer ladder. The oscillator can be used as it is, the FSM can be extended for the increase in number of loops and the scalability of the decoder is discussed previously.

Additionally, the fact that the final design uses an external clock leaves breadth for the use of a number of different reagents that require different mixing times. It is important to provide application flexibility while designing a device and that is maintained in the design of this device.

10 Conclusion and Future Work

The lab procedure serial dilution has been automated on a microfluidic chip such that it requires only one constant vacuum to power and one clock signal as per the nature of the reagents involved.

While this is a good achievement in automation of liquid handling procedures, it is still a rough proof of concept that is fairly unreliable and requires very careful tuning to run. We aspire to get rid of this requirement as well and thus aim to optimize this design in future. Further, the design can benefit some reduction in the circuit density since very high circuit density makes it difficult to assemble and run the device. This problem can be possibly solved by miniaturizing the individual components in the circuit keeping in mind the recent advances in pneumatic logic density [17] or by using a larger chip estate for integrating all the components. Thus, this report can be summed up by realizing the stated achievements and the scope for improvement for the betterment of the device.

11 References

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