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Design of Pulsed-coherent Lidar

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Design of Pulsed-coherent Lidar

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by

Li-Yang Chen

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ABSTRACT OF THE DISSERTATION

Design of Pulsed-coherent Lidar

by

Li-Yang Chen
Doctor of Philosophy in Electrical and Computer Engineering
University of California, Los Angeles, 2021
Professor C. -K. Ken Yang, Chair

Lidars are becoming common components for remote sensing and ranging in many emerging applications such as autonomous vehicles and facial recognition. To accurately visualize the point cloud for further data processing, metrics such as precision, sampling rate, and linearity are important. Several architectures are often used for the distance detection. Coherent phase detection has been widely used for high precision; however, resolving the ranging ambiguity beyond one carrier period lowers the system acquisition rate. Another, pulsed direct time-of-flight (ToF) detection provides a high sampling rate using single-shot pulses and measuring their reflection, but the delay's dependence on the reflected energy limits the precision. Frequency-modulated continuous-wave (FMCW) lidar has the advantages of long-distance and high precision; however, the linearity is not sustainable for operating over a wide dynamic range.

In this work, we present a pulsed-coherent detection to combine the advantages from both the pulsed detection with a high sampling rate and the phase detection with high precision. A CW laser source is amplitude modulated by a high RF carrier and a low-frequency pulsed envelope modulation. At the receiving end, the ToF detection is segmented into coarse,

intermediate, and fine. The receiver's algorithm measures the phase shift of the RF carrier as fine ToF. It also counts the arrival time of the low-frequency mask's envelope as intermediate and coarse ToF. This pulsed-coherent lidar can simplify the optical setup while achieving high precision and a high sampling rate.

We demonstrate three receiver architectures in two test chips: The first one is an analog-based receiver with separate coarse and fine detection paths. It records the arrival time of the pulse's post-edge as the coarse ToF and measures the phase shift of the carrier as the fine ToF. The proposed post-edge detection with an automatic gain control loop provides better suppression of walk error. The second one is a homodyne receiver using a digital signal processor (DSP), in which we reuse the same chip of analog-based receiver and collect the data using a sub-sampling ADC. Both the coarse detection and fine detection are calculated in the DSP. This receiver improves the immunity to process, voltage, and temperature (PVT) variation and inherently aligns the segmented measurements using the sampling clock as the reference hence achieving better precision at higher sampling rates. The last one is a DSP-based heterodyne receiver. It takes a lower frequency clock as the reference input and uses a local phase-locked loop (PLL) to generate the clock for the down-conversion mixer. This local oscillator (LO) generation reduces the coupling between the clock and the incoming signal. The two-step down-conversion with digital down-mixing improves the power efficiency and immunity to PVT variation without additional calibration.

In addition to the innovation of the architecture, this work also presents some novelties of the circuit implementations: (1) we introduced narrowband input-matching to improve the noise performance which uses direct wire-bonding between the photodiode (PD) bare die to the low noise amplifier; (2) we implemented phase-invariant amplifiers to operate the lidar system in wide dynamic range; (3) we built a low phase noise LO generator based on a ring-VCO-based PLL.

Two test chips are fabricated in TSMC 28-nm CMOS technology. We successfully demonstrated the lidar systems with both 1-D scanning and 2-D scanning. The system achieves

<10-μm precision with 5-MHz integration bandwidth and 30-μm INL at 2.5-m distance.

The dissertation of Li-Yang Chen is approved.

Aydin Babakhani

Greg Pottie

Chee Wei Wong

C. -K. Ken Yang, Committee Chair

University of California, Los Angeles

2021

To my parents and my wife

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Li-Yang Chen, Abhinav Kumar Vinod, James McMillan, Chee Wei Wong, Chih-Kong Ken Yang,"A 6m-Precision Pulsed-Coherent Lidar with a 40-dB Tuning Range Inverter-Based Phase-Invariant PGA," *IEEE Custom Integrated Circuits Conference (CICC)*, Apr. 2021.

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Li-Yang Chen, Abhinav Kumar Vinod, James McMillan, Chee Wei Wong, Chih-Kong Ken Yang,"A 19-GHz Pulsed-Coherent ToF Receiver with 40-μm Precision for Laser Ranging Systems," in *IEEE Solid-State Circuits Letters (SSC-L), vol. 2, no. 9, pp. 191-194*, Sept. 2019.

Li-Yang Chen, Abhinav Kumar Vinod, James McMillan, Chee Wei Wong, Chih-Kong Ken Yang,"A 19-GHz Pulsed-Coherent ToF Receiver with 40-μm Precision for Laser Ranging Systems," in *ESSCIRC, pp. 191-194.*, Cracow, Poland, 2019.

CHAPTER 1

Introduction

1.1 Ranging System

Ranging is a process of determining the distance between one location to another location. The ranging system has its ability to remotely construct a detailed environmental mapping both indoors [1, 2] and outdoors. It can be used in a variety of applications such as autonomous self-driving systems [3–5], terrestrial [6–8] or airborne [9] environmental assessments and 3-D model sketching. The system can be realized as "passive" sensing, such as a camera that detects the light intensity reflected from an object [10–12], or "active" sensing in which a system transmits a signal and receives the signal bounced back from the object. The camera system has advantages of color detection and robustness to the interference; however, it doesn't work well on ranging resolution, and it takes effort to process the data. The most common active sensing system is using radio frequencies for detection and ranging (radar) [13–15]. It can overcome difficult weather conditions and operate without light; however, both the range and angular resolution are limited by the frequency of the radio waves. Active sensing systems with higher precision can be implemented using directed light from a laser as the carrier signal for detection and ranging (lidar). Table 1.1 summarizes the pros and cons of the ranging systems.

Lidars can be utilized in a multitude of applications ranging from atmospheric sensing and meteorology to navigation and topographical mapping, with examples of the 3D point clouds. It has been shown to provide an important independent modality to 3-D imaging.

	Lidar	Radar	Camera
Night operation	☺	☺	☹
Angular resolution	☺	☹	☺
Range resolution	☺	☺	☹
Velocity detection	☺	☺	☹
Processing overhead	☺	☺	☹
Adverse weather	☹	☺	☹
Robustness to interference	☹	☹	☺
Color detection	☹	☹	☺
Field of view	☺	☺	☹
Device cost	☹	☺	☺
Classification	☺	☹	☺

Table 1.1: Comparison table of ranging systems.

Fig. 1.1 shows the applications of lidar. One important application of lidar is to the field of robotics. It is being used today as an important sensing modality on autonomous vehicles and unmanned aerial vehicles to map out geographic features and urban environments and on robots operating indoors to navigate cluttered and compact spaces.

Despite the fine precision and accuracy, one major drawback of current lidar systems is the tradeoff between achievable range and scan speed, and simultaneously satisfying both requirements is challenging. The potential of a high sampling rate and high precision system enables their use in new applications. Demand for ranging systems with high depth precision and fast acquisition has emerged for various applications such as mobile 3D scanning and remote biometrics.

This work presents an idea of pulsed-coherent segmented ToF detection to enhance the sampling rate while achieving precise scanning results. The system design can be flexibly

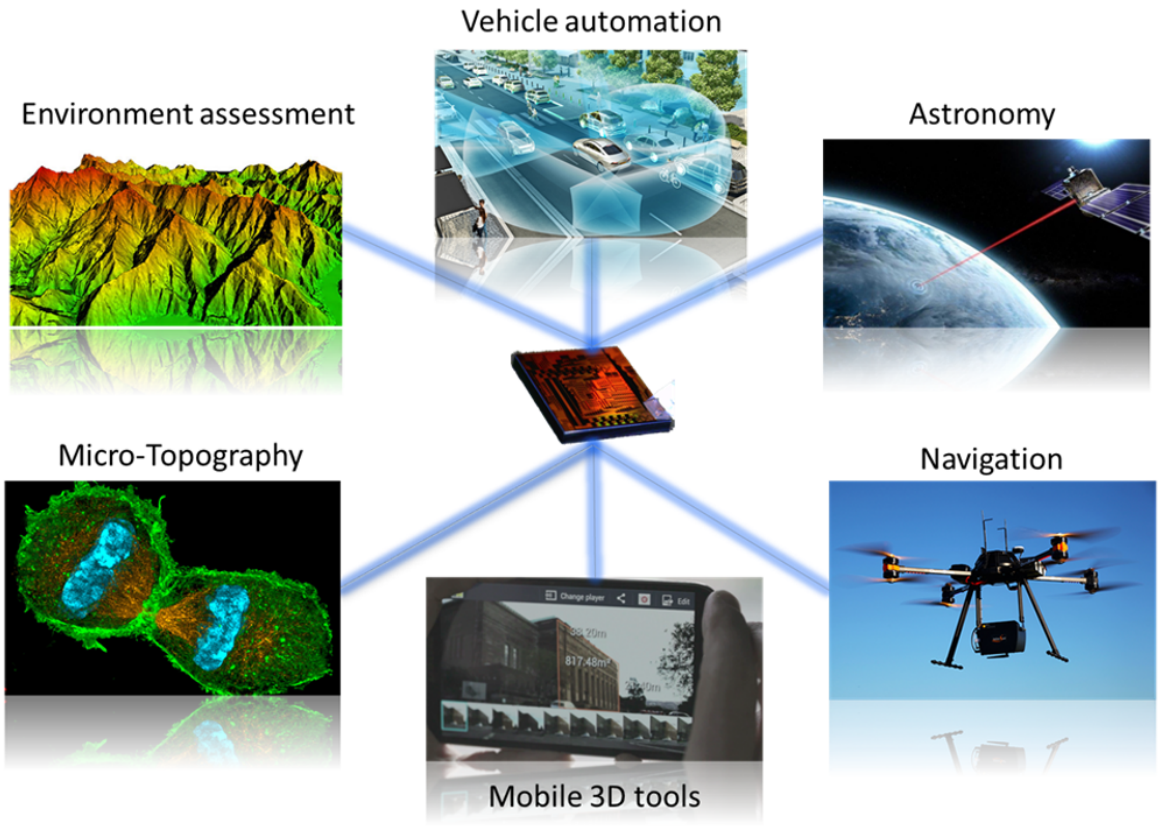

Figure 1.1: Lidar application.

adjusted based on various application requirements. We design our system to be segmented and allow for a change of parameters in an onboard digital signal processor (DSP) to optimize the range, precision, and signal-to-noise ratio (SNR) tradeoff as per the requirement. For the applications that require high precision, the encoded transmission sequence can be extended to increase the integration time and gather more energy from the target, thus improving the accuracy and the measurement distance. For fast acquisition applications, a shorter transmission format can accelerate the sampling speed. This flexibility helps the ranging in a dynamical and complex environment.

1.2 Terminology

To characterize and evaluate the system's performance, we introduce some essential metrics as follows [16]:

• Accuracy – It describes the closeness of the measurement value to the actual value. It consists of systematic errors such as linearity, walk error, and random error such as shot noise and quantization noise. It can be the absolute measurement (absolute accuracy) or the difference to a reference point (relative accuracy).

• Precision – The precision is the statistical measure of uncertainty from noise usually noted as rms error (σ). Some well-known noise sources exist in a lidar system, such as clock noise, quantization noise, thermal noise of the circuits, and acoustic noise.

• Resolution – Within a point cloud, this indicates the data density within the space of measurement. Typically it is limited by the beam size and the beam divergence of the emitted laser. Filtering and interpolation can be post-processed to improve the resolution further.

• Data acquisition rate – It describes how fast the lidar can collect the data. It is usually noted as sample per second (Sa/s) or pixel per second (Pixel/s) for a single-shot measurement and frame rate (frame/s) for a complete 2-D scanning.

• Scanning angle – The incident angle is that the laser beam can deviate from the focus plane, also known as the field of view (FoV). The scanning angle depends on applications and scanning topologies [17] such as mechanical scanning [4], phase array [18–20], or MEMS mirror [21].

• Output power – It is the optical power emitted from the transmitter. The safety regulation constraints the output power. For instance, 21 Code of Federal Regulations (CFR) Part 1040 in the US defines the classes of the emitted laser power, and American National Standards Institute (ANSI) Z136 [22, 23] controls the laser power by measuring the maximum permissible exposure (MPE) limits and accessible exposures limits (AELs).

1.3 Organization

The dissertation consists of 6 chapters. Chapter 2 introduces multiple lidar principles, including direct time-of-flight (ToF) detection (also known as pulsed lidar) and indirect time-of-flight detections, such as phase-based lidar and frequency-modulated continuous-wave (FMCW) lidar. We show each architecture with its pros and cons, and we compare the state-of-the-art lidar systems in a plot with the precision versus the acquisition rate. We also point out the desired design goal of our lidar system.

Chapter 3 presents the concept behind the pulsed-coherent lidar. We first discuss the segmented detection principle of the pulsed-coherent detection and its limiting factors, such as clock noise and the noise from the analog frontend circuit. The dominant noise sources are considered in our noise model. Next, we describe the step-by-step evolution of the pulsed-coherent lidar. We start from the essential building blocks of the coarse and fine detection to three different receiver architectures. One is an analog receiver with post-edge envelop detection; the others are two DSP-based receivers with homodyne and heterodyne architectures. We also estimate the link budget and the noise budget at the end of this chapter.

Chapter 4 shows the system implementations of both analog and DSP-based receivers. In the analog receiver, the fundamental building blocks include phase-invariant amplifiers and post-edge detection using an agile automatic gain control loop and measuring the arrival time of the envelope's post-edge to suppress the walk error. In the DSP-based receiver, we utilize a narrowband matching network to improve the sensitivity of the system. We also implement an inverter-based phase-invariant programmable gain amplifier which improves the linearity and the immunity to PVT variation, and a low phase noise LO generation using a type-II phase-locked loop with a ring-type voltage-controlled oscillator.

Chapter 5 shows the measurement results from several test chips. We first characterize the performance of the building blocks in the receivers individually. Then we present the

entire lidar system integrating the electrical receiver with the optical transmitter to validate its ranging ability. The 1-D scanning setup characterizes the system's linearity, precision, and segmented measurement results. Scanned 3-D images are shown with different 2-D scanning setups. In Chapter 6, we summarize this work.

CHAPTER 2

Lidar Detection Principle

This chapter reviews three commonly employed lidar architectures. Discussion of their advantages and drawbacks accompanies the description of each of these approaches. The chapter starts with the pulsed lidar followed by the phase-based (coherent) lidar. The frequency-modulated continuous-wave lidar is presented last followed by a discussion of our design goals and the motivation to explore a different architecture.

2.1 Pulsed Lidar

Pulsed lidar measures the time-of-flight (ToF) directly. In Fig. 2.1, the transmitting laser is modulated to send out a single pulse of light. Upon the transmission, a high-frequency counter starts to count. When the receiver detects the echoed signal, the counter stops and the resulting count reflects the ToF. The distance (d) can be converted from the ToF (Δt)

$$d = c \times \frac{\Delta t}{2}, \tag{2.1}$$

where c is the speed of light.

There are four main nonidealities of the pulsed lidar: (1) The clock jitter (σ_{clk}) of the reference clock; (2) the walk error, which is an error of the arrival time due to different received power; (3) the aperture jitter (σ_j) which is mainly from the circuits' shot noise and thermal noise; (4) the quantization error (σ_q) and the nonlinearity of the time discriminator such as time-to-digital converter (TDC). The walk error and the nonlinearity of the TDC limit the accuracy of the lidar system, whereas the clock jitter, aperture jitter, and the

quantization error limit the precision.

The aperture jitter (σ_j) can be further expressed as

$$\sigma_j = \frac{0.35}{SNR \cdot BW \cdot \sqrt{N}}, \tag{2.2}$$

where SNR is the signal-to-noise ratio at the receiver frontend, BW is the bandwidth of the receiver, and $\sqrt{N}$ is the averaging factor of how many pulses are collected for averaging. With considering all the major error sources, the precision (σ_d) of the pulsed lidar can be depicted as

$$\sigma_d = c \times \frac{\sqrt{\sigma_{clk}^2 + \sigma_j^2 + \sigma_q^2}}{2}. \tag{2.3}$$

Considering the quantization noise of the TDC, high precision TDCs have been published, such as measuring the delay difference by using Vernier delay line with two delay buffer chains [24]; however, the hardware complexity grows exponentially with a wider dynamic range. The TDC in [25] utilizes successive approximation to achieve ps-precision in a wide dynamic range. Still, ps-precision is not sufficient for sub-100μm precision since 1-ps temporal precision corresponds to 150 μm. Delta-sigma TDC [26, 27] would be a choice to reach sub-picosecond temporal precision. Unfortunately, it is not suitable for the pulsed lidar with one-shot measurement since it relies on the memory of the previous quantization error and oversampling to suppress the in-band noise.

For a conventional pulsed lidar with a typical receiver bandwidth smaller than 500 MHz [28–30] even with high SNR as 40 dB, the aperture jitter would still contribute 7-ps rms jitter which corresponds to 1-mm precision. One solution to suppress the aperture jitter is to increase the averaging factor (N), but it directly trades off with the acquisition speed. The sampling rate has to drop to 1/4 of the original speed to reduce the aperture jitter by half. Another possible way is to increase the receiver's bandwidth so that the incoming signal would have a sharper transition edge. The slope of the transition is inversely proportional to the bandwidth; however, the noise bandwidth also increases proportionally, and SNR drops

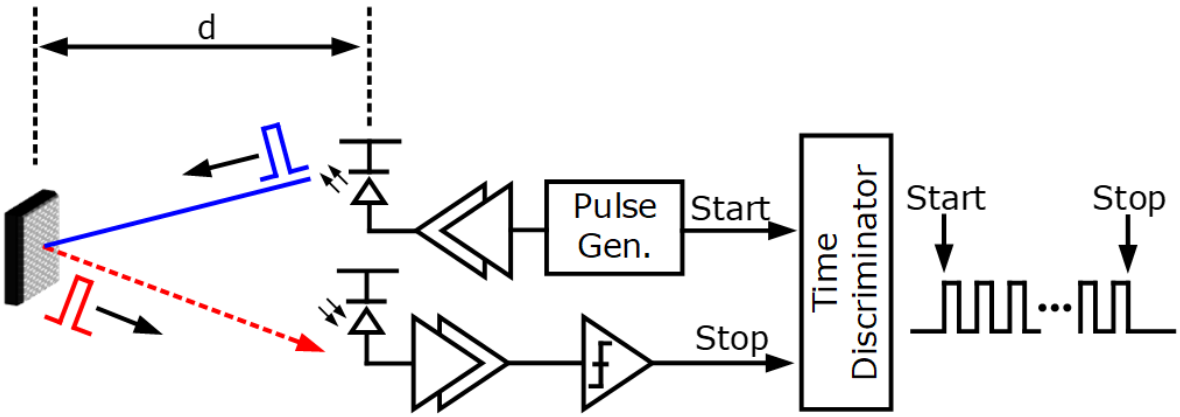

Figure 2.1: Pulsed lidar detection principle.

by a factor of $1/\sqrt{BW}$. Therefore, increasing the receiver's bandwidth does not directly lead to improve accuracy.

Besides the limited precision, the performance of the pulsed lidar also suffers from the walk error. The delay dependence on the input signal strength can be calibrated with a large lookup table. However, the table is susceptible to the environment, resulting in inaccurate measurement results. In [29], a high-pass timing discriminator compensates the dc offset. [30–32] use a high pass filter to convert the pulse to bipolar pulse and define the crossing point as the arrival time. Finding the slew rate with dual-threshold detection [33] has also been used to extrapolate the arrival time. Overall, the walk error limits the accuracy to a few millimeters accuracy with the first-order compensation.

To improve the accuracy, [34–37] introduce indirect ToF measurement which uses multiple integrate-and-dump integrators in different time frames to interpolate the actual arrival time. It can achieve sub-100μm precision. Still, additional skew calibration for the integration start and stop time has to be done before the operation, and the linearity is not sustainable for a wide dynamic range.

2.2 Phase-based Lidar

Another indirect ToF measurement is called phase detection. The approach is often referred to as coherent detection, but the term can be overloaded and hence is avoided in this dissertation. The transceiver architecture is shown in Fig. 2.2. The transmitter sends a continuous sine wave at a carrier frequency f_{ref}, a phase detector then detects the phase shift ($\Delta\phi_{ref}$) of the received signal. The measured distance (d) can be calculated as

$$d = c \times \frac{(\Delta\phi_{ref}/2\pi) \times T_{ref}}{2}, \tag{2.4}$$

where T_{ref} is a period of the carrier, $1/f_{ref}$. The phase detection can be either in optical domain which is known as interferometry [38–45], or in electrical domain by amplitude-modulated continuous-wave (AMCW) [46–50]. Comparing to the pulsed lidar, the aperture jitter in phase detection is

$$\sigma_j = \frac{1}{2\pi f_{ref} \cdot SNR}, \tag{2.5}$$

which indicates that the slope of the signal at the zero-crossing point can be decoupled from the receiver's bandwidth with a narrowband filter. Therefore the phase lidar can achieve higher precision by shifting the carrier to higher frequency with a constant bandwidth. Furthermore, the walk error is suppressed since the dc component can easily be removed by ac-coupling.

The main challenge of the phase lidar is aliasing. Since the transmitted signal is periodic, the receiver cannot distinguish the difference beyond one carrier period. The common solution to extend the measurable distance is with segmented measurements. In [49, 51], two laser sources at different wavelengths are modulated by electro-optic (EO) modulators separately. One at a high frequency of 10 GHz and another one at 300 MHz. At the receiving end, the circulators and optical filters split the two carriers. The photodiodes and the phase meters then measure the phase shifts at two different modulation frequencies individually. The 300-MHz low modulation frequency measures the full range of distance. Within a 10-GHz period, the high carrier frequency takes over the measurement with higher precision.

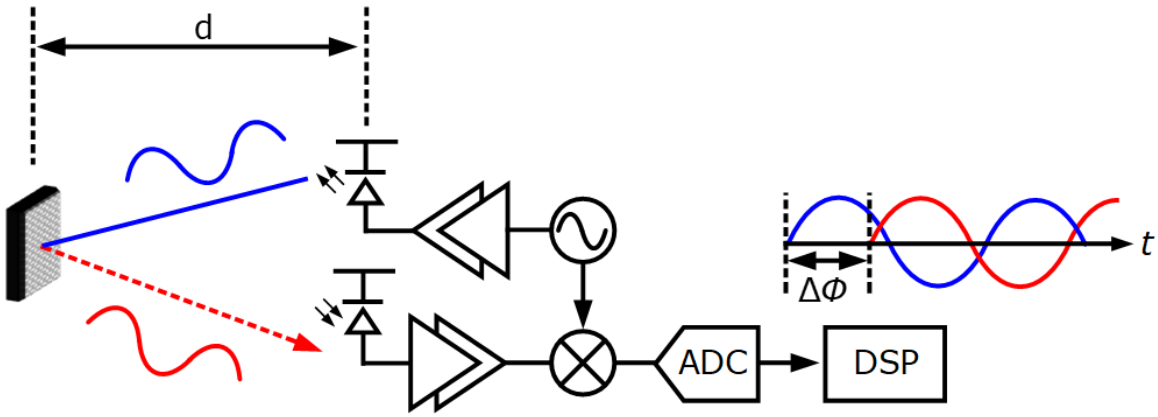

Figure 2.2: Phase-based lidar detection principle.

This segmented detection extends the measurable distance by 32 times. However, the system has several drawbacks: first, with two separate detection paths, the system burns twice the power consumption; secondly, to meet the safety regulation, the peak power is reduced since the transmitter emits two laser carriers at the same time hence limiting the reachable distance; thirdly, the receiver requires two separate paths in the coarse and fine measurements which would then require alignment that is sensitive to the environment.

2.3 Frequency-modulated Continuous-wave Lidar

Frequency-modulated continuous-wave (FMCW) lidar is another common approach to measure the ToF. There are two different frequency modulation schemes. One is to use an arbitrary waveform generator (AWG) to generate a chirp waveform shown in Fig. 2.3. This chirp waveform controls the tunable laser source and modulates the laser wavelength [20,52]. Another way is to perform frequency modulation in the electrical domain and modulate the laser by an EO modulator [53–56]. After the analog-to-digital converter (ADC) samples the received signal, the beat frequency of the transmitted and the echoed signal (Δf) can be found by doing a fast Fourier transform (FFT). The distance information then can be

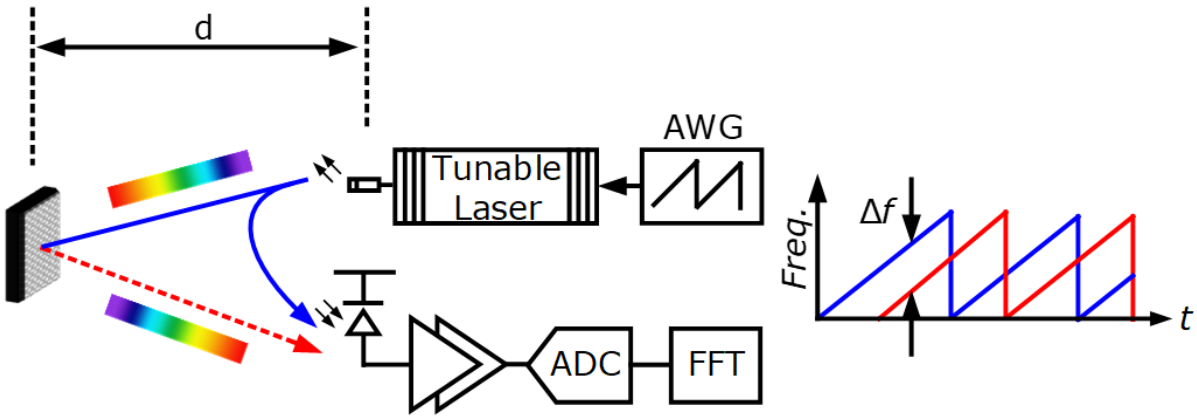

Figure 2.3: FMCW lidar detection principle.

obtained by

$$d = c\frac{\Delta f}{2\gamma}, \tag{2.6}$$

where γ is the slope of the FM chirp. Although FMCW detection can achieve good precision and detect multiple objects simultaneously, it is very challenging to obtain good linearity of the frequency modulation. In [52–55], electro-optic phase-locked loop (EO-PLL) is adopted to linearize the frequency modulation and improve the linearity of the distance measurement; however, it still not sustainable for a wide dynamic range. Furthermore, the accuracy and precision have a direct tradeoff to the resolution bandwidth of the FFT; therefore, the sampling rate is usually below a few hundred kilohertz.

2.4 Design Goal

Fig. 2.4 shows the state-of-the-art lidar systems in terms of the tradeoff between precision and sampling rate. As shown in the chart, the different methods of ranging occupy different portions of the space in the tradeoff. Precision-oriented lidars, which can achieve better than sub-millimeter precision, are mainly based on coherent detection or FMCW detection. Speed-oriented lidars, which can do fast scanning, are primarily implemented in direct ToF detection. The lidars at the top-right corner have better performance in terms of both

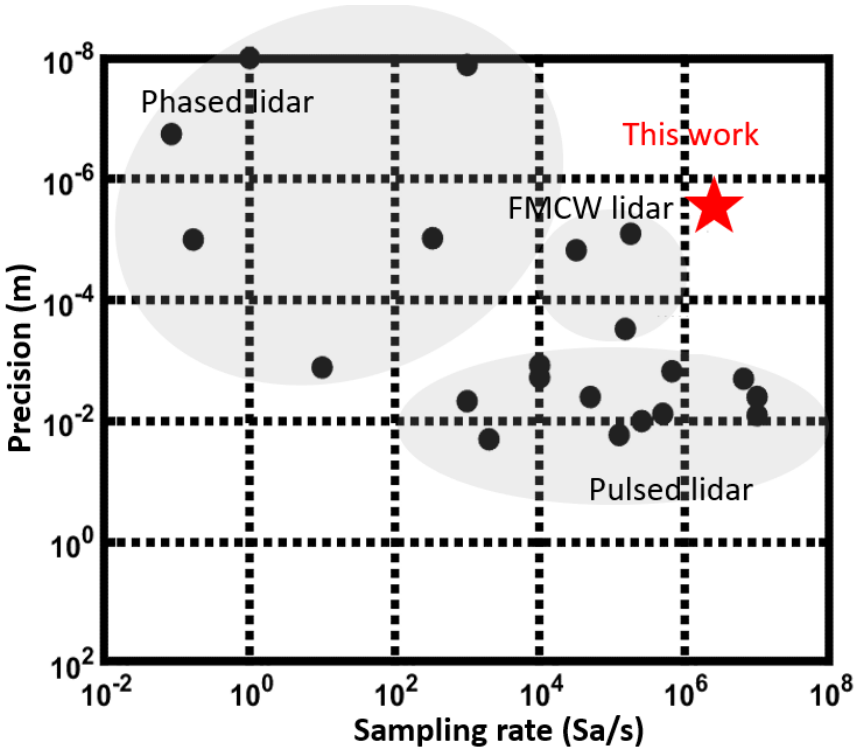

Figure 2.4: Design goal and the state-of-the art lidar systems.

precision and speed. The potential of a high sampling rate and high-precision system extends the use of lidars to applications such as biometrics and manufacturing quality assessment. In this thesis, our design goal is to develop a lidar system that can achieve high precision ($<$10 μm) while keeping the fast scanning speed ($>$1 MHz).

CHAPTER 3

Pulsed-Coherent Lidar

This chapter will first discuss the detection principle of the pulsed-coherent detection and the noise sources in the system. Also, we will discuss the tradeoffs in the design of the modulation scheme. Next, we describe the architecture which includes a transmitter and two types of receivers. Lastly, we estimate the link budget of the system.

3.1 Detection Principle

The idea of pulsed-coherent detection is to combine the advantages of both direct ToF detection and phase detection. The pulsed envelope modulation enables the high-speed acquisition, and the coherent phase-detection provides high precision. Fig. 3.1 illustrates the pulsed-coherent waveform. The CW laser source is amplitude modulated by both a high RF carrier (f_{ref}) and a low-frequency pulsed envelope modulation (f_m). To find the ToF, the coarse detection is measured through counting the arrival time of the pulse envelope, and the fine detection is by measuring the phase shift of the RF carrier. The pulsed-coherent detection not only has a better precision-speed tradeoff but also simplifies the optical setup. Comparing to amplitude modulation [49, 51] which uses two laser carriers and two receiving channels, the pulsed-coherent detection only requires a single laser source and a single-channel receiver. Also, the measurable distance can be further extended by increasing optical power and adding more registers to the coarse counter.

Instead of transmitting a single pulsed envelope, the sequence can be encoded with mul-

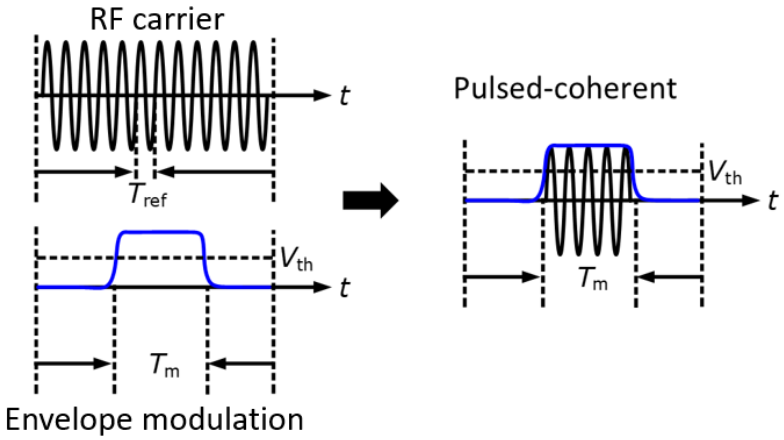

Figure 3.1: Concept of the pulsed-coherent detection.

Figure 3.2: Transmission waveform of the pulsed-coherent system.

tiple pulses and averaged for higher precision. Fig. 3.2 shows an example of the encoded waveform. The carrier frequency is modulated by an 1010... pattern followed by long run zeros. The deadtime (T_{dz}) is a blank period to prevent multiple reflections. Furthermore, if we encode the pulsed envelope by an encrypted code as an identifier, it can avoid interference from multiple transceivers operating at the same time [57].

At the receiving end, the overall ToF (ToF_{all}) is partitioned into three parts as shown in Fig. 3.3. The coarse detection (T_c) is counting the ToF at the envelop modulation rate (f_m). In a modulation period, the intermediate stage (T_i) counts at a rate of the carrier frequency (f_{ref}). And the fine detection (T_f) finds the phase shift within a carrier's period ($1/f_{ref}$). The overall time-of-flight is expressed as

$$ToF_{all} = N_1 \frac{1}{f_m} + N_2 \frac{1}{f_{ref}} + \frac{\phi_{ref}}{360^\circ} \frac{1}{f_{ref}}, \tag{3.1}$$

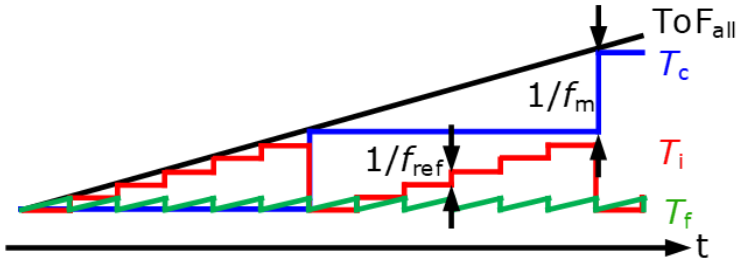

Figure 3.3: Algorithm of the segmented pulsed-coherent detection.

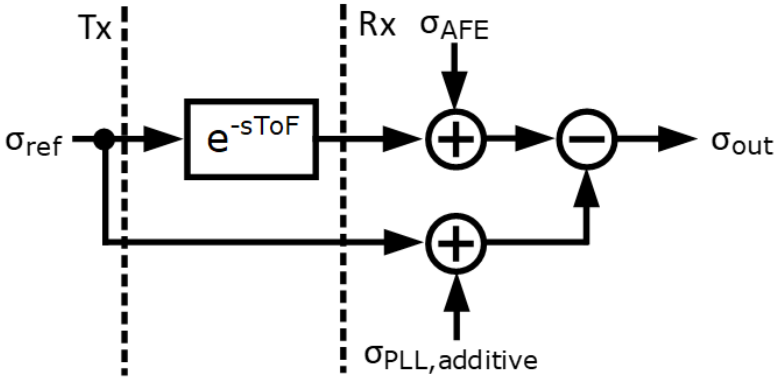

Figure 3.4: Noise model for the phase detection.

where N_1 and N_2 are the counts of the counters, and ϕ_{ref} is the phase shift of the RF carrier.

3.2 Noise Analysis

To estimate the system's performance, we use a simplified noise model of the coherent detection shown in Fig. 3.4 which illustrates the dominant noise sources. The main noise sources are from the reference clock for the phase detection (σ_{clk}), and from the receiver's analog frontend (σ_{AFE}) including the shot noise of the photodiode and the thermal noise from both the photodiode and the analog frontend circuit.

3.2.1 Clock Noise

The clock noise, σ_{clk}, includes correlated and uncorrelated noise. The phase noise of the reference clock, σ_{ref}, is a correlated noise source since it is used to synchronize both the transmitter and the receiver. The uncorrelated noise is primarily from the additive noise from the local oscillator (LO) generation, which is typically from a phase-locked loop, ($\sigma_{PLL,additive}$).

The ToF delay is e^{-sToF} in s-domain. A phase detector compares the phase to the reference by down-converting the carrier to dc. Assuming that the reference clock of the transceiver is $V_1 cos(\omega t + \phi_1)$ and the received signal is $V_2 cos(\omega t + \phi_1 + \Delta\phi)$, the output with a low-pass filter can be expressed as $0.5 V_1 V_2 cos(\Delta\phi)$ which indicates that the phase is subtracted at the output. The output noise of the correlated noise can then be modeled as

$$\sigma_{out,ref}^2 = \sigma_{ref}^2 \times |1 - e^{-sToF}|^2, \tag{3.2}$$

which shows a high-pass response due to the noise filtering. Fig. 3.5(a) shows the phase noise of the reference filtered by different time-of-flights from 1 ns to 1000 ns.

The noise characteristic of the LO generation varies between architectures, here we assume that the LO generation is a conventional PLL. The main noise sources are from the phase-frequency detector (PFD), the charge pump (CP), and the voltage-control oscillator (OSC). Fig. 3.5(b) shows the additive noise from the PLL with different integration bandwidths from 1-kHz frequency offset. The in-band noise is primarily contributed from the PFD and the CP where the VCO's phase noise is the dominant noise source out of band. The output rms jitter, ($\sigma_{j,out}$), can be expressed as

$$\sigma_{j,out}^2 = \sigma_{ref}^2 \times |1 - e^{-sToF}|^2 + \sigma_{AFE}^2 + \sigma_{PLL,additive}^2, \tag{3.3}$$

and the precision in terms of distance, σ_d, is scaled by the speed of light

$$\sigma_d = \frac{c}{2} \cdot \sigma_{j,out}. \tag{3.4}$$

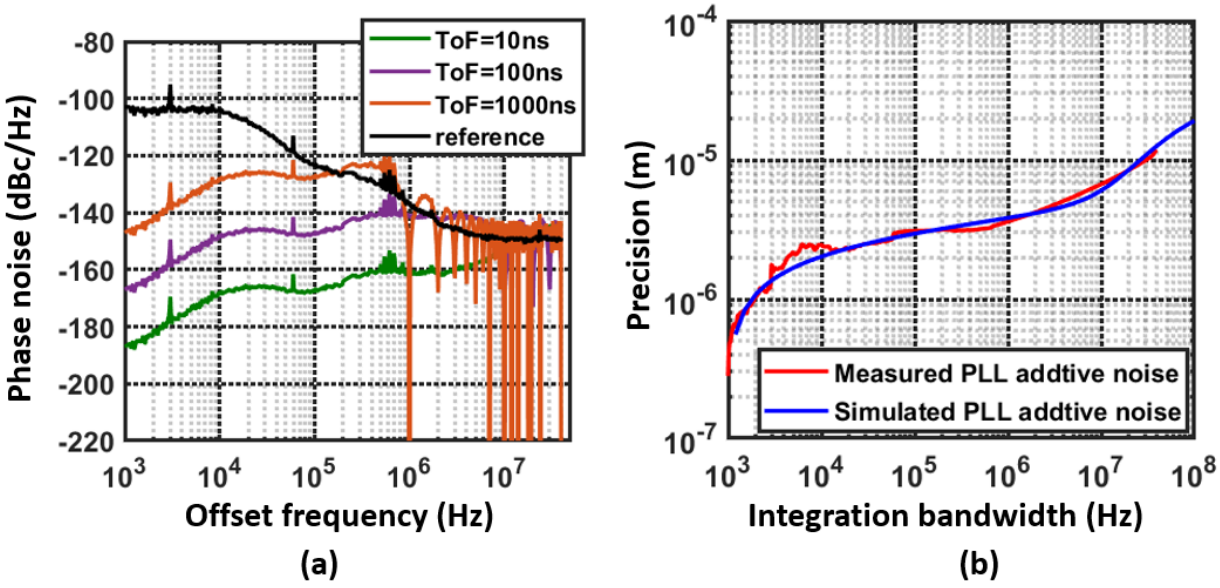

Figure 3.5: (a) Phase noise of the reference clock at the transmitting end and the receiving end, and (b) the noise contribution from the additive noise of the LO generation.

3.2.2 Analog Frontend Noise

Fig. 3.6 shows the noise model of the analog frontend (AFE). The diode's model consists of a signal's current (i_{sig}), a dark current (i_{dark}), and parasitic resistance (R_s) and capacitance (C_{pd}). A matching network performs the impedance matching of the photodiode and the AFE circuit with a noise factor of F. The AFE noise (σ_{AFE}) is

$$\sigma_{AFE}^2 = \left(\frac{1}{2\pi f_{ref}} \frac{1}{SNR}\right)^2, \tag{3.5}$$

where the signal-to-noise ratio (SNR) is

$$SNR = \sqrt{\frac{i_{sig}^2}{i_{n,in}^2 \times BW}}, \tag{3.6}$$

where $i_{n,in}$ is the total input-referred noise, and BW is the integration bandwidth of the receiver. The total noise includes two parts. First, the shot noise of the photodiode includes the dark current, expressed as $i_{s,d}$ in the equation

$$i_{s,d}^2 = 2qi_{dark}, \tag{3.7}$$

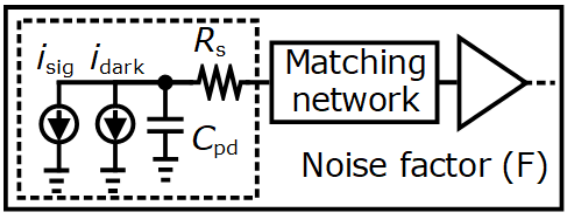

Figure 3.6: AFE noise model.

and the signal current, expressed as $i_{s,s}$ in the equation

$$i_{s,s}^2 = 2qi_{sig}, \tag{3.8}$$

where q is the electric charge $1.6e^{-19}$. Second is the thermal noise from the photodiode's parasitic resistance and the noise from the amplifiers. With a narrowband matching network, the analysis in [58–60] indicates that the thermal noise current, i_{th}, is

$$i_{th}^2 = 4KT(2\pi f_{ref} C_{pd})^2 R_s F, \tag{3.9}$$

where K is Boltzmann constant $1.380649 \times 10^{-23} J \cdot K^{-1}$, and T is the temperature in Kelvin. The concept of the narrowband optical receiver has been widely used in radio-in-fiber (RFoF) communication [61–65] but it hasn't been utilized in lidar to improve the noise performance. Combining Eq. 3.2.2 - Eq. 3.9, we obtain an overall total noise equation for the AFE,

$$\sigma_{AFE}^2 = \frac{1}{4\pi^2}\frac{BW}{i_{sig}^2}\frac{i_{n,in}^2}{f_{ref}^2} = \frac{1}{4\pi^2}\frac{BW}{i_{sig}^2}\left(\frac{2q(i_{dark}+i_{sig})}{f_{ref}^2} + 4KT(2\pi C_{pd})^2 R_s F\right). \tag{3.10}$$

Fig. 3.7 shows the precision considering the AFE noise versus the carrier frequency (f_{ref}) with the received current swept from 100 nA to 1 mA. Here, we use actual photodiode characteristics of which noise factor (F) is 2, parasitic resistance (R_s) is 10 Ω , parasitic capacitance (C_{pd}) is 100 fF, dark current (i_{dark}) is 400 pA, and the integration bandwidth (BW) is 1 MHz. This result indicates that: (1) the shot noise is inversely proportional to the carrier frequency, and (2) the thermal noise is independent of the carrier frequency. The shot noise limits the noise floor at low carrier frequencies where the thermal noise is dominant at high carrier frequencies.

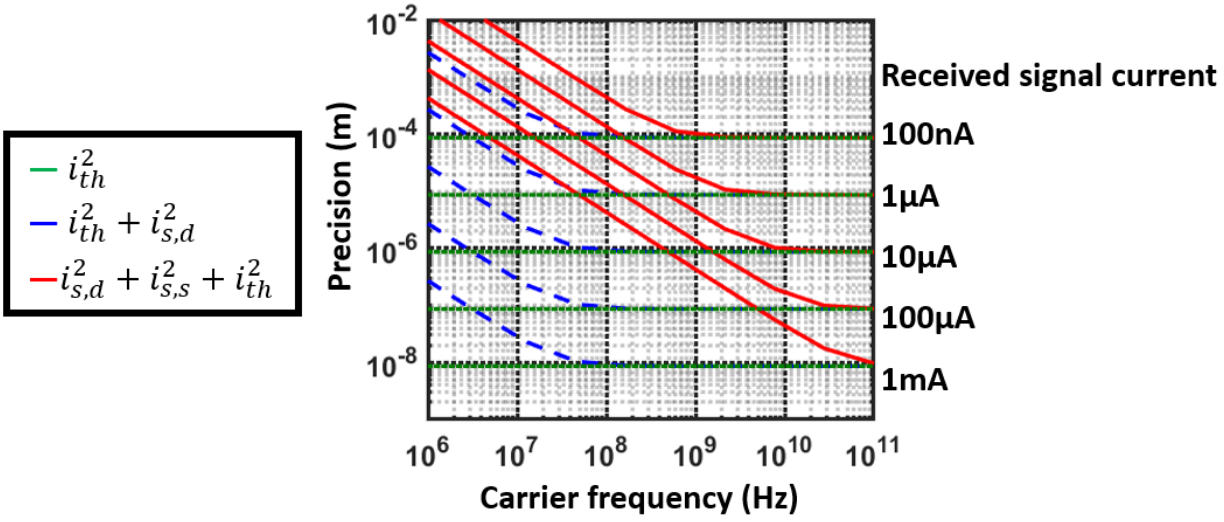

Figure 3.7: Comparison of the precision versus different RF carrier frequencies.

3.2.3 Noise Limitation

When considering both the AFE noise and the clock jitter, Fig. 3.8 shows the precision versus the carrier frequency with constant AFE noise and clock jitter in the range of 10 fs to 1 ps. The noise floor at a high carrier frequency is either dominated by the AFE's thermal noise or the clock jitter, whichever is higher. From Fig. 3.7 and Fig. 3.8, we can determine the noise budget of the lidar system. To achieve better than 10-μm precision, the clock jitter should be <100 fs with 1-MHz integration bandwidth and the carrier frequency >10 GHz to suppress the shot noise.

By using an ADC to measure the phase shift, we also have to consider the quantization error. Fig. 3.9 shows the tradeoff between the effective number of bits (ENOB) requirement and the carrier frequency. For a 10-GHz carrier, 7-bit ENOB is sufficient.

Fig. 3.10 shows the precision and integration bandwidth with varying ToF. We first consider the noise from the clock, including reference clock noise and the PLL's additive noise. Since the transfer function of the reference clock is a high-pass response where the corner frequency is at 1/ToF, the noise contributed from the reference clock is negligible

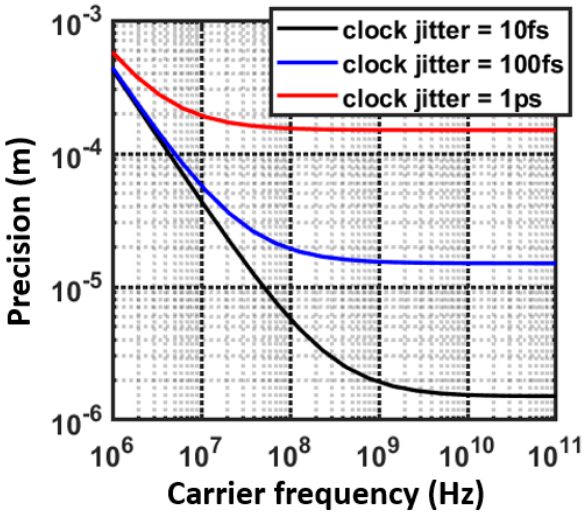

Figure 3.8: Precision performance versus the carrier frequency with different clock jitters.

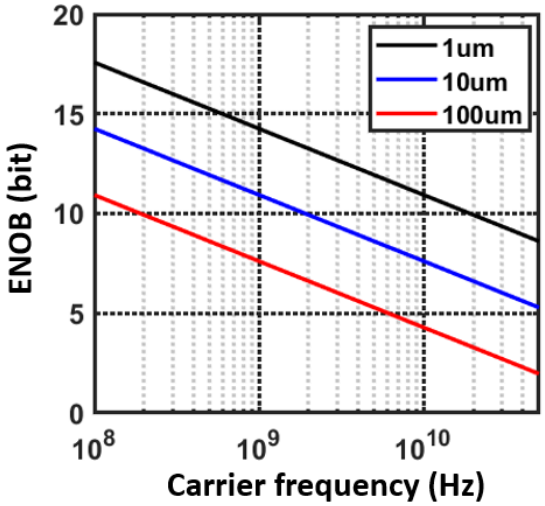

Figure 3.9: ADC's ENOB requirement versus the carrier frequency for the targeted precision.

for a short distance with ToF $<$ 200 ns. When the ToF $>$ 200 ns, the reference clock noise gradually becomes comparable to the PLL's additive noise. Calculating the distance from Eq. 2.1, the 200-ns ToF corresponds to a 30-m distance. There are additional system-dependent factors that contribute to the actual range, such as the internal fiber length in the erbium-doped fiber amplifier (EDFA), which causes latency and the noise of the PLL's

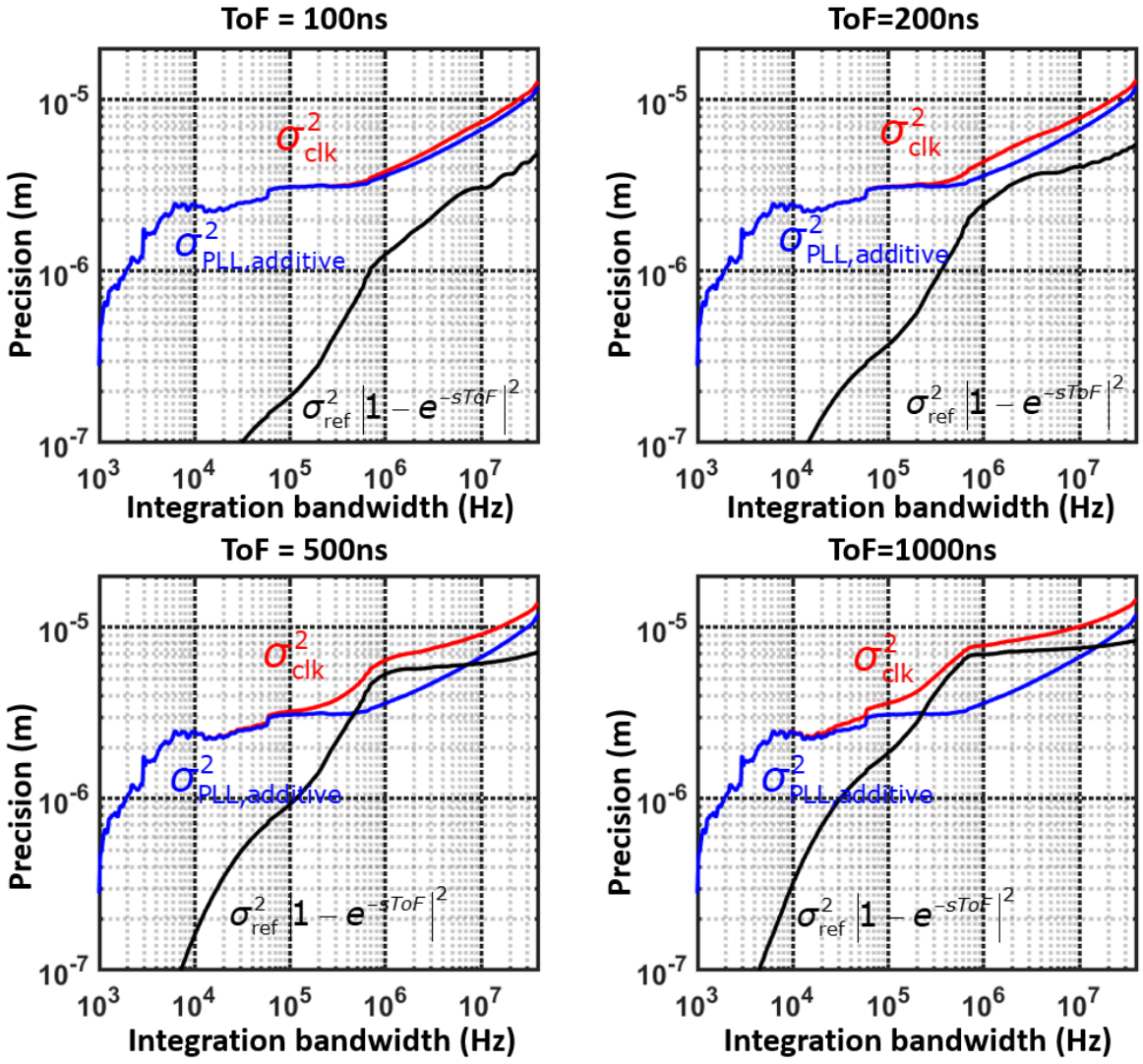

Figure 3.10: Precision versus integration bandwidth with 100-ns, 200-ns, 500-ns, and 1000-ns time-of-flight.

additive noise.

Fig. 3.11 includes the AFE's noise at different SNR conditions. The plot shows the results of varying input currents from 1 μA to 8 μA which covers a dynamic range of 18 dB. For a 1-MHz integration bandwidth target, the AFE's noise is dominant when the SNR $<$ 50 dB. As the input power increase, the clock noise becomes the limiting factor. This plot indicates

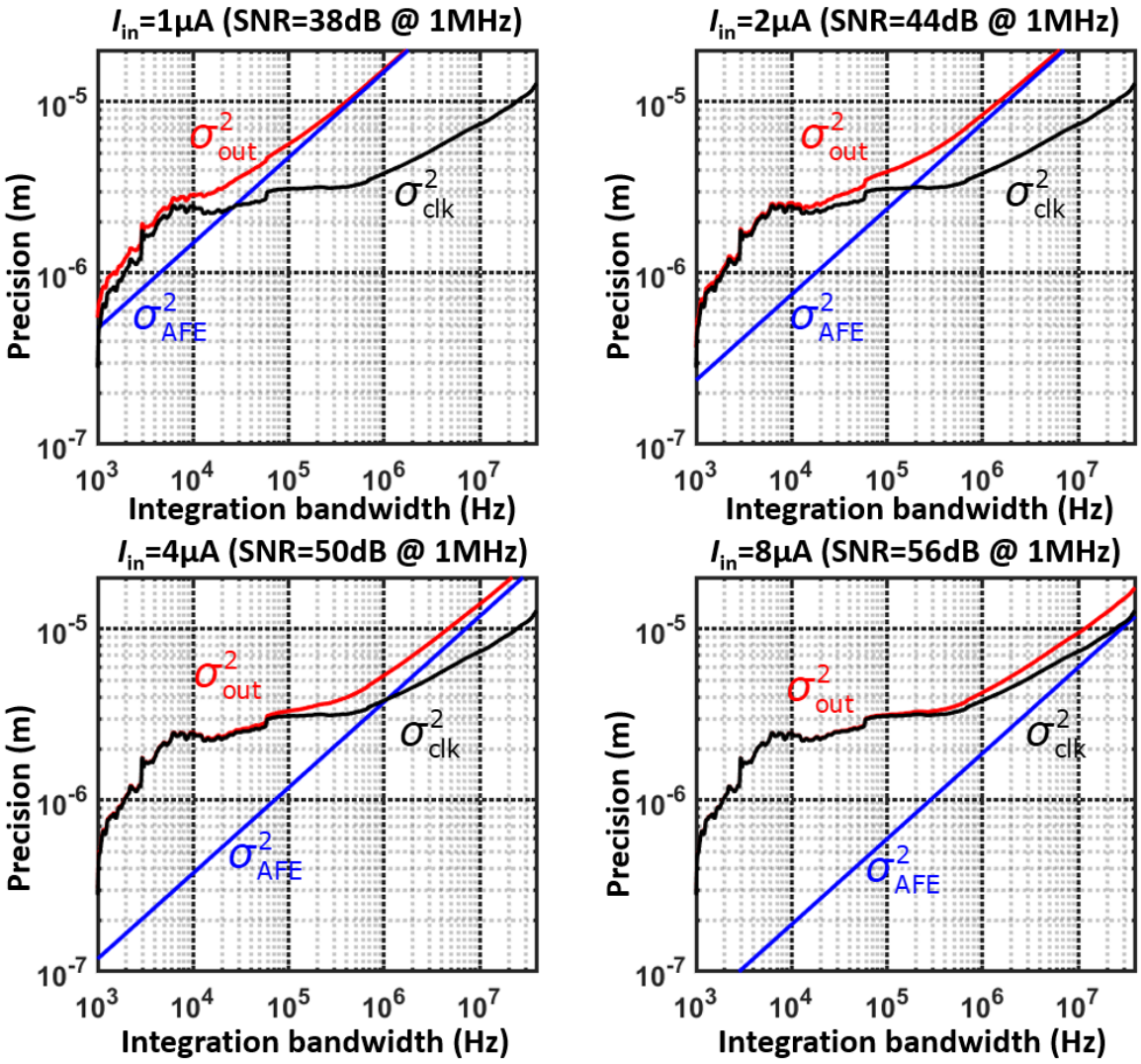

Figure 3.11: Precision versus integration bandwidth with input signal-to-noise ratio of 38 dB, 44 dB, 50 dB, and 56 dB.

that both the high-quality clock generation with low phase noise and the low-noise analog frontend are essential to the precision of the system.

3.2.4 Optic System Consideration

In the analysis so far, we only consider the limitation of the electrical system. Note that the input signal power is determined by the optical setup, particularly the receiver frontend's focal lens. Different optical setups would lead to different choices of photodiodes.

In one scenario, assuming that the lens can focus the light to an area smaller than any given photodiode, the input power is then constant regarding the active area of the photodiode. According to Eq. 3.10, the AFE noise is proportional to the size of the photodiode, A_{pd}, since

$$\sigma_{AFE}^2 \propto \frac{C_{pd}^2 R_s}{i_{sig}^2}, \tag{3.11}$$

where the $C_{pd} \propto A_{pd}$ and $R_s \propto 1/A_{pd}$. Therefore, a smaller photodiode is desired to minimize the AFE noise. The simulation results are shown in Fig. 3.12(a). At high carrier frequency, the noise floor shifts lower with a smaller photodiode.

In a different, more common scenario, because beam divergence, unfortunately, trades with the depth-of-the-view. For any application that requires a wide dynamic range of the depth-of-the-view, the beamwidth of the returned signal is usually larger than the diameter of the photodiode. This is especially the case for the high-speed p-i-n photodiode which has a small aperture. A larger active area is then desired since the signal current (i_{sig}) is increased with a larger aperture. Fig. 3.12(b) shows the simulation results when the input power is proportional to the active area of the photodiode. Here, we show another advantage of the narrowband pulsed-coherent lidar over the broadband design. For the conventional pulsed lidar with a broadband termination, the bandwidth limits the size of the photodiode by the RC time constant. The pulsed-coherent lidar, on the contrary, provides the flexibility of the photodiode's selection to optimize the noise performance since we can customize the matching network according to the different photodiodes.

Besides the electrical receiver limitation, a chip-scale frequency comb [66–70] can be integrated into the system to purify the phase noise of the reference clock. Moreover, the

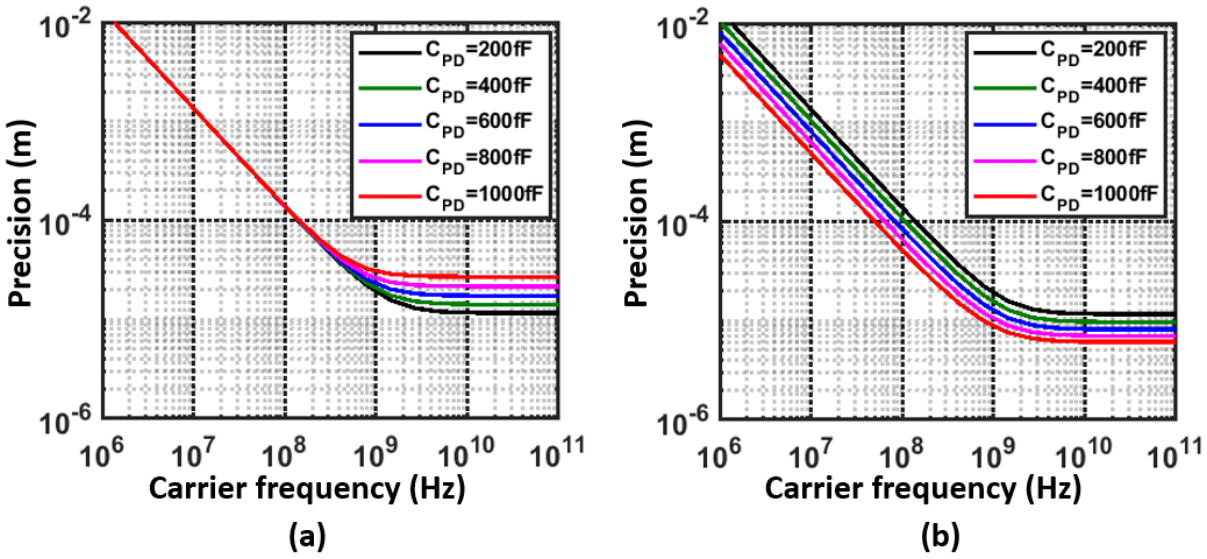

Figure 3.12: Precision versus carrier frequency assuming: (a) input power is constant with different active area of the photodiode, and (b) input power is proportional to the active area of the photodiode.

frequency comb can be used for parallel scanning [71, 72]. The spectral comb teeth enable parallelism, which can improve the sampling rate.

3.3 Architecture

This section describes each of the two primary elements of a lidar system, the transmitter and the receiver. This dissertation explores two different receiver designs which are described in greater detail in 3.3.3 (an analog receiver) and 3.3.4 (a DSP-based receiver).

3.3.1 Transmitter

The fundamental building blocks of the pulsed-coherent lidar transmitter are shown in Fig. 3.13. We design the laser wavelength at 1550 nm cascaded with two EO modulators (EOMs) to perform both RF modulation and envelope modulation. The first EO modula-

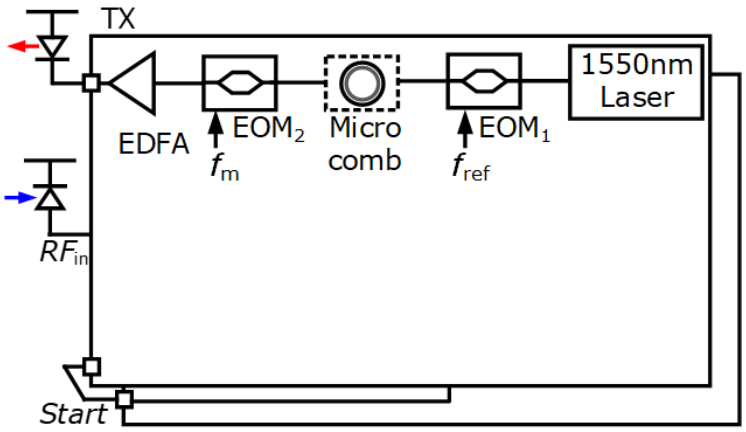

Figure 3.13: Pulsed-coherent lidar transmitter with CW laser source, two EO modulators and and EDFA.

tor is modulated by the RF carrier (f_{ref}), and a pulse-generator modulates the second EO modulator at a lower rate of f_m. An erbium-doped fiber amplifier (EDFA) then amplifies and sends out the amplitude-modulated signal. To achieve precision better than 10 μm and use an ADC with a reasonable ENOB around 8-9 bit as the phase detector, we design the RF carrier at 19 GHz. The low-frequency envelope modulation is designed at 148 MHz ($1/128 f_{ref}$) so that the low-frequency modulation handles around the 8-9 bit range. For the precision of the low-frequency modulation, the last two significant bits overlap with the fine detection to manage the handover between the segmented detection. To further improve the performance, a chip-scale frequency comb [67] can be inserted between the EO modulators to further filter the phase noise of the RF reference clock.

3.3.2 Receiver

Fig. 3.14 illustrates the essential building blocks of a pulsed-coherent lidar receiver. A variable-gain AFE accurately controls the amplitude of the received signals. This variable-gain AFE further helps reduce complexity and maintain the linearity toward accurate fine detection. To measure the envelope's edge, the variable-gain AFE's output (V_{env}) is fed to a

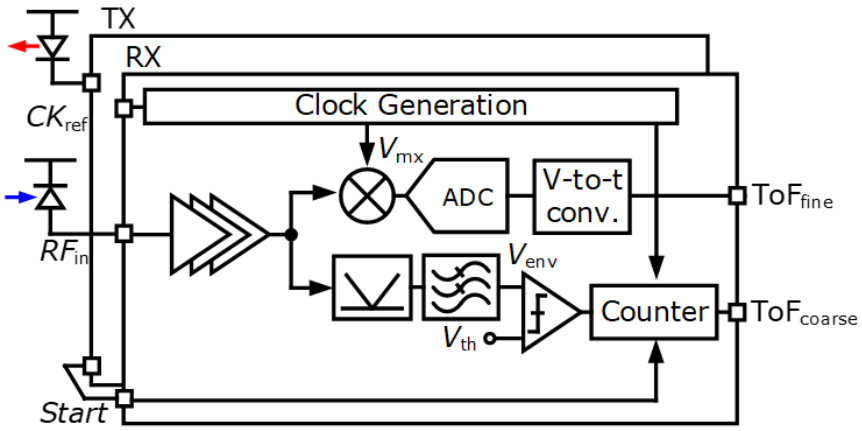

Figure 3.14: Essential building blocks of the pulsed-coherent receiver.

power detector before the counter. The counter starts the counting from a synchronized start signal ($Start$) and stops when the envelope's edge across the comparator's threshold (V_{th}). The count is recorded as coarse ToF (ToF_{coarse}). A phase detector and an ADC measure the coherent phase. The ADC converts the phase information to the voltage domain, then a voltage-to-time (V-to-t) converter calculates the fine ToF (ToF_{fine}). A clock generation provides reference clocks for LO of the phase detector, the sampling clock of the ADC, and the clock for counting the ToF.

3.3.3 Analog-based Receiver

If we consider the input power, the envelop detection would have the same walk error problem, just like the pulsed lidar. This walk error is typically at a range of millimeters to centimeters. The fine detection becomes meaningless since the error is larger than a clock period of 19 GHz. The proposed solution is shown in Fig. 3.15 which applies an automatic gain control (AGC) loop to precisely control the amplitude of the received signals [73]. The AGC loop keeps the signal power before the envelope detector constant and linear. After the loop is settled, we take the sample to measure the fine ToF, and a track-and-hold (T/H) switch breaks the AGC loop, and the comparator waits for the pulse's edge. Instead of

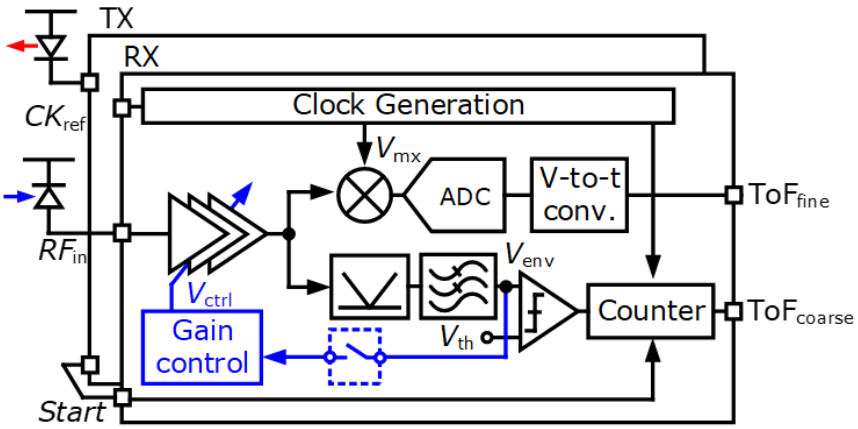

Figure 3.15: Analog-based receiver with AGC loop.

measuring the rising edge for the coarse ToF, we now detect the falling edge of the envelope whose amplitude is fixed regardless of the input signal strength. With this AGC loop, the walk error can now be suppressed within one clock cycle, and the fine detection takes over the measurement within a cycle.

This analog-based receiver design is challenging since: (1) the clock generation must provide a low noise reference for the coherent fine detection; (2) tuning the gain of the amplifiers inevitably introduces the phase shift and hence, we have to reduce the cost of the gain tuning with amplifiers that are phase-invariant; and (3) the AGC loop should react quickly to preserve the advantage of the fast sampling rate.

Since the phase shift is proportional to the operating frequency [74], it is more difficult to maintain the phase-invariant at high carrier frequencies. A practical solution is to down-convert and segment the gain tuning to ease the amplifier's design. Fig. 3.16 shows the architecture of the segmented down-conversion. The gain tuning is partitioned into the coarse and the fine stages where the RF variable-gain amplifier only handles 1-bit discrete coarse tuning. This arrangement lowers the occupied area, power consumption, and phase variation.

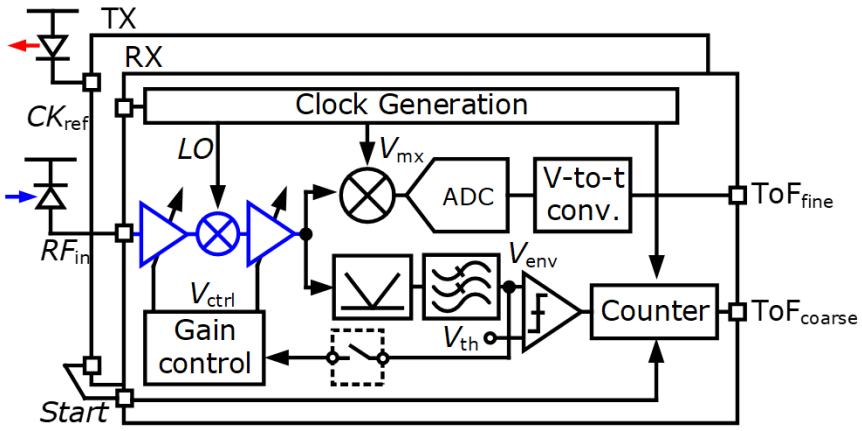

Figure 3.16: Segmented down-conversion.

3.3.4 DSP-based Receiver

Although the analog-based pulsed-coherent receiver can achieve high precision with a high sampling rate, the system is sensitive to the environment. The alignment is susceptible to the PVT variation hence needs to be closely monitored. Moreover, the coarse and fine detection alignment must be calibrated before the normal operation to be able to combine the segmented results.

Instead of finding the coarse ToF and the fine ToF separately in the analog-based receiver, an enhancement is to use a DSP-based receiver as shown in Fig. 3.17 then combines two detectors into one. An ADC samples the IF signal, and a digital signal processor (DSP) post-processes both the coarse ToF and the fine ToF in the digital domain. The pulsed modulation is oversampled by the ADC hence can be reconstructed in the digital domain. The AGC loop becomes a digitally controlled loop to adjust the gain of the AFE. A dual-threshold over-range detection of the ADC senses whether the signal is over-range or under-range. This DSP-based receiver improves the sensitivity to PVT variation. It inherently aligns the segmented measurements using the sampling clock as the reference hence achieves better precision at higher sampling rates.

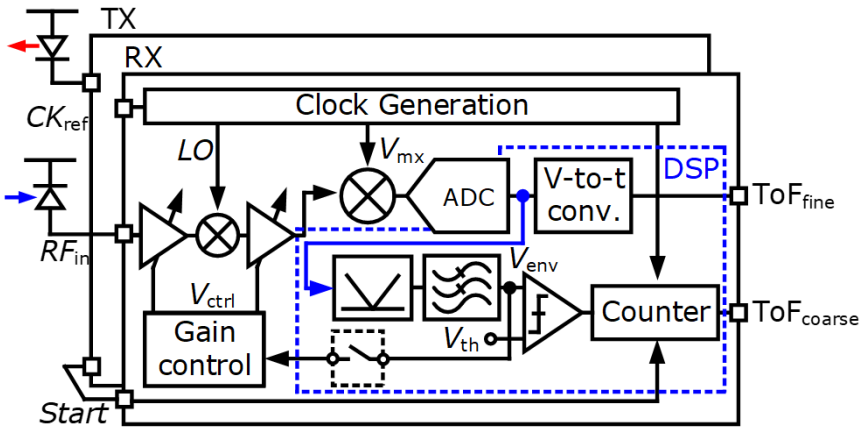

Figure 3.17: DSP-based receiver.

3.3.4.1 Homodyne receiver

The system architecture is shown in Fig. 3.18. The down-conversion reuses the architecture in [73]. A dual-channel ADC directly sub-samples the in-phase and the quadrature-phase IF signals. A 19-GHz reference drives the EO modulator in the transmitter. It also sends to the receiver as the clock input. The dividers and an up-converted mixer synthesize the LO (LO_1). The I/Q mixer down-converts the RF signal to IF centered at the 2^{nd}-order harmonic of the ADC's sampling frequency (CK_s). Two ADCs sub-samples the IF signals and convert them directly to the baseband (BB). It uses a simple LO generation which only has dividers and a mixer to minimize clock jitter. Also, the coarse detection and the fine detection are automatically aligned by the same ADC clock. As will be shown in Section 5.2, measurement results show that this approach leads to a performance improvement as compared to the analog-based receiver.

This homodyne approach of directly down-converting the phase information to baseband has several limitations. First, the crosstalk between the reference clock and the echoed signal at the same frequency lowers the sensitivity and the linearity. Specifically, the reference leaks to the incoming signal path hence introducing an in-band spur. Simultaneously, the received

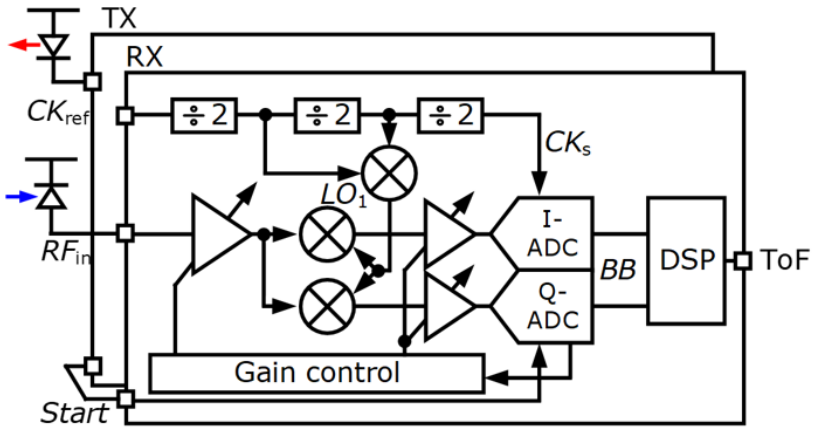

Figure 3.18: DSP-based homodyne receiver.

signals with different power pull the clock phase and cause input-dependent phase shifts; secondly, I/Q IF channels result in needing two high-speed ADCs in order to reconstruct the mask's envelope. The ADCs lead to high power consumption. Additionally, any I/Q mismatch must be calibrated before a ranging acquisition.

3.3.4.2 Heterodyne Receiver

To mitigate the aforementioned coupling and the mismatch issues, we further enhance the architecture with a heterodyne receiver (Fig. 3.19) which takes a lower frequency clock as the reference input and uses a local PLL to generate the LO for the down-conversion mixer. The LO frequency (LO_1) is designed at 17.2 GHz, and the down-converted signal locates at the middle of the ADC's sampling frequency and its Nyquist rate to provide wide bandwidth. After the signal is sampled by the ADC, a complex digital mixer then down-converts the baseband signal (BB_1) to DC (BB_2). More details of the frequency planning will be discussed in Section 4.2.

The low-frequency reference clock reduces the coupling and the pulling between the clock and the echoed signal, and therefore, improves the sensitivity and the linearity. The heterodyne receiver only requires a single channel at IF; thus, the power consumption is

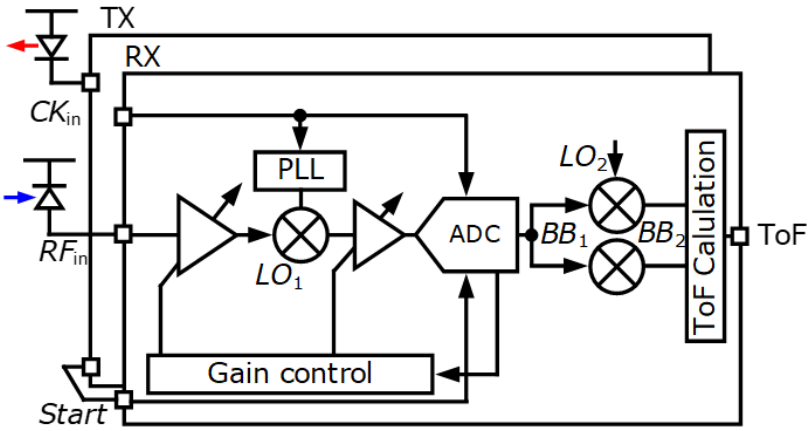

Figure 3.19: DSP-based heterodyne receiver.

reduced, and no I/Q mismatch calibration is needed.

There are two main challenges in the receiver design: first is to keep the PLL phase noise low so that we won't introduce much additive noise to the phase measurement; and second, to operate in a wide dynamic range, a variable-gain amplifier (VGA) is adopted at the frontend so that the signal covers the full dynamic range of the ADC. Since we measure the phase shift of the carrier, similar to the prior architectures, the phase response can not change across different gain settings. Again, a special-purpose phase-invariant amplifier is needed.

3.4 Link Budget

We conclude this chapter with a discussion of the link budget for the pulsed-coherent architecture. The link budget can be estimated as followed: first, from the simplified equation of the lidar link budget [75, 76]

$$P_{rx} = \frac{P_{tx} D_{rx}^2 \rho cos\theta}{4d^2} \eta_{sys} \eta_{atm}, \tag{3.12}$$

where P_{tx} is the transmitted power, D_{rx} is the receiver aperture diameter, ρ is the target reflectance, θ is the incidence angle, d is the distance, η_{sys} is the system transmission factor,

and η_{atm} is the atmosphere transmission factor. The atmosphere transmission factor, η_{atm}, can be calculated as

$$\eta_{atm} = 10^{-2d\alpha/10000}, \tag{3.13}$$

with α as atmospheric attenuation coefficient in dB/km which is 0.2 dB/km for a clear sight and 4 dB/km in a haze condition at 1550-nm wavelength [77].

As specified in safety regulations, the transmitted laser power has been classified into four classes by wavelength according to the damage it can cause. The maximum transmitted power can be calculated depending on the usages and applications.

Converting the optical received power to electrical power through a photodiode with a responsivity, R, the received current can be calculated by

$$i_{sig} = P_{rx} \cdot R. \tag{3.14}$$

The sensitivity of the RF narrowband reciever is

$$P_{Rx} = -174 + NF_{Rx} + SNR_{min} + 10log(\frac{BW}{1Hz}), \tag{3.15}$$

where NF_{Rx} is the noise figure of the receiver, SNR_{min} is the minimum SNR requirement for the targeted precision, and BW is the receiver bandwidth.

Based on the targeted precision, the SNR_{min} can be found by

$$SNR_{dB} = 20log(\frac{1}{2\pi_{ref}\sigma_j}), \tag{3.16}$$

where σ_j is $2\sigma_d/c$. With the information of the received power, the receiver profile, and the SNR requirement, the integration bandwidth then can be determined.

Here, we take facial recognition as an example. To perform a full face scan, the scanned diameter is around 16 cm. Assuming the system is integrated with a micro-electromechanical system (MEMS) mirror with $\pm 5^\circ$ field of view, the distance (d) has to be longer than 1 m. Note that at this distance, the atmosphere loss is negligible. To satisfy the Class 1 laser regulation, the maximum transmitted power is 10 mW at a 1550-nm wavelength. With

P_{rx}	D_{rx}	ρ	P_{tx}	d	θ	η_{atm}	η_{sys}
224nW	3cm	10%	10mW	1m	5°	1	1

Table 3.1: Lidar link parameters.

10-% reflectance of the human skin at 1550 nm [78] and a 3-cm diameter focal lens at the receiving end, we can then calculate the received power of 224 nW. Converting the optical received power to electrical power through a photodiode with 0.9 W/A responsivity, the received current is 200 nA which corresponds to –87 dBm electrical power. The parameters are shown in Table. 3.1.

For a target of 30-μm precision, we can derive the SNR requirement from Eq. 3.16. The SNR_{min} of 32 dB can be obtained with a 20-GHz carrier frequency. With a 5-dB noise figure receiver, we can then derive the integration bandwidth of 100 kHz.

The performance of the architecture is promising but depends on the implementation of the circuit elements. The design of key components are discussed in the next chapter.

CHAPTER 4

System Implementations and Building Blocks

In this chapter, we will discuss the essential building blocks in both the analog-based receiver and the DSP-based receiver. In the analog-based receiver, we will focus on the phase-invariant-amplifiers including the RF amplifier and the IF amplifier, and also the automatic gain control loop to adjust the signal power. Following the phase-invariant amplifier, we then show the circuit implementation of the post-edge detector. In the DSP-based receiver, the input narrowband matching network is implemented to enhance the sensitivity and reduce the input-referred noise. We also propose a discrete-controlled inverter-based phase-invariant programmable gain amplifier for a discrete gain control loop. Lastly, we will describe the LO generation including the choice of the architecture to optimize the noise performance and its building blocks.

4.1 Analog-based Receiver

The receiver architecture is implemented as shown in Fig. 4.1. The AFE provides a 60-dB dynamic range, which consists of a 1-bit phase-invariant variable-gain low-noise amplifier (PI-VGLNA), an I/Q down-conversion mixer, a 1-bit programmable-gain amplifier (PGA), and a VGA with an analog-based automatically gain control. Each amplifier provides a 20-dB gain tuning range. In the clock generation path, we split a portion of the power from a continuous 19-GHz source and divide the clock to provide 14.25-GHz and 4.75-GHz LOs for down-conversion and fine ToF detection. A superharmonic injection-locked multipath ring oscillator (SHIL-MPRO) [79] and up-conversion mixers provide I/Q LOs. The coarse ToF

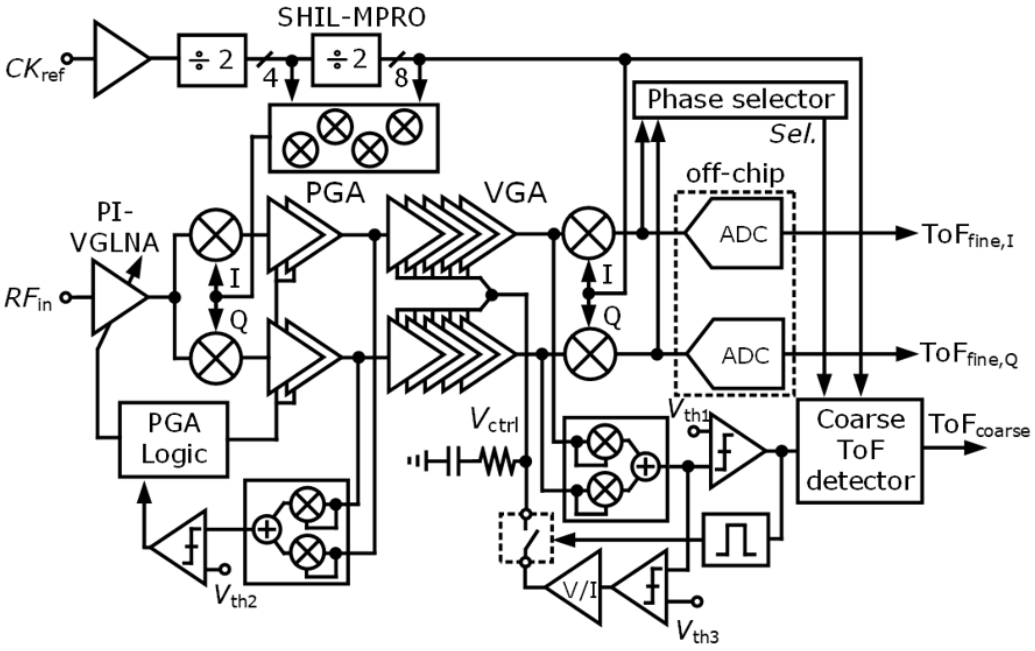

Figure 4.1: System implementation of the analog-based receiver.

detector takes the output from a self-mixing power detector and a signal detector to find the envelope's post-edge transition. For fine ToF detection, two single-sideband (SSB) mixers act as a phase detector. In this prototype, an off-chip ADC then reads out the results.

4.1.1 Phase-invariant Amplifiers

To achieve a wide dynamic range of the input power with high accuracy, the AFE requires a wide gain tuning range and low phase error across different gain settings. The design choices of the gain-controlled circuit are shown in Fig. 4.2. It can be done with passive attenuation [80–84], but it degrades the sensitivity of the receiver if the attenuator is placed at the first stage; another way is to co-design with an active element. A variable-gain amplifier can be implemented, and the gain can be adjusted by either tuning the load impedance or tuning the transconductance. Tuning the load impedance introduces a large phase shift across the gain tuning range since the positions of the poles and zeroes have been changed.

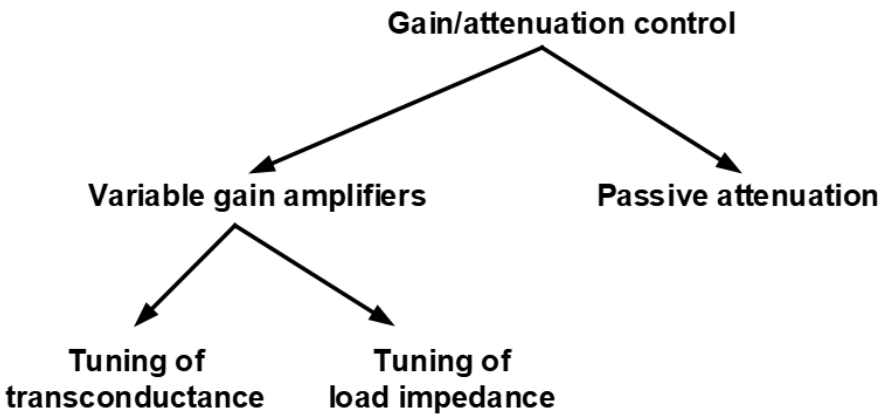

Figure 4.2: Tuning mechanisms of the Variable-gain circuits.

The phase response stays relatively constant by tuning the transconductance of the variable-gain amplifier, therefore achieving phase-invariant response. In [74], a single-ended phase-invariant cascode amplifier has been implemented by tuning the bias voltage of the input common-emitter stage. The first-order phase compensation is done by choosing the emitter's inductance in the common-emitter stage and the base capacitance in the common-base stage to balance the positive and the negative phase variations. It achieves 3° and 6° with 12-dB and 20-dB gain tuning. In [85], a differential two-stage phase-invariant amplifier achieves inherent phase uniformity with source degeneration to compensate for the variation of the parasitic capacitance. This amplifier achieves $< 5°$ phase shift across an 18-dB gain tuning range. In [86], the current-steering gain-tuning topology neutralizes the phase shift formed by the gate-drain capacitors. This amplifier has a 21-dB gain tuning range with only 2° phase shift.

The proposed PI-VGLNA and PGA/VGA are shown in Fig. 4.3(a) and Fig. 4.4(a), respectively. An LNA with a current-steering cascode structure is chosen to stabilize the phase response of the amplifier. A complementary 1-bit digital control tunes the gain via the gate voltage (V_c and V_{cb}) of the transistors in the cascode stage. To further suppress the phase variation, we insert inductors, L_1 and L_2, between the common-source and the

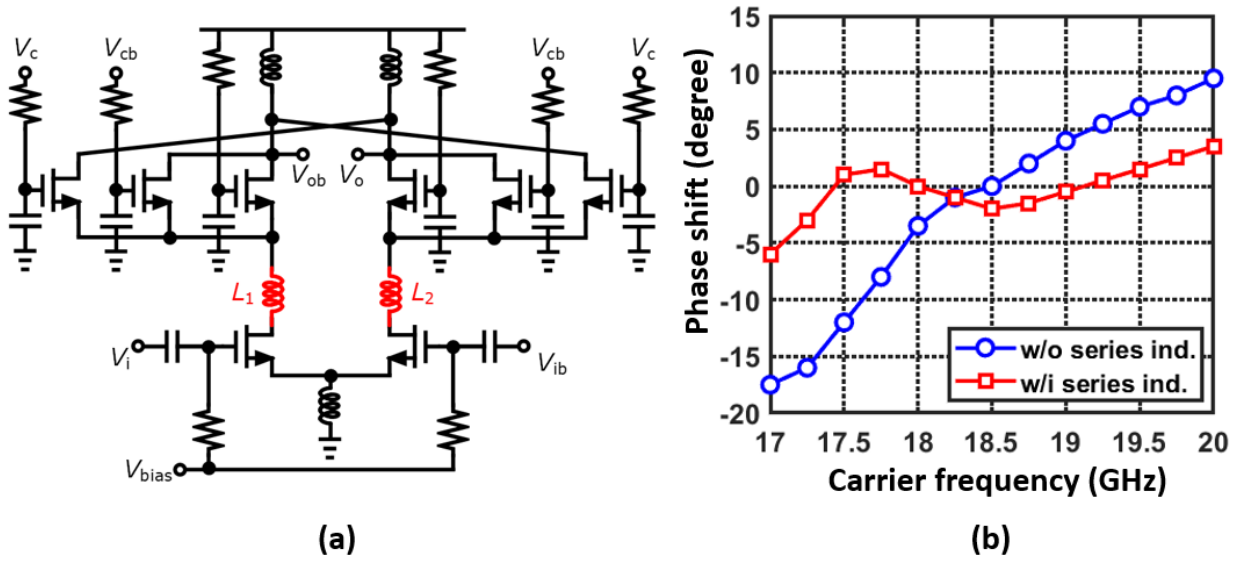

Figure 4.3: (a) Schematic of the phase-invariant programmable-gain low-noise amplifier design, and (b) relative phase shift with 20-dB gain change.

common-gate stages. These inductors not only enhance input-output isolation but also reduce the sensitivity of phase variation. Fig. 4.4(b) shows the comparison with and without the series inductors. The maximum phase deviation across 1-GHz bandwidth centered at 18.5 GHz with 20-dB gain tuning reduces from $\pm 5^\circ$ to $\pm 1^\circ$.

The PGA and the VGA are also implemented in the current-steering structure controlled by single-to-differential voltage-to-current (V/I) converters. Two flying capacitors, C_1 and C_2, introduce a frequency zero to compensate for the phase shift at 4.75 GHz. Fig. 4.4(b) shows the relative gain and phase responses of the VGA. The gain response is linear-in-dB with a 25-dB tuning range with a maximum of 0.5° relative phase shift.

4.1.2 Automatic Gain Control Loop

The design of the AGC loop is shown in Fig. 4.5. The control logic applies segmented control with a 2-bit thermometer digital control and an analog control to prevent a long recovery time from saturation with high input power. We break one loop into two: the discrete AGC

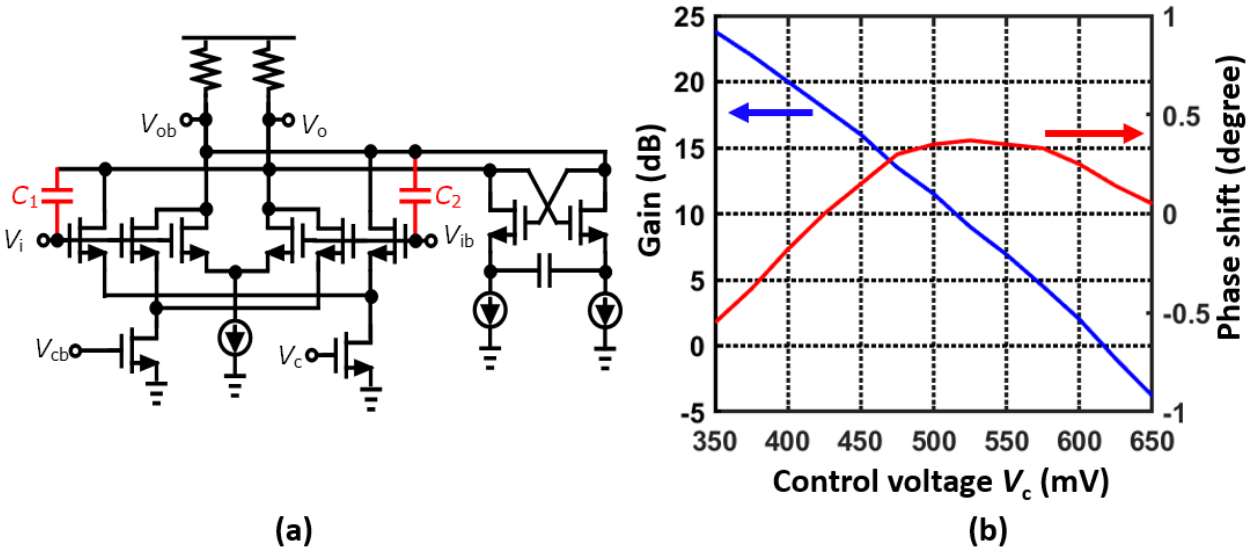

Figure 4.4: (a) Schematic of the phase-invariant programmable-gain amplifier design, and (b) gain and relative phase shift with control voltage sweep.

loop with an over-range detector is shown in blue color, and the analog AGC loop is shown in red color. The discrete loop provides a coarse gain tuning with 1-bit for PI-VGLNA and 1-bit for PGA; each of them has a 20-dB tuning range. The analog loop then provides a fine gain-tuning with a 20-dB dynamic range.

For the analog AGC loop, an envelop detector, described later in this section, captures the magnitude of the signal. The loop starts when the signal is detected by the signal detector with a threshold voltage of V_{th1}. The magnitude then is compared to a target threshold, V_{th3}. The result of the comparison is amplified by a V/I converter which is implemented using a folded-cascode amplifier to provide both high gain and high output impedance. A frequency zero is introduced in the loop filter with 250-MHz loop bandwidth to achieve a fast transient response by a series R-C low-pass filter. A pulse generator after signal detector provides a 4-ns settling window for the AGC loop. A track-and-hold switch holds the control voltage of the VGAs and releases it after detecting the envelope's falling edge.

The power detector is implemented by using a self-mixing mixer with both I/Q channels

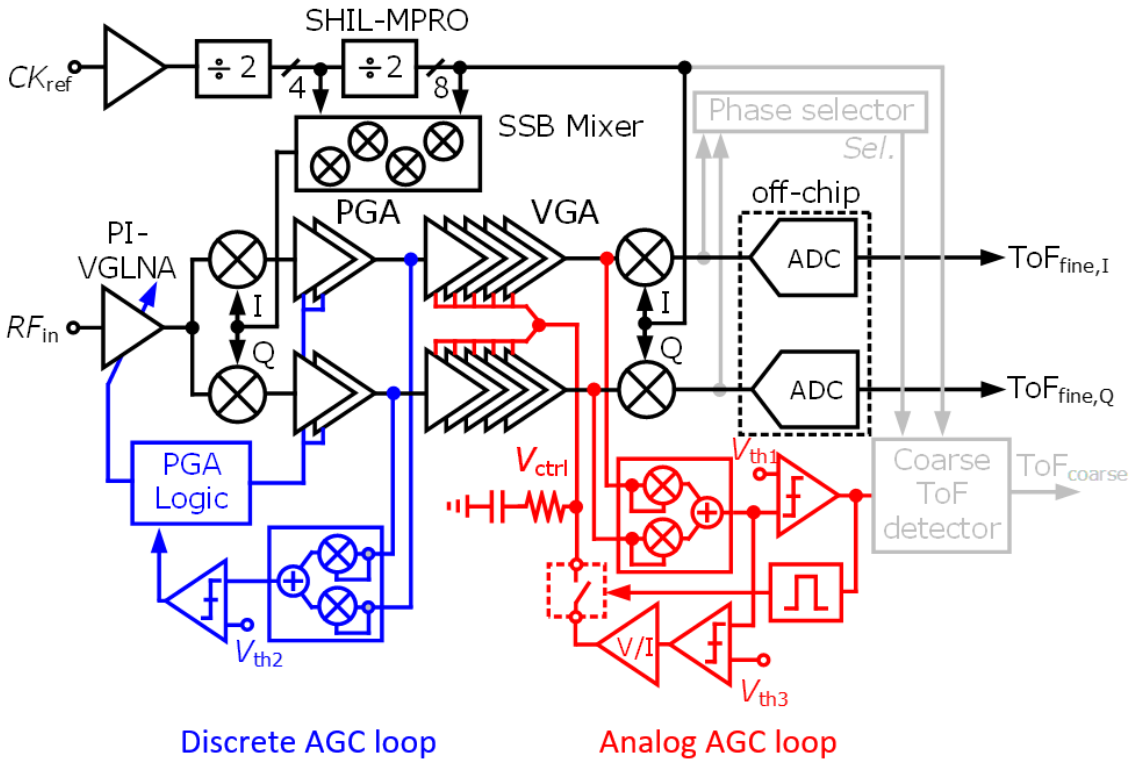

Figure 4.5: Dual automatic gain control loops with a discrete AGC loop and an analog AGC loop.

shown in Fig. 4.6(a). The IF I/Q signals are leveraged to extend the loop bandwidth. The output can be expressed as

$$V_{env} = (V_1 sin\omega t)^2 + (V_1 cos\omega t)^2 = {V_1}^2, \tag{4.1}$$

where $V_1 sin\omega t$ is the input signal. The I/Q self-mixing power detector inherently suppresses the harmonics. In comparison, a single-channel self-mixing power detector as shown in Fig. 4.6(b) leads to an output expression

$$V_{env} = (V_1 sin\omega t)^2 = \frac{{V_1}^2}{2}(1 - cos2\omega t), \tag{4.2}$$

where the signal contains both a DC signal indicating the input power and a 2^{nd}-order harmonic. To suppress the harmonic, a low-pass filter with a bandwidth lower than 2^{nd}-order

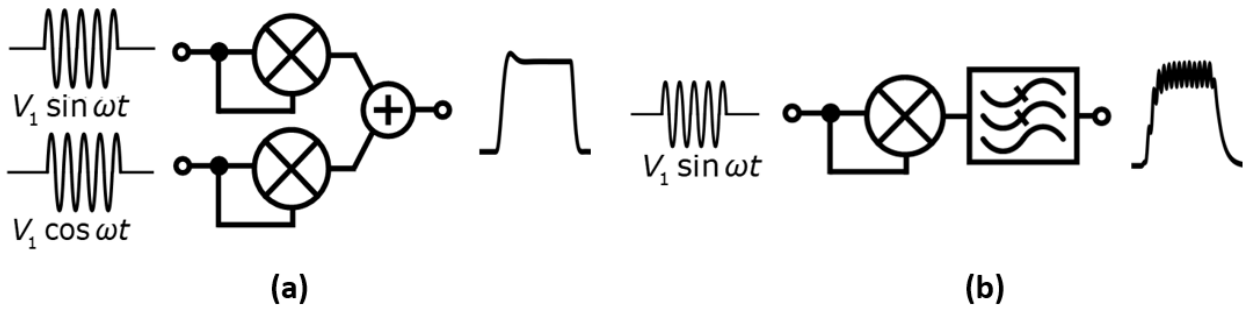

Figure 4.6: (a) Self-mixing power detector design using both I/Q signals, and (b) self-mixing power detector.

harmonic has to be placed after the power detector. For a wideband AGC loop, the low-pass filter degrades the feedback loop's phase margin, thus limiting the AGC's bandwidth. An I/Q-based self-mixer does not suffer from this limitation.

4.1.3 Post-edge Detector

The post-edge coarse ToF detector is illustrated in Fig. 4.7(a). The output of the power detector is filtered prior to counting. Since the AGC loop has a small amount of input-dependent gain error, the filter has a small degree of adjustability to compensate for the phase shift that results. Varactors are adjusted according to the control voltage (V_{ctrl}) of the AGC loop as a signal strength indicator to adjust the transition time. The filter is followed by an 8-way time-interleaved sampler, an 8-to-16 demultiplexer, and XOR gates to detect the transition time at low rates accurately. The 8-way interleaved sampler provides the effectively 19-GHz sampling clock to count the coarse ToF. To avoid metastability, a phase-selector selects 0° or 180° of the 19-GHz phase according to the fine detection. Fig. 4.7(b) shows the timing diagram of the phase selector.

The 8-way interleaved clock phases are provided by a SHIL-MPRO shown in Fig. 4.8. The injection-locked input stage is co-designed with an embedded harmonic-rejection phase interpolator [87–89]. The phase interpolator can be used for the coarse and fine alignment.

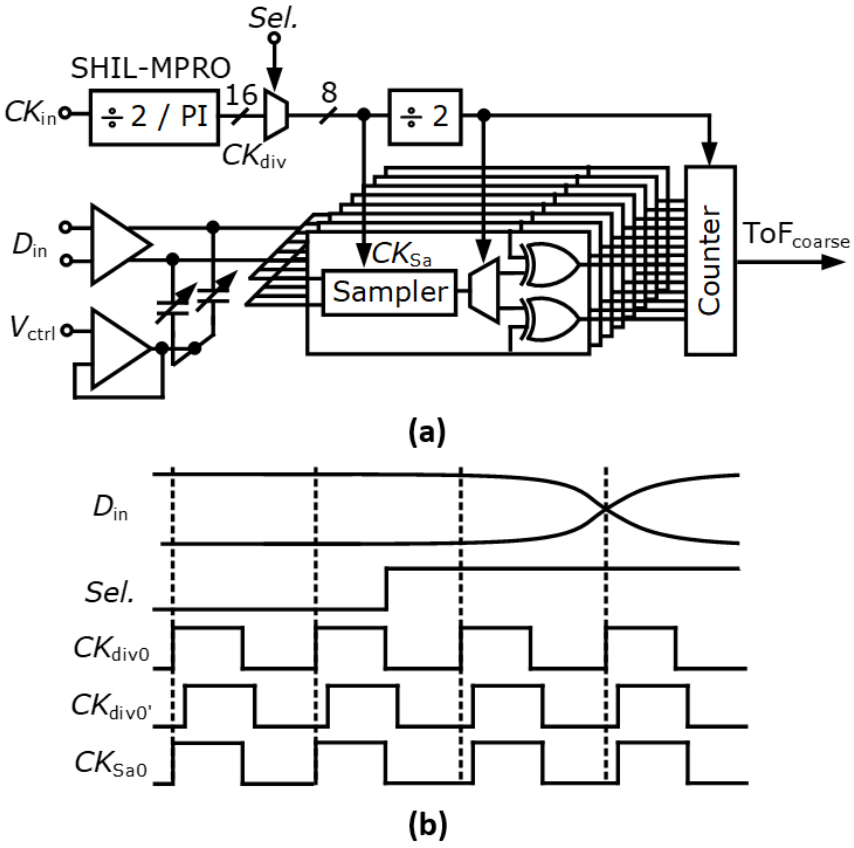

Figure 4.7: (a) Post-edge coarse ToF detector, and (b) its timing diagram.

Fig. 4.9 shows the delay cell in the SHIL-MPRO. The delay cell consists of two inputs, V_{in1} and V_{in2}, with a cross-coupled PMOS load. One of the input, V_{in2}, is injection-locked from the phase interpolator. The harmonic rejection is done by interpolating the inputs of 0°, 45°, and 315°(−45°) with a ratio of $\sqrt{2} : 1 : 1$. At the fundamental frequency, three vectors form a constructive output. At the 3^{rd}-order harmonic and the 5^{th}-order harmonic, all vectors cancel each other out, therefore, improve the linearity of the phase interpolation. Two branches are 45° apart at $f_{ref}/4$ and can be rotated 45° to cover the calibration range of the coarse and the fine detection. The interpolated current then injects into the ring oscillator. The phase selector (*Sel.*) in Fig. 4.7(a) selects in-phase or quadrature-phase based on the relation between I/Q fine measurement to effectively double the sampling rate of the detector. This approach reduces the routing complexity of clock signals.

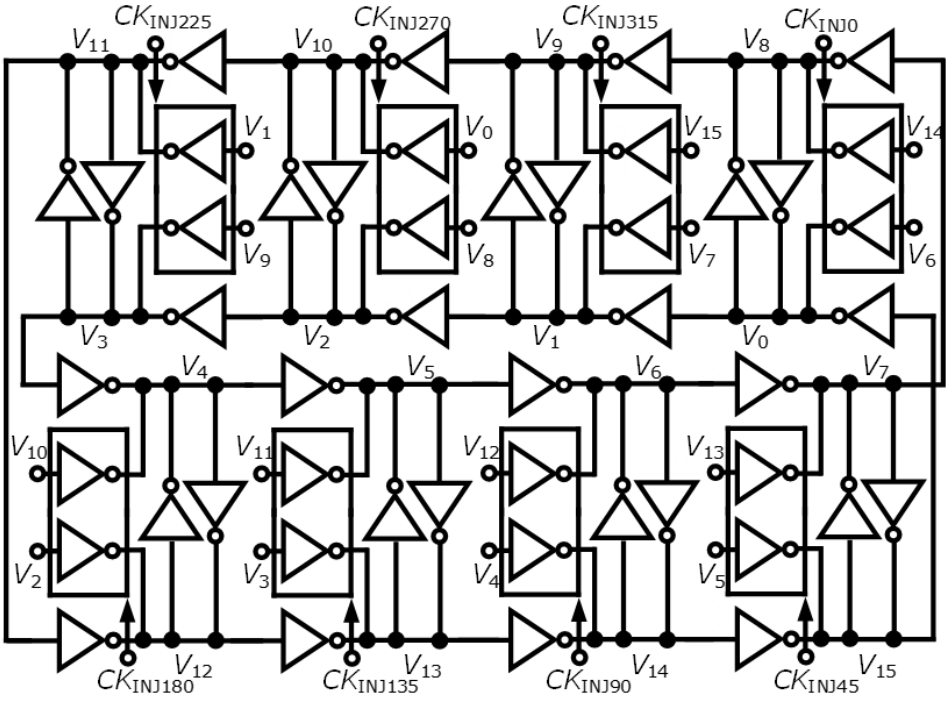

Figure 4.8: Multi-phase ring oscillator design.

4.2 DSP-based Receiver

The system architecture of the DSP-based receiver is shown in Fig. 4.10. An optical transmitter is formed by a single wavelength laser source at 1550 nm with two cascaded electro-optical modulators (EOMs) modulated by a 19-GHz reference clock (f_{ref}) and a 148-MHz ($f_m = 1/128 f_{ref}$) pulsed pattern generator (PPG). An erbium-doped fiber amplifier (EDFA) then amplifies and transmits the modulated laser. At the receiving end, a two-channel analog frontend (AFE) is implemented. A high-speed p-i-n photodiode converts the echoed optical signal to the electrical RF signal. A 1-bit phase-invariant programmable-gain low noise amplifier (PI-PGLNA) [73] and a 2× subharmonic mixer (SHM) with transimpedance amplifier (TIA) load (Fig. 4.11) [90] amplify and down-convert the RF signal into IF. Since the signal is at 19 GHz with 148 MHz modulation and its 3_{rd}-order harmonic, the frontend requires a bandwidth of 1 GHz. To satisfy this requirement, the ADC has to operate at

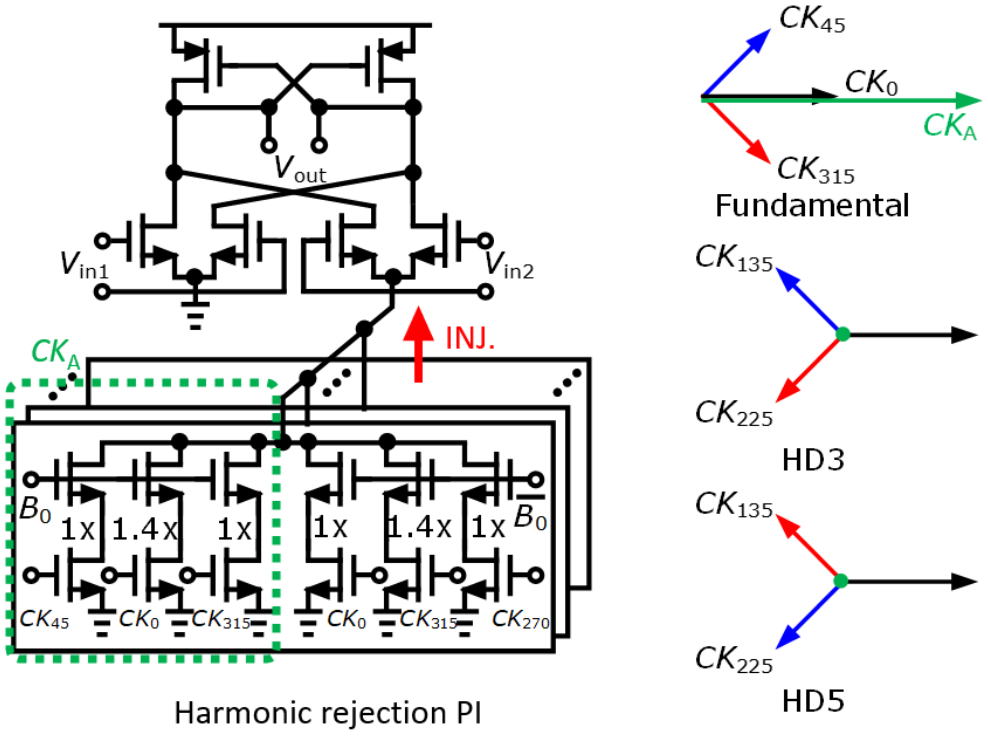

Figure 4.9: Delay cell of the multi-phase ring oscillator with harmonic rejection phase interpolator.

higher than 2 GHz to avoid aliasing. An external divide-by-8 divider (HMC862A) provides a 2.375-GHz reference to the local PLL (CK_{in}) and the ADC. We set the IF frequency (f_{IF}) at 1.78 GHz ($3/32 f_{ref}$) which is centered between the ADC sampling clock and its Nyquist rate; therefore, we can maintain the maximum available bandwidth of 1 GHz. Next, we can calculate the LO frequency (f_{LO1}) based on the RF frequency of 19 GHz and the IF frequency of 1.78 GHz, which is 17.2 GHz ($29/32 f_{ref}$). To synchronize the transmitter and the receiver, the same pulse sequence is also used as a timestamp. It is embedded in the LSB of the ADC, acting as a reference starting point for ToF calculation. A chain of PI-PGAs with 4-bits of tuning covering 50-dB gain range amplifies the IF signal and is followed by a subsampling ADC. The ADC applies a dual-threshold over-range detection, ORA and ORB, to adjust the gain with automatic gain control (AGC) loop for wide dynamic range.

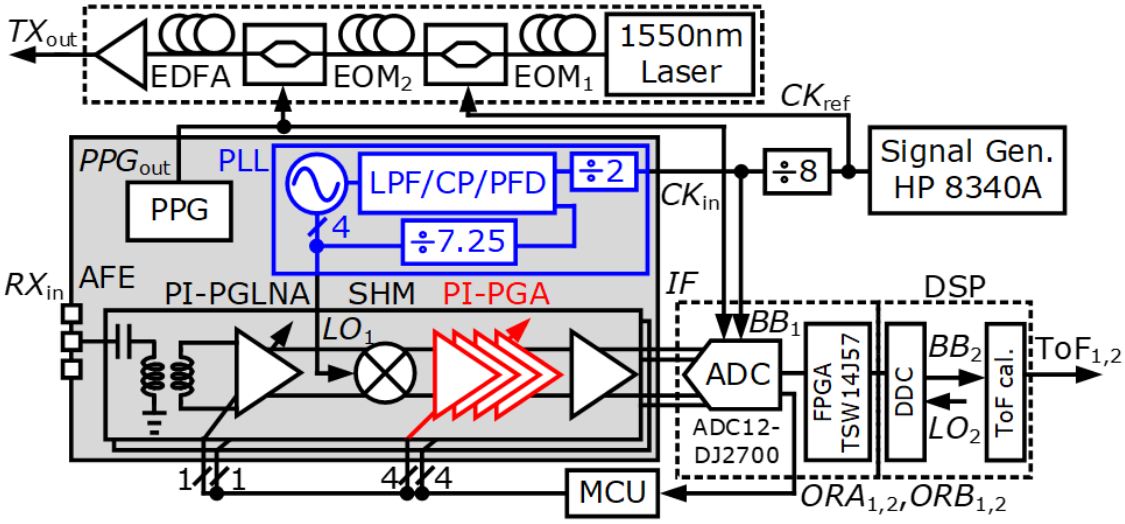

Figure 4.10: DSP-based receiver system implementation.

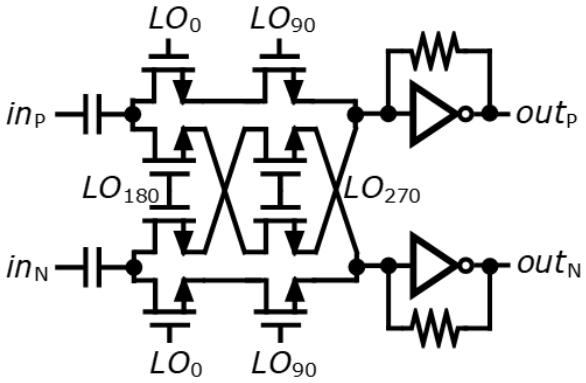

Figure 4.11: 2× subharmonic mixer design.

A digital signal processor digitally down-converts (DDC) the captured data with a digital complex LO ($f_{LO2} = 1/32 f_{ref}$) to calculate the segmented and overall ToF.

4.2.1 Narrowband Optical Frontend

Since the signal is narrowband, we apply the narrowband matching approach to get the best noise performance. Fig. 4.12(a) shows the schematic and the photograph of the matching network. A photodiode bare die with 20-μm diameter is directly wire-bonding to our AFE

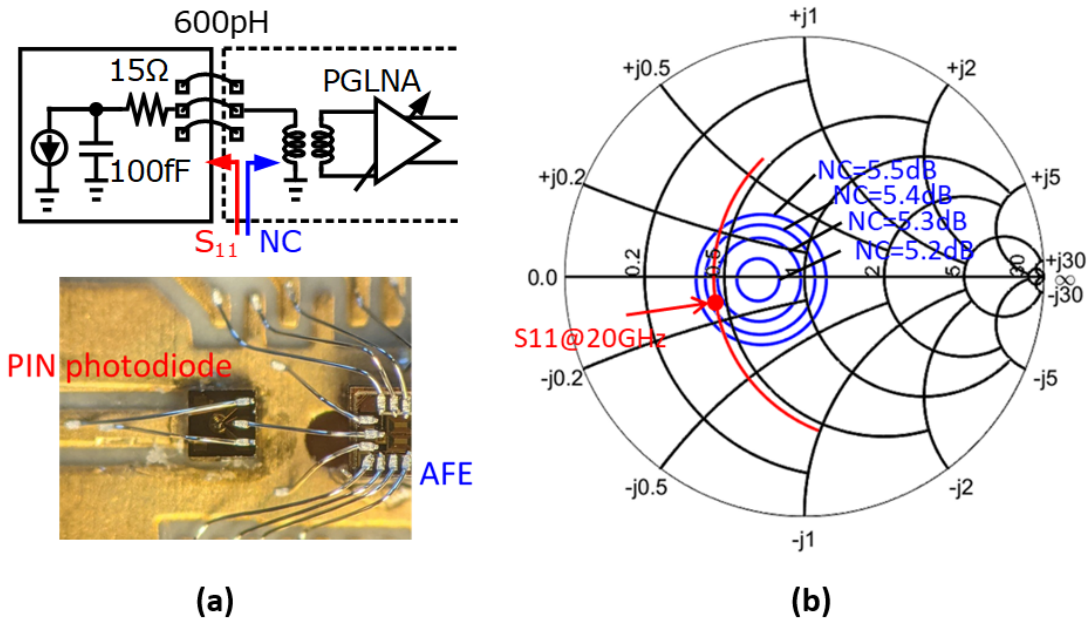

Figure 4.12: (a) Narrowband matching network frontend and photograph of direct wire-bonding from a p-i-n photodioe to the receiver, and (b) Smith chart with AFE noise circcle and S_{11} of the photodiode model.

chip, and the 600-pH bond-wire acts as a matching network. We use a simplified RC model to emulate the parasitic of the photodiode with a 100-fF parasitic capacitance and 15-Ω series resistance. The noise circle (NC) of the receiver frontend and the S_{11} of the photodiode model are shown on a Smith chart in Fig. 4.12(b).

The narrowband matching reduces the input-referred noise current by 2× comparing to using an off-the-shelf photodiode module (EOT-3500F) with an internal 50-ohm termination. The simulation results of the noise performance are shown in Fig. 4.13 where the input-referred noise current density is 19 pA/$\sqrt{Hz}$ with direct wire-bonding and 60 pA/$\sqrt{Hz}$ with the off-the-shelf photodiode module.

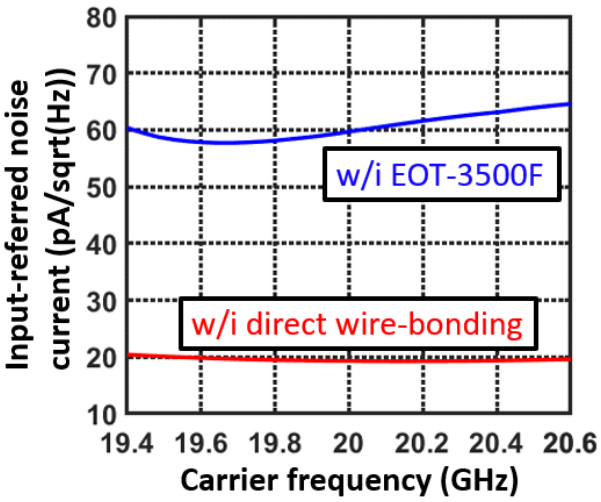

Figure 4.13: Comparison of the input-referred noise current with EOT-3500F and with direct wire-bonding.

4.2.2 Inverter-based Phase-invariant Programmable-gain Amplifier

The proposed inverter-based PI-PGA design is shown in Fig. 4.14(a). While phase variations can be calibrated, providing a phase-invariant design improves the sensitivity substantially and calibrated accuracy. An inverter-based design is chosen for better linearity comparing to the Current mode logic (CML). The unit cell of the PGA is shown in Fig. 4.14(b), which is an inverter with a control signal that enables it. The PGA can be viewed as a transconductance (G_m) with a load structure (R_l).

A current-steering transconductance stabilizes the input and output impedances to minimize the phase variation among the gain settings. The amplifier achieves the maximum gain when all forward units are turned on where the equivalent G_m is g_{m1}. To reduce the gain of the amplifier, we turn off some units (α) in the forward path, and at the same time, turn on the same amount of the unit cells in the cross-forward path. The conducting currents from both paths are subtracted at the output node, thus reducing the effective transconductance.

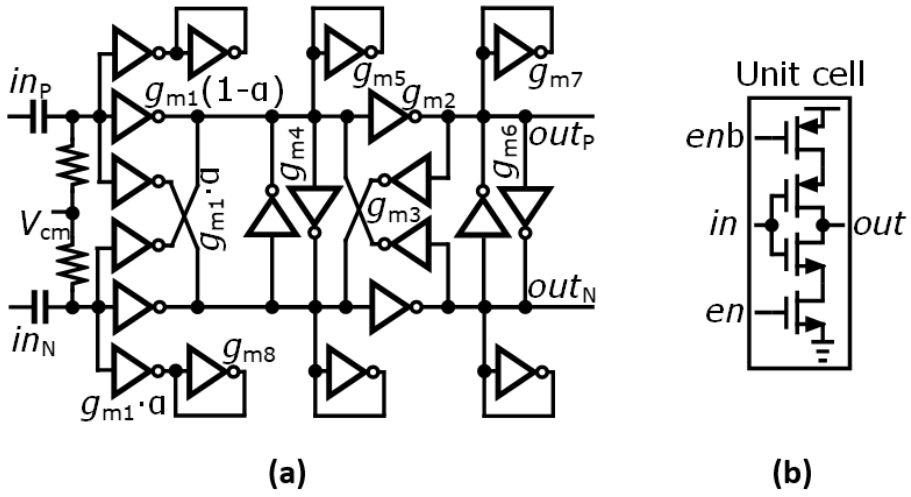

Figure 4.14: Phase-invariant programmable-gain amplifier (PI-PGA) design: (a) schematic of single-stage PI-PGA, and (b) its unit cell.

The equivalent G_m of the phase-invariant amplifier is

$$G_m = g_{m1}(1 - 2\alpha). \tag{4.3}$$

The total units of the on-inverters remain the same across different gain settings. With the fixed amount of on-units, the input and output impedances have a small variation across the gain tuning range.

The gain tuning range and the relative phase shift are shown in Fig. 4.15. The 4-stage PGA achieves a 50-dB gain tuning range with only 2.8° relative phase shift. An additional phase-compensation unit is added to further compensate for the variation caused by the change of the Miller capacitance in the forward path and the cross-forward path. When we turn on the cross-forward inverters, we also enable the same amount of units in the compensation branch. After compensating the difference of the Miller capacitance, the relative phase shift is further reduced to within 0.7°.

The amplifier's load design is realized by cross-coupled inverters ($g_{m4,6}$) and diode-connected inverters ($g_{m5,7}$). This implementation decouples the common-mode gain and the differential mode gain [91]. The common-mode gain is suppressed by 48 dB shown in

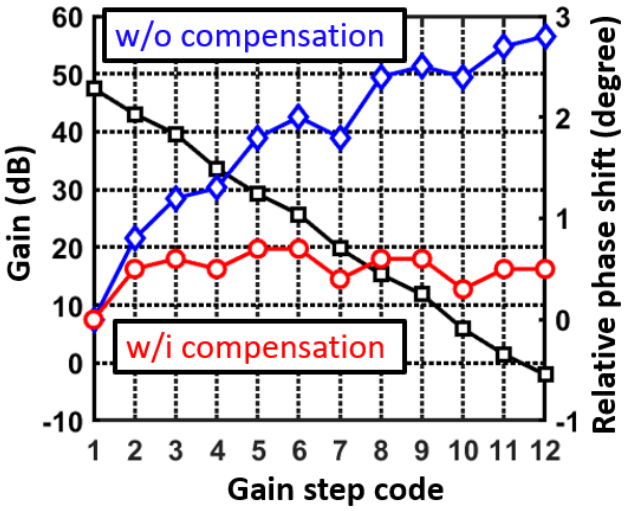

Figure 4.15: Gain response and relative phase shift with different gain settings.

Fig. 4.16(a). The equivalent load in differential mode is

$$R_{l1,diff} = \frac{1}{g_{m5}} // \frac{-1}{g_{m4}}, \tag{4.4}$$

where the equivalent load in common mode is

$$R_{l1,comm} = \frac{1}{g_{m5}} // \frac{1}{g_{m4}}. \tag{4.5}$$

The decoupling of the common-mode gain and the differential mode gain enables one-stage active feedback. Without the common-mode gain suppression, the load forms an unstable positive feedback loop in common mode. The active feedback loop with g_{m2} and g_{m3} extends the bandwidth, the gain is equal to

$$g_{m1}(1-2\alpha)\frac{g_{m2}R_{l1,diff}R_{l2,diff}}{1+g_{m2}g_{m3}R_{l1,diff}R_{l2,diff}}, \tag{4.6}$$

where

$$R_{l1,diff} = \frac{1}{g_{m5}} // \frac{-1}{g_{m4}}, \tag{4.7}$$

and

$$R_{l2,diff} = \frac{1}{g_{m7}} // \frac{-1}{g_{m6}}. \tag{4.8}$$

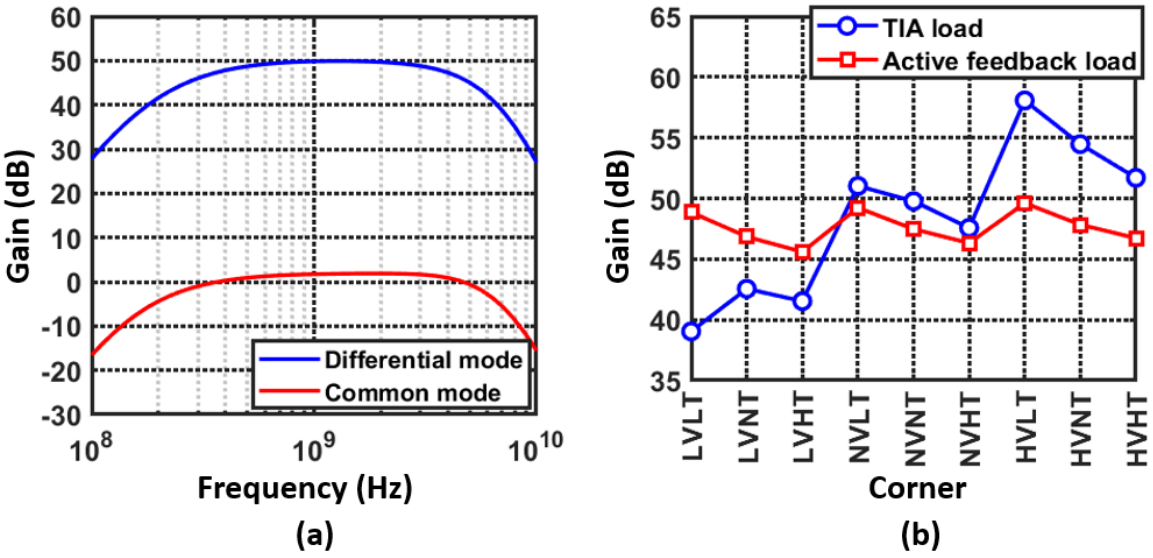

Figure 4.16: (a) Common mode gain and differential mode gain, and (b) gain variation in different temperature and supply corners.

The closed-loop gain is approximately $g_{m1}(1-2\alpha)/g_{m3}$. In comparison to a transimpedance amplifier (TIA) load (inverter with resistive feedback), the active feedback load provides better immunity to PVT variation since the gain only depends on the ratio of the transconductances, g_{m1} and g_{m3}. Fig. 4.16(b) compares these two different structures in simulation. The gain variation with the active feedback load reduces from 20 dB to 5 dB across $-20°C$ to $125°C$ and $\pm 10\%$ supply variation.

4.2.3 LO Generation

The design goal of the PLL is to synthesis the 17.2-GHz LO frequency from the 2.375-GHz reference. There are two possible approaches as shown in Fig. 4.17(a) and Fig. 4.17(b): One is to operate the PLL at full rate, which the VCO is operating at 17.2 GHz; or we can design a half-rate PLL at 8.6 GHz, and use the subharmonic mixer to effectively double the LO frequency.

Operating the VCO at half rate has a benefit of preventing the pulling between the LO

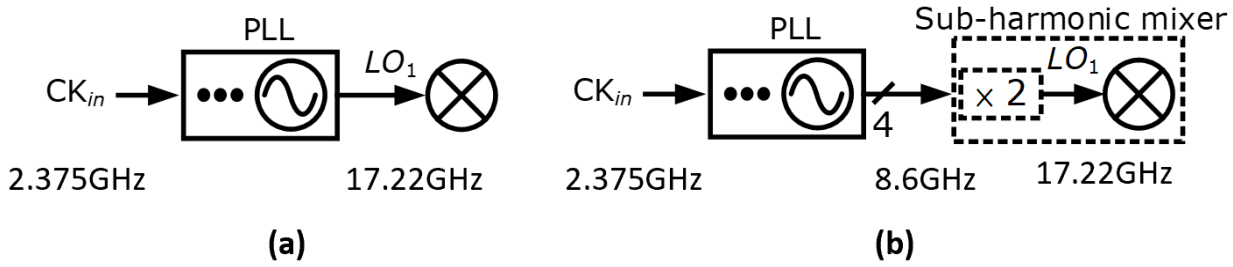

Figure 4.17: PLL architectures in (1) full-rate operation, and (b) half-rate operation.

and the incoming signal; also, the ring-type VCO can be implemented at half rate, which has a very small footprint and inherently provides multi-phase outputs comparing to the LC-tank VCO; however, one concern is that the ring-type VCO has higher phase noise, so we have to design it carefully to filter the phase noise.

We adopt the conventional type-II PLL architecture as shown in Fig. 4.18. With the design constraints of the input clock at 2.375 GHz and the output frequency at 8.6 GHz, we have to select proper divide ratios of the feedforward divider (M)and the feedback divider (N), and the loop bandwidth to optimize the noise performance. We start the optimization from operating the loop in the integer-N mode where $M = 8$ and $N = 29$.

The noise transfer function of the VCO in the PLL loop is [92]

$$H_{n,VCO}(s) = \frac{\Phi_{out}}{\Phi_{VCO}} = \frac{1}{M}\frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}, \tag{4.9}$$

where

$$\zeta = \frac{R_2}{2}\sqrt{\frac{I_{CP}C_2K_{VCO}}{2\pi N}}, \tag{4.10}$$

and

$$\omega_n = \sqrt{\frac{I_{CP}K_{VCO}}{2\pi N}}, \tag{4.11}$$

where I_{CP} is the charge-pump's output current, K_{VCO} is the frequency gain of the VCO, R_2 and C_2 are the loop filters. Since the VCO's noise experiences a high-pass response, the loop bandwidth is set at its highest allowed frequency, 1/10 of the reference, to suppress the noise contributed from the VCO.

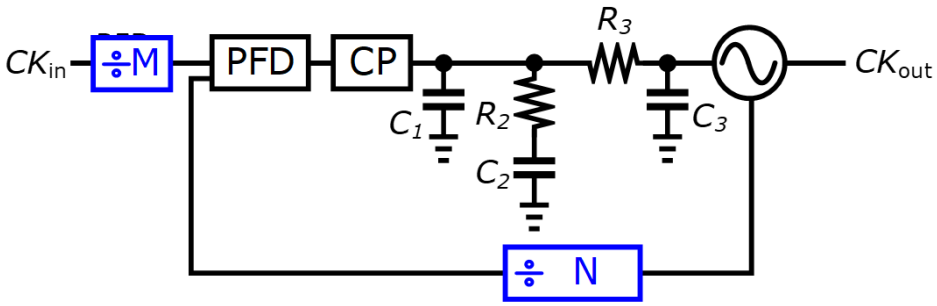

Figure 4.18: PLL architecture.

Considering the charge-pump's noise, the noise has a low-pass response

$$H_{n,CP}(s) = \frac{\Phi_{out}}{\Phi_{CP}} = \frac{(2\pi/I_{CP})N(2\zeta\omega s + \omega_n^2)}{s^2 + 2\zeta\omega_n s + \omega_n^2}. \tag{4.12}$$

Assuming that the integration bandwidth of the ToF calculation is 5 MHz, the overall rms jitter from the PLL is 130 fs where the VCO contributes 125 fs rms jitter, and the charge pump contributes 25 fs rms jitter. Unfortunately, the rms jitter is too high for the target precision of 10 μm. Note that we separate the reference noise from our noise model (Fig. 3.4); therefore we only consider two dominant sources of the PLL's additive noise.

From the calculation above, we can observe that the VCO's phase noise is the dominant noise source. To further suppress the VCO's noise, one way is to increase the loop bandwidth; however, the loop bandwidth cannot exceed 1/10 of the reference clock. In order to extend the loop bandwidth, we must lower the divide ratio of the feedforward divider (M) to raise the reference clock, and operate the feedback divider in the fractional-N mode. Fig. 4.19 shows the rms jitter with different design choices of the divide ratio. The noise is reduced as the bandwidth increases (smaller divide ratio), but it eventually limits by the charge-pump's noise. Table 4.1 shows the design parameters of the divide ratios and the required VCO's output phases for the fractional-N operation. Considering the requirement of the VCO's phases and the performance, we select $M = 2$, $N = 7.25$ and the loop bandwidth of 100 MHz. The divide-by-7.25 divider and the subharmonic mixer can share the same in-phase

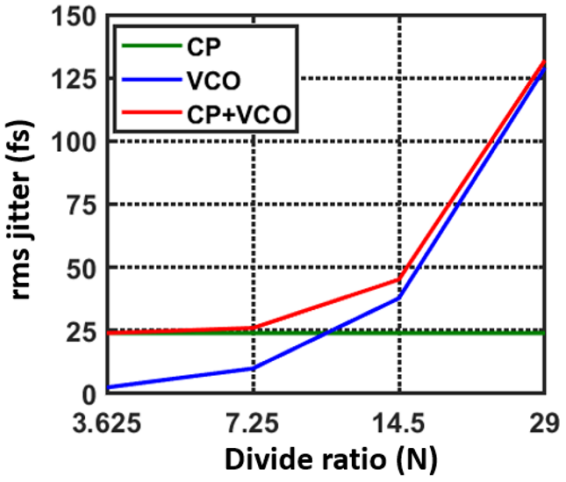

Figure 4.19: PLL's additive noise with different loop parameters.

CK_{in}	CK_{out}	M	N	VCO phases	Bandwidth (f_{BW})
2.375GHz	8.6GHz	1	3.625	8	250MHz
2.375GHz	8.6GHz	2	7.25	4	125MHz
2.375GHz	8.6GHz	4	14.5	2	62.5MHz
2.375GHz	8.6GHz	8	29	1	31.25MHz

Table 4.1: PLL design choice.

and quadrature-phase outputs from the VCO.

The PFD shown in Fig. 4.20(a) is a conventional structure that consists of two D-flip flops triggered by the reference clock and the feedback clock from the divider chain. A NOR gate resets the D-flip flops when the inputs trigger both. The auxiliary differential output controls the up and down current of the charge pump. A dummy transmission gate matches the delay of the inverter. The charge pump is shown in Fig. 4.20(b) adopts the design in [93] with a complimentary output to improve the phase noise performance. A unity gain buffer replicates the output voltage to the auxiliary path. This auxiliary path reduces the charge

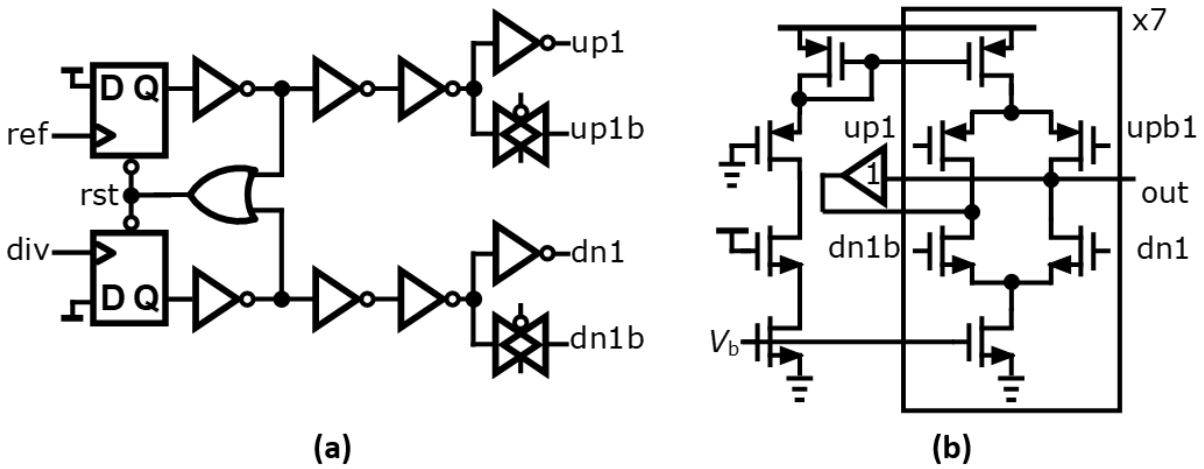

Figure 4.20: (1) The phase frequency detector design, and (b) the charge pump design.

I_{cp}	C_1	C_2	R_2	C_3	R_3	K_{vco}
1mA	200fF	12pF	900Ω	200fF	450Ω	5GHz/V

Table 4.2: PLL design parameters.

sharing to the loop filter and prevents the current sources from being fully turned off when the charge pump disconnects from the loop filter. The output current source is partitioned into seven units, and each unit conducts 200 μA. The nominal output current is 1 mA.

Table 4.2 shows the design parameters of the PLL. In the loop filter, C_1, C_3, and R_3 reduce the reference and the fractional spur. The loop dynamic simulation is shown in Fig. 4.21 where the loop bandwidth is 100 MHz with a phase margin of 70°.

The proposed 2-stage differential ring-type VCO and its delay cell are shown in Fig. 4.22. The elements are all modified from the clocked inverter in the standard cell library. The small and compact footprint improves the matching of the delay cell and the output phases. The VCO's operating frequency is tuned by interpolating delays of the discrete-tuning path and the analog-tuning path. The hybrid frequency tuning covers a wide tuning range across the PVT variations, also reduces the K_{VCO} to minimize the perturbation to the VCO.

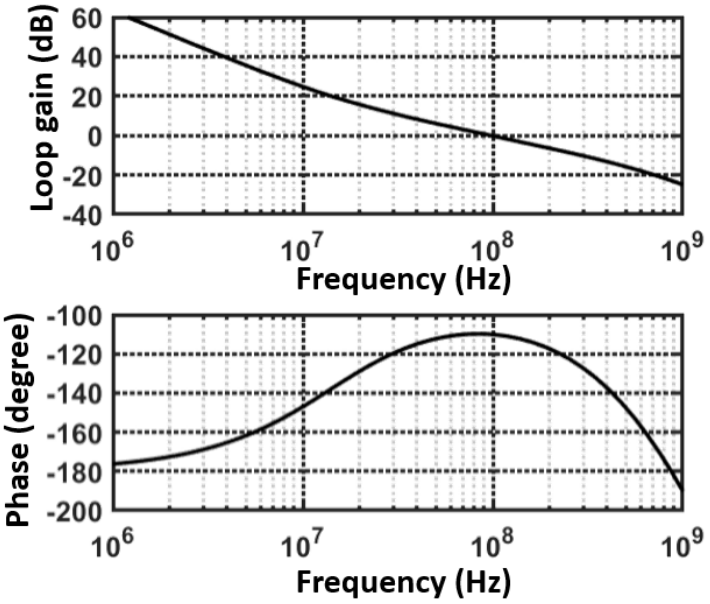

Figure 4.21: Bode plot of PLL's open loop gain and phase margin.

In the discrete tuning path shown in blue color, the inverters with enable signal are controlled by 3-bit digital word (en[2:0], enb[2:0]) which provides 8-discrete bands to cover the process variation. In the analog-tuning path shown in the red color, the delay cell consists of parallel inverters in cascade with transmission gates. The analog-tuning range is designed to accommodate the temperature (-20°C to 125°C) and supply variation ($\pm 10\%$) within a process corner. In the transmission gates, all NMOSs are connected to the loop filter of the PLL. Half of the PMOSs are tied to high ($tieH$), and the rest of the PMOSs are tied to low ($tieL$). The programmable connection to high or low provides a tuning knob to linearize the frequency tuning curve.

The frequency tuning range is shown in Fig. 4.23(a). This VCO can operate from 5 GHz to 12 GHz with eight discrete bands and a 1-GHz operating range for each band with both discrete tuning and analog tuning. The frequency calibration process is as follows: (1) The loop filter is disconnected from the charge pump and is set to half of the supply voltage ($1/2V_{DD}$); (2) the discrete band is set at the mid-band which is B_3; (3) we send the

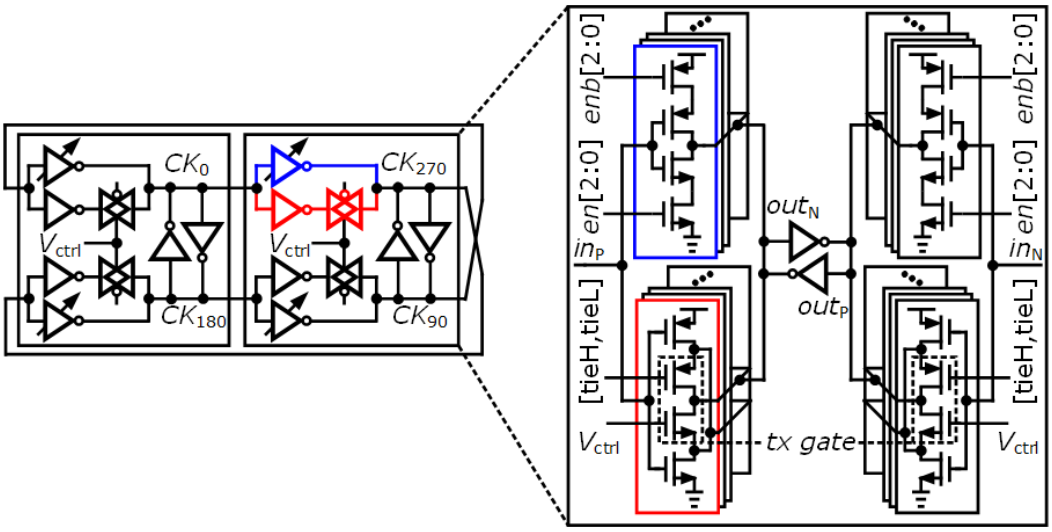

Figure 4.22: Ring-type VCO design.

output from the fractional divider, and the output from the reference divider to the DSP; (4) the DSP detects the beat frequency of the reference frequency and the VCO frequency and performs the binary search of the discrete band selection; (5) after the frequency error narrows down to within 3% of the operating frequency, the loop filter switches back to the closed-loop mode. Fig. 4.23(b) shows the simulation results of the phase noise at 9 GHz. At 1-MHz offset frequency, the phase noise is –76 dBc/Hz.

Fig. 4.24(a) shows the divide-by-7.25 fractional divider design, and Fig. 4.24(b) shows its timing diagram. The fractional divider consists of two 4-to-1 multiplexers with one-hot control, a divide-by-7 divider, a ring counter, and a re-timer. The operating starts from resetting the ring counter with one-hot output (S_{0-3}). Every seven input-clock cycles, the divide-by-7 divider (CK_c) triggers the ring counter, and the ring counter shifts one bit. The re-timer then senses the change of the ring counter, and its output (D_{0-3}) selects the next input phase of the 4-1 multiplexer. The input clock (CK_a) then shifts 90° and generates the fractional divider ratio. The 4-input phases match carefully to reduce the fractional spur.

The overall phase noise of the PLL is shown in Fig. 4.25. The overall rms jitter is 175 fs

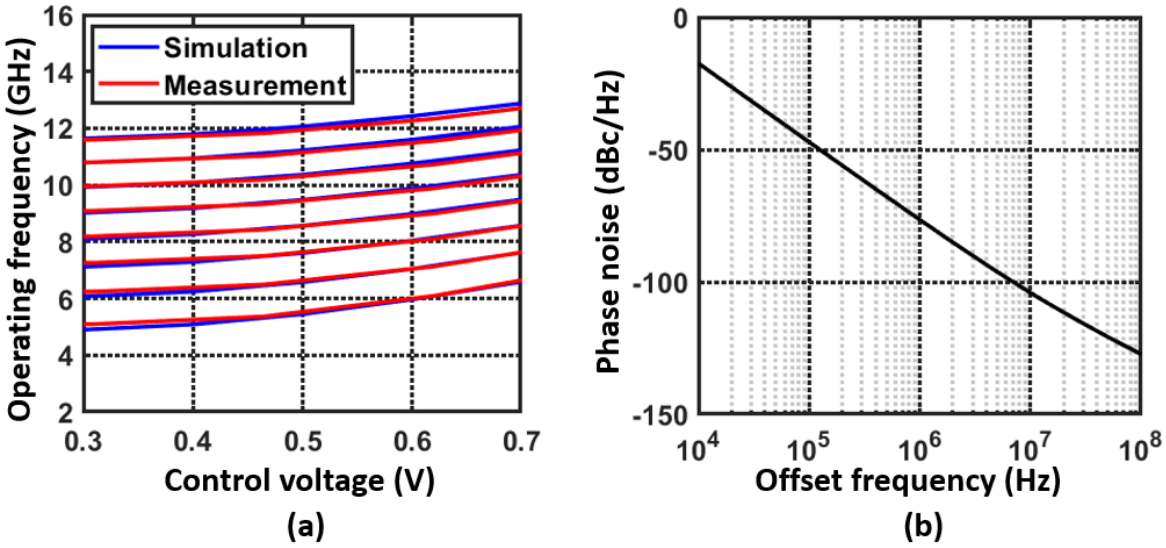

Figure 4.23: Ring-type VCO: (a) tuning range, and (b) phase noise at 9 GHz.

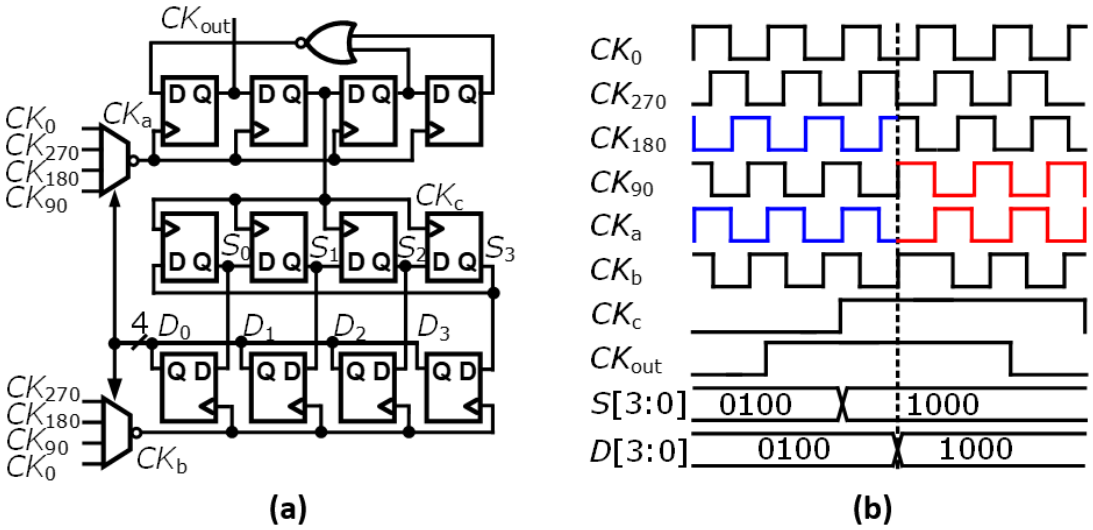

Figure 4.24: (a) Divide-by-7.25 fractional divider design, and (b) its timing diagram.

with the integration bandwidth from 1-MHz to 1-GHz offset frequency. The reference clock, charge pump, VCO, and the fractional divider contribute 25-fs, 76-fs, 152-fs, and 10-fs rms jitter.

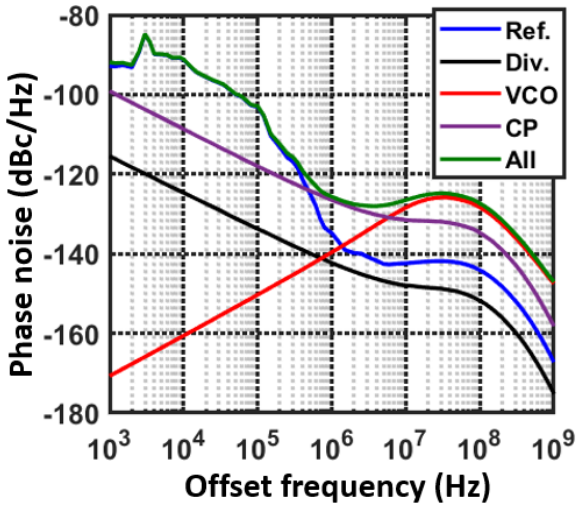

Figure 4.25: Phase noise of the PLL.

4.2.4 Digital Signal Processor

The digital signal processor (DSP) is shown in Fig. 4.26. The DSP processes the ToF offline using MATLAB. After the IF signal at $3/32f_{ref}$ is sampled by an ADC at a rate of $1/8f_{ref}$, the signal is converted to baseband (BB_1) at $1/32f_{ref}$ (Fig. 4.27(a)). The DSP first extracts the embedded start signal from the least significant bit by calculating modulo 2 to find the start point of the ToF counting. The extracted sequence then correlates with the transmitted pulsed waveform. The index of the maximum is the ToF starting reference index (I_{start}). A complex digital mixer with the LO frequency(BB_2) at $1/32f_{ref}$ then down-converted the baseband signal (BB_1) to DC (Fig. 4.27(b)).

A second correlator find the correlation of the transmitted pulsed waveform and the down-converted pulse envelope of the received signal, which is reconstructed from the digitized I/Q (V_I and V_Q) by absolute function

$$V_{env} = |V_I + jV_Q|. \tag{4.13}$$

The correlation index (I_{coarse}) is quantized by f_s/f_m yielding the corase ToF (T_c). This correlation also provides the alignment for the subsequent intermidiate ToF (T_i) and fine

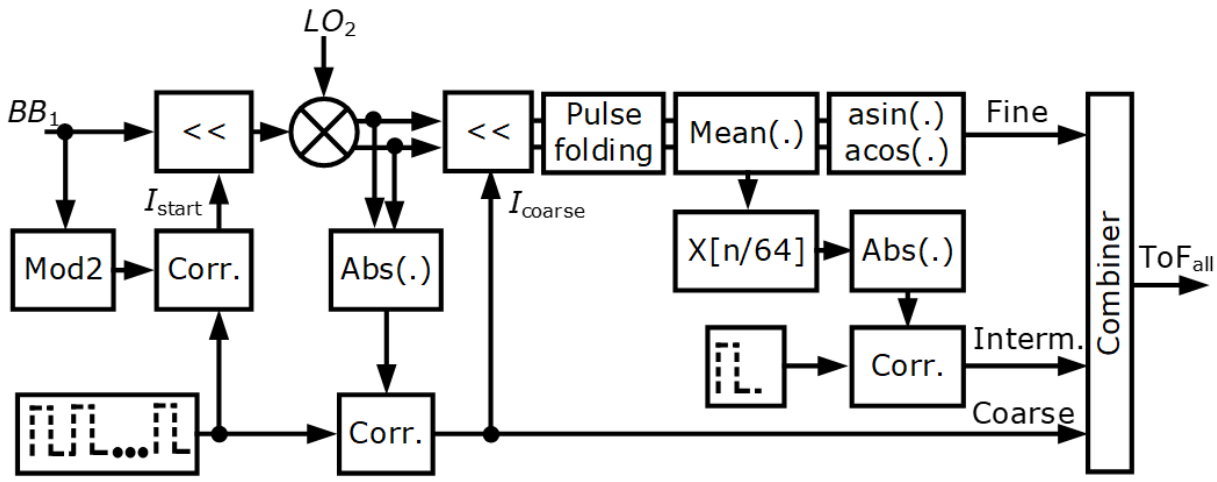

Figure 4.26: Digital signal processor design.

ToF (T_f) calculations. The phase shift of the pulse envelope (ϕ_{env}) is then detected to yield T_i. As long as the quantization error of T_i is $< 0.5 \times 360°/(f_c/f_m) = 1.4°$ which corresponds to a half cycle of T_c, there is sufficient handoff between the segments and the precision is determined by the fine phase measurement.

Fig. 4.27(c) and Fig. 4.27(d) demonstrate the process of pulse folding from folding a pulse sequence to a single pulse. The envelope is reconstructed from the averaged in-phase and quadrature-phase signals. By using an FIR filter with an interpolation factor of 64, a correlator then finds the phase shift of the pulse envelope. This phase shift then be quantized by (f_{ref}/f_m) yielding intermediate ToF (T_i).

To detect phase information of the modulated pulse envelope, instead of post-filtering to reconstruct the envelope, we pre-filter the received signals before reconstructing the envelope by folding and summing I/Q signals into a single period of $1/f_m$. Two envelope detections are shown in Fig. 4.28(a). Fig. 4.28(b) illustrates the difference between the two approaches in terms of integral nonlinearity (INL) with 3-ps ToF per step. The additive noise to the signal introduces nonlinearity after the power detector that exceeds the tolerable quantization error with the post-filtering. By pre-filtering, the effective SNR is increased before the power detector, thus reduces the noise-dependent INL.

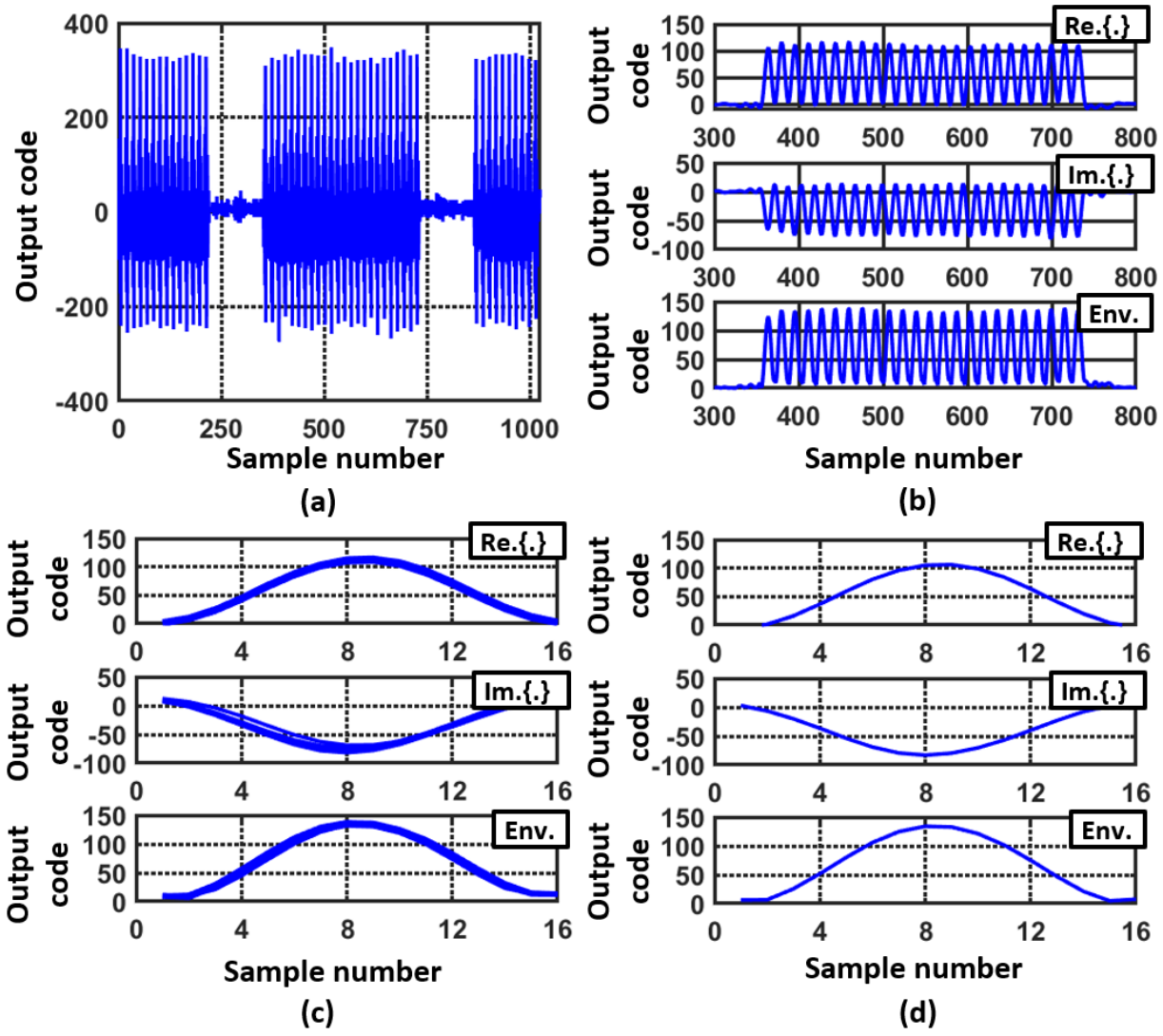

Figure 4.27: DSP signals in time domain: (a) ADC output (BB_1), (b) down-converter signals (BB_2) after digital complex mixer, (c) signal after pulsed folding, and (d) signal after pulsed folding and averaging.

Lastly, we take the middle two ADC samples in each folding pulses and use arcus functions

$$\theta = sin^{-1}(V_I/\sqrt{{V_I}^2 + {V_Q}^2}) \; or \; \theta = cos^{-1}(V_Q/\sqrt{{V_I}^2 + {V_Q}^2}) \tag{4.14}$$

whichever is at the most linear region to find fine ToF (T_f) (Fig. 4.29). In order to avoid the discontinuity from 360° to 0° in the averaging process, four mean values are calculated

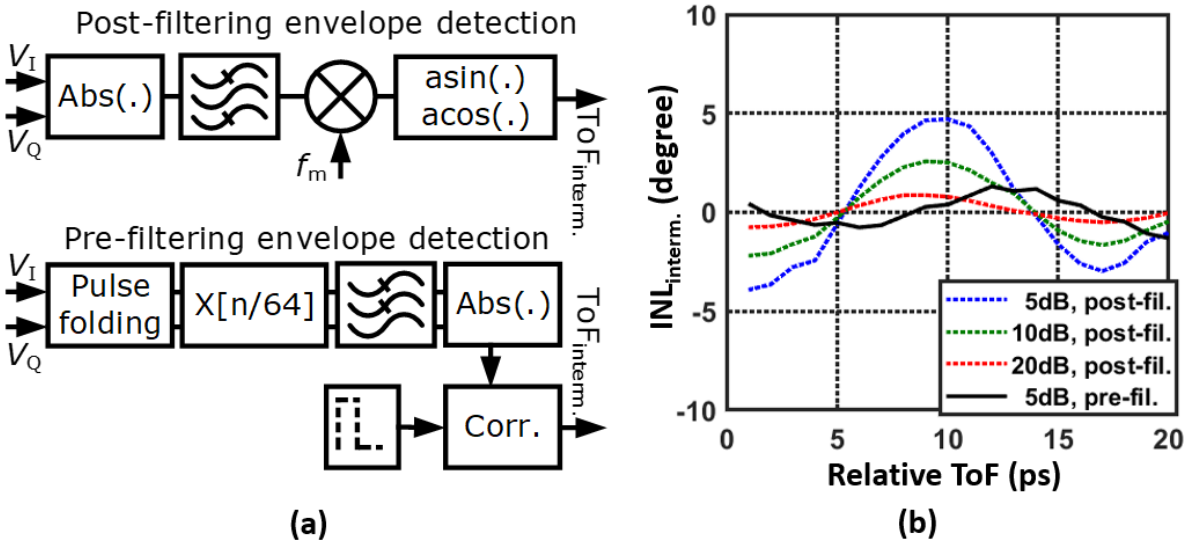

Figure 4.28: (a) Comparison of the envelope detections with the post-filtering envelope detection and the pre-filtering envelope detection, and (b) INL with ToF sweep.

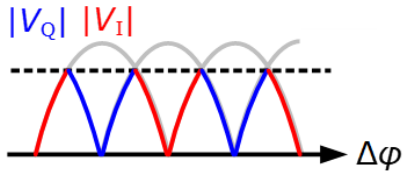

Figure 4.29: Phase detector with I/Q selection.

according to different reference phases (0°, 90°, 180°, 270°), and the one with the least mean square is selected as the fine ToF result.

4.3 Summary

This chapter has introduced the essential building blocks of both the analog-based receiver and the DSP-based receiver. The arrangement of the operating frequency has also been discussed. In the analog-based receiver, we implemented a hybrid discrete/analog tuning with a 1-bit RF amplifier, a 1-bit programmable gain amplifier, and an analog-tuning variable-gain

amplifier. We utilized the in-phase and quadrature-phase IF signals for the power detector, therefore, improved the speed of the AGC loop. In the DSP-based receiver, the IF amplifier is substituted by an inverter-based programmable gain amplifier, which improves the area, power consumption, and linearity. The phase noise of the LO generator has been analyzed to optimize the noise performance. A hybrid tuning ring-type VCO is implemented to reduce the K_{vco} while covering the PVT variation. A fractional divider has been used in order to increase the bandwidth of the PLL. In the next chapter, we will show the experimental results of both the building blocks and the lidar system.

CHAPTER 5

Measurement Results

In this chapter, we will show the experimental results of both the building blocks and the scanning results of the lidar system. Two chips have been fabricated in TSMC 28-nm CMOS technology. We measured the performance of the phase-invariant amplifiers by tuning an optical attenuator to mimic a real ranging acquisition. We will also show the noise performance of the clocking circuitry. Different scanning setups and their measurement results will be demonstrated.

5.1 Analog-based Receiver

The prototype of the analog-based lidar receiver has been designed and fabricated in TSMC 28-nm CMOS technology. The receiver consumes 121 mA from a 1-V supply where two PI-VGLNAs in the clock path and the signal path consume 32 mW, the down-conversion mixer, PGA, VGA, and coarse ToF detector consume 48 mW, and the clock path consumes 36 mW. Fig. 5.1 shows the die photograph of the analog-based receiver which occupies 1.2 mm $\times$ 1.2 mm including the pad ring. This receiver has not been integrated with optics and the results are measured using an RF signal that has been variably attenuated.

5.1.1 Phase-invariant Amplifiers

Fig. 5.2(a) shows the transient response of the pulsed envelope with the AGC loop. It shows the responses with different relative input powers of 0 dB, 8 dB, and 16 dB referenced to

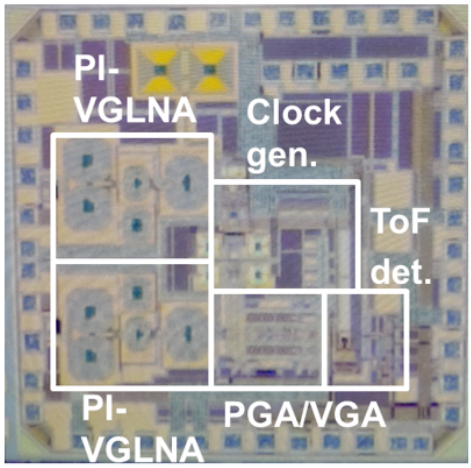

Figure 5.1: Die photograph of analog-based pulsed-coherent lidar receiver.

the minimum detectable SNR of 12 dB before the signal detector. We can observe that the rise-edge has a larger walk error comparing to the post-edge. Fig. 5.2(b) quantifies the walk error between rise-edge detection and the proposed post-edge detection. For a single-threshold rise-edge detection, the walk error across the 16-dB dynamic range can be as large as 600 ps, whereas the proposed post-edge detection reduces the walk error to 26 ps. With the error of less than one cycle, the coherent phase-detection takes over the measurement; therefore, the walk error no longer impacts the accuracy of the measured ToF.

Fig. 5.3 shows the measurement results of the phase-invariant AFE. The phase error across 20-dB tuning range is $\pm 0.14^\circ$ of PI-VGLNA, $\pm 0.11^\circ$ of PGA, and $\pm 0.5^\circ$ of VGA, which corresponds to ± 16.5-μm accuracy.

Fig. 5.4(a) depicts the rms error (σ_e)

$$\sigma_e = \frac{\sigma}{\sqrt{N}} \tag{5.1}$$

of the coarse ToF readouts with 70 detected post-edges. The rms error of the fine ToF measurement is shown in Fig. 5.4(b). With 1-μs integration time ($N = 140$), the rms error is 130 fs with an SNR of 12 dB and 42 fs with high SNR. The corresponding precision is 19.5 μm and 6.3 μm, respectively.

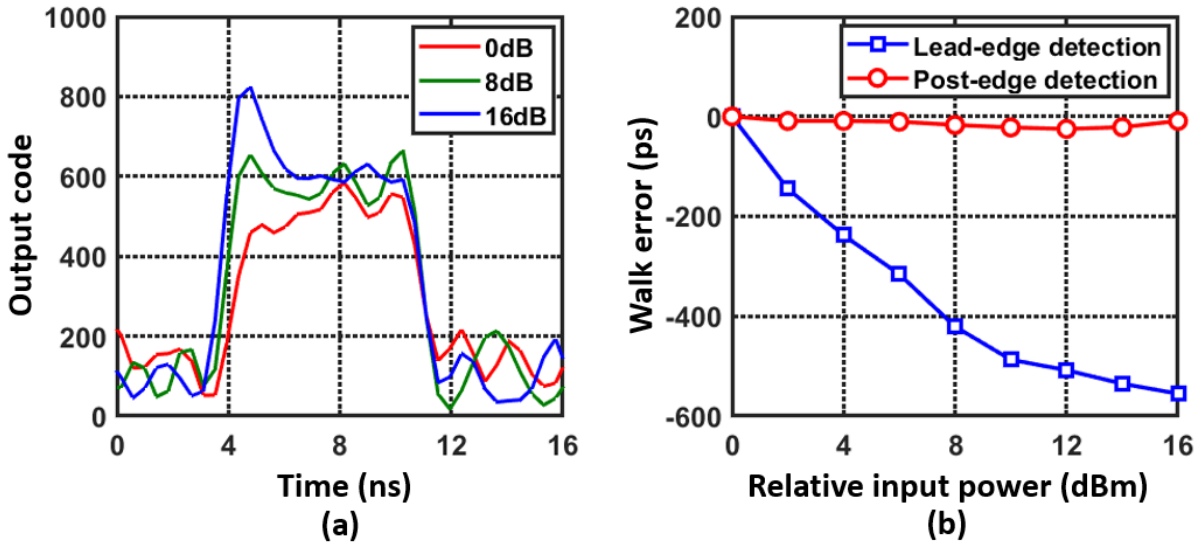

Figure 5.2: Measurement results: (a) transient responses of the pulsed-envelope with AGC loop, and (b) walk error comparison of rise-edge envelope detection and post-edge envelope detection.

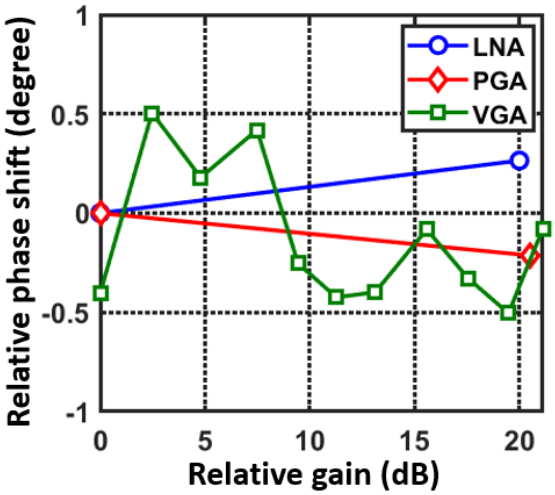

Figure 5.3: Measurement results of phase-invariant VGAs.

5.1.2 Clock Generation

Fig. 5.5(a) shows the spectrum of the 4.75-GHz signal output with 74-MHz ($1/256 f_{ref}$) pulsed modulation. Fig. 5.5(b) shows the phase noise of the 4.75-GHz clock at divider

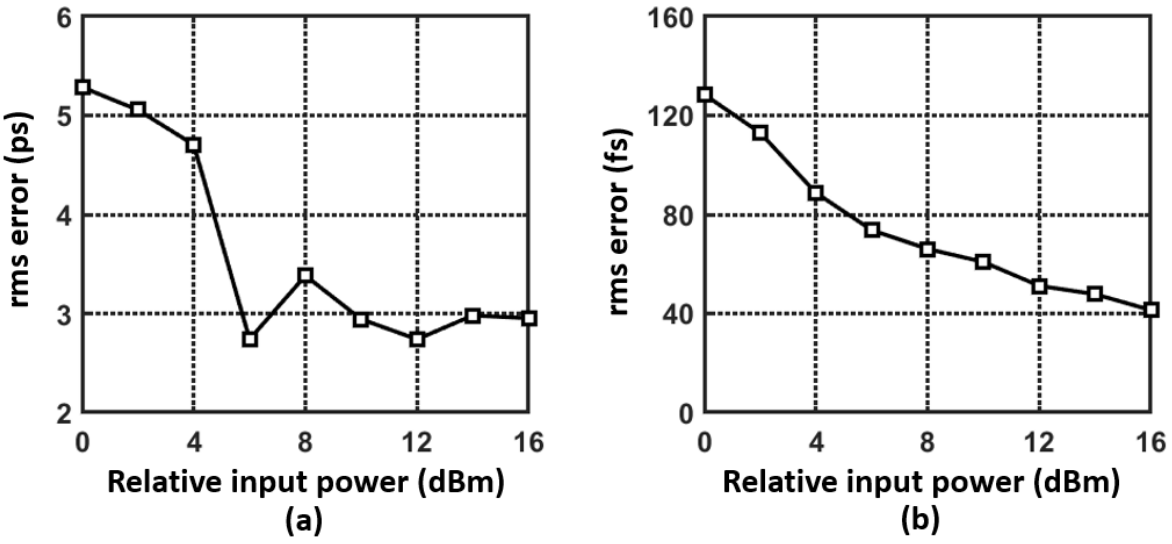

Figure 5.4: Measurement results: (a) rms error of coarse ToF. (b) rms error of fine ToF.

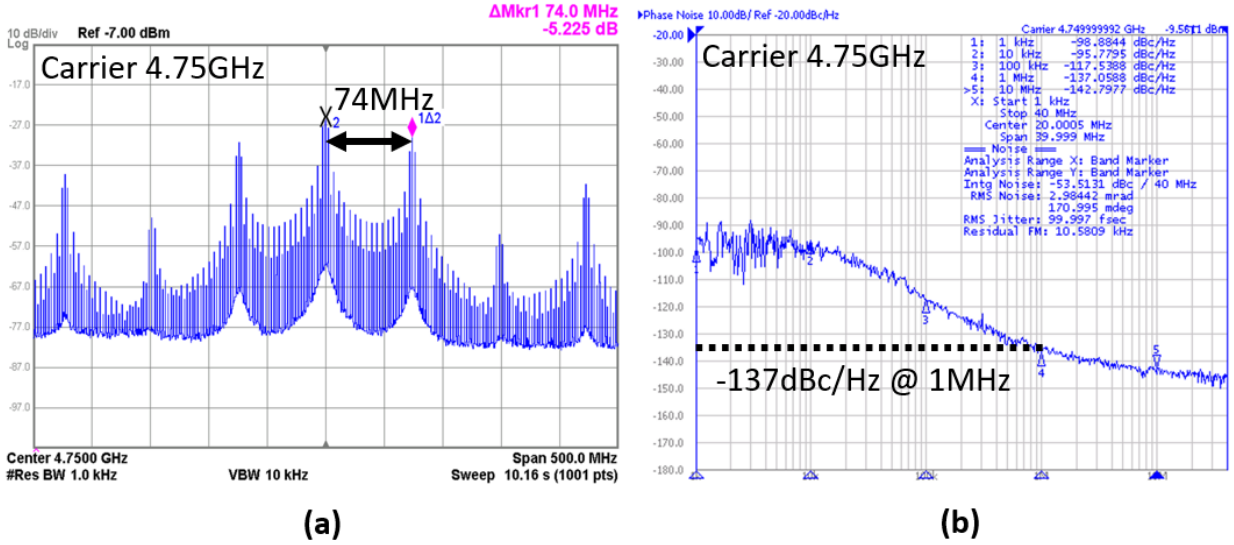

Figure 5.5: Measurement results: (a) spectrum of the received modulated signal, and (b) spectrum of the clock jitter at 4.75 GHz.

chain's output. The rms jitter integrated from 1 kHz to 40 MHz is 100 fs.

Combining the rms error and the phase offset due to the VGAs, the accuracy of 40 μm can potentially be achieved.

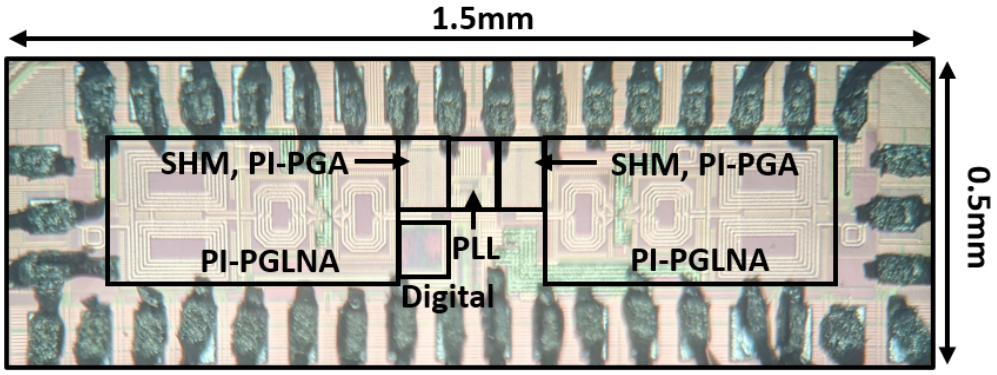

Figure 5.6: Die photograph of the DSP-based receiver frontend.

5.2 DSP-based system

The die photograph of the DSP-based receiver is shown in Fig. 5.6. The receiver is fabricated in TSMC 28-nm CMOS technology with 1.5 mm × 0.5 mm area, including the ESD bonding pad ring. The occupied active area is 0.39 mm^2, including two analog frontend channels, a shared local LO generator, and a synthesized digital logic block.

5.2.1 Narrowband Matching Network

In the DSP-based lidar system, we first verified the narrowband matching of the frontend circuits. We used a single chip and utilized both receiver channels to make the comparison. The measurement setup is shown in Fig. 5.7. One of the frontend channels is using narrowband matching with directly wire-bonding from a p-i-n photodiode bare die (GCS Do231_20μm_C3) with 20-μm diameter of the active area and 80-fF parasitic capacitance. The wire-bonding is 800 μm as a matching network for noise matching. Another receiving channel input is wire-bonding to the transmission line on the printed circuit board (RO4003) with an onboard matching network to 50-Ω termination. The PCB trace is then connected to a broadband photodiode module (EOT-3500F) with an internal 50-Ω termination via SMA cable.

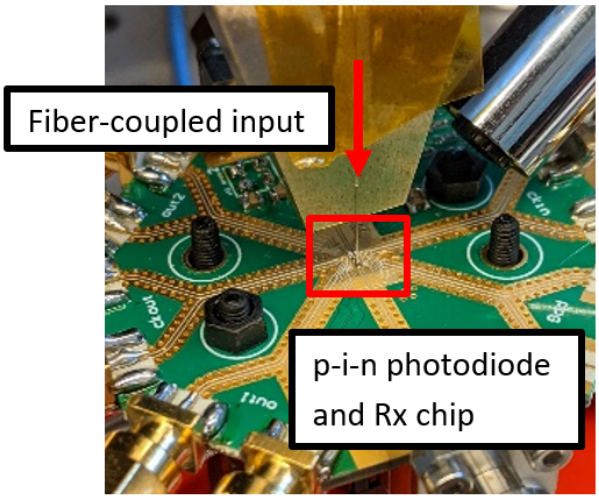

Figure 5.7: Measurement setup for direct wire-bonding from a photodiode bare die.

Both channels are directly received from EDFA with –3-dBm optical output power via fiber. Fig. 5.8(a) shows the frequency response of both implementations. The measurement results indicate that the narrowband approach extends the bandwidth and boosts the gain. The narrowband receiver has a peak gain at 20 GHz, where the broadband approach only provides less than 18-GHz bandwidth. The difference of the gain response is more than 15 dB at low frequency to 25 dB beyond 20 GHz (Fig. 5.8(b)).

Fig. 5.9 shows the comparison of the rms error by using the photodiode module and by using the direct wire-bonding photodiode. With an 1-MHz integration bandwidth, the rms error of using photodiode module (EOT-3500F) is 15 μm where the rms error of direct wire-bonding is 6.6 μm.

5.2.2 Phase-invariant Amplifiers

Fig. 5.10 shows the measurement setup for characterizing the performance of the phase-invariant amplifiers in the DSP-based system. The phase-invariant PGA is characterized by a variable fiber optical attenuator (VOA) mimicking a realistic environment. Using an optical attenuator is because of the tuning mechanism that moves the blocking device to achieve

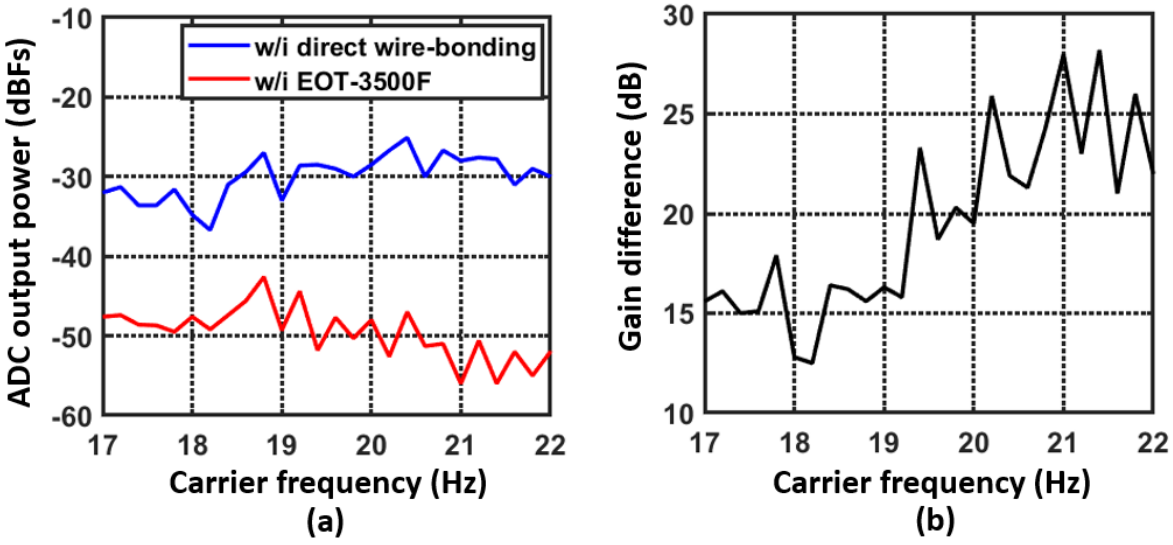

Figure 5.8: Measurement results: (a)comparison of the receiver bandwidth with using direct wire-bonding and using a photodiode module, and (b) gain difference of two designs.

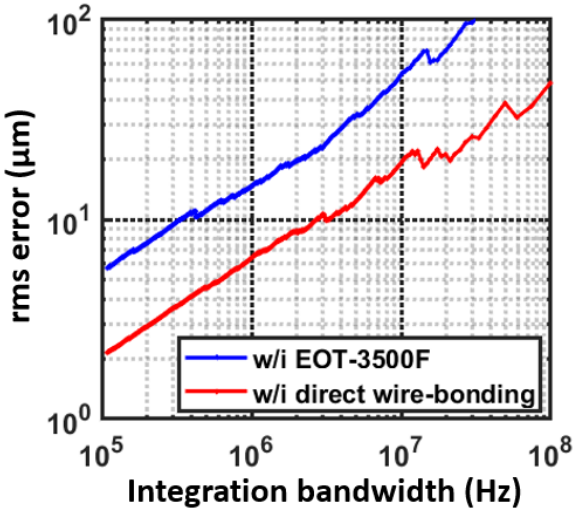

Figure 5.9: rms error comparison of using photodiode module and direct wire-bonding.

the desire attenuation. Comparing to an electrical attenuator, the optical attenuator has a minimum impact on the phase of the RF carrier. We adjust the input power to the PGA and measure the relative phase shift by the ADC. The measurement results are shown in Fig. 5.11. The PI-VGLNA achieves 17-dB gain tuning with 1-bit digital control centered at

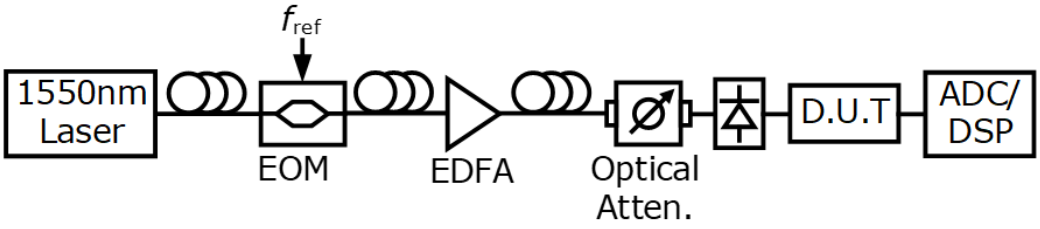

Figure 5.10: Measurement setup for characterizing the performance of the phase-invariant amplifiers.

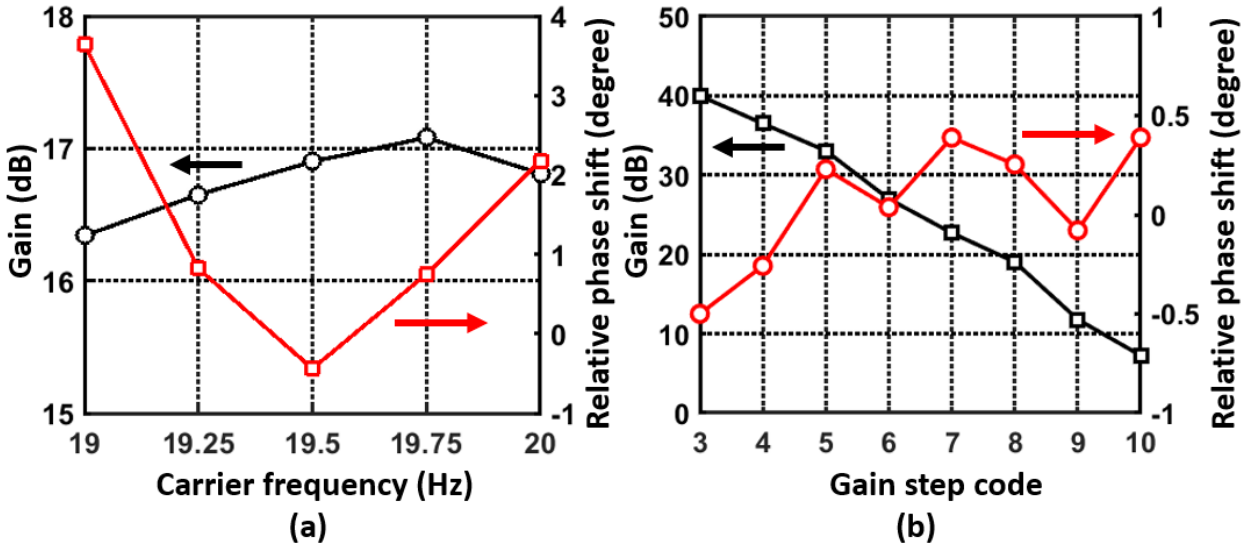

Figure 5.11: Measurement results: (a) phase-invariant programmable low noise amplifier gain response and relative phase shift, and (b) phase-invariant PGA gain and relative phase shift across different gain settings.

19.5 GHz and less than 0.5° phase shift. The inverter-based phase-invariant PGA achieves a low phase variation of ±0.5° across the 40-dB gain range, which corresponds to ±10-μm accuracy.

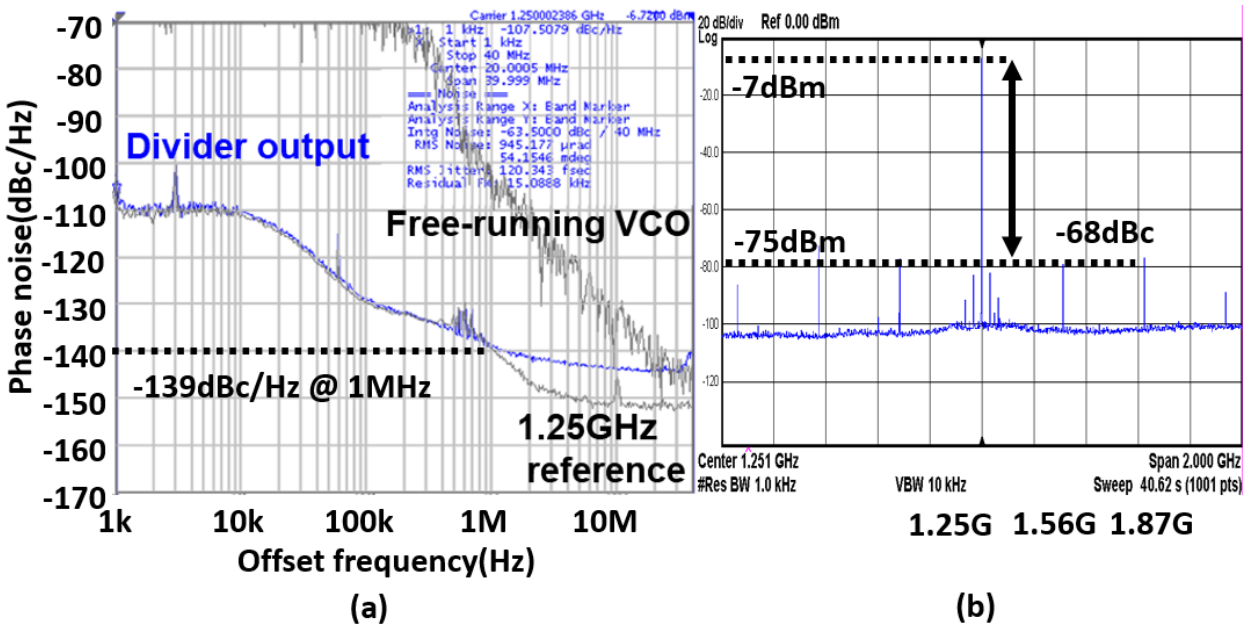

Figure 5.12: Measurement results: (a) phase noise of the fractional divider's output, and (b) spectrum of the fractional divider's output.

5.2.3 LO Generation

The PLL phase noise measured at the divide-by-7.25 output (1.25 GHz) is shown in Fig. 5.12(a). The phase noise of the free-running VCO and the 1.25-GHz reference clock is also shown in the plot. The rms jitter of the PLL is 120 fs integrated from 1 kHz to 40 MHz, and the phase noise is –139 dBc/Hz at 1-MHz offset frequency. Fig. 5.12(b) shows the spectrum of the clock output at 1.25 GHz. The fractional spurs are –70 dBc and –68 dBc at 312.5-MHz and 625-MHz offset frequency. The 2^{nd}-order harmonic of the fractional spur causes the in-band leakage and limits the receiver's sensitivity. The sensitivity of the receiver is –65 dBm without leakage cancellation. The leakage cancellation can be implemented in the DSP to improve the sensitivity further.

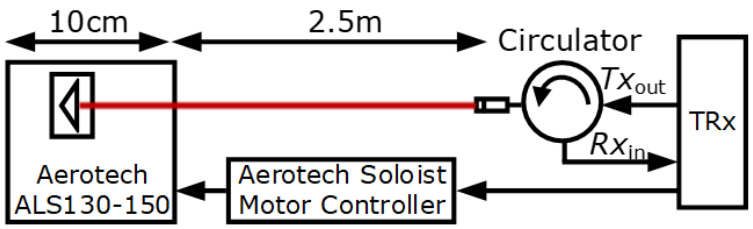

Figure 5.13: Measurement setup for characterizing the linearity and the precision of the lidar system.

5.2.4 1-D Scanning

The precision and the linearity are characterized in the 1-D scanning free-space measurement setup shown in Fig. 5.13. A mirror target with the motor stage (Aerotech ALS130-150) driven by an encoder is placed at 2.5-m away from the transceiver with 6-dBm output power. A circulator isolates the emitted and the returned laser beams. Fig. 5.14 shows the results of the overall and the segmented measured distance with a 10-cm dynamic range and 1-mm movement per step. Fig. 5.15 shows the INL and the precision of the 1-D scanning. The maximum INL is 30 μm with the rms error of 13 μm, and the mean of the precision across the 10-cm dynamic range is 6 μm with a 5-MSa/s sampling rate.

5.2.5 2-D Scanning

The 2-D scanning is performed in different optical setups. The first 2-D scanning setup is shown in Fig. 5.16(a). We use a motor stage that can move in both X and Y directions to scan objects. The target is a staircase formed by four gauge blocks with a 1-mm increment per step and is placed at 0.3 m away from the bi-axial optic transceiver. The scanning process is with 0.5 mm step size in both X and Y direction. The 3-D image is shown in Fig. 5.17(a). Fig. 5.17(b) shows the amplitude of the received signals with and without the AGC loop.

In Fig. 5.18, we scanned a 3-D printed target with less reflectivity. The target is a

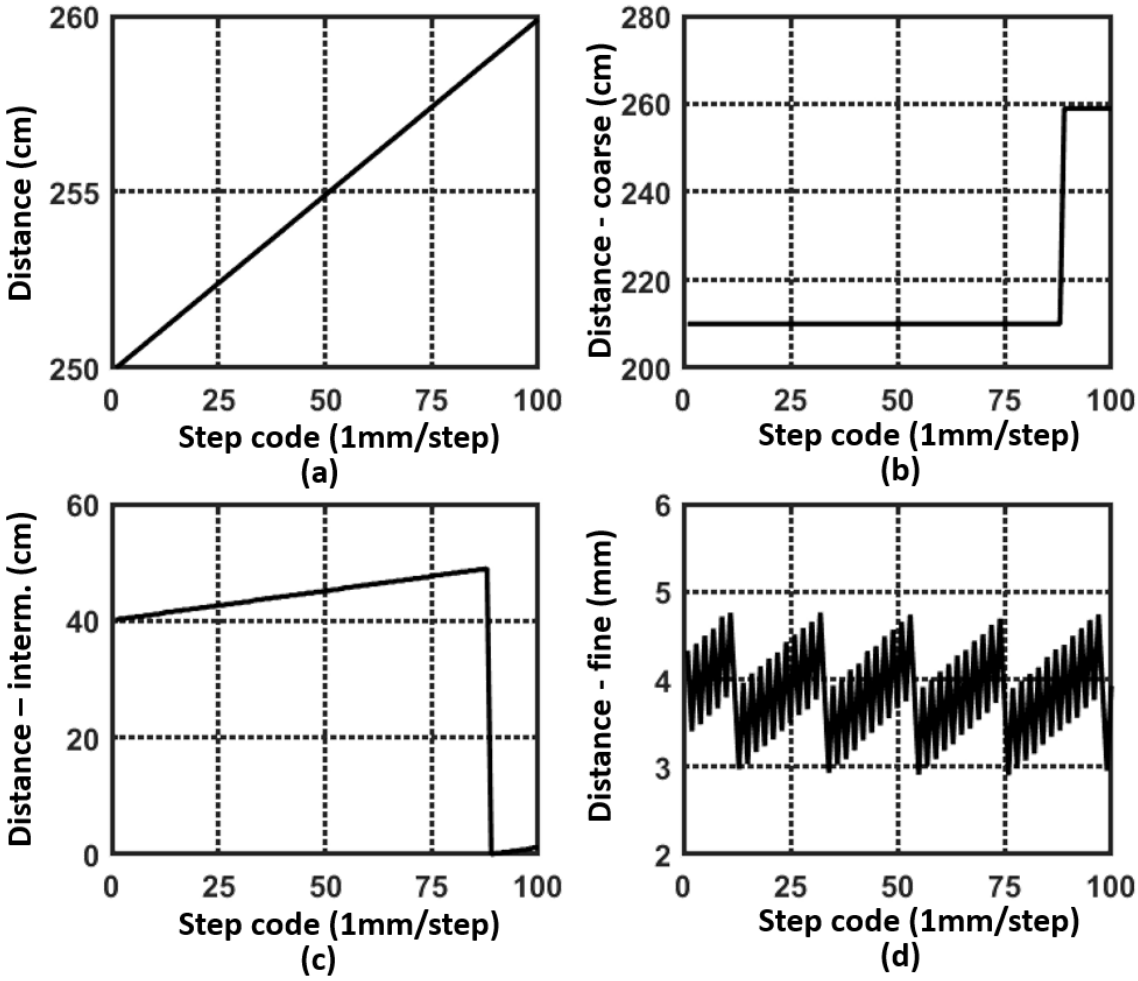

Figure 5.14: Measurement results: 1-D scanning at 2.5 m with (a) overall distance, (b) coarse distance, (c) intermediate distance, and (d) fine distance.

staircase with a 3-mm increment per stage and a mark on each stage with 1-mm depth. The overall height is 1.5 mm, which is over a period for the fine ToF measurement. The 3-D image shows the successful handover between the segmented depth measurement. Another target is shown in Fig. 5.19, a UCLA logo with a 1-mm increment of each letter. The target is scanned by 30 pixels $\times$ 85 pixels.

The second optical setup with a MEMS mirror is also demonstrated in Fig. 5.20. A polarizing beam splitter is inserted between the transmitter, the MEMS mirror, and the

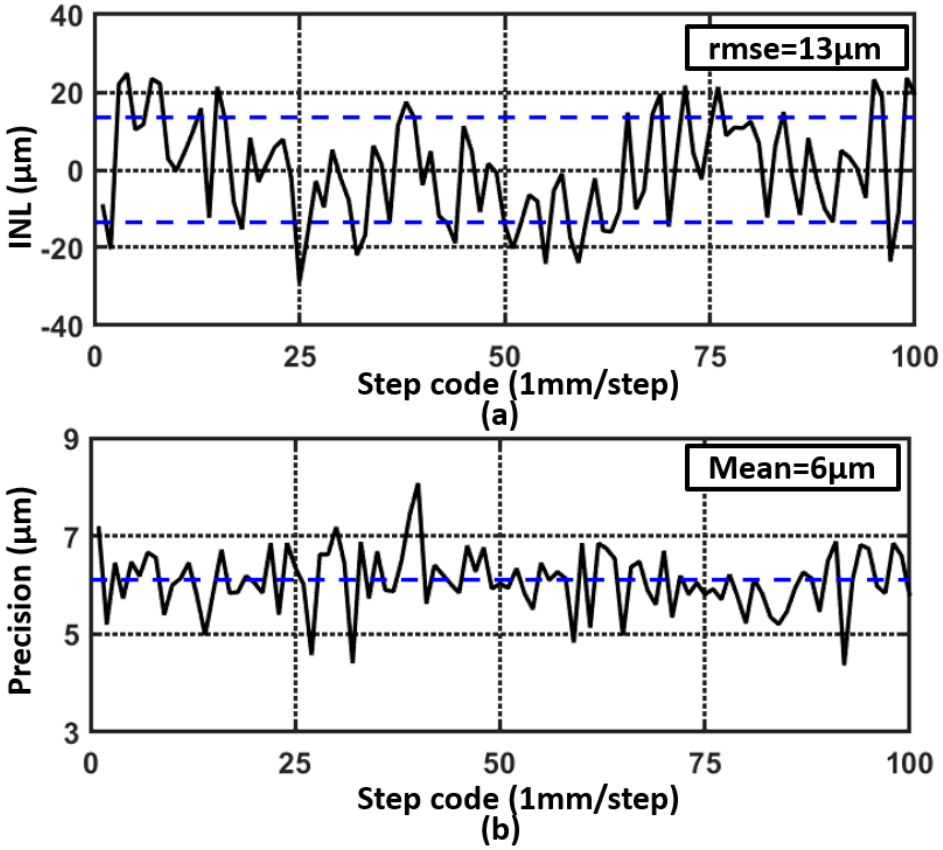

Figure 5.15: Measurement results: (a) INL, and (b) precision.

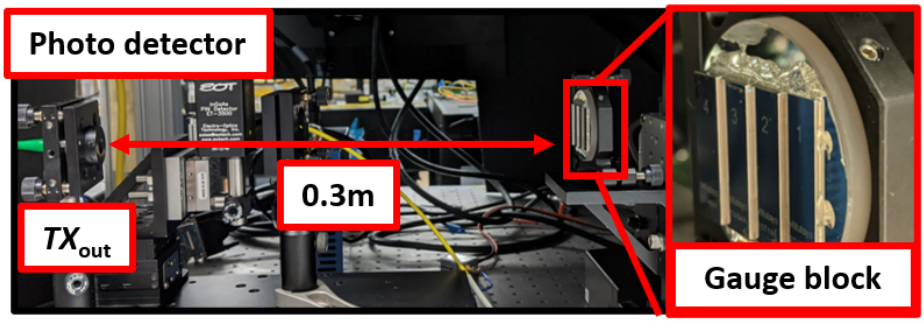

Figure 5.16: 2-D scanning setup.

photodetector. It improves the isolation of the transmitter and the receiver. The MEMS mirror is from MirrorcleTech with a 5-mm diameter. The scanning angle is ±5° in both X and Y direction. We paint the UCLA logo with 1-mm depth as a target to collect the

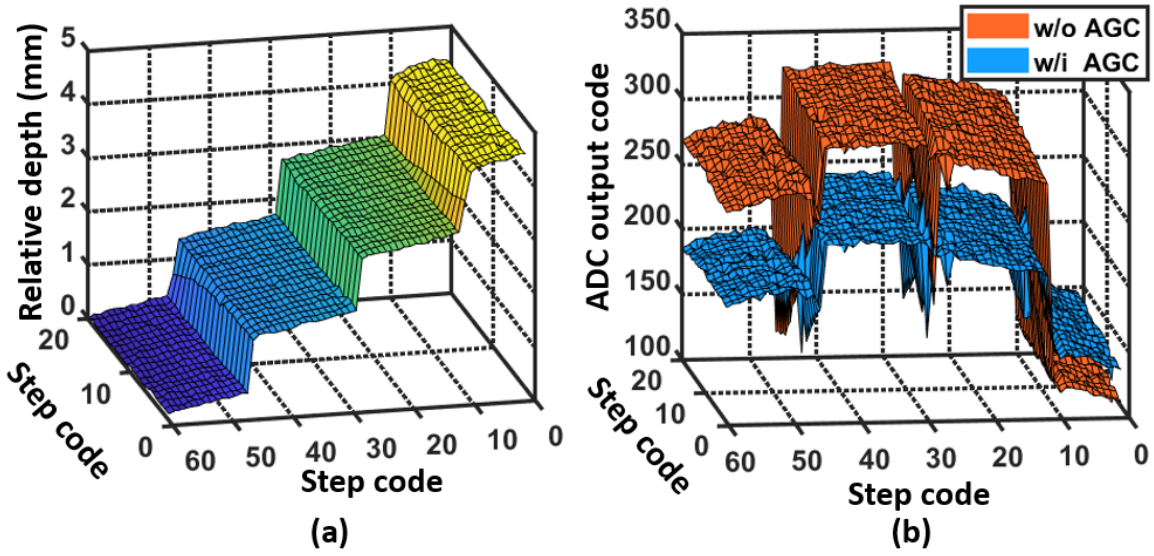

Figure 5.17: Measurement results: (a) scanned results of a star of gauge blocks, and (b) magnitude maps with AGC loop and without the AGC loop.

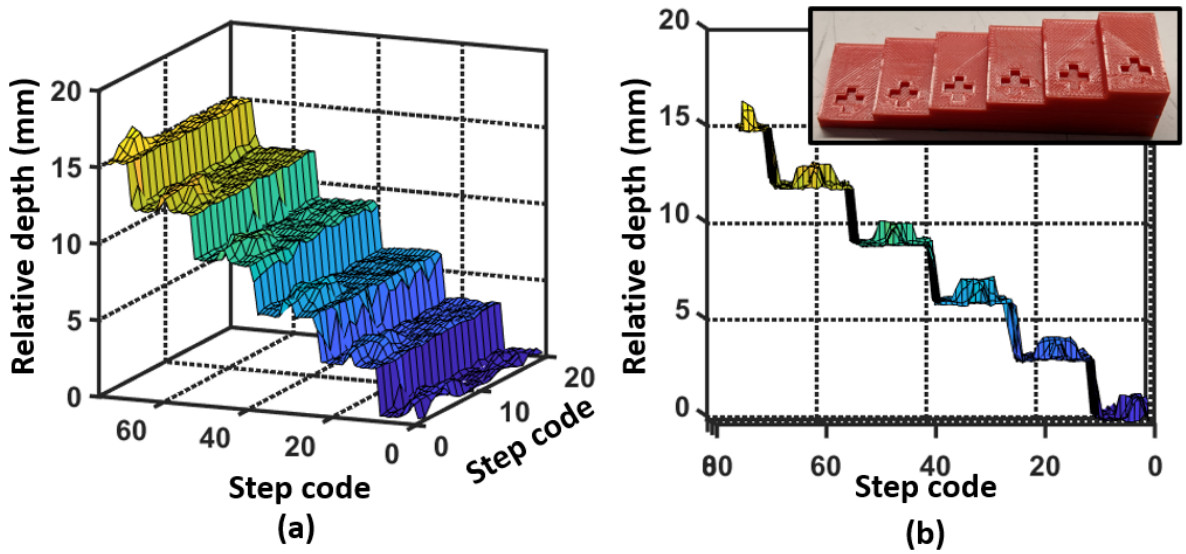

Figure 5.18: (a) and (b) are stairs' 2-D scanning results at different angles.

Lambertian reflectance from the target. The scanned results is shown in Fig. 5.21. The curvature of the surface plane is due to the varied scanning angles, which can be calibrated

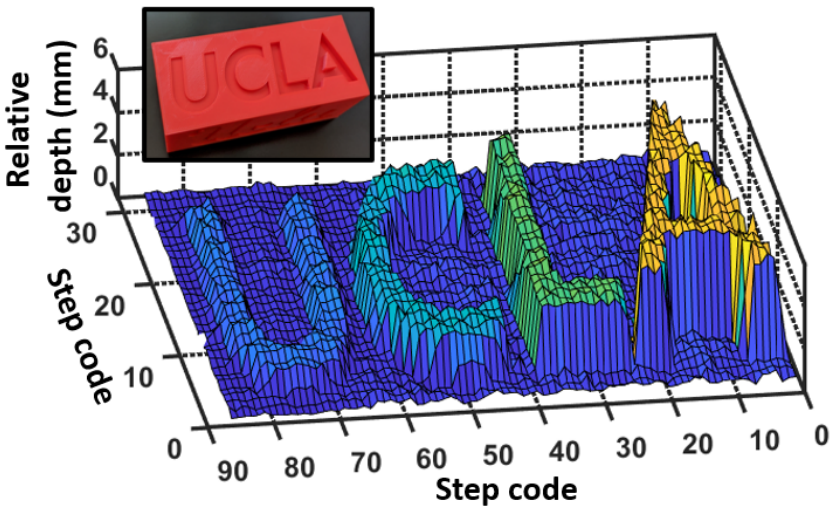

Figure 5.19: 2-D scanning result with an UCLA logo.

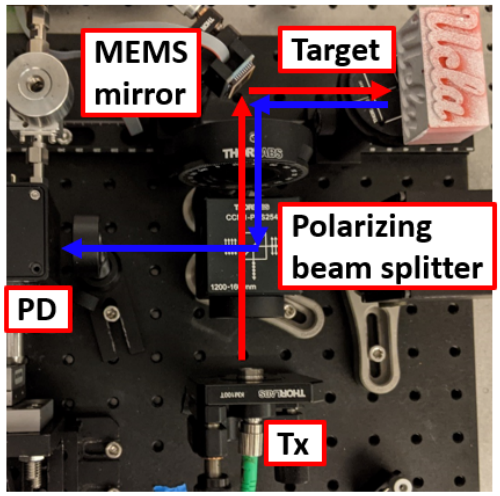

Figure 5.20: Measurement setup of 2-D scanning with MEMS mirror.

with a flat surface reference plane.

5.2.6 System Performance Summary

Table 5.1 summarized the performance of the DSP-based receiver. The power consumption of the AFE and the PLL are shown in Fig. 5.22(a) and Fig. 5.22(b), respectively. At 1-V

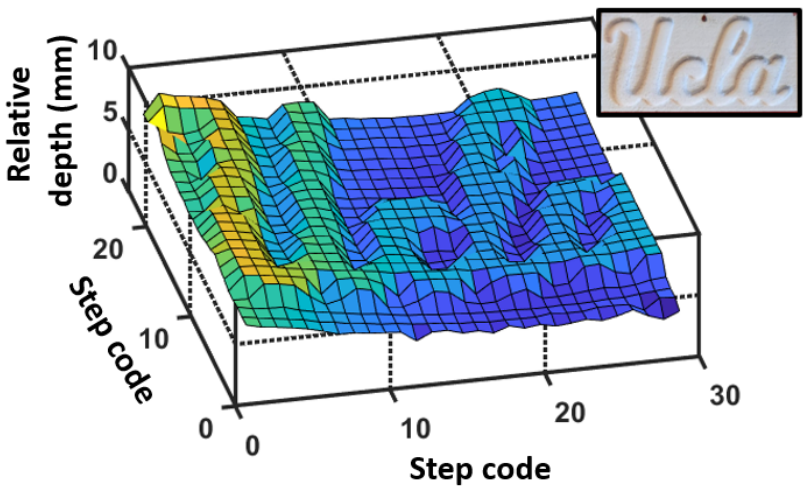

Figure 5.21: Scanning result with MEMS mirror.

supply, the total power consumption is 108 mW, including two AFE channels and a shared local PLL where the AFE dissipates 36 mW per channel and the local PLL dissipates 36 mW with the LO driver. The AFE achieves –65-dBm sensitivity with 60-dB gain tuning range with only ±0.5° relative phase shift. The ring-type VCO has a wide operating range from 5 GHz to 12.5 GHz with 120-fs rms jitter integrated from 1 kHz to 40 MHz offset frequency. According to the figure-of-merit (FoM_{PLL}) of the PLL

$$FoM_{PLL} = 10log[(\frac{\sigma_{t,PLL}}{1s})^2 \frac{P_{PLL}}{mW}], \tag{5.2}$$

where $\sigma_{t,PLL}$ is the rms jitter of the PLL and P_{PLL} is the power consumption of the PLL, the FoM_{PLL} of the this ring-type VCO based PLL is –242 dB.

Table. 5.2 summarizes the circuit performance and compares this work to the state-of-the-art lidar systems. This DSP-based pulsed-coherent lidar system achieves the maximum INL of 30 μm and the precision of 6 μm with 5-MHz integration bandwidth across a 10-cm dynamic range at 2.5-m displacement. A figure-of-merit (FoM_{lidar})

$$FoM_{lidar} = 10log[(\frac{P_{tx}}{D^2})(\frac{\sigma_d^2}{f_{Sa}})], \tag{5.3}$$

is introduced to help to compare receivers. We factor in both the photodiode and the

Receiver	
Technology	28nm CMOS
Active Area	1.3mm×0.3mm
Building block	PI-PGLNA, SHM, PI-PGA, output driver, PLL, and PPG
Supply	1V
Power consumption	108mW
# of channel	2

AFE	
Sensitivity	-65dBm
tuning range	60dB
Phase variation	±0.5°
PLL	
VCO type	ring-VCO
Divide ratio	7.25
Op. freq.	5GHz-12.5GHz
RMS jitter (1kHz – 40MHz)	120fs

Table 5.1: Performance summary of the receiver frontend.

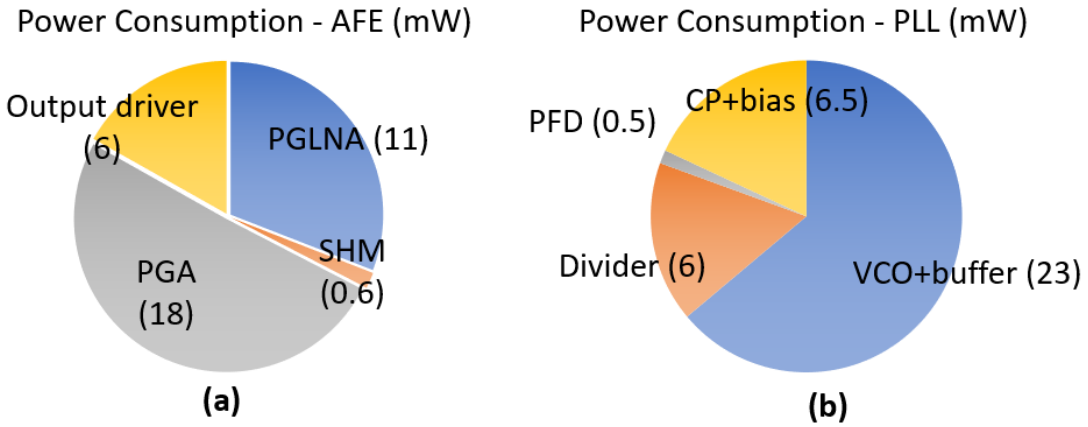

Figure 5.22: Power consumption of: (a) the analog frontend per channel, and (b) the PLL.

electrical readout circuit. The term P_{tx}/D^2 indicates the received optical power (P_{tx} is the transmitted optical power, and D is the displacement). Since the received optical power is not often provided directly in prior publications, we derive the received optical power from the emitted power, the displacement, and assuming optimal path loss. We believe it is reasonable since, in the comparison table, all published results use a mirror as the target to characterize the depth precision. Our receiver achieves a low FoM_{lidar} of –203 dB-J.

	[*ISSCC 2016*]	[*JSSC 2019*]	[*SSC-L 2020*]	[*TIM 2021*]	This work
Architecture	FMCW	Pulsed	Pulsed-coherent	AMCW	Pulsed-coherent
Technology	180nm CMOS 250nm Si-ph	110nm CIS	28nm CMOS	N/A	28nm CMOS
Wavelength	1550nm	473nm	1590nm	1531nm 1534nm	1550nm
Emitted Power (P_{Tx})	10dBm	-5dBm	6dBm	−3dBm	6dBm
$Range_{Max}$	1.4m	16cm	2.5m	5m	2.5m
INL_{Max}	N/A	230µm	100µm	38µm	30µm
Displacement (D)	5cm	14.75cm	250cm	500cm	250cm
Dynamic range	±0.1cm	±1.25cm	±10cm	±0.03cm	±10cm
Depth Precision (σ)	8µm	64µm	9µm	19.2µm	6µm
Sampling rate (f_{Sa}) (Per Pixel)	180kHz	25Hz	5MHz	64kHz	5MHz
FoM_{lidar} (dB-J)	−148	−117	−200	−189	−203

Table 5.2: Performance summary of the lidar system.

5.3 Summary

This chapter demonstrated the measurement results of the lidar system. We characterized the phase-invariant amplifiers. All amplifier achieves less than 1° phase shift. The 1-D scanning has been performed with the precision of 6 μm and the maximum INL of 30 μm. Also, scanned results of the 2-D scanning have been shown with different optical setups using the mechanical stage and MEMS mirror. We proposed a figure of merit to compare the receiver performance where our receiver achieves a low FoM_{lidar} of –203 dB-J.

CHAPTER 6

Conclusion

In conclusion, this thesis presents a pulsed-coherent lidar system that achieves high linearity and sub-10 μm depth precision with a 5-MHz sampling rate. The pulsed-coherent lidar simplifies the optical transmitter design with a single laser source. We developed an analog-based pulsed-coherent receiver with post-edge envelope detection to suppress the walk error and utilize the segmented measurement to detect the carrier's phase shift to improve the precision. Two DSP-based receivers have also been implemented to enhance the robustness of the system to the environment. The homodyne receiver combines the segmented ToF calculation into the DSP. This DSP-based receiver automatically aligned the coarse and the fine measurement by the ADC's clock. The heterodyne receiver with an on-chip LO generation reduces the power consumption and the calibration process, such as I/Q mismatch and the leakage cancellation. The noise analysis of the phase-detection allows us to understand the design choices better, such as the carrier frequency, the dimension of the photodiode, and the ADC requirement. We also develop the narrowband matching network to improve the sensitivity and efficiency of the receiver.

Different architectures of the phase-invariant variable gain amplifiers have been implemented for the circuit implementations, including an RF low-noise amplifier, an analog-tuning variable gain amplifier in CMOS logic, and a discrete-tuning inverter-based programmable gain amplifier. The phase-invariant AFE achieves less than 1° phase shift. In addition, different clock generations, including a type-II PLL using a ring-type VCO, have been used to minimize the noise contribution from the additive noise.

We integrate the electrical receiver with an optical transmitter and perform both 1-D and 2-D scanning for the system integration. The system successfully achieves the targeted precision and the sampling rate. We also show the scanned image results. With the capabilities of high precision and high sampling rate in our system, this system can enhance the current usages and enable new territories of the applications.

There are several avenues of future work to further enhance the performance. Discrete components for optics and electronics introduced performance variability and noise coupling. The system can achieve better range integrating the photodiodes, multi-channel AFE, on-chip ADCs, and DSP into a single chip. Frequency spurs also limited our frontend performance. We can potentially improve the injected noise by using a better designed fractional-N frequency synthesis by the PLL. Furthermore, a frequency comb can be utilized for the parallelism scanning as mentioned in section 3.2.4 to accelerate the scanning frame rate.

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