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A 13.56-MHz −25-dBm-Sensitivity Inductive Power Receiver System-on-a-Chip with a Successive-Approximation Resonance Compensation Front-End for Ultra-Low-Power Medical Implants

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Abstract

Battery-less and ultra-low-power implantable medical devices (IMDs) with minimal invasiveness are the latest therapeutic paradigm. This work presents a 13.56-MHz inductive power receiver system-on-a-chip with an input sensitivity of −25.4 dBm (2.88 μW) and an efficiency of 46.4% while driving a light load of 30 μW. In particular, a real-time resonance compensation scheme is proposed to mitigate resonance variations commonly seen in IMDs due to different dielectric environments, loading conditions, and fabrication mismatches, etc. The power-receiving front-end incorporates a 6-bit capacitor bank that is periodically adjusted according to a successive-approximation-resonance-tuning (SART) algorithm. The compensation range is as much as 24 pF and it converges within 12 clock cycles and causes negligible power consumption overhead. The harvested voltage from 1.7 V to 3.3 V is digitized on-chip and transmitted via an ultra-wideband impulse radio (IR-UWB) back-telemetry for closed-loop regulation. The IC is fabricated in 180-nm CMOS process with an overall current dissipation of 750 nA. At a separation distance of 2 cm, the end-to-end power transfer efficiency reaches 16.1% while driving the 30-μW load, which is immune to artificially induced resonance capacitor offsets. The proposed system can be applied to various battery-less IMDs with the potential improvement of the power transfer efficiency on orders of magnitude.

Index Terms—

back-telemetry; energy-harvesting; implantable medical device (IMD); inductive power receiver; IR-UWB; rectifier; resonance compensation; resonant power transfer; successive approximation; voltage regulation; wireless power transfer

I. Introduction

Wireless power transfer has been widely used for medical implants. Prior art in real-time and regulated power transfer for implantable medical devices (IMDs) has primarily tackled scenarios where the power consumption of IMDs is in the range from mW to W [1–6].

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Meanwhile, IMDs with less power consumption and the associated invasiveness become one of the latest paradigms [7–16]. As the power consumption of IMDs is reduced to tens-μW or less, the power link can be substantially elongated with a moderate Tx power, which could open the door to many therapeutics that are yet to come [8]. These IMDs are also expected to form distributed sensory and actuation systems in place of conventional centralized counterparts [17–19]. The cardiac sensing and pacing network based on wirelessly powered micro-devices directly implanted in the heart is a such system [8]. The continuous movement requires frequent and periodic adaptation of the energy-harvesting front-end.

Sophisticated designs of wireless power transfer systems in the power ratings from few-μW to hundreds-μW have not been insensitively discussed in the literature. These systems should prioritize sensitivity and stress less on the power transfer efficiency which tends to be higher for heavier loads [2–4, 20, 21]. Therefore, in terms of the rectification topology, active rectifiers consisting of power-hungry high-speed comparators may simply be replaced with optimally designed passive rectifiers [22, 23].

One particular challenge for energy-harvesting IMDs is the vulnerability to resonance variations, which could be induced from fabrication mismatches, different implantation sites, movement, buildup of scar tissue, and varying load conditions, etc. The actuation device, in particular, would pose a different equivalent input capacitance of the rectifier depending on the stimulation strength and on/off status [24]. One approach is to purposefully decrease the quality factor in a trade-off for a wider bandwidth, which, of course, sacrifices the optimal efficiency [24–26]. Recent researches start to investigate the active compensation method [5, 27–30], where a capacitor bank is adaptively tuned to compensate for resonance variations. The ideal implementation of such circuits should converge to the optimal solution fast and cause negligible power consumption overhead that would otherwise hamper the sensitivity of the system.

Another challenge is the output voltage regulation. A typical way to regulate the harvested power is a cascaded two-step approach, i.e., RF-DC rectification and DC regulation, with the corresponding two-step losses [5, 9, 10, 15, 30]. To combine the two stages, the resonant regulating rectification method has recently been adopted [1, 4, 18], where the operation of the rectifier is duty-cycled to stabilize the output voltage. However, the high-speed comparators in the active rectifiers pose a challenge for low-power IMDs. The method is also associated with excessive output voltage fluctuations.

This work presents a 13.56 MHz inductive power receiver system-on-a-chip for IMDs in the power range from few-μW to hundreds-μW. It achieves an input power sensitivity of 2.88 μW and regulates the output voltage from 1.7 V to 3.3 V with over 40 dB regulation. An ultra-wideband impulse radio (IR-UWB) back-telemetry is employed to transmit the digitized output voltage. A longstanding issue for power-receiving IMDs, i.e., resonance variations, is addressed with a novel successive-approximation-resonance-tuning (SART) technique, which offers a 6-bit compensation dynamic range and causes negligible power consumption overhead. Targeting a 30-μW load at the link distance of 2 cm, the system achieves an end-to-end efficiency of 16.1% regardless of an artificially induced 10-pF

resonance capacitor offset. The resonance adaptation technique could improve the power transfer efficiency by orders of magnitude for realistic IMDs.

The following of the paper is organized as follows. Section II describes the overall architecture. Section III discusses the implementation of SART, optimization of the rectifier, and the magnetic link. Section IV describes the implementation of the ADC and IR-UWB back-telemetry for voltage regulation from the transmitter. Section V presents the measurement results and comparisons with the prior art. Finally, section VI concludes the paper.

II. System Overview

The overall block diagram of the IC is shown in Fig. 1, which consists of an RF-DC rectifier with SART, a 7-bit SAR ADC for digitizing the harvested voltage, $V_{DD,HARV}$, and an IR-UWB transmitter as the back-telemetry. Their operations are heavily duty-cycled to reduce the power consumption as shown in the schedule map in Fig. 2. The clock signal is generated by a relaxation oscillator running at approximately 5 kHz. Each SART execution only lasts less than 0.5% of the system cycle, and therefore, does not hamper the power-receiving efficiency. The system cycle including SART, voltage digitization, and back-telemetry operations is executed at about 2 Hz to address the ever-changing dielectric environments and loading conditions.

A coarse bandgap reference (BGR-course) and a local low-dropout regulator (LDO) implemented in 3.3-V process generate the voltage supply for the internal circuitry at approximately 1.6 V. Another fine bandgap reference (BGR-fine) creates a stable voltage reference with a power-supply-rejection-ratio (PSRR) over 60 dB. The ADC is designed with seven effective bits to provide 42 dB regulation of the output voltage. An IR-UWB transmitter is implemented as the back-telemetry due to its low power consumption and potential sharing with other bioelectric sensory functions. A 4-bit header and the 7-bit ADC output forming 11 bits are serially streamed to the transmitter.

III. Power-receiving Front-end with Successive Approximation Resonance Tuning

A parallel capacitor, C_P, is typically needed to tune the resonant frequency of the receiving coil to boost the voltage swing and improve the power transmission efficiency [8]. The latest research focuses on active compensation for any resonance variations by tuning the resonance capacitor. While [28] employs thermometer-coded capacitors based on PMOS varactors to realize a 3-bit dynamic range, [5, 27, 29] implement binary-weighted capacitor banks at the rectifier input. On-chip optimization logics have been implemented as the hill-climbing algorithm [5, 29], in which each step of operation only adapts to an adjacent code. Therefore, the convergence time exponentially grows with the dynamic range. [30] proposes a gradient descent algorithm with concerns on the logic complexity and the associated power consumption. Also, the work monitors the rectified output voltage requiring excessive time before stabilization [30]. It is noteworthy that for most IMDs, resonance compensation is not

only needed as a one-time calibration, as the dielectric environment and loading condition may change over time.

To address these challenges, this work proposes the SART scheme which accurately and timely compensates for any resonance capacitor offsets. SART is periodically executed to address the ever-changing resonance variations while the rectifier continuously salvages the inductive power. This technique can be applied to a variety of energy-harvesting IMDs.

A. Architecture and Compensation Logic

The circuit schematic of the proposed power-receiving front-end with SART is illustrated in Fig. 3. A 6-bit binary-weighted capacitor bank is implemented in parallel with a Dickson-stage passive rectifier [31]. Each capacitor bank selection leads to a variation in the RF signal amplitude. The swings corresponding to two consecutive capacitor bank selections are detected and sampled on two hold capacitors, respectively. The comparison between the two is made by a zero-static-power StrongARM latch comparator [32] as the input to the SART logic.

The impedance of a coil is approximately symmetric against the offset of the resonance capacitor. And the higher impedance leads to a larger voltage swing. Therefore, the proposed resonance compensation algorithm is essentially to adapt the capacitor bank to achieve the maximum voltage swing. The SART algorithm is illustratively depicted in Fig. 4 in a 4-bit scenario. It starts from comparing ¼ and ¾ of the full-scale dynamic range, i.e., ‘0100’ and ‘1100’, and the result is updated as the MSB. Then, it compares ¼ and ¾ of the rest of the range, i.e., ‘MSB,010’ and ‘MSB,110’, with the result updated as the second significant bit, and so forth.

For an N-bit dynamic range, the algorithm requires N such comparisons, or 2N clock cycles, to achieve the optimal selection code. The convergence time of SART is proportional to the dynamic range, while the prior art exhibits an exponential relationship [5, 27–29]. A complete logic-flow chart for adapting a 6-bit capacitor bank is shown in Fig. 5.

B. Rectifier

The passive rectifier consists of 5 stages (N=5) and employs native transistors to boost the rectification efficiency [25]. The load current, I_{LOAD}, on the order of few-μA is the design target, which represents the dissipation of typical IMDs. The width of each transistor is sized to be 5 μm while the gate length is kept at the minimal value of 0.5 μm. The simulated rectification efficiency versus I_{LOAD} is shown in Fig. 6. It exceeds 50% for I_{LOAD} from 0.6 μA to 10 μA. The optimal gate-sizing for other load ratings can be simply achieved by proportionally scaling up or down the transistors’ width, while only in the high-power regime, active rectifiers would result in better efficiencies [22, 23]. The rectification efficiency against the output voltage, V_{OUT}, is shown in Fig. 7 demonstrating stable performances for the targeted loads.

C. Switched Capacitor bank

Switched capacitors in binary-weighted values have been implemented in prior resonance compensation front-ends, which could easily suffer from nonlinearity issues due to fabrication mismatches [5, 27, 30]. This work implements the capacitor bank as 63 identical unit cells each consisting of a 400-fF metal-insulator-metal capacitor and an NMOS switch with W/L=24 μm/0.18 μm as shown in the schematic in Fig. 8(a), which contributes to a sufficiently high quality-factor of approximately 1000 or dissipation factor of 1/1000 according to circuit simulation (note that it is only the quality factor or dissipation factor of a switched capacitor unit, not the Rx tank). Due to the parasitic capacitance of the switch, the unit cell exhibits an equivalent capacitance of approximately 20 fF in the *off* state. Therefore, the tuning resolution would be 380 fF and the overall range equals 24 pF. The layout of the capacitor bank is shown in Fig. 8(b).

D. Magnetic Coupling Link

Tx and Rx coils are designed as shown in Fig. 9 and Table I demonstrates their key parameters. The Rx coil is designed with a small diameter of 12 mm to fit miniaturized IMDs. The inductances of the Tx and Rx coils are simulated to be 5.76 μH and 6.36 μH, respectively. A 21.7-pF parallel capacitor, C_P, is required to make the Rx coil resonate at 13.56 MHz, and the Tx coil employs an additional L-matching section to match the 50-Ω power source.

The offset of C_P, $C_{\Delta P}$, will affect the voltage swing and, therefore, the power transfer efficiency. $C_{\Delta P}$ up to 10 pF is considered, which mimics realistic situations when the Rx coil is placed in different dielectric media, for example, in water as a contrast to in the air. The power transfer efficiency for different $C_{\Delta P}$ is normalized as shown in Fig. 10. As expected, systems with higher quality factors are more vulnerable to the offset.

IV. Voltage Regulation and UWB Telemetry

Conventional wireless power receivers typically employ separate LDOs to regulate rectified voltages [5, 9, 10, 15, 30]. The two-step conversion incurs additional inefficiency. Also, two large decoupling capacitors are typically required before and after the regulation to reduce the ripple of the harvested voltage and to stabilize the regulation feedback, respectively. The resonant regulating rectification scheme is associated with timing-induced losses of the comparators. To address the challenge, either power-hungry high-speed comparators can be used [1, 4, 18] or is the system's complexity significantly increased with the adoption of latency-compensation schemes [33].

This work intends to regulate the harvested voltage from the transmitter via the on-chip voltage digitization and back-telemetry. A 7-bit ADC provides about 42 dB regulation ratio. An IR-UWB transmitter with negligible power consumption is implemented for potential sharing with other sensory functions as well.

A. SAR ADC

A bottom-plate sampling SAR ADC with a 7-bit dynamic range is implemented as shown in the schematic in Fig.11. All sample-and-hold buffers are power-gated only for the operation duration as shown in Fig. 3 to minimize power consumption. The 7-bit ADC output is serialized and packetized with a '0101' header for back-telemetry transmission.

B. UWB Transmitter

IR-UWB is widely used in IMDs due to its low power consumption and miniaturized antenna form factors [34–37]. This work employs the filtered edge-combining technique for generating FCC-compliant UWB impulses [34, 38–40]. A mono-pulse is initially generated from a delay cell and subsequently passed through an on-chip passive filter as shown in the schematic in Fig. 12.

M_1 operates in class-C and the upper cascode transistor, M_2, is implemented to avoid voltage overshooting. The values of the filter components, C_1, C_2, L_1, and L_2 equal 981 fF, 444 fF, 614 pH, and 1.69 nH, respectively. The estimated drain capacitance of M_2 equals 221 fF and is absorbed to C_1 to determine the filtering characteristics as shown in Fig. 13. The transient waveform of each emitted impulse on a 50-Ω load and the corresponding frequency spectrum are shown in Fig. 14(a) and (b), respectively. The system only requires transmitting about twenty impulses per second, which easily complies with the FCC emission mask [38].

Since the transmitter is triggered by the positive edge, the input symbols are first converted to return-to-zero formats. Each logical '1' and logical '0' are converted to '10' and '00', respectively. Hence, the symbol rate of the transmitter is half of the clock frequency. Each impulse is simulated to consume about 65.6 pJ (DC energy) and the emitted energy is about 2.7 pJ. Twenty emissions per second correspond to the power dissipation of 1.3 nW.

V. Measurement

The IC was fabricated in 180-nm CMOS process with the microphotograph shown in Fig. 15. The overall size of the IC is about 1.7 mm^2. Its current dissipation is measured to be 750 nA. The IC operates at a minimal $V_{DD,HARV}$ of 1.7 V, which requires an input power of 2.88 μW or −25.4 dBm that defines the sensitivity of the system. The power breakdown chart is demonstrated in Fig. 16.

The Tx and Rx coils as shown in Fig. 9 are fabricated on FR4 laminates. The Tx coil is matched to a 50-Ω signal source at 13.56 MHz. The power receiver incorporates a simple monopole antenna of 12 mm length for IR-UWB back-telemetry. A horn antenna cascaded with a band-pass filter and a low-noise amplifier is positioned 30 cm away as the back-telemetry receiver as shown in Fig. 17.

The ADC output versus the harvested voltage is wirelessly measured with remarkable linearity as shown in Fig. 18. The result also verifies the proper design of the auxiliary blocks such as the BGRs and the local LDO. The integral nonlinearity (INL), i.e., the discrepancy between the measurement codes and the ideal values (red line), is plotted in Fig. 19, which rarely exceeds a half LSB.

Two power receivers #A and #B are assembled with #B incorporating an additional 10-pF parallel capacitor as shown in Fig. 20. They are used to drive a 300-kΩ resistor that manifests a typical tens-μW IMD. Upon wireless power onset, sample #A automatically adapts SW_5~SW_0 to '100100', while #B adapts to '001010'. The code difference is 26 that corresponds to 9.9 pF as each switched capacitor unit contributes 380 fF. This result is remarkably close to the nominal value of the additional capacitor, 10 pF.

The power transfer efficiency as a function of the Tx-Rx distance is investigated. The measurement is performed at the distances of 2 cm, 3 cm, 5 cm, and 8 cm. The Tx power is adjusted until the wireless reading shows '1001100' indicating an output voltage of 3 V as shown in Fig. 21. The end-to-end efficiency is calculated as the ratio between the load power, 30 μW, and the Tx power (Fig. 22). At 2 cm, the overall link efficiency reaches as high as 16.1%. The efficiencies for samples #A and #B are remarkably close with a discrepancy of less than 10%.

Since the rectification and loading efficiencies equal 49.9% and 93.02% (10/10.75), respectively, the inductive coupling efficiency as the theoretical power transfer limit can be speculated and plotted in Fig. 22. The power breakdown of the 2-cm scenario given the Tx power of 186.2 μW is shown in Fig. 23.

The input impedance of the rectifier is simulated to incorporated a parallel resistor of 3.27 kΩ [24]. Therefore, considering the inductance of the Rx coil, the quality factor of the front-end tank approximately equals 6. Without resonance compensation, a capacitor offset of 10 pF would degrade the link efficiency by 89% according to simulations in Fig. 10. The speculated result without SART is also plotted in Fig. 22.

A piece of 1.5-cm thick pork loin is used to entirely cover the power receiver to verify the operation of the inductive coupling and IR-UWB data links as shown in Fig. 24. Particularly, while the IR-UWB signal shows a weakened swing due to tissue losses (Fig. 24(c–f)), the power transfer link efficiency does not change at all, which is manifested by the unchanged harvested voltage. It is consistent with the nature of magnetic coupling. The feature was also verified in our recent *in vivo* experiment in which induction-based power transfer was demonstrated through a porcine model's chest [8].

Exemplary waveforms of the SW_5~SW_0 adaptation are demonstrated in Fig. 25. Once SART is executed, the convergence only takes 12 clock cycles or 2.4 ms. The response of the power receiver to transient resonance capacitor offsets is measured with the assist of an off-the-shelf digitally controlled capacitor, IXYS NCD2100, that is connected in parallel at the front-end (Fig. 26). The output node of the power receiver connects the load resistor of 300 kΩ and a decoupling capacitor of 47 μF. The capacitor offset is changed between 11 pF and 28 pF every 8 s and the output waveform is shown in Fig. 27. While a voltage droop occurs with each switching, the output voltage will resume a close value. The recovery time is dependent on the decoupling capacitance.

The capacitance of NCD2100 is swept in its full range. 6.6 pF to 37.553 pF is covered with 10 control bits including course and fine bits. The capacitance as a function of the control code is demonstrated in the inset of Fig. 28 according to its datasheet [41]. The dependence

is not entirely linear. Measurement shows that the proposed IC accurately compensates for the offset in its full dynamic range as shown in Fig. 28. The output voltage stays relatively stable for the resonance capacitor offset from 6.6 pF to about 29 pF as shown in Fig. 29, which corresponds to the self-resonant frequency of the Rx tank up to about 26.5 MHz. Small fluctuations exist as the system's operation is based on discrete compensation capacitance values. Only when the capacitor offset is out of the compensation range, will there exhibit a dramatic drop of the output voltage.

The proposed resonance compensation technique is compared with the prior art as summarized in Table II. The SART technique is time- and energy-efficient, and, therefore, not only addresses one-time calibration but offers the real-time adaptability to ever-changing dielectric environments and loading conditions. State-of-the-art inductive power receivers for low-power IMDs are further compared in Table III. This work features the lowest input power sensitivity making it particularly suitable for powering ultra-low-power IMDs. An end-to-end efficiency of about 16% is achieved regardless of a 10-pF capacitor offset when driving a 30-μW load. Since a high power transfer efficiency is increasingly more challenging for lighter loads, the efficiency normalized to the corresponding load is considered.

VI. Conclusion

This work proposes a 13.56 MHz inductive power receiver system-on-a-chip for ultra-low-power IMDs. The power receiver achieves an input power sensitivity of −25.4 dBm and an efficiency of 46.4% while driving a 30-μW load. The output voltage from 1.7 V to 3.3 V can be regulated from the transmitter based on an IR-UWB back-telemetry carrying the real-time harvested voltage readings. To mitigate the challenge of resonance variations in energy-harvesting IMDs, this work proposes a successive approximation resonance compensation scheme that converges efficiently and causes negligible power consumption overhead. This technique not only addresses one-time calibration but offers the real-time adaptability to ever-changing dielectric environments and loading conditions. Precise compensation accuracy is verified through experiments in which resonance capacitor offsets are artificially induced. The end-to-end power transfer efficiency reaches 16.1% at 2-cm Tx-Rx distance when driving the 30-μW load. The proposed power-receiving system-on-a-chip can be applied to various battery-less IMDs and improves the power transfer efficiency by orders of magnitude.

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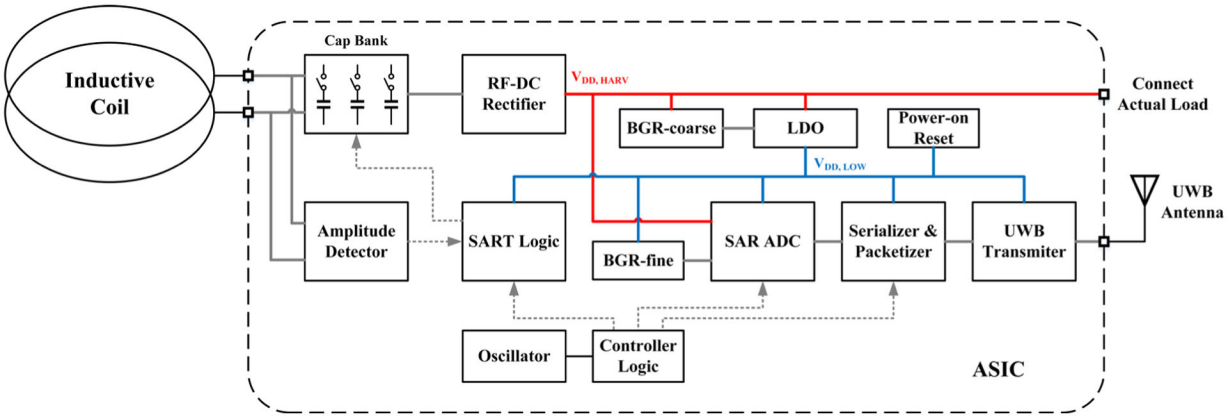

Fig. 1.
Overall block diagram of the proposed inductive power receiver.

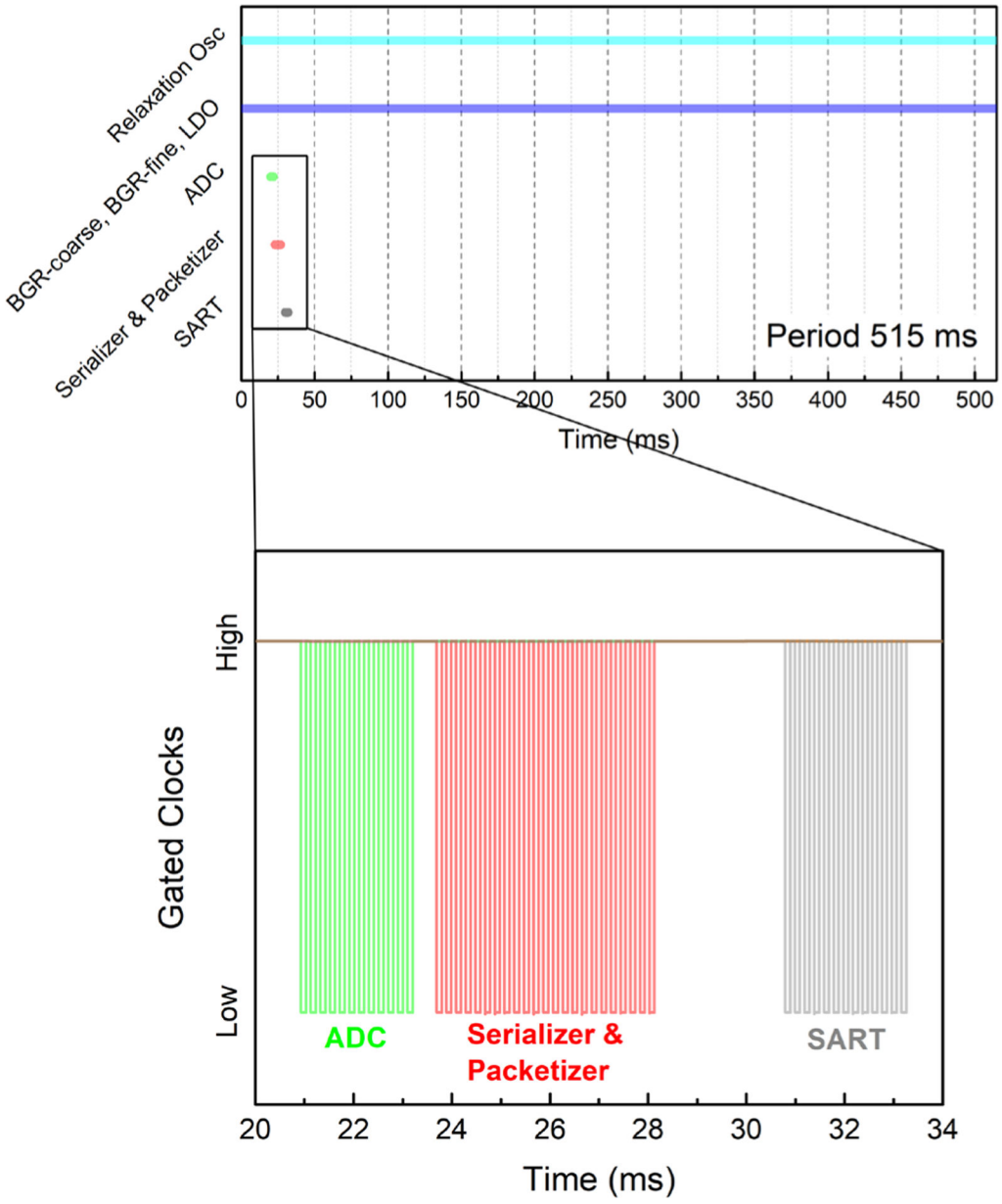

Fig. 2.
System timing schedule for duty-cycling.

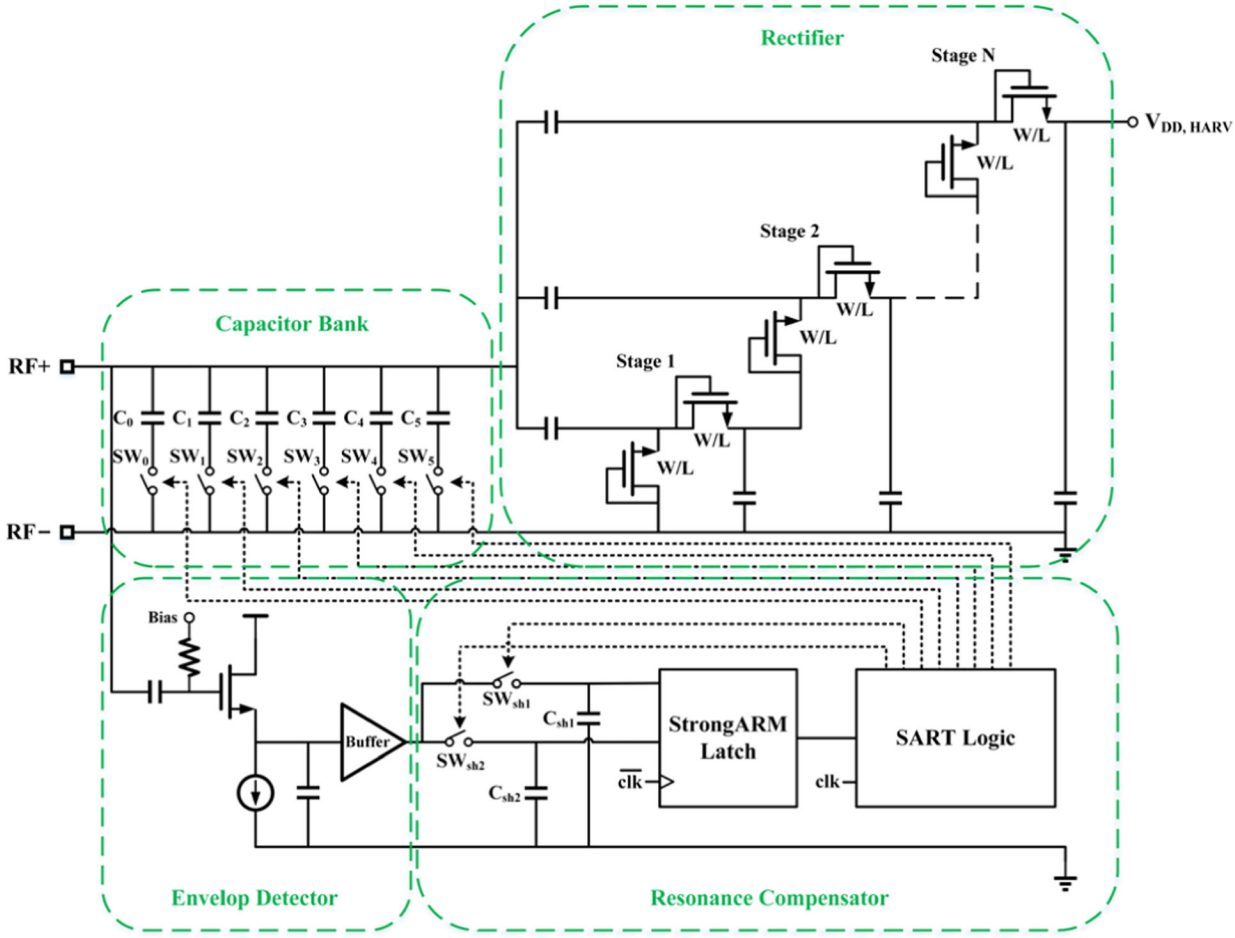

Fig. 3.
Circuit schematic of the proposed power-receiving front-end with SART.

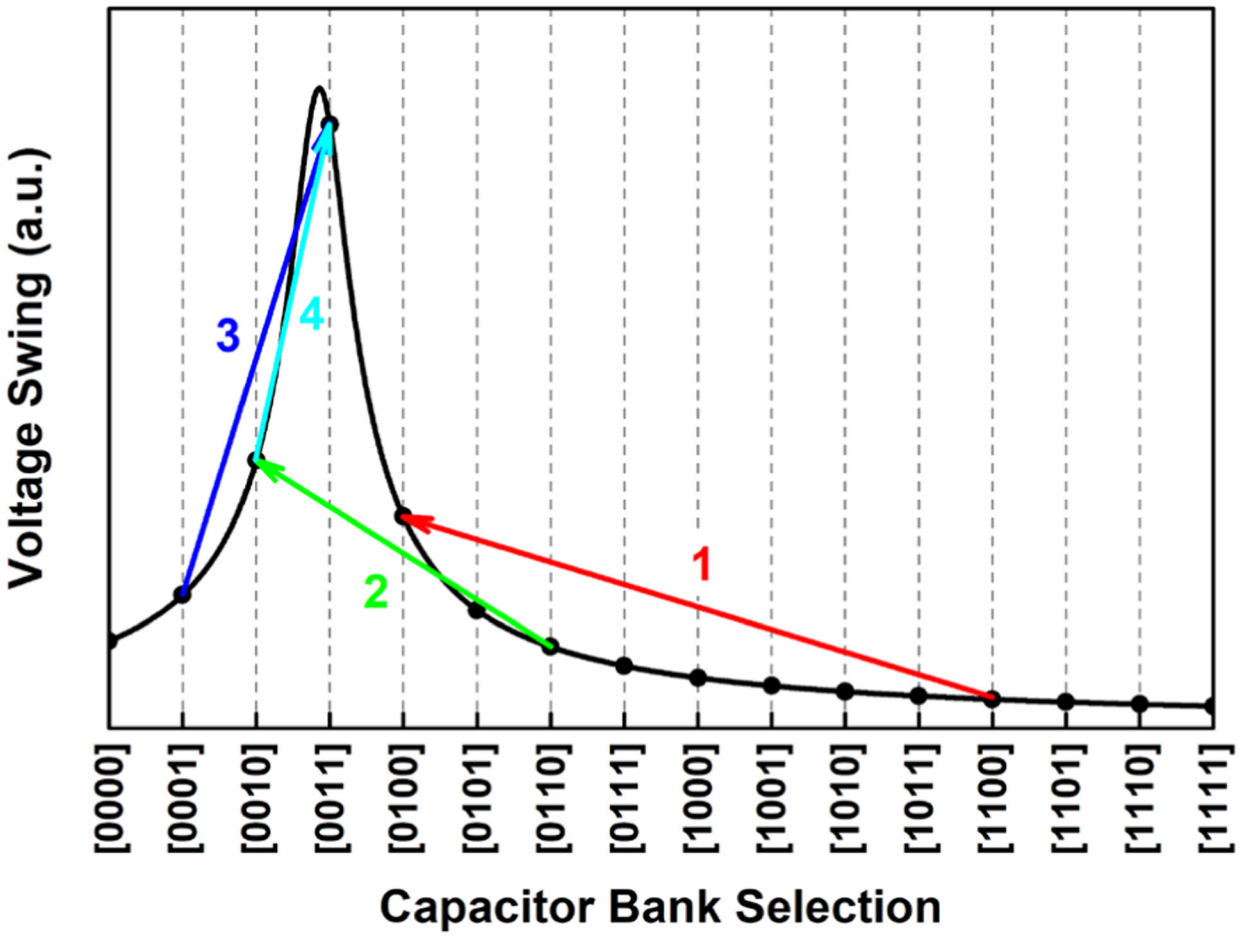

Fig. 4.
Illustration of the successive approximation algorithm in a 4-bit scenario.

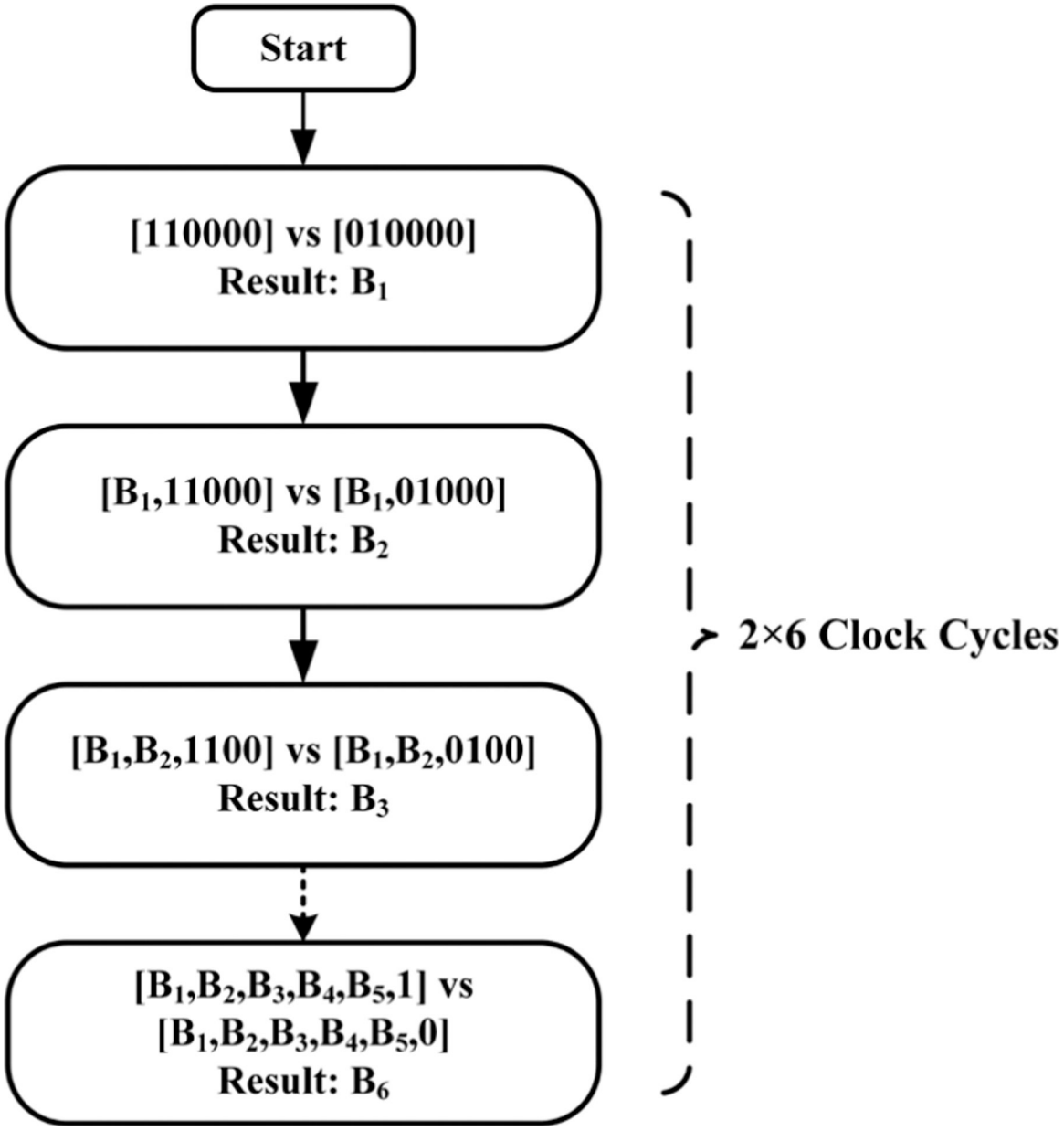

Fig. 5.
Logic-flow chart for the 6-bit SART.

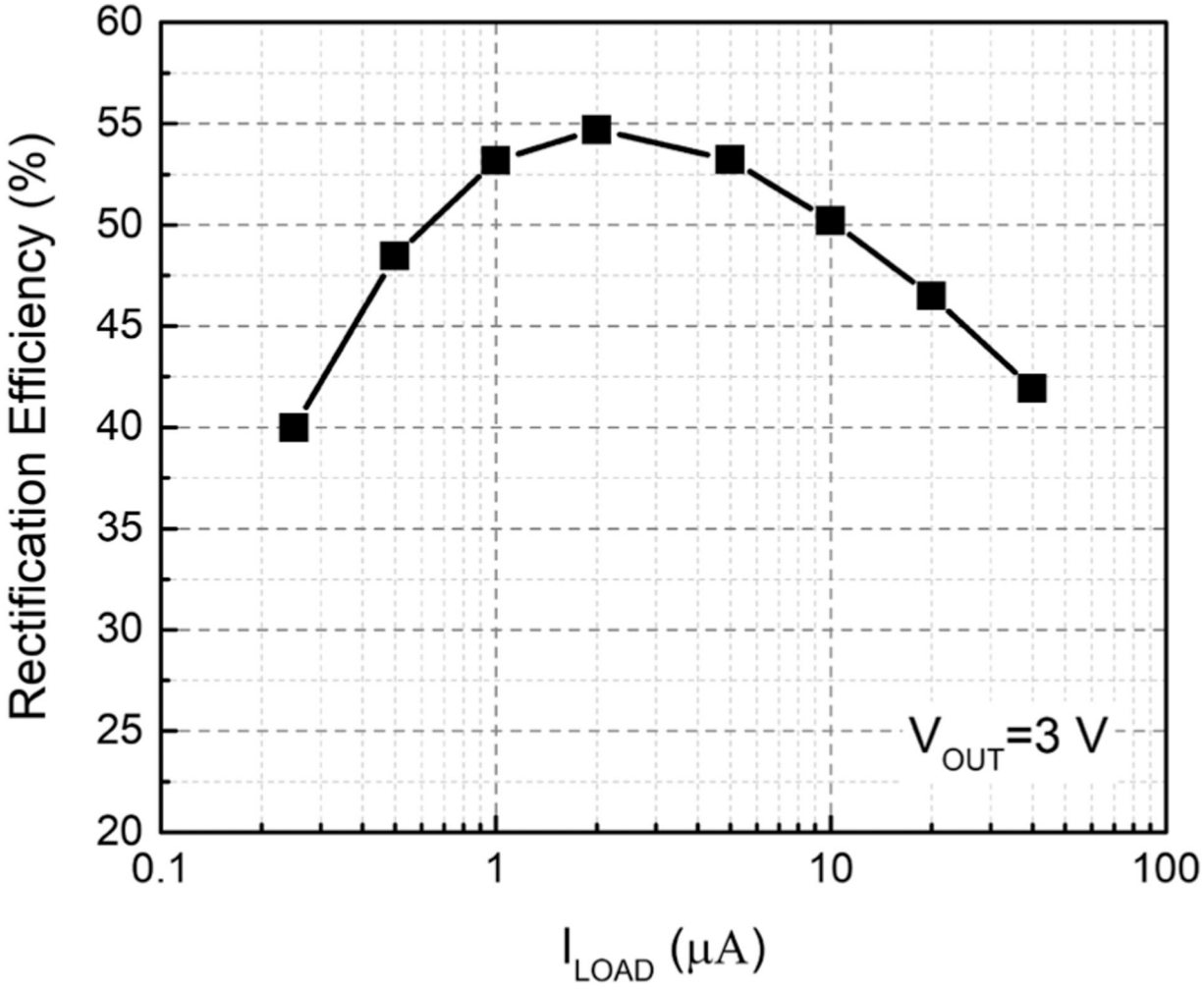

Fig. 6.
Rectifier efficiencies for different I_{LOAD} at V_{OUT} of 3 V.

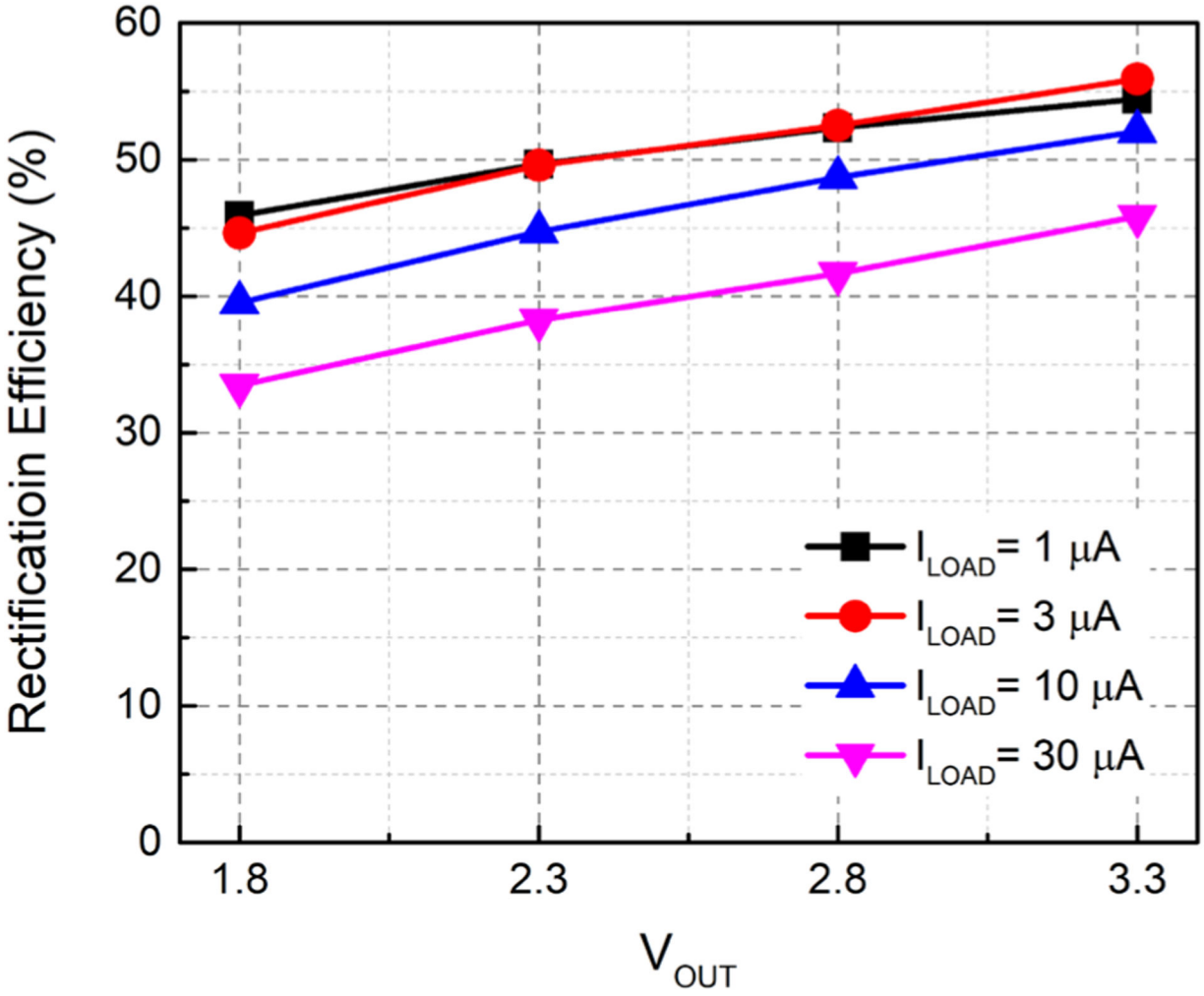

Fig. 7.
Rectifier efficiencies at different V_{OUT} for I_{LOAD} of 1 µA, 3 µA, 10 µA, and 30 µA, respectively.

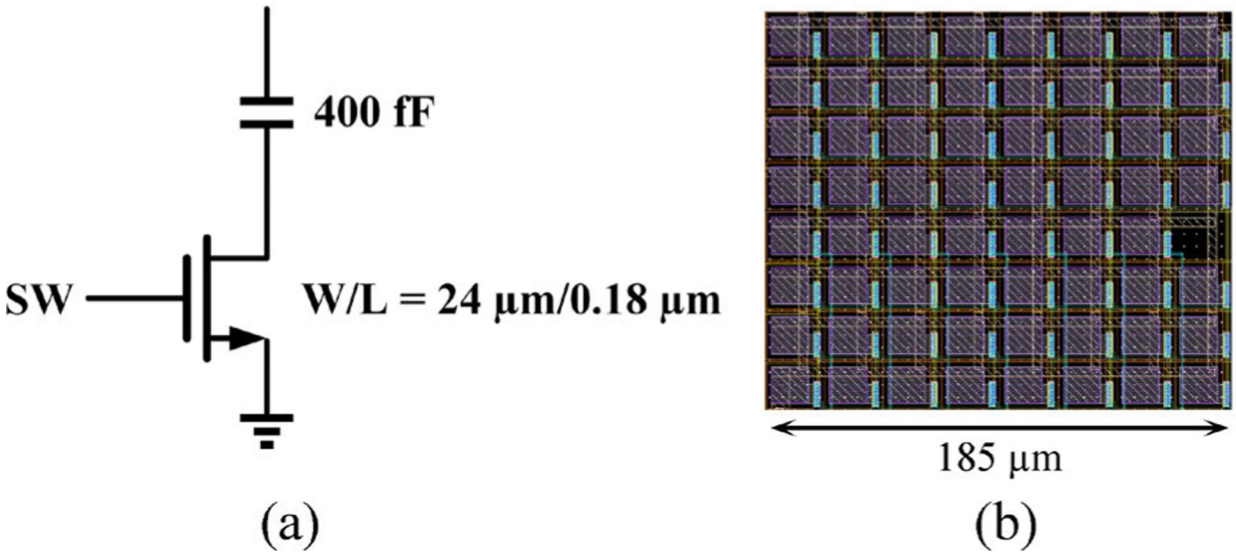

Fig. 8.
(a) Circuit schematic of each switched capacitor unit. (b) Layout of the 6-bit switched capacitor bank array.

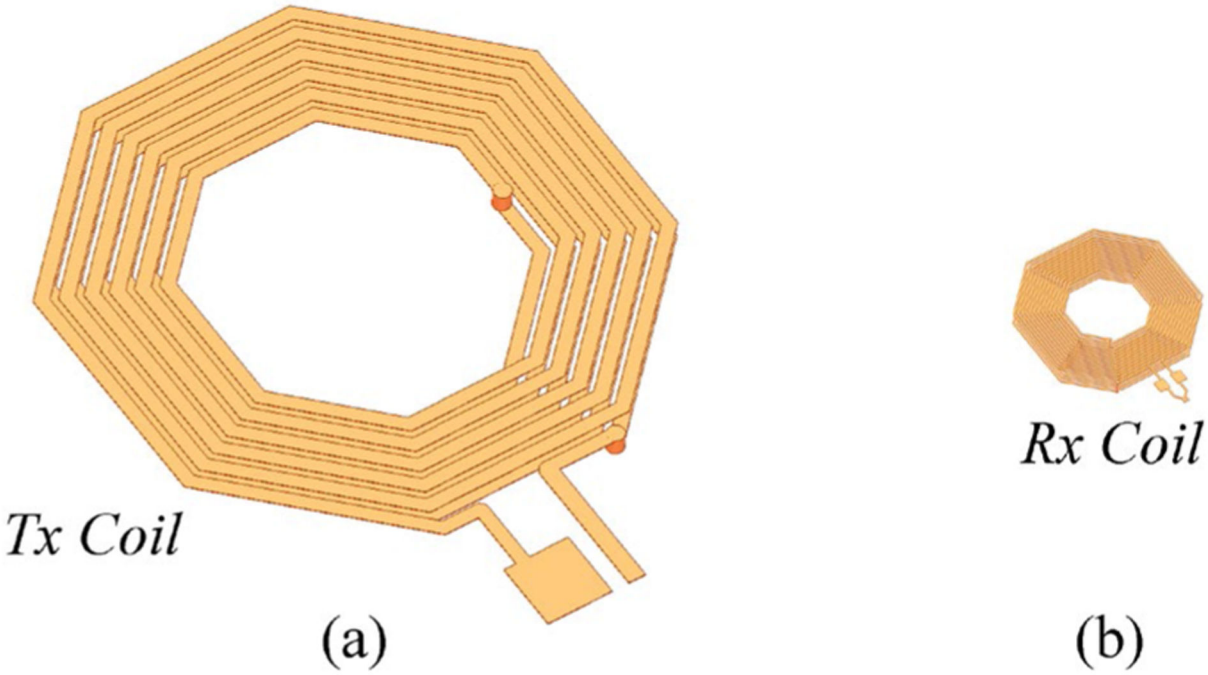

Fig. 9.
Tx and Rx coils.

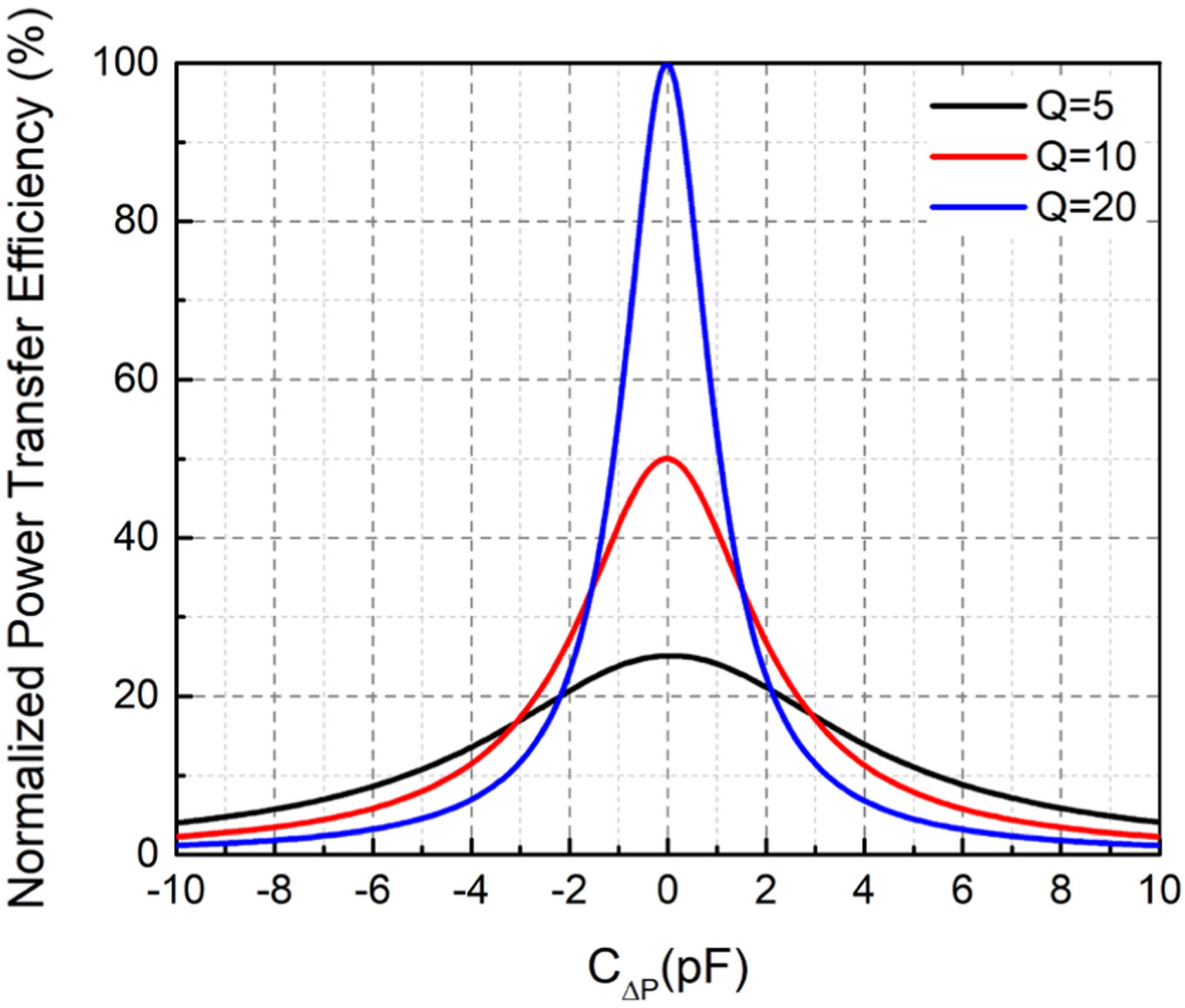

Fig. 10.
Normalized power transfer efficiency against the resonance capacitor offset in the Rx coil.

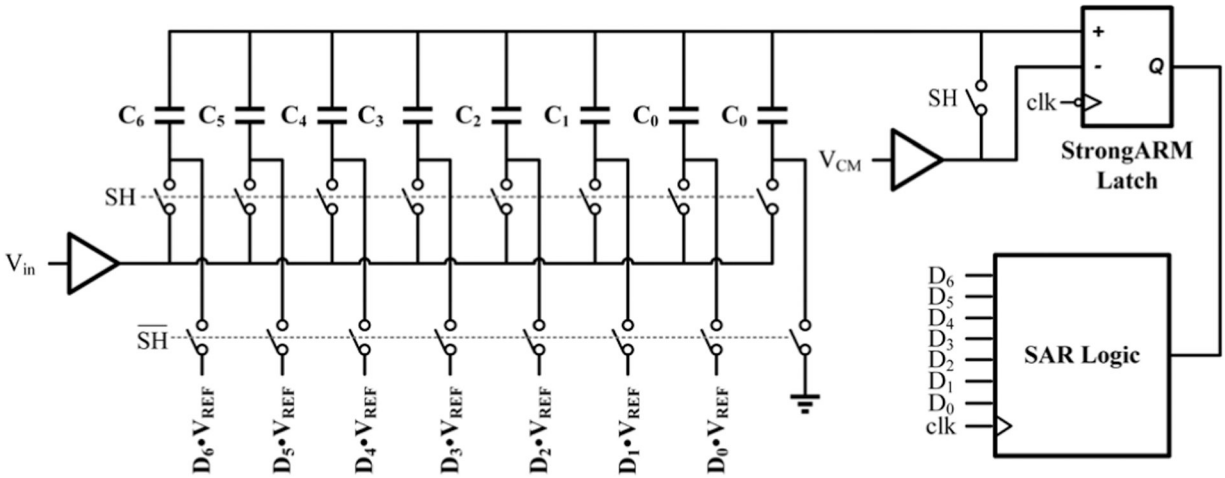

Fig. 11.
Circuit schematic of the bottom-plate sampling SAR ADC.

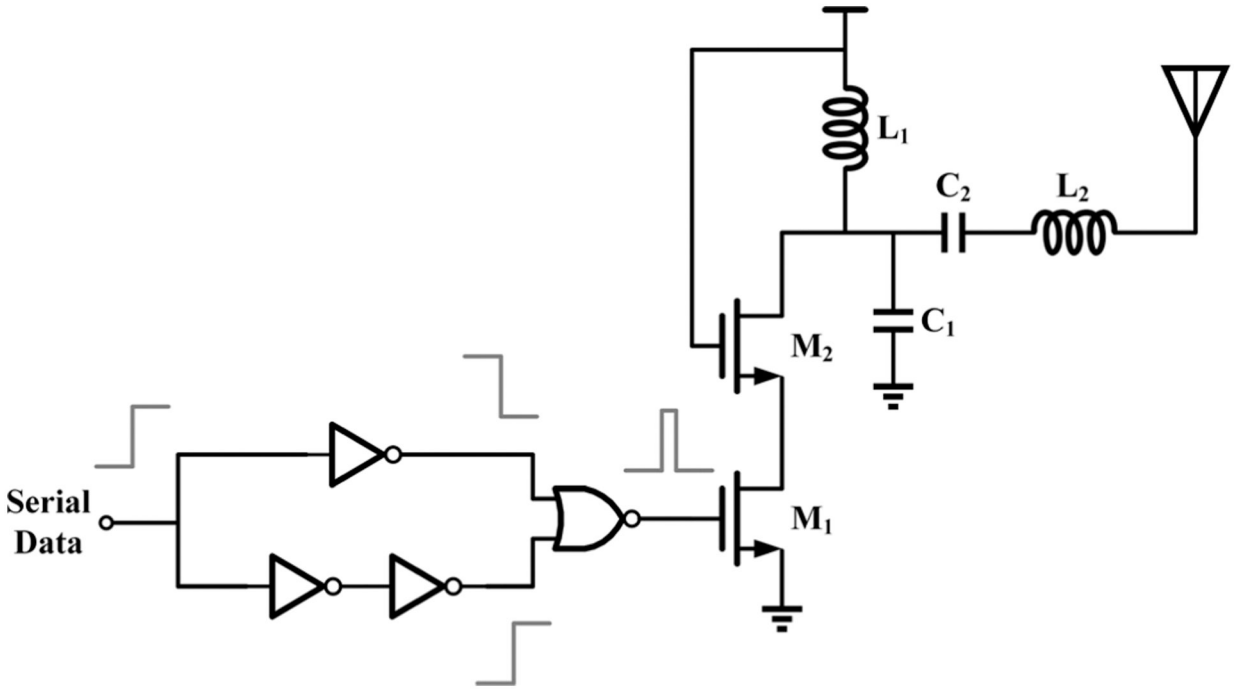

Fig. 12.
Circuit schematic of the IR-UWB transmitter.

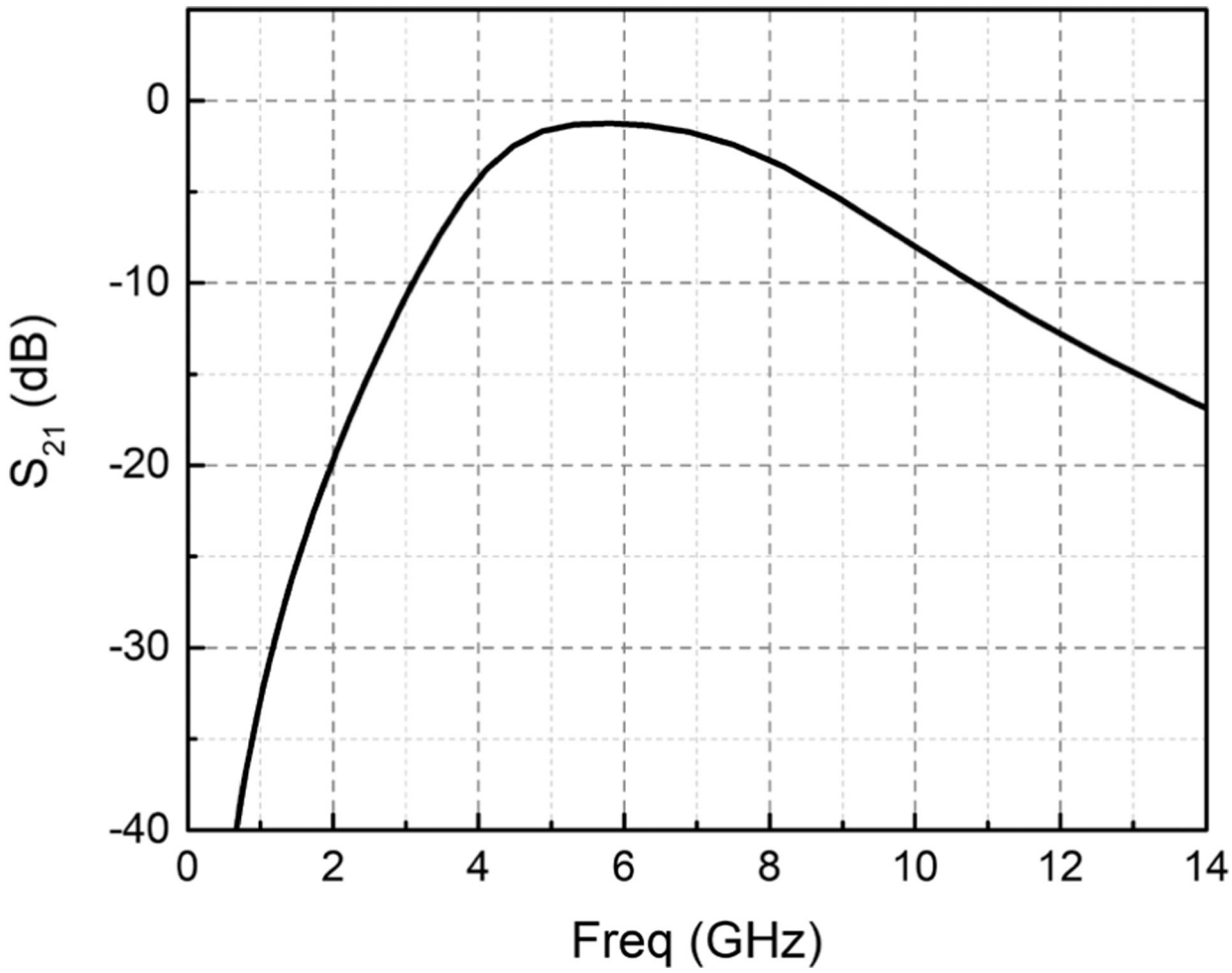

Fig. 13.
S_{21} of the on-chip UWB filter.

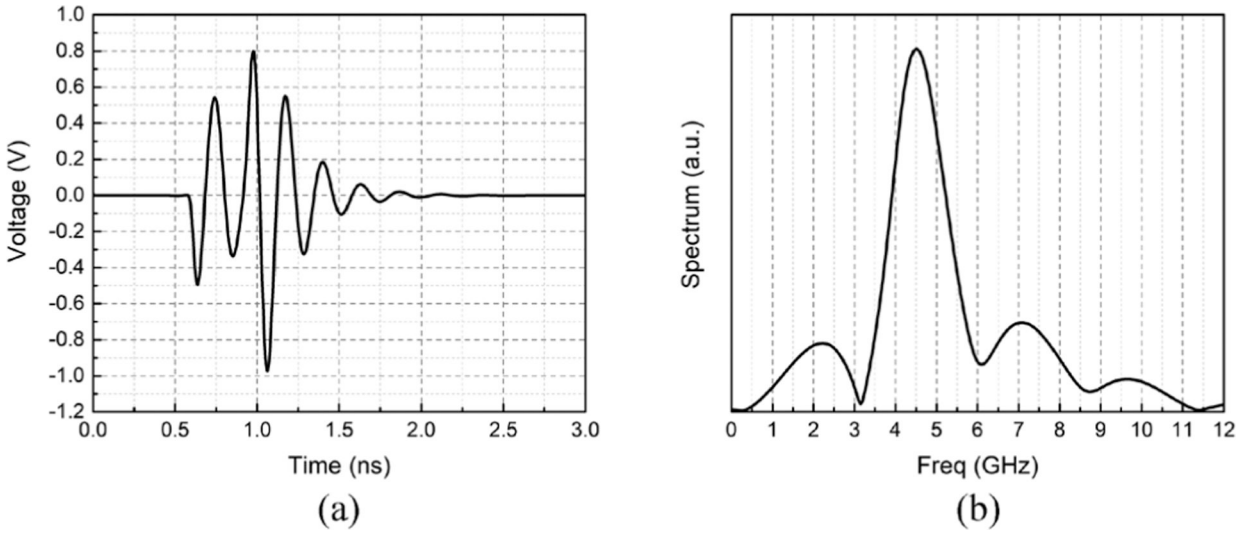

Fig.14.

(a) Transient waveform and (b) frequency spectrum of the UWB impulse.

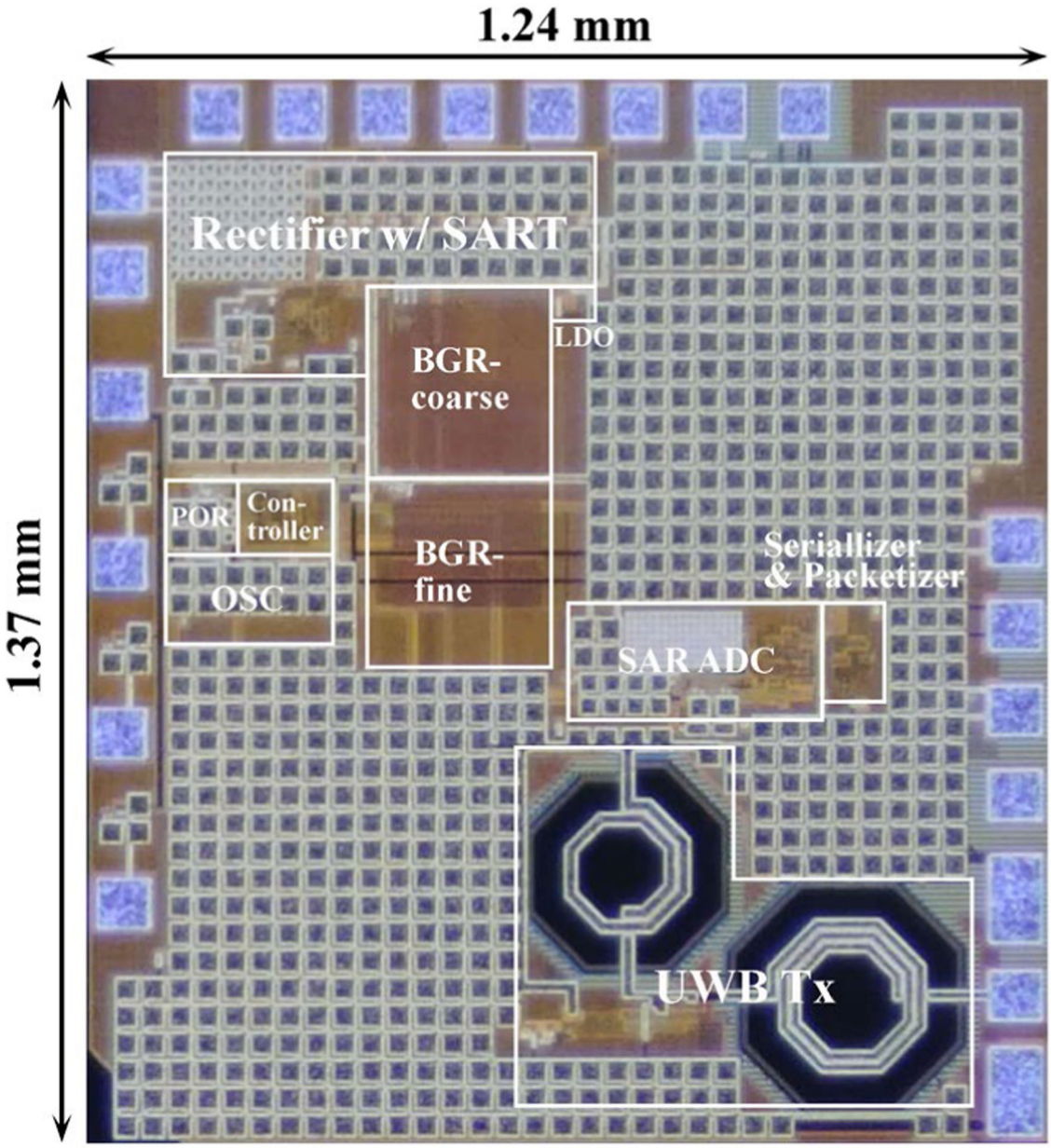

Fig. 15.
Microscopic picture of the power receiver IC.

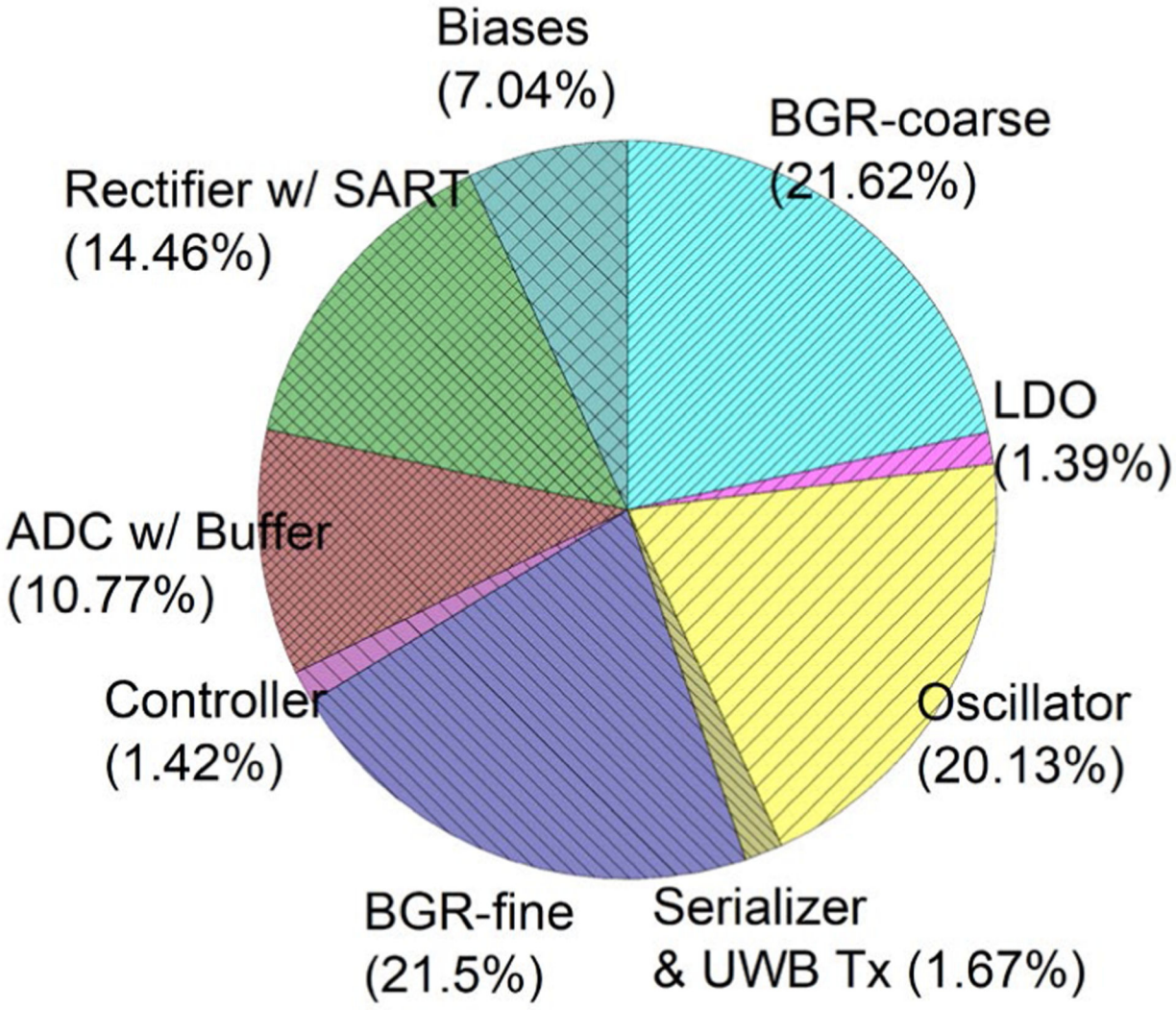

Fig. 16.
Power breakdown.

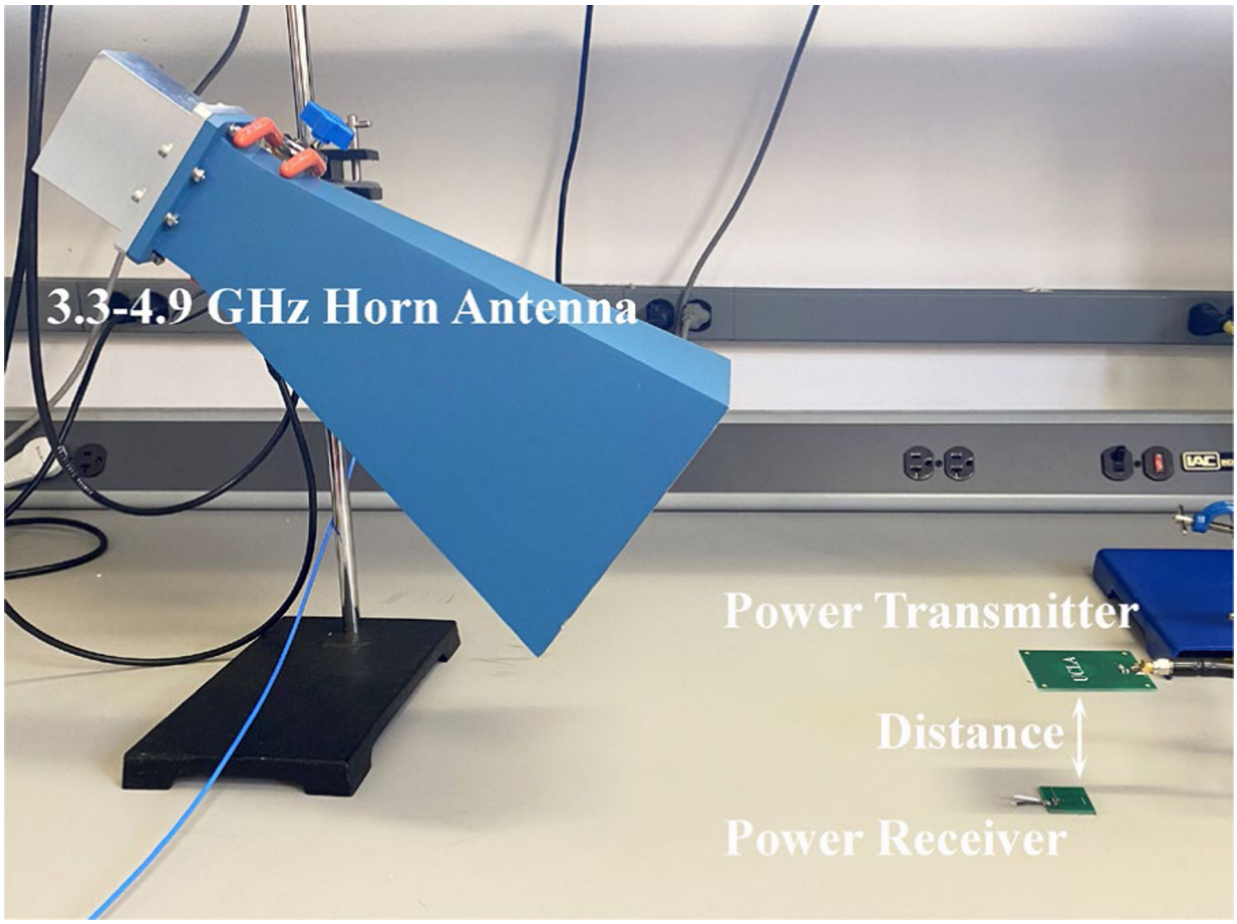

Fig. 17.
Measurement setup.

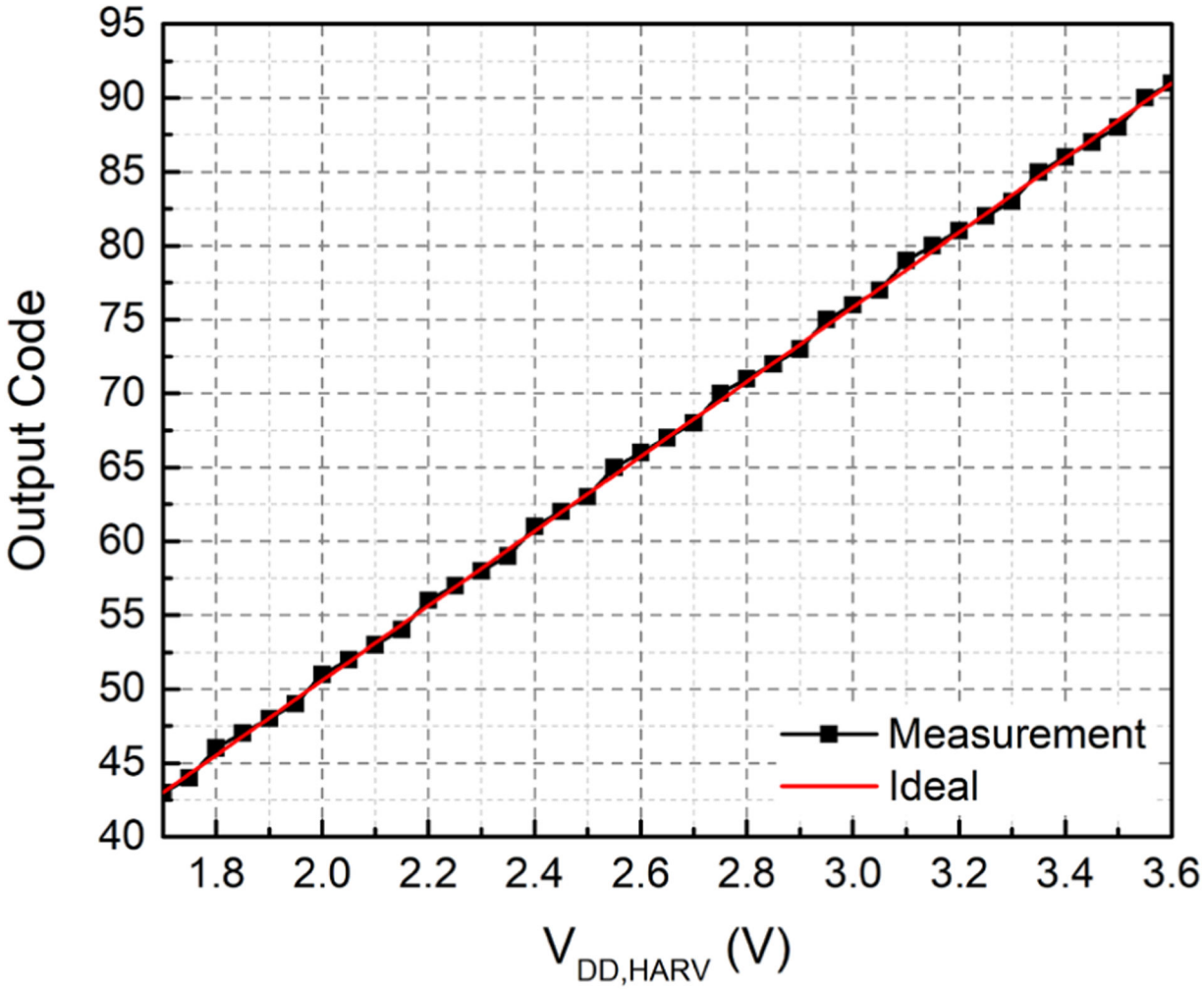

Fig. 18.
Wirelessly measured ADC output codes versus the harvested voltage.

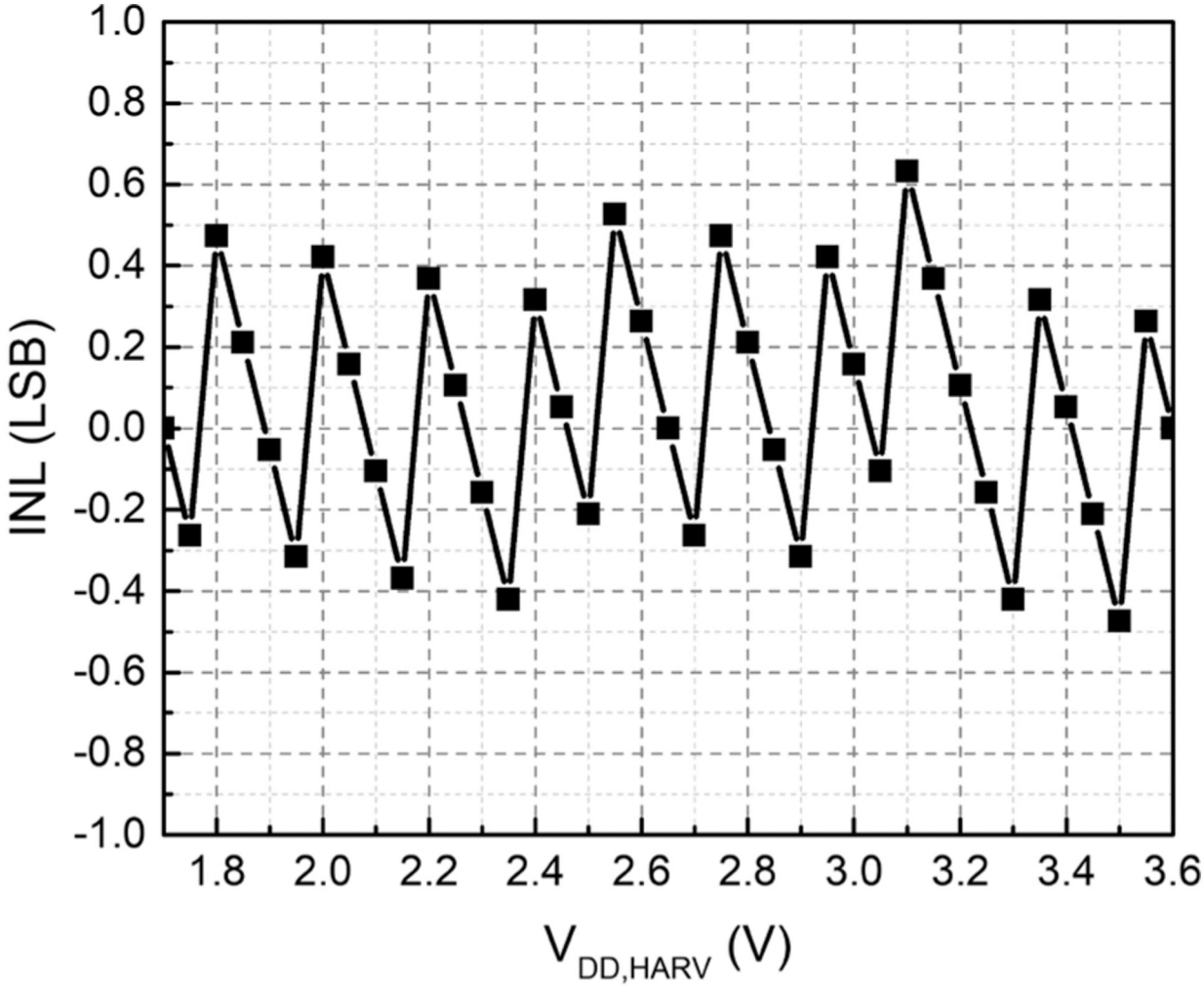

Fig. 19.
INL of the ADC.

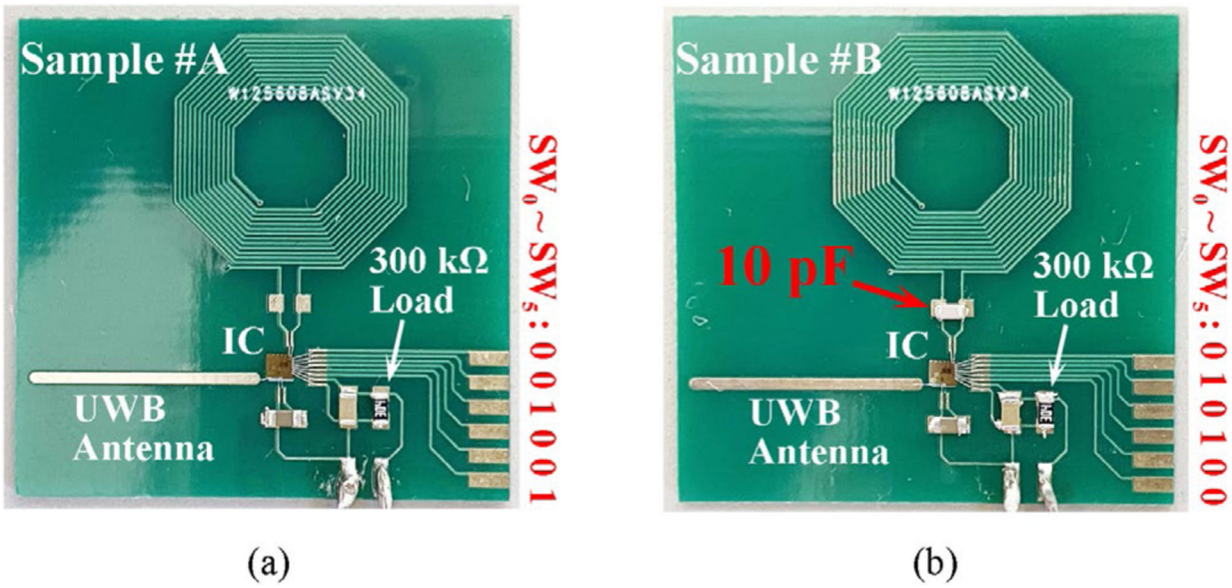

Fig. 20.

Pictures of samples (a) #A and (b) #B with #B incorporating an addition 10-pF parallel capacitor. #A and #B respectively adapt to capacitor bank codes, ‘100100’ and ‘001010’.

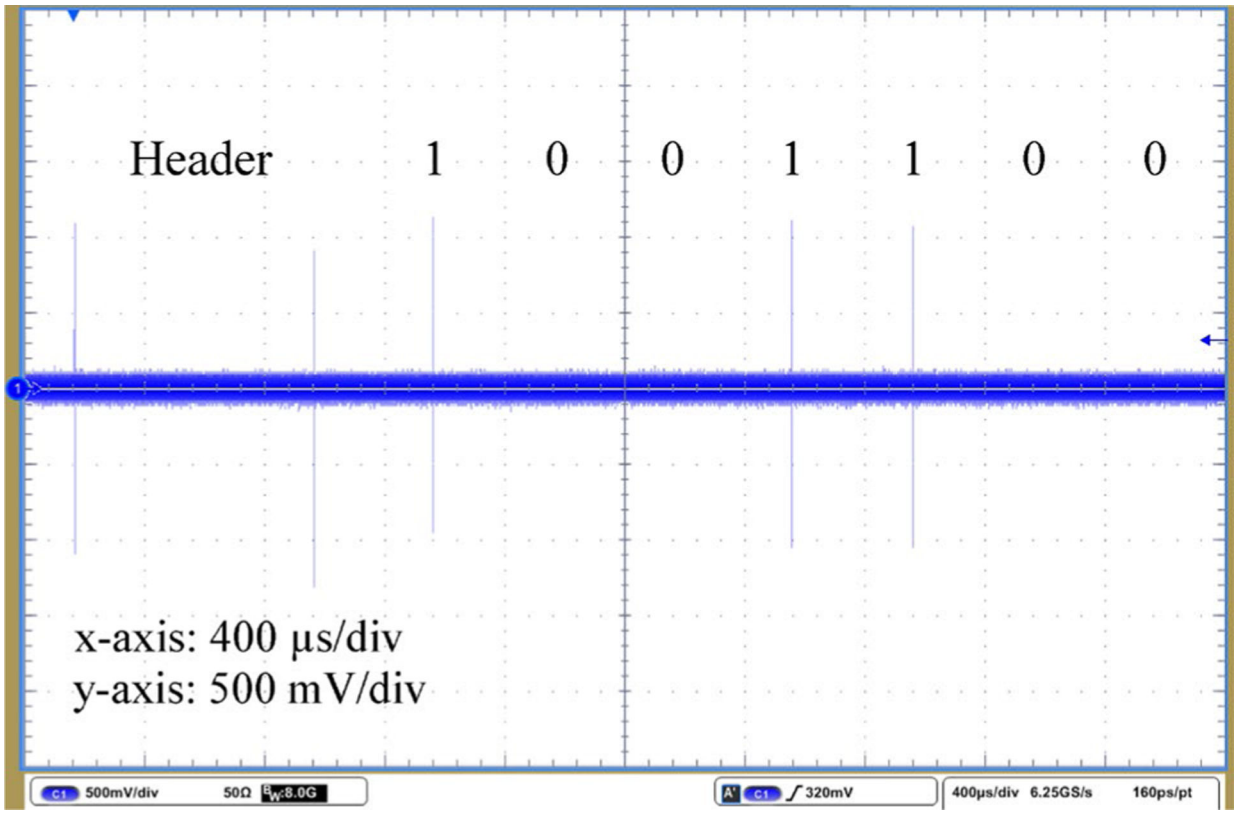

Fig. 21.
Transient waveform of the IR-UWB signal ‘1001100’.

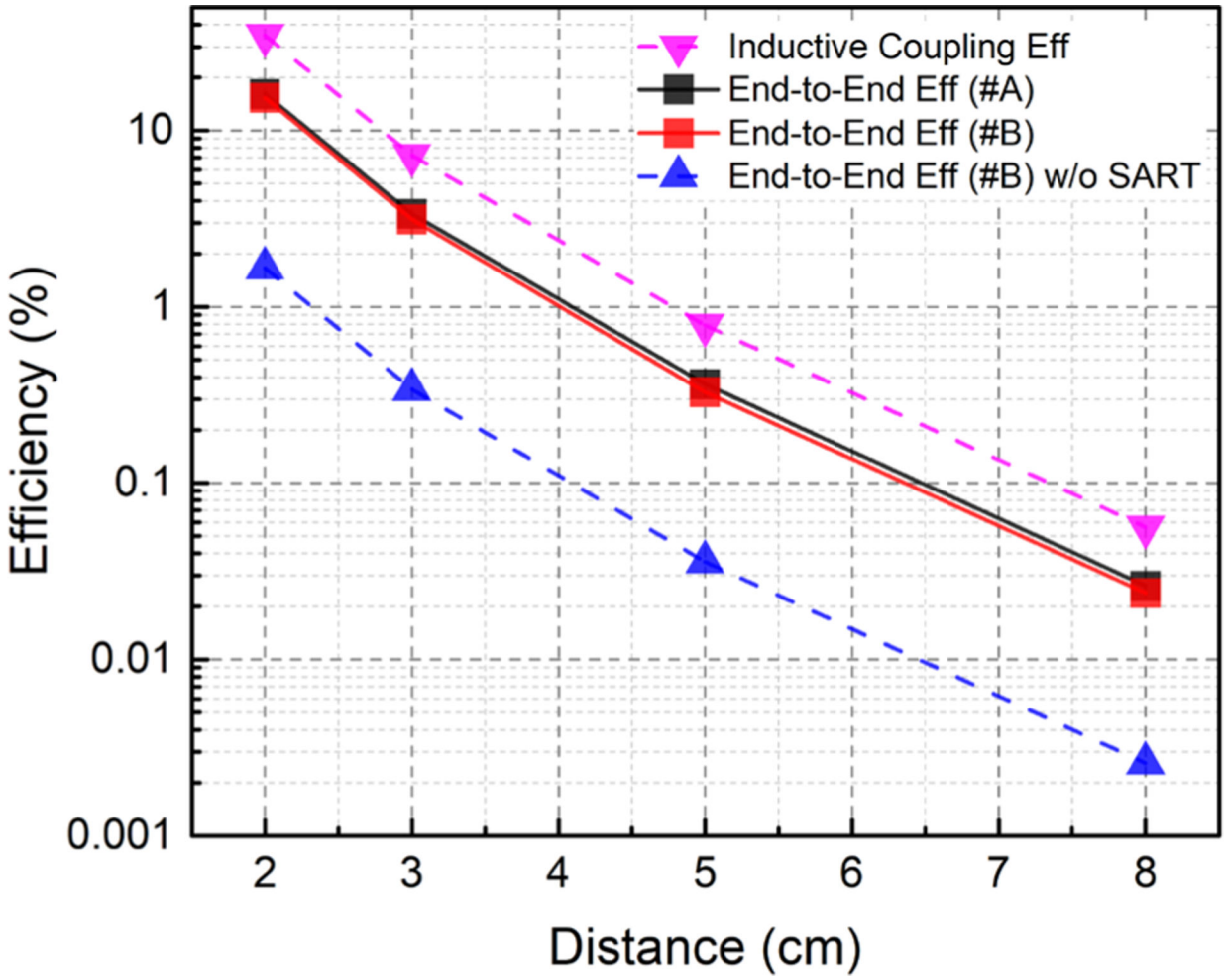

Fig. 22.

End-to-end efficiency at different Tx-Rx distances for samples #A and #B and the speculated inductive coupling and end-to-end efficiencies without SART.

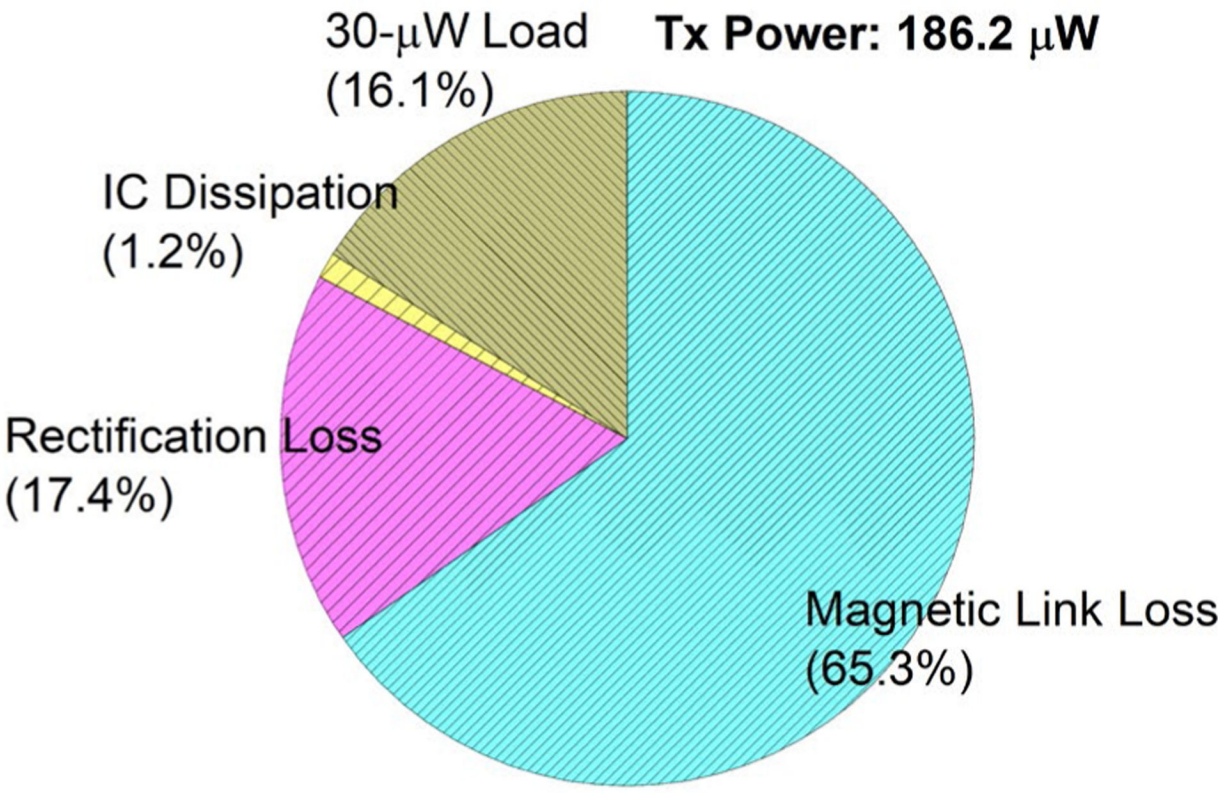

Fig. 23.
Breakdown of the power in the 2-cm power transfer link given the Tx power of 186.2 μW.

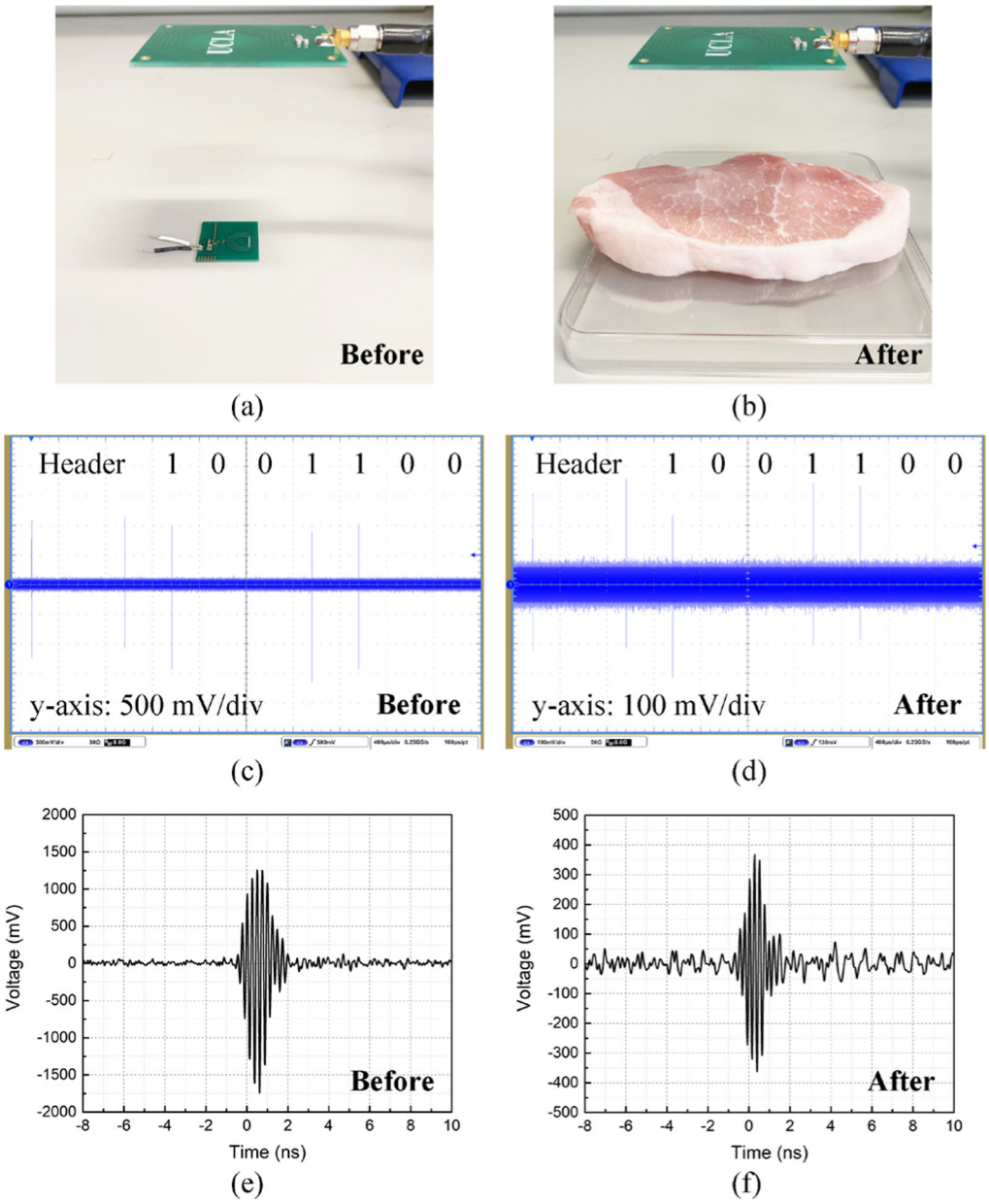

Fig. 24.

In vitro experiment with a piece of pork loin covering the power receiver. (a) Before and (b) after the pork loin covering the device. The corresponding transient waveforms of the IR-UWB signals are shown in (c, e) and (d, f), respectively. The IR-UWB data maintains the same with and without the pork loin.

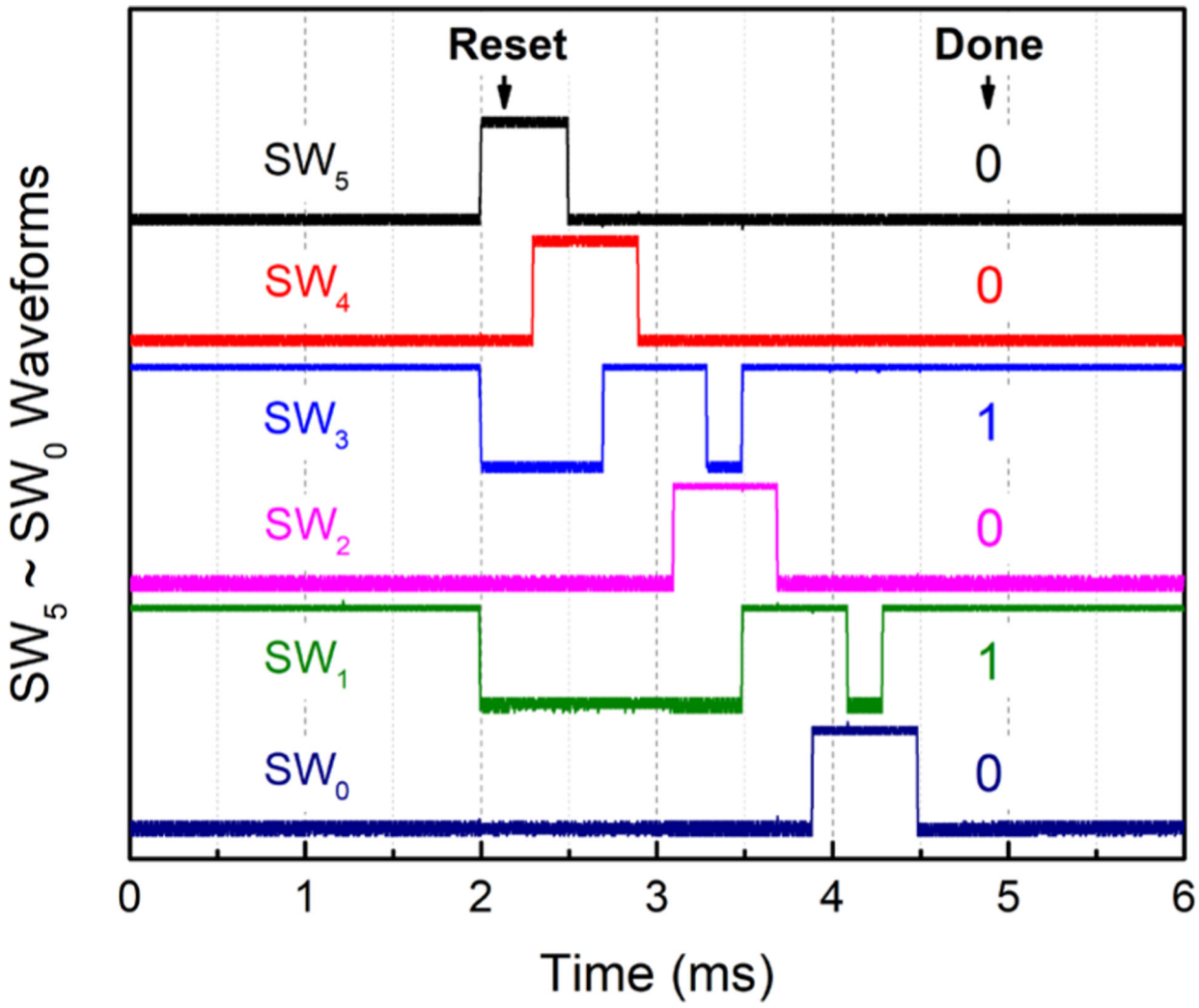

Fig. 25.
Measured resonance compensation logic waveforms during adaptation.

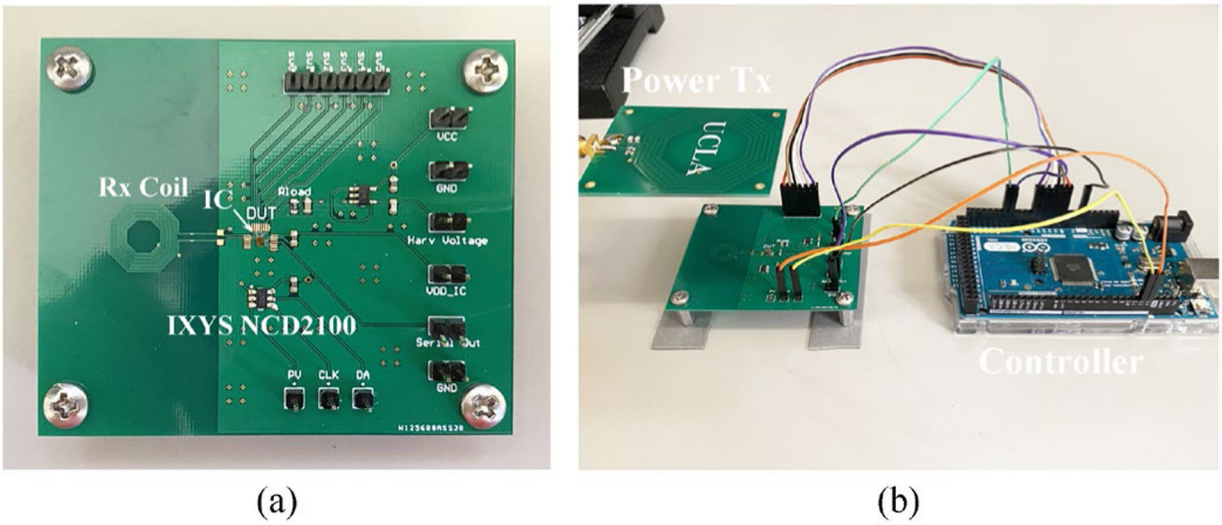

Fig. 26.

Power receiver incorporating a digitally controlled capacitor at the energy-harvesting front-end. (a) Photo of the printed circuit board housing the proposed IC, Rx coil, and the digitally controlled capacitor, NCD2100. (b) Overall setup in which a microcontroller is used to program the capacitor and retrieve data from the IC.

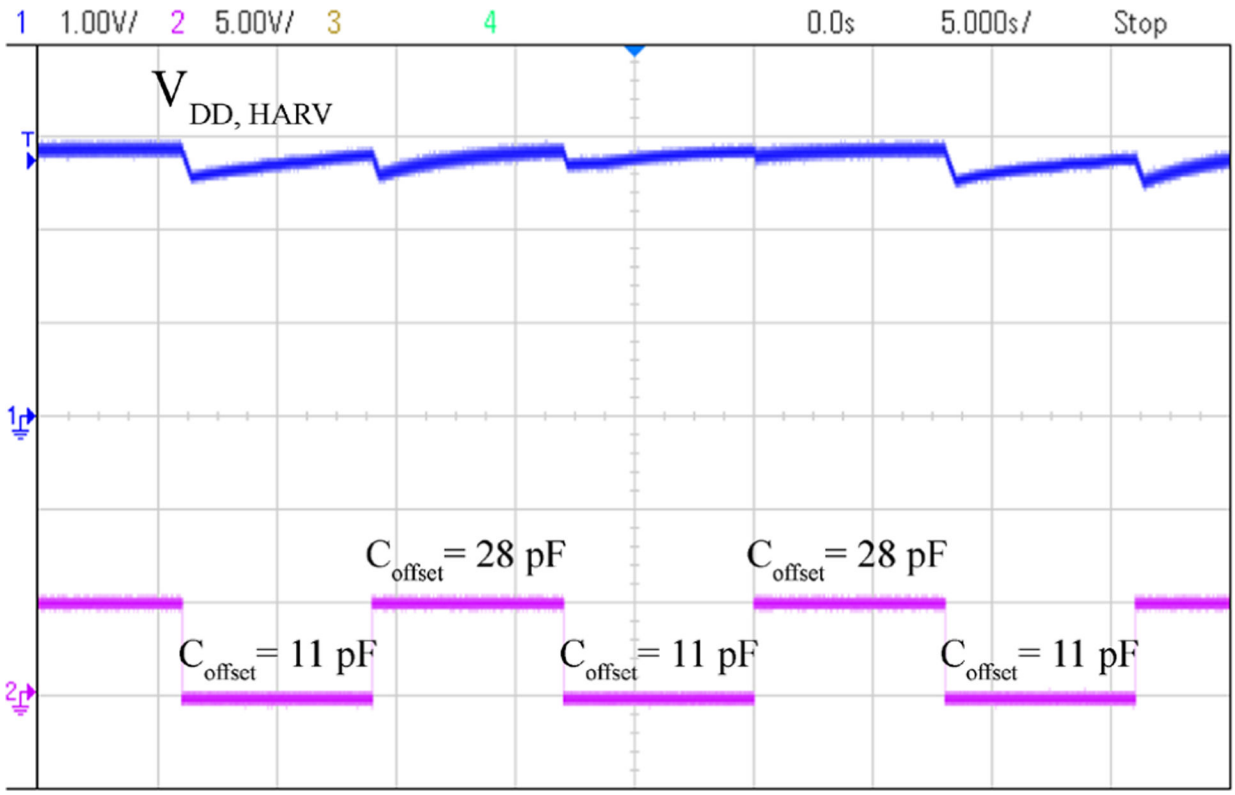

Fig. 27.
Output voltage waveform in response to transient resonance capacitor offsets.

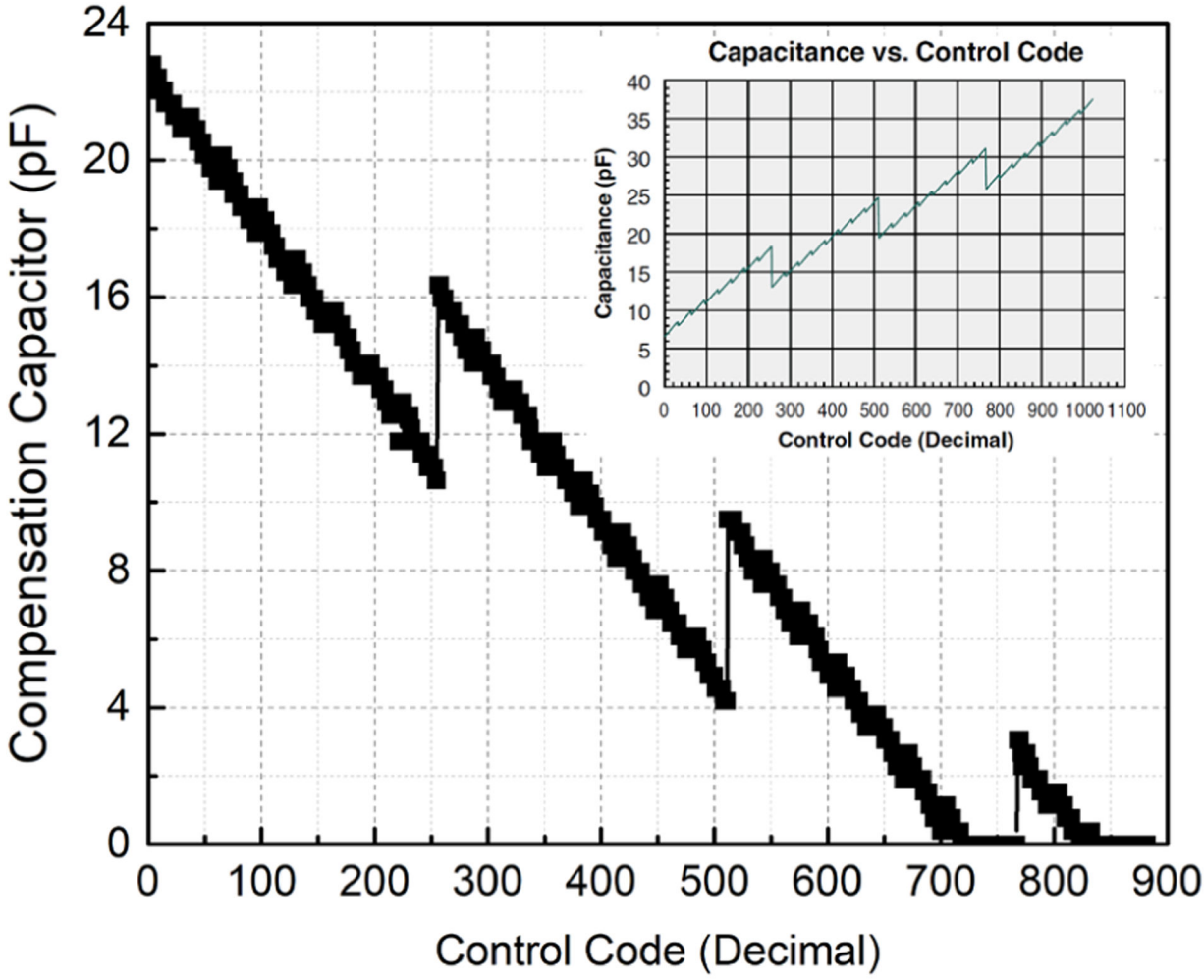

Fig. 28.

Compensation capacitor of the IC adapted to the capacitance of NCD2100. The inset shows the NCD2100 capacitance as a function of the control code according to its datasheet.

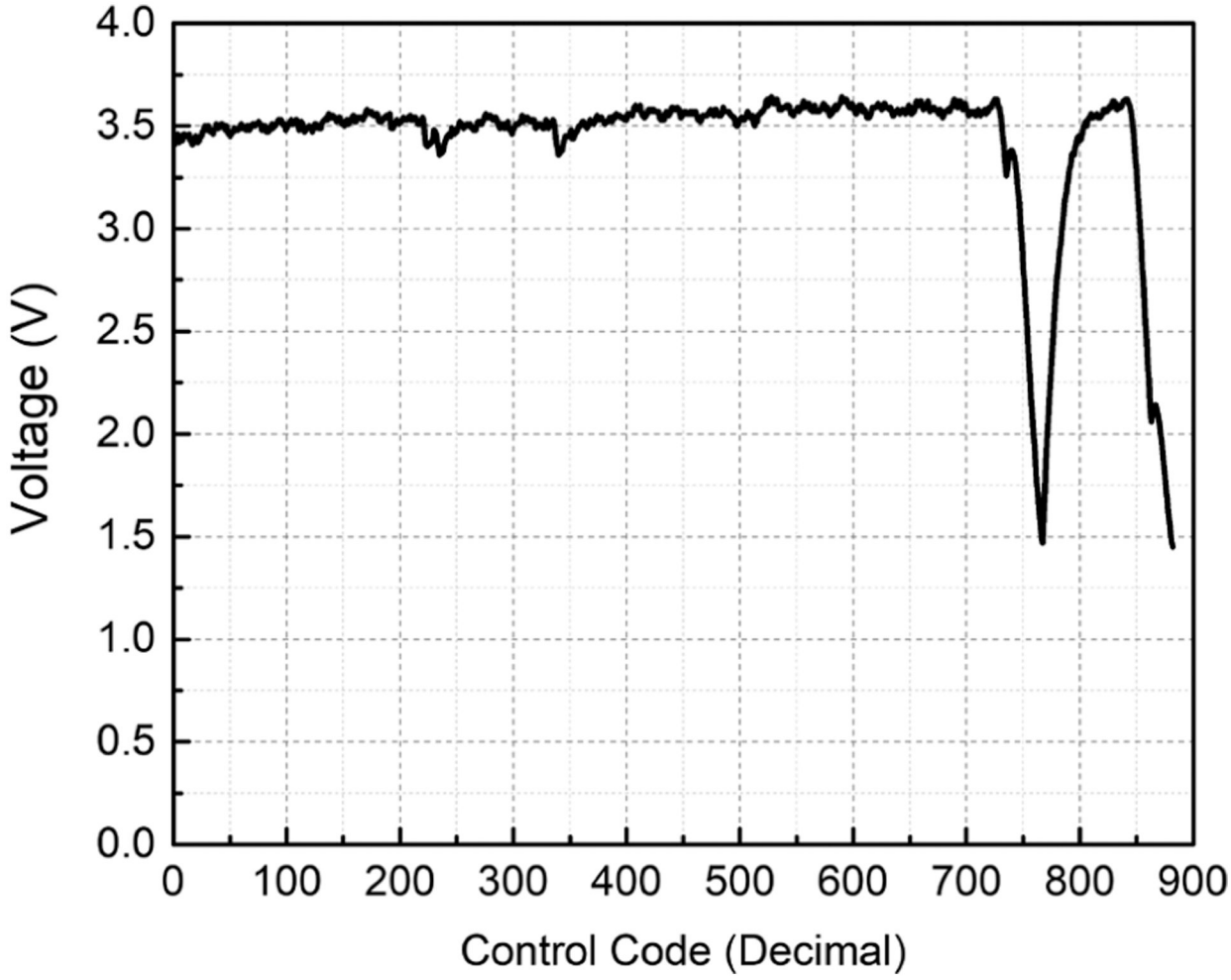

Fig. 29.
Generated output voltage at each control code of NCD2100.

Table I

Parameters of Tx and Rx Coils.

	Number of Turns	Inner Diameter	Outer Diameter	Trace Width	Trace Spacing	Inductance
Tx	Top side 6 + Bottom side 6	25.1 mm	45.3 mm	1.2 mm	0.58 mm	5.76
Rx	Top side 13 + Bottom side 13	5.8 mm	12.1 mm	0.15 mm	0.1 mm	6.36 μH

Table II

Comparison of Resonance Compensation Techniques in Power-Receiving Front-ends.

	This work	2013 ISCAS [28]	2016 TBioCAS [5]	2019 JSSC [29]	2013 ESSCIRC [30]
Power Frequency	13.56 MHz	N/A	13.56 MHz	13.56 MHz	160 MHz
Capacitor Tuning Range	6-bit, unit 380 fF	3-bit, unit 0.51 pF	10-bit, unit 0.5 pF	6-bit, unit 2pF	4-bit, unit 203 fF
Detection Target	Swing amplitude	Rectified current	Swing amplitude	Rectified current	Rectified voltage
Integrated Resonance Compensation Logic	Yes	Yes	Yes	Yes	Yes
Algorithm	Successive approximation	Monotonic sweeping	Monotonic sweeping	Monotonic sweeping	Gradient descent
Needed Clock Cycles	12	8	512	128	< 128
Silicon Verification	Yes	No	Yes	Yes	Yes

Table III

Comparison of State-of-the-art Inductive Power Receivers for Low-power Imds.

	This work	**2015 JSSC [4]**	**2017 JSSC [18]**	**2018 JSSC [3]**	**2016 TBioCAS [5]**
Power Frequency	13.56 MHz	13.56 MHz	144 MHz	13.56 MHz	13.56 MHz
Rectifier Type	Passive rectifier	Active rectifier	Active rectifier	Active rectifier	Active rectifier
Voltage Regulation Method	Back-telemetry and Tx control	Rectifier modulation; Back-telemetry and Tx control	Rectifier modulation	Rectifier modulation; Back-telemetry and Tx control	LDO; Back-telemetry and Tx control
Back-telemetry	UWB	LSK	No	LSK	LSK
Input Sensitivity	2.88 μW	≈ 3 mW	20 μW	≈ 7 mW	357 μW
$\Delta V_{OUT}/V_{OUT}$	0.8%	3.1%	1.87%	2%	N/A
Rx Coil Diameter	12 mm	9 mm	3 mm	20 mm	34 mm
Load	10 μA@ 3 V	16.7 mA @ 3.6 V	30 μA @ 0.8 V	2.5 mA @ 2.2 V	6.6 mA @ 3.3 V
Tx-Rx Distance	2 cm	0.3 cm	1 cm	0.6 cm	2 cm
Power Receiver Efficiency	46.4%	92.6%	50%	N/A	76.2%
End-to-end Efficiency	16.1%	50%	0.4%	31%	13.5%
Normalized End-to-end Efficiency / Load	1	0.0016	0.0312	0.0105	0.0012
IC Process	180 nm CMOS	350 nm CMOS	180 nm CMOS SOI	65 nm CMOS	350 nm CMOS