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Advanced Channel Engineering for Thin Body Transistors

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Advanced Channel Engineering for Thin Body Transistors

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requirements for the degree Doctor of Philosophy

in Electrical Engineering

by

Po-Yen Chien

2016

ABSTRACT OF THE DISSERTATION

Advanced Channel Engineering for Thin Body Transistors

by

Po-Yen Chien

Doctor of Philosophy in Electrical Engineering

University of California, Los Angeles, 2016

Professor Jason C. S. Woo, Chair

As transistor dimension kept scaling down, many challenges arises such as worse electrostatic control and higher variability. In order to address these issues, thin down body thickness is widely accepted and device structures such as FinFET and SOI are employed. Although FinFET has been adopted as main device structure by major foundries like Intel and TSMC in 20nm node and beyond, its analog performances like g_m and f_T are still lagging behind the bulk and SOI and prevent it from applying to SOC applications. In order to maintain the scaling trend, new materials and/or novel device design is needed. Therefore, channel engineering by using laterally composed with different electron affinities along the channel is proposed to show improved analog performance.

Besides thinning down body thickness, there are other methods to realize thin body and one of them is applying channel engineering by employing deeply retrograde doping profile (DRCP)

in bulk device. The doping profile is designed such that it behaves like a thin body device while maintaining bulk device structure. The advantage of DRCP device is that it is relatively cheap and less complicated in terms of manufacturing than those device structures with physically thinner silicon body like FinFET and SOI. It is then instructive to understand whether DRCP device can deliver comparable device performance as FinFET and SOI in 20nm regime. The physics of DRCP device is investigated by TCAD simulation tools and compared with halo device (conventional bulk device) to show the origin of the superior performance. The device performances of bulk device, DRCP, FinFET and SOI are compared to show the capability of DRCP device.

The other approach to make thin body is to utilize 2D materials like transition metal di-chalcogenides (TMDs) as channel material of transistor owning to its ultra-thin body property. 2D materials such as MoS_2 and WSe_2 were extensively exploited recently for FET fabrication due to the good short channel effect control and potential superior carrier transport. Among these 2D materials, WSe_2 is particularly attractive since p-type doping has been achieved making it possible for depletion mode p-FET. However, lack of reliable doping technique makes the doping of the WSe_2 difficult to be accomplished. In this dissertation, WSe_2 doped by controllable W:Ta co-sputtering process and synthesized by post selenization is demonstrated. The material synthesis and characterization of WSe_2 are discussed. The transmission line method (TLM) structure is used to extract the sheet resistance and contact resistance with palladium contact. The MESFET is fabricated and the performance are discussed.

The dissertation by Po-Yen Chien is approved.

Brian C. Regan

Chih–Kong Ken Yang

Jason C.S. Woo, Committee Chair

University of California, Los Angeles

2016

To my parents and my wife

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Po-Yen Chien, Ming Zhang, Shao-Chia Huang, Min-Hung Lee, Hung-Ru Hsu, Yen-Ting Ho, Yung-Ching Chu, Chao-An Jong, Jason Woo, “Reliable doping technique for WSe_2 by W:Ta co-sputtering process” Silicon Nanoelectronics Workshop, IEEE 2016

Ming Zhang, Po-Yen Chien, and Jason C. S. Woo, "Comparative simulation study on MoS_2 FET and CMOS transistor," SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), IEEE 2015

Ming Zhang, Po-Yen Chien, and Jason C. S. Woo, "Comparative simulation study on MoS_2 FET and FinFET," IEEE TENCON 2015 (Invited)

Jason Woo, P.Y. Chien, Frank Yang, S.C. Song, Chidi Chidambaram, Joseph Wang, Geoffrey Yeap, “Improved device variability in scaled MOSFETs with deeply retrograde channel profile” Microelectronics Reliability vol.54, Issue 6-7, pp.1090-1095 2014

Jason Woo, P.Y. Chien, Frank Yang, S.C. Song, Chidi Chidambaram, Joseph Wang, Geoffrey Yeap, “Improved device variability in scaled MOSFETs with deeply retrograde channel profile” ICMAT 2013

Chapter 1

Introduction

1.1 Overview

As transistor dimension kept scaling down, many challenges arises. Device performance degrades due to worse electrostatic control like larger drain-induced-barrier-lowering (DIBL) and subs-threshold swing (SS) [1]. Power consumption increases due to higher device density per area. Lower operation voltage (V_{DD}) can lower both the static and dynamic power efficiently but it is impeded by V_{TH} variation and widely discussed in SRAM [2]. In order to address these issues, thin body concept is widely accepted and device structures such as FinFET and SOI are proposed [3,4]. In 20nm node and beyond, FinFET is adopted as main device structure by major foundries like Intel and TSMC [5,6]. Although FinFET can achieve good digital performance, its analog performances like g_m and f_T are still lagging behind the bulk and SOI and prevent it from applying to SOC applications [7]. In order to maintain the scaling trend, new materials and/or novel device design is needed. Channel region is the core of the transistor and most of the problems mentioned above is closely related to it. Therefore, it is particularly important and attractive to investigate the influence of channel engineering in such thin body device.

Besides FinFET and SOI, there are other methods to realize thin body and one of them is doing channel engineering by employing deeply retrograde doping profile (DRCP) in bulk device. The doping profile is designed such that it behaves like thin body device and improves short channel effect while maintaining bulk device structure [8]. The advantage of DRCP is that it is relatively cheap and less complicated in terms of manufacturing than those device structures

with physically thinner silicon body like FinFET and SOI. It is therefore interesting and helpful to understand the physics of DRCP and whether DRCP can deliver comparable device performance as FinFET and SOI devices in short channel regime (in L_G<30nm).

The other approach to make thin body is to utilize 2D materials such as transition metal di-chalcogenides (TMDs) as channel material of transistor owning to its ultra-thin body property. TMDs like MoS_2 and WSe_2 were exploited recently for FET fabrication due to the good short channel effect from the nature of thin body and potential superior carrier transport [9]. Unlike MoS_2, there are relatively few studies on WSe_2 and also among these 2D materials, WSe_2 is particularly attractive since it can be used as p-FET and makes the CMOS operation feasible [10]. However, lack of reliable doping technique makes the precise doping of the WSe_2 very difficult to achieve [10,11]. It would be helpful and interesting to investigate the doping technique, characteristics and transistor behaviors of doped WSe_2 and such investigation is crucial for the further applications of WSe_2 channel device.

1.2 Motivation and Objective

For 20nm and beyond, FinFET has been adopted as one of the major devices by industries for digital applications due to its superior electrostatic control and the necessity of increasing current per foot print [5,6]. However, the analog performance of FinFET is still facing challenges such as lower transconductance (g_m) and cut-off frequency (f_T) due to worse carrier transport and higher parasitic resistance and capacitance [7]. In order to address this issue, novel device design and/or different material system are needed. In this dissertation, the TCAD simulation is

calibrated to experimental data in order to capture the required physics in short channel regime. The channel engineering regarding to graded channel concept by utilizing different electron affinities along the channel is then proposed to improve analog performance of FinFET such as g_m, output resistance (R_{out}) and intrinsic gain. Such channel design can improve analog performance and make FinFET suitable for SOC applications.

Power consumption is a big issue when scaling down CMOS and lower the operating voltage (V_{DD}) is very helpful to reduce both the static (I_{off}*V_{DD}) and dynamic power (1/2*CV_{DD}*f). However, lower the operation voltage is seriously obstructed by V_{TH} variation [2]. V_{TH} variation is consisting of two components which are inter-die and intra-die. Inter-die is caused by manufacturing fluctuation such as critical dimension (CD) variation and can be compensated by some circuit techniques like adapted back gate bias. However, the later one is caused by some physical mechanisms like random dopant fluctuation (RDF), line edge roughness (LER) and metal grain granularity (MGG) and require other means to improve it [12-15]. Among these mechanisms, RDF is the dominating mechanism and is more than 50% of the total variations at 45nm as shown in Fig. 1.1 [16].

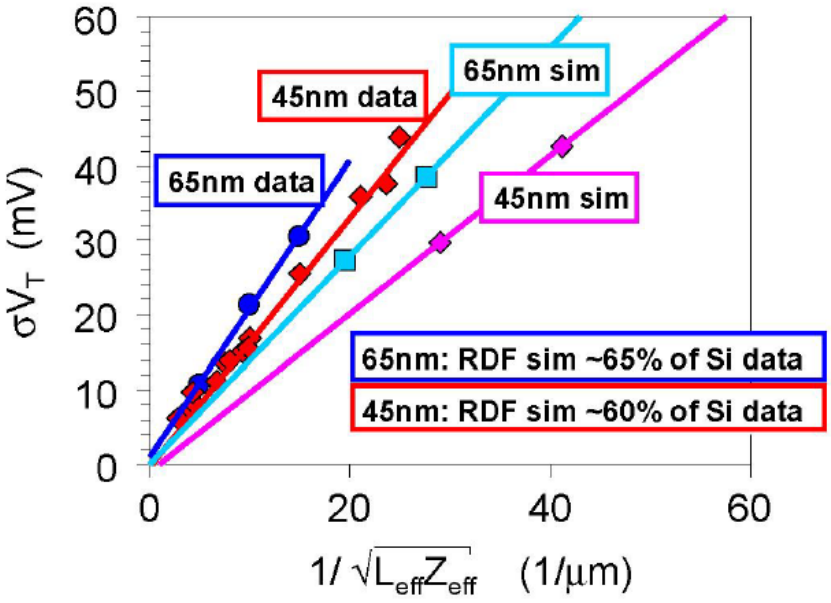


Fig. 1.1 V_{TH} variation for 65nm and 45nm bulk devices.

It is found that advanced device structures such as SOI and FinFET can reduce V_{TH} variability from RDF due to the low channel doping levels, but these solutions are more expensive and complicated in terms of manufacturing compared to planar bulk MOSFETs [3,17]. Recently, with the advance in silicon epitaxial growth, scaled planar MOSFETs with DRCP was proposed to reduce V_{TH} variability due to RDF and attempt to extend planar MOSFET beyond the 20nm-node [15,18,19]. However, prior literatures about DRCP mainly focus on the capability of delivering higher device performances rather than explaining the physics behind [8,20,21]. It is therefore critical to understand whether DRCP can deliver comparable or better device performance compared with SOI and FinFET in 20nm-node and beyond. In this dissertation, the physics of DRCP is investigated by using TCAD simulation tools. The device performance of

DRCP, halo device (typical bulk device), SOI and FinFET are compared and show the limitation of DRCP device.

Recently, transition metal di-chalcogenides (TMDs) like MoS_2 and WSe_2 draws much attentions for FET fabrication due to their good electrostatic control, owning to the nature of thin body and non-zero bandgap, and potential superior transport properties [9,22,23]. Among these 2D materials, WSe_2 is particularly attractive since the p-type doping has been achieved making it possible for depletion mode p-FET [10]. However, the precise doping of WSe_2, especially in the case of high doping concentration, is difficult due to the absence of a controllable doping technique [10,11]. The low hole mobility is also a concern for non-exfoliated (CVD related synthesized) WSe_2 though exfoliated WSe_2 can reach high hole mobility ($140cm^2/Vs$) [24]. In this dissertation, WSe_2 doped by controllable W:Ta co-sputtering process is investigated. Using this technique, high accepter doping concentration and good hole mobility were obtained. Low sheet resistance and contact resistance were also obtained in transmission line method (TLM) structure [25]. WSe_2 channel Transistor was fabricated and analyzed. Although the simulation study shows that 2D materials can't deliver comparable on current than silicon based thin body devices such as FinFET and SOI devices [26], the high doping and good mobility achieved by co-sputtering process can still make WSe_2 a potential channel material in thin film transistor for back-end applications.

1.3 Organization

The dissertation is organized as following chapters:

In chapter 1, the overview and background knowledge of the dissertation is provided. The importance of channel engineering is emphasized.

In chapter 2, The TCAD simulation tools are calibrated to 14nm-node SOI and FinFET experimental data to capture the needed physics in short channel regime. The graded channel concept by using different electron affinities materials in channel region is proposed to improve analog performance at 14nm-node. It shows higher g_m, R_{out} and intrinsic gain by improving the carrier transport and short channel effect in terms of DIBL. Optimization of the graded channel is also discussed.

In chapter 3, the physics of deeply retrograde device is investigated by TCAD simulation and show the reason why it can deliver higher drain current, suppress the short channel effect in terms of lower drain-induced-barrier-lowering (DIBL) and lower V_{TH} variability compared to the halo device at L_G=29nm. It is also found out that it has higher g_m, R_{out} and intrinsic gain due to higher mobility and lower DIBL. The device performance of DRCP device is also compared with bulk, SOI and FinFET to show the capability of DRCP device.

In chapter 4, Preparation and material characterization of WSe_2 by using W:Ta co-sputtering doping technique and post selenization synthesis are discussed. WSe_2 was then used as channel materials for MESFET and TLM fabrication. The TLM measurement results show low sheet resistance and contact resistance when contact with palladium and MESFET's extraction results show high p-type doping concentration and good hole mobility.

In chapter 5, the conclusion of the dissertation is summarized and the future work is proposed.

Chapter 2

Graded channel for improved analog performance

2.1 Introduction

Shrinking down body thickness is a straightforward idea to achieve thin body such as FinFET and SOI and FinFET has been adopted as one of the major devices by industries for digital applications since it can deliver higher current per footprint [5,6]. Although FinFET and SOI shows comparable digital performance [5,27], the comparison of the transfer characteristics and g_m versus bias current for FinFET and SOI shows that FinFET actually has 36% lower I_{on} and 40% lower g_m compared to SOI device if the drain current is normalized to real channel width (2*fin height + channel width) instead of the fin pitch at 20nm channel length as shown in Fig. 2.1. This degradation is believed to be due to both the worse carrier transport from lower channel mobility and larger source/drain parasitic resistance.

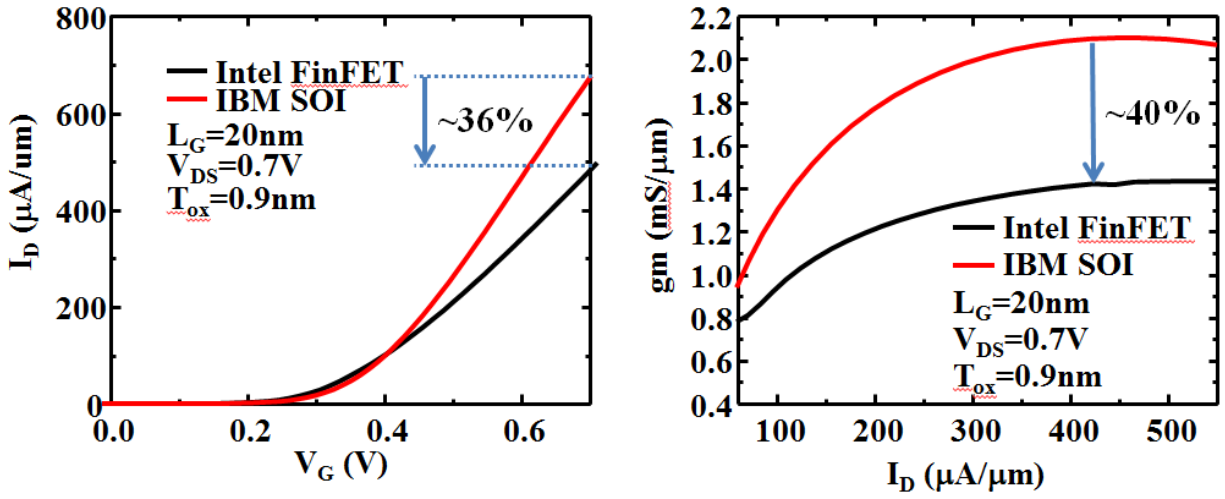


Fig. 2.1 Comparison of drain current and transconductance for FinFET and SOI devices at 20nm channel length

Fig. 2.2 compares the measured results of g_m versus channel length for FinFET and planar bulk MOSFET. The g_m of FinFET is 20% lower than planar bulk MOSFET at V_{GT}=0.2V, V_{DS}=1V and larger g_m degradation is expected with larger gate bias because of parasitic resistance [7].

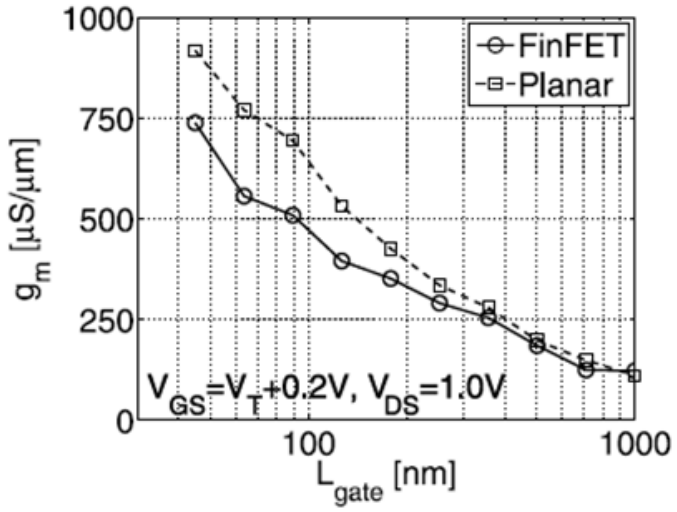


Fig. 2.2 Transconductance versus channel length for FinFET and planar bulk MOSFET

Fig. 2.3 shows the intrinsic gain and f_T versus channel length for bulk device, SOI device and FinFET. [4-7, 28-34] It shows that the intrinsic gain of FinFET is around twice larger than SOI and bulk device despite of lower g_m at 20nm L_G, which implies that FinFET has much higher (more than twice) output resistance than bulk device and SOI device. This suggests that the electrostatic control and short channel effect suppression of FinFET is better than both bulk device and SOI device since R_{out} is related to drain-induced-barrier-lowering (DIBL) and channel length modulation (CLM). On the other hand, the f_T of FinFET's is only 60% of the bulk device and SOI device. (~150GHz versus 250GHz and 300GHz at 20nm regime) This indicates that FinFET not only has lower g_m, but also larger intrinsic parasitic capacitance compared to bulk

device and SOI device [35]. In order to address this issue and make FinFET suitable for SOC applications, novel device design or different material system need to be proposed. In this chapter, TCAD simulation tools are calibrated to 14nm-node SOI and FinFET experimental data to catch the necessary physics in short channel regime. The graded channel concept is then proposed and optimized to improve FinFET's carrier transport and analog/RF performance such as *gm*, output resistance (R_{out}), intrinsic gain, and f_T.

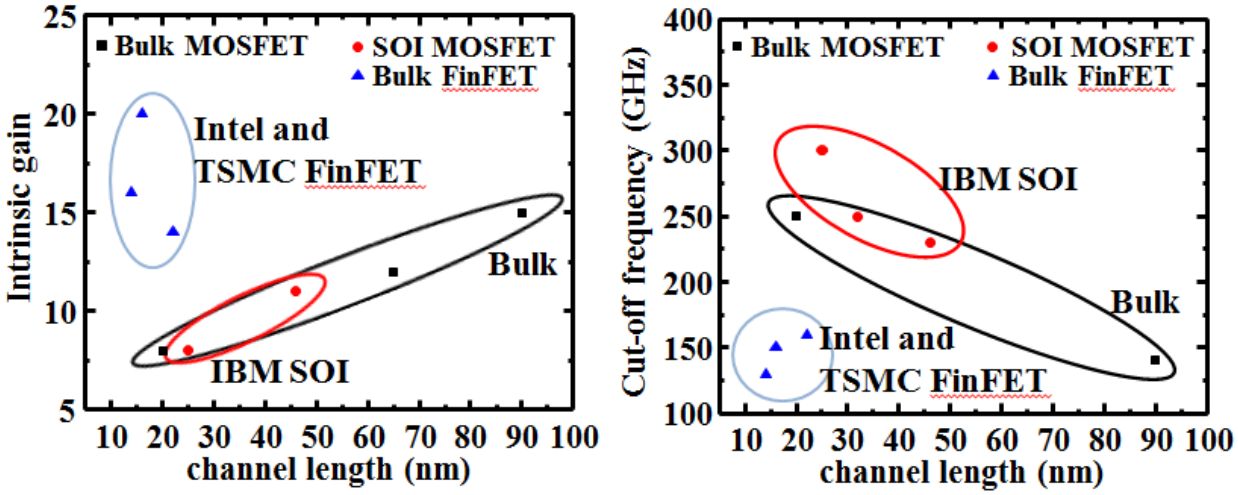


Fig. 2.3 Intrinsic gain and cut-off frequency versus channel length for SOI device, bulk device and FinFET

2.2 Simulation Calibration

The TCAD simulation tool is used to investigate and compare the analog performance of different devices before proposing any solution [36]. However, simulation tools can't provide convincing results without calibration. Therefore, it is calibrated to experimental data before any investigations. It is calibrated to the state-of-the-art experimental data from major foundries such as Intel and IBM and the relevant device parameters are listed in Table 2.1. [5,27] Those device

parameters that are required but not specifically shown in the literature such as source/drain contact resistances, doping gradient and doping levels are chosen from other published literature and ITRS report [3,4,17,28,30,37]. Graded channel concept involves in modifying the carrier velocity and density profiles along the channel and therefore catch the necessary physics for velocity profile is important to demonstrate the graded channel concept. The Monte Carlo simulation is not used here since it needs many input parameters such as mean free paths and collision cross-sections for electron and hole and might lead to wrong simulation results if some of them are not correct [38]. Hydrodynamic model is not adopted either since the energy balance model can't be solved correctly without accurate input parameters for mean free path and interfaces [39,40]. In order to capture the velocity overshoot phenomenon, which may have positive effect in short channel regime, saturation velocity is calibrated with drift-diffusion transport model to provide the reasonable results while maintain computational efficiency [41,42]. Additional mobility model is also included in the mobility model to account for the mobility degradation phenomenon due to the thickness fluctuation in thin silicon body [43]. Quantum confinement of the carriers due to the thin body is considered by using calibrated density gradient model [44]. Fig. 2.4 shows the simulation and experimental structures and Fig. 2.5 is the calibration results for FinFET and SOI devices [5,27]. Not only the transfer characteristics and output characteristics of FinFET fit to experimental data within 5% error but also It also fits to SOI experimental data. It indicates that the simulation results produced by calibrated TCAD simulation tools can reproduce convincing data both for FinFET and SOI device with single set of models, which means the calibrated simulation tool is robust and can apply to different devices in short channel length (L_G=20nm). It is also accurate enough (<5%

difference) for us to further investigate analog performance even for second order analog performances like linearity.

Device parameters	FinFET	Device parameters	SOI
Channel length (nm)	20	Channel length (nm)	20
Fin height (nm)	42	Body thickness (nm)	5
Fin width (nm)	8	BOX thickness (nm)	20
Fin pitch (nm)	42	Gate oxide thickness (nm)	0.67
Gate oxide thickness (nm)	0.9	Spacer length (nm)	5

Table 2.1 Device parameters from literatures for calibration

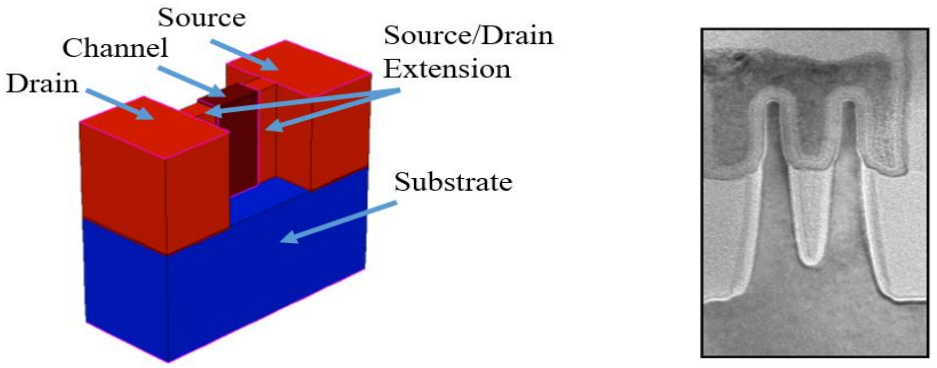
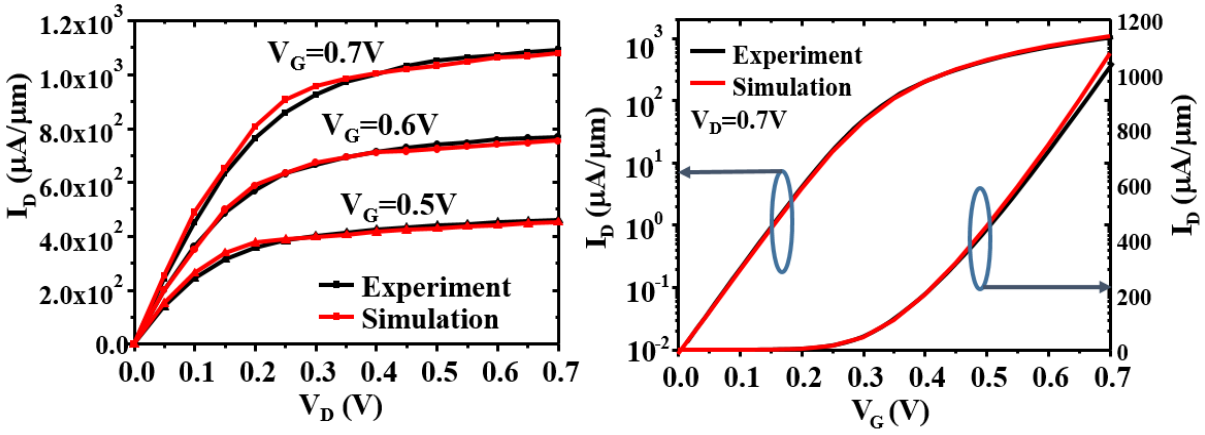
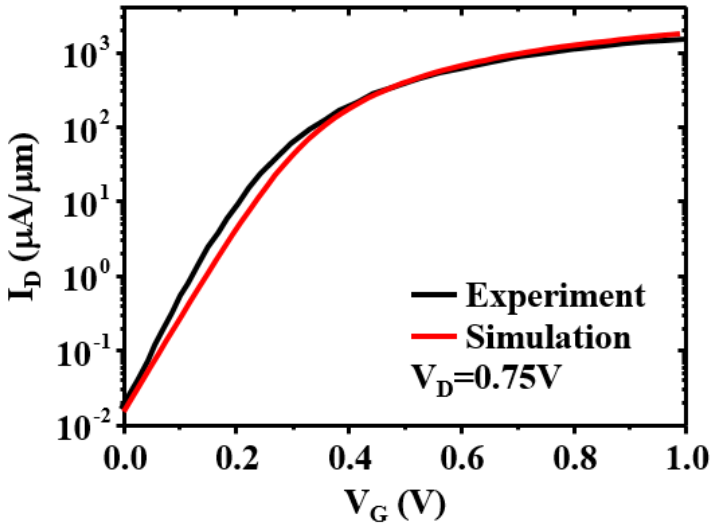


Fig. 2.4 FinFET simulation and experimental structures for calibration



(a) I_D-V_G and I_D-V_D calibration results for FinFET



(b) I_D-V_G calibration results for SOI device

Fig. 2.5 Calibration of simulation results to experimental data for (a) FinFET and (b) SOI device

2.3 Device structure and concept

2.3.1 Simulation setup and device structure

In digital applications, FinFET with tall fin height is widely adopted as one of the main devices for 20nm and beyond. In order to mimic such FinFET structure (high aspect ratio) while maintaining computational efficiency, double gate structure is chosen for simulation. Device simulation employed the calibrated TCAD simulation tools mentioned in previous section. Device parameters are based on ITRS report and experimental data [37,5]. Fig. 2.6 shows the proposed simulated structure which is consist of two materials with different electron affinities along the channel. Silicon with smaller electron affinity (4.05eV) is close to source side and tensile strained silicon with larger electron affinity (4.22eV) is close to drain side. This results in a large threshold voltage close to source side and a small threshold voltage close to drain side.

When this device is turned on at saturation regime, it will induce more uniform inversion charge distribution along the channel than pure silicon device (homojunction device). Therefore, it will cause the redistribution of lateral electric field, which enhance electric field at the source side and reduce electric field at drain side compared to homojunction device. The reduced electric field at drain side can suppress channel length modulation and therefore increase the R_{out}. The increased electric field at source side can enhance the transport of injected carriers, which results in higher g_m. [45-47] The improvement of both g_m and R_{out} then leads to improved intrinsic gain as will indicated in the following section.

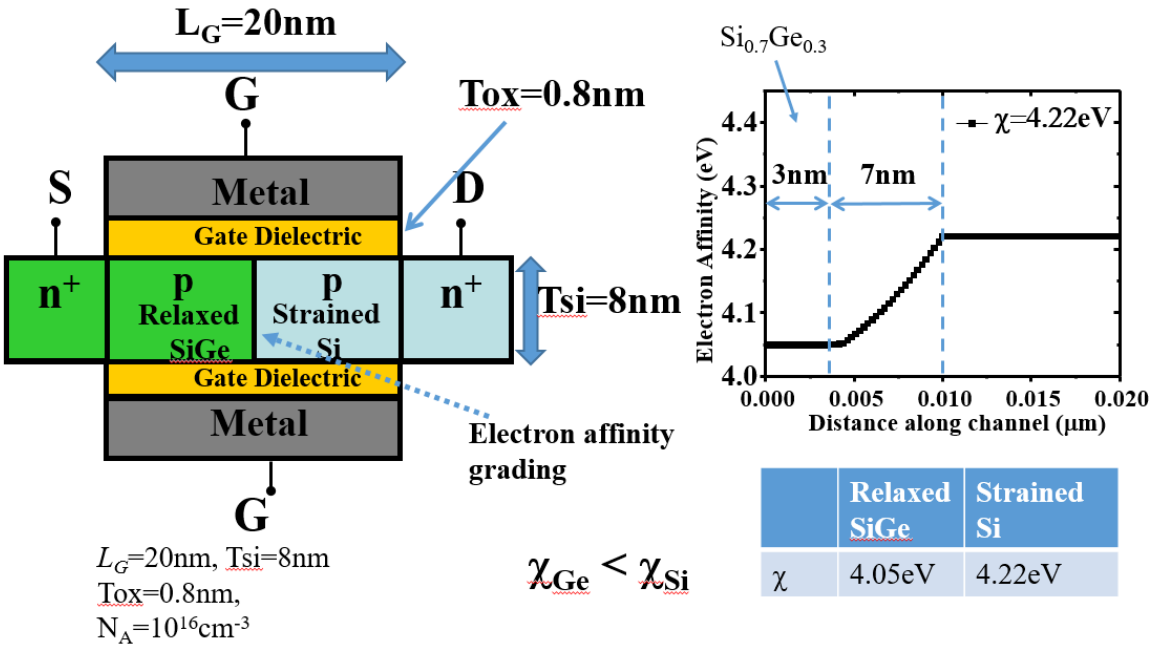


Fig. 2.6 Simulated structure of double gate graded channel device and the electron affinity changes along the channel

2.3.2 Device theory

The idea of graded channel is to make the electron density and electron velocity distribution along the channel more uniform than homojunction device. Fig. 2.7 shows the comparison of

graded channel device and the homojunction device for these distributions. It shows that the graded channel device has more uniform electron density and electron velocity distributions than homojunction device. This uniform distribution makes the lateral electric field to redistribute, which results in increases of the electric field at source side and decreases of the electric field at drain side as shown in Fig. 2.8. Higher electric field at the source side will induce higher carrier velocity at the beginning of the channel, which translate to higher injection velocity. Lower electric field at the drain side will reduce the channel length modulation (CLM) and results in better output resistance [45-47].

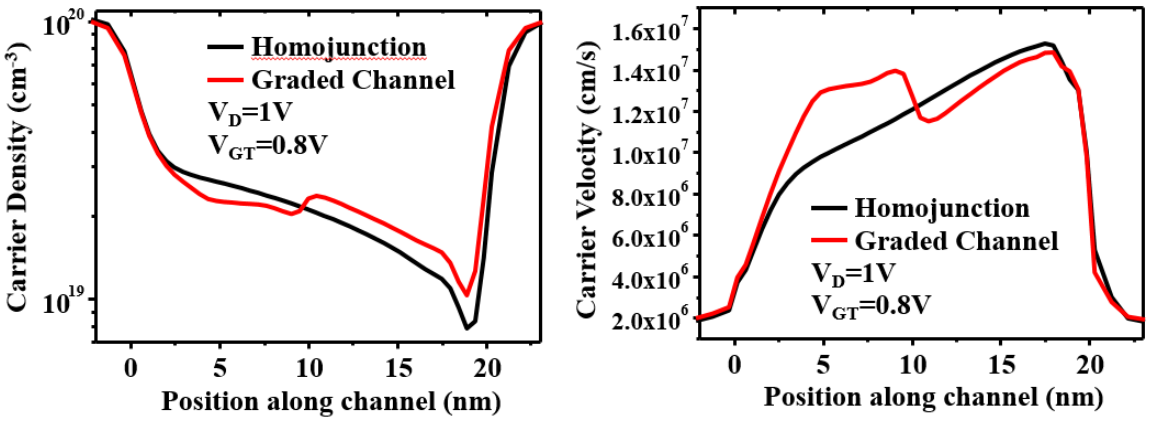


Fig. 2.7 Carrier density and velocity distribution along the channel for graded channel device and homo junction device

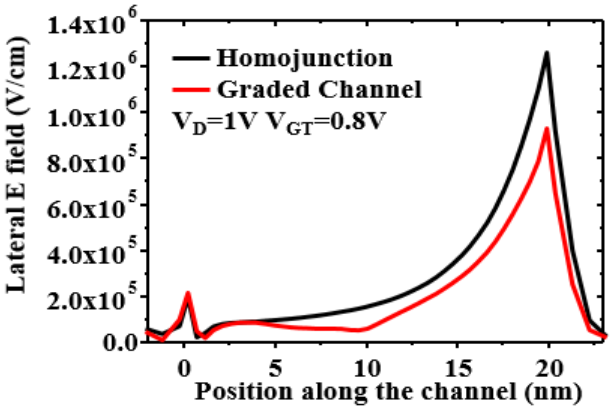


Fig. 2.8 Lateral electric field distribution along the channel for graded channel device and homo junction device

It is well known that, as channel decreases, the potential in drain side will pull down the barrier and induce diffusion current and lower threshold voltage. This phenomenon is called DIBL. In graded channel device, the smaller affinity close to source side results in higher threshold voltage. This difference of the electron affinity and threshold voltage will screen the penetration of electric field from the drain side and reduce the diffusion current and lower drain-induced-barrier-lowering (DIBL). Lower DIBL will then increase output resistance. Fig. 2.9 shows the conduction band distribution along the channel in subthreshold regime for graded channel and homojunction device. It shows that the graded channel device has smaller barrier height changes than homojunction device [48].

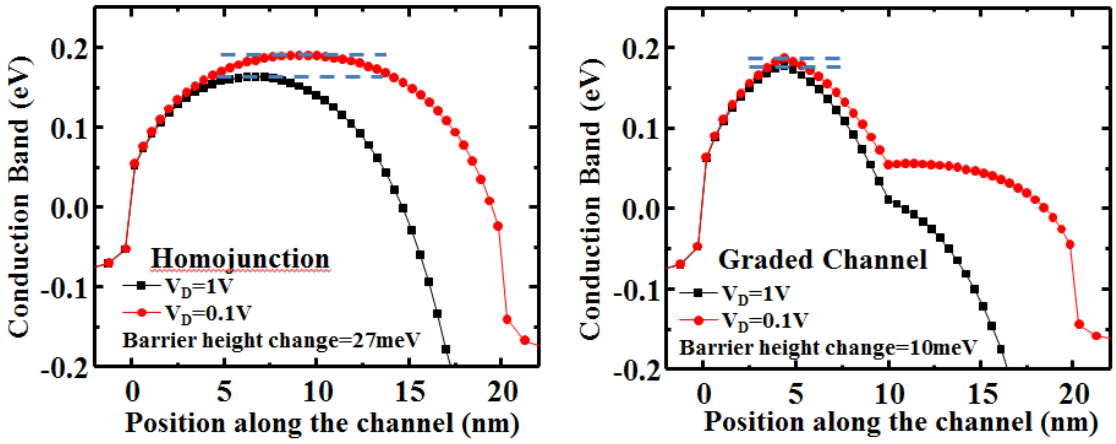


Fig. 2.9 Conduction band profiles along the channel for graded channel device and homo junction device

2.4 Simulation studies

2.4.1 Enhanced carrier transport

Fig. 2.10 shows the transfer characteristics and output characteristics for graded channel device and homojunction device. The graded channel device shows higher drain current device

although graded channel device has slightly higher substhreshold swing (~2mV/dec difference). Fig. 2.11 shows the transconductance of graded channel device and homojunction device versus bias current. The transconductance of graded channel device is higher than homojunction by 5%. This is due to the redistribution of the carriers along the channel as mentioned in Fig. 2.7, which results in enhanced electric field and increased injection velocity in the source side as in Fig. 2.8. Fig. 2.11 also shows that graded channel device has larger g_m/I_{on} than homojunction device, which makes graded channel device a more efficient device (g_m/I_{on} is a measure of the speed-to-power-dissipation [49]). The small amount of improvement on transconductance is due to the large parasitic resistance of FinFET at source/drain region compared to bulk device as shown in Fig. 2.12 [7,72]. In order to gain more improvement on transconductance, source/drain resistance need to be lowered and the co-optimization of the graded channel along with source/drain region is needed.

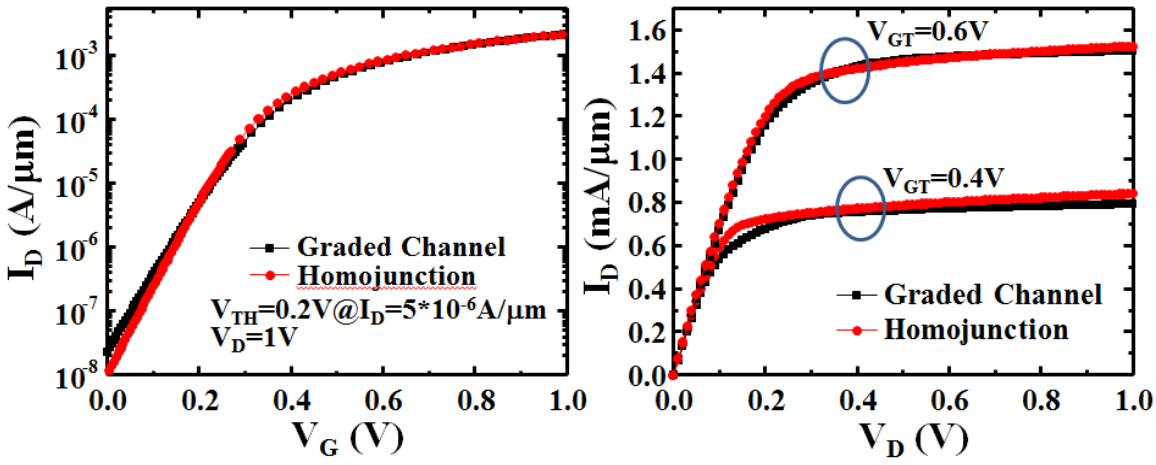


Fig. 2.10 Transfer characteristics and output characteristics for graded channel device and homojunction device

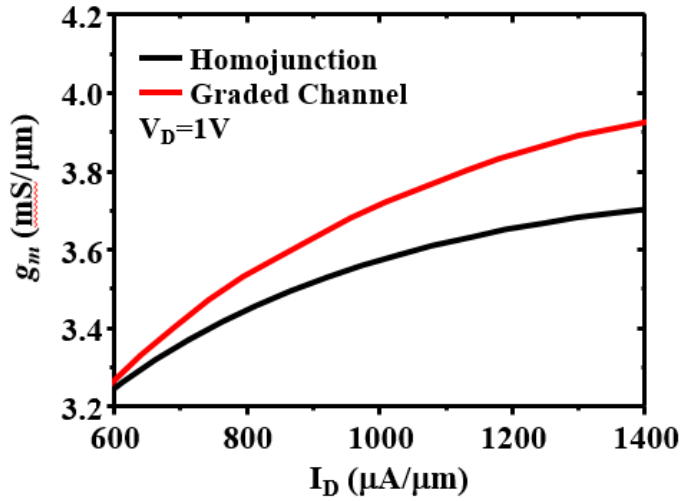


Fig. 2.11 Transconductance of graded channel device and homojunction device versus drain current

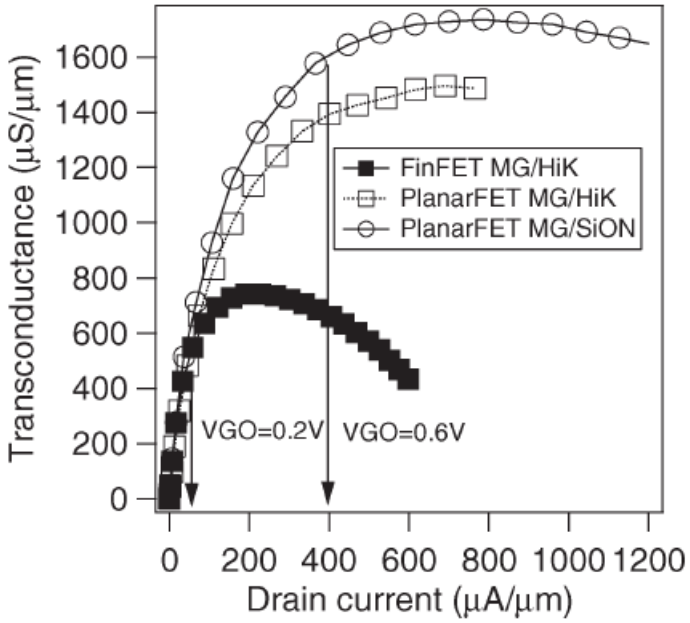


Fig. 2.12 The transconductance vs. drain current for bulk device and FinFET

2.4.2 Improved output resistance

The ouput resistance of MOSFET is affected by CLM and DIBL. And the graded channel device can improves DIBL by screening the electric field from the drain side as mentioned in Fig. 2.9. Fig. 2.13 shows the output resistance of graded channel device and homojunction device versus different bias current. It shows that the graded channel device can have substantially better output resistance than homojunction device. (~65%) This is because the graded channel device can suppress the DIBL and improves the output resistance. Fig. 2.14 shows the intrinsic gain comparisons of graded channel device and homojunction device. It shows that the graded channel device has much higher intrinsic gain (75% higher) than homojunction device. This is due to the improvement from both transconductance and output resistance.

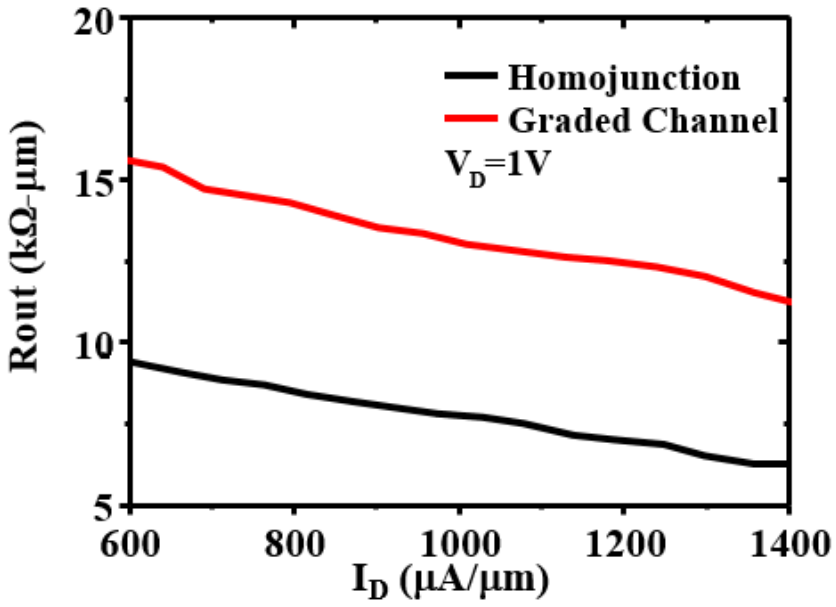


Fig. 2.13 Output resistance of graded channel and homojunction devices

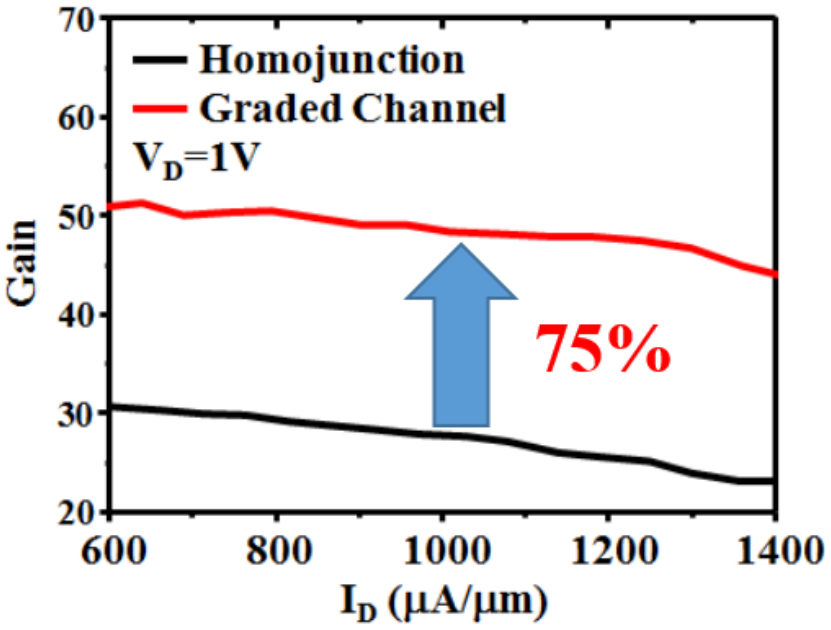


Fig. 2.14 Intrinsic gain of graded channel and homojunction devices

2.4.3 Other device performance

Other second order analog device performances like the cut-off frequency and linearity are also examined for graded channel device and homojunction device. Fig. 2.15 shows that both of the performances for graded channel device are similar to homojunction device. This is due to the g_m improvement is small (~5%) and the cut-off frequency and linearity are directly related to g_m. To improve f_T and linearity, g_m improvement is needed and therefore lower source/drain resistance is required as described in section 2.4.1. In order to further improve these analog performances, co-optimization of graded channel and lower parasitic resistance is needed.

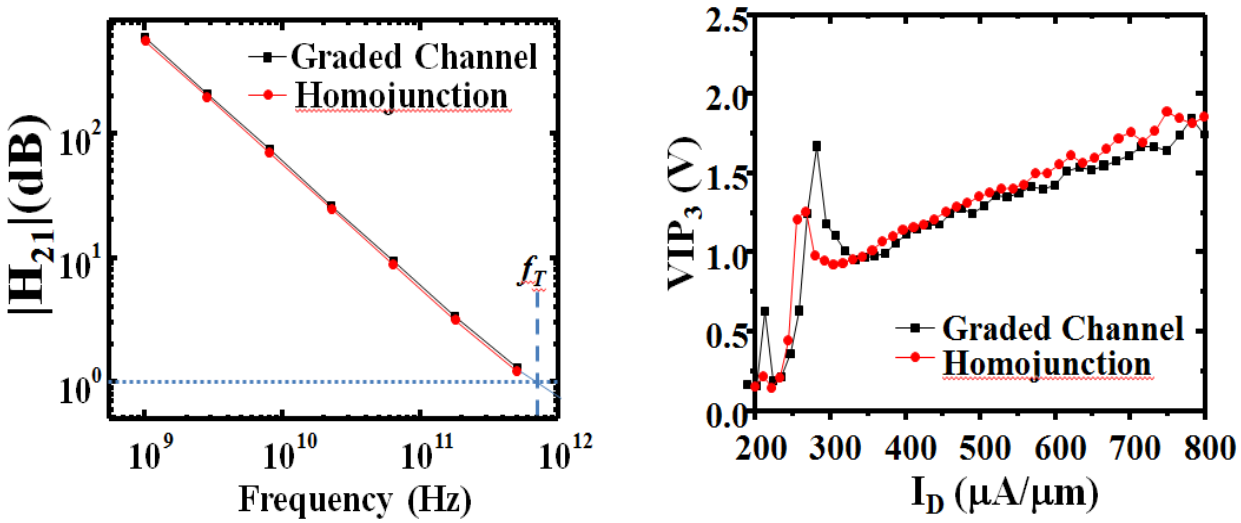


Fig. 2.15 Cut-off frequency and linearity of graded channel and homojunction devices

2.4.4 Graded channel device with various electron affinities

Since graded channel device can improves device performance by chaning the electron affinity, one might think that increases the electron affinity difference will provide more improvement. Fig. 2.16 shows the transconductance for graded channel device with different electron affinities. The results show that the the transconductance increases with higher electron affinity difference. However, the saturation of transconductance is observed. This is due to the reason that the inversion charges close to source side is decreasing when the electron affinity difference is increasing. Therefore, the improvement of transconductance saturates.

Fig. 2.17 shows the output resistance of graded channel device with various electron affinities. It can be seen that, at first, the improvement of output resistance increases with electron affinity difference increases, but the improvement starts to decrasing after the electron

affinities reaches an optimal value. When the electron affinity difference increases, the carriers become more uniform. However, it also affects the pinch-off region, which in turn affects output resistance. Therefore, there is an optimal point for output resistance improvement. This optimal point may varies for different channel length.

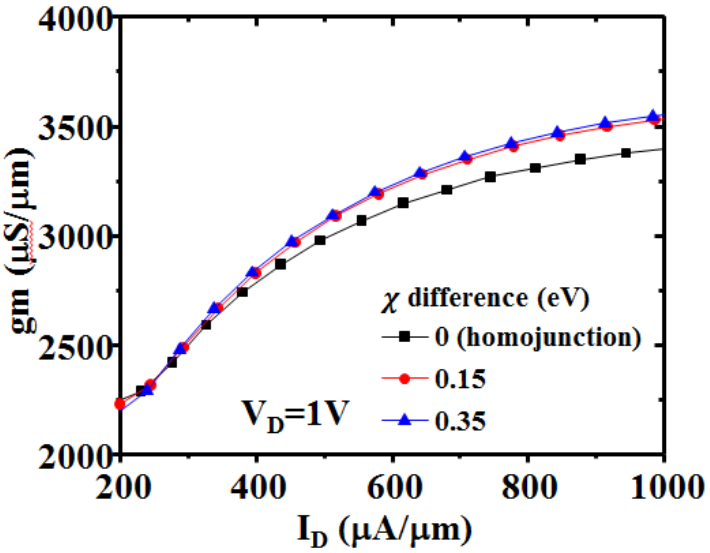


Fig. 2.16 Transconductance of graded channel device with various electron affinities

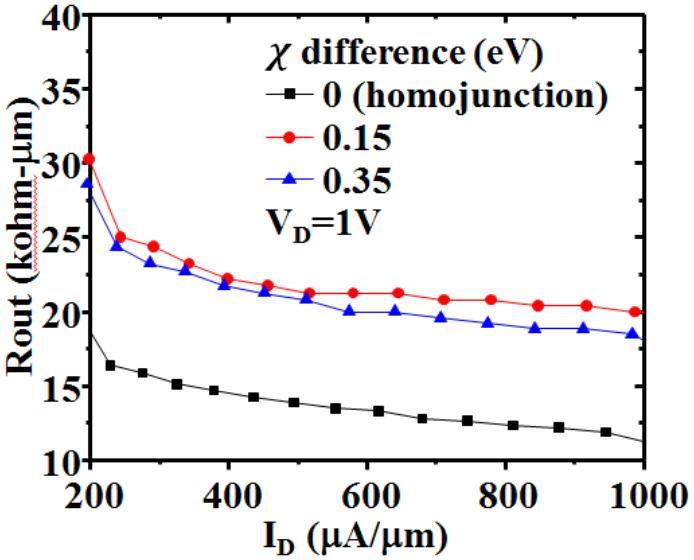


Fig. 2.17 Output resistance of graded channel device with various electron affinities

2.4.5 Graded channel device with different junction locations

The other design space of graded channel device is where does the junction locate. Fig. 2.18 shows the transconductance for graded channel device with different junction positions. (7nm means the junction is 7nm away from source, 10nm refers to the middle of the channel and 15nm refers to the junction is closer to drain) It shows that there is an optimum point for transconductance improvement. As the junction is closer to the source, the improvement of enhanced electric field and carrier velocity is significant. However, the junction itself purturbs the build-in electric field between source and channel and results in worse subthreshold wing and the transcondictance degradation. As the junction moves toward drain, the electric field enhancement is far away from source and contributes less to the injection carriers. Therefore, there is an optimal point regarding to the junction location for the improvement of transconductance [48].

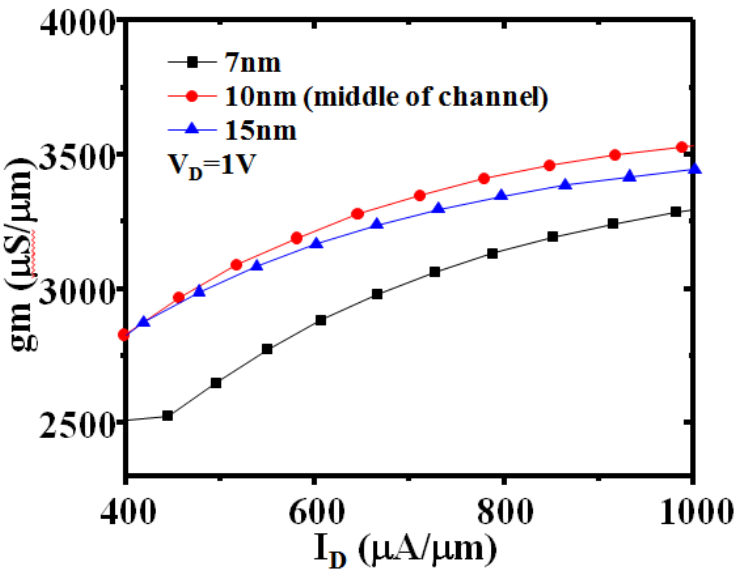


Fig. 2.18 Transconductance of graded channel device with different junction positions

Fig. 2.19 shows the output resistance for graded channel device with different junction location. As mentioned previously in the section 2.3.2, the graded channel device improves output resistance by decreasing the DIBL. As the junction is closer to drain side, the output resistance decreases. This is due to the fact that, as the junction moves toward the drain, the conduction band profile is becoming similar to the homojunction device, which makes the DIBL improvement smaller. Therefore, the improvement of output resistance is smaller when the junction is closer to drain [48].

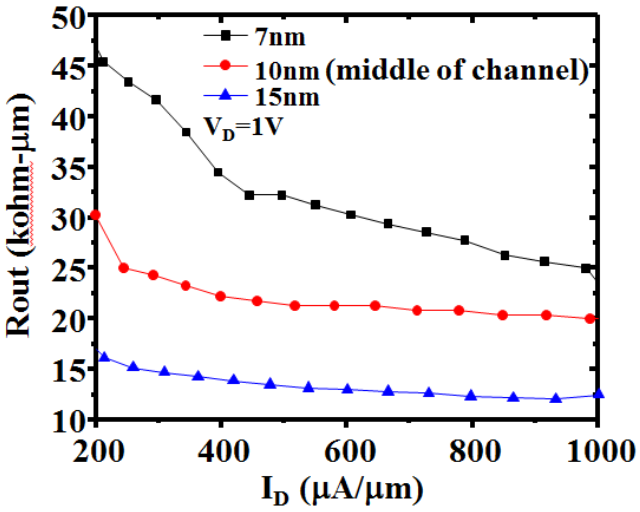


Fig. 2.19 Output resistance of graded channel device with different junction positions

2.5 Summary

In this chapter, TCAD simulation tools were calibrated to 14nm-node SOI and FinFET experimental data to capture the physics needed in short channel regime. Graded channel device with different electron affinities along the channel is then proposed and optimized. With proper design, graded channel device shows 5% improved g_m, 65% improved R_{out} and total 75% improved intrinsic gain compared to homojunction device in L_G=20nm regime. The

improvement is due to the redistribution of carriers and velocity along the channel, which results in enhanced electric field and increased injection velocity close to source side, and reduced electric field and decreased DIBL close to the drain side. This contributes to higher transconductance and output resistance and results in higher intrinsic gain.

Chapter 3

Deeply retrograde channel doping profile for improved digital performance

3.1 Introduction

In addition to thin down body thickness to achieve thin body like SOI and FinFET, there are other means to achieve it and deeply retrograde channel doping (DRCP) on bulk device is one of them. This doping profile can be properly designed such that the bulk device behaves like thin body device by reducing the short channel effect. While long channel DRCP devices was found to have lower drain current due to larger body factor in spite of the higher surface mobility [8,20,21], the DRCP device shows attractive characteristics in the sub 45nm regime [15,18,19]. However, the different characteristics between the reported long channel vs. short channel DRCP devices have not been well-understood in publications. In this chapter, the device physics, performance and optimization of deeply scaled MOSFETs with DRCP compared to devices with halo source drain (HSD) is investigated in detail by TCAD simulation. Our TCAD results revealed the origin of the superior DRCP short channel device (L_G=29nm), including the improved I_{on}/I_{off} (12% higher I_{on} and17% higher I_{eff} at a fixed I_{off} of 10nA/μm), 35% reduction in DIBL and 57% improvement in V_{TH} variability. The 14% higher transconductance and 40% higher output resistance also leads to 60% higher intrinsic gain and makes it attractive for SOC applications. Moreover, DRCP device is also compared with FinFET and SOI to show the capability of the DRCP device in short channel regime.

3.2 Device structure and concept

The ideal deeply retrograde channel profile consists of low surface doping and high retrograde doping as shown in Fig. 3.1. By properly design, the depletion region will only extend to the edge of the high retrograde doping and makes it a thin body like device. Fig. 3.2 shows the sharpest channel doping profile that can be achieved in experiment and it is 3.3nm/dec over two decades of doping changes [50,51].

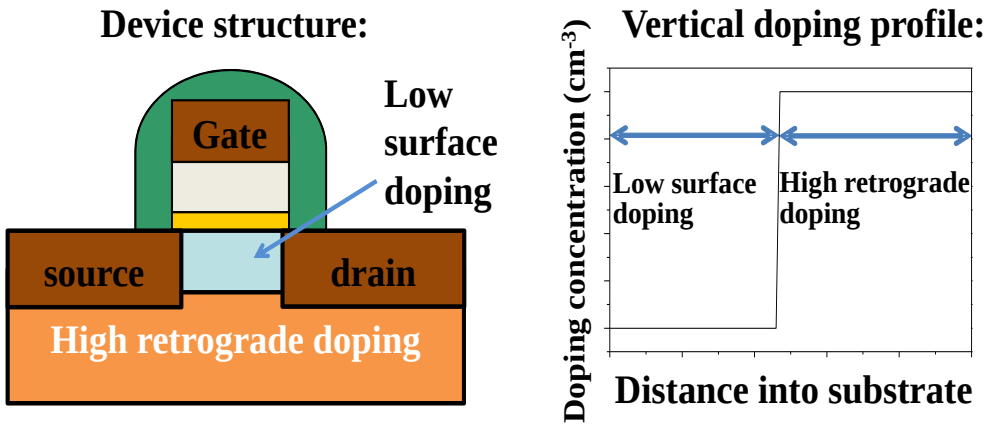


Fig. 3.1 Deeply retrograde channel doping profile

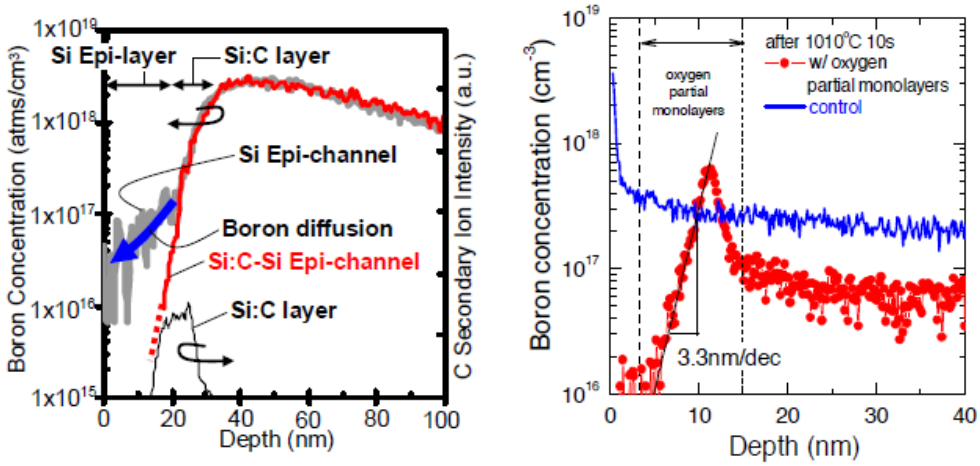


Fig. 3.2 Realistic doping profiles for deeply retrograde channel profile

In long channel, deeply retrograde MOSFET showed lower drain current and larger *SS* due to large body factor despite the higher surface mobility as can be seen in Fig. 3.3. [8,20,21] However, it showed higher I_D and I_{eff} in short channel due to the higher channel mobility in Fig. 3.4 [18]. This is due to the I_{on} is limited mainly by velocity saturation rather than carrier pinch-off near the drain, which will be addressed in details in the following sections. Therefore, unlike the long channel case, the backgating factor has only small effect on V_{DSAT}, as shown in Fig. 3.5.

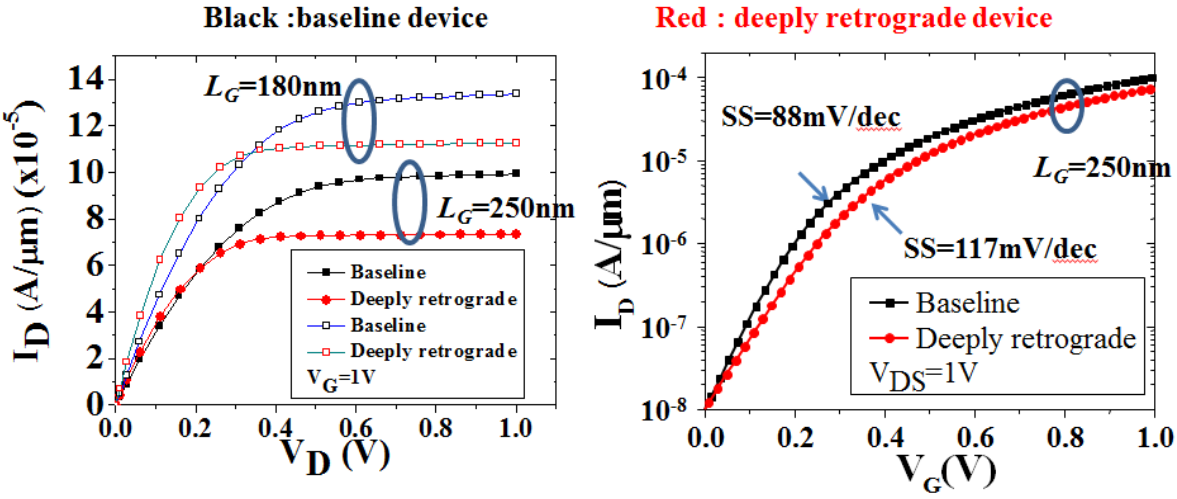


Fig. 3.3 I_D-V_D and I_D-V_G curves of long channel MOSFETs with deeply retrograde channel profile

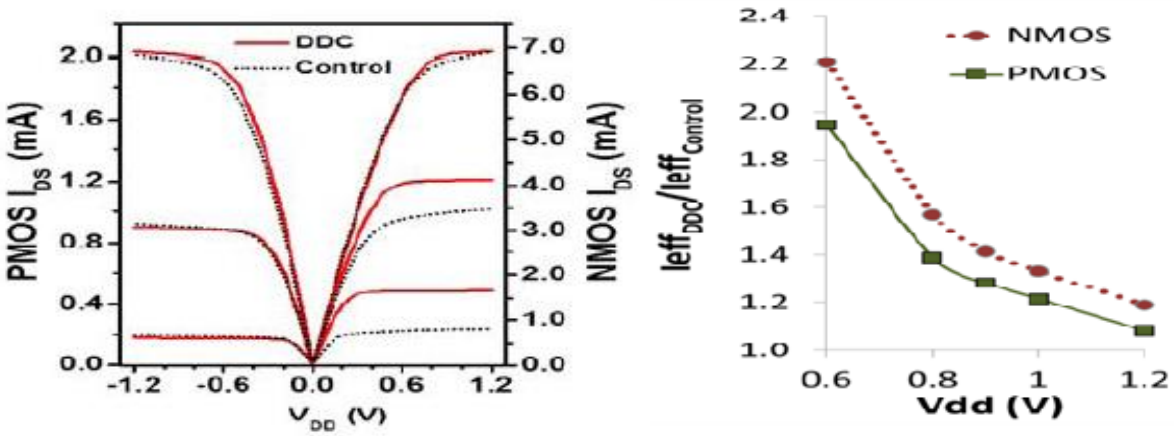


Fig. 3.4 I_D-V_D curves and I_{eff} of scaled MOSFET with deeply retrograde channel profile

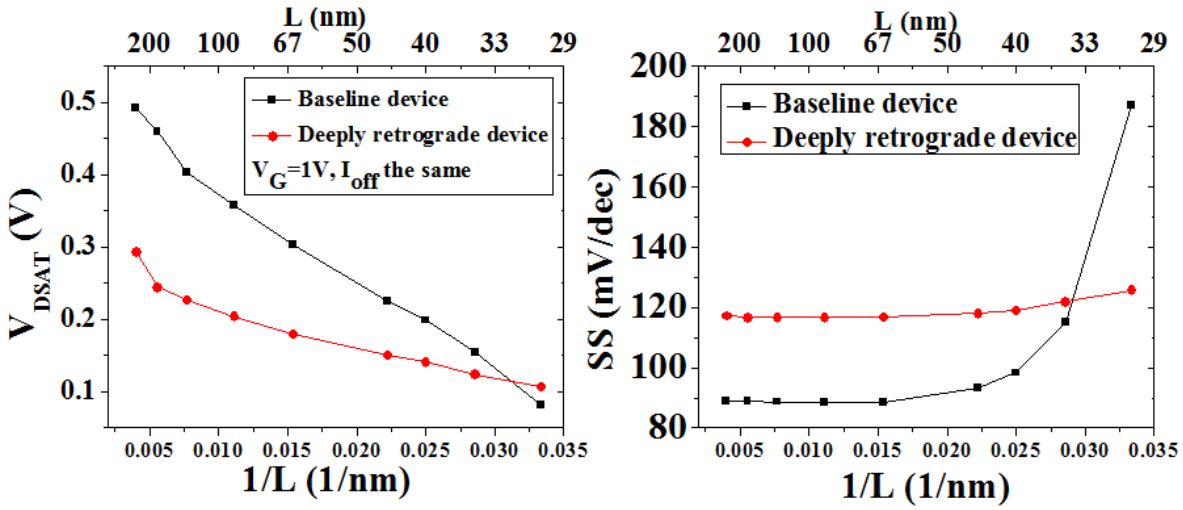


Fig.3.5 V_{DSAT} and *SS* v.s. 1/L for two channel profiles

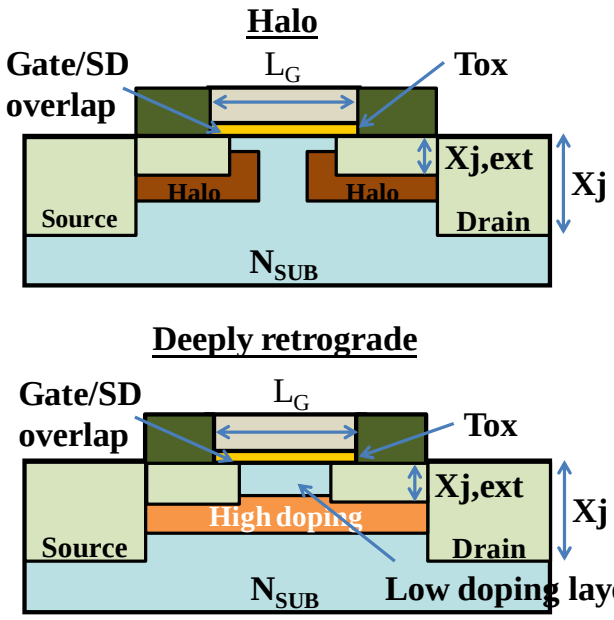
3.3 Simulation results

3.3.1 Simulation methodology and simulated device structures

In order to examine the physics of DRCP closely, device simulations were performed by using Sentaurus TCAD simulation software [36]. The simulation includes drift-diffusion transport, bandgap narrowing effect, and doping dependent, vertical field dependent and high field saturation model for mobility model. The drift-diffusion model was used for simplicity reason. The quantum-mechanical (QM) model was not included since it was estimated and found out it is not too critical in terms of comparing two devices. One might argue that DRCP device with thin low doping layer behaves like a quantum well, and therefore QM model is needed. However, the thinnest layer we are investigating in this chapter is 8nm, which QM effect is not too important. [44] The device structural parameters are from either ITRS or experimental data and the simulation was calibrated to experiment before simulation [37,15].

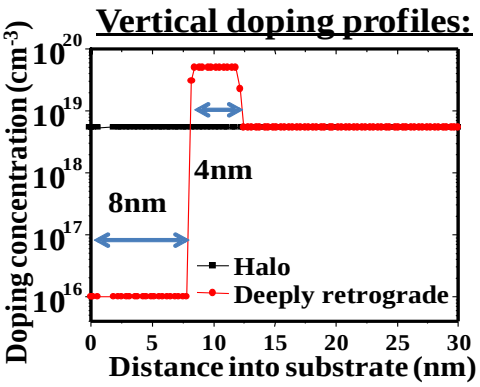
The V_{TH} variability simulation was done by impedance field method (IFM) approach [52,53]. IFM is an efficient way to evaluate the variability since it involves AC simulation and only need to simulate one device instead of many devices and calculate the mean and the standard deviation. It is based on linear response theory using Green's function technique and provides a faster and accurate alternative for statistical variability analysis. One more thing need to be mentioned about the variability simulation is, only RDF is included as the variability source and other sources are not considered. This is because the main source of V_{TH} variability in 45nm is RDF and DRCP offers low channel doping and therefore lower RDF compared to conventional device.

The DRCP device was investigated by comparing it with conventional bulk device (halo device). Fig. 3.6 shows the device structures for the two different channel profiles. One is DRCP device and the other one is conventional device with halo source drain. (HSD) For understanding physics purpose, abrupt junction and doping profiles (BOX-like) are assumed for both devices. The vertical channel doping profiles for the DRCP and HSD devices are shown in Fig. 3.7. They are considered to be practical case and optimized in terms of digital performance (I_{on}/I_{off}, subthreshold swing (SS), drain-induced-barrier-lowering (DIBL), and V_{TH} variability) by changing the halo and retrograde charge/dose as shown in Fig. 3.8 and 3.9. The halo charge was chosen to be $1x10^{13}cm^{-2}$ since it has overall optimal device characteristics (lowest SS, good I_{on}/I_{off}, low DIBL, and small V_{TH} variability). The optimal deeply retrograde charge was found to be $2x10^{13}cm^{-2}$, which happens to be the minimum amount to ensure the depletion width does not extend beyond the high doping layer.



L_G (nm)	29
Tox (nm)	0.9
$N_{SUB}(cm^{-3})$	$4.5x10^{18}$
Xj (nm)	29
Xj,ext (nm)	10.5
Gate/SD overlap (nm)	3.7

Fig. 3.6 Simulated device structures and device parameters for deeply retrograde and halo channel profiles



HSD	DRCP
Distance between top of Halo and Si/SiO_2 interface (nm) = 2nm	Doping concentration and depth for Low doping layer = $1x10^{16}cm^{-3}$ & 8nm
Doping concentration for halo = $1x10^{19}cm^{-3}$	Doping concentration and thickness for high doping layer = $5x10^{19}cm^{-3}$ & 4nm

Fig. 3.7 Simulated vertical channel doping profiles for halo and deeply retrograde

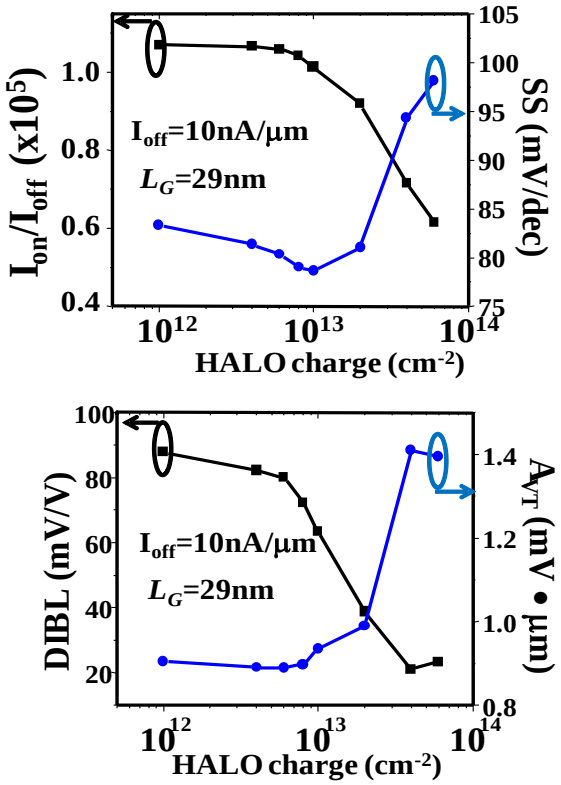


Fig. 3.8 Trade-off in terms of I_{on}/I_{off}, SS, DIBL and V_{TH} variability by changing the halo charge. The halo charge was chosen to be $1x10^{13}cm^{-2}$ here

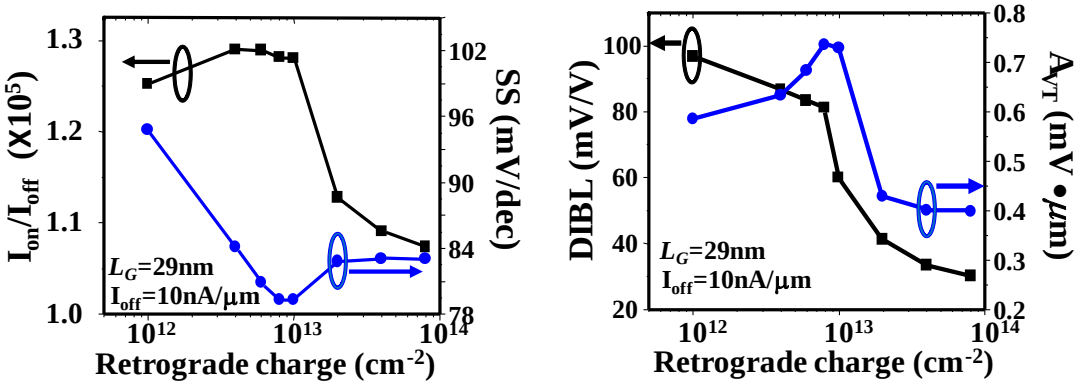


Fig. 3.9 Trade-off in terms of I_{on}/I_{off}, SS, DIBL and V_{TH} variability by changing the retrograde charge. The retrograde charge was chosen to be $2x10^{13}cm^{-2}$ here

3.3.2 Improved digital performance

Fig. 3.10 (a) shows the output characteristics of the two devices with L_G=29nm. It is apparent that the DRCP transistor shows much more ideal-like behavior than HSD. The digital device performances for the two devices are extracted out and listed in Table 3.1. The DRCP has 12% higher I_{on}/I_{off}, 17% higher I_{eff}, 35% lower DIBL, and a small 3mV/dec higher SS. Unlike the longer channel case, DRCP has improved I_{on} due to higher channel mobility even though it has larger backgating factor. The difference is that in scaled device, I_{on} is limited mainly by velocity saturation rather than carrier pinch-off near the drain. Therefore, unlike the long channel case, the backgating factor has only small effect on V_{DSAT}, as can be seen in Fig. 3.10 (b). I_{eff}, which is defined to be $(I_H+I_L)/2$ with I_H is the I_{DS} when $V_{GS}=V_{DD}$ and $V_{DS}=V_{DD}/2$, and I_L is the I_{DS} when $V_{GS}=V_{DD}/2$ and $V_{DS}=V_{DD}$, is known to be a better matrix for gate delay [54]. Due to the higher output resistance resulting from improved DIBL, DRCP device has larger improvement in I_{eff} than I_{on} compared to HSD device, further indicating the advantage of scaled transistors with DRCP.

The DIBL improvement of DRCP can be explained by Fig. 3.11. It shows the DRCP can diverge the lateral electric field from drain side to the high retrograde doping layer, in addition to providing charges to reduce the drain side electric-field as in the case of HSD. Therefore, DRCP is more effective in minimizing drain junction's influence on the virtual cathode. As a result, the device with DRCP is more effective in suppressing SCE than HSD device. Fig. 3.12 shows the DRCP has smaller $\Delta\phi$ (ϕ is the diffusion barrier) compared to HSD when V_{DS} increases from 0.1 to 1V. This translates to a DIBL improvement of 35%.

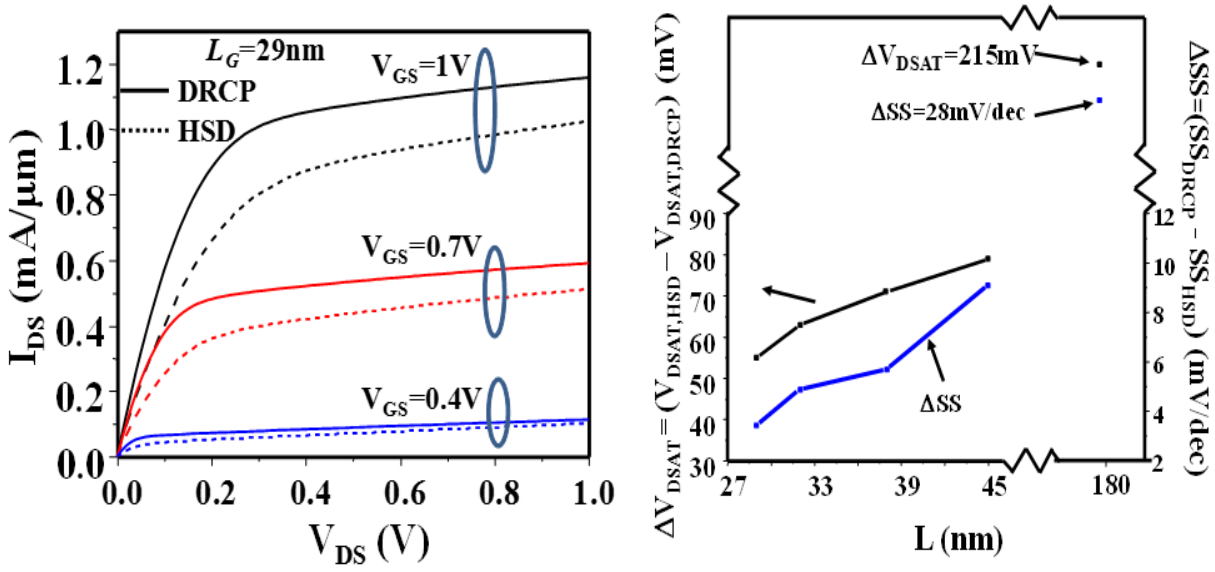


Fig. 3.10 (a) Output characteristics of DRCP and HSD device (b) The V_{DSAT} and SS difference vs channel length for two doping profiles

	Halo	**Deeply retrograde**	**Improvement by deeply retrograde**
I_{on}/I_{off}	1.02×10^5	1.15×10^5	+12.7%
I_{eff} (A/μm)	5.62×10^{-4}	6.59×10^{-3}	+17.2%
DIBL (mV/V)	68.8	44.4	-35%
SS (mV/dec)	78.4	81.8	+3.4mV/dec

Table 3.1 Digital device performance comparison for deeply retrograde and halo devices

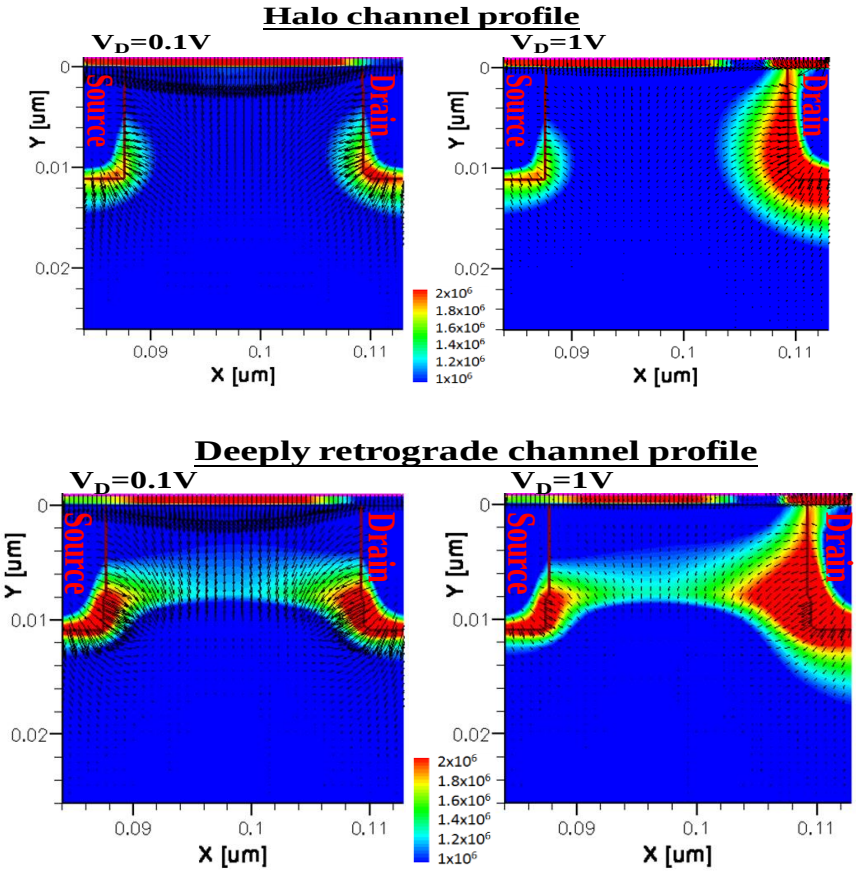


Fig. 3.11 The 2-D electric field distribution with arrows to pointing the direction of electric field for halo and deeply retrograde channel profiles inside the channel region

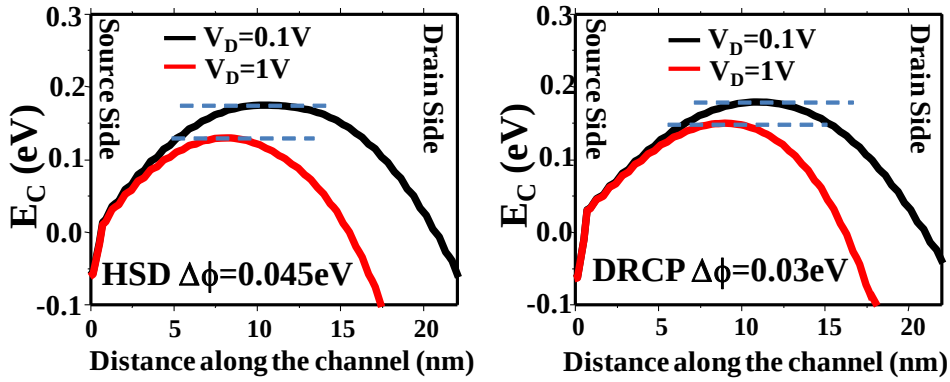


Fig. 3.12 The conduction band edge comparison of the deeply retrograde and halo channel profile inside the channel region for V_D=1V and 0.1V

3.3.3 Improved threshold voltage variability

The variability makes the system more power consuming, degrade system speed and cause low noise margin. The V_{TH} variability sources include random dopant fluctuation (RDF), line edge roughness (LER), gate edge roughness (GER) and interface trapped charge (ITC) and the main origin of the V_{TH} variability is RDF in 45nm technology node for planar device. [16,55] The origin of the RDF is due to the variation in number and position of dopant atoms in the transistor channel. These obstacles can be minimized by adopting novel device structures such as FDSOI or FinFET in scaled MOSFET as shown in Fig. 3.13 [3,17,56]. However, these solutions are more expensive and complicated compared to planar bulk MOSFETs.

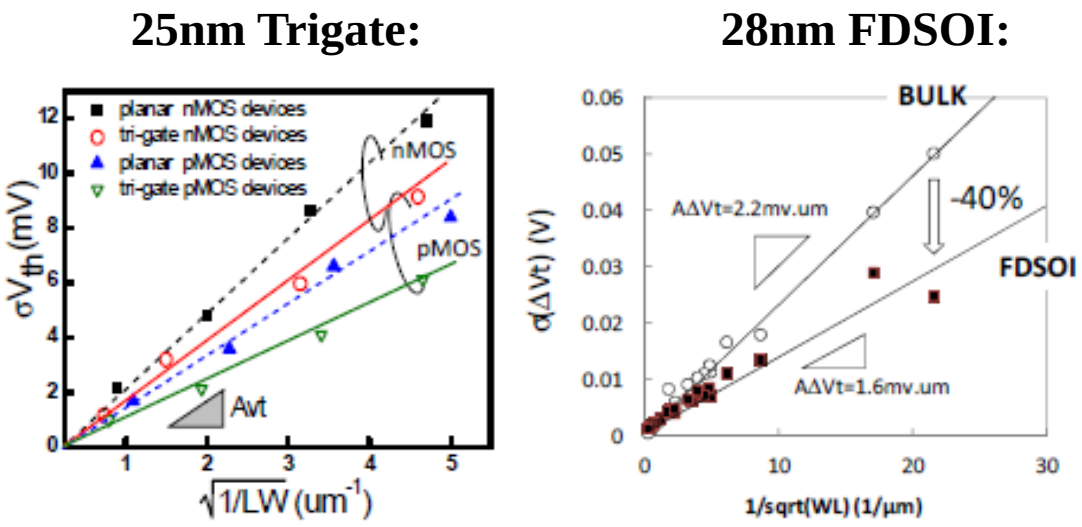


Fig. 3.13 V_{TH} variability by adapting 3D and FDSOI device structures

To first order, DRCP device can improves variability by lower the surface doping concentration compared to conventional device. The empirical model indicates that the relationship between V_{TH} variability and doping concentration is [57]:

$$\sigma V_T = 3.19\times10^{-8}\times\frac{t_{ox}N_A^{0.401}}{\sqrt{L_{eff}W_{eff}}}$$

where t_{ox} is effective oxide thickness, N_A is channel doping concentration, L_{eff} is channel length and W_{eff} is channel width, all dimensions are in centimeters. Simulation was done to verified this and the results shows that DRCP has A_{VT} of 0.435mV*μm and HSD device has 1mV*μm, which suggesting 57% lower A_{VT}. The low A_{VT} compared to the experimental data [58,59] is due to two reasons: 1. the ideal BOX-like profile used in simulation, 2. the simulation only considers RDF as the variability source. RDF is ~60% of the overall V_{TH} variability in 45nm node [16]. Adding these two effects up makes the simulated A_{VT} comparable to experimental results as shown in Fig. 3.14. Gaussian profiles with different standard deviation in Fig. 3.15 were also simulated to examine the impact of the doping profile sharpness (non-ideal BOX-like doping profile). As expected, the higher the standard deviation (that is, profile which is less deeply retrograde), the higher the A_{VT} and the A_{VT} of DRCP will behaves like HSD device since the channel doping profile is more or less uniform as shown in Fig. 3.16.

Simulation of devices with different retrograde and halo doping concentrations were also performed to check how the doping level affects the variability as shown in Fig. 3.17 and 3.18. As shown in Fig. 3.18, the V_{TH} dependence on the retrograde doping concentration of DRCP is much smaller than V_{TH} dependence on channel doping of HSD. Similarly, the V_{TH} of DRCP device has only weak dependence on the retrograde profile depth. These results correlate well with the results of A_{VT} and indicate that the DRCP has intrinsically better variability immunity.

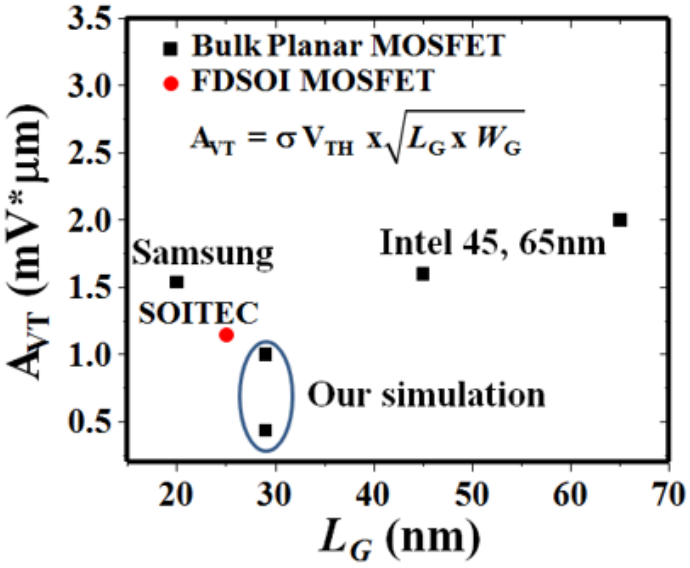


Fig. 3.14 A_{VT} comparison between our simulation and experiments

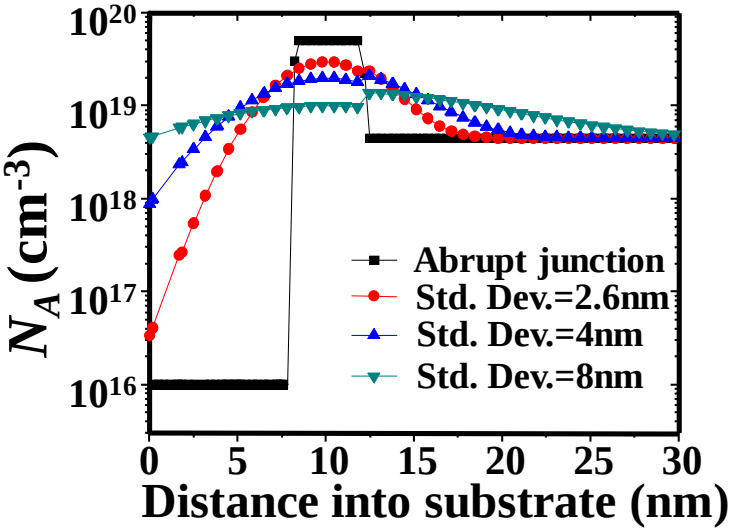


Fig. 3.15 Vertical doping profiles when changing the standard deviation of Gaussian profile for deeply retrograde channel profile devices

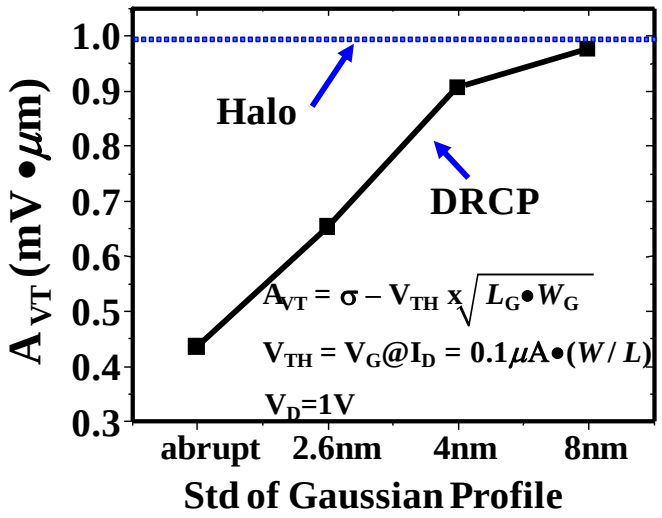


Fig. 3.16 A_{VT} of deeply retrograde Gaussian channel profiles with different standard deviation.

A_{VT} increases with increasing standard deviation

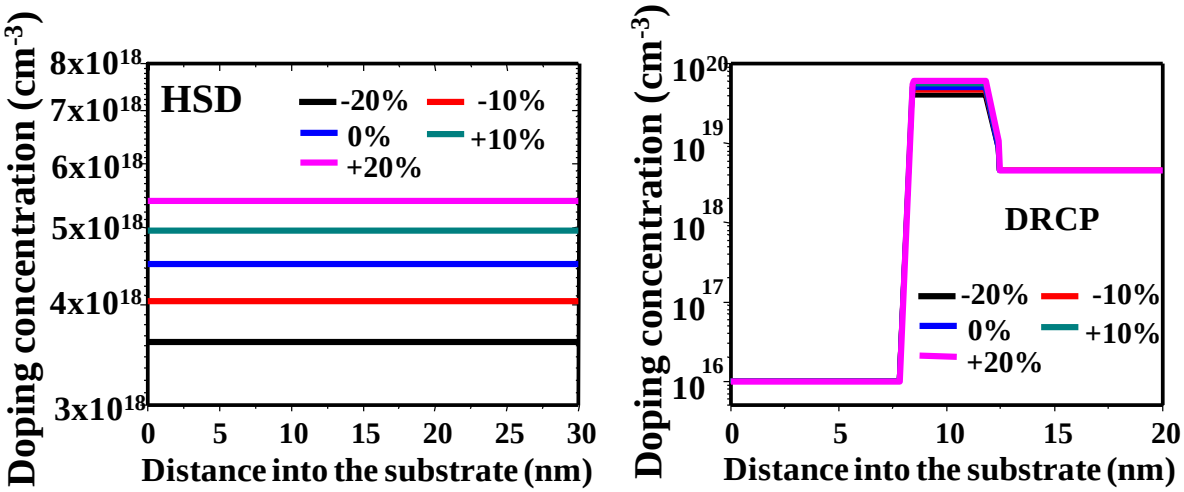


Fig. 3.17 DRCP devices with different deeply retrograde channel doping concentrations and HSD devices with different substrate doping

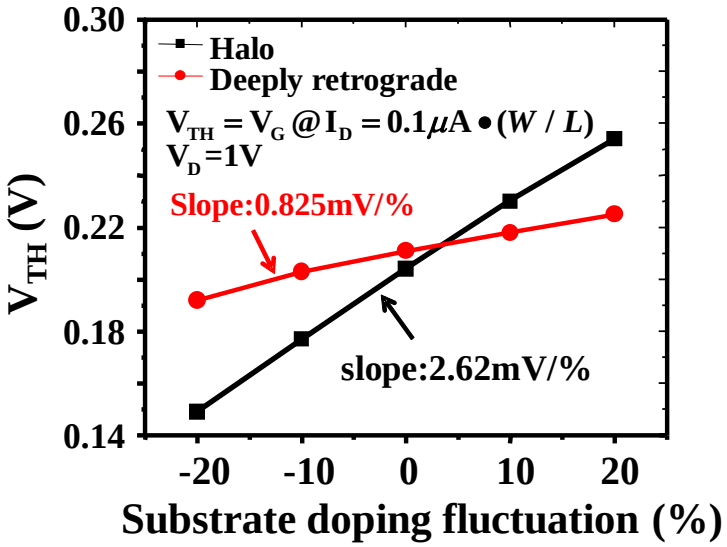


Fig. 3.18 V_{TH} variation by changing the doping concentration for two channel profiles. DRCP shows smaller slope than HSD and the difference correlate well to the A_{VT} results

3.3.4 Improved analog performance

Besides digital performance, the analog performance of DRCP and HSD are also compared to investigate whether DRCP can be applied for SOC applications. For analog applications, transistors are typically biased at small I_{DS} for good dynamic range. Fig. 3.19 shows that at a fixed I_{DS} of 200μA/μm, due to the higher channel mobility, DRCP device has 14% higher g_m compared to the HSD device. Note that while I_{on} benefit from high μ, it is ultimately limited by v_{sat} so such ~15% improvement may not be maintained in high drain current regime. At low I_{DS} (small V_G-V_T), v_{sat} is not the limiting factor. I_{DS} and therefore g_m at small V_G-V_T are basically determined by μ, and show bigger improvements compared to I_{on}. The DRCP also has improved gate control (i.e. reduced SCE) which also contributes to higher g_m. In long channel transistors, the R_{out} is determined by the channel length modulation (CLM). For scaled devices, both CLM

and DIBL contribute to R_{out}. While long channel MOSFETs with deeply DRCP has worse CLM due to the larger backgating factor, this is not the case for scaled devices as evident in almost identical SS for both doping profiles as shown in the 3.3.2 section. On the other hand, scaled devices with DRCP have 35% smaller DIBL, which is responsible for the R_{out} improvement as shown in Table 3.1. Due to both the improvement from g_m and R_{out}, DRCP device has a significant higher intrinsic gain (g_m*R_{out}) of 60% compared to the HSD device, especially when the biasing current, I_{DS}, is small as shown in Fig. 3.20.

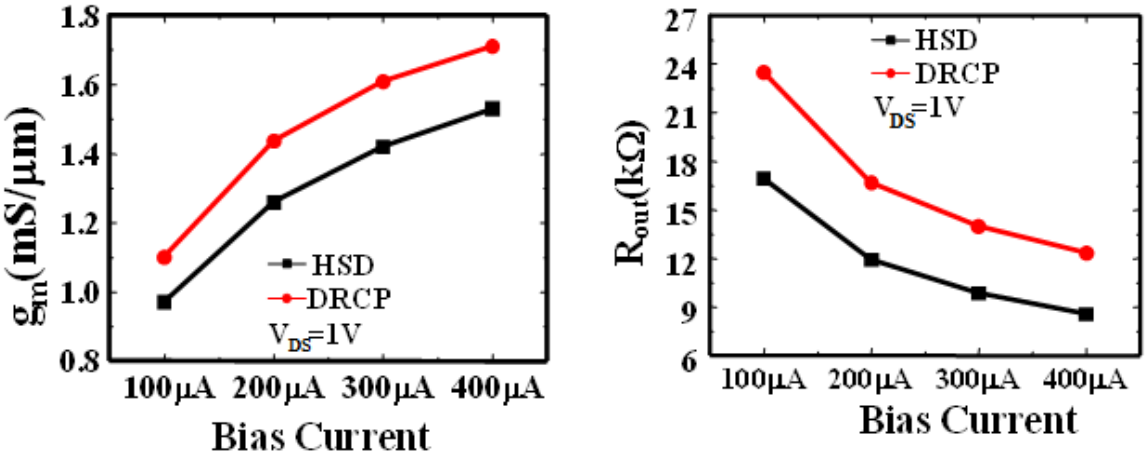


Fig. 3.19 The g_m and R_{out} vs bias current for deeply retrograde and halo channel profiles.

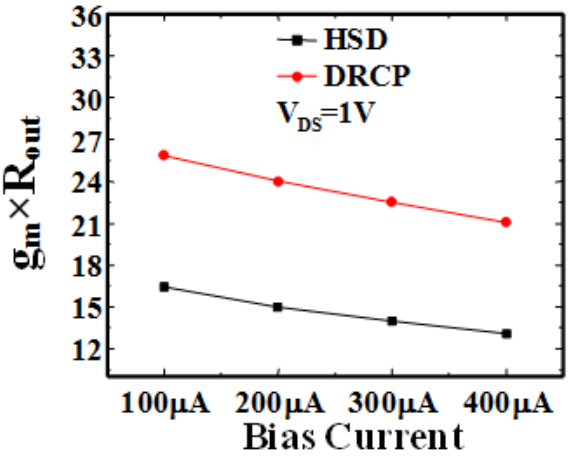


Fig. 3.20 The intrinsic gain (g_m x R_{out}) vs bias current for deeply retrograde and halo channel profiles

3.3.5 Comparisons of DRCP device, conventional bulk device, SOI and FinFET

DRCP device has shown improved digital and analog performances (higher I_{on}/I_{off}, higher I_{eff}, lower DIBL, lower variability, higher g_m, higher R_{out} and higher intrinsic gain) compared to halo device at L_G=29nm. It is also cheaper and less complicated in manufacturing aspect compared to SOI and FinFET. It is then interesting to learn whether DRCP device can outperform SOI and FinFET, especially in short channel regime since SOI and FinFET have been adopted in L_G=20nm regime. Different device performances of DRCP device, bulk device, SOI and FinFET are compared in this sections. The comparisons of V_{TH} variability for DRCP device, bulk device, SOI and FinFET are shown in Fig. 3.21 [3,5,16,18,58,59,60,61,62]. It shows that DRCP device can deliver around 2 times lower V_{TH} variability than conventional bulk device down to L_G=29nm and DRCP has similar variability (~A_{VT}=1.2mV*μm) as SOI and FinFET at 20nm regime since the doping concentration of channel region in SOI and FinFET are also very low and leads to reduced variability from RDF.

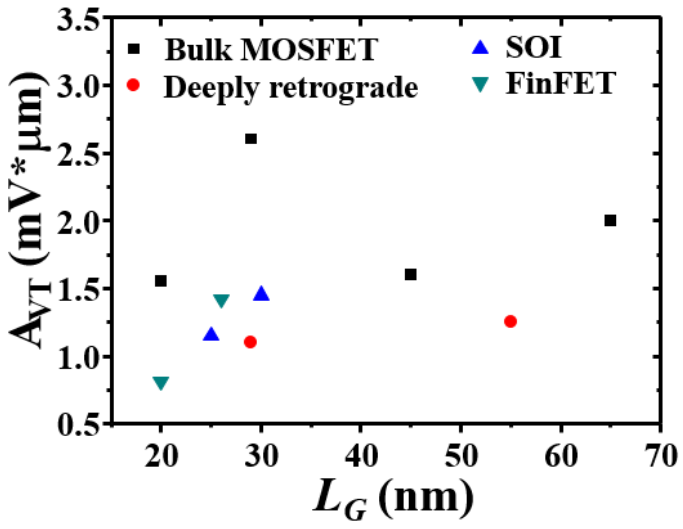


Fig. 3.21 V_{TH} Variability comparisons of DRCP device, halo device, SOI device and FinFET

The short channel effect in terms of DIBL and SS are also compared in Fig. 3.22 [3,5,26,27,63,64,65,66,67]. Basically, DRCP device has comparable DIBL and SS as SOI and FinFET due to good short channel effect control. As for the on-current shown in Fig. 3.23 [3,5,26,27,63,64,65,66,67], DRCP device can also deliver same order of magnitude on current as SOI and FinFET in spite of slightly higher V_{DD} (1V vs. 0.7-0.9V). However, such comparable performance is only observed down to L_G=29nm since the depth of high retrograde doping (thickness of low surface doping layer) in our simulation is 8nm and the doping difference between high retrograde doping and low surface doping is 3.5 decades, which means ~2.3nm/dec is required to realize such channel doping profile. The sharpest doping profile in today's technology is 3.3nm [51] and sharper doping profile is needed to maintain the DRCP device's short channel effect (DIBL and SS) and on current as compared to SOI and FinFET when channel length decreases.

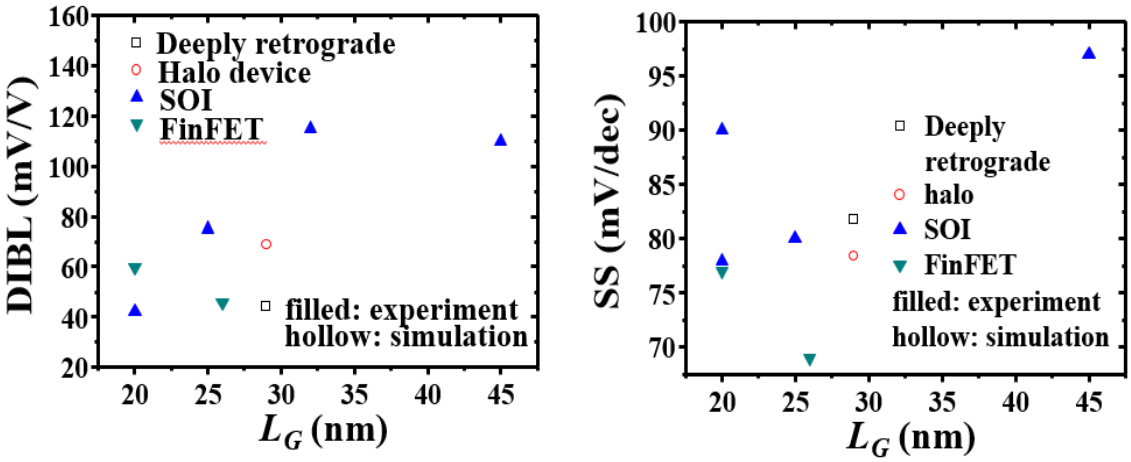


Fig. 3.22 DIBL and SS comparisons of DRCP device, halo device, SOI device and FinFET

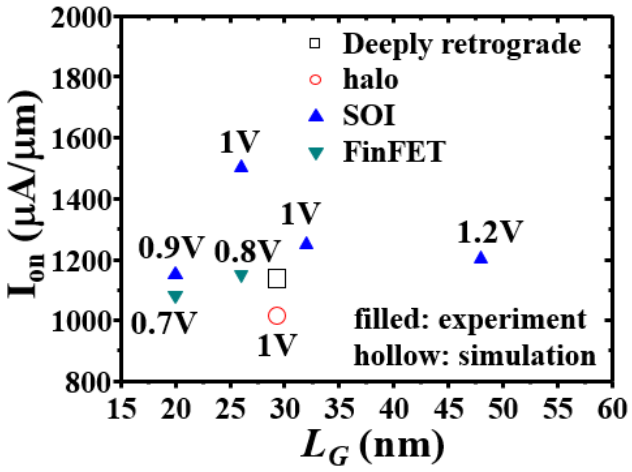


Fig. 3.23 On current comparisons of DRCP device, halo device, SOI device and FinFET

3.4 Summary

In this chapter, the physics and advantages of scaled planar MOSFETs with DRCP was examined in detail. It was shown that this device has substantial performance advantages compared to HSD MOSFETs. In terms of digital applications, ideal DRCP devices have 12% higher I_{on}/I_{off}, 17% higher I_{eff}, 35% lower DIBL, and 57% lower V_{TH} variability at a fixed I_{off} of 10nA/μm. This is due to the better SCE control, higher channel mobility and lower doping concentration in the channel. As for the analog performance, it has 14% higher transconductance and ~40% higher output resistance, which results in 60% higher intrinsic gain. These results indicate DRCP is a promising choice for analog/SOC and high performance digital applications down to L_G=29nm. The DRCP device is also compared with conventional bulk device, SOI and FinFET to show the capabilities. It shows that the DRCP device has comparable A_{VT}, DIBL, SS and on-current down to 29nm regime. However, it needs sharper doping gradient to maintain this trend when channel length decreases.

Chapter 4

Doped WSe_2 channel field-effect transistor for back end applications

4.1 Introduction

Using two dimensional (2D) materials such as transition metal di-chalcogenides (TMDs) as channel material is another approach to form thin body transistor. TMDs were recently investigated to exploit their advantages such as better electrostatic control and potential superior transport properties for field effect transistor fabrication [9,22,23,24]. It is expected that it can provide higher on-current due to the improved short channel effect from the ultra-thin body. Nonetheless, device simulation based on drift-diffusion model shows that MoS_2 channel transistor can't deliver comparable on-current as other thin body transistors like FinFET and SOI down to 10nm regime, though it shows better short channel effect such as smaller DIBL and SS as shown in Fig. 4.1 and Fig. 4.2. Moreover, the on-current can't be further improved by higher mobility since it is limited by the saturation velocity as shown in Fig. 4.3 [26].

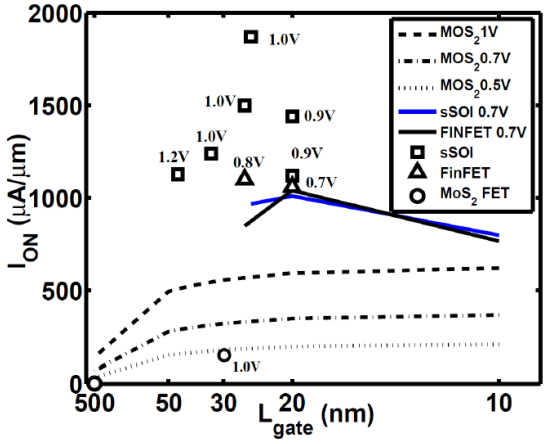


Fig. 4.1 On current comparisons of MoS_2 channel FET, SOI device and FinFET

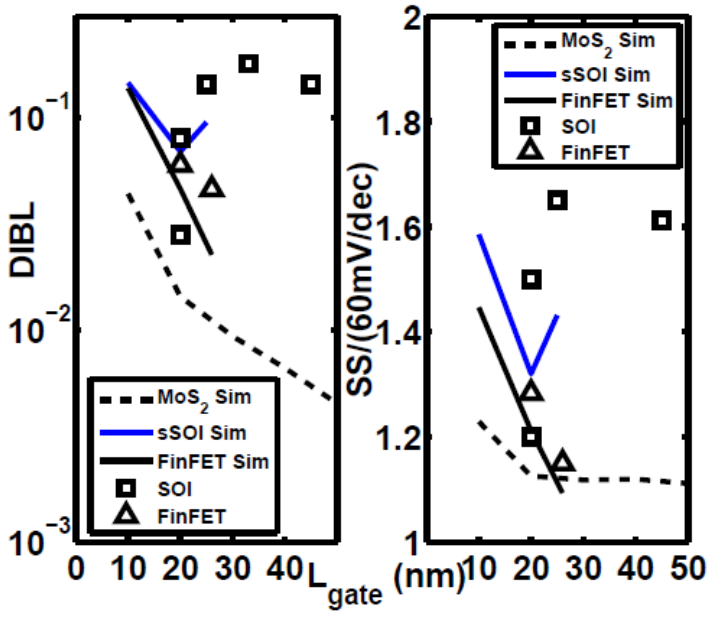


Fig. 4.2 Short channel behaviors comparisons of MoS_2 channel FET, SOI device and FinFET

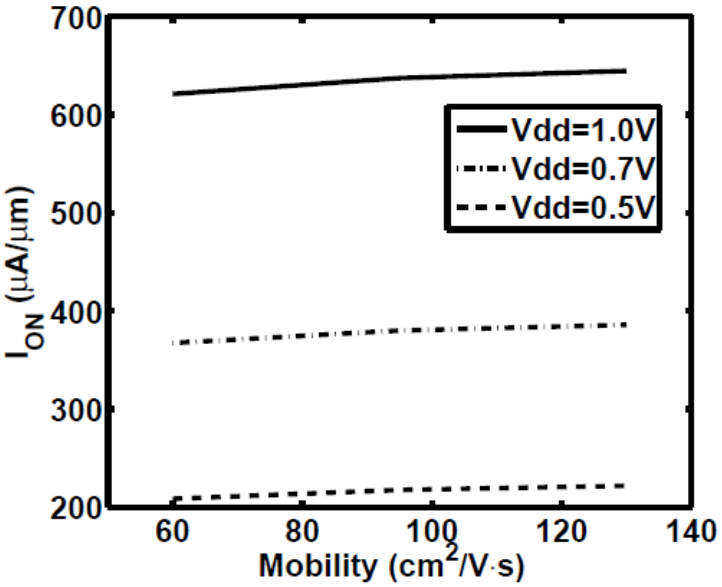


Fig. 4.3 On current improvement of MoS_2 channel FET from mobility

However, WSe_2 may have better performance than MoS_2 since it is not investigated completely like MoS_2. Among these 2D materials, WSe_2 is also particularly attractive since it can be used as p-FET and makes the CMOS operation feasible [10]. However, lack of reliable doping technique makes the precise doping of the WSe_2 very difficult to achieve [10,11]. In this chapter, WSe_2 doped by controllable W:Ta co-sputtering process and synthesized by post selenization is investigated. Material preparation and characterization of WSe_2 are discussed. Using this technique, high accepter doping concentration (N_A=6x$10^{13}$$cm^{-2}$) and good hole mobility (=16.5cm^2/Vs) were extracted from MESFET transfer curve. Low sheet resistance (17kΩ/sq) and contact resistance (11.4kΩ-μm) were obtained by using palladium metal in transmission line method (TLM) structure. Although the simulation study shows that 2D materials like MoS_2 can't deliver comparable on current than silicon based thin body devices such as FinFET and SOI devices, the high doping and good mobility achieved by co-sputtering process and post selenization can still make WSe_2 a potential channel material in thin film transistor for back-end applications.

4.2 WSe_2 thin film preparation and material characterization

4.2.1 WSe_2 thin film preparation

There are many different ways to prepare WSe_2 thin film for transistor fabrication like mechanical exfoliated, and CVD related synthesis [23,68,69]. Among these methods, CVD related synthesis is more feasible for VLSI applications due to the non-controllable position and thickness produced by exfoliated method. Therefore, CVD-like synthesis by using post selenization is chosen to prepare the WSe_2 film in this chapter. In addition, WSe_2 was doped by

W:Ta co-sputtering process since the doped WSe_2 film is essential to lower source/drain contact resistance and enable the CMOS operation.

The following Fig. 4.4 shows the preparation flow of the doped WSe_2 thin film. First, W and Ta were co-sputtered to deposit thin film on top of the SiO_2 film (90nm SiO_2 is chosen so that WSe_2 can be observed under optical microscope). The p-type doping concentration in the film can be controlled by the sputter power ratio of the W and Ta. Second, selenization was done at 750°C-800°C by using 15% H_2Se as precursor in furnace. The H_2Se serve as the selenization source to form WSe_2 and the selenization process can be optimized by tuning the H_2Se concentration and furnace temperature to obtain WSe_2 with good quality.

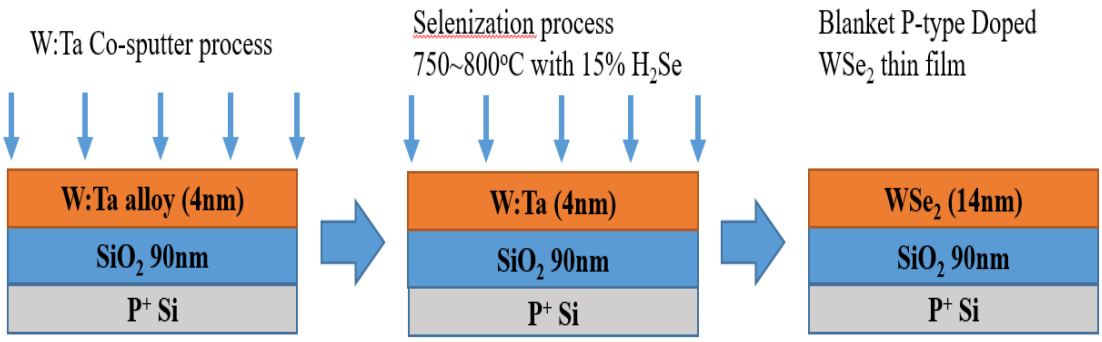


Fig. 4.4 Preparation flow of WSe_2 thin film prepared by W:Ta co-sputtering process and post selenization process

4.2.2 Material characterization of WSe_2 film

Different material characterizations were used to analyze the composition and the film structure of the films, as shown in Fig. 4.5 Raman spectroscopy with 532nm wavelength was used to check the existence and thickness of the WSe_2. A typical Raman spectrum for WSe_2 is observed after co-sputtering process and it closely matches the experimental data for bulk WSe_2

[70]. XRD analysis shows that there is a c-axis prefer-oriented (002) peak without peak shift. TEM picture show that the thickness is ~14nm after selenization. XPS analysis is also conducted with only W-Se and Ta-Se bond signals detected, which suggests that substitution between dopant Ta and W atom are achieved during the co-sputtering process. Hall measurement is employed to estimate p-type doping concentration and hole mobility – around ~$10^{13}cm^{-2}$ and around ~10 cm^2/Vs were measured, suggesting that WSe_2 is highly p-doped after preparation.

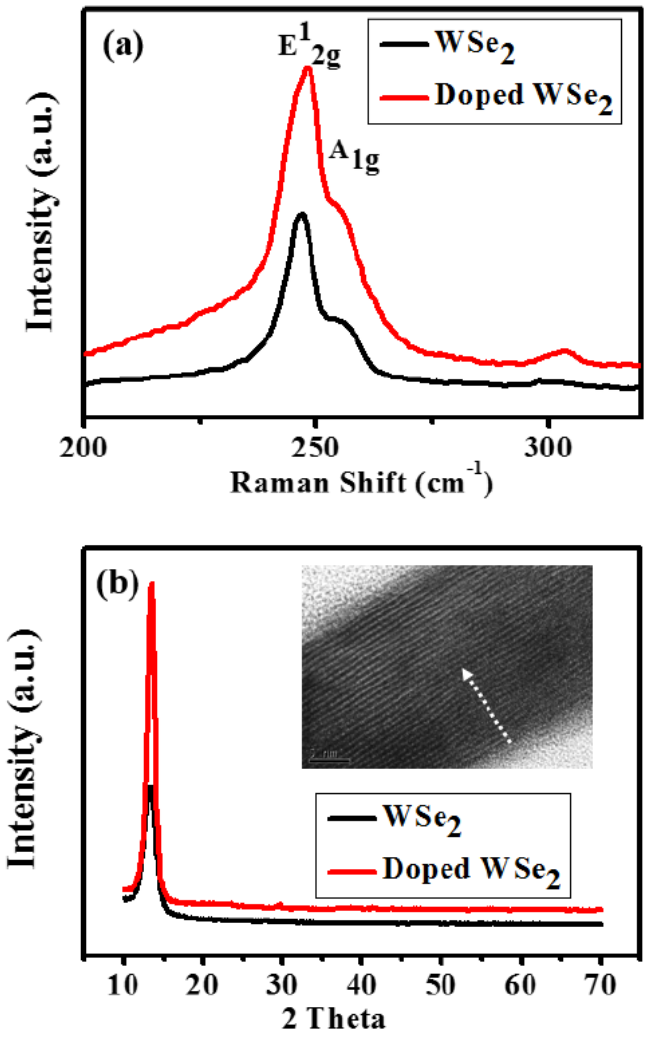


Fig. 4.5 Raman spectrum, XRD analysis and TEM picture after the WSe_2 preparation

4.3 Contact resistance and sheet resistance measured by TLM structure

4.3.1 TLM fabrication process

In order to lower the source/drain contact resistance for transistor operation, TLM structure is used to measure the contact resistance and sheet resistance. Since the doped WSe_2 film is p-type, palladium which has large work function (~5.12eV) is used as contact metal. The following is a table (Table 4.1) depicts the process flow of the TLM structure fabrication and the Fig. 4.6 is the layout for TLM structure. The contact length of the layout is 20um and the width is 20um.

Process flow steps	**Description/details**
Starting materials	14nm WSe_2/90nm SiO_2/p-type silicon wafer
S/D formation	Image reversal lithography + deposit 40nm Pd/80nm Au as S/D pad + lift off
Active area definition	Lithography + SF6 etch 150W 30s + strip PR

Table 4.1 Process flow of TLM structure

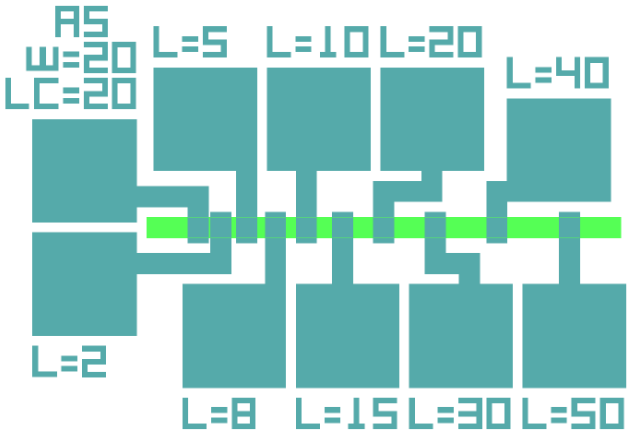


Fig. 4.6 TLM structure mask pattern

4.3.2 The characteristics of TLM structure

Fig. 4.7 shows the characteristics of Pd/WSe_2 TLM structure. Large current level (15μA/μm at V_D=1V and channel length=2μm) was obtained and the current voltage curves are very linear for TLM structures with different length. The contact resistance and sheet resistance were extracted out to be 11.4kΩ-μm and 17kΩ/sq from resistance versus length relationship based on TLM model. This results are compared with other WSe_2 literatures published recently and found out that they are comparable or better [23]. In order to have a rough idea of how much p-type doping concentration is achieved by using co-sputtering process, back envelope calculation is used. The calculation results show that the doping concentration would be $1x10^{14}cm^{-2}$ if assuming mobility as $10cm^2/Vs$ and such doping is very high even compared to silicon case. Such high p-type doping concentration in WSe_2 implies why the contact resistance and sheet resistance is low and suitable for FET operations. However, it also serves as an evidence to explain why the MESFET can't be completely turned off as will be shown in the next section.

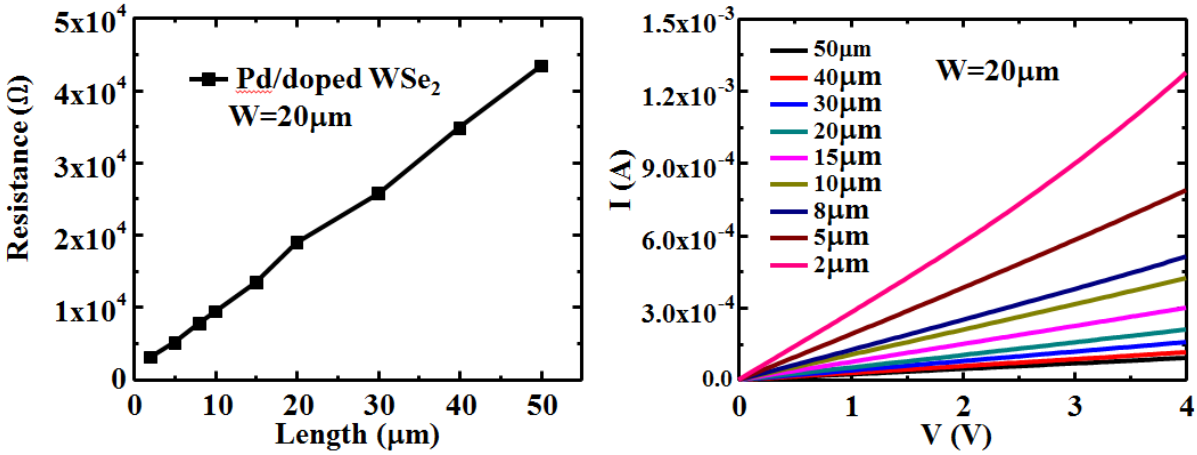


Fig. 4.7 TLM characteristics of Pd/p-type doped WSe_2

4.4 Fabrication and characteristics of WSe_2 MESFET

4.4.1 WSe_2 MESFET fabrication

After the analysis of TLM, WSe_2 was used as channel material for MESFET fabrication to examine the device performance. MESFET was chosen since the metal/WSe_2 interface quality might be better than dielectric/WSe_2 interface quality and provide better gate modulation. Another advantage of MESFET is that it is easier to fabricate than MOSFET and provide faster feedback. The table 4.2 depicts the process flow of the MESFET fabrication. It makes the device fabrication free from transfer process with WSe_2 sits on top of the SiO_2. Source/drain palladium metal was deposited before etching WSe_2 film to ensure the large contact area. Aluminum metal was chosen to be the gate metal to form large barrier between Al/WSe_2 and ensure the low gate leakage current.

Process flow steps	**Description/details**
Starting materials	14nm WSe_2/90nm SiO_2/p-type silicon wafer
Source/Drain definition	Image reversal lithography with PR AZ-5214-E
Source/Drain deposition	E beam evaporation 40nm Pd/80nm Au
Source/Drain formation	Strip PR by lift-off using acetone
Active area definition	Lithography with PR AZ-5214-E
Remove mask	Strip PR with acetone
Gate definition	Image reversal lithography with PR AZ-5214-E
Gate deposition	E beam evaporation 120nm Al
Gate formation	Strip PR by lift-off using acetone

Table 4.2 Process flow of MESFET structure

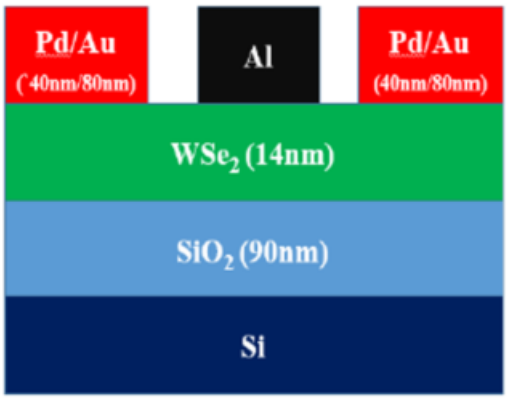


Fig. 4.8 Device structure for MESFET

4.4.2 Characteristics of WSe_2 MESFET

The transfer curve and output curves of MESFET are shown in Fig. 4.9 and Fig. 4.10. It clearly displays p-type behavior with large on-current (6μA/μm at V_D=1V and channel length=6μm) and very linear output behaviors. It is worth noting that the device cannot be turned off completely, implying that the depletion width cannot extend to the whole WSe_2 film due to extremely high doping concentration. In Fig. 4.11, back gate bias is also applied to provide more gate modulation but it only changes drain current by less than 2%, which implies that the doping of the WSe_2 is very high. In order to verify this and compare with the TLM measurement results, the p-type doping concentration (N_A) and mobility (μ_p) are extracted from the MESFET's transfer characteristics at V_D=0.1V by using transconductance method. W is channel width and L is gate length. The underlap resistance (R_{ul}) of MESFET is calculated by assuming $V_D/I_D=R_{ch}+2R_{ul}$. The slope of the I_D-V_G, given by $R_{ch}=(1/q\mu_p N_A)\times(L/W(14\text{nm}-W_D))$ where W_D =

$\sqrt{2\epsilon_{WSe_2}(V_{bi}+V_{GS})/qN_A}$ is used to obtain the N_A and μ_p. The relative permittivity ϵ_{WSe2} is assumed to be 4.5 based on [71]. The build-in potential V_{bi} is calculated to be 0.85eV by assuming the electron affinity of WSe_2 and work function of Al to be 3.9eV and 4.05eV, and the bandgap of WSe_2 is 1eV since 14nm WSe_2 is considered to be similar to bulk WSe_2 [70]. The calculated values of N_A and μ_p are $6x10^{13}cm^{-2}$ and $16.5cm^2/Vs$, respectively. It shows that WSe_2 is heavily p-type doped and it also agrees with Hall measurement results in 4.2 section.

There is a discrepancy between the sheet resistance measurement results from TLM (17kΩ/sq) and the calculation results from transistor's results (6.3kΩ/sq). It might be attributed to the non-uniformity of the WSe_2 film during the co-sputtering process. Another possible reason might be due to the influences introduced from Al metal gate on top of the WSe_2 film.

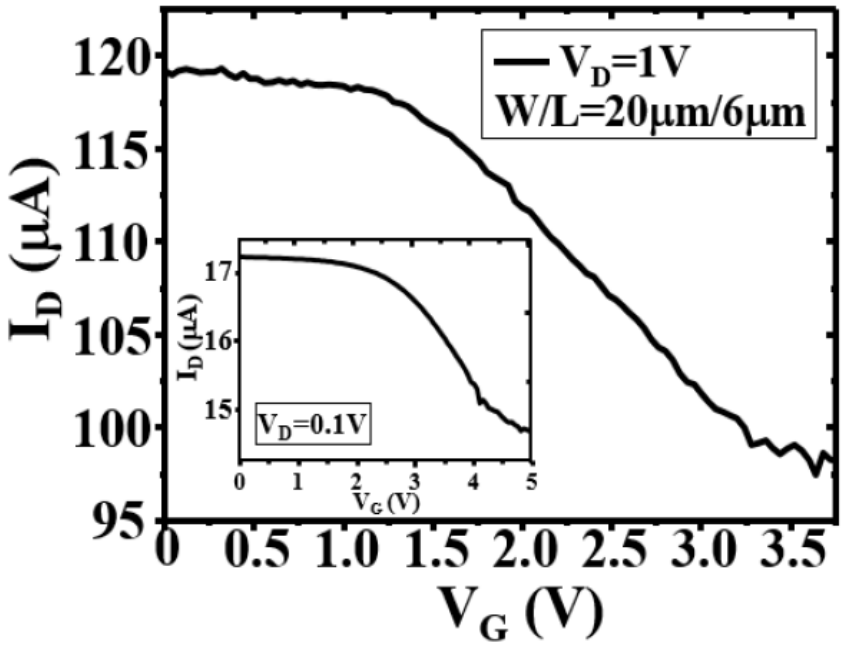


Fig. 4.9 MESFET's transfer characteristics

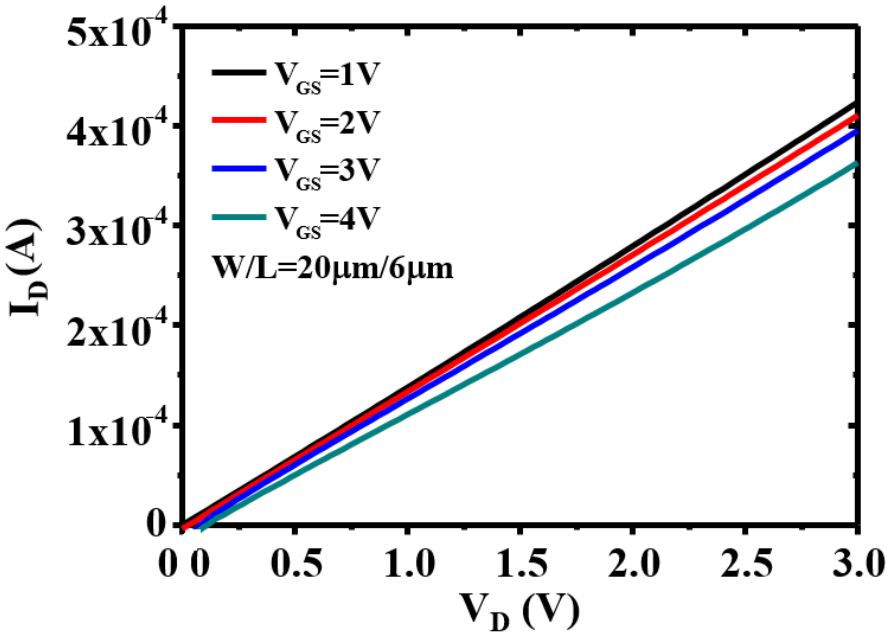


Fig. 4.10 MESFET's output characteristics

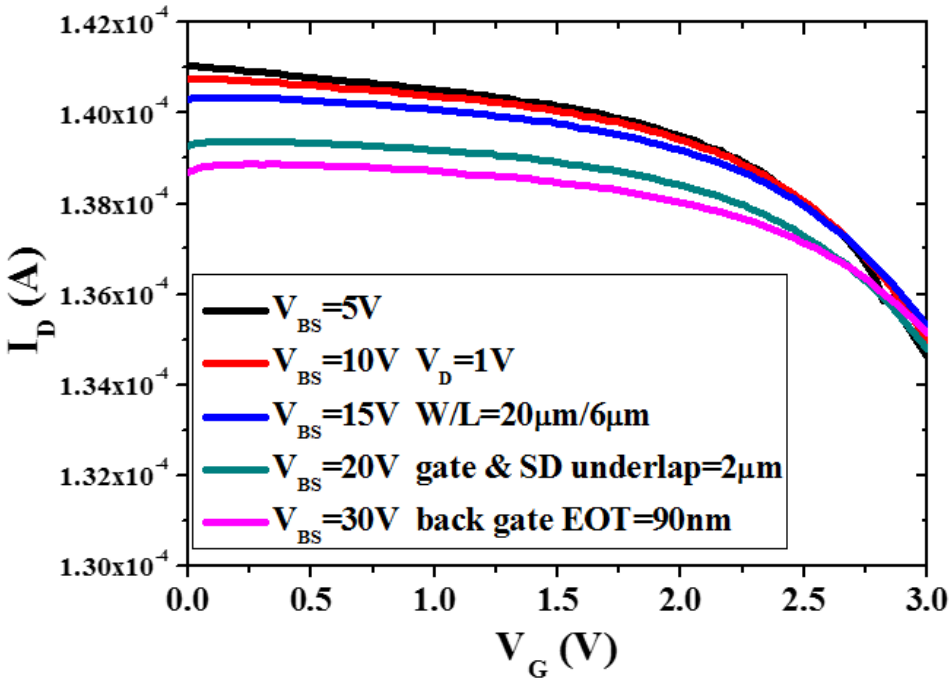


Fig. 4.11 MESFET's transfer characteristics with different back gate bias

4.5 Summary

In this chapter, WSe_2 is doped with Ta by using W:Ta co-sputtering process and synthesized by post selenization. The material characterization is used to verify the quality of the thin film after selenization. Typical Raman spectrum of WSe_2 is observed and only W-Se and Ta-Se bond signals were detected in XPS, which suggests that the substitutional process is complete during co-sputtering and selenization process. TLM structure is employed to check the sheet resistance and contact resistance and shows comparable results (R_c=11.4kΩ-μm and R_{sh}=17kΩ/sq) with recent literatures. It was then used as channel material for MESFET fabrication and shows very linear output characteristics. MESFET can not be completely turned off due to the high p-type doping concentration in channel region. High p-type doping concentration and good hole mobility were extracted out to be $6x10^{13}cm^{-2}$ and $16.5cm^2/Vs$ from transconductance method.

Chapter 5

Conclusion and Future Work

5.1 Conclusion

For FinFET (thin body transistors), the TCAD simulation tools are first calibrated to 14nm-node SOI and FinFET experimental data to capture the needed physics in short channel regime. Second, the graded channel concept by using different electron affinities materials in channel region is proposed to improve analog performance at 14nm-node. It changes the carrier density and velocity distribution along the channel and results in more uniform distributions compared to homojunction device. Therefore, it leads to higher g_m, R_{out} and intrinsic gain by improving the carrier transport and short channel effect in terms of DIBL compared to homojunction device.

For bulk device with deeply retrograde doping profile (DRCP), the physics of DRCP device is investigated by TCAD simulation and show the reason why it can deliver higher drain current, suppress the short channel effect in terms of lower drain-induced-barrier-lowering (DIBL) and lower V_{TH} variability compared to the halo device at L_G=29nm. It is also found out that it has higher g_m, R_{out} and intrinsic gain due to higher mobility and lower DIBL. The device performance of DRCP is also compared with bulk device, SOI and FinFET to show that DRCP can only deliver comparable performance as FinFET ans SOI down to 29nm regime.

For WSe_2 channel transistor, preparation, material characterization and electrical characterization of WSe_2 by using W:Ta co-sputtering doping technique and post selenization synthesis are discussed. WSe_2 was then used as channel materials for MESFET and TLM fabrication. The TLM measurement results show low sheet resistance and contact resistance

when contact with palladium and MESFET extraction results show high p-type doping concentration and good hole mobility.

5.2 Future Work

The followings are some possible directions for further investigations:

- **Experiment for graded channel device:** The graded channel concept can be experimentally implemented by SiGe epitaxial growth in FinFET. The Source/drain region of FinFET in 20nm-node is consist of SiGe wrap around silicon and it can be the source of the SiGe growth. Design and optimize the experiment can be investigated and compared with simulation results to verify the effectiveness of graded channel concept. Co-optimization of the graded channel along with the source/drain resistance reduction can also be investigated to provide more improvement on analog performance.
- **Lower p-type doping concentration of the WSe_2 film:** It was found out in our experiments that the p-type doping concentration in WSe_2 thin film doped by co-sputtering process is very high (N_A=6x$10^{13}$$cm^{-2}$) and MESFET can't be turned off completely. The fine tune of the co-sputtering process and post selenization to achieve lower p-type doping concentration is needed. In addition, design of experiment for locally doped WSe_2 is also desired to realize the enhancement mode FET.
- **Process integration of WSe_2 FET:** The on-current of WSe_2 channel MESFET is large (6μA/μm at V_D=1V and channel length=6μm) and comparable to other

literature but the gate modulation weak. Lower doping concentration of WSe_2 can improve gate modulation but other aspects like using different gate dielectric and surface treatments can also be investigated to lower the interface states and improves device performance.

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