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Offshoring in the Semiconductor Industry: A Historical Perspective

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Abstract:

Semiconductor design is a frequently-cited example of the new wave of offshoring and foreign-outsourcing of service sector jobs.[1] It is certainly a concern to U.S. design engineers themselves.[2]

In addition to the current wave of white-collar outsourcing, the industry also has a rich experience with offshoring of manufacturing activity. Semiconductor companies were among the first to invest in offshore facilities to manufacture goods for imports back to the U.S. A brief review of these earlier manufacturing experiences and their impact on the fortunes of the domestic industry and its workers can help to illuminate the current debates over offshoring in services.

Because meaningful data about the impact of the offshoring of chip design (and even manufacturing) are limited, we rely on a more qualitative analysis for our key points. We have conducted dozens of interviews with engineers and managers at numerous semiconductor and related companies in the United States, Asia, and Europe over the past six years. Our research also incorporates the rich store of publicly available information in trade journals and company reports.

This paper describes the two previous stages of offshoring semiconductor assembly jobs and of outsourcing semiconductor manufacturing and the impact they had on the U.S. semiconductor industry. We argue that the initial concern about losing domestic jobs in both stages turned out to be unfounded as the industry used the situation to its competitive advantage by becoming cost competitive (assembly stage) and by developing the fabless sector (manufacturing stage). We then analyze the on-going stage of offshoring design jobs, and compare this stage to the two that came before in order to explore the possible impact on domestic jobs and the U.S. semiconductor industry. We begin in section one with a brief description of the stages of semiconductor production and our analytical framework. Section two looks at the offshoring of assembly jobs, and section three analyzes the foreign outsourcing of manufacturing. Section four explores the offshoring of design jobs, and concludes with a discussion of what this means for the U.S.

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[1] See for example "The New Global Job Shift," Business Week, February 3, 2003, cover story and "Another Lure Of Outsourcing: Job Expertise," Wall Street Journal, April 12, 2004; Page B1.
[2] "2004 Salary Survey: It's an outsourced world, EEs acknowledge," EE Times, August 27, 2004.

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I. Introduction: The Industry and Analytical Framework

In order to understand the process of outsourcing of activities in the semiconductor industry, we begin by describing the stages of production.

The most important type of semiconductor, and the one which concerns us here, is the integrated circuit, or "chip," which is basically a network of tiny wires fabricated on a surface connecting transistors that switch on and off for processing data in binary code. The development and manufacturing of semiconductors involve three primary activities in the value chain: design, fabrication (front end), test and assembly (back end).

During design, the desired electronic circuits progress through a series of abstract to physical representations. During fabrication, the circuits of the chips are built up on the surface of a flat, round silicon wafer in successive layers Assembly is, typically, the process of cutting the wafer into individual chips (or die), which can number up to 1000, depending on die size, and packaging the delicate chip in a protective shell that includes connections to other components. The semiconductor industry has successively undergone phases of offshoring—first assembly, then fabrication, and now design.

The economic characteristics of each step of the process differ significantly. Design is skill intensive, and requires expensive EDA (electronic design automation) tools, which tend to be licensed per design engineer Fabrication required a huge fixed investment (currently on the order of $2 billion) to build a plant (called a fab) that holds a wide variety of expensive equipment and that meets extreme requirements of cleanliness. Assembly requires expensive test and assembly equipment, but the overall costs of plant and equipment are much lower than for the fab. Overall, worker skill requirements go up along the value chain.

Semiconductors can be cost-effective to offshore in any location with adequate transportation facilities because their very high value-to-weight ratio reduces the penalty for long hauls between factory and customer or between stages of production. However, equipment costs dominate labor costs, especially for fabrication, and this has limited the attractiveness of low-cost labor locations. Even the most labor-intensive activity, chip assembly, has become more automated over time. As discussed below, other costs, including those relating to land, taxes, and government regulations, often affect decisions to offshore.

The framework within which we will analyze the offshoring of the stages of the industry value chain relies on the concept of competitive advantage (Porter, 1985). A sustained advantage over rivals can be built on product (i.e., the intellectual property that defines functionality), price (i.e., the cost of production), or market attributes (i.e., new customers, customer service, brand reputation, and links to legacy products). These sources of competitive advantage provide the three principal reasons that firms offshore one of their activities: access to location-specific resources including engineering talent, cost reduction, and market development.

When a firm with some non-imitable advantage moves an activity offshore to reduce its costs or improve access to resources, it improves (barring cases where the move is mismanaged) its competitive position against its rivals. In an expanding market like that for chips, the firm will grow and will hire more workers, some of whom will be in the home country and some offshore.

However, some or all of the workers in the home country who were engaged in the activity that shifted offshore may lose their jobs, so that only the remaining home country workers benefit from the firm's move offshore, along with the consumers of the lower-price products (see, for example, Garner, 2004). In addition, both exports and imports are increasing with market growth and the net impact of trade on jobs must be considered (Groshen, et al., 2005).

Numerous firm-level investments in a foreign location may change the location in such a way that it presents a new set of opportunities that lead to a transformation of the industry. A foreign location that is initially little more than a source of lower costs, especially labor, might develop over time as a specialized supply base. The changes can increase the value of the location to the point that the industry will eventually restructure around the new distribution of skills, and offshoring becomes the preferred mode for this activity. We will discuss below how this occurred for semiconductor assembly, but it has also taken place in other industries, such as hard disk drives (McKendrick, et al., 2000).

II. Offshore Assembly: from offshoring to outsourcing

Assembly was the easiest stage of production to be moved offshore. It was functionally separate from the other stages of production even when performed in close proximity to fabrication. Furthermore, assembly began with a relatively high use of less-skilled direct labor.

During the 1980s, the US offshore companies switched to automation in response to a combination of increasingly intricate packaging requirements and higher equipment costs along with rising wages in some South-East Asian nations. As a result, the output per worker increased, and the typical plant still employs 1,000 or more workers. As of the mid-1990s, low-skilled workers made up about 80% of the staff of offshore assembly plants. The share of engineering and professional jobs was about 6%, and technicians made up another 13%.[3]

The move to offshore assembly led to a "hollowing out" of the US chip assembly sector, but kept the US chip industry cost-competitive as new rivals appeared in Europe and Japan. Over time, Asian suppliers appeared and took over a large portion of the business, so it went from offshoring to outsourcing, although most IDMs still own some assembly plants in Asia.

The main lesson from this period of offshoring is that giving up one part of the value chain (at least as far as domestic production is concerned) may be necessary to "save" the domestic industry. The second lesson is that the initial moves offshore can have unforeseen dynamic consequences such as the emergence of foreign suppliers who dominate the industry segment.

A. Offshoring, job loss, and competition

Because of their high value-to-weight ratio, semiconductors could profitably be fabricated in the United States, air-freighted to Asia for assembly, and then returned to the United States for final testing and shipment to the customer. This system allowed the U.S. companies to take advantage of the specialized skilled and semi-skilled labor in the United States for design, fabrication, and key managerial functions while tapping the lower cost unskilled labor, land, and taxes of Asia for assembly. Today, this trans-oceanic division of labor between fabrication and assembly still takes place. Final testing was often added to Asian assembly plants in the 1980s, which allows the finished chips to be shipped directly to customers from Asia, which is where a large share of the market is also located. From 1984 to 2004, the share of semiconductor sales in Asia, including Japan, has risen from 38 to 63% of the world total.[4]

The earliest offshore investment in semiconductor assembly was made in 1961 by Fairchild Semiconductor in Hong Kong for the assembly of discrete transistors. Over the next

[3] The Advanced Micro Devices chip assembly subsidiary in Penang, Malaysia employed 160 engineers and 380 technicians out of 2,900 workers ("Firm to make new microchips," The Star, May 25, 1996). This ratio is similar to that for the whole semiconductor-dominated Malaysian-American Electronic Industry group in 1994 as reported in their Annual Survey of 17 members over the preceding five years (MAEI, 1995).

[4] Calculated from Semiconductor Industry Association market statistics available at http://www.sia-online.org/pre_statistics.cfm.

fifteen years, this pioneering investment was followed by assembly investments by other companies in seven other economies of the region. By the mid-1970s, there were dozens of U.S.-owned assembly plants throughout the region employing about 1,000 workers each (Henderson, 1989: 51).

Developing economies in the Western hemisphere such as Mexico and El Salvador received assembly investments, but during the 1970s gradually receded from one-quarter to one-tenth of US re-imports in the face of political or social unrest, and East Asia made up the difference (Flamm, 1985: Table 3-7). The Asian countries offered plenty of low-skilled workers and stable governments that adopted pro-investment policies.

All large U.S. "merchant" (selling to other companies) chip firms invested in offshore assembly. The two primary "captive" (for internal use) producers, IBM and AT&T, initially kept their assembly in the United States and adopted a higher level of automation than the offshore plants (Flamm, 1985: 52). AT&T opened chip assembly plants in Singapore and Thailand in 1985. For at least one U.S. company, Philco, an attempt to automate in the U.S. ended badly because of the rapid obsolescence of the equipment (ibid.: 69).

Several factors contributed to the movement offshore. First, Japanese manufacturers, who automated their assembly lines, provided stiff competition for American producers in the consumer market (Henderson, 1989: 45). Automation was a more feasible strategy for the Japanese because of their relatively greater reliance on high-volume memory chips, which involve long production runs. U.S. companies produced a wider range of products which were less economical to automate (Flamm, 1985: 92). Also, the importance of the military, which had been the primary early adopter of semiconductors, was steadily replaced by the consumer electronics industry, with its attendant price pressures, during the 1960s (Henderson, 1989: 43). Furthermore, U.S. policy was permissive because tariffs were limited to the value added offshore, which in the case of assembly was a relatively small portion of the total – about 12% in the late 1970s (Flamm, 1985: Table 3-10).

By 1977, U.S. companies employed close to 100,000 workers in offshore assembly plants, compared to 114,000 domestic employees, of whom 64,000 were directly involved in production (Flamm, 1985: 91). The overseas expansion resulted in a decline in domestic assembly jobs. U.S. factories were closed during recessions, and new jobs added overseas during upturns. Job-loss data from the period of peak overseas expansion (1968-1972) aren't available; but from 1975 to 1982, 8,500 former chip assembly workers were certified for trade-adjustment assistance, and another 3,000 applied but were refused (Flamm, 1985: 96).

There was, however, an offsetting gain in consumer surplus from the low prices of the re-imported chips. Flamm (1985) estimates the welfare cost of repatriating assembly and making it profitable with tariff barriers to be about $1 billion for 1983, which can be thought of as an upper bound for the consumer surplus of the move offshore (p.96).

In terms of assembly, the U.S. chip industry "hollowed out." Flamm (1985) estimated that in 1978 around 80% of U.S. semiconductor production was assembled abroad (p.82). The figure is now probably above 95%, with most remaining U.S. facilities predominantly engaged in prototyping and military jobs.

History suggests that the move offshore helped keep U.S. chip firms competitive with the new rivals from Asia, and this was important for protecting the remaining jobs in the industry. When Flamm published his landmark study, the U.S. chip industry was in a period of decline, but in spite of the move to offshore assembly rather than because of it. When the industry sought U.S. government help, the fabrication stage of production was where the U.S. capability was seen as deficient, and fabrication was the focus of the joint public-private research consortium, SEMATCH, launched in 1986.

Thus chip assembly provides an example where the offshoring of one part of the value chain to reduce costs was important for maintaining competitive advantage against international rivals, albeit at the expense of specific jobs in the short run.

B. Offshoring and the appearance of new suppliers

Offshore chip assembly offers an additional lesson that is worth noting briefly, namely that offshoring involves technology diffusion to foreign companies.

In countries where entrepreneurial conditions are favorable, foreign investment stimulates the emergence of local companies. In the case of chip assembly, this has meant the emergence of a number of contract assemblers that complement and strengthen the US semiconductor industry.

The entrance of companies from industrializing economies into the chip assembly business has not brought about the exit of U.S. companies from the activity. Many U.S.-owned offshore assembly plants from the industry's early days are still in operation, and new ones are still being built, such as Intel's assembly plants in China.[5]

Beginning in the late 1960s, local Asian firms started offering contract chip assembly services to the U.S.-owned plants. Today, roughly one quarter of all chip assembly is outsourced. The top 10 assembly contractors, with about 60% of total contracting revenue in 2003, are all Asia-based, which reflects a strong link to the initial locational choices of U.S. firms.[6]

These Asian companies have become important technology partners for U.S. producers. The requirements for chip packages have become quite sophisticated with the growing complexity of chips, the need to fit size-sensitive products like mobile phones, and the increasing number of package-induced electrical problems. The engineers at the leading Asian assembly companies are able to participate with the chip designers at an early stage to avoid problems with the final product.[7] The availability of multiple Asian suppliers allows chip companies access to the large array of package types that are now available, since few U.S. firms have the scale to supply internally all types that they need.

III. Outsourced Fabrication: from foreign outsourcing to industry restructuring

The case of wafer fabrication is very different from that of assembly because it is a story of foreign outsourcing without an earlier period of offshore investing. Fabrication was offshored via investment in only a few cases, and primarily for market access in Japan and Europe, where trade barriers made U.S. exports uneconomical (Henderson, 1989: 45). Cost reduction via offshore investments was not a feasible strategy because fabrication is so capital-intensive that labor typically accounts for 16% of costs (including depreciation) in U.S. fabs producing 200mm wafers, and less than 10% in the newer 300mm fabs, which undercuts the major labor cost advantage of most industrializing countries.[8]

In a survey of industry executives, Leachman and Leachman (2004, p.226) found that the top five reasons, rated very close together, for fab site selection were "Tax advantages," "Supply of engineering and technical talent," "Quality of water supply and reliability of utilities," "Proximity to existing company facilities," and "Environmental permitting process and/or other regulations." This multiplicity of concerns surrounding such a major investment accounts for the relatively few cases of U.S.-built fabs in industrializing countries, even with the rich subsidies that have been offered by countries like Singapore.

Instead, offshore fabrication of U.S.-designed chips occurs mainly on an outsourced basis, to suppliers that were created as part of focused government programs in industrializing countries. These suppliers, known in the industry as "foundries," manufacture chips to the designs

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[5] "Intel to build second IC assembly plant in Chengdu," EE Times, March 23, 2005.
[6] "Outsourcing for IC-packaging continues to climb," Silicon Strategies, May 7, 2004.
[7] See "How Amkor's packaging proficiency helped Cisco's switches," Electronics Design Chain, Fall 2004, for a detailed case study.
[8] Authors' calculations based on data in Appendix 2 of Howell, et al, 2003. Labor costs for 200mm fabs are 8% in Taiwan and 3% in China.

of other companies and sell no chips of their own design. Although some integrated companies, most notably IBM, offer foundry services, the pure-play companies are the most important source of such services.

The foundry model was initially ridiculed by industry executives, most famously by Jerry Sanders, then-CEO of Advanced Micro Devices, who is reputed to have dismissed the phenomenon of outsourced fabrication with the claim that "Real men have fabs."[9] The foundry model has, however, proved to be extremely successful, and its technology level is now close to the industry "bleeding edge" of companies such as Intel and IBM.

The dedicated foundry model originated in Taiwan in 1987, when the government brought together investors, licensed dated production technology from the United States, and attracted Taiwanese engineers and managers with experience in the U.S. chip industry. The initial foundry, Taiwan Semiconductor Manufacturing Corporation (TSMC), remains the largest in an increasingly crowded field (Table 1). TSMC was founded by Morris Chang, a Chinese-born, MIT-educated executive with 25 years' experience at Texas Instruments who moved to Taiwan in 1985.

TSMC's chief rival is an older Taiwanese government-backed company, United Microelectronics (UMC), which sold off its design activities in the late 1990s and adopted the foundry model. The third biggest foundry, Chartered Semiconductor, is located in Singapore and is part-owned by the government.

The newest entrant, China-based Semiconductor Manufacturing International Corporation (SMIC), was founded in 2000 by Richard Chang, a Taiwanese expatriate with experience in Taiwan's foundry business following a U.S. graduate education and twenty years' experience at Texas Instruments. SMIC's investors include international venture capitalists and Chinese government entities. SMIC has successfully attracted a range of technology partners and customers, primarily from the United States, attracted Taiwanese engineers with foundry experience, from TSMC[10] and successfully listed its shares on the New York Stock Exchange in 2004.

The technology level of China's fabrication capability is theoretically limited by the Wassenaar Arrangement of 1996, by which more than thirty countries agreed to restrict exports of dual-use technologies that might undermine international security. Interpretation and enforcement, however, are left up to individual member states, and most countries with chip equipment industries other than the United States have been unwilling to curb exports of advanced chip-making equipment to China.[11] In 2003, the U.S. government issued SMIC a special license specifying that it does not make chips for military use, which allowed U.S. equipment makers to compete on a more even basis with their Japanese and European rivals.[12]

TABLE 1: Top Five Pure-Play* Foundries, 2004

Company	Country	2004 Revenue (US$ millions)	2004 Share of Total
TSMC	Taiwan	$7,648	46%
UMC	Taiwan	$3,900	23%
Chartered	Singapore	$1,103	7%
SMIC	China	$ 975	6%
Vanguard	Taiwan	$ 474	3%

[9] Although the phrase is universally attributed to Mr. Sanders, the exact date and wording is obscure.
[10] "TSMC Sues SMIC," Electronic News, December 22, 2003.
[11] "Chip-equipment export rules to China are unclear and 'ineffective'," Semiconductor Business News, February 15, 2002.
[12] "SMIC obtains special license for advanced U.S. fab gear," Silicon Strategies, September 30, 2003.

Source: IC Insights, reported in "China gains in 2004 pure-play foundry rankings," EE Times, March 28, 2005.
* "Pure-play" foundries are those dedicated to foundry services and exclude companies that manufacture their own chips as well as offer foundry services.

At the time TSMC was created, a handful of U.S. chip companies, such as Xilinx and Chips & Technologies, were already outsourcing all of their manufacturing, primarily to integrated Japanese manufacturers. This arrangement entailed certain risks over access to capacity and control of intellectual property.

The advent of government-funded manufacturing in Asia raised concerns about a potential loss of manufacturing jobs in the United States, especially since the U.S. semiconductor industry had seen its fortunes slip during the 1980s as U.S. DRAM makers lost market dominance to Japanese companies. However the foundries contributed to the resurgence of the U.S. chip industry, since they facilitated the blossoming of design-only (or "fabless") chip companies, especially in California, during the 1990s (Macher, et al., 1998).

Over the last ten years, fabless revenue (C.A.G.R. of 20%) has been growing faster then the semiconductor industry as a whole (C.A.G.R. of 7%); worldwide fabless revenue was $20.6 billion in 2003. Of the top thirty fabless firms that year, twenty were U.S.-based and had a combined revenue of $13.5 billion. The next most important location for fabless companies is Taiwan, where six of the top 30 firms (combined revenue of $2.8 billion) of 2003 are located.[13] Table 2 shows the top 10 fabless firms of 2004.

TABLE 2: Top 10 Fabless Companies, 2004
(Total Revenue: $33 billion)

Company (Location)	2004 Revenue (US $ millions)
Qualcomm (Calif.)	$3,224.0
Broadcom (Calif.)	$2,400.6
ATI Technologies (Canada)	$2,140.9
Nvidia (Calif.)	$2,010.0
SanDisk (Calif.)	$1,777.1
Xilinx (Calif.)	$1,588.7
MediaTek (Taiwan)	$1,252.5
Marvell Semiconductor (Calif.)	$1,224.6
Altera (Calif.)	$1,016.4
Conexant (Calif.)	$ 914.6

Source: Fabless Semiconductor Association, cited in "Worldwide Fabless Revenue Grew 27% in 2004, FSA Revealed," Nikkei Electronics Asia Online, March 18, 2005.

In addition to supporting the increasingly important fabless sector, the Asian foundries are also permitting integrated firms, from smaller players all the way up the world's third-largest chip firm, Texas Instruments, to hedge the enormous risk of building new factories by using the foundries for buffer capacity and even for fabricating leading-edge chips that have a short product life or uncertain volume. Because of the enormous depreciation expense of fab ownership, full utilization of capacity is critical. Fab-owning companies (called integrated device manufacturers, or IDMs) can keep their own fabs fully booked and shift excess demand to the foundries. The

[13] Data from IC Insights reported in "SanDisk, Silicon Labs leap in 2003 fabless rankings," Silicon Strategies, March 18, 2004.

foundries adjust their prices as their capacity utilization varies. IDMs began shifting business to foundries in the mid-1990s and in recent years have accounted for approximately 45% of foundry revenue.[14] Looked at another way, 20 to 25% of the value of the semiconductor industry is being manufactured on an outsourced basis.[15]

Although the outsourcing trend represents a shift of manufacturing to Asia, it seems unlikely that the U.S. semiconductor industry will ever entirely cease domestic fabrication. At the leading edge, companies like Intel, IBM, and Texas Instruments derive advantage from implementing advanced process technologies for their flagship products at the earliest possible time. Companies like Freescale (formerly Motorola) and Micron benefit from running non-standard processes. In all these cases, fab ownership affords closer interaction between the design and manufacturing functions and helps to ensure the protection of key trade secrets. Nevertheless, as the foundries add capacity and smaller fab-owning firms decline to invest in new plants, the number of fab-owning firms will likely decline.

There is a limit to the eventual size of the foundry sector. For example, Intel will continue internal fabrication of its PC microprocessors because they depend on leading-edge process technology. Samsung, the leading memory maker, will continue internal fabrication of its memory chips, since they require high volume, low cost production runs with short product life cycles. Intel and Samsung, the top two semiconductor companies worldwide, accounted for 21.4% of sales in 2004.[16] The major category of chips that are manufactured by foundries are logic chips, including a range of general-purpose and application-specific products, and mixed-signal chips, which primarily use standard processes. All told, outsourced manufacturing will probably never exceed 50% of the semiconductor industry.[17]

Another way to look at semiconductor fabrication in the United States is to consider where fab investment takes place, and the data suggest a growing shift away from U.S. investment in domestic fabs. Our historical data come from our colleagues Leachman and Leachman (2004). Table 3 shows fab capacity in terms of where it's located in 1980, 1990, and 2001.[18] The shift of capacity from Japan and the United States to the rest of Asia (primarily South Korea and Taiwan) is striking. Japan and the United States accounted for 80% of fab capacity in 1980, but only 49% of capacity in 2001.

TABLE 3: Regional Location and Ownership of Worldwide Fabrication Capacity

(For each year, capacity location is shown on top and capacity ownership is shown beneath it in parentheses.)

Year	Asia ex-Japan	Europe/ Middle East	Japan	North America
1980	4% (3%)	16% (15%)	38% (37%)	42% (44%)
1990	12% (12%)	13% (9%)	45% (45%)	30% (36%)
2001	38% (39%)	13% (8%)	20% (24%)	29% (38%)

Source: Leachman and Leachman (2004), Tables 8.2, 8.4

[14] Data reported by Semico Research Corp, reported in "System houses remain weak link for silicon foundries," Silicon Strategies, May 11, 2004.
[15] Authors' calculations, assuming that foundry revenue represents about one-third the value of the final chip price.
[16] Gartner Dataquest data reported in "Gartner differs with rivals in top-10 chip rankings," EE Times, March 23, 2005.
[17] See "More Changes Ahead for Foundries, Industry," Electronic News, December 4, 2003, for a similar analysis.
[18] Because older fabs use a range of wafer sizes and linewidths, the underlying data have been normalized using a capacity metric based on the number of functions, where a function is one memory bit or one logic gate.

Note: The ownership row total for 2001 adds to more than 100 because jointly owned capacity was credited in full to all owners.

However if we look at the same data in terms of region of ownership (shown in parenthesis), we see that although the rise of capacity owned by companies in Asia ex-Japan mirrors the rise of location capacity, the decline of capacity owned by U.S. companies is less severe than the fall in capacity located in the U.S. Although only 29% of fab capacity in 2001 was in the United States, U.S. companies had ownership stakes in almost 40% of global capacity.

Because so many fabs owned by companies in one region are located in another, these data do not directly answer the question of how much U.S.-owned capacity is located outside the United States. Rob Leachman generously helped us to make this calculation.[19] In 2001, approximately one-third of U.S.-owned capacity was located offshore, primarily Japan and Europe, which reflects the rise of joint ventures to share risk as the cost of fabs increased (see Table 4). Conversely, about 22% of the fab capacity located in North America was owned by companies based in other regions.

TABLE 4: Distribution of North-American-Owned Fab Capacity, 2001

North America	65.4%
Europe/Middle East	18.6%
Japan	13.0%
Asia ex-Japan	3.0%

Source: Calculations courtesy of Rob Leachman.

The trend toward Asian manufacturing is continuing. The largest, most efficient fabs today utilize 300mm (12-inch) diameter wafers. Taiwan has one of the largest concentrations of these mega-factories, which are needed by the foundries to keep their unit costs low (see Table 5). Leading U.S. firms, such as Intel and Texas Instruments, were early adopters of the 300mm technology, but are slowing down their commitment to new fabs, in part because of their ability to turn to foundries for buffer capacity. SMIC's newest fab constitutes China's entry in the 300mm list.

The 300mm capacity being equipped or under construction equals 520,000 wafers per month, which is being added to existing capacity of 690,000 wafers per month, and each fab will require annual revenues of $5-$7 billion to be profitable.[20] As has occurred in the past in the semiconductor industry, the new fabs may result in overcapacity by the time they come online.

[19] The Leachman data do not include ownership shares for jointly-owned fabs. We divided such fabs by the number of regions (2 or 3) involved in ownership to estimate the U.S. share. As much as 10% of U.S.-owned capacity was in joint venture fabs in 2001, but those fabs were spread across all regions, so our estimation error is not likely to be more than 1 or 2 % up or down from the figures in the table.

[20] "Fab Capacity: When, Where, How Much, Too Much?" Semiconductor International, October 1, 2004.

TABLE 5: 300mm Fabs Producing, Equipping, or Under Construction, mid-2004

Taiwan	33%
U.S.	20%
Europe	14%
Japan	11%
SE Asia	9%
S.Korea	8%
China	5%

Source: Strategic Marketing Associates, reported in "Outlook on the Global Fabless Semiconductor Industry", Fabless Semiconductor Association presentation at IC Industry Development Forum, Shanghai, April 22, 2004.

Although the advent of outsourced manufacturing in Asia did not represent a transfer of capacity that entailed a shutdown of U.S. facilities, it has very probably reduced the number of facilities that would otherwise have been built here, which represents the loss of a number of potentially high-skilled jobs. TSMC, which accounts for about half the pure-play foundry market, currently operates one 300mm and five 200mm fabs in Taiwan (plus one in Washington state).

We don't have detailed staffing data for 300mm fabs, but we have data on earlier-generation fabs gathered in the mid-90s by the Berkeley Competitive Semiconductor Manufacturing (CSM) Program. The data describe the average employment distribution at a sample of fabs running 150mm and 200mm wafers in four countries.[21]

As wafer size increases, output rises for a given level of wafer throughput, and both materials handling and information systems become more automated. Automation changes the composition of the workforce as the need increases for engineers and declines for operators. In the CSM data, engineers increase from 15% to 24% of the total workforce between 150mm- and 200mm-generation plants, with a corresponding decline in operators from 73% to 62% (see Table 6) even as the overall employment level of the fab stayed approximately the same at about 750 workers.

TABLE 6: Work Force Composition
(Mean Headcount in Matched 150mm and 200mm Fabs)

	150mm	200mm
Operators	547 (73%)	470 (62%)
Technicians	91 (12%)	107 (14%)
Engineers	114 (15%)	181 (24%)
Total	752	758

Source: Brown and Campbell, 2001.

The initial pay of technicians and engineers is over one-third higher in the high-tech 200mm fabs, and their pay premium compared to operators has increased (see Table 7). If we look at the returns to experience, which is proxied by the maximum pay, we see that experienced technicians and operators have the same pay improvement in the high-tech fab as do the new hires, and the technicians' improvement in pay relative to operators holds for experienced as well as newly hired workers. However the experienced engineers in the high-tech fabs do not fare as well as the new hires. In fact, the experienced engineers are losing out over time as their mean

[21] Twenty-three fabs in four countries were part of the CSM survey. For this table, the 150mm wafers fabs were matched to the 200mm wafers fabs by company, so that the company human resource policies are comparable between the two groups, which reduced the sample to fourteen.

maximum salary is actually lower in the 200mm fabs. In interviews, we learned that fabs liked having young engineers with knowledge of new technology and they did not worry about losing older engineers. Over time, consequently, fabs were willing to increase wages of new hires without raising the wages of experienced engineers. Rapidly changing technology plus an ample supply of new hires and low turnover allowed the companies to flatten engineers' career ladders with no adverse consequences.

The shifting of jobs from operators to engineers in the transition from 150mm to 200mm fabs results in the growth of engineering jobs paying from $29,000 to $56,000 per year and the decline in operator jobs paying $14,000 to $37,000 per year (see Table 7)..

TABLE 7: Work Force Compensation
(Mean Wage or Salary in Matched 150mm and 200mm Fabs)

	150mm		200mm	
	Initial pay	Maximum pay	Initial pay	Maximum pay
Operators (hourly)	$5.88	$15.47	$7.12	$18.44
Technicians (hourly)	$6.68	$11.50	$9.12	$15.83
Engineers (monthly)	$1,785	$5,019	$2,381	$4,689

Source: Brown and Campbell, 2001.

We do not have comparable data for the 300mm fab, which typically costs $2-3 billion (depending upon the size), has 100% automation of materials handling and wafer processing, and fabricates a wafer that is 2.25 times larger than the 200mm wafer. Because these new 300mm fabs are processing advanced circuits, such as 90nm processes, the amount of inspection, metrology steps, and in-line engineering-related activities are significantly higher than their older 200mm counterparts for the same wafer throughput. As a result, most of the 300mm worker savings achieved with the automation of materials handling, often cited to be approximately 30% less labor input, is now being re-applied to the new engineering tasks, which are much higher value added, more intellectually challenging, and include troubleshooting. Therefore the number of workers has not been reduced as a result of the advanced factory automation; instead there has been a shift in task composition. The percentage of workers with higher engineering and technical problem-solving skills has greatly increased, while the percentage of workers needed for wafer movement and equipment starting and stopping has greatly decreased. However the proportion of engineers has not increased. The overall the cost per chip in the 300mm fab is more than 30 percent lower compared to the 200mm fab.[22]

So what is the net employment impact of fabrication offshoring and outsoucing? According to the Semiconductor Industry Association, U.S. chip firms employed 103,000 engineers in 2003, of which 30% were located offshore. The share of offshore employment had not grown since 1998, and in fact fell during the Internet/telecom bubble before returning to 30%.[23]

[22] Personal communication, April 2005.
[23] Data are from the annual SIA Semiconductor Workforce Strategy Committee Survey, referenced in "SIA Workforce Strategy Overview," a presentation by David R. Ferrell to the Electrical and Computer Engineering Department Heads Association annual meeting, March 22, 2005. Accessible as of April 21, 2005 at http://www.ecedha.org/Temp04-05/agenda.html.

As a back of the envelope calculation, we estimate that if all foundry production were based in the United States instead of Asia, it might add 11,000 jobs, of which some 2,600 would be highly-paid engineers.[24] As a point of comparison, the Fabless Semiconductor Association reported that publicly-traded fabless companies in North America employ approximately 45,000 workers as of December 2004.[25] A review of company information suggests that more than half of these are software or hardware engineers, although an unknown share of them are located offshore.

To summarize this section, the availability of outsourced fabrication in Asia played to the U.S. strength in design by facilitating the emergence of the fabless chip industry. The Asian foundries are probably also part of a long-run reduction of U.S. chip manufacturing, but the loss of U.S. manufacturing jobs has been gradual. Even in chip fabrication, the workforce includes fewer operators and more engineers. Most importantly, the loss of chip manufacturing jobs to foundries has probably been offset to some extent by the increase in design jobs. The reliance of the U.S. semiconductor industry on high-end design jobs is one of the reasons that chip design, the latest frontier for offshoring, to which we now turn, may be a cause for greater concern.

IV. Offshore Design

The picture for offshore and outsourced design by U.S. semiconductor companies is still taking shape. Although some design has been done offshore since at least the 1970s, the pace of offshoring has noticeably increased in the last few years, and there is growing evidence that the U.S. market for chip design engineers has been adversely affected.

A. The economics of chip design

Chip design is highly skill-intensive, since it employs only college-trained engineers. A couple of medium-size chip designs will employ as many electrical engineers as a fab for a year or more. The design of a complex chip like Intel's Pentium 4, with 42 million transistors on a 180nm linewidth process, engaged hundreds of engineers for the full length of the five-year project.[26] In practice, design teams can also be as small as a few engineers, and project duration varies from months to years. Team size depends on the complexity of the project, the speed with which it must be completed, and the resources available.

The design of an integrated circuit is a hierarchical procedure that passes through identifiable stages. With some simplification, they are specification, logic design, and physical design. Once the part has reached the prototype stage, it needs to be validated in a hardware simulation of a complete system. Parallel with this process, the design must be repeatedly verified, and the software that will be part of the chip, and that will run on it, needs to be written.

The highest-level design stage is the general specification for how the chip as a whole will behave within the system of which it's a part. This is a high-value-added function that applies the company's market knowledge and intellectual property in deciding what feature set will be most profitable.

The next stage, logic design (sometimes called "front-end"), uses symbolic abstractions to describe how signals will be processed within the chip, first at the register level, then at the gate level.

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[24] TSMC, which accounts for about half the foundry industry, has one 150mm, one 300mm, and five-and-a-half 200mm fabs outside the United States. These fabs probably have different rated capacities, but we can approximate employment by calculating 750 workers per plant, which works out to 5,625. Doubling that to approximate the entire foundry sector brings us to 11,250.

[25] FSA "Global Fabless Fundings and Financials Report, Q4 2004".

[26] "Comms held Pentium 4 team together," EE Times, November 1, 2000.

The final step, physical design (or "back end"), involves the translation of the abstract version into a map of actual wires and devices interconnecting across multiple layers on the silicon surface.

Design automation includes both the use of EDA tools by engineers in their designs and the actual automation of specific parts of the design with less engineering input, especially at the later stages of mainstream digital designs.

Table 8 shows the change in the effort required at each stage of design over succeeding generations of process technology, from 350 nanometer linewidths, first introduced in the mid-1990s, to 130nm, which entered volume production in 2003. The underlying project is assumed to be a digital logic design, the industry's typical product. Other types of design, such as analog or memory chips, require different engineering inputs.

TABLE 8: Engineer Hours to Design 1 Million Logic Transistors

	350nm	250nm	180nm	130nm	Change from 350nm to 130nm
Specification	23.0	29.8	91.4	271.6	1081%
Logic Design	714.2	738.4	756.4	837.7	17%
Physical Design	311.0	357.2	391.7	473.5	52%
Validation	103.7	127.6	164.5	197.4	90%
Software	378.4	672.4	985.7	1798.3	375%
Total	**1530.3**	**1925.4**	**2389.7**	**3578.5**	**134%**

Source: International Business Strategies (2002)

Note: The average number of transistors in a typical logic design increases by a factor of about two with each reduction in linewidth, so table normalizes the hours required for 1 million transistors at each generation.

The biggest changes involve the importance of software in the design process. Although software is typically not considered part of chip design as such (and software engineers are not included in counts of chip designers below), software expertise is increasingly important for the competitive advantage of semiconductor firms (Linden, et al, 2004). Chips are increasingly integrated to system-level complexity because of the size, reliability, and other advantages this brings. This greater integration means that the system software must be generated in parallel with the system-level chip for reasons of coherence and, especially, time-to-market. It is this need to plan carefully for the hardware-software co-design that has caused the specification portion of chip designs to explode by 1081% over the last four technology generations.

Similarly, the software effort itself has increased by 375%. According to one software executive, a typical chip in 1995 went into a stand-alone product and required 100,000 lines of code. In 2002, a major chip for a networked programmable product requires a million lines of code.[27]

It is also the software on top of the greater complexity of chips themselves that has caused validation hours to grow by 90% for each million transistors.

By comparison, the growth levels for the actual design engineering jobs of logic and physical design for each million transistors are a relatively modest 17 and 52%, respectively. This is largely because, as chips have gotten more complex, the process of chip design has become more automated (Hemani, 2004). The number of transistors that can be fabricated on a given area

[27] Jerry Fiddler, chairman of Wind River Systems, cited in "Keynoter says chip value is in its intellectual property," EE Times, June 14, 2002.

of silicon has doubled every 18 months for roughly 40 years, a phenomenon known as "Moore's Law," after Gordon Moore, one of the founders of Intel. In the early 1960s, digital ICs contained fewer than 50 transistors (Borrus, 1988: 75). The industry can now place some 100 million transistors on a chip, and Intel predicted a billion-transistor processor by 2007.[28]

The automation that enables the design of today's complex chips has evolved in parallel with the rise in complexity. At the beginning of the industry, designs were hand-drawn and hand-transferred to a template that was used to make the actual circuit. In the 1970s, the later stages of the process were computerized, and in the 1980s they were automated.

The introduction of automation, along with the advent of high-bandwidth telecommunications, created the ability of chip companies to subdivide the design process across multiple locations.

These advances pertain primarily to digital designs, i.e., those that work on binary streams of data. Designs that utilize all, or mostly, analog circuits, which process continuous signals such as sound waves, are done with a variety of EDA tools, but are not easily automated and require more experienced designers with specific training.

We now consider offshoring and outsourcing in turn.

B. Offshore design

The primary reasons for opening offshore design centers are the need for closer contact with customers, access to specialized skilled labor, and cost reduction.

Most early offshore design investments by U.S. companies through the 1970s were market-driven and limited to Japan and Western Europe (Henderson, 1989: 48). By the mid-1980s, a handful of offshore design investments had been made in Hong Kong, Taiwan, Singapore, which are the more advanced economies of East Asia outside Japan (ibid.: Figure 4.2). These design centers were dedicated to adapting existing chips to local market needs (ibid.: 58).

The prime example of the market access motivation for offshore investment is the "application-specific" IC (ASIC), a logic chip designed for a specific customer. U.S.-based ASIC producers like IBM and LSI Logic have established design centers in all major markets of Europe and Asia to facilitate the interaction of their engineers with their customers. In this case, globalization of design is primarily driven by market access. These companies also maintain other offshore design centers that develop the "cells" or building blocks that are later combined in various ways at the customer service centers.

Specialized skills are another reason that U.S. semiconductor companies invest overseas. Britain, for example, has developed expertise in consumer multimedia, and Scandinavian countries are noted for their skills in wireless network technology. These specialized skill bases are often accessed by acquisition of an existing company that continues as a subsidiary. Examples are easy to find. In 2000, Broadcom acquired Element 14, a British fabless company with 68 employees specializing in central office ADSL technology that became Broadcom UK Ltd.[29] In 2001, Agilent acquired Sirius, a Belgian designer of cellular chips for the CDMA standard with 19 employees, and made it a research and design center for next-generation cellular technology.[30] In 2005, Intel acquired Oplus, a successful maker of chips for digital television with 100 workers and that will remain an independent subsidiary.[31]

As was true of fabrication, design offshoring works both ways, and many foreign companies maintain a Silicon Valley or other U.S. design center to take advantage of the high skills and productivity available here as well as have access to U.S. knowledge networks. Philips

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[28] "Intel readies road map for billion-transistor processors," EE Times, January 4, 2002.
[29] "Broadcom acquires Element 14 for $600 million, enters ADSL chip market," Semiconductor Business News, October 4, 2000.
[30] "Agilent to buy Belgium's Sirius to offer new CDMA chip solutions," Semiconductor Business News, May 21, 2001.
[31] "Intel buys into consumer sector with Oplus acquisition," Silicon Strategies, February 24, 2005.

of the Netherlands, for example, bought VLSI Technology, a major ASIC company with over 2,000 employees (about one-third of whom were fab workers), in 1999 for nearly $1 billion.[32] Hitachi Semiconductor has a semiconductor design group several hundred strong.[33] Toshiba has a network of seven ASIC design centers around the United States.[34] Even foreign start-ups may need to have a U.S. design team to work with U.S. customers or to access leading-edge analog design skills.

The category of design offshoring that is perhaps growing the fastest – or at least getting the most attention – is cost reduction. Larger U.S. firms typically establish multiple U.S. design centers before looking offshore. Although some U.S. locations have average engineering salaries that are up to 20% lower than salaries in the Silicon Valley, these salaries are still much higher than salaries in India and elsewhere, as we discuss below.[35] The prospects for cost reduction offshore are better than ever because of changes in the last 20 years that have seen high-bandwidth infrastructure extended around the globe and the economic liberalization of large economic areas in Eastern Europe, and especially Asia (Ernst, 2004).

Dividing chip designs across locations presents a number of managerial challenges, as we have learned from interviews and press reports. The sacrifice of face-to-face interaction between different parts of the design team can adversely affect productivity, and distance makes it harder to evaluate and reward individual contributions to team performance. Task assignments must be more carefully codified for offshore teams than for in-house engineers, and managers will need to travel periodically between locations. When the separation is across borders, there are also cultural differences that can make communication less effective. An Intel engineer was reported to say that cultural differences were the single biggest problem in managing design teams between California and Israel,[36] and this separation did not include any language differences.

Cost-driven offshoring includes other costs that partially offset the difference in salaries, especially during the early stages of establishing an offshore design center. One that is often mentioned is the lower quality and productivity of inexperienced engineers. This raises monitoring costs, and offshore engineers may also require a longer training period than a U.S. team would need. Additional controls may also be needed to protect key intellectual property. According to a venture capitalist, the actual savings from going offshore is more likely to be 25 to 50% rather than the 80 to 90% suggested by a simple salary comparison.[37]

Design offshoring can also face national security barriers. For example, the U.S. government placed limits on the export of advanced encryption technology. Communications chips that employ such technology are difficult to design offshore. Either the chip design must be compartmentalized, with the encryption block designed only in the United States, or government approval, subject to possible delays, must be obtained in advance.[38]

Yet despite these pitfalls, the amount of offshore design has noticeably expanded over the last decade. Some companies value the opportunity to design on a 24-hour cycle because of the enormous pressure to reach the market ahead of, or no later than, competitors. One established U.S. chip company described a rolling cycle between design centers in the United States, Europe, and India.[39] More common is the bi-national arrangement used by a Silicon Valley start-up that had all of its design beyond the initial specification done by a China subsidiary established only months after the head office was set up. Ten executives in the head office had to train the mostly

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[32] "Philips to acquire VLSI Technology for $953 million," Semiconductor Business News, May 3, 1999.
[33] "Hitachi Forms North America Semiconductor Systems Solutions Unit," Hitachi Press Release, September 2, 1998.
[34] "Toshiba Expands Soc Design Support Network With Opening Of San Diego Design Center," Toshiba Press Release, November 26, 2002.
[35] "Mean wages edge closer to six-figure mark," EE Times, August 25, 2004.
[36] "Global chip design raises promises and challenges," EE Times, January 11, 1999.
[37] Interview, May 2004.
[38] Interview, December 2004.
[39] Interview, April 1998.

inexperienced staff in Beijing, which was about 30-strong.[40] The Silicon Valley staff would review Beijing's work from the previous day then spend up to three hours on the phone (starting around 5pm California time) providing feedback and reviewing assignments for that day in Beijing. In a single-location firm, this work-feedback cycle would take two days.

Venture capitalists have reportedly begun to require start-ups to include some offshoring or outsourcing in their business plans in order to better leverage their resources. A typical comment is, "We don't fund chip designs that don't outsource to India. If you rely on Indian contractors for the things they do well, you can get a chip out for under $10 million. If you don't, you can't, and you won't be competitive. It's that simple."[41] PortalPlayer, the company behind the key multimedia chip in Apple's iPod, is a recent example of a successful start-up that set up an Indian software and chip design subsidiary within a few months of its founding in 1999.[42]

We will discuss offshore subsidiaries further below.

C. Outsourced design

Low-cost design engineers are also available through outsourcing. All parts of a design, including the whole procedure from specification to finished chips, can be outsourced. In addition to the traditional work-to-order model, companies can also license standardized portions (e.g., a USB interface) of a system-level chip designed at the logic or physical level to save time. These reusable modules are known in the industry as "cores" or "IP blocks" (Linden and Somaya, 2003).

The easiest part of chip design to outsource is physical design because it is a relatively standardized task. It is also the least sensitive part of design in terms of revealing the customer's intellectual property. However for designs requiring leading-edge process technology, layout has become much less straightforward because of the sensitivity of the atomic-scale wiring. In such a case, physical design is likely to be outsourced only by small and medium companies that lack the resources to develop the necessary expertise in-house. On the other hand, we interviewed one start-up whose initial design was so complex that outsourcing any parts wasn't an option.[43] Needless to say, the company attracted an above-average level of funding to accomplish this design.

Another factor influencing outsourcing by small companies is the relatively large fixed cost of EDA tools, which are typically licensed per engineer. One consultant estimated that the minimum annual software expense for a small company is $10 million (IBS, 2002). For the industry as a whole, EDA expense runs close to 1% of revenue, which would translate in this case to $1 billion, which is a level that only the nine largest fabless companies achieved in 2004. The high cost of EDA tools makes it hard for a start-up chip company to enter the market, since the average size of publicly announced rounds of venture capital funding for fabless companies in 2004 was $12.5 million. One consultant estimated that outsourcing even within the United States would save a small start-up doing fewer than five designs a year up to two-thirds the cost of doing the work in-house.[44]

Another type of customer for outsourced design services are the systems companies, such as Apple Computer or Cisco. Although these companies often design chips in-house either to protect intellectual property or to reduce the cost of custom chips, they may turn to outside (and possibly offshore) service providers for specific tasks.

A great deal of outsourcing takes place in the United States. Many interviewees reported that they employed small local companies to outsource physical design on an as-needed basis.

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[40] Interview, August 2004.
[41] William Quigley, managing director at Clearstone Venture Partners (Menlo Park, Calif.), quoted in "Venture capitalist explains new rules for IC startups," EE Times, January 16. 2003.
[42] "Designs for Digital Audio, Auto Electronics," Nikkei Electronics Asia, October 2002.
[43] Interview, November 2004.
[44] Interview, April 2004.

The leading suppliers of design services worldwide are the leading design automation software vendors, Cadence Design Systems, Synopsys, and Mentor Graphics. Their annual services revenue is about $300 million out of a total outsourced design market estimated at $2.5 billion.[45] As this suggests, the remaining market is highly fragmented.

As might be expected from the increasing interaction of physical design with advanced processes, foundries work closely with design services providers. TSMC and UMC each have equity ties to a Taiwanese design service provider (Global UniChip and Faraday, respectively). In China, the emergence of low-cost foundries have also given rise to design services companies. The most advanced of these, IPCore and VeriSilicon, were both founded in 2001 by executives with years of experience in U.S. and Asia. In India, where there is no chip manufacturing to speak of, large IT service providers such as Wipro and Tata Consultancy Services have expanded into semiconductor design services for international clients. Design services revenues for Indian companies in 2001 were a relatively modest $149 million, and more recent data are unavailable.[46] Elsewhere, there are dozens of companies around the world able to help customers complete all or part of their chip designs. However most of the concern about foreign competition from low-cost chip designers focuses on China, Taiwan, and India, which are the countries that we believe will have the greatest impact on the availability of design engineers outside the United States in the years ahead.

D. Taiwan, China, and India

Outsourcing is driven in part by the steady advance of semiconductor process technology, which has created vast areas of "silicon real estate" for complex chips that could potentially be designed. The inability of design automation to keep pace with Moore's Law is sometimes referred to as a design "productivity gap" (Semiconductor Industry Association, 2003). The gap is to some extent overblown, since a relatively small percentage of designs are done at the leading edge in any one year,[47] and even fewer are done by emerging fabless companies. Nevertheless, there is an acknowledged need for more design engineers, especially with systems and analogue skills, as the industry continues to grow amid the increase in design complexity.

In order to understand what is at stake for design engineers, we created rough estimates for engineering salaries, the number of annual engineer college graduates, and the number of chip designers (excluding embedded software) for the U.S. and the three key Asian countries (see Table 9). The numbers, which are based on a combination of published sources and interviews, suggest that engineers in the United States earn much higher pay, and are more likely to be in high-level jobs such as chip design, compared to Asian engineers.

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[45] "Complex chips reignite demand for design services," EE Times, October 11, 2004.
[46] Data from NASSCOM, India's IT industry trade group, in "Designed To Win." Business India, September 1, 2003.
[47] "SOC-Mobinet, R&D and Education in SoC Design," presentation by Hannu Tenhunen at International Symposium on System-on-Chip 2004, Tampere, Finland on November 16-18, 2004, accessible at http://www.cs.tut.fi/soc/Tenhunen04.pdf as of April 19, 2005.

TABLE 9: Recent Engineering Statistics, Selected Countries

	Annual design engineer salary	Annual engineering bachelor degrees Conferred	# of chip designers
United States	$100,000	60,000	45,000
Taiwan	$ 25,000	25,000	14,000
China	$ 15,000	200,000	7,000
India	$ 15,000	100,000	4,000

Source: Authors' estimated calculation based on various sources; available upon request.

These data must be interpreted carefully. For example, the salaries represent the approximate orders of magnitude and the variance is large, in part because of U.S. profit sharing bonuses that vary over the business cycle. Benefits packages and options also cloud the picture. In the United States, for example, a full salary with benefits can be $200,000 to $250,000, which suggests a much larger gap with Asia. However the gap is narrower for comparable key employees. One report claimed in 1999 that for experienced design engineers or managers, the salary ratio between the U.S. and India is only 3-to-1.[48]

The other columns also must be interpreted carefully. The number of engineering graduates, while indicative of political and social commitment, does not translate directly to chip design capability. According to some sources, the number of chip designers being added each year in India and China is on the order of 400 each.[49]

Even the stated number of chip designers in the third column can be misleading. One industry executive claimed that the number of "qualified IC designers" in China is only 500.[50] There can even be confusion about the definition of "chip designer" We were surprised to discover that a Taiwan consultant didn't consider the later (and lower skilled) stage of physical design, called "place and route," to be part of chip design.[51] This group amounts to about 30% of Taiwan designers as we count them.

Overall these salary and headcount numbers indicate that the potential competition, especially from the emerging giant economies of China and India, may be a cause for alarm in terms of the potential future impact on the U.S. design engineering labor market.

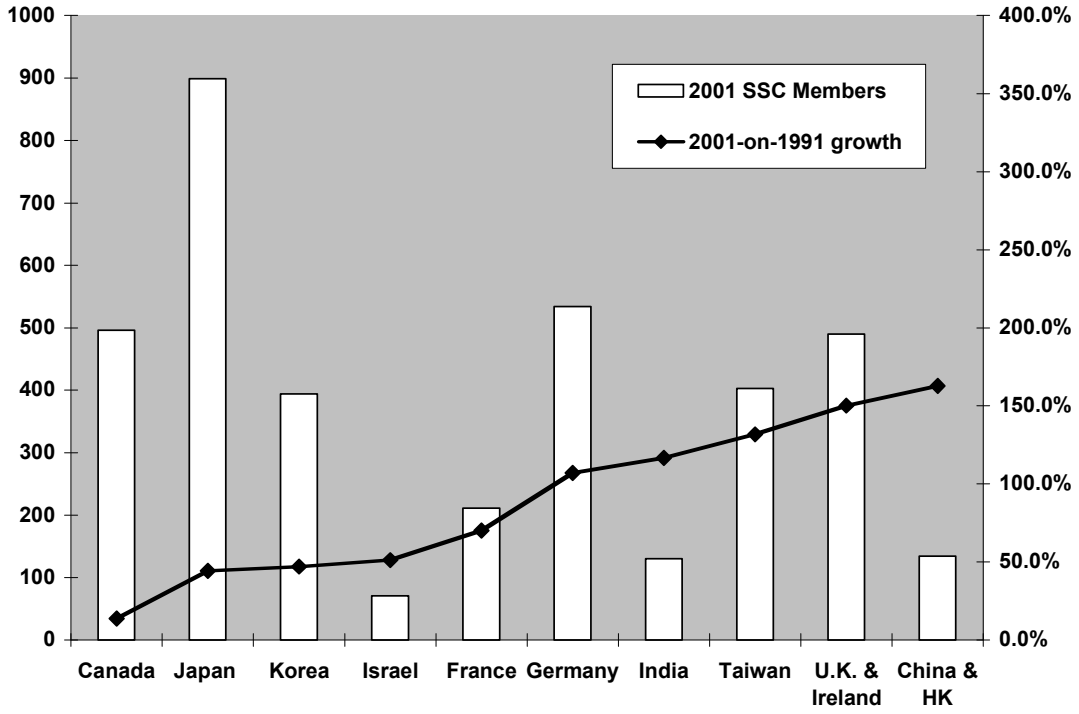
To attempt to get a clearer picture of the world-wide availability of "qualified IC designers," we consulted the Institute of Electrical and Electronics Engineers (IEEE), the leading professional organization for engineers, with almost 40% of its 365,000 members located outside the United States.[52] Of IEEE's several technical societies, the one most closely associated with chip design is the Solid-State Circuits Society (SSCS). Among other benefits, membership in the SSCS reflects an interest in accessing the latest research in the field.[53] We looked at the

[48] "Special report: India awakens as potential chip-design giant," EE Times, January 22, 1999.
[49] For India: "Designs on the future," IT People, February 10, 2003; for China: "China's Impact on the Semiconductor Industry," PriceWaterhouseCoopers, December 2004, p.7.
[50] "China's Impact on the Semiconductor Industry," PriceWaterhouseCoopers, December 2004, p.7.
[51] E-mail exchange, March 2005.
[52] From "IEEE Quick Facts," current as of January 2005. Accessed in April 2005 at http://www.ieee.org/portal/site/mainsite/menuitem.818c0c39e85ef176fb2275875bac26c8/index.jsp?&pName=corp_level1&path=about/&file=quick_facts.xml&xsl=generic.xsl
[53] This has become less true in recent years now that libraries at universities and elsewhere offer electronic access to IEEE publications. The data presented here end in 2001 when this was less an issue.

geographic distribution of membership in 2001, and compared it to 1991 (estimated)[54] for individual countries. We limited our attention to a mix of developing and developed countries with an active commercial chip-design sector (see Figure 1).[55] Because the U.S. dominates membership and requires a different scale, it is not shown in Figure 1.

In 2001, the SSCS had 19,715 members worldwide, of whom 56% were outside the United States. This was up from 13,788 in 1991, when only 45% were outside the United States. Among the countries shown, China, Taiwan and India were three of the four highest growing SSCS memberships. The United States had 8,747 SSCS members in 2001, which is estimated to have grown 16% over the preceding decade, which is less than the growth rate for all countries shown except Canada (14%).

FIGURE 1: Solid State Circuits Society Membership (2001) and Growth (1991-2001), selected countries outside the U.S.



Source: IEEE data and authors' calculations.

How do these three countries compare in their chip design capabilities?

Taiwan has the most well-established chip design sector, having benefited from focused government programs and the return of U.S. educated and trained engineers during the late 1980s (Saxenian, 2002). The Taiwanese chip design sector is mostly locally-owned, with a few multinational companies also operating design subsidiaries. Taiwanese companies have particularly embraced the fabless model, with some 60 fabless companies listed on the Taiwan

[54] Solid-State Circuits was a "Council" prior to 1997, when it became a society. Our colleague David Hodges, a member of the SSCS Administrative Council, suggested a means of estimating the 1991 membership by using a ratio involving two of the old council's sponsoring society. Details available on request.

[55] The top three countries for growth during the period were Poland, Malaysia, and China, but the first two grew from very small bases (only four and five members, respectively, in 1991).

Stock Exchange in December 2004.[56] By comparison, there were about 70 fabless companies listed on NASDAQ at that time. The 2004 output value of all Taiwan's locally-owned design companies was reported by the Taiwan Semiconductor Industry Association to be $8.15 billion.[57]

While Taiwan's design teams were praised in our interviews for their execution, which is a vital trait in an industry where time-to-market is often the difference between profit and loss, Taiwanese companies were mostly fast followers, and locked in to some extent by their reliance on the local systems firms, who are themselves as much as a generation behind the leading-edge technology (Breznitz, 2005). However competition for chips using last-generation technology has shortened the market windows during which U.S. fabless companies can recoup their investments.

China appears to be following a similar pattern to Taiwan: government sponsorship, local access to system firms such as Haier, Huawei, and TCL that are engaged in world markets, and active involvement of expatriates returning from the United States (Saxenian, 2002). As of 2003, China claimed to have over 400 fabless design firms with total revenue of $547 million.[58] Many of these are small and do not have a product of their own. One interviewee, echoed by others, claimed that outside the top 10 firms, whose total revenue was $328 million in 2003, the rest are engaged in various types of reverse engineering, much of which is illegal.[59] Foreign firms are often reluctant to bring suits in China for fear of displeasing the authorities and the unlikelihood of winning, but at least two U.S. companies have started lawsuits against Chinese rivals.[60]

China is not yet an important destination for offshoring. As many as fifteen of the world's top twenty semiconductor companies have design centers in China, but most of these are targeting the local market for the time being, and, according to various press reports, some are engaged in software or system design rather than chip design *per se*.

India presents a very different picture, with benign neglect by the government, a lack of manufacturing for chips and systems, and weaker levels of brain circulation with its U.S.-based expatriates (Saxenian, 2002). Not surprisingly, India has no major fabless companies, with its chip designers engaged in design services or working at the subsidiaries of foreign chip companies, especially U.S. and European firms. The foreign chip companies were attracted by Indian engineers' use of English and the already existing software industry. Many of the early Indian investments by chip companies were software-focused, writing the microcode that becomes part of the chip. Over time, the Indian affiliates have taken on a bigger role, eventually extending to complete chip designs from specification to physical layout. This transition can happen quite quickly. Intel, for example, opened a software center in Bangalore in 1999, then started building a design team for 32-bit microprocessors in 2002.[61]

A number of U.S. semiconductor companies have software and chip development operations in India, including Texas Instruments (1,000 employees), Freescale (200), Cypress Semiconductor (200), and National Semiconductor (80), as well as a host of fabless companies including Qualcomm and Nvidia. The oldest and largest of these is Texas Instruments (TI), which opened a software center in 1985. Most other U.S. investments in India have been made since the mid-1990s. Let us look at the case of TI India because it shows the potential for offshore chip design in India as the newer design centers develop over time.

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[56] FSA "Global Fabless Fundings and Financials Report, Q4 2004".
[57] NT$260.8 billion converted at NT$32:US$1. Datum from "TSIA: Taiwan's 2005 semiconductor production value to rise 6.7% on year," DigiTimes.com, March 18, 2005.
[58] Chinese government data cited in "TSMC: China IC design industry only a few years behind Taiwan," DigiTimes.com, September 10, 2004.
[59] Interview with a European chip executive with extensive China experience, December 2003.
[60] See "An offshore test of IP rights," Electronic Business, May 2004; and "SigmaTel Sues Chinese Chipmaker over IP," Electronic News, January 6, 2005.
[61] "Intel, TSMC Set Up Camps In Developing Asian Markets," WSJ.com, August 30, 2002.

Texas Instruments was the first semiconductor company to invest in India when it opened an office in Bangalore to work on it design automation software for internal use.[62] In 1988, the company added design for mixed-signal (analog and digital combined) chips. In 1995, TI added design for DSP devices, the company's flagship product line. In 1998, the company announced that it had taken its first DSP core from specification to working silicon over the preceding 2 years, and integrated a controller with the DSP function for the first time.

In 2003 TI India announced that it had created a highly integrated DSL chip that was the first to market to include significant analog elements on the same chip as the DSP and network processor. During the specification phase, a team of 20 engineers went to TI's Dallas headquarters and worked for 3 months with TI system engineers and dealt directly with TI customers about their requirements. The 130nm-linewidth, 13-million-transistor design was completed in India over the next year by a team of 70, worked the first time, and gave rise to eight patent applications for improvements to DSL technology. TI India had 225 U.S. patents as of August 2003.

TI India also develops design library elements, the basic building blocks needed for physical design, for TI's new processes. Although library elements are low-level intellectual property, they are critical inputs to the design process and used throughout TI's R&D infrastructure. Moreover, the designers engaged in library construction are gaining valuable experience with designing for leading-edge process technology.

Since 1999, TI India has won several awards from EDN Asia, a design industry publication, for its chips. In 2004, a very high performance analog-to-digital converter was touted during an interview by the company's CEO, who mentioned in passing that it had been designed primarily in Bangalore.[63]

Texas Instruments is clearly the pioneer among the large, vertically integrated companies in terms of outsourcing chip design to India, but it is far from unique. The trade press regularly publishes announcements by the other semiconductor companies of expansions of their Indian design centers., most of which were created in the 1990s. A fabless company we interviewed described how they started their Indian team in 2004 with logic design and will eventually expand it to doing complete derivative products.[64] A quarter of the company's 500-plus design engineers are now located in India.

We now turn to the thorny and complex question of the impact of offshoring and outsourcing on U.S. engineers.

E. What this means for the U.S.

The picture in the U.S. is unclear, but the short-term dynamic has been relatively bleak. However past experience in the semiconductor industry reminds us to be cautious in extrapolating from the present. During the past five years, the many forces affecting the semiconductor industry include the severe recession during 2001 and the recovery that stalled in 2004, the large decline in venture funding for chip start-ups that is only beginning to pick up, changes in the number of H1-B visas, and a drop in foreign student applications to U.S. graduate engineering school since 9-11. The labor market for semiconductor engineers has been weak since 2001, and it is difficult to disentangle the effect of the business cycle from any underlying long-run trend that reflects offshoring, especially of design jobs. With this caveat in mind, we look briefly at the unemployment rate and salaries for electrical and electronics engineers.

The BLS unemployment rate for electrical and electronics engineers shows that the unemployment rate spiked to 6.2% in 2003, as it converged for the first time in 30 years with the

[62] The following description is based on a compilation of published accounts and the corporate web site.
[63] "Texas Instruments collects on split fab strategy bet," EE Times, May 17, 2004.
[64] Interview, December 2004.

general unemployment rate, before falling back in 2004 to a more typical rate of 2.2%.[65] Much of the unemployment problem seems to involve electrical engineers, whose employment had not recovered to its level in 2000 (162,400) as of 2003 (149,540), whereas employment for electronics engineers exceeded the 2000 level (123,690) in 2002 (126,020) and continued growing.[66] We do not know the unemployment rate for design engineers, who comprise a fraction of electrical-electronics engineers and semiconductor engineers. Data on recent graduates and new hires show that 4-10% of EE new graduates go into the semiconductor industry and that EEs are 14-22% of all semiconductor engineer new hires during 2000-2004.[67]

More disturbing than the temporary spike in the unemployment rate are the indications of what has been happening to salaries. The IEEE reported that the median wage of its members declined in 2003, the first time since 1972, by 1.5% to $99,500.[68] The labor market situation is especially difficult for older engineers, who face rapid skill obsolescence and competition from new graduates, who are trained with the newest technology and command lower salaries. The 2004 salary survey by the EE Times found almost no difference in engineers' average salary at 40-44 years old ($104,000) versus 55-59 ($105,000).[69] Experienced design engineers are often forced to work on mature technologies, which pay less. For example, in the 2004 EE Times salary survey, the average annual salary for U. S. and European engineers skilled at designing for the latest chip process technology was $107,000, whereas engineers designing for the more mature analog technology averaged $87,000.[70]

The U.S. EE labor market is affected by supply-side forces as well as the demand side, or domestic jobs available. Government policies regulating immigration, especially the issuance of H1-B (Non-Immigrant Professional) and L-1 (Intra-Company Transfer) visas, have an important impact on the number of foreign engineers engaged in semiconductor and software work. In addition, higher education policies, which reflect both university decisions and government funding, determine the number and country of origin of engineering graduates at all levels. The importance of foreign nationals in our MS and PhD programs in EE and CS has a direct impact on the supply of engineers both in the United States as well as China and India. Foreign graduates of U.S. engineering schools must obtain temporary visas, usually H1-B visas for up to six years, before they can work in the U.S. after graduation. The complex issues relating to immigration and educational policies are controversial and beyond the scope of this paper. Experts cannot even agree if the U.S. is educating too few engineers (and scientists) or is facing an engineer shortage.[71]

When the number of H1-B visas issued was dramatically cut in 2002 and 2003 in response to the recession, many U.S. companies used the opportunity to send foreign nationals with U.S. education and experience back to India and China to help build operations there. Although the salaries are much lower, the purchasing parity comparisons indicate that engineers still enjoy a high standard of living after returning home. For example, the PPP-adjusted salary of

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[65] Data were provided by Ron Hira. BLS redefined occupations beginning with the 2000 survey covering 1999, but there is no evidence that the redefinition has contributed to the post-bubble unemployment rise. See also "It's Cold Out There", IEEE Spectrum, July 2003.

[66] Data are from the BLS Occupational Employment Statistics web site, http://www.bls.gov/oes/home.htm, accessed April 15, 2005.

[67] Data are from the annual SIA Semiconductor Workforce Strategy Committee Survey, referenced in "SIA Workforce Strategy Overview," op.cit.

[68] "EEs' median income declines for first time since '72," EE Times, December 22, 2004.

[69] "Mean wages edge closer to six-figure mark," EETimes, August 25, 2004.

[70] "After 10-year surge, salaries level off at $89k," EE Times, August 28, 2003.

[71] See for example Freeman, Richard B., "Trade Wars: The Exaggerated Impact of Trade in Economic Debate" (September 2003). NBER Working Paper No. W10000; Task Force On The Future Of American Innovation, 2005; National Research Council, Building a Workforce for the Information Economy, National Academy Press, 2001; National Research Council, Forecasting Demand and Supply of Doctoral Scientists and Engineers, National Academy Press, 2000; Butz, William, Terrence Kelly, David Adamson, G. Bloom, D. Fossum, and M. Gross, Will the Scientific and Technical Workforce Meet the Requirements of the Federal Government? RAND, 2004.

design engineer is $77,300 in India and $69,400 in China, compared to $100,000 in the U.S.[72] Using data from 'PhDs…Ten Years Later', a study of foreign-born US PhDs in science and engineering shows the importance of personal values, work-related considerations, and formal and personal ties, as opposed to purely economic motivation, in the decision to return home (Gupta, 2005a). The foreign-born PhDs who left the US were also likely to be significantly more satisfied with their jobs, especially those in academia, than their peers who stayed (Gupta, 2005b).

As we saw in the earlier examples of assembly offshoring and fabrication outsourcing, there are both costs and benefits for the economy as a whole, and in the past the domestic industry has responded to global competition in a way that rejuvenated itself. Recall that the shift of assembly offshore helped American companies to stay competitive with low-cost rivals and to maintain high-value jobs at home. The availability of offshore fabrication by foundries gave rise to the growth of fabless companies and helped fab-owning incumbents manage the enormous fixed costs and their inherent risks.

The offshoring of design is being driven by the continual need to reduce rapidly rising costs in order to keep demand expanding, especially in consumer markets. The large fixed costs associated with developing chips and in building fabs require that companies develop high-volume products to amortize their investments. Today's competition is not coming from lower-cost Asian competitors, as was the case in assembly offshoring, but rather from other established competitors in Europe and Japan. Moreover, as we have seen in the case of Texas Instruments India, the jobs moving offshore are very close technologically to what's being retained at home, as we experienced during the rise of manufacturing abroad (but in contrast to the movement of assembly abroad).

We may be seeing some of the same dynamics of job movement over the business cycle as occurred during the offshoring of assembly. A wave of design offshoring took place at the height of the dot.com bubble. When the cascading effect of the subsequent downturn reached the semiconductor industry, chip companies cut staff at home. Now that the recovery requires expansion of design operations, chip companies appear to be expanding design operations abroad faster than at home.[73]

The question is to what extent can the industry benefit from the expansion of design operations abroad in developing new or larger markets, in improving the global competitive position of U.S. companies, or in restructuring the industry so that the United States maintains its leadership in innovation?

The reduced design costs and the flexibility provided by regional design centers has allowed both new entrants and incumbents in the U.S. to maintain a competitive position despite the rising cost of the typical chip design. The lower costs have translated into growing consumer markets, both for advanced products in the developed countries and for scaled-down products in developing countries, especially fast-growing Asian markets. In addition, U.S. companies have carefully considered what intellectual property they must protect and keep close to home, and what activities can be sent offshore, often with new protections in place. U.S. companies have also become savvy about how to develop products for regional markets, and often locate design and marketing activities accordingly. In addition, fab-owning companies like Intel and TI, are mindful of when integration of design and manufacturing know-how helps in product development and time to market, and so keeps those activities at home and close together when necessary. The executive team at domestic headquarters understands the importance of controlling global activities, especially in the chip development stage, and management jobs will

[72] This calculation is based on the PPP of .194 for India and .216 for China reported in the Testimony for the IEEE by Ron Hira to the Small Business Committee, available at http://www.cspo.org/products/lectures/061803.pdf. The PPP is applied to the estimated $15,000 salary reported in authors' Table 9 (above).

[73] See, for example, "The perfect storm brews offshore," Electronic Business, March 2004, accessible at http://www.reed-electronics.com/eb-mag/toc/03%2D01%2D2004/

remain critical in overseeing the global supply chain and knowledge network. Among the professions cited as safest from offshoring in A.T.Kearney's report on Silicon Valley are managers of global teams, select engineering, marketing, venture capitalists, and lawyers (A.T.Kearney, 2004: p.viii).

To what extent do the observed trends indicate the rise of market leaders (and competitors) in other countries at the loss of U.S. industry leadership and U.S. design jobs? The secondary lesson from offshore assembly, that local firms will emerge as subcontractors, is relevant to design. Design subcontractors have already appeared. But because the activity offshored is more central to the firm than was assembly, the "local firm" effect may give rise to new rivals, as we observe in Taiwan, although the fabless sector is nearly a generation behind U.S. rivals in terms of innovative products. For now, local firms in India have generally avoided the fabless model, but in China there are an increasing number of fabless firms targeting world markets. Although for now Chinese firms lack experienced engineers and managers and appear to be behind Taiwan in their development of innovative products, this will gradually shift in the years ahead.

There are diffuse benefits from offshoring in the short-run. Consumers benefit from lower prices and new products, although much of that benefit is received outside the United States.

Even if there should prove to be positive net social benefits, they are irrelevant to the "losers" if they aren't compensated by the "winners" from the global shift. Currently, white-collar workers like chip designers don't qualify for trade-adjustment assistance from the government when their jobs are sent abroad.

At the end of the day, we at the beginning of a dynamic process that will unfold, and predictions would be foolhardy. Although we observe an expansion of design jobs offshore compared to design jobs in the U.S., it's hard to say how important this is to the U.S. labor market. At this point we are not sure what the impact will be on the competitive position of the U.S. semiconductor industry, how long it will take for the economy to adjust, and whether the new equilibrium will be acceptable. We join the chorus of many observers that more labor market data, both for the U.S. and our trading partners, are needed in order to facilitate research on these questions. We believe that what happens to the U.S. semiconductor industry and its workers have important consequences for the country, including the jobs created and the technology developed. Until we have better data, our national policies affecting education, labor markets, and innovation will continue to be based upon informed speculation.

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