UNIVERSITY OF CALIFORNIA,
IRVINE

Environmental Effects on Indium Arsenide Composite Channel (IACC) High Electron Mobility Transistors (HEMT) Performance

DISSERTATION

submitted in partial satisfaction of the requirements
for the degree of

DOCTOR OF PHILOSOPHY

in Engineering
with a concentration in Materials and Manufacturing Technology

by

Besmeh Farhan Raya

Dissertation Committee:
Professor G.P. Li, Chair
Professor Martha Mecartney
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2019

DEDICATION

To

My Enormous, Growing Family

Table of Contents

List of Figures

Page

List of Tables

Page

Acknowledgments

I would like to acknowledge everyone in my life who has made this degree possible. This has been my dream and I cannot thank everyone enough. First, I would like to acknowledge my advisor, Dr. G.P. Li. He was the one who introduced me to my research group. He helped me get through the research when I didn't know anything about semiconductors. I cannot thank him enough.

I would like to thank my committee members, Dr. Martha Mecartney and Dr. Marc Madou. They have been patient with me finishing up my research. Dr. Mecartney gave me the chance to start at UCI and I am so thankful she took a chance on me. I am thankful to the rest of my UC Irvine people who have helped me put all this together; Aileen Broccardo, Alana Valencia and Marc Palazzo. They helped me schedule meetings and pay lab fees. These things wouldn't have been solved and completed if it wasn't for their help and understanding.

I was able to learn so many things about microscopy during this research project due to Dr. Jian-Guo Zheng's help at the UC Irvine Materials Research Institute (IMRI). I already had experience with a SEM/EDS for a few years but Dr. Zheng helped me understand and operate a SEM/FIB, TEM and STEM. I owe a great lot to Dr. Zheng on how to analyze my HEMTs. Evans Analytical Group also helped analyze HEMTs and gave me tips on how to cross-section them.

I now have to thank my entire, huge family. My family grew during my time as a graduate student. I never thought it would during this time, but it happened and it is wonderful. I want to thank my parents. I was drawn to science and Galileo when I was a little girl instead of playing with dolls and my parents let me experience it all. I naturally excelled in math and science during my K-12 years and chemistry became my undergraduate degree. I ended up with an engineering career at one of the largest companies in the world. I got married while I was in the middle of my Ph.D., and my husband has had all the patience in the world while I had very early mornings to attend 8 am classes because we lived 90 miles away from UCI, had late nights in the lab and encouraged me to continue even when things looked grim. We then had our first child together and raising my baby while my husband took a job 400 miles away from us for 18 months and trying to finish up my degree was a challenge. I couldn't have done it without my parents and in-laws taking care of my baby when I needed to work on my research. I also want my son to hopefully grow up and understand that you can do anything as long as you persist and work hard; and women can excel in engineering with a family if they want to.

I want to thank my Materials and Processes Engineering family for all their support. They allowed me to be part-time so I can finish up my degree and work around my schedule. I am so thankful to everyone especially Barbara Kurtin who has been an amazing mentor and wonderful inspiration. Kurt Carlson peer reviewed my papers and encouraged my writing.

Lastly, but not least, I want to thank all those who gave me recommendation letters to enter this degree, Dr. Dale Conner, Dr. Behzad Bavarian, Greg Moore, Dr. Samad Elyamani. I want to thank everyone for their kind words and encouragement to start this degree and gave me the opportunity to do this while working.

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FIELD OF STUDY

Failure analysis and reliability of Nanometer-Range Indium Arsenide Composite Channel InP High Electron Mobility Transistors

CONFERENCE PRESENTATIONS

- Nanomilling of a Sub-50 nm Indium Arsenide Composite Channel High Electron Mobility Transistor. SAMPE Conference Proceeding, 2018.
- FIB-STEM Imaging of a Sub-50 nm Indium Arsenide Composite Channel High Electron Mobility Transistor. ASM Meeting, 2018.
- Can we rely on technology as it decreases in size? Associated Graduate Students Symposium, UC Irvine, 2018.
- FIB-STEM Imaging of a Sub-50 nm Indium Arsenide Composite Channel High Electron Mobility Transistor. Microscopy and Microanalysis Meeting, 2017.
- Reliability of a Sub-50 nm Indium Arsenide Composite Channel High Electron Mobility Transistor. Brown Bag Lecture Series, Northrop Grumman, 2017.

Abstract of the Dissertation

Environmental Effects on Indium Arsenide Composite Channel (IACC) High Electron Mobility Transistors (HEMTs) Performance

By

Besmeh Farhan Raya

Doctor of Philosophy in Engineering, Materials and Manufacturing Technology

University of California, Irvine, 2019

Professor G.P. Li, Chair

The nanometer-range Indium Arsenide Composite Channel (IACC) High Electron Mobility Transistors (HEMTs) are fabricated on 100 mm Indium Phosphide (InP) substrates. This technology offers the best performance for low-noise and high-frequency, space and military applications. Typical failure mechanisms are observed in III-V HEMT technologies, including gate sinking and oxidation. Experiments were conducted to determine if these failure mechanisms degrade the IACC HEMTs after updating the new HEMT. The experiments conducted were life tests completed at accelerated temperatures and biases with a thin Si_3N_4 passivation layer; the devices' electrical characteristics were measured at each stress interval. The failure mechanisms examined within this dissertation include: gate sinking, which is the interdiffusion of the metal gate into the semiconductor. Therefore, a temperature stress was done to initiate the mechanism; oxidation is the migration of oxygen atoms into materials are induced by a high electric field and high temperature. The Si_3N_4 passivation thickness was then increased to determine if the degradation of the electrical parameters could be decreased. Four HEMTs were placed on a Low-Noise Amplifier (LNA) circuit, therefore, an additional LNA assessment was completed to determine which device degraded and where the defect might be located; the Low-Noise Amplifier (LNA) Circuit assessment determines the limiting HEMT in the LNA

circuit. Since many of the known III-V semiconductor failure mechanisms physically degrade or damage HEMTs, cross-sections are important to prepare to detect these mechanisms. Advanced microscopy techniques, with sub-nanometer resolutions, examined physical characteristics of the HEMT at the atomic scale. Each device was cross-sectioned with a Focused Ion Beam/Scanning Electron Microscope (FIB/SEM) and polished with a Nanomill to about 100 nm thickness at the gate fingers to look for the failure mechanisms. The Scanning Transmission Electron Microscope (STEM) along with Energy Dispersive Spectroscopy (EDS) was then used to see the oxygen in the titanium gate layer and no gate sinking. TCAD modeling simulations were used to verify these results and show that the Schottky barrier height changes and the oxygen diffuses faster through the titanium gate layer due to the electric-field increase.

Chapter 1 **The High Electron Mobility Transistor (HEMT)**

Introduction

Background

The High Electron Mobility Transistor (HEMT) is a type of Field Effect Transistor (FET) that was demonstrated in 1979 by Dr. Takashi Mimura [1]. The gate length of the first HEMT was 2 µm [2]; since then, the HEMTs have decreased exponentially in size due to shrinking technologies. Moore's Law is an observation made by Intel co-founder Gordon Moore in 1965 that suggested the number of transistors per square inch on integrated circuits would double every two years for the foreseeable futur [3] e. His prediction has remained true, except for the fact that they have been increasing faster than "every two years." The smaller HEMTs require smaller gate lengths, which have now reached the nanometer range [4].

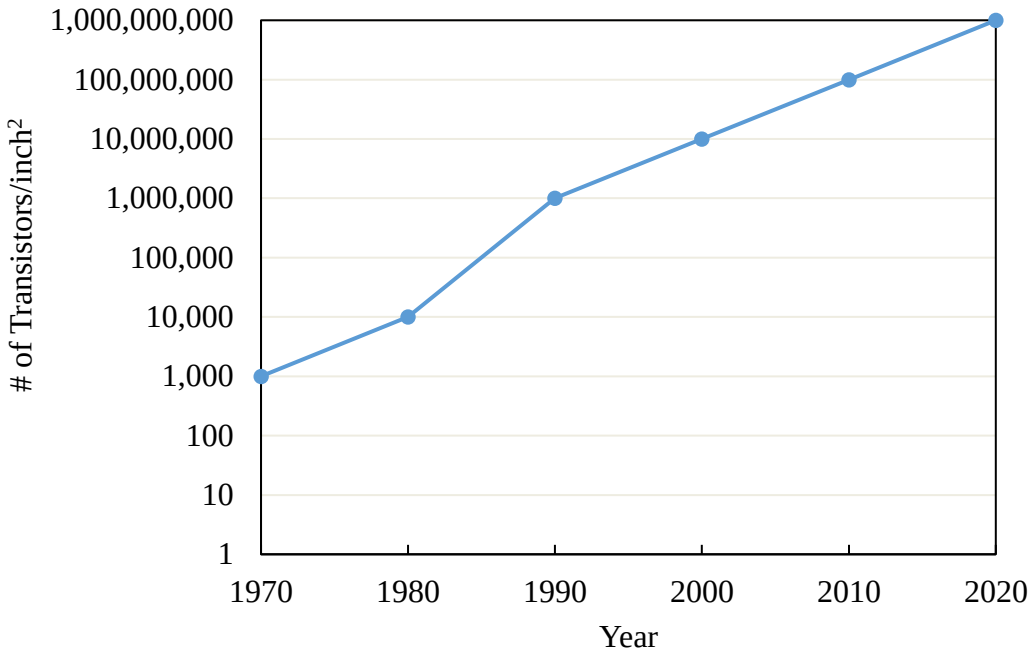

Figure 1.1: Moore's Law: extrapolation of number of transistors placed on a circuit over time [3]

Even though the HEMTs have become smaller, their performance has not diminished. It has been shown in [5] that as the HEMTs decreased in size, and the gate-to-channel distance

decreases, their cutoff frequencies (f_T) have increased. Recently, Mei, et. al. developed a Terahertz Monolithic Integrated Circuit (TMIC) amplifier based on a 25 nm InP HEMT process. It demonstrated amplification at 1.0 THz (1000 GHz) with 9 dB measured gain at 1.0 THz; this is the first ever demonstration of amplification in a transistor-based circuit at 1.0 THz reported. Table 1.1 below shows the roadmap of the development to the terahertz circuit [4].

Table 1.1 Summary of InP HEMT processes developed to reach the THz cutoff frequencies

Gate length	100 nm	70 nm	35 nm	30 nm	25 nm
Year introduced	1998	2503	2507	2010	2013
In(x)Ga(1-x)As channel indium composition	60%	75%	100%	100%	100%
Source-Drain spacing (μm)	2	2	1.5	1.0	0.5
R_c (mΩ.mm)	0.12	0.1	0.04	0.04	0.04
G_{mp} @ 1 V (mS/mm)	1000	1400	2500	2500	3000
f_{max} (THz)	0.4	0.6	1.1	1.3	1.5
Associated f_T (THz)	0.2	0.25	0.4	0.5	0.61
Highest frequency amplifier demonstrated (THz)	0.19	0.24	0.48	0.85	1.0
Associated amplifier device width (μm)	30	30	20	14	8

InP HEMTs offer the best performance for low-noise and high frequency applications [6] due to their superior inherent transport properties [7]. For these reasons, and others, InP HEMTs are widely used in Low-Noise Amplifier (LNA) Monolithic Microwave Integrated Circuits (MMICs). These devices are used in space and military applications including deep space communications and radio astronomy, where the signal amplification requires cryogenic operation of the HEMTs at temperatures of ~10 Kelvin.

This paper investigates the indium arsenide (InAs) composite channel (IACC) InP HEMT with a 250 Å Si_3N_4 passivation later. This technology offers state-of-the-art performance for low-noise and high-frequency applications due to its inherent material properties such as high electron mobility, high saturation velocity and high sheet carrier density. This sub-50 nm IACC HEMT profile provides 25% higher electron mobility than InGaAs (indium/gallium/arsenide), which

provides ultra-low power at low frequencies, fast speed and highest gain. It has demonstrated transconductances (G_m) up to 2500 to 2500 mA/mm and cut-off frequencies (f_t) in the range of 250 to 300 GHz.

The sub-50 nm Indium Arsenide Composite Channel (IACC) High Electron Mobility Transistors (HEMTs) are fabricated on 100 mm Indium Phosphide (InP) substrates. Figure 1.2A shows a top view SEM image of an IACC HEMT and 1.2B displays the cross-section of a 35 nm InP HEMT T-gate [7].

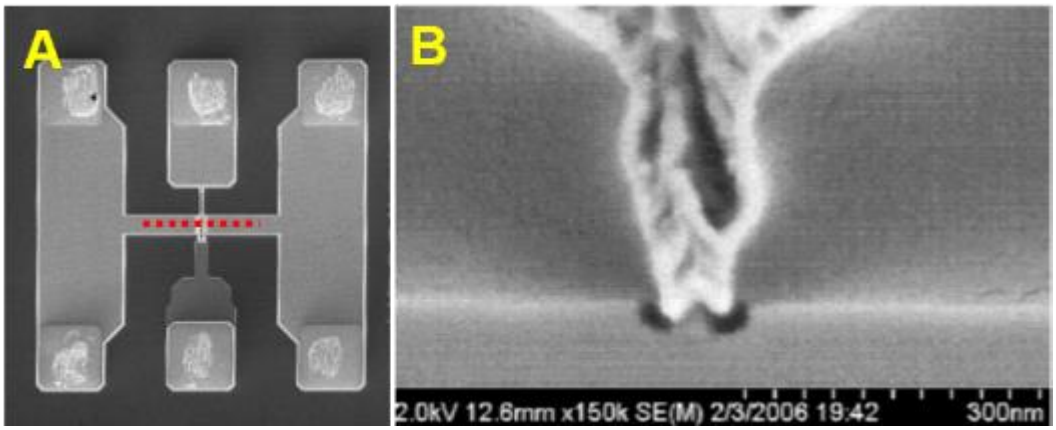

Figure 1.2: (A) Top view SEM image of InP HEMT. The red dotted line indicates the location of the cross-section. (B) Cross-section of a 35 nm InP HEMT

Figures 1.3A and B show the extrapolated device Fmax based on unilateral gain (U) of 1.2 THz and maximum stable gain (MSG)/maximum available gain (MAG) of 1.1 THz, which is the first extrapolated device Fmax above 1 THz [7].

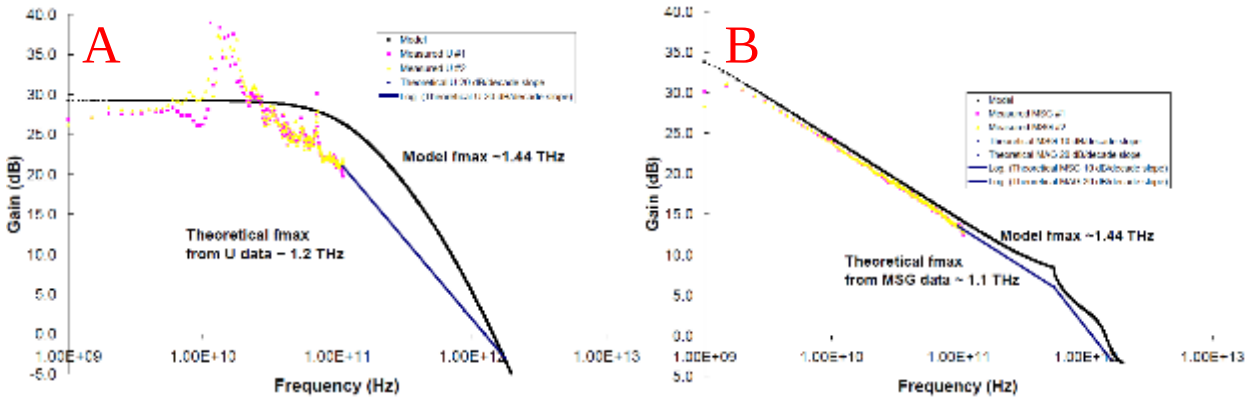

Figure 1.3: (A) SEM cross-section image of a 35 nm InP HEMT T-gate; Calculated and extrapolated Fmax based U (B) and MAG/MSG (C) for 2f20 um InP HEMT from measured S-parameters (theoretical extrapolation with 20 dB/decade for U and MAG and -10 dB/decade for MSG; calculated from equivalent circuit model)

Previous InP HEMT technologies were manufactured using a titanium/platinum/gold (Ti/Pt/Au) gate metal stack without a barrier layer between the metal gate and the semiconductor [8] and with a platinum barrier [9]. In both instances, gate sinking i.e. metal diffusion into the semiconductor, was the main degradation mechanism but for space and military applications, it was deemed sufficient. Then, in 2005, a new Northrop Grumman Metal Electrode Technology (NGMET), was shown to improve the gate sinking effects from the previous technologies [10] in a nitrogen environment. This paper will focus on the reliability of this new NGMET material through electrical lifetests in air, with a silicon nitride (Si_3N_4) passivation layer, to determine if these space and military application devices, placed in hermetically sealed instruments, can withstand being outside of nitrogen-filled environments for commercial-use advantages. The new NGMET material, which has shown to reduce the interdiffusion of the metal into the semiconductor, is shown in a schematic diagram in Figure 1.4. The devices undergo electrical bias lifetesting and are then cross-sectioned with the Focused Ion Beam/Scanning Electron Microscope (FIB/SEM) to relate the physical behavior of the Schottky barrier to its electrical characteristics. The Scanning Transmission Electron Microscope/Energy Dispersive Spectroscope (STEM/EDS) will then be used to analyze the physical features of the cross-section and its chemical structure.

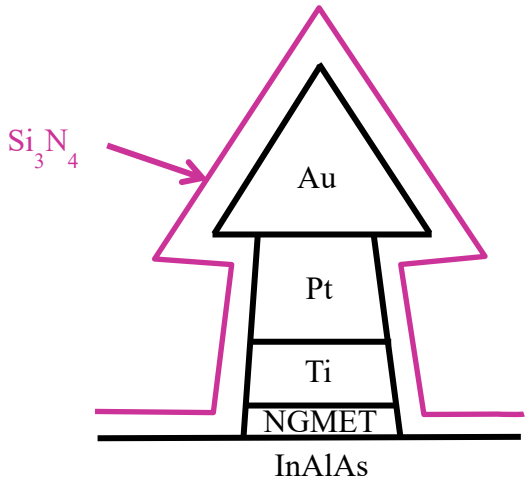

Figure 1.4: Schematic diagram of a cross-section of Schottky gate

Operation and Structure

The HEMT works by the current flowing between two Ohmic contacts, source and drain, and controlled by a third contact, the gate. The gate is a Schottky contact, which is a metal-semiconductor union with a large barrier height and a low doping concentration that is less than the density of states in the conduction or valence band [1]. The current flows into the source and out of the drain as a voltage is applied through the gate. Varying the voltage alters the amount of current traveling through the transistor. The transistor then takes these current signals and can either amplify them into larger signals, or turn them on and off, similar to a switch. Figure 1.5 shows the current flow and layers of an IACC HEMT structure.

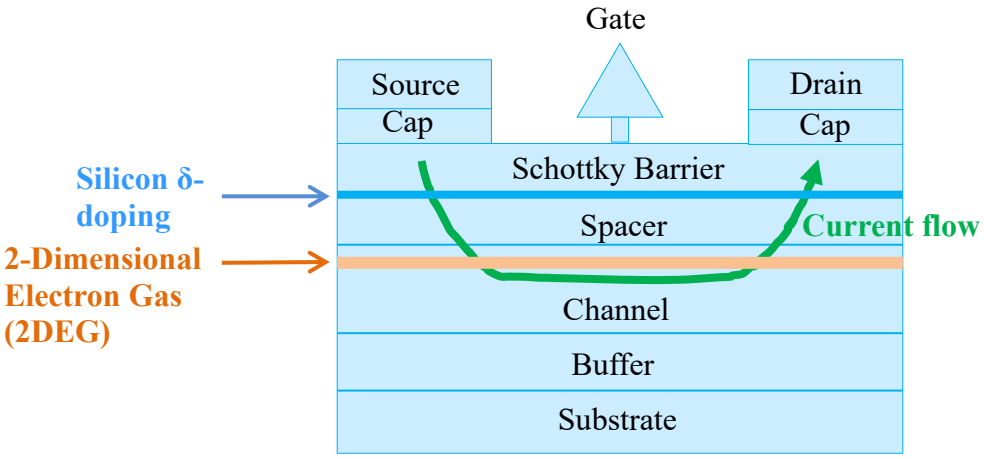

Figure 1.5: Cross-section of a HEMT structure and layers

Each layer of the HEMT provides a unique function to enhance the HEMTs electrical characteristics. The silicon delta-doping (δ-doping) layer is a highly doped layer that is only a few angstroms thick. The δ-doping layer is grown by Molecular Beam Epitaxy (MBE) by the crystal growth suspension and evaporation of impurities on the non-growing crystal surface. The δ-doping layer is placed between the Schottky Barrier and Spacer layers to provide electrons to the channel. When two semiconductors come into contact, they form a heterojunction. Heterojunction structures benefit from the improved electron mobility appearing in the quasi-triangular quantum well formed at the boundary of the heterojunction. The 2DEG forms in the quantum well at the interface of the heterojunction, in the channel layer side. Initially, the electron concentration depends on the doping density of the barrier layer. The electrons drain into the potential well and form the 2-dimensional electron gas (2DEG) in the channel since they occupy the lowest energy state. The Spacer layer assures the separation between the electrons and the silicon-donors. This reduces impurity scattering, which in turn, improves electron mobility in the channel. The Cap is a highly n-doped layer (n = electron concentration) that helps minimize the contact resistance of the source and drain contacts. When the heterojunction is formed, the excess of electrons of the n-type doped InGaAs barrier layer will move to the InAs channel layer trying to minimize their

energy until the balance of the Fermi level between the two materials takes place and equilibrium state is established, Figure 1.6 [11]. This delivers high doping levels with high electron densities [2]. Therefore, high transconductances, current densities and cut-off frequencies are possible. If the channel is built only by a single heterojunction, the electrons are penetrating into the buffer under the channel very easily where their mobility is usually lower and the control of the gate is poor. To keep the electrons in the channel, a second energy barrier below the channel can be introduced by a material with a higher E_c than the channel material.

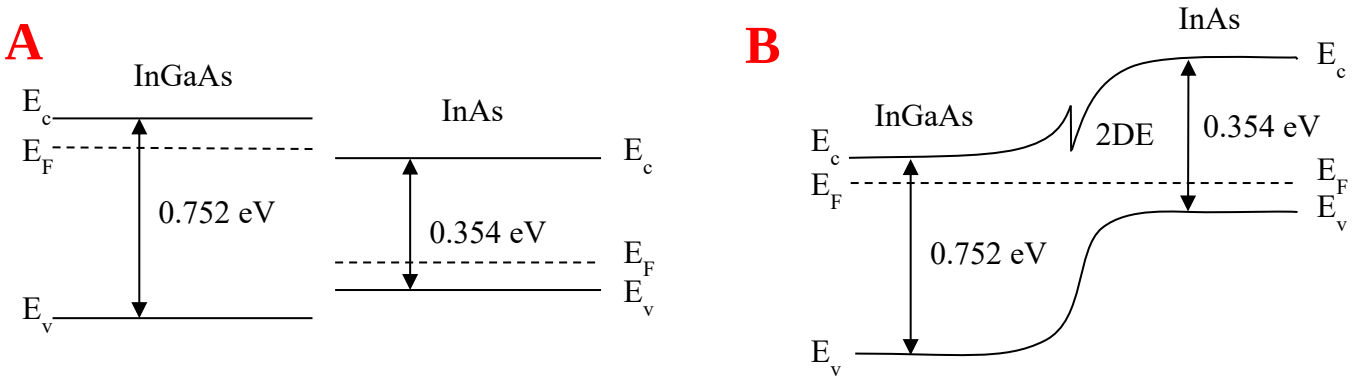

Figure 1.6: (A) Diagram of the band structures of InGaAs and InAs at equilibrium; (B) Semiconductors in contact at equilibrium. A 2DEG is formed at the interface

The Schottky Barrier layer provides rectifying characteristics between the gate-metal and semiconductor materials. It prevents large currents from flowing through the gate and limits tunneling to the channel [3], which will be described further in detail in the next section. The substrate is the semiconductor material used to move charges.

Metal-Semiconductor Contacts (Schottky Junction)

The Schottky Barrier

To understand the environmental effects on the Schottky gate, we treated the HEMT as the simplest semiconductor, a diode, by biasing the Schottky gate under various conditions. The

Schottky gate typically passes current in only one direction, therefore, making it easier to see what is happening within the device by its electrical characteristics in this one region. The band diagrams of the metal and semiconductor will provide an understanding on how the electrical characteristics relate to the physics of the semiconductor shown in Figure 1.7. In order to form a Schottky contact, the metal work function must be larger than the semiconductor work function. Otherwise, an Ohmic contact is formed if the metal work function is smaller. When the Schottky junction is formed, the Fermi levels must line up at equilibrium. The Fermi level (E_{Fermi}) is the energy point where the probability of occupation of an electron is 50%, or 0.5. Metals do not have band gaps (E_g), unlike semiconductors; the valence (E_V) and conduction bands (E_c) overlap where free electrons are available for electrical conduction. The n-type semiconductor includes a band gap where electrons are forbidden to have energy in this region. When the electron from E_v acquires enough energy to detach from the atom, it reaches E_c. Since the semiconductor is an n-type material, the majority mobile carriers are free electrons and the average energy of the electrons is close to the conduction band. Therefore, the electrons in the n-type semiconductor sit in the conduction band, and since the metal work function is larger, the conduction band of the semiconductor is higher than the Fermi level of the metal. Therefore, as the two materials come together, the electrons in the semiconductor move into the empty energy states above the Fermi level of the metal and the Fermi levels come to equilibrium. This then leaves a positive charge in the semiconductor and an excess of electrons, a negative charge, in the metal, creating a contact potential in the opposite direction of the movement of electrons. Figure 1.8 shows the contact potential being formed. [12]

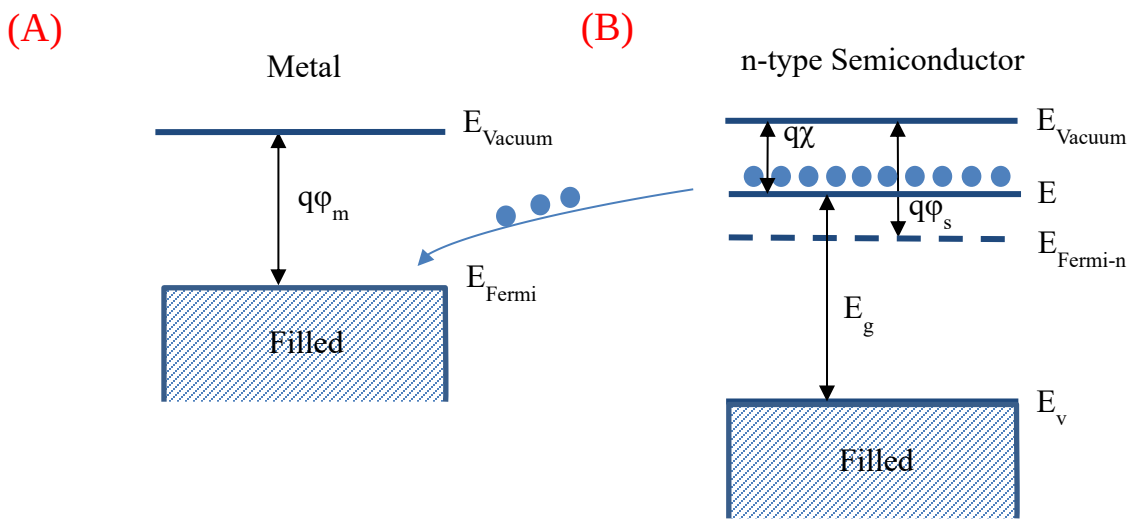

Figure 1.7: (A) Band diagram of a metal; (B) Band diagram of an n-type semiconductor

The semiconductor Fermi level will lower relative to the metal by an amount equal to the difference between the two work functions. The work function is the energy difference between the vacuum level and the Fermi level. The metal work function is denoted as φ_m and the semiconductor work function as $\varphi_s = \chi + \varphi_n$, where χ is the electron affinity from the bottom of E_c to vacuum level and φ_n is the energy difference between E_c and the Fermi level. The contact potential is the potential difference between $\varphi_m - (\chi + \varphi_n)$ [12].

When the metal and semiconductor come into contact, the gap is transparent to the electrons and we get the limiting value of the barrier height ($q\varphi_{Bn0}$).

$$q\varphi_{Bn0} = q(\varphi_m - \chi)$$

The Schottky barrier height is the difference between the metal work function and electron affinity of semiconductor. In an ideal contact:

$$q\varphi_{Bp0} = E_g - q(\varphi_m - \chi)$$

Therefore, the sum of the barrier heights on n-type and p-type substrates is equal to the bandgap.

$$q(\varphi_{Bn0} + \varphi_{Bp0}) = E_g$$

This contact potential is a barrier which prevents further motion of the electrons to the metal, called the Schottky barrier (φ_B) given as:

Equation 1.1 $\varphi_B = (\varphi_m - \varphi_s) + (E_C - E_{F-n}) = \varphi_m - \chi_s$

After contact, the Schottky junction is formed and the semiconductor's bands bend upward towards the metal in the direction of the electric field (positive to negative charge, opposite of the contact potential), shown in Figure 1.8. The band bending is a result of the electrons that are removed from the surface of the semiconductor with a certain depth, called the depletion region (W_D), Figure 1.9. A built-in potential is created in the Schottky junction, V_0, and is the difference between the work functions.

Equation 1.2 $\varphi_m - \varphi_s = eV_0$

The work function of the metal is constant, where the work function of the semiconductor varies depending on the dopant concentration. [12]

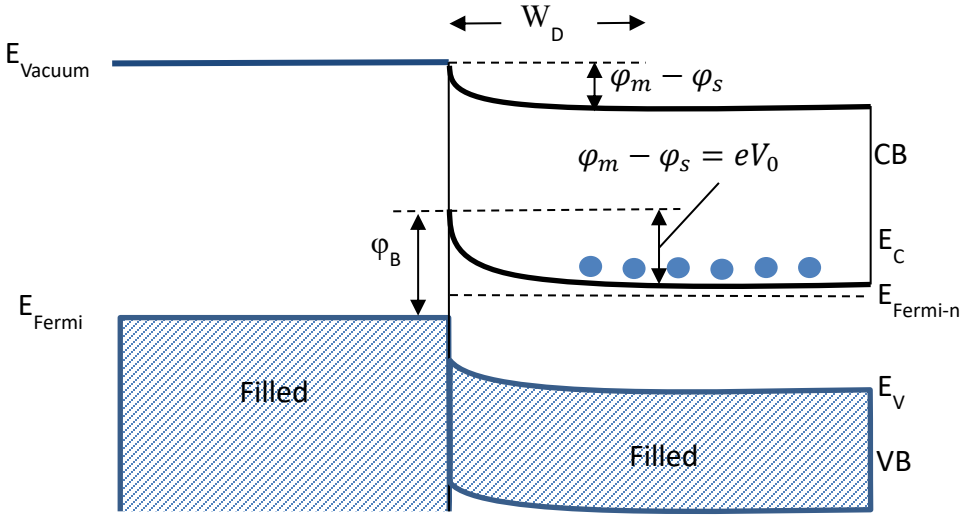

Figure 1.8 Schottky junction band diagram showing the upward band bending of the semiconductor as the materials come into contact

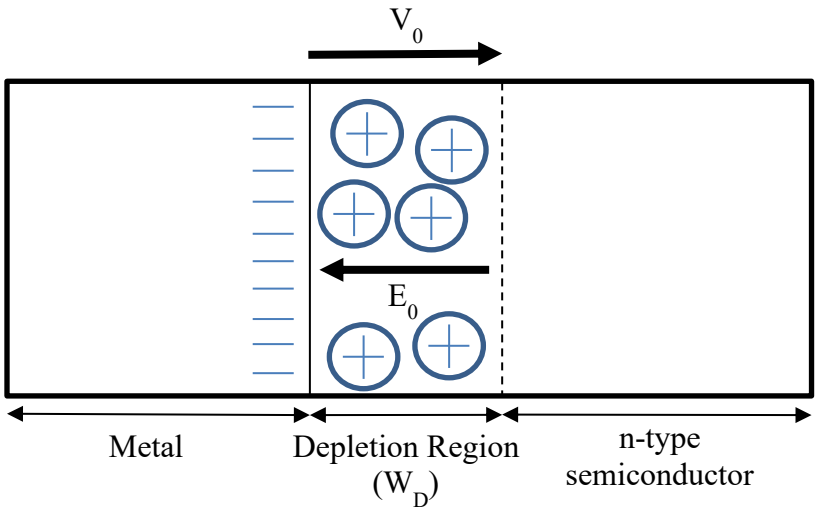

Figure 1.9 Schematic of how the contact potential is formed as the metal and semiconductor come together

With an external bias, the Fermi levels no longer line up and the magnitude of their shift depends on the applied voltage, Figure 1.10. This is due to the external electric field that opposes the built-in potential and the voltage drop is across the depletion region, it has the highest resistivity. As a forward bias is applied between the two ends of the Schottky junction, free electrons and holes will gain enough energy to cross the junction as the depletion layer width is decreased. The current in the circuit then increases with increasing bias. The current in the Schottky under forward bias is given by

$$\textbf{Equation 1.3}\ J = J_0[\exp\left(\frac{eV}{k_B T}\right) - 1]$$

Where J is the current density for an applied potential of V. J_0 is the saturation current and depends on the Schottky barrier (φ_B) for the system and the expression is

$$\textbf{Equation 1.4}\ J_0 = A^* T^2 \exp\left(-\frac{q\varphi_B}{k_B T}\right)$$

Where A* is the Richardson constant for thermionic emission and is a material property. Equation 1.3 (J) shows that in the forward bias, the current exponentially increases with applied voltage. [12]

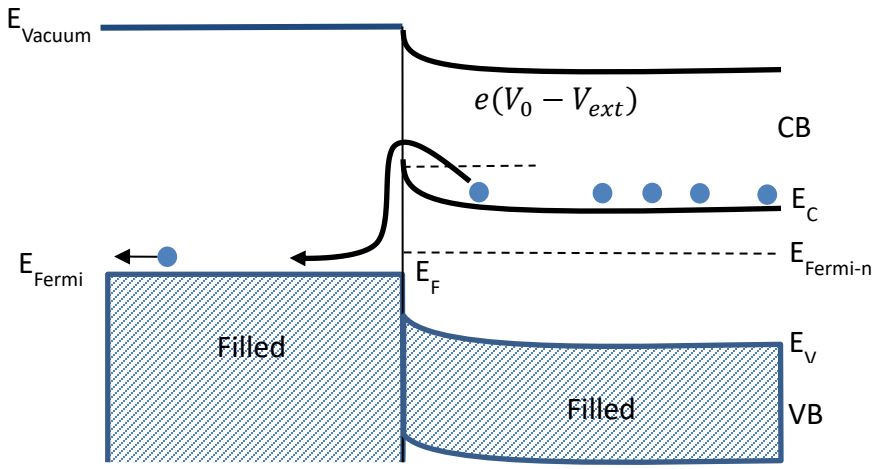

Figure 1.10: Band diagram of Schottky junction under forward bias

In the reverse bias, shown in Figure 1.11, the external bias is applied in the same direction as the built-in potential. The Fermi levels, like in the forward bias, do not line up but the barrier increases for the electrons that move from the semiconductor to the metal. The electron flow moves from the metal to the semiconductor and the barrier is shown as (φ_B). The following equation shows that there is a constant current in reverse bias equal to J_0. With this equation, it can be shown that the current in the forward bias is orders of magnitude higher than the current in the reverse bias (due to the exponential dependence on potential). The Schottky junction acts as a rectifier i.e., it conducts in forward bias but not in reverse bias. [12]

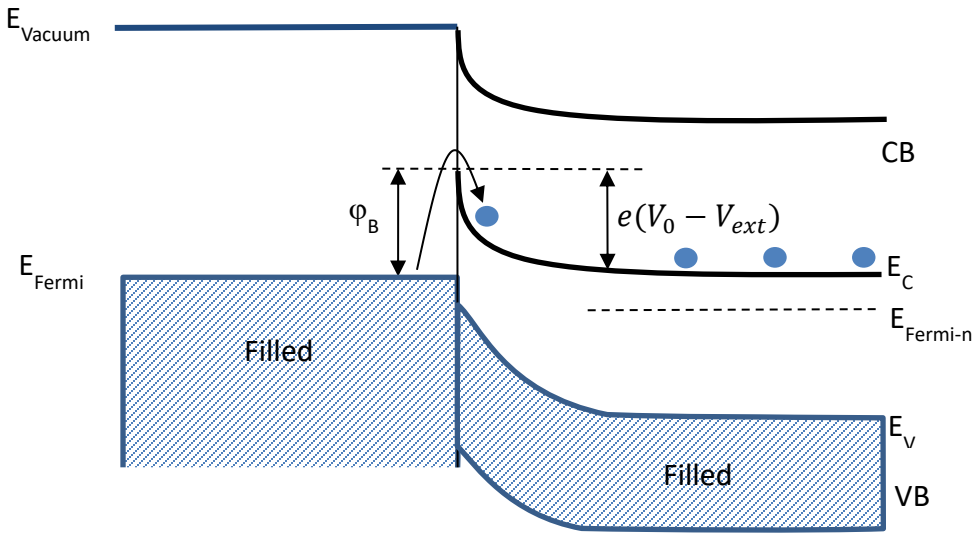

Figure 1.11: Band diagram of Schottky junction under reverse bias

The work functions of metals and electron affinities of semiconductors are established quantities; the materials focused in this paper are shown in Table 1.2. The values of the work function are very sensitive to surface contamination. Main deviations for experimental barrier heights from ideal conditions: (1) an unavoidable interface layer, where there is something between the metal and semiconductor and they are not in complete contact with each other and (2) the presence of interface states. [12]

Table 1.2: Work function and electron affinities of the materials used in the IACC HEMT

Material	Work Function (eV)	Electron Affinity (eV)
Tungsten (W)	4.5	-
Titanium (Ti)	4.33	-
Indium/Aluminum/Arsenide (InAlAs)	-	0.55
Indium/Gallium/Arsenide (InGaAs)	-	0.752

Interface States

The barrier heights of the metal-semiconductor system are determined by the metal work function and the interface states. Two assumptions are made for the barrier height expression: (1) the barrier height is transparent to electrons with an interfacial layer of atomic distances but can

withstand a potential across it, (2) the interface states per unit area per energy at the interface are a semiconductor surface property and are independent of the metal [12].

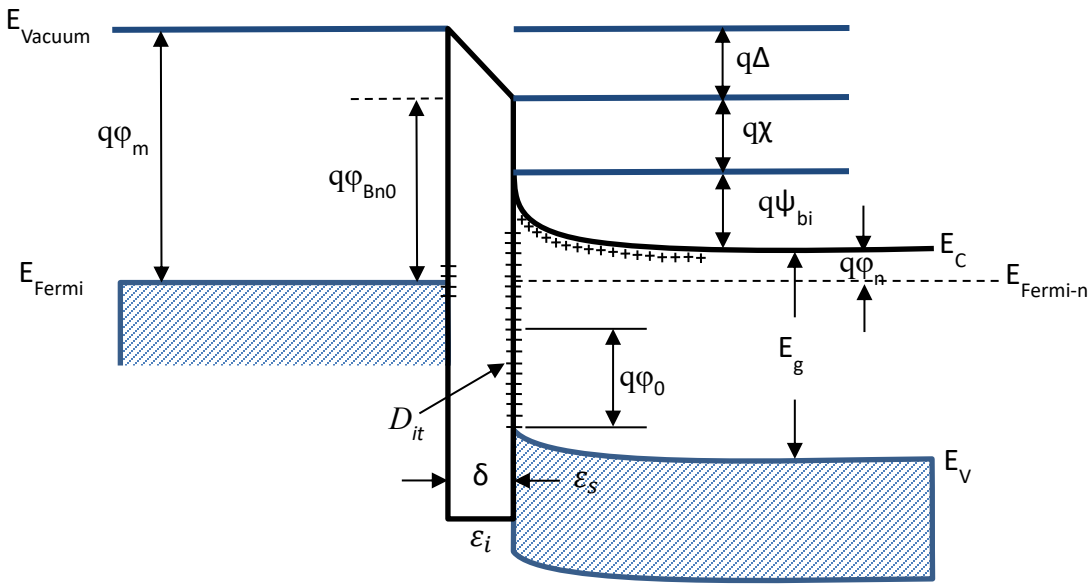

Figure 1.12: Energy band diagram of metal-semiconductor contact with an interfacial layer (vacuum) on the order of atomic distances

The neutral level, $q\varphi_0$, is above E_v at the semiconductor surface. It is above the interface states that are of acceptor type (neutral when empty, negatively charged when full) and below the states that are of donor type (neutral when full of electrons, positively charged when empty). When the Fermi level lines up with the neutral level, the net interface-trap charge is zero. This energy level pins the semiconductor Fermi level at the surface before the metal contact was formed. $q\varphi_{Bn0}$ is the barrier height of the metal-semiconductor contact that is overwhelmed by electrons flowing from the metal to the semiconductor. In our assumptions, the interfacial layer has a thickness of a few angstroms and is essentially transparent to electrons. The density is D_{it} [states/cm^2-eV] and is constant to the Fermi level and the interface-trap charge density on the semiconductor is then negative. D_{it} (the interface-trap density) times the energy difference gives the number of surface states above the neutral level that are full. ε_i is the permittivity of the

interfacial layer. δ is the thickness of the interfacial layer. Δ is defined in the equation below; this equation validates that the Fermi level must be constant throughout the system at thermal equilibrium. [12]

Equation 1.6 $\Delta = \varphi_m - (\chi + \varphi_{Bn0})$

From the barrier height, φ_{Bn0}, we can include the interfacial properties that have two limiting cases: (1) when the interface-trap density is infinite,

Equation 1.7 $q\varphi_{Bn0} = E_g - q\varphi_0.$

The Fermi level at the interface is pinned by the surface states at $q\varphi_0$ above the valence band. The barrier height is independent of the metal work function and is determined entirely by the surface properties of the semiconductor. When (2) D_{it} is zero, then

Equation 1.8 $q\varphi_{Bn0} = q(\varphi_m - \chi).$

This equation is identical to ideal Schottky barrier height equation where surface states are neglected. [12]

Schottky Barrier Height Measurements

Several methods are used to measure the Schottky barrier height of a metal-semiconductor contact. We will be using two in this paper: (1) current-voltage and (2) threshold voltage.

Current-Voltage Measurements

The total current density, which consists of both thermionic emission and tunneling shown in Equation 3 and for doped semiconductors, the I-V characteristics in the forward direction with $V_F > 3kT/q$ is given by:

Equation 1.10 $J = J_0 \left[exp\left(\frac{eV}{k_B T}\right) - 1 \right]$

Where the barrier height is:

Equation 1.11 $\varphi_{Bn} = \frac{kT}{q} \ln\left(\frac{A^* T^2}{J_0}\right)$

For reverse bias when $V_R > 3kT/q$, the main voltage dependence is due to the Schottky barrier lowering:

Equation 1.12 $J = A^* T^2 \exp\left[-\frac{q\left(\varphi_{B0} - \sqrt{qE_m/4\pi\varepsilon_S}\right)}{kT}\right]$

When the barrier height $q\varphi_{B0}$ is much smaller than the bandgap so the depletion layer generation-recombination current is small in comparison with the Schottky emission current, then the reverse current will increase gradually with the reverse bias mainly due to the barrier lowering effect. [12]

The I-V characteristics are shown in Figure 1.13 below with gate current (Ig) versus gate voltage (Vg). The Ig-Vg characteristics show how the gate current exponentially increases in forward bias and is small in reverse bias. This is important to determine and understand the Schottky barrier characteristic behavior of the HEMT gate.

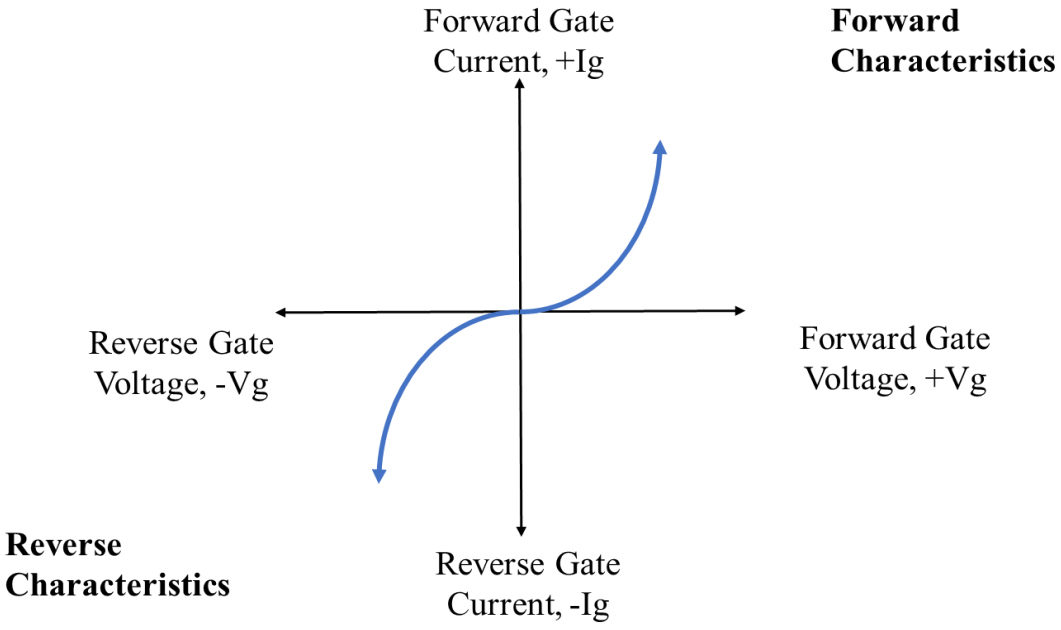

Figure 1.13: Ideal Ig-Vg characteristic curve of a Schottky junction

Threshold Voltage

The threshold voltage (V_{th}) is the turn-on voltage of the device defined by Equation 1.13 below. The threshold voltage is directly related to the Schottky barrier height, therefore, observing the threshold voltage in the electrical characteristics of the HEMT during accelerated stress, will illustrate what is happening with the Schottky barrier height.

Equation 1.13 $$V_{th} = \varphi_B + \frac{E_{F0}}{q} - \frac{qn_D d}{\varepsilon} - \frac{\Delta E_C}{q}$$

Motivation for Work

Previous InP technologies are used in hermetically sealed instruments for space and military applications. In order to determine if the new devices can be used for additional applications including for commercial uses, the IACC HEMTs will have to be tested in ambient air environments. These devices are protected with a 250 Å Si_3N_4 passivation layer. After the accelerated life tests, the passivation thickness was increased to 1000 Å to understand whether the Schottky barrier height is changed due to environmental effects. Table 1.3 lists the differences between the InGaAs technologies and the IACC HEMTs.

Table 1.3: Differences of the IACC compared to previous InP technologies

Differences from InGaAs
Uses IACC channel
Higher mobility carriers in the channel
Includes refractory metal barrier layer
Sub-50 nm gate lengths vs. 0.1 µm
G_m up to 2500 mS/mm
Epi profile scaling for the sub-50 nm gate

The difference between these IACC HEMTs and previous technologies is that the previous technologies were manufactured with an InGaAs channel. They had various degradation mechanisms that included gate sinking. The InGaAs technologies were then scaled

down in size as the maximum cutoff frequencies increased to the THz range and the active channel layer was updated to an InAs composite channel (IACC). The IACC channel has higher mobility than other InP HEMT technologies that use $In_{0.53}Ga_{0.47}As$. Increasing the percentage of indium, increases electron mobility in the channel. The IACC HEMTs also include an NGMET barrier layer that is placed between the titanium gate metal and the semiconductor. The new barrier layer is placed to decrease gate sinking. These properties provide maximum cutoff frequencies in the THz range with sub-50 nm gates and transconductances up to 2500 mS/mm. The maximum THz cutoff frequencies and the new materials open doors for new applications including for commercial uses.

Outline of the Dissertation

The objectives of this dissertation is to give a better understanding of how InAs/InP HEMTs have recently developed and what those advantages are for the future. Chapter 1 has gone into an introduction of the InP HEMT technologies and the motivation for this work. Chapter 2 will go into reliability testing of the new IACC HEMT devices and why certain experiments were chosen. Chapter 3 will give an overview of the microscopy tools chosen to analyze the IACC HEMTs and what information we were able to gather. Chapter 4 will discuss how we were able to improve these devices in air and Chapter 5 simulates the device data in TCAD Sentaurus to verify our hypothesis and results. Chapter 6 explains our conclusions and further work for this technology.

Chapter 2 InAlAs/InAs/InP Reliability Evaluation

InP HEMT Failure Mechanisms and Reliability

Reliability is the quality in the confidence of device performance. The device performance over a long period of time can be shown by accelerated life testing. The accelerated

life tests are chosen based on the types of failures that are of concern in the specific environments that the devices will be exposed to. This chapter will define the accelerated life tests that will help to expand the customer base of the HEMTs into the commercial world. In the commercial world, the devices could be exposed in an ambient air environment. In an ambient air environment, the concerns are gate sinking and oxidation. An illustration of these physical mechanisms is shown in Figure 2.1 below and how these mechanisms are induced is in Table 2.1.

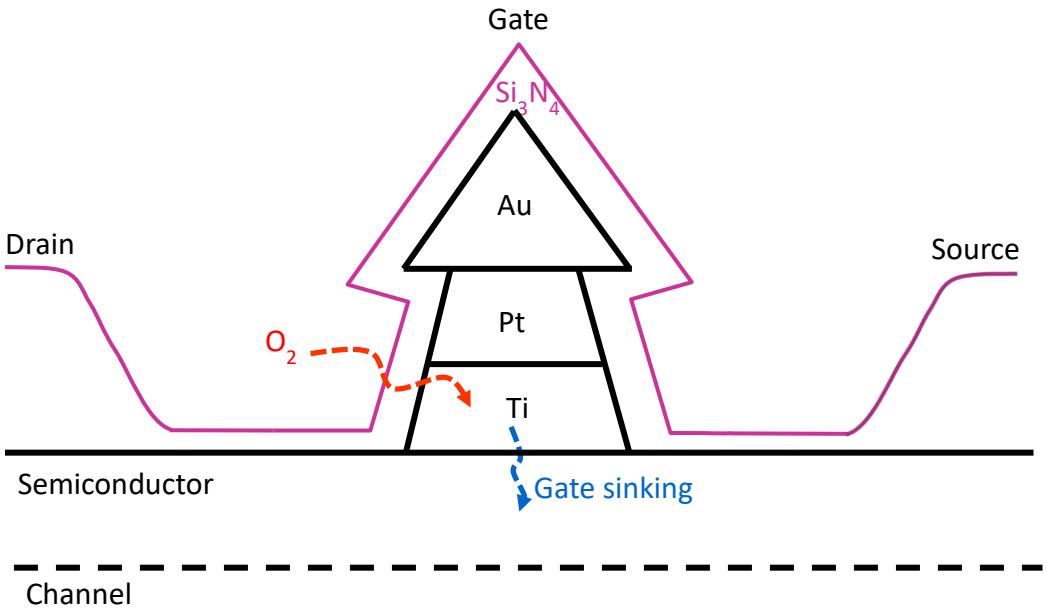

Figure 2.1 Examples of typical III-V failure mechanisms

Table 2.1 List of typical III-V failure mechanisms

Failure Mechanism	Initiation
Gate Sinking	High temp, electrical bias
Oxidation	High temp, electrical bias, ambient air environment

Since in previous technologies with titanium barrier layer exposed to an ambient air environment, gate sinking occurred and updating that barrier layer to an NGMET and exposing it to an oven-nitrogen-filled environment and found high reliability [13], these new devices with

the NGMET barrier layer will need to be exposed in ambient air environments to determine their reliability for commercial use.

The accelerated life tests chosen were based on its known conditions such as environment, temperature and electrical bias. Due to the HEMTs wide array of applications, different operating conditions were chosen, shown in Figure 2.2. First, a temperature only test was chosen to see how the device behaves without electrical bias at elevated temperatures to serve as a baseline. Then, three different electrical biases were selected: (1) a normal operating condition was tested at elevated temperatures to determine its typical behavior under electrical bias in ambient air under elevated temperatures. This mode increases the channel current and the electric field. The stresses at knee voltage and pinch-off conditions are opposite of one another: (2) the knee condition maximizes the channel current and decreases the electric field, while (3) the pinch-off condition minimizes the channel current and increases the electric field. Each of these conditions promotes the specific failure mechanisms of concern.

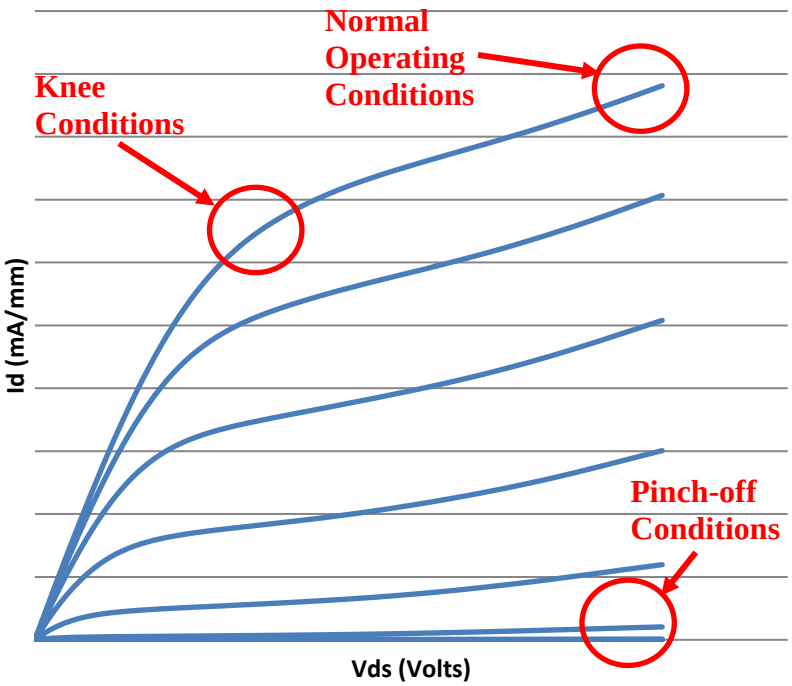

Figure 2.2 I_d-V_d curve showing the operating conditions for the accelerated life tests

Gate Sinking

Gate sinking is the interdiffusion of materials from the gate metal into the semiconductor. This sinking causes a reduction in the spacing between the metal and active channel where the electrons flow. The Ti/Pt/Au gate is known to physically sink into the semiconductor without the proper barrier and greatly degrade a HEMT DC performance. A 0.15 um Ti/Pt/Au gate GaAs PHEMT was stressed at Vds of 5.2 V and Ids of 250 mA/mm in an ambient air environment at $T_{ambient}$ of 210°C, 235°C, and 250°C. This showed gate sinking of the titanium into the AlGaAs Schottky barrier layer.

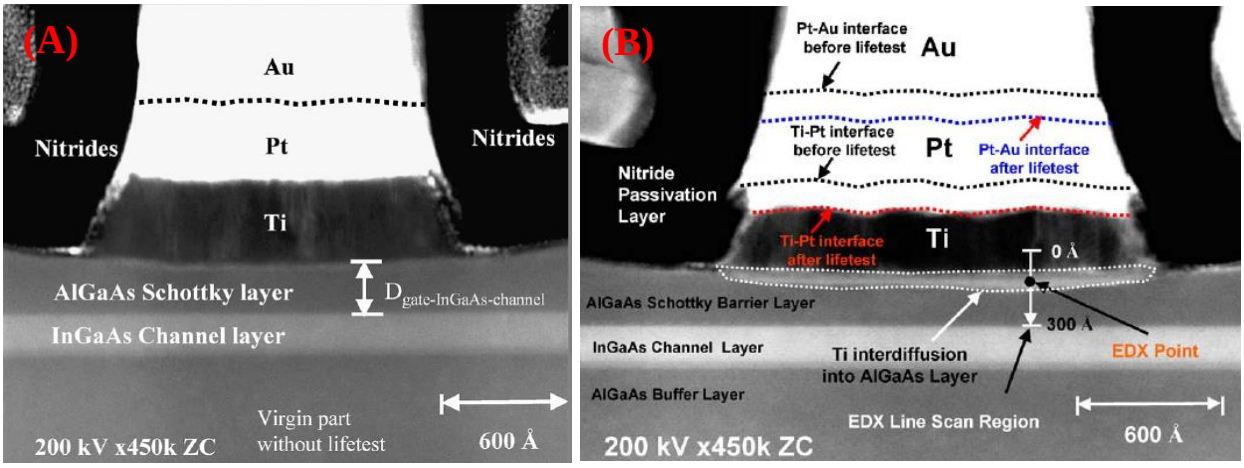

Figure 2.3 STEM image of 0.15 um InP HEMT (A) unstressed, (B) with Pt diffusion at Tchannel 235°C for 96 hours [14]

Later, a 0.1 um Pt/Ti/Pt/Au gate was used on an InAlAs/InGaAs/InP HEMT. The devices were subjected at $T_{channel}$ of 220°C and 235°C with V_{ds} at 1.5 V and I_{ds} at 150 mA/mm [9]. These devices showed Pt diffusing into the InAlAs Schottky barrier layer with transconductance increase (Gm) and positive threshold voltage (Vth) shift, shown in Figure 2.4.

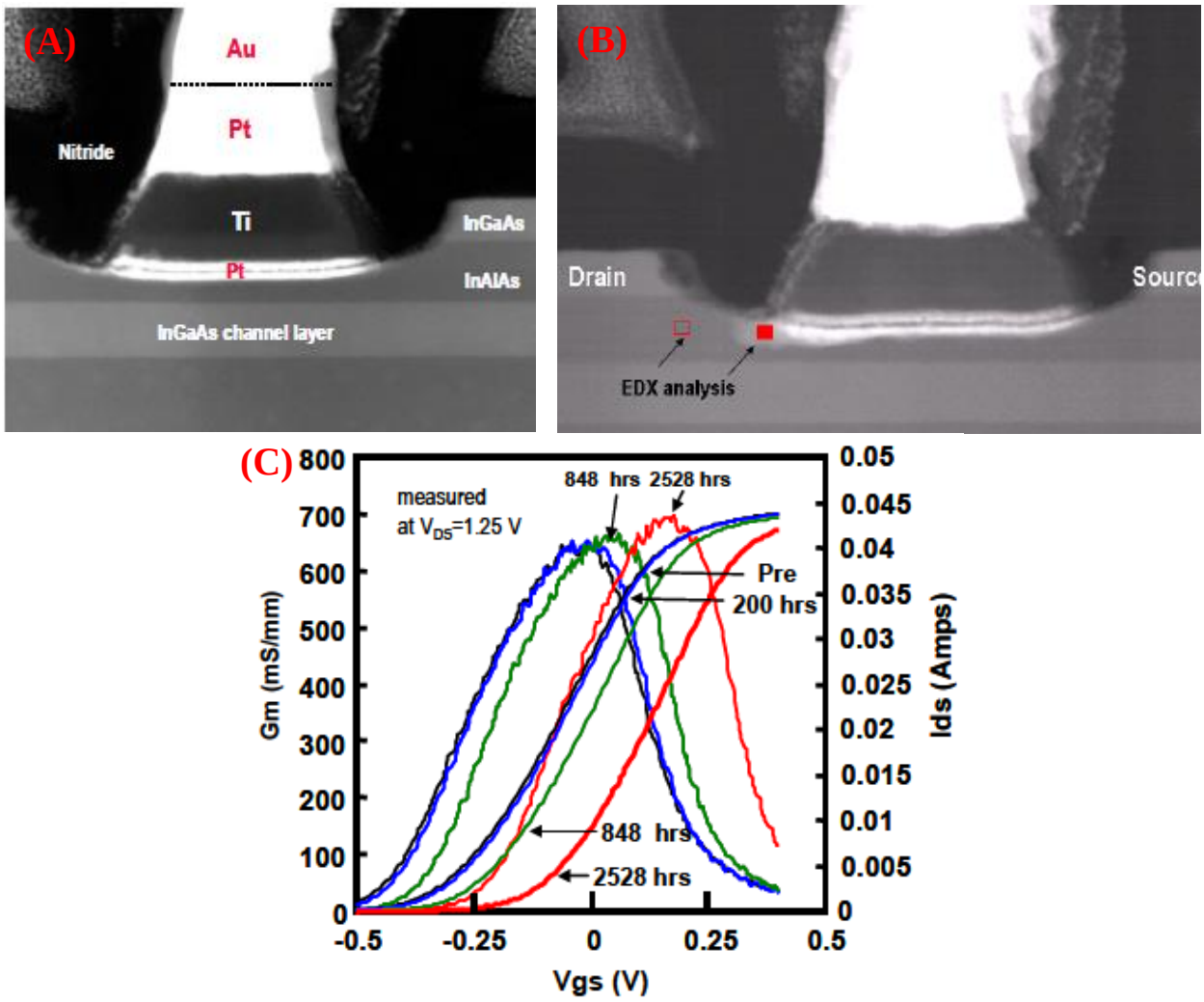

Figure 2.4 STEM image of 0.1 um InP HEMT (A) unstressed, (B) with Pt diffusion at Tchannel 220°C for 2528 hours, (C) positive shift in Gm and Vth [9]

The improvement of this degradation mechanism was to use a New Gate Metal Electrode Technology (NGMET) refractory metal [10], instead of the Pt-sunken gate, which showed to alleviate the Schottky junction degradation in a nitrogen-filled oven. This research continues to thoroughly investigate the reliability of this new gate metal in an ambient air environment.

Accelerated Life Tests

Temperature Acceleration

A temperature stress was first conducted to serve as a baseline without electrical stress. The IACC HEMT wafers were placed on a hot chuck instrument in ambient air at 175°C without

electrical stress. The electrical plots measured included the transconductance (G_m), maximum drain current (I_{dmax}), gate leakage current (I_g) and I_d-V_d curves (DCIV).

Typical Operating Conditions

In previous papers, gate sinking occurred at high temperatures with high electric fields and high current densities. Therefore, one of the electrical accelerations was done at 175°C with V_{ds} at 1.0 V and I_{ds} at 300 mA/mm.

Electric-field Acceleration

The electrical acceleration test labeled as pinch-off stress was done at a high electric-field and low current density. These stresses were completed with Vds at 1.0 V and Ids at 0.9 mA/mm. When enough of an electric field is induced in a HEMT, the electrons traveling through the high electric field will gain enough energy to undergo scattering events with bonded electrons in the valence bands. The excess energy will transfer to an electron which is lifted into conduction band creating a new electron-hole pair. This second electron-hole pair can also have high enough energy to continue creating additional electron-hole pairs. This can either create an Avalanche breakdown, in which, more and more carriers are generated and multiplication results in thermal runaway and carrier density increases or impact ionization where the electron-hole pair is separated by the electric field and the holes close to the gate contact are trapped. This causes a negative shift of the threshold voltage [15]. Increasing the electric field can also cause a positive shift in the threshold voltage and increases the drain resistance due to the generation of surface traps between the SiN passivation layer and the semiconductor between the gate and drain [16].

Current-induced Acceleration

The HEMTs were also induced by high current densities and low electric-field. The purpose of this test was to understand if the effects we see are exacerbated by the electric field or

the current density. The current induced stress was completed at Vds of 0.3 V and Ids at 450 mA/mm.

Reliability Parameters

Depending on how certain characteristics behave, it is telling on what is physically happening to the device. The electrical plots monitored in this research include the DCIV curves, maximum peak transconductance (Gmp), threshold voltage (Vth) and maximum drain current (Idmax). With the DCIV curves, we are looking at the initial linear slope which is calculated and labeled as Ron. These parameters will help us try to understand what might be happening to the device and what physical features we should be looking for.

As previously stated, transconductance was one of the parameters measured during the accelerated life tests. Transconductance is defined as the gain of the device, which is the change in output drain current over the change in input gate voltage:

Equation 2.1 $G_m = \frac{\partial I_d}{\partial V_{gs}}$.

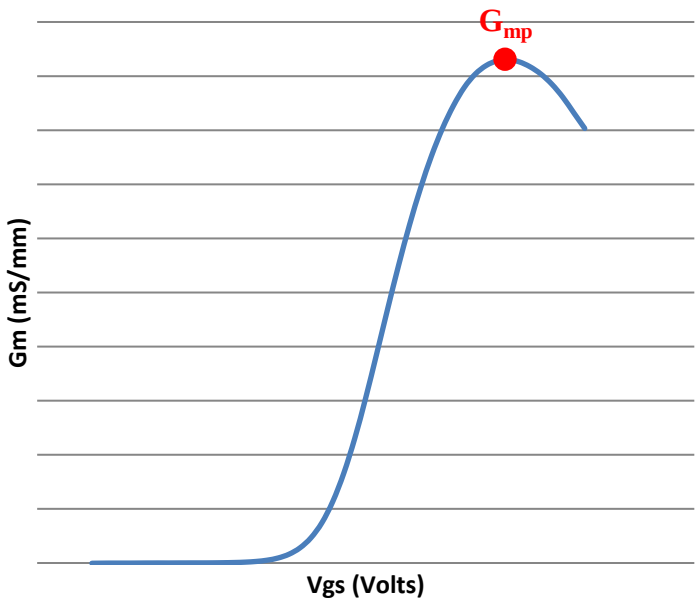

Figure 2.5 G_m-V_g curve showing G_m peak

G_m is related to the distance between the gate metal and the channel, gate width (W) and the electron's saturation velocity (v_{sat}) by the following equation [17]:

Equation 2.2 $G_m \sim \frac{\varepsilon v_{sat} W}{d}$

The gate sinking failure mechanism decreases the distance between the gate metal and the channel, therefore, increasing the transconductance value.

The threshold voltage (V_{th}) is when the device turns on; it is the minimum voltage at which conduction happens. The V_{th} equation is defined in Equation 1.13 [17], where φ_B is the Schottky barrier, E_{F0} is the Fermi level at zero 2DEG density, q is the electron charge, n_D is the ionized donor charge, d is the distance between the gate metal and the channel, ΔE_C is the conduction band discontinuity of the heterojunction and ε is the dielectric constant. If φ_B changes, that will directly affect V_{th}. V_{th} is determined by extrapolating the Id-Vg curve.

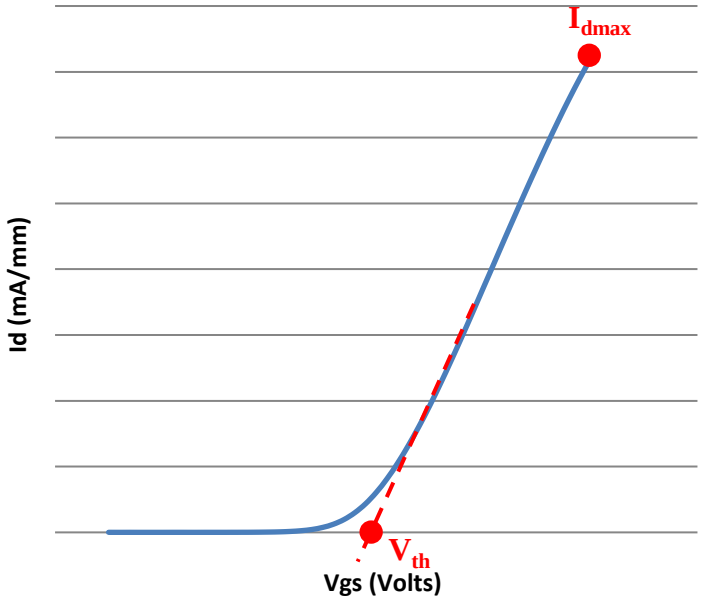

Figure 2.6 Source-to-drain current versus gate-to-source voltage plot determining threshold voltage (V_{th}), maximum drain current (I_{dmax}); I_d at V_d = 0.5 V

The DCIV curve will show lots of information regarding the behavior of the device. The parameter we are focusing on is Ron. The wafer on-resistance (Ron) is the transistor resistance

and is built up of several components: the source and drain resistances, and channel resistance (Equation 2.4):

Equation 2.4: $R_{on} = R_{source} + R_{drain} + R_{channel}$

As previously stated, if the drain resistance increases under the electric field stress, this could be due to the traps increase between the passivation layer and the semiconductor or between the gate and the semiconductor.

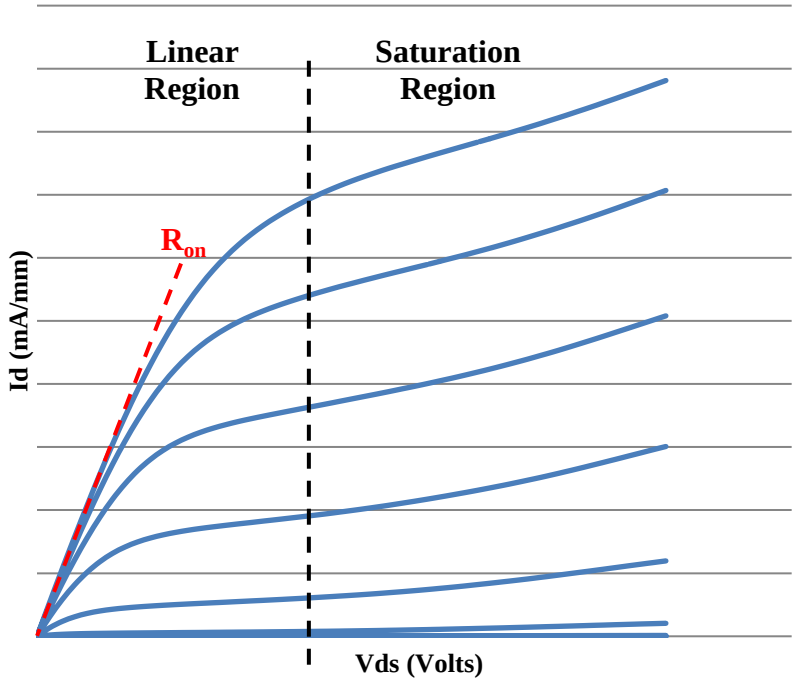

Figure 2.7 DCIV curve showing R_{on}

Hot Chuck System Evaluations

The hot chuck system is used for device characterization in air. It is a thermal chuck with a probing station to heat or cool a wafer during electrical testing. The hot chuck used in this paper is a Cascade Microtech with a Temptronic temperature controller. The top surface of the chuck has vacuum holes to stabilize the wafer during testing and probes to bias the devices as the temperature changes.

Experimental

Four experiments were chosen to verify the reliability of these devices. First, a temperature only lifetest was completed to see how increasing temperature affects the InP HEMT; the devices were annealed at 175°C without electrical bias stress. Then, electrical bias was taken into consideration in addition to increasing temperature. The next group of experiments were done at 175°C at three different electrical bias stresses: (1) typical operating conditions at V_d = 1.0 V, I_d = 300 mA/mm, (2) pinch-off at V_d = 1.0 V, I_d = 0.9 mA/mm, and (3) knee voltage at V_d = 0.3 V, 450 mA/mm. All devices were subjected in a laboratory air environment.

The temperature stress was used to see how the HEMT behaves with thermal acceleration only before taking electrical bias into consideration. Stress under typical acceleration is used to identify how the device works with higher temperature as it is turned on. Biasing the HEMT into pinch-off reduces the channel current by injecting the electrons in the gate into the empty surface states that maintain the 2DEG, and reduces the 2DEG [18]. This decreases the current and increases the electric-field. Stress at the knee voltage is at high current and low electric-field. Each of these experiments determines the behavior of the HEMT devices at various operations to further identify its failure mechanisms.

Results

The Ig-Vg curves in Figure 2.8 show the IACC technology before and after temperature stress; (A) Ti/Pt/Au gate without a metal barrier layer, (B) with the new NGMET material. Figure 2.8A shows an increase in gate current leakage, compared to the HEMT with the NGMET, in both the reverse and forward bias. In Figure 2.8B, the two curves almost identically overlap. This supports the data shown in [9] where gate sinking has been reduced. This also

shows that the device, even at higher temperatures in an ambient air environment, is more stable than the Ti-gate.

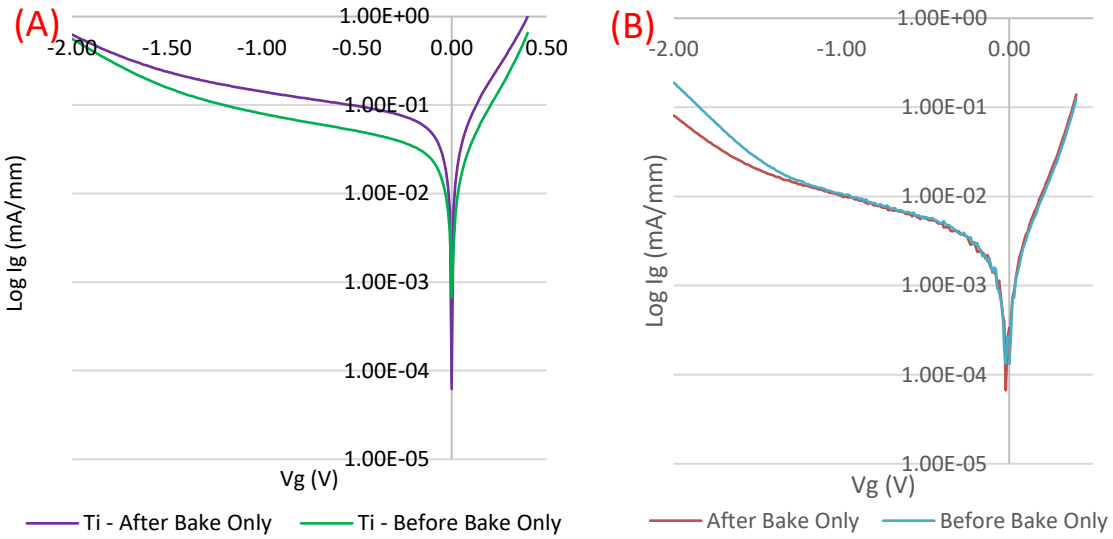

Figure 2.8 (A) I_g-V_g curve of Ti-metal-gate HEMT before temperature stress and after; (B) I_g-V_g curve of refractory metal-gate HEMT before temperature stress and after

The other three life tests I_g-V_g curves compared to the temperature stress are shown in Figure 2.9.

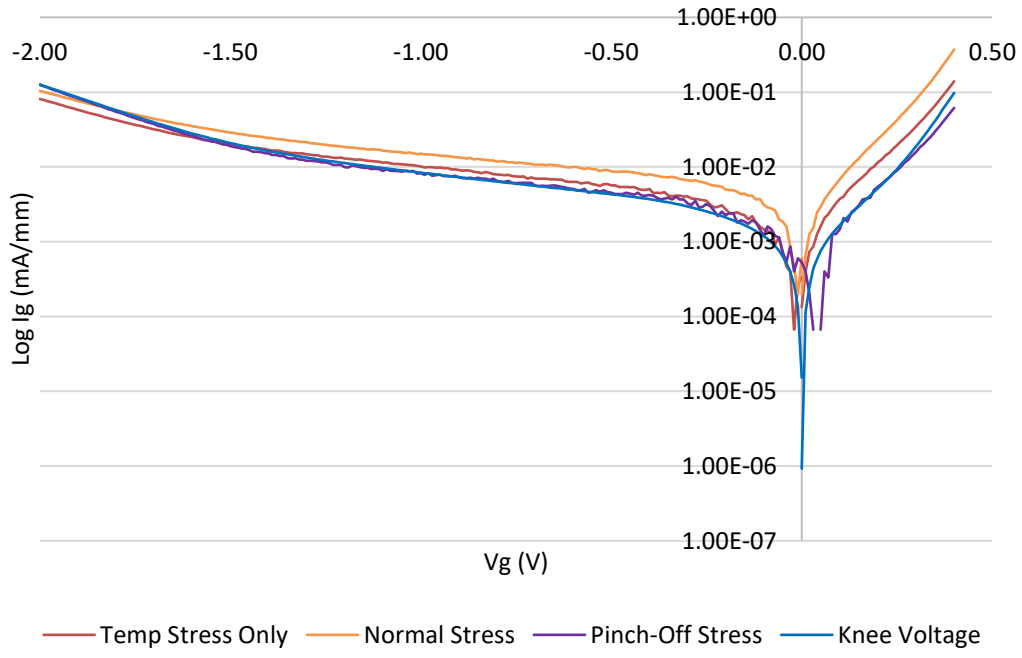

Figure 2.9 I_g-V_g curves of refractory metal-gate HEMT after temperature (blue), typical (pink), pinch-off (orange) and knee voltage stress (brown)

Table 2.2 Percent change of Ig

Stress	ΔIg%
Temperature	-8.3
Pinch-off	-75.1
Knee Voltage	-29.5
Normal	-46.1

The gate leakage current of the pinch-off and knee stresses are very similar to each other in both reverse and forward bias. The temperature only stress increases in Ig leakage slightly, a little more in the forward bias. The typical operating condition at elevated temperature is at an even higher Ig. Even though the Ig leakage increases slightly, it does not increase not even an order of magnitude. This shows the stability of the NGMET technology and the gate over time at various electrical biases in an ambient air environment.

Transconductance (Gm) curves are shown below in Figure 2.10. These curves show Gm decreasing and moving in a negative gate voltage direction, except for the pinch-off life test where Vg shifts positively. Equation 2.2 above shows the relation between Gm and the distance (d) between the gate metal and the channel. The equation shows as Gm decreases, d increases, which is what happened in our plots. Therefore, according to Equation 2.2, since Gm decreases and the gate metal and channel is increasing, gate sinking is probably not a failure mechanism degrading these HEMTs. The distance, d, would decrease if gate sinking was a mechanism because the gate metal would sink into the semiconductor and it would be at a closer distance from the channel. So far, there is no electrical parameter indicating that gate sinking is occurring.

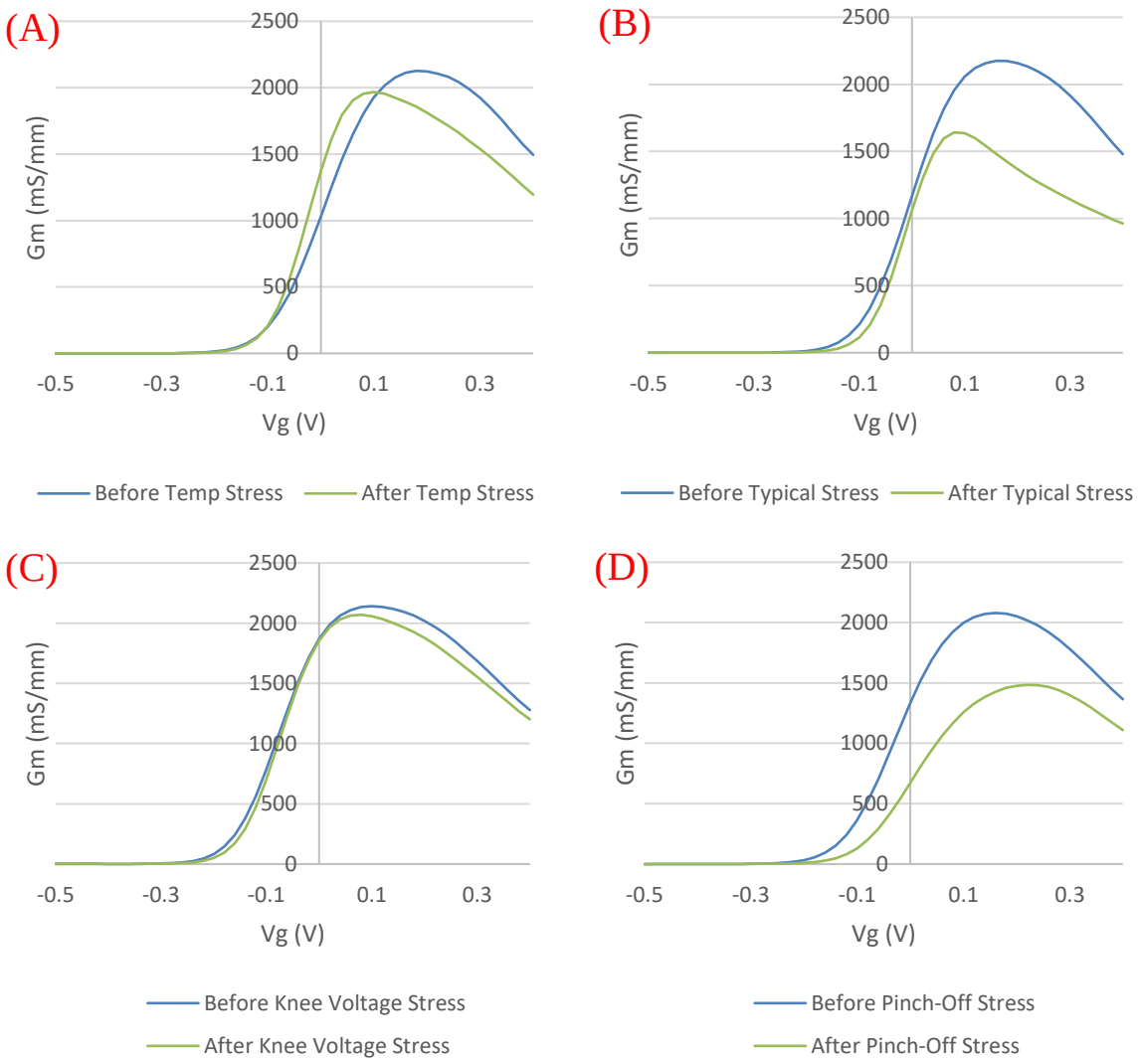

Figure 2.10 G_m at V_d = 1.0 V before and after (A) temperature, (B) typical operating conditions, (C) knee voltage and (D) pinch-off life tests

Table 2.3 Percent change of Gm

Stress	ΔGm%
Temperature	-3.8
Pinch-off	-27.5
Knee Voltage	-5.6
Normal	-38.5

The transfer curves, Id-Vg, were measured and are shown in Figure 2.11. This is the maximum drain current as gate voltage is increased. Again, a higher percentage decrease of Idmax after the pinch-off stress than after the other life tests. The extracted Vth, in Figure 2.11,

taken at the intercept of the gate voltage of the linear extrapolation of the drain current, was found after each stress condition [19]. The life tests show that Vth shifts positively after each accelerated life test; however, stays the same after temperature only stress. Similar thermal results were shown in the AlGaN/GaN HEMT in [19]. A positive Vth is attributed to electrons being injected and trapped into the barrier layer from the 2DEG due to tunneling. When Vth decreases, the gate voltage is high and holes are injected and gate leakage increases [11]. This is consistent with our experimental Ig leakage curves in Figure 2.7. Summary tables in Tables 2.2 and 2.3 show the Vth percent change along with Ig. They are consistent with each other, which was expected since they are both related to the Schottky barrier height.

Looking back at Equation 1.13, Vth is directly related to the Schottky barrier height. The Schottky barrier height is also related to the work function of a material in Equation 1.1. The work function changes due to material changes. There might be another type of diffusion or the potential change across the interfacial layer and the occupation of the interface states as a result of the applied forward voltage [18]. The plots show that the pinch-off stress has the most effect on the HEMT behavior, which directs us to believe the failure mechanism is induced by a high electric field than a high current.

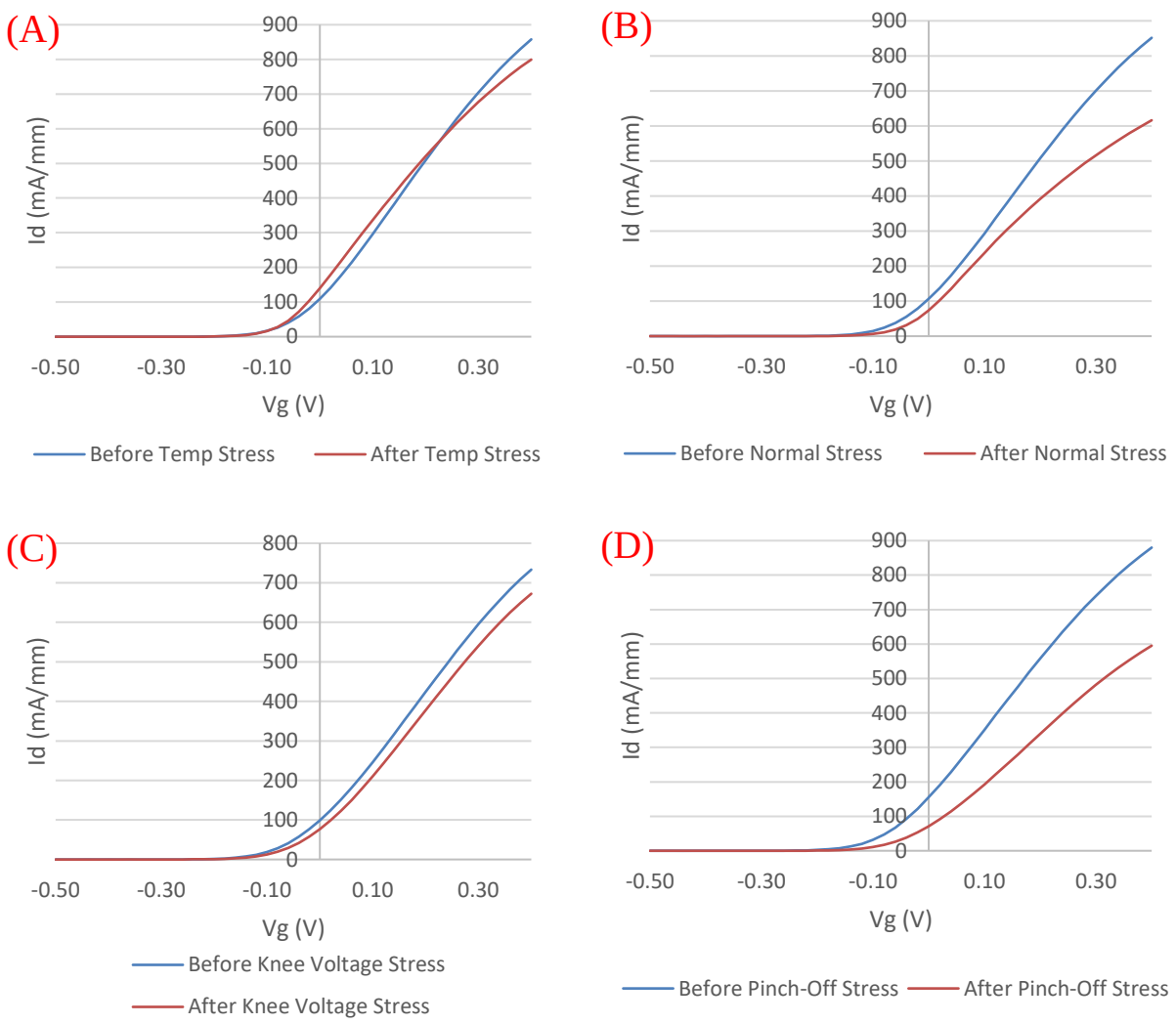

Figure 2.11 Transfer curve I_{dmax} at V_d = 1.0 V before and after (A) temperature stress, (B) typical operating conditions, (C) knee voltage stress, (D) pinch-off stress

Table 2.4 Percent change of Idmax and Vth

Stress	ΔIdmax%	ΔVth%
Temperature	-4.5	0
Pinch-off	-34.8	-28.6
Knee Voltage	-8.3	-20
Normal	-40.3	-60

Direct-current (DC) I-V curves were generated in Figure 2.12 below. These curves also show the greatest degradation under pinch-off stress when looking at the slope of the linear region of the curves, Ron.

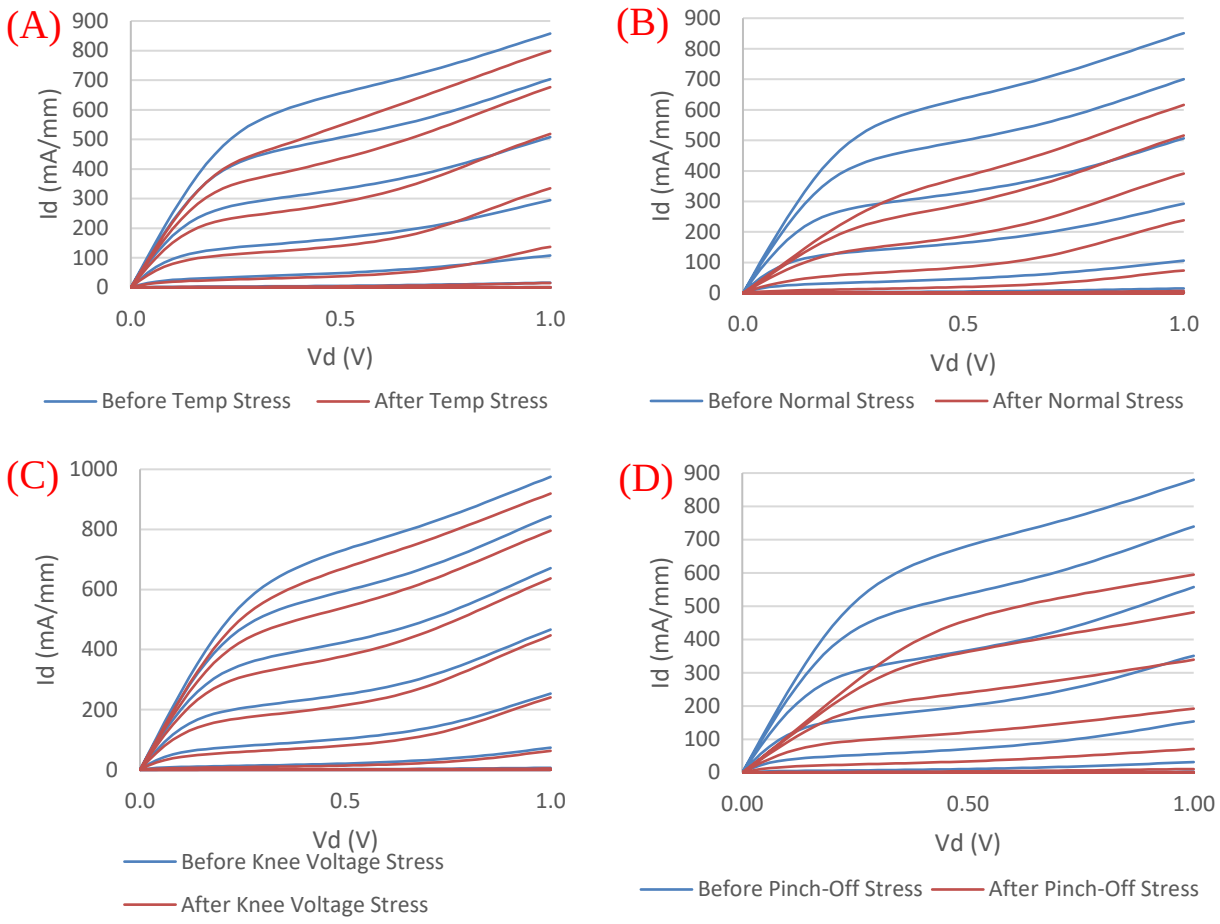

Figure 2.12 DCIV curves before and after (A) temperature, (B) typical operating conditions, (C) knee voltage and (D) pinch-off stresses

R_{on} was calculated at V_g 0.4 V as the slope in the linear region of the DCIV curves, where $R_{on} = I_d/V_d$. According to Table 2.4, R_{on} increases by 124.1% after pinch-off stress whereas it only increases by 7.8% after knee voltage stress. With an increase in on-resistance, this indicates an increase in the contacts resistances, channel resistance or both.

Table 2.5 Percent change of Ron

Stress	ΔRon%
Temperature	0.7
Pinch-off	124.1
Knee Voltage	7.8
Normal	135

The plots above show that the pinch off stress decreases the HEMT electrical characteristics degradation faster than under the knee voltage stress. Therefore, we can conclude that with a higher electric field, the higher degradation of the electrical behavior. To determine the physical and chemical features of the HEMT after the increased electric field, the devices were cross-sectioned at the gate.

Chapter 3 Microanalysis Characterization of InAlAs/InAs/InP

Scanning Electron Microscope/Focused Ion Beam (SEM/FIB)

The electron microscope was invented by Max Knoll and Ernst Ruska in 1931 [Tim Palucka, Early History of Electron Microscopy, Caltech]. In 1965, the first commercial Scanning Electron Microscope (SEM) was introduced. The SEM is used to look at small samples and features that cannot be seen by a light microscope. It uses an electron beam which scans focused beam of electrons on a sample and creates an image. This image will reveal information regarding the surface topography and composition of the sample. The main components of a SEM include:

- Electron gun: includes condenser lenses, apertures, scan coils, and objective lens
- Vacuum electron column with electromagnetic lenses
- Electron detector
- Sample chamber
- Computer and display to view images.

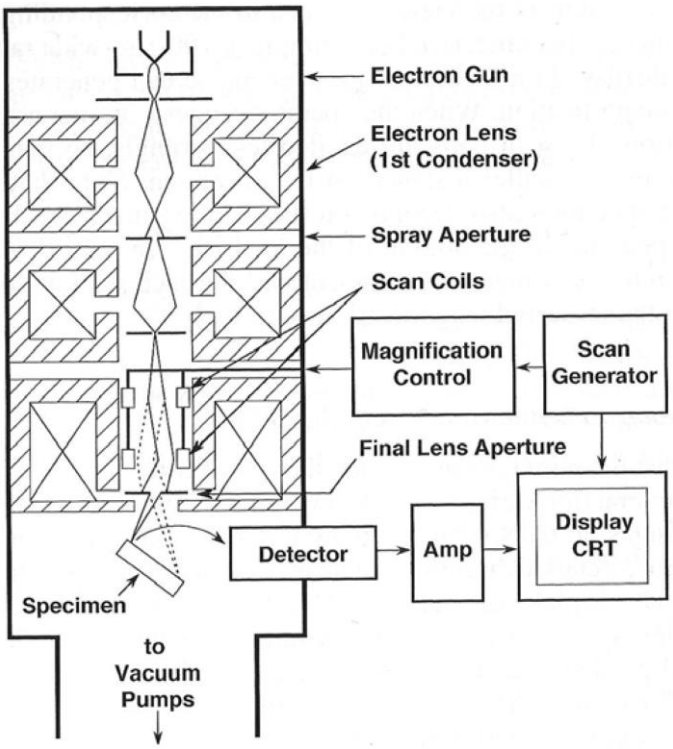

Figure 3.1 SEM schematic drawing

The electron beam of the SEM comes from a thermal field emission source with a chosen accelerating voltage. An aperture, condenser and objective lens are selected and the beam is focused with magnetics coils. The beam hits the surface of sample and an interaction volume goes into the surface a few micrometers depending on the accelerating voltage. Figure 3.2 below shows the interaction volume that goes into the surface at a 20-kV accelerating voltage.

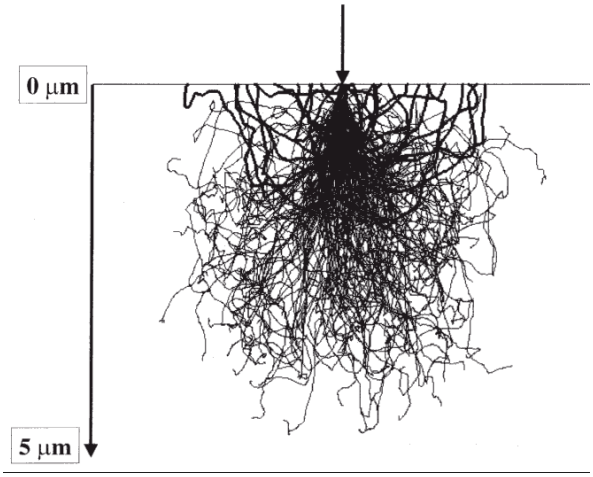

Figure 3.2 SEM interaction volume into a sample surface at a 20 kV accelerating voltage [19]

The SEM used in this research is combined with a Focused Ion Beam (FIB). The FIB is similar to a SEM except it uses an ion beam instead of electrons in order to remove material. With the combination of the SEM, the operator can view the sample as the material is removed. The FIB can be used for various operations, but in this work, the FIB was used to create cross-sections of the HEMT and the Scanning Transmission Electron Microscope (STEM) was used to look at the HEMT layers. It was important to see the layers of the HEMT before and after life testing to see how the materials physically and chemically reacted inside the device.

Figure 3.3 FEI Quanta 3D FEG SEM/FIB of IMRI

In order to analyze the device in the STEM and to see the details of the layers, the sample must be carefully prepared and thin enough, approximately 80 to 100 nanometers thick for this project, for the electron beam to transmit electrons through the material. The FIB uses a gallium ion source to mill away material and prepare the sample with nanometer precision. In order to create a thin cross-sectional sample of our area of interest, chemical vapor deposition (CVD) injects an approximate 1-3 micrometers of platinum gas to protect our area of interest. Figure 1 below shows SEM images from the top of the HEMT. This particular device included a gold airbridge which acted as a protectant of the gate fingers, which in turn, helped us to skip the platinum vapor deposition step. However, with other samples without the airbridge, a platinum layer was first placed before milling the sample. Next, two trenches are created by milling material on either side of the area of interest and to expose the sample. Then, three J-shaped cuts are created under the sample, a probe comes in and attaches to the edge of the sample by CVD and then one

final cut is made to remove the cross-sectioned sample from the HEMT. The probe then attaches the sample to a copper grid to continue thinning and polishing. At this point, the sample is approximately 1 micrometer in thickness. The thinning process continues to reduce the thickness of the sample; however, it is very difficult to thin the sample uniformly and without damaging the area of interest. With a homogenous material, you may be able to damage some of the area of interest without completely ruining it. However, with a semiconductor, there are very specific features that just cannot be damaged in any way. The operator must be as precise as possible and the ion beam can easily damage your sample and create amorphous layers where nothing can be seen. Therefore, another instrument called the Nanomill can continue polishing the sample and removing the amorphous layers to create a very thin, uniformly polished sample.

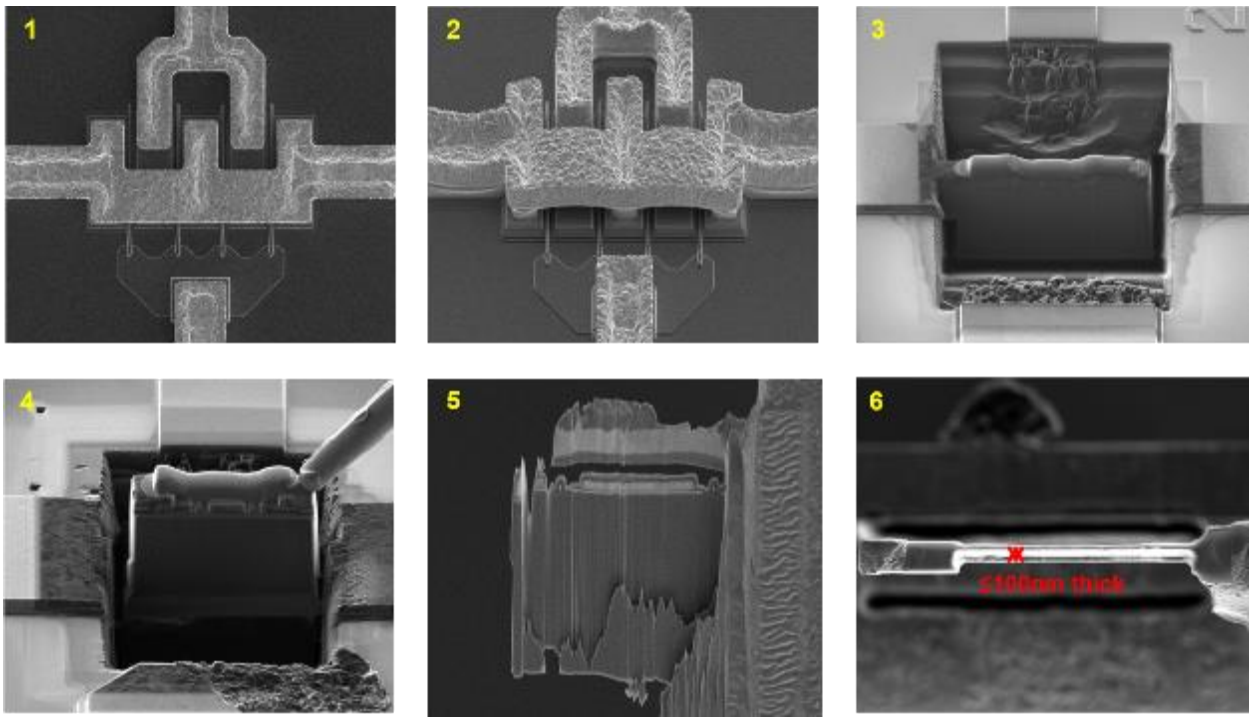

Figure 3.4 SEM images of FIB steps

Nanomilling

The Fischione Nanomill 1040 assists in preparing STEM samples for post-FIB processing and conventionally prepared specimens. The Nanomill also uses an ion beam similar

to the FIB, however, it's targeted with a beam size as small as 1 micrometer and it allows specimens to be prepared without amorphization, implantation or redeposition, unlike the FIB.

For the HEMT sample, an accelerating voltage of 700 eV for 20 minutes was used twice for a coarser polish. Then, 300 eV for 10 minutes was used for a fine polish of the sample site. Figure 2 below shows an image that is generated by the ion-induced secondary electrons from the targeted area of the specimen.

Figure 3.5 Ion image of nanomilled sample

Scanning Transmission Electron Microscope/Energy Dispersive Spectroscopy

The STEM/EDS was used to identify the physical and chemical changes of the access region under the HEMT gate. The STEM uses the concepts of the Scanning Electron Microscope (SEM) and the Transmission Electron Microscope (TEM). The STEM includes an electron beam

with scan coils which scans the surface and includes brightfield (BF) and annular dark field (ADF) detectors. The BF detector intercepts the transmitted beam and the dark field detector surrounds the transmitted beam to collect scattered electrons. Figure 3 below shows a schematic diagram of the main components of a STEM [20].

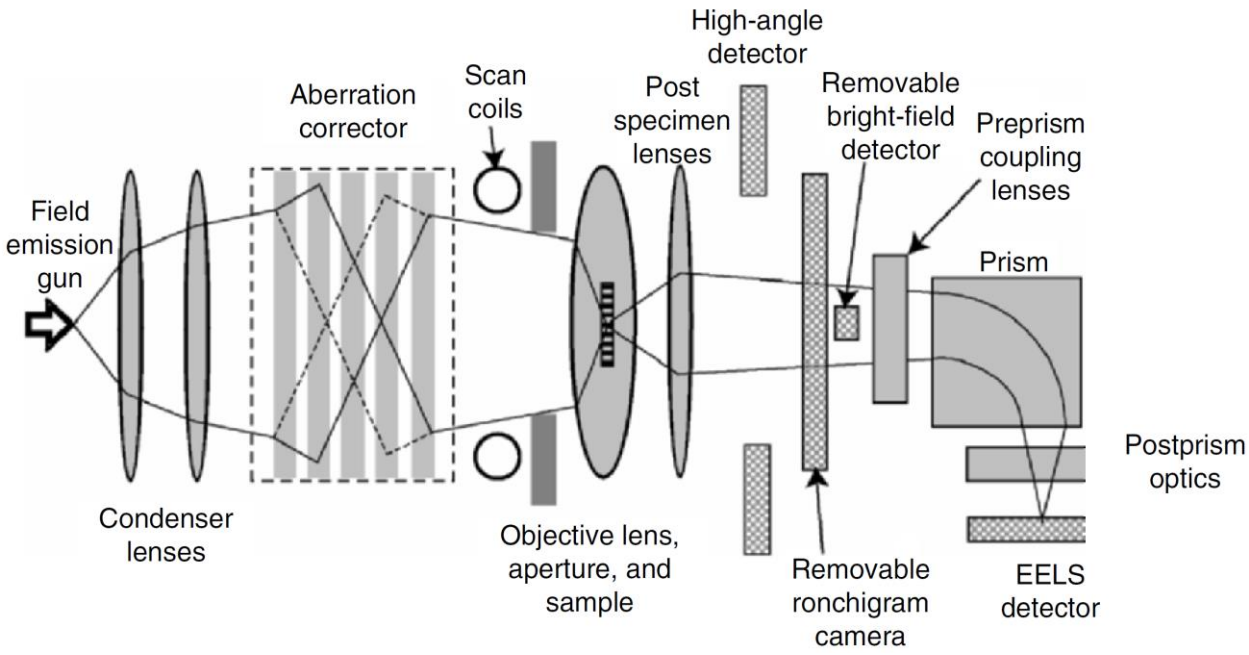

Figure 3.6 Schematic diagram of a STEM

The electron beam in the STEM transmits through a thin sample and looks at those beam electrons transmitted by the sample. The advantage of the STEM over the TEM is that it can be used other signals including secondary electrons, scattered beam electrons, characteristics X-rays and electron energy loss. The advantage of the STEM over the SEM is the improvement in special resolution due to the decreasing electron wavelength where atomic configurations can be seen. A bright field (BF) detector includes the transmitted beam and the holes appear bright. The dark field (HAADF) detector excludes the transmitted beam and the holes appear dark [20].

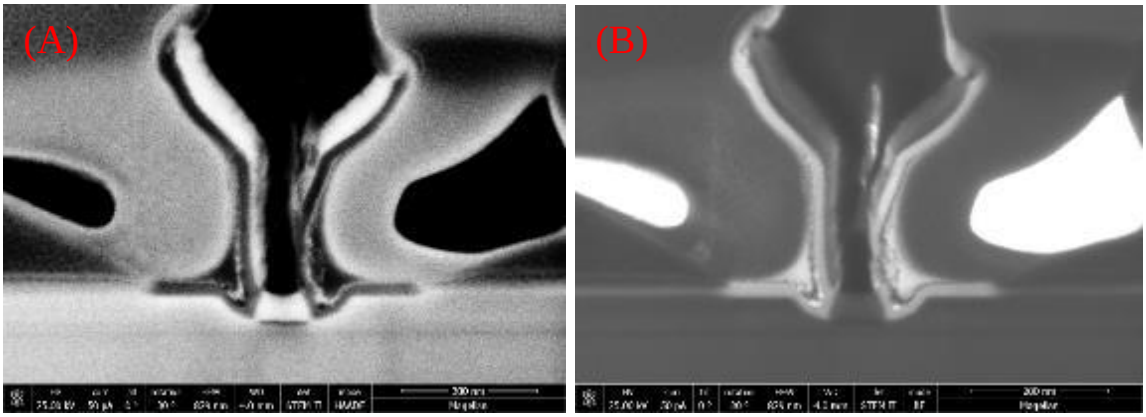

Figure 3.7 (A) Examples of a STEM-HAADF image and (B) STEM-BF image

A vast amount of time is put into sample preparation to get the sample thickness 100 nanometers or thinner to see the atomic-range features. If the sample is not prepared properly, the features are blurred and it is back to thinning the sample in the FIB or Nanomill. Figure 3.8A below shows how the sample was not properly prepared to see the important features under the gate. It is impossible to see if any metals diffused into the semiconductor or if the gate metal stacks had physically changed in any way. Once the sample was properly polished, Figure 3.8B below shows how it is clear if there were physical changes to the gate metal stacks and the semiconductor.

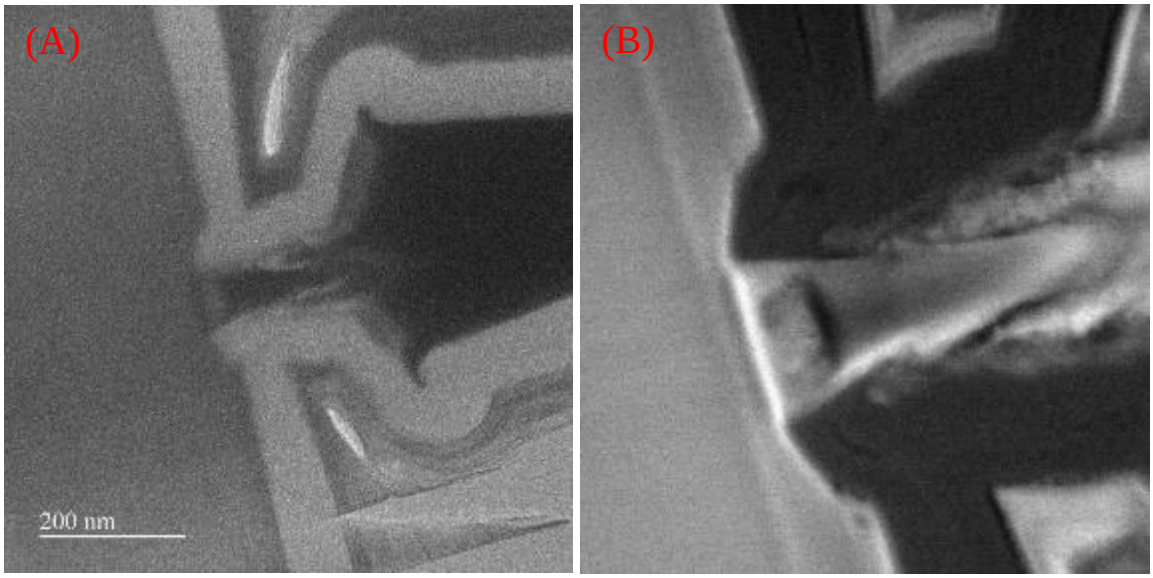

Figure 3.8 (A) STEM image of HEMT gate after nanomilling once; (B) STEM image of HEMT gate after nanomilling twice

Energy Dispersive Spectroscopy (EDS) helps to chemically identify materials. An EDS spectrum is generated based on the x-ray energy of electrons. As a beam of electrons hits the sample surface, it can collide with another electron, and with enough energy, can remove the electron from its orbit, shown in Figure 3.9. An electron vacancy appears and an electron from an outer electronic layer with higher energy will fill it. As this electron with higher energy fills the vacancy to a lower energy, the electron loses energy by emitting an X-ray. The X-ray emitted value is characteristic for each element, shown in Figure 3.10 [21].

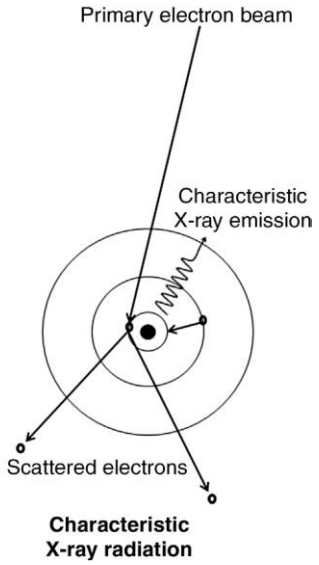

Figure 3.9 Schematic diagram of characteristic X-ray radiation

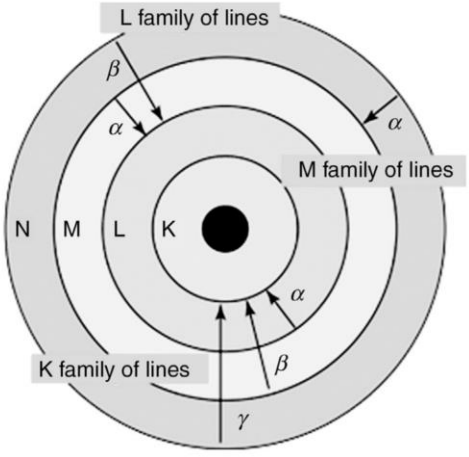

Figure 3.10 Schematic diagram of how an atom behaves in EDS [21]

Results

The results of the STEM/EDS analysis were surprising. Since the pinch-off conditions showed a higher electrical parameter degradation than under current-induced, it should show the worst-case scenario with the most physical changes. Therefore, STEM images were taken of an unstressed device and after the pinch-off stress, shown in Figures 3.11A and 3.11B, respectively.

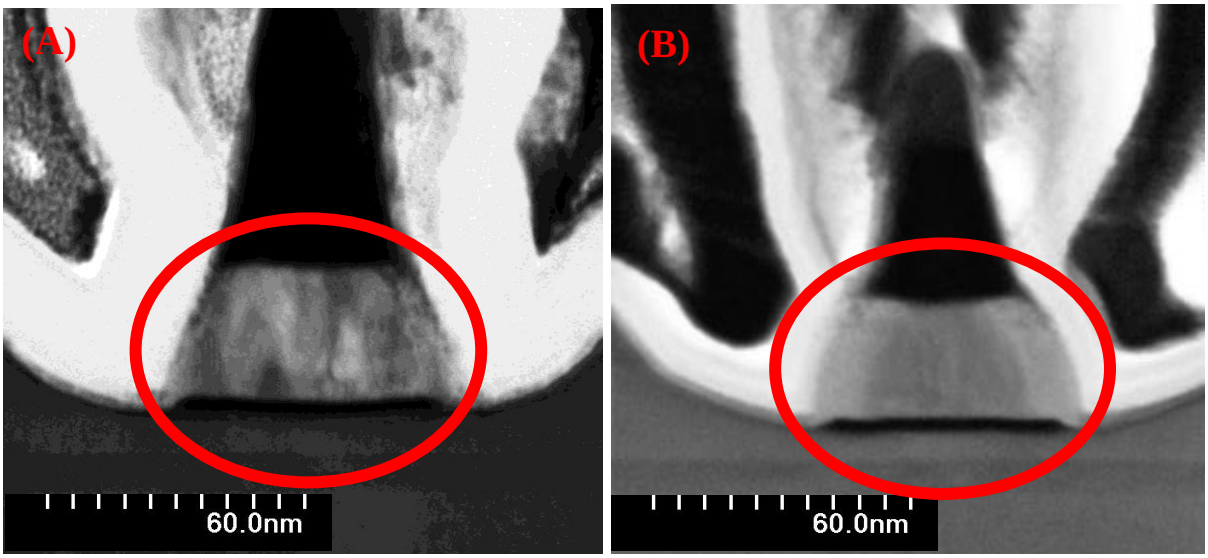

Figure 3.11 (A) STEM image of an unstressed IACC HEMT; (B) STEM image of IACC after pinch-off conditions

The STEM images of the IACC HEMTs show that there is no gate sinking occurring which confirms that that the NGMET refractory metal is preventing the gate sinking failure mechanism to happen. The electrical characteristics showed the prevention of gate metals into the semiconductor and the STEM images confirm that; we continue to see this deterrence after stressing under the normal operating conditions. Even with a high electric field, gate sinking still does not happen in ambient air. This shows that the new NGMET refractory metal is doing its job and we found the right barrier layer for this device.

The other issue was to find out what other failure/degradation mechanism is degrading the device if it is not gate sinking. EDS was taken of the gate metal and the semiconductor to see

if there was a chemical change to the materials because it cannot necessarily be seen. EDS of the inner and outer areas of the titanium were taken because the titanium looks lighter in the STEM on the outer edges of the titanium and darker inner of the titanium.

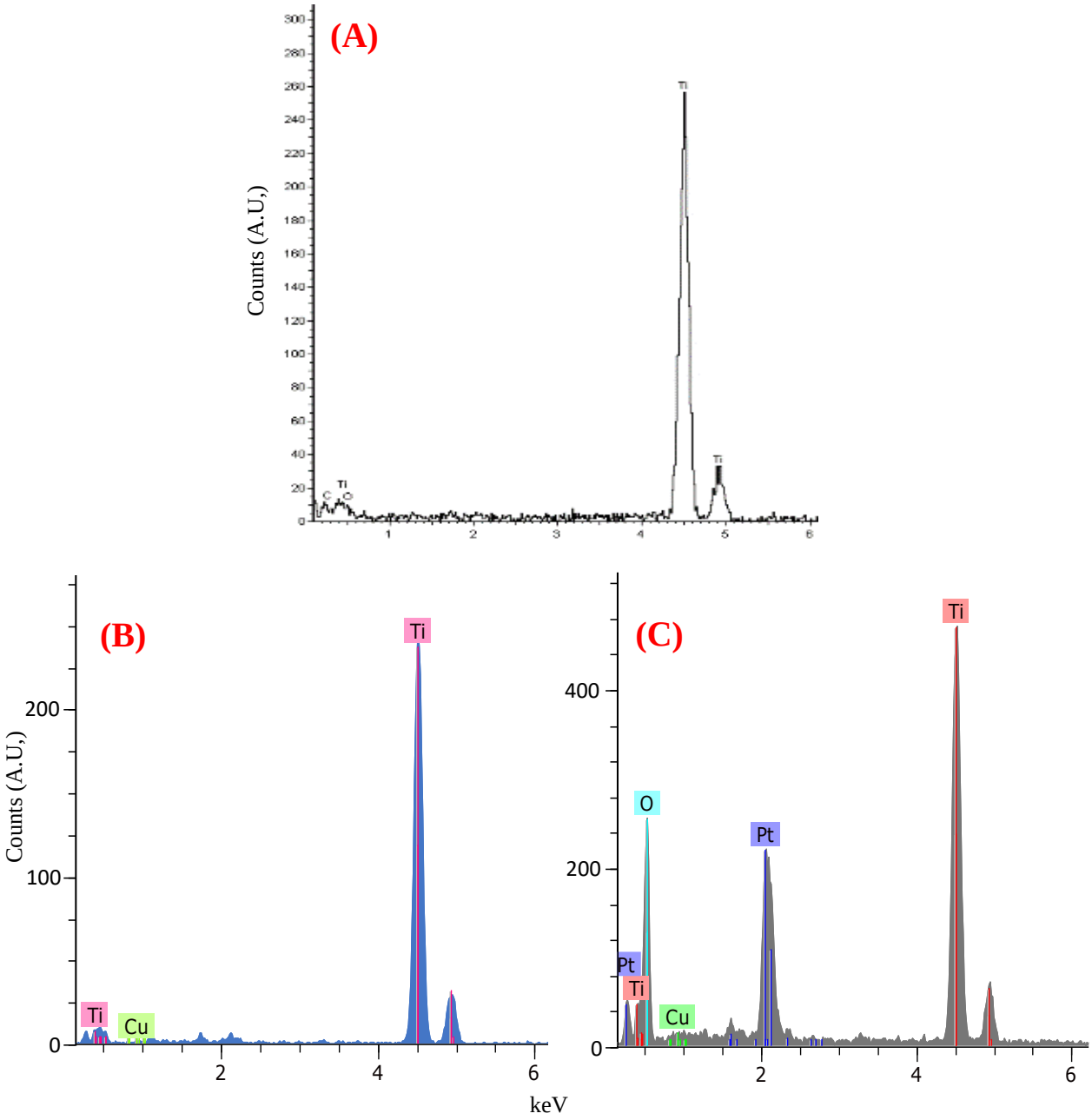

Figure 3.12 EDS spectrum of the (A) outer edge of titanium in unstressed device (B) inner and (C) outer titanium gate metal

The EDS spectra in Figure 3.12 show a higher concentration of oxygen on the outer edges of the titanium than the inner. This shows that the Si_3N_4 is porous enough to allow oxygen

atoms to diffuse all the way into the titanium gate metal. Figure 3.13 below shows that oxygen did diffuse into the Si_3N_4 passivation layer. With the higher degradation rate of the devices under higher electric fields,

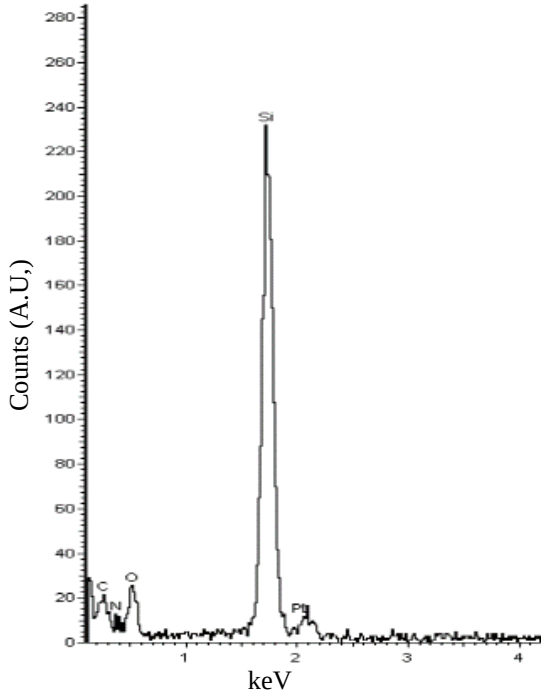

Figure 3.13 EDS spectrum of Si_3N_4 with oxygen diffusing through the passivation layer

Chapter 4 Improvement of IACC HEMTs

Silicon Nitride (Si_3N_4) Passivation

Silicon nitride has shown to be a necessary mtaerial of the InP HEMT [22]. It is an insulator which protects the HEMT from external damage and the environment [23], [24], [25], [26]. As shown from the results of this paper, a 250 Å Si_3N_4 could be too thin in an ambient air environment under high electric fields, predicting impact ionization and oxygen diffusion as failure mechanisms. However, these devices are not gate sinking and the NGMET has proved to be a reliable barrier layer for this technology even in ambient air environments.

Since the Si_3N_4 is a porous material, increasing its thickness might support to decrease the rate of the oxygen diffusion into the gate metals and the degradation rate of the IACC HEMTs. Therefore, the thickness of the passivation was increased to 1000 Å to understand what role the Si_3N_4 plays in the degradation rate of the HEMT under high electric fields. The same typical operating conditions were used to life test the devices in an ambient air environment since this was the higher degrading life test.

Reliability Test Results

The reliability tests included hot chuck evaluations to compare to the thinner passivated devices. Table 4.1 below shows the percent change comparison of the 250 Å and 1000 Å I_g. The leakage current (I_g) has a larger change after the pinch off stress than the knee voltage stress, which shows how the electric field has a larger impact than current density. However, the change has decreased significantly after increasing the thickness of the passivation layer. It appears that the thicker Si_3N_4 reduces the I_g leak degradation rate.

Table 4.1 Percent change of Ig with 250 Å versus 1000 Å

Stress	250 Å ΔIg%	1000 Å ΔIg%
Temperature	-8.3	-1.9
Pinch-off	-75.1	-29.6
Knee Voltage	-29.5	-14.0
Normal	-46.1	-26.4

The drain current after pinch-off stress was then compared to the thinner nitride passivation. After pinch-off stress, the drain current not only was higher before stress but decreased at a lower rate. With the 250 Å Si_3N_4, I_d decreased by about 34.8% while with the thicker nitride decreased by only 13.9%. The V_{th} continues to move in the positive Vg direction with 1000 Å Si_3N_4, but with less change, shown in Table 4.2.

Table 4.2 Percent change of Idmax and Vth

Stress	250 Å ΔIdmax%	1000 Å ΔIdmax%	250 Å ΔVth%	1000 Å ΔVth%
Temperature	-4.5	-10.8	0	0
Pinch-off	-34.8	-13.9	-28.6	-12.5
Knee Voltage	-8.3	-8.4	-20	-8.3
Normal	-40.3	-23.5	-60	-42.9

Analyzing the G_m curves, they follow the I_d curves' patterns. The degradation of G_m decreases from 27.5% to 3.4% after increasing the Si_3N_4 thickness with the pinch-off stress. The G_m peak with 1000 Å Si_3N_4 also increases before stress.

Table 4.3 Percent change of Gmp

Stress	250 Å ΔGmp%	1000 Å ΔGmp%
Temperature	-3.8	+0.9
Pinch-off	-27.5	-3.4
Knee Voltage	-5.6	-3.2
Normal	-38.5	-11.3

DCIV curves degradation also decreased shown in Table 4.4. R_{on} degradation drastically decreased from 124.1% to 12.5% with the thicker passivation.

Table 4.4 Percent change of Ron

Stress	250 Å ΔRon%	1000 Å ΔRon%
Temperature	0.7	3.3
Pinch-off	124.1	12.5
Knee Voltage	7.8	8.4
Normal	135	47.7

These numbers are considerably motivating showing how increasing the Si3N4 passivation thickness not only decreases the degradation of the electrical parameters but also improves some of the HEMT performance. Further work will be required to completely understand how the HEMT performance can be enhanced. However, this does point towards the theory that the environmental effects can be reduced by manipulating the barrier (Si3N4 passivation layer) between the environment and the HEMT device.

In addition to the development of the HEMT by increasing the passivation thickness, the HEMT devices were manufactured on a low-noise amplifier (LNA) circuit. This allowed us to life test four HEMT devices at a time, instead of just one. This gave higher statistics in a shorter amount of time. However, when testing the entire circuit, we cannot differentiate which transistor is the most susceptible to degradation. In order to identify the HEMT which degraded faster, we had to do an additional LNA circuit analysis.

Additional Low-Noise Amplifier Circuit Assessments

An entire LNA circuit is measured during the accelerated life tests. Each LNA circuit has four (4) HEMTs, Figure 4.7. Since the whole circuit is measured, it is difficult to determine which of the four transistors degraded. Therefore, an additional LNA circuit assessment was used to determine which HEMT was the weakest link and might be able to direct us to the failure mechanism we are searching for. This was helpful in narrowing down our HEMT choice for microscopy work. The circuits were tested after each accelerated life test.

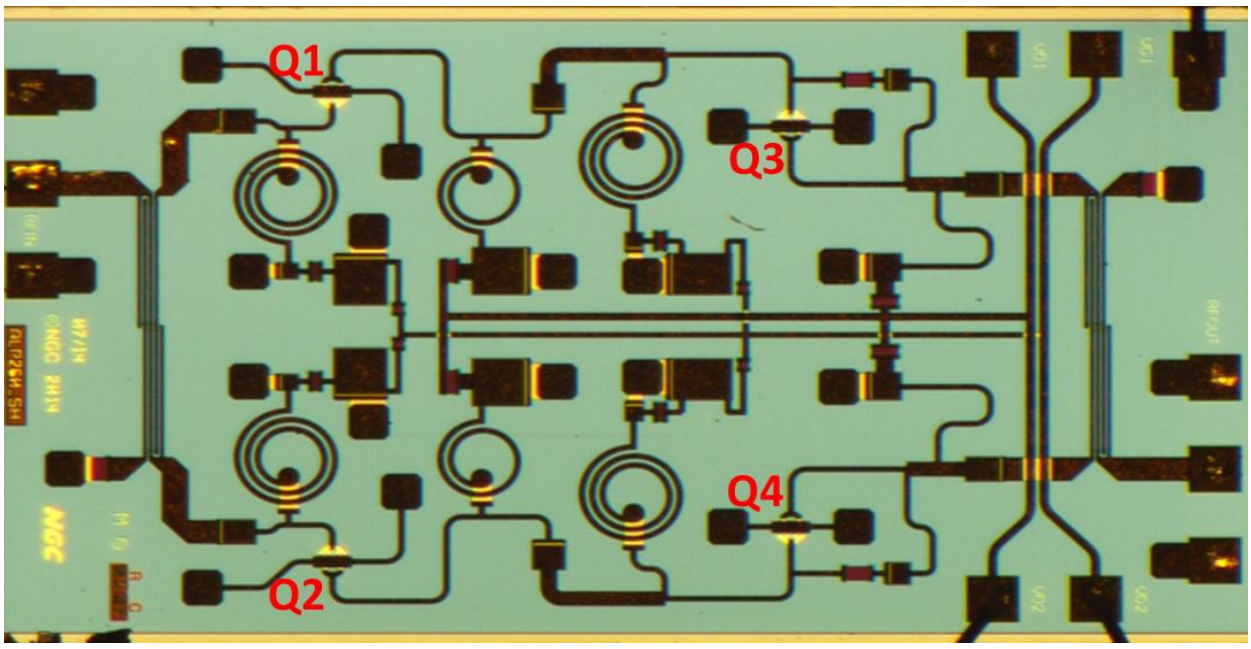

Figure 4.1 Image of an LNA Circuit with 4 HEMTs

LNA Circuit Assessment Results

The results of a few of the LNA circuit assessments are shown in Table 4.1 below as examples. The highlighted HEMTs are the ones that had degraded the most from each circuit. Henceforth, we were able to determine the worst-case electrical degradation and try to look for physical degradation mechanisms by using our microscopy techniques.

Table 4.5 LNA assessment results for five circuits

Circuit	HEMT	G_{mp} (mS/mm)	I_{dmax} (mA/mm)	V_{th} (V)	R_{on} (Ω)
1	Q1	1704	404	0.140	9.10
	Q2	1700	416	0.130	17.0
	Q3	1842	489	0.110	7.84
	Q4	1611	372	0.150	9.69
2	Q1	1616	439	0.090	10.0
	Q2	1405	373	0.100	16.7
	Q3	1035	259	0.110	13.9
	Q4	1133	334	0.070	10.8
3	Q1	895	282	0.030	22.0
	Q2	1309	423	0.030	19.1
	Q3	1298	474	-0.020	13.2
	Q4	1138	382	0.020	14.6
4	Q1	1491	493	0.030	10.5
	Q2	1512	492	0.020	10.5
	Q3	gate current compliance			
	Q4	1503	473	0.050	10.4
5	Q1	1365	447	0.020	12.5
	Q2	1402	440	0.050	11.7
	Q3	1387	472	0.010	11.7
	Q4	gate current compliance			

Microscopy

The STEM of the 1000 Å Si_3N_4 passivated devices after stressing them at a high electric field is shown in Figure 4.2 below. With the increase in passivation thickness, as suspected, gate sinking does not occur, similar to the thinner passivation. However, the titanium gate metal does not look physically expanded and there is no phase division between the inner and outer edges of

the titanium as there was with the thinner nitride. The lessened degradation in the electrical behavior of the devices shows in the physical aspects of the device. The EDS spectrum showed a lessened oxygen concentration of the outer edge of the titanium as well.

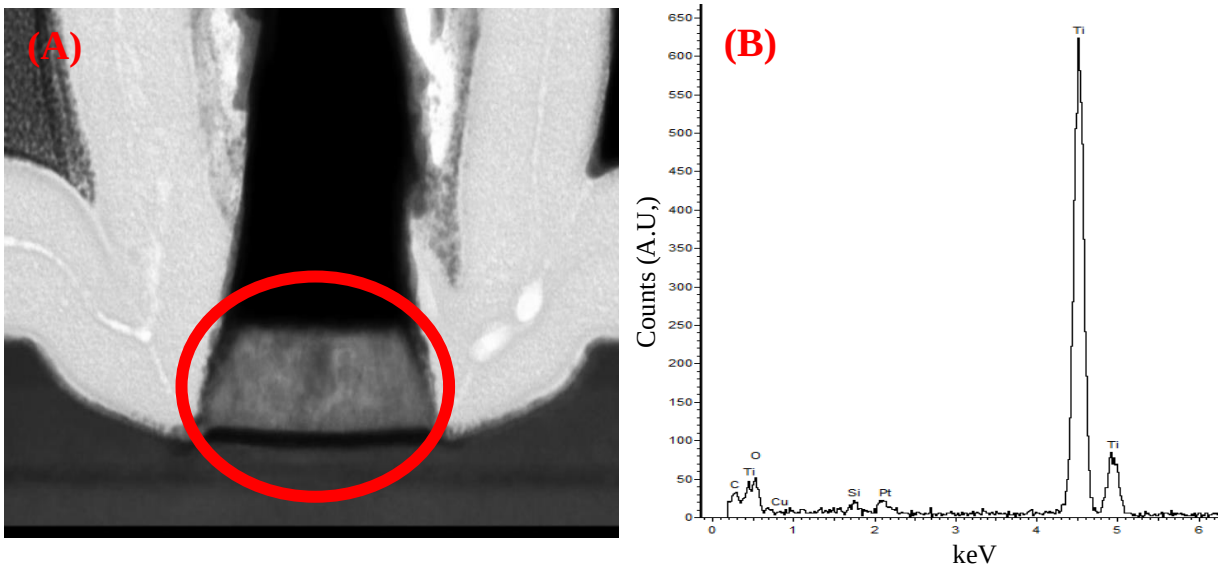

Figure 4.2 (A) STEM image of 1000 Å Si_3N_4 device after a high electric field life test; (B) EDS spectrum of the outer edge of the titanium metal showing less concentration of oxygen

In order to verify our results and hypothesis, TCAD Sentaurus modeling tool was used to understand how the Schottky barrier height is affected and how the electric field behaves throughout the device.

Chapter 5 TCAD Sentaurus Modeling of Failure Mechanisms

TCAD Sentaurus Introduction

Synopsys TCAD (Technology Computer-Aided Design) Sentaurus is a computer modeling software which designs and simulates various types of semiconductors, including a HEMT. Sentaurus helps to identify the electrical behaviors of a HEMT under various conditions as materials and dimensions are changed before producing it to understand its behaviors and

reliability. In this paper, we are using Sentaurus to understand what failure mechanisms are being effected by the environmental factors of our experiments.

In order to properly model the HEMT, there is a specific process which creates the device and then simulates its behavior. The process flow below in Figure 5.1 shows how to verify the simulation works properly.

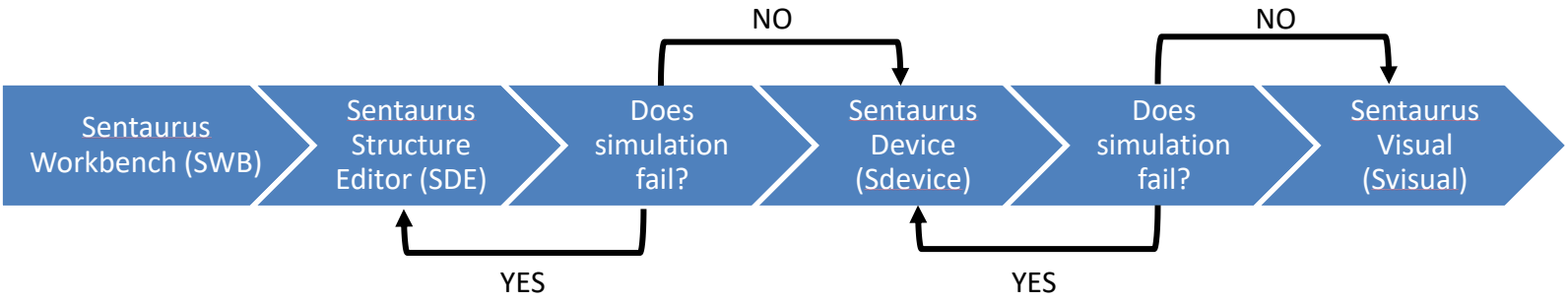

Figure 5.1 Synopsys TCAD Sentaurus process flow

After opening up the Sentaurus Workbench (SWB), the various tools shown in Figure 5.2 must be entered including Sentaurus Structure Editor (SDE) and Sentaurus Device (Sdevice). Figure 5.2 shows how each tool is entered in the software to analyze it. Each tool has commands that are entered into it which specify dimensions, parameters and definitions.

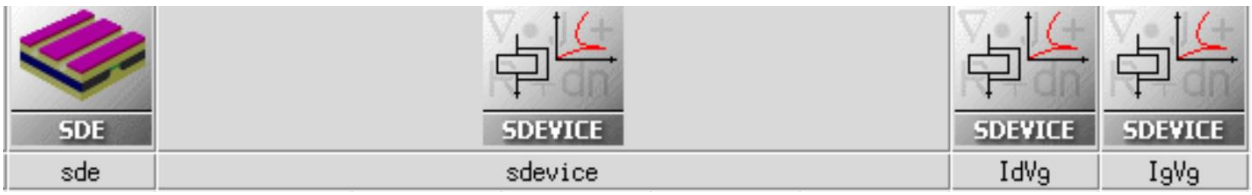

Figure 5.2 Sentaurus Workbench (SWB) interface

The HEMT is first designed by entering its dimensions, layers and doping concentrations as commands and allowing Sentaurus Device Editor to model the structure [27]. The HEMT contacts, the gate, source, drain and base positions are defined as well. An example of the commands is shown in Figure 5.3.

```
Geometry Dimensions (
        )
Derived Quantities (
        )
Layers Positions (
        )
Contacts (
        )
Doping Definitions (
        )
Meshing (
        )
```

Figure 5.3 Example of commands used in the SDE tool file

Once that is completed, the most important part of the HEMT analysis is the mesh. The mesh creates the finite-element device structure by nodes. Each node has specific material properties associated with it where electric fields, current and voltage are calculated. Figure 5.4 is an example of the structure of a device with its mesh. As shown, the mesh density is higher in the more current and doping dense areas, including the channel and delta-doping layer since these layers show more variation in their physical quantities. Therefore, increasing the mesh density, increases the precision of the calculations. However, as the refinement of the mesh increases, the simulation time also increases; it is essential to find the middle ground between the precision and simulation time to gain the most of the modeling software.

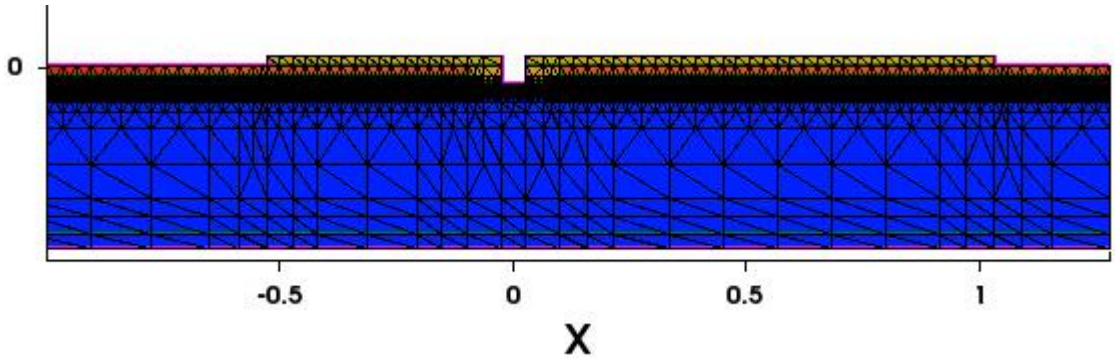

Figure 5.4 TCAD Sentaurus InP HEMT model with mesh

After creating the model, the electrical simulations can be calculated. Another command file must be generated to simulate the electrical parameters needed. The Sentaurus device tool [28] gathers the physical models and the associated material properties and combines them with the electrical parameters to create the electrical simulations. For this device, we have plotted I_g-V_g, I_d-V_g, DCIV and electric-field to explain the device behavior under ambient air environments.

```
File (
        *InputFiles
        *OutputFiles
        )
Electrode (
        Name=“”
        )
Physics (
        Mobility
        Recombination
        )
Plot (
        eDensity
        Doping
        )
Math (
        Extrapolate
        NoCheckTransientError
        )
Solve (
        Coupled (Poisson Electron)
        Quasistationary
        )
```

Figure 5.5 Example of commands used in the sdevice tool file

TCAD Electrical Simulations

Each of the simulations below were derived using separate Sentaurus device tools in order to be able to easily vary parameters without effecting other variables.

I_g-V_g Curves

The I_g-V_g curves were calculated using a diode V_g sweep from -0.5 to +0.4 V. The device commands were first verified by calibrating with an unstressed device, Figure 5.6A. This is shown as a baseline for the rest of the simulations. Figure 5.6B shows how the I_g-V_g curve has changed with the Schottky barrier height. This verifies our results and hypothesis that the Ig changes with the Schottky barrier heights.

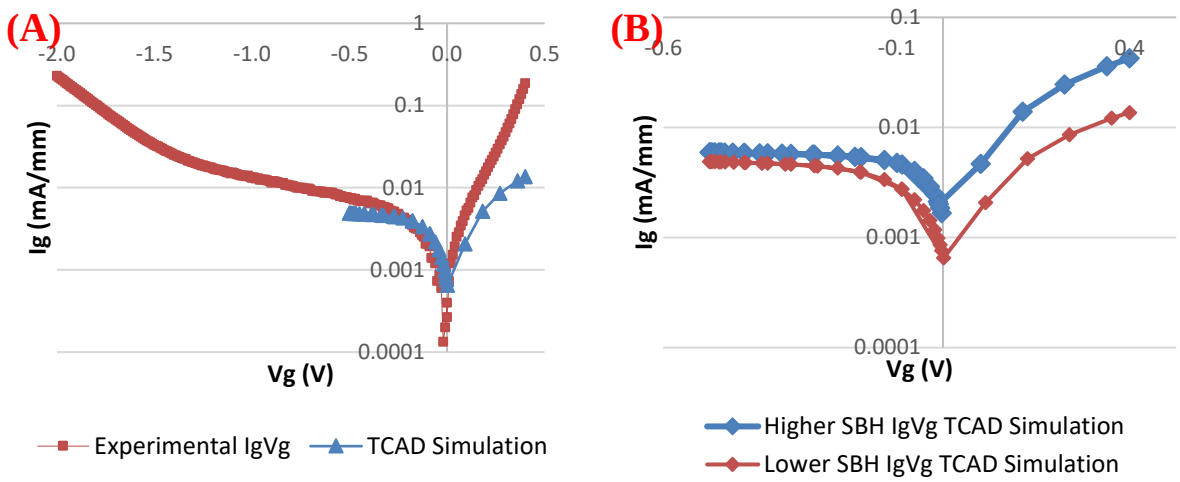

Figure 5.6 (A) IgVg of unstressed device against TCAD simulation; (B) IgVg curve of TCAD simulation with Schottky barrier change

DCIV Curves

DCIV curves were also simulated with TCAD. The curves were taken with Vd from 0 to 1.0 V with Vg swept from -0.5 V to +0.4 V. Figure 5.7 shows the DCIV curves simulated by TCAD. Figure 5.7A is also another baseline to calibrate the device commands with an unstressed device. With this verification, Figure 5.7B shows how the DCIV curves changed with the Schottky barrier height change.

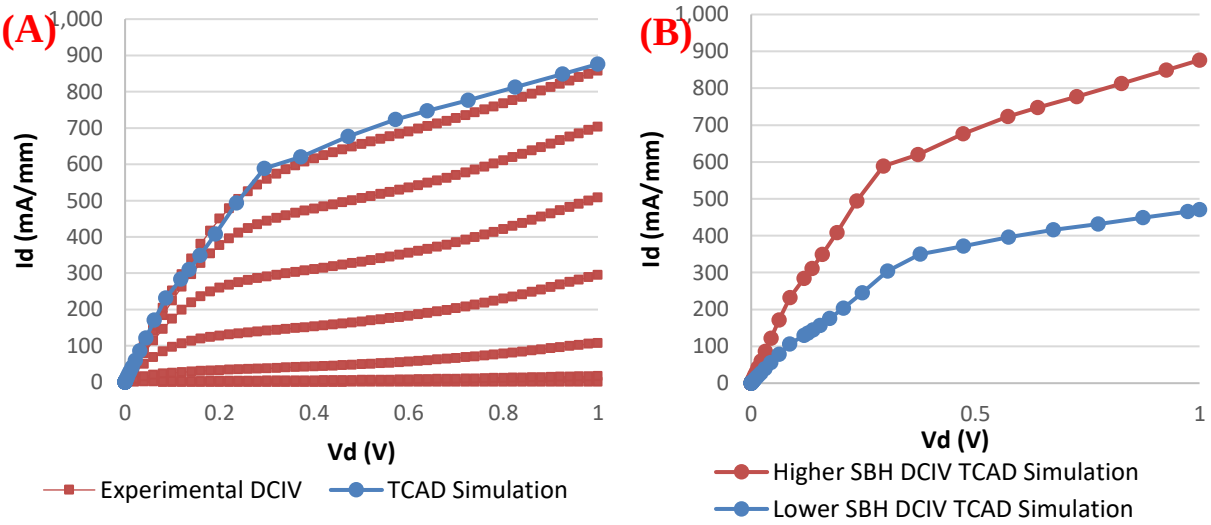

Figure 5.7 (A) Baseline DCIV with experimental DCIV versus TCAD simulations; (B) DCIV Schottky barrier change

Electric-Field

The electric-field is a vector parameter which describes how the electric-field stress is distributed throughout the device. Figures 5.8A and 5.8B shows the electric-field distribution at the two stresses of concern: (1) at pinch-off and (2) knee voltage stress, respectively.

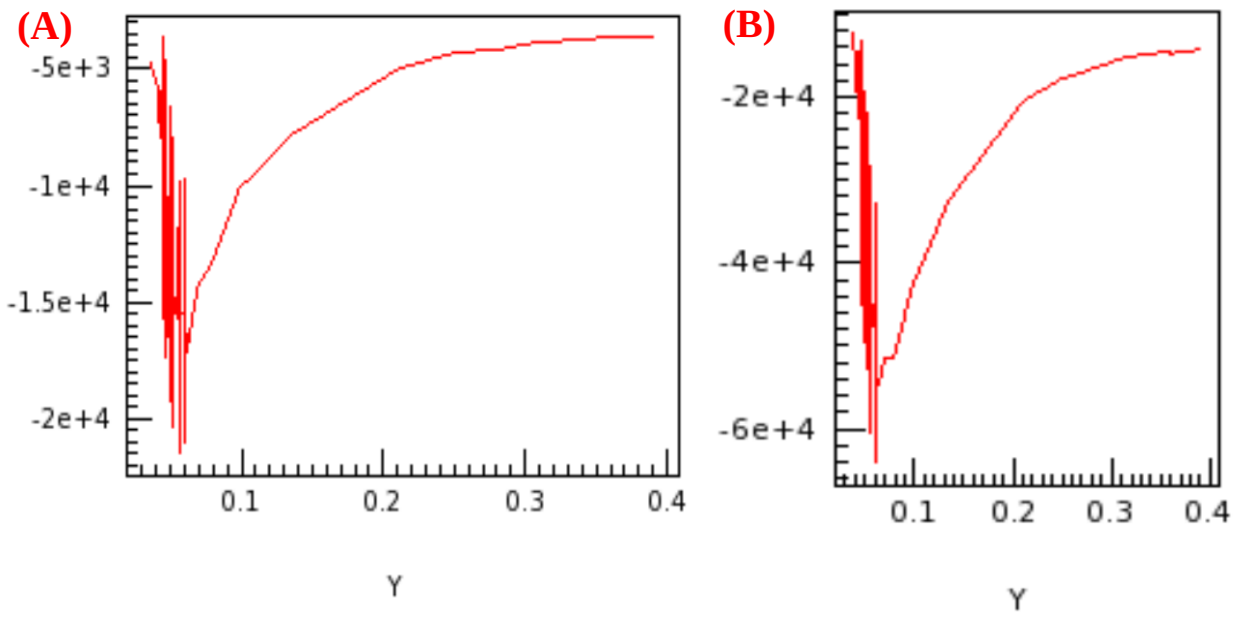

Figure 5.8 Electric-field distribution through the gate at (A) pinch-off stress; (B) knee voltage stress

The electric-field distribution shows that the electric-field stress at pinch-off stress is higher than under the knee voltage stress, which is current-induced. The pinch-off stress simulation was taken with Vd = 1.0 V and Vg = -0.5 V. The knee voltage was taken at Vd = 0.2 V and Vg = 0.4 V. Both distributions were taken through the gate of the device. This confirms the hypothesis of this work that the oxygen diffusion through titanium is induced further with a high enough of an electric-field.

Chapter 6 Conclusions and Future Work

This work has shown that the new NGMET barrier layer has improved the device gate sinking failure mechanism. The IACC HEMT does not degrade by gate sinking even in an

ambient air environment, which shows very high gate sinking reliability, unlike previous InP HEMT technologies. With enough oxygen content and high enough electric-field, the device parameters degrade. However, with a thick enough passivation layer, the degradation of the electrical parameters decreased. The TCAD simulations along with EDS spectra show that with a higher electric-field, the oxygen diffuses through the titanium faster and the Schottky barrier height changes.

Future work will include optimizing the passivation thickness for maximum power and frequency of the IACC HEMTs. There will also be additional TCAD simulations to verify these results of optimal thickness.

References

[1] M. T., "The Early History of the High Electron Mobility Transistor (HEMT)," *IEEE Transactions on Microwave Theory and Techniques,* vol. 50, no. 3, pp. 780-782, 2002.

[2] Takashi Mimura, Satoshi Hiyamizu, Toshio Fujii and Kazuo Nanbu, "A New Field-Effect Transistor with Selectively Doped GaAs/n-AlxGa1-xAs Heterojunctions," *Japanese Journal of Applied Physics,* vol. 19, no. 5, 1980.

[3] I. History, "Moore's Law and Intel Innovation," Intel, [Online]. Available: https://www.intel.com/content/www/us/en/history/museum-gordon-moore-law.html.

[4] Xiaobing Mei, Wayne Yoshida, Mike Lange, Jane Lee, Joe Zhou, Po-Hsin Liu, Kevin Leong, Alex Zamora, Jose Padilla, Stephen Sarkozy, Richard Lai and William R. Deal, "First Demonstration of Amplification at 1 THz Using 25-nm InP High Electron Mobility Transistor Process," *IEEE Electron Device Letters,* vol. 36, no. 4, pp. 327-329, 2015.

[5] Akira Endoh, Yoshimi Yamashita, Keisuke Shinohara, Kohki Hikosaka, Toshiaki Matsui, Satoshi Hiyamizu and Takashi Mimura, "InP-Based High Electron Mobility Transistors with a Very Short Gate-Channel Distance," *Japanese Journal of Applied Physics,* vol. 42, no. 48, 2003.

[6] W. Deal, "InP HEMT for Sub-Millimeter Wave Space Applications: Status and Challenges," in *39th International Conference on Infrared, Millimeter, and Terahertz waves (IRMMW-THz)*, Tucson, AZ, USA, 2014.

[7] R. Lai, X. B. Mei, W.R. Deal, W. Yoshida, Y. M. Kim, P.H. Liu, J. Lee,, J. Uyeda, V. Radisic, M. Lange, T. Gaier, L. Samoska, A. Fung, "Sub 50 nm InP HEMT Device with Fmax Greater than 1 THz," in *IEEE International Electron Devices Meeting*, Washington, DC, USA, 2007.

[8] Y.C. Chou, H. Guan, G. P. Li, R. Lai, R. Grundbacher, D. Leung, D. Eng, T. Block and A. Oki , "Degradation analysis of 0.1 μm InP HEMTs using low frequency noise characterization," in *16th IPRM International Conference on Indium Phosphide and Related Materials*, Kagoshima, Japan, 2004.

[9] Y.C. Chou, R. Lai, D. Leung, Q. Kan, D. Farkas, D. Eng, M. Wojtowicz, P, Chin, T. Block, A. Oki, "Gate Sinking Effect of 0.1 μm InP HEMT MMICS Using Pt/Ti/Pt/Au," in *Indium Phosphide and Related Materials Conference Proceedings*, Princeton, NJ, USA, 2006.

[10] Y. C. Chou, R. Grundbacher, D. Leung, R. Lai, Q. Kan, D. Eng, P.H. Liu, T. Block, A. Oki, "Degradation Mechanism and Reliability Improvement of InGaAs/InAlAs/InP HEMT MMICs New Gate Metal Electrode Technology," in *International Conference of Indium Phosphide and Related Materials*, Glasgow, Scotland, UK, 2005.

[11] J. A. Z. Flores, "Device Characterization and Modeling of Large-Size GaN HEMTs," Kassel University Press, Germany, 2012.

[12] Simon M. Sze, Kwok K. Ng, Physics of Semiconductor Devices, 3rd Edition, Hoboken, NJ: John Wiley & Sons, Inc., 2006.

[13] R. G. D. L. R. L. Q. K. D. E. P. H. L. T. B. a. A. O. Y.C. Chou, "Degradation Mechanism and Reliability Improvement of InGaAs/InAlAs/InP HEMTs Using New Gate Metal Electrode Technology," in *International Conference on Indium Phosphide and Related Materials*, Glasgow, Scotland, UK, 2005.

[14] Y.C. Chou, D. Leung, R. Grundbacher, R. Lai, Q. Kan, P.H. Liu, D. Eng,, "Gate metal interdiffusion induced degradation in space-qualified GaAs PHEMTs," *Microelectronics Reliability*, vol. 46, pp. 24-40, 2006.

[15] M. Dammann, A. Leuther, F. Benkhelifa, T. Feltgen, and W. Jantz, "Reliability and degradation mechanism of AlGaAs/InGaAs and InAlAs/InGaAs HEMTs," *Physica Status Solidi*, vol. 195, no. 1, pp. 81-86, 2003.

[16] Menozzi, Roberto, "Hot electron effects and degradation of GaAs and InP HEMTs for Microwave and Millimeter-Wave Applications," *Semiconductor Science and Technology*, vol. 13, pp. 1053-1063, 1998.

[17] C. C. D. P. W. X. J. Z. Muhammad Asif, "Improved DC and RF Performance of InAlAs/InGaAs InP based HEMTs Using Ultra-Thin 15 nm ALD-Al2O3 Surface Passivation," *Solid State Electronics*, vol. 142, pp. 36-40, 2018.

[18] P. P. a. Y. W. U.K. Mishra, "AlGaN/GaN HEMTs: An Overview of Device Operation and Applications," *Proceedings of the IEEE*, vol. 90, no. 6, pp. 1022 - 1031, 2002.

[19] D. E. N. D. C. J. C. E. L. P. E. E. L. L. S. J. M. Joseph Goldstein, Scanning Electron Microscopy and X-Ray Microanalysis: Third Edition, New York, NY: Springer Science + Business Media, Inc., 2003.

[20] A. R. L. M. V. A. Y. B. Y. P. M. P. O. K. v. B. M. F. C. S. J. Pennycook, "Scanning Transmission Electron Microscopy for Nanostructure Characterization," in *Scanning Microscopy for Nanotechnology*, New York, NY, Springer, 2006, pp. 152-191.

[21] M. F. F. L. d. L. A. L. D. R. Osvaldo N Oliveira Jr, "Scanning Electron Microscopy," in *Nanocharacterization Techniques*, Kidlington, Oxford, United Kingdom, William Andrew imprint of Elsevier Inc, 2017, pp. 1-35.

[22] J. Y. a. X.-J. L. Ying-Hui Zhong, "Impact of the Silicon-nitride Passivation Film Thickness on the Characteristics of InAlAs/InGaAs InP-based HEMTs," *Journal of the Korean Physical Society,* vol. 66, no. 6, pp. 1020-1024, 2015.

[23] X.-H. M. B. H. J.-J. Z. Y.-H. C. Wei-Wei Chen, "Impacts of SiN passivation on the degradation modes of AlGaN/GaN high electron mobility transistors under reverse-bias stress," *APPLIED PHYSICS LETTERS,* vol. 105, no. 173507, 2014.

[24] T. K. H. T. a. M. K. S. Ohi, "Effect of passivation films on DC characteristics of AlGaN/GaN HEMT," in *IEEE International Meeting for Future of Electron Devices, Kansai (IMFEDK)*, Kyoto, Japan, 2014.

[25] H.-L. Y. F.-H. H. Heng-Kuang Lin, "An alternative passivation approach for AlGaN/GaN HEMTs," *Solid-State Electronics,* vol. 54, no. 5, pp. 552-556, 2010.

[26] T. M. S. H. M. I. F. T. Y. M. I. T. Y. S. S. S. Hideyuki OKITA, "Comparisons of SiN Passivation Film Deposited by PE-CVD and T-CVD Method for AlGaN/GaN HEMTs on SiC Substrate," *IEICE Transactions on Electronics,* vol. E92.C, no. 5, pp. 686-690, 2009.

[27] Synopsys, "Sentaurus Structure Editor," 2015. [Online].

[28] Synopsys, "Sentaurus Device," 2015. [Online].

[29] J. F. Z. a. J. C. Z. Yue Hao, Nitride Wide Bandgap Semiconductor Material and Electronic Devices, Boca Raton, FL: CRC Press, 2017.

[30] B. B. A. K. M. S. a. N. Y. A. Turut, "The Bias-Dependence Change of Barrier Height of Schottky Diodes under Forward Bias by Including the Series Resistance Effect," *Physica Scripta,* vol. 53, no. 1, pp. 118-122, 1996.

[31] Y. Z. K. M. L. a. K. J. C. Yong Cai, "Control of Threshold Voltage of AlGaN/GaN HEMTs by Fluoride-Based Plasma Treatment: From Depletion Mode to Enhancement Mode," *IEEE TRANSACTIONS ON ELECTRON DEVICES,* vol. 53, no. 9, pp. 2207-2215, 2006.

[32] S. E. T. R. H. H. S. I. M.A. Huque, "Temperature dependent analytical model for current–voltage characteristics of AlGaN/GaN power HEMT," *Solid-State Electronics,* vol. 53, pp. 341-348, 2009.

[33] T.-C. H. S.-H. H. C.-F. H. Y.-H. W. G. S. S. Y. C. L. Ting-Fu Chang, "Threshold Voltage Instability in AlGaN/GaN HEMTs," in *IEEE 11th International Conference on Power Electronics and Drive Systems*, Sydney, NSW, Australia, 2015.

[34] Y. C. Chou, D. L. Leung, M. Biedenbender, D. C. Eng, D. Buttari, X. B. Mei, C. H. Lin, R. S. Tsai, R. Lai, M. E. Barsky, M. Wojtowicz, A. K. Oki and T. R. Block, "High Reliability Performance of 0.1 um Pt-Sunken Gate InP HEMT Low-Noise Amplifiers on 100 mm InP Substrates," in *22nd International Conference on Indium Phosphide and Related Materials (IPRM)*, Kagawa, Japan, 2010.