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High modulation efficiency electro-optic modulator: Material and Design

A dissertation submitted in partial satisfaction of the  
requirements for the degree Doctor of Philosophy

in

Electrical Engineering (Applied physics)

by

Kang-Wei Wang

Committee in charge:

Professor Paul Yu, Chair  
Professor Renkun Chen  
Professor Zhaowei Liu  
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Professor Joanna McKittrick

2018

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Chair

University of California San Diego

2018

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Chapter 3 covers the GaN nano-pillars arrayed waveguide

development. The fabrication is done by Kangwei Wang, Renjie Chen, and Woojin Choi.

Chapter 4 in full, is currently being prepared for submission for publication of the material. Pappert, Steve, Sun, CK, Chen, Dingbo, Yu, Paul K. L. The dissertation author was the primary investigator and author of this material. This chapter includes the nano-slot conductive waveguide directional coupler modulator (DCM). This work is done by Dr. Steve Pappert, Dr. CK Sun, Dr. Dingbo Chen, Kangwei Wang, and Prof. Paul Yu.

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### Conference paper:

- Paul K. L. Yu, Kangwei Wang, Steve Pappert, Dingbo Chen, CK Sun, “Recent advances in optical modulator for high-performance fiber-optic links,” in International Conference on Electron Devices and Solid-State Circuits (EDSSC), 2017
- Kangwei Wang, Haoliang Qian, Zhaowei Liu, Paul K.L. Yu, ”Second-harmonic susceptibility enhancement in Gallium nitride nano-pillars,” in Electron Devices Technology and Manufacturing Conference (EDTM), 2017

- Dylan Lu, Haoliang Qian, Kangwei Wang, Jimmy J Kan, Eric E Fullerton, Paul K. L. Yu, Zhaowei Liu, “Light emission enhancement by using patterned multilayer hyperbolic metamaterials” in Conference on Lasers and Electro-Optics Pacific Rim, 2015

**Abstract of the dissertation**

High modulation efficiency electro-optic modulator: Material and Design

by

Kang-Wei Wang

Doctor of Philosophy in Electrical Engineering (Applied Physics)

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Professor Paul Yu, Chair

Data explosion generates huge data traffic within the data center. The bottleneck of the data transportation is the optical transceiver. We study the critical component in the optical transceiver- optical modulator. The Figure-of-Merit (FOM),  $3\text{dB bandwidth}/V_{\pi}$  defines the modulation efficiency. In this dissertation, two approaches will be presented: 1. Utilizing GaN nano-pillars as electro optic material. GaN nano-pillars exhibits high second harmonic susceptibility,  $\chi^{(2)}$ , which is proportional to the electro-optic coefficient. 2. A new design of the optical modulator: nano-slot conductive waveguide directional coupler modulator (DCM). The DCM modulation performance evaluation is based on Beam Prop mode simulation analysis. Using the  $50\Omega$  terminated lumped-element to calculate the 3dB bandwidth, the DCM shows a FOM of 202 GHz/V where the state-of-the-art silicon-organic hybrid (SOH) Mach-Zehnder modulator (MZM) is 150.3 GHz/V. The advantage of applying DCM as the modulator platform for high EO coefficient polymer is not only the DCM has higher modulation FOM, but also the ease of the modulator design and fabrication. The DCM does not require two phase shifters, Si waveguide to polymer slot waveguide couplers, and multi-mode interferometer (MMI). To prove the principle of the strong cross-coupling characteristic in DCM, we design and fabricate an air-slot, non-slab DCM, which includes the input/output mode size converter, adiabatic S-bend, and the air-slot waveguides. By scanning the central wavelength of the incident light, the output power collecting from each of the two ports exhibits wavelength dependence. The extinction ratio is  $\sim 10$  dB and the peak-to-valley separation is  $\sim 1$  nm. The measurement result matches with the Beam Prop simulation.

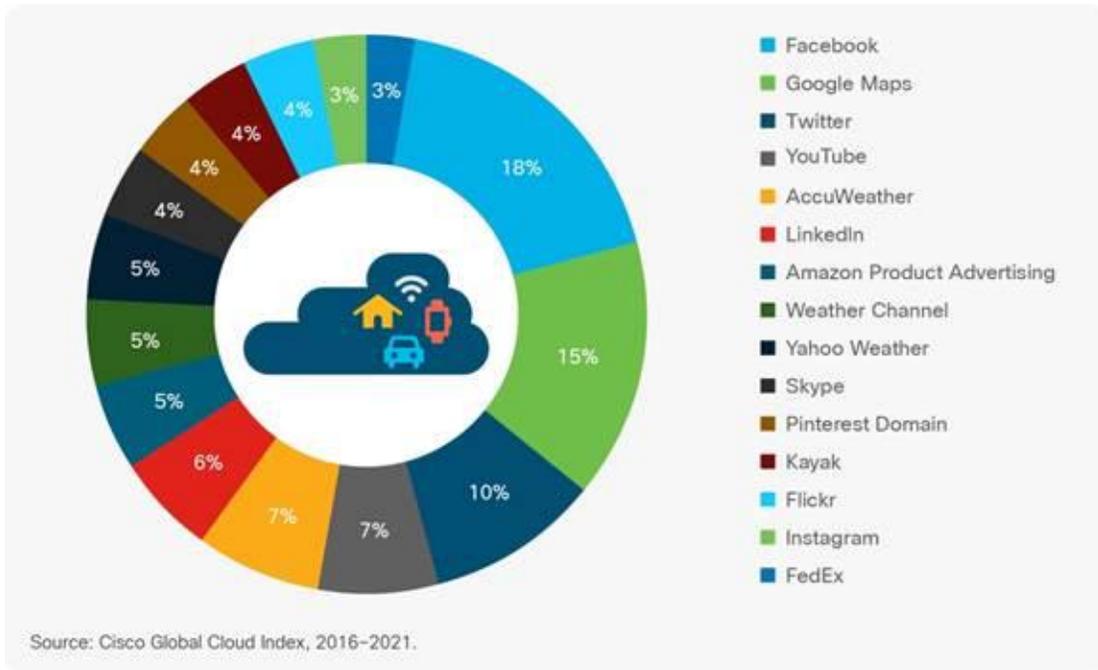
# CHAPTER 1

## INTRODUCTION AND RESEARCH GOALS

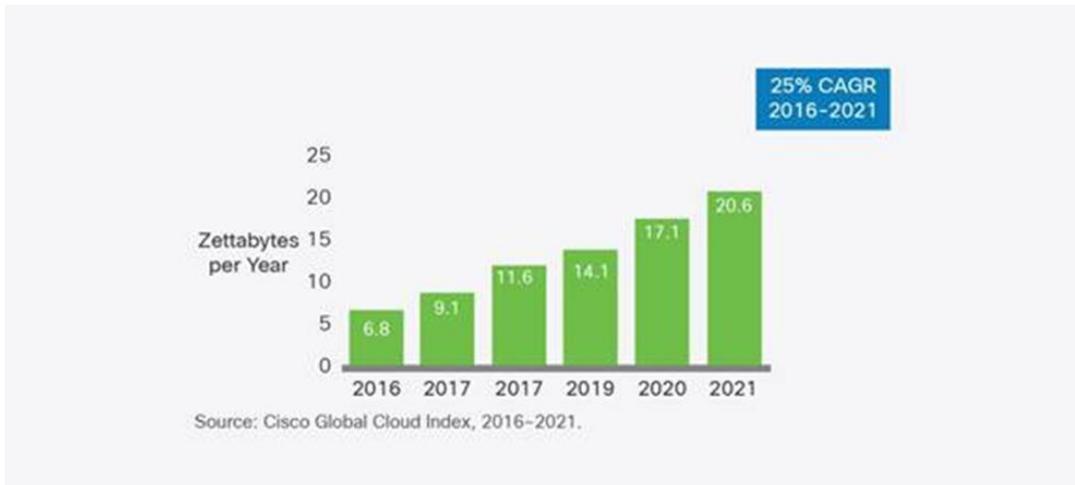
It is evident that the optical transceiver development is of great importance in both analog fiber link and Datacom. In Telecom wireless base station, antenna remoting, and CATV application, low optical insertion loss and low  $V_{\pi}$  optical modulator is the key to achieve high link gain [1]. In Datacom market, optical transceiver is no doubt the key solution to response the need of higher data rate, higher energy efficiency, and lower cost in data center.

Nowadays people create more and more data via our daily communication, such as emails, text messages, social network...etc. **Figure 1.1** shows the prediction of the application program interface (API) which attract the attention of users and web developers in year of 2016 to 2021 [2]. In addition, new technology includes Internet-of-Things (IOT) and all kinds of sensors generate data as well. Therefore, the data explosion follows an exponential increase. In software industry, machine learning and artificial intelligence (AI) speed up the process of converting random data into useful information. However, the processing speed is limited by the data center and super computer infrastructure. According to the forecast by Cisco (**Figure 1.2**) [2], the volume of the data is continuously growing. In 2021, the predicted data traffic will be 20.2 Zettabytes per year. Furthermore, if we examine the data destination from the data center, 71.5% of the data traffic happens within

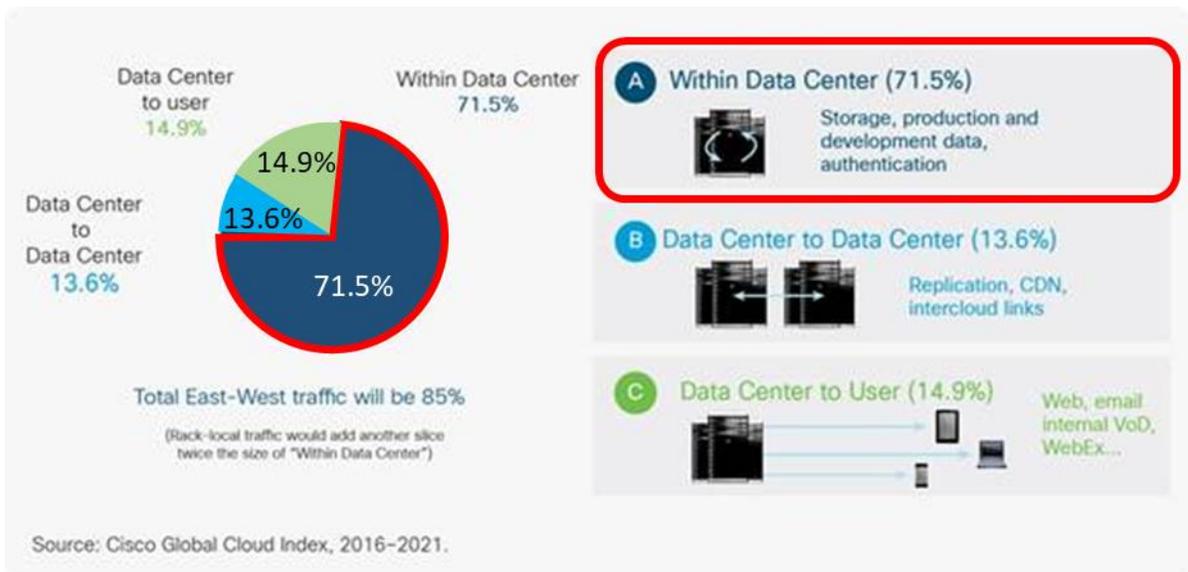
the data center itself (**Figure 1.3**). It explains the importance of development of the optical transceiver.



**Figure 1. 1.** The prediction of application program interface interests developers and users.



**Figure 1.2.** The global data center traffic growth prediction for year 2016 to 2021 in Zettabytes per year.



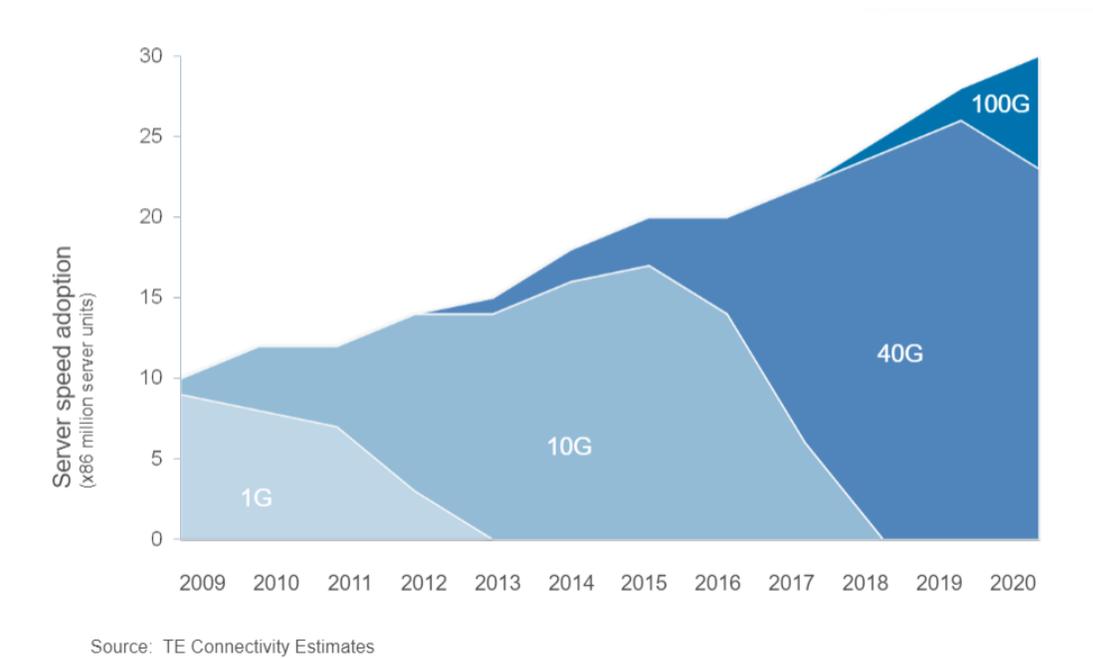
**Figure 1.3.** Prediction of data center traffic by 2021

For optical transceiver, according to the Datacom market estimation [3], the mainstream bandwidth of optical transceiver is 40 Gbps and the demand for 100 Gbps surfaced in 2018. On the other hand, in telecom industry, even though the 5G is still in the “Standard” stage, it is predicted that the demand for optical transceiver will exceed 10 million in quantity for 5G base station [4].

Besides, in military and aerospace communication, signal transporting through optical fiber does not generate electromagnetic interference (EMI) and is not affected by external EMI sources. Compared to copper cable, fiber optics show the light weight and less space occupancy.

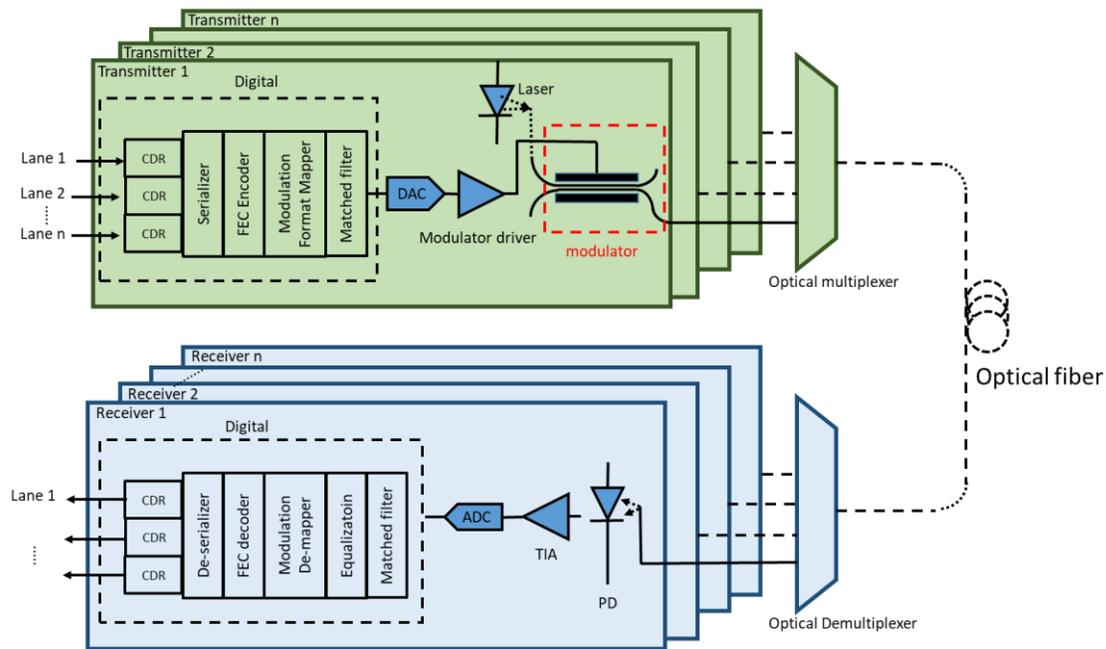
To sum up, a high bandwidth, high modulation efficiency (low  $V_{\pi}L$ ) optical modulator is demanded by military, Datacom, and Telecom markets. In this dissertation, I will introduce three major optical modulators and the development of Silicon photonics in chapter 1. In chapter 2, we will focus on implementing new electro optic material to meet the requirement of creating a high modulation efficiency optical modulator. The GaN nano-pillars will be presented. It offers high second harmonic susceptibility,  $\chi^{(2)}$ . We fabricated single GaN nano-pillars in different diameters ranging from 150 to 400 nm then measured their second harmonic intensity. As the diameter of the GaN nano-pillar reduces, the surface to volume ratio increases and leads to a higher effective  $\chi^{(2)}$ . Since electro optic coefficient is proportional to  $\chi^{(2)}$ . In chapter 3, I summarize the design, fabrication, and measurement results of GaN nano-pillars arrayed waveguides and discuss the future work for this approach. In chapter 4, novel optical modulator platform for high  $r_{33}$  material will be presented. it is a conductive waveguide directional coupler modulator (DCM) that has a

better Figure-of-merit (FOM),  $3\text{dB bandwidth}/V_{\pi}$  than the state-of-the-art silicon-organic hybrid (SOH) Mach Zehnder modulator (MZM). We propose a solution for next generation optical transceiver which will consist of extremely high EO coefficient material that can be filled into the nano-slot of a conductive waveguide directional coupler modulator (DCM). In chapter 5, I will show the fabrication development of the conductive waveguides DCM. In chapter 6, future work of improving the DCM performance will be listed and the simulation results of the current DCM will be reported. It could be a useful reference for researchers who are working on the design and fabrication of a conductive waveguide DCM.



**Figure 1.4.** Estimation of 10/40/100 Gbps progression [3].

## 1.2 Optical modulator categories



**Figure 1.5.** An illustration of an optical transponder. CDR: clock and data recovery, FEC: forward error correction, DAC: digital-to-analog converter, PD: photo diode, TIA: Trans-impedance amplifier, ADC, analog-to-digital converter.

**Figure 1.5** depicts an optical transponder system. At the optical transceiver (green box), the data come from several electrical lanes go into digital-signal-processor (DSP) then convert into analog signal at digital-to-analog converter (DAC). The output from DAC then amplified to voltages to modulate the optical modulator. A continuous-wave (CW) laser provides the light at the carrier frequency to be modulated. The modulated light propagates through the fiber, then reaches the receiver (blue box). At the receiver, the light

first captured by the photo diode then amplified by the trans-impedance amplifier (TIA). The amplified analog signal is digitalized by the analog-to-digital converter (ADC) before entering the DSP.

Later in this dissertation, I will present new design and new potential material which can be implemented for high efficiency (i.e. high bandwidth/  $V_{\pi}$ ) optical modulator. (**Figure 1.5**, red dash box). The optical modulator is a key component of the optical transceiver because it is a transducer which converts the data from electrical domain into optical domain so that it can be transmitted in the optical channel. Three categories of optical modulators are listed in **Table 1.1**.

**Table 1.1.** Three categories of optical modulator.

Type	Modulating real part of refractive index	Modulating imaginary part of refractive index
Electro-optic modulator	Pockels effect	none
Electro-absorptive modulator	None	Franz-Keldysh effect
MOS/ PN junction modulator	Plasma-dispersion effect	Plasma-dispersion effect

The new design and new potential material which I will present in the following chapters both belong to the electro-optic modulator categories.

### 1.3 Silicon photonics

As the microprocessor development schedule in all the foundry cannot meet the “Moore’s Law” prediction: the number of transistors on a chip double every 18 to 24 months. The cost of development of the next generation chip increases, but only few fabless IC design company shows their interest on next generation transistor. The concept of “More-than-Moore” is to diversify the application of a foundry’s capability into other applications. e.g. radio frequency (RF) devices, microelectromechanical system (MEMS), Silicon photonics...etc. [5]. Silicon photonics includes varieties on passive and active optical components into a highly integrated photonic-electronic circuit [6] [7]. A key building block is the optical interconnect. Due to the absence of second harmonic susceptibility,  $\chi^{(2)}$ , in Silicon, pure-Si optical modulators rely on the free-carrier dispersion through injecting or depleting electron and holes in a diode or a MOS structures. However, these devices do not meet the goal of a high bandwidth ( $> 50$  Gbps in single wavelength), low drive voltage ( $\leq 1$  V), low power consumption, and a small foot print (sub millimeter). In chapters 4 and 5, we present a new platform to incorporate the high EO polymer into a pure-Silicon base EO modulator, namely, conductive waveguide directional coupler modulator (DCM). Its modulation sensitivity,  $V_{\pi}L$  is lower than the state-of-the-art silicon-organic hybrid (SOH) Mach Zehnder modulator (MZM), and its Figures-of-merit (FOM): 3dB bandwidth/ $V_{\pi}$  is 35% better than the SOH MZM as well. The DCM does not require a complicated coupler design to split the light evenly into two arms and thus is immune from the potential risk of power imbalance in the two arms of MZM.

# CHAPTER 2

## SECOND-HARMONIC SUSCEPTIBILITY ENHANCEMENT IN GALLIUM NITRIDE NANO-PILLARS

### 2.1 introduction

Optical materials with high second-order nonlinear response have many applications. In bio-imaging, second harmonic generation (SHG) is less destructive to cells compared to fluorescence dyes [8]. In our study, high second-order nonlinearity in electro-optic materials are exploited for their strong Pockels effect (linear electro-optic effect), which can be used to make linear electro-optic modulator. Among the second-order nonlinear materials, LiNbO<sub>3</sub> is the most common to make an electro-optic (EO) modulator. It offers relatively large linear EO effect, represented in term of a second rank EO tensor,  $\{r\}$  (e.g. the coefficient  $r_{33}=30.9$  pm/V), and is highly transparent at 1310 nm and 1550 nm wavelengths [9]. However, it is desirable to have a modulator technology that is easily integrated with an optical emitter as well as electronic components on a common substrate. Consequently, extensive research has been focused on novel material effects to enhance the second-order nonlinear response, including: strain [10] [11], polymer [12], surface effect on nano-structure, metamaterials [13] and plasmonic effect [14]. In our previous study, we observed enhancement of linear EO effect in InP nanowires [15]. However, due

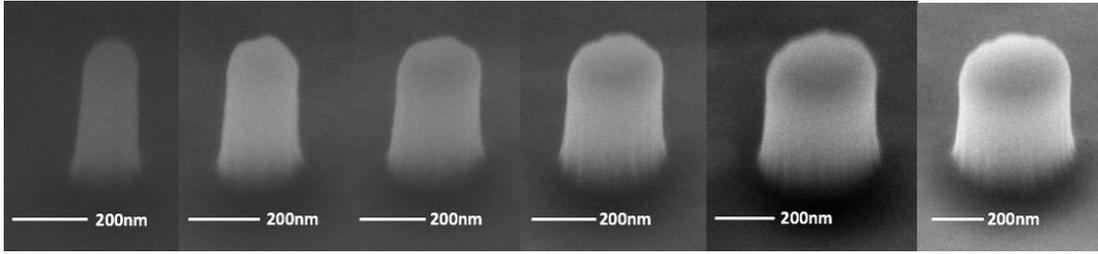
to the bottom-up nanowires growth employed, the length of the nanowires showed high variation, which caused the uncertainty in determining the fill factor and thus the difficulty in determining the relationship between the linear EO coefficient and nanowire surface area [16]. Recent published papers reveal that the second harmonic generation (SHG) could be enhanced by using nano-wires/nano-pillars instead of bulk compound semiconductor materials. These include GaAs [17], GaP [18] [19] [20], ZnS [21], and ZnTe [22] nanowires. In R. Sanatinia *et al* 's work [20], surface second harmonic tensor of GaP nanowire was created to resolve the second harmonic susceptibility of the surface ( $\chi_s^{(2)}$ ) and the bulk ( $\chi_{bulk}^{(2)}$ ). They estimated  $\chi_s^{(2)}$  is larger than  $\chi_{bulk}^{(2)}$  and its surface effective thickness is within 15-20 nm from the nanowire surface. GaN belongs to the group of wurtzite crystals and has a crystal symmetry different from those of InP and GaP (zinc-blende crystals), it would be of interest to explore its surface SHG properties.

In this chapter, we investigate second harmonic response in single GaN nano-pillar. The nano-pillar is fabricated via a top-down approach which ensures individual pillar is perpendicular to the substrate and facilitates the fabrication of the electro-optic modulator. GaN is a high bandgap material and has small absorption in the visible and infrared wavelengths. Furthermore, it has wide application in high speed, high power electronics, as well as light emitters. In our SHG measurement, the effective second harmonic susceptibility  $\chi_{eff}^{(2)}$  at 900 nm fundamental excitation is found to be ~7 times higher than GaN bulk on *c*-sapphire, and our analysis shows that the enhancement of SHG is most

likely comes from the nano-pillar surface area. The results suggest that the GaN nano-pillar is a strong material candidate for effective electro-optic modulator.

## 2.2 Single GaN nano-pillar fabrication

A GaN layered structure was grown by metal-organic vapor phase epitaxy (MOVPE) on a 2-inch diameter single side polished *c*-plane sapphire wafer using trimethylgallium (TMG) and  $\text{NH}_3(\text{g})$  as precursors for gallium (Ga) and nitrogen (N) respectively. Hydrogen was used as carrier gas, and the total gas flow rate was  $\sim 5$  slm. The GaN layered structure consists of undoped GaN (0.4  $\mu\text{m}$ ), GaN buffer layer (0.1  $\mu\text{m}$ ). After epitaxy, the wafer was cleaned in standard organic solvents, rinsed in de-ionized water and blow-dried under nitrogen gas. Single GaN nano-pillars were patterned by E-beam lithography (Vistec EBPG 5200). The resulting nano patterns were then transferred from the HSQ e-beam resist to the GaN layer by dry etching (Oxford Plasmalab 80 reactive ion etcher (RIE)). The RIE RF power is set at 200 W;  $\text{Cl}_2$ , at a flow rate of 5 sccm and  $\text{BCl}_3$ , at 50 sccm were injected. After dry etching of GaN, buffered oxide etchant (BOE) was used to remove the HSQ from the nano-pillars. The nano-pillars have the same height of 432 nm as determined from the RIE etching time. **Figure 2.1** shows a series of single GaN nano-pillars fabricated.

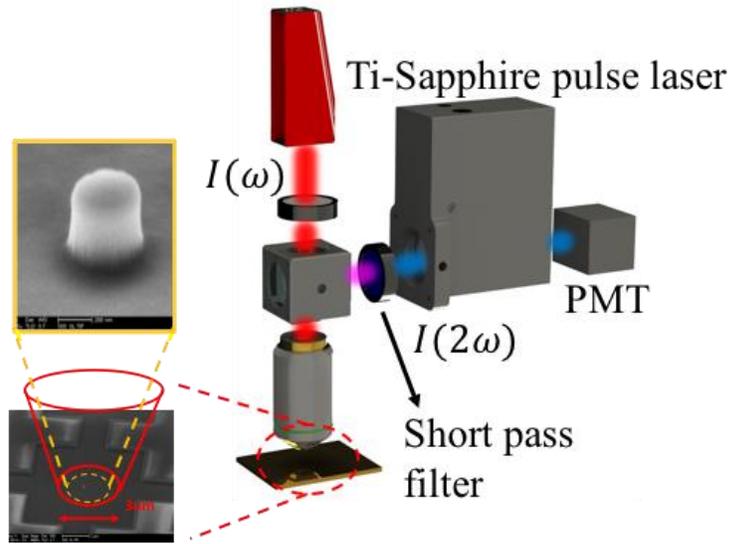


**Figure 2.1.** 45° tilted SEM images of single nano-pillars. Diameter (from left to right): 150, 200, 250, 300, 350, and 400 nm.

### 2.3 Second harmonic generation measurement

We performed the reflective SHG measurement of the GaN nano-pillar samples at room temperature in a back-scattering geometry (**Figure 2.2**) with mode-locked Ti:Sapphire laser (Mai Tai, Spectra-Physics) operating at 900 nm wavelength, at a pulse duration of 100 fs, and 80 MHz repetition rate. The laser output power (at 900 nm) is 2.3W and the attenuated incident light power at the GaN nano-pillar sample is 127.6 mW for the focused spot area. A 20X microscope objective lens with a numerical aperture of 0.45 was used. With this configuration we obtained a laser spot size about 3  $\mu\text{m}$  in diameter.

The reflected fundamental beam and SHG ( $\lambda_{2\omega}=450$  nm) signals were collected by the same objective lens and separated by a dichroic mirror. Several short pass filters (SPF) were used to block the fundamental beam. The SHG signal was directed through a monochromator and subsequently to a photomultiplier tube (PMT). **Table 2.1** lists the intensity of the SHG signals from single GaN nano-pillar with an average diameter ranged from 150 to 400 nm.



**Figure 2.2.** Reflective second harmonic generation (SHG) measurement setup. The single GaN nano-pillar is at the middle of a focus spot with a 3  $\mu\text{m}$  diameter.

**Table 2.1.** The reflective second harmonic measurement result of the single GaN nano-pillars in the diameter range from 150 nm to 400 nm

Nano-pillar diameter (nm)		150	200	250	300	350	400
<b>Input Parameters</b>	Input Power (mW)	127.6	127.6	127.6	127.6	127.6	127.6
	Transmission (%)	85.2	86.1	85.9	86.6	87.1	85.2
<b>SHG signal</b>	SHG (counts)	80	95	85	245	260	400
	Reflectivity (%)	17.4	14.8	15.2	17.3	17.2	17.4
	$\chi_{eff}^{(2)}$ (pm/V)	136.0	90.2	53.7	58.6	44.2	42.7

**Table 2.1** shows the SHG measurement results for single GaN nano-pillar in the range of 150-400 nm diameter (the fundamental excitation is at 900 nm). The transmission means the percentage of 900 nm fundamental light illuminates on to the nano-pillar; the SHG reflectivity indicates the percentage of the generated SHG being collected by the objective lens. The  $\chi_{eff}^{(2)}$  is calculated based on the **Equation 2.3** below [23].

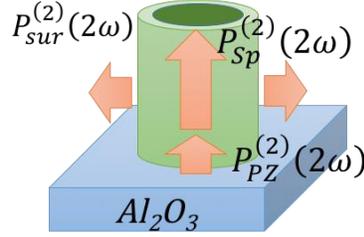
## 2.4 Results and discussion

There are three popular methods to measure the second harmonic generation (SHG) - phase matched method, parametric fluorescence, and Maker fringe method [23]. The second order non-linearity is related to the second order susceptibility via

$$P^{(2)}(2\omega) = \epsilon_0 \chi^{(2)} E(\omega)^2 \quad \text{(Equation 2.1)}$$

where  $P^{(2)}$  is the amplitude of the component of nonlinear polarization oscillation at frequency  $2\omega$ ,  $\chi^{(2)}$  is the second order susceptibility. For GaN bulk material, most of the reported  $\chi^{(2)}$  uses the Maker fringe method-by rotating a GaN film through which the fundamental beam and SHG generate constructive and destructive interference. The GaN grown on *c*-sapphire substrate shows a  $\chi_{33}^{(2)} \sim 20$  pm/V [24] [25] [26]. Its nonlinear effect originates from the spontaneous polarization and piezoelectricity [27]. In the case of GaN nano-pillar, due to lack of a flat film surface, we choose phase matching method to measure its  $\chi^{(2)}$ . The dangling bonds at the surface lead to a third contribution to the surface nonlinear effect. Therefore, the overall effective  $\chi^{(2)}$  for GaN nano-pillars can be expressed as  $\chi_{eff}^{(2)} =$

$\chi_{sp}^{(2)} + \chi_{pz}^{(2)} + \chi_{sur}^{(2)}$ . (sp: spontaneous; pz: piezoelectric; sur: surface) (**Figure 2.3**), where  $\chi_{sp}^{(2)}, \chi_{pz}^{(2)}$  are both intrinsic bulk properties and  $\chi_{sur}^{(2)}$  is the surface contribution. GaN grown on *c*-sapphire substrate has a non-centrosymmetric, hexagonal structure (crystal group: 6mm) that gives spontaneous polarization in the vertical direction. The lattice mismatch between GaN and sapphire ( $\text{Al}_2\text{O}_3$ ) generates piezoelectric polarization [28] [29].  $\chi_{sur}^{(2)}$  is originated from the broken symmetry at the nano-pillar sidewall [30], and the surface polarization is not radially distributed, but depends on the broken Ga-N bond.



**Figure 2.3.** Schematic illustration of the three types of polarizations (spontaneous, piezoelectric, and surface) that contribute SHG from a single GaN nano-pillar on sapphire ( $\text{Al}_2\text{O}_3$ ) substrate.

First, the intensity of the second harmonic signals,  $I(2\omega)$ , is related to the amplitudes as:

$$\begin{aligned}
 I(2\omega) &\propto [P^{(2)}(2\omega)]^2 \propto [P_{sur}^{(2)}(2\omega)]^2 + [P_{bulk}^{(2)}(2\omega)]^2 \\
 &\propto [\chi_{sur}^{(2)} E^2(\omega)]^2 + [\chi_{bulk}^{(2)} E^2(\omega)]^2 \\
 &\propto [(\chi'_{sur}^{(2)} \cdot S) \cdot E^2(\omega)]^2 + [(\chi'_{bulk}^{(2)} \cdot V) \cdot E^2(\omega)]^2
 \end{aligned}$$

$$\propto A_{sur} \cdot S^2 + B_{bulk} \cdot V^2 \quad \text{(Equation 2.2)}$$

Herein, we define  $P_{sur}^{(2)}(2\omega)$  and  $P_{bulk}^{(2)}(2\omega)$  as the amplitude of the component of nonlinear polarization at the surface and in the bulk at frequency  $2\omega$ , respectively.  $\chi_{sur}^{(2)}$  and  $\chi_{bulk}^{(2)}$  are the surface and volume distributed second harmonic susceptibility, respectively.  $A_{sur}$  is the coefficient related to the nano-pillar surface contribution, and  $B_{bulk}$  is the coefficient related to the bulk contribution.  $S$  is the nano-pillar's surface area, and  $V$  is its volume. In **Table 2.2**, the fitting results show that the SHG from single GaN nano-pillar is dominated by the surface effect. **Figure 2.4** (left) shows the measured SHG signal counts and the fitting result based on **Equation 2.2**. **Figure 2.4** (right) is the normalized SHG counts versus different diameters of single nano-pillar, one can see the increasing percentage of the surface contribution to SHG as the diameter of the nano-pillar decreases. We also observed that when GaN nano-pillar diameter is in the range of 150 - 400 nm, the volume of the nano-pillar only accounts for < 10% of the SHG signals. In this model, we assume the E-field distribution remains constant at the surface.

Second, the second harmonic susceptibility,  $\chi^{(2)}$  of single GaN nano-pillar is an important factor to evaluate its potential use in electro-optic modulator. To measure the  $\chi_{eff}^{(2)}$  of single GaN nano-pillars ( $\chi_{eff}^{(2)} = \chi_{sp}^{(2)} + \chi_{pz}^{(2)} + \chi_{sur}^{(2)}$ ), we accurately calibrate the system setup, including, (a) the power decay between the laser outlet and the actually power excites the single nano-pillar, (b) the incident light (900 nm) transmissivity, (c) objective lens collection efficiency of the SHG light (450 nm), (d) SHG signals are attenuated while

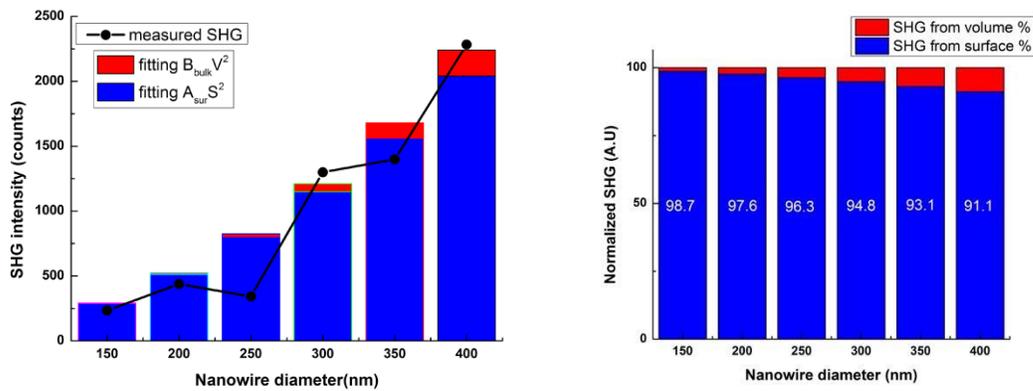
traveled through four short pass filters. The relationship between the SHG intensity and the second harmonic susceptibility can be written as [31]:

$$I(2\omega, l) = \frac{\omega^2(\chi_{eff}^{(2)})^2 l^2}{2n_{2\omega}n_{\omega}^2 c^3 \epsilon_0} \left( \frac{\sin(\Delta kl/2)}{\Delta kl/2} \right) I^2(\omega) \quad \text{(Equation 2.3)}$$

where  $I(2\omega, l)$  is the intensity of SHG for nano-pillar with length  $l$ ,  $I(\omega)$  is the intensity of fundamental light,  $\omega$  is the light frequency,  $\chi_{eff}^{(2)}$  is the effective second harmonic susceptibility,  $n_{2\omega}$  and  $n_{\omega}$  are the refractive indices of light at frequencies  $\omega$  and  $2\omega$  respectively.  $\sin(\Delta kl/2)/\Delta kl/2$  is the phase matching term,  $c$  is the light speed, and  $\epsilon_0$  is the vacuum permittivity. Since nano-pillars are only 432 nm tall, phase-matched term is taken to be unity. Note that the  $\chi_{eff}^{(2)}$  is normalized to the fill factor (FF). The calculated  $\chi_{eff}^{(2)}$ 's are summarized in **Table 2.2**. As the diameter of the nano-pillar decreases, the  $\chi_{eff}^{(2)}$  is seen to increase. For 150 nm diameter nano-pillar,  $\chi_{eff}^{(2)}$  reaches 136 pm/V, which is  $\sim 7$  times higher than GaN bulk ( $\chi_{33}^{(2)} = \sim 20$  pm/V). The smaller the nano-pillar diameter is, the higher is the surface-to-volume ratio. Consequently, the  $\chi_{eff}^{(2)}$  of small diameter nano-pillars is dominated by the surface term ( $\chi_{sur}^{(2)}$ ).

**Table 2.2** SHG intensity fitting result. The SHG intensity of single GaN nano-pillars is corrected by subtracting the background signal. Two-variable linear regression fitting was applied to retrieve  $A_{\text{sur}} \cdot S^2$  and  $B_{\text{bulk}} \cdot V^2$ .

Nano-pillar diameter (nm)	$S^2$ ( $\text{m}^4$ ) $\cdot 10^{26}$	$V^2$ ( $\text{m}^6$ ) $\cdot 10^{40}$	SHG (counts) Pump at 900 nm	$A_{\text{sur}} \cdot S^2$	$B_{\text{bulk}} \cdot V^2$
150	4.2	0.6	460	287.8	3.9
200	7.4	1.9	643	512.0	12.4
250	12.0	4.5	558	795.7	30.2
300	17.0	9.3	1420	1148.6	62.5
350	23	17	1509	1563.8	116.3
400	30	30	2304	2041.2	198.3



**Figure 2.4.** (Left) the measured SHG and fitting result based on Equation 2.2. (Right) The percentage of SHG generated from the surface (blue) and the bulk (red) are displayed with the surface percentage shown.

Our result and analysis show the surface polarization is dominant when GaN nano-pillar diameter goes below 400 nm. Since the surface polarization is larger than the bulk polarization (summation of the spontaneous and piezoelectric polarizations), when the nano-pillar diameter is reduced, the surface-to-volume ratio increases and increases the  $\chi_{eff}^{(2)}$ . Based on our results, we project when the diameter of nano-pillar is below 50 nm, its  $\chi_{eff}^{(2)}$  will exceed that of LiNbO<sub>3</sub>. This means the electro-optic modulators made with GaN nano-pillars can potentially be efficient linear modulators. The SHG enhancement contributed from nano-pillars surface area can also be applied to other nanostructured materials.

## 2.5 Acknowledgement

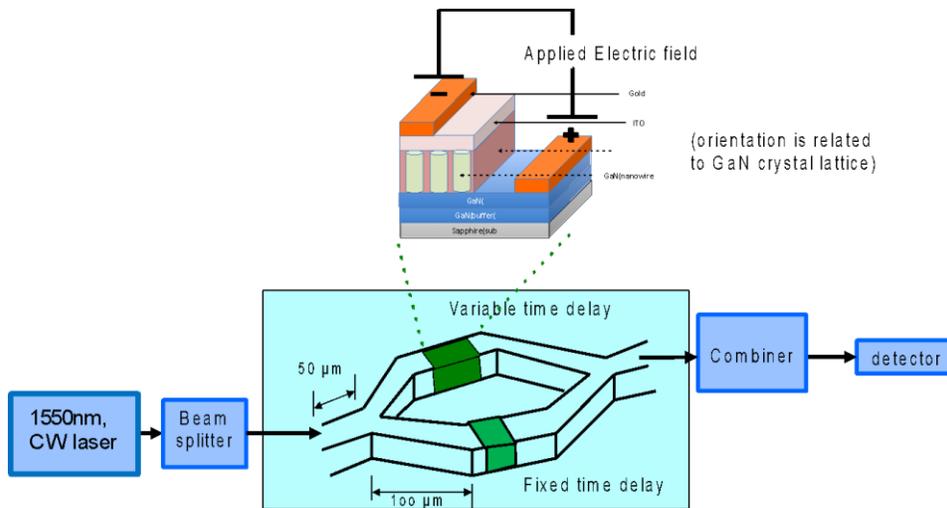
Chapter 2, in full, is currently being prepared for submission for publication of the material. Qian, Haoliang, Liu, Zhaowei, Yu, Paul K. L. The dissertation author was the primary investigator and author of this material. This chapter covers the work of second harmonic susceptibility measurement of single GaN nano-pillars. This work is achieved by Kangwei Wang, Haoliang Qian, Prof. Zhaowei Liu, and Prof. Paul Yu. This work is supported by the ONR-Multidisciplinary University Research Initiative (MURI) (grant number: N00014-13-1-0678). I acknowledge Dr. Maria Isabel Montero Ramirez for electron beam lithography writing, Dr. Dingbo Chen for the nano-pillar fabrication suggestion, Haoliang Qian for the reflective second harmonic measurement, Prof. Zhaowei Liu and Prof. Paul Yu for their guidance of this project.

# CHAPTER 3

## GAN NANO-PILLARS ARRAYED MODULATOR DEVELOPMENT

In chapter 2, we presented the second harmonic susceptibility enhancement in single GaN nano-pillars. The enhancement implies GaN nano-pillars would be a suitable material to implement into a high modulation efficiency EO modulator. In this chapter, we will report the development of GaN nano-pillars arrayed modulator. The device schematic is shown in **Figure 3.1**. It is a Mach-Zehnder modulator (MZM) design: the input light is split in two arms, one arm is set as reference for one light beam which experiences a fixed time delay (also contains GaN nano-pillars array), and at the other arm the other part of the split light experiences the electro-optic effect induced index change which leads to a variable time delay. Since the area of the fundamental mode is  $\sim 2-3 \mu\text{m}^2$ , we simply use a GaN single mode waveguide as a fiber-to-chip edge coupler. The beam splitter (and combiner) can be a Y-branch or a multi-mode interferometer (MMI).

In the following section, we will describe the experimental and simulation results of the beam splitter and the MZM, respectively.

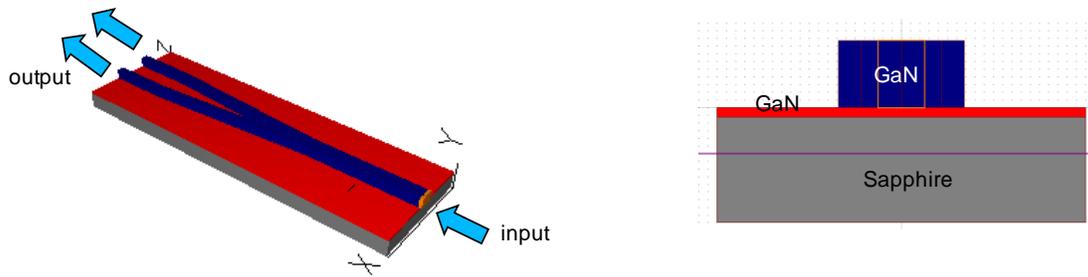


**Figure 3.1.** The schematics of GaN nano-pillars arrayed EO modulator.

### 3.1 GaN beam splitter

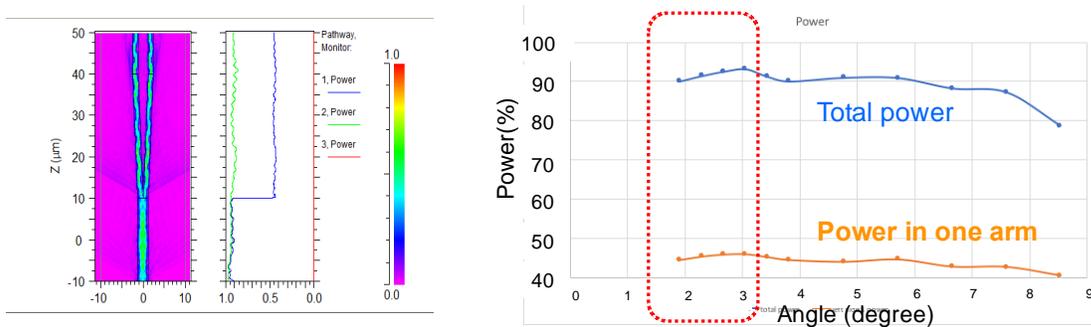
#### 3.1.1 GaN Y-junction beam splitter

We use R-soft CAD simulator which is based on Beam Propagation Method (BPM) to design the Y-junction beam splitter. **Figure 3.2** (left) indicates the Y-junction structure which has one input and two outputs. **Figure 3.2** (right) shows the cross-sectional view of the input GaN ridge waveguide. Due to the EO effect at the MZM section, we intentionally use a 200 nm tall of GaN ridge to conduct the current into the GaN nano-pillars arrayed region.



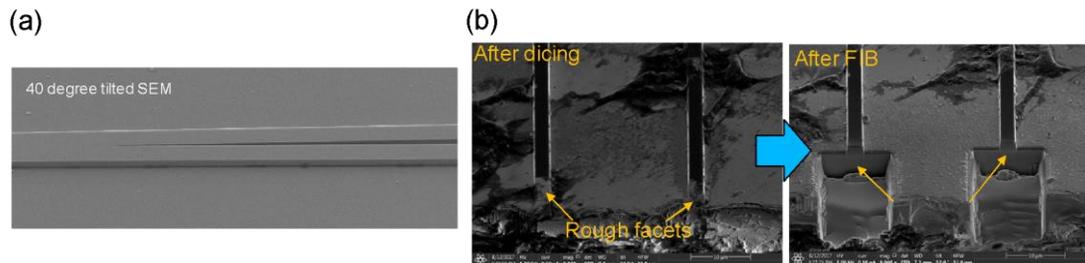
**Figure 3.2.** (Left) The simulated structure of the GaN Y-junction beam splitter. (Right) The cross-sectional view of the ridge GaN waveguide at the input area.

We simulated the power change through different Y-junction angles. **Figure 3.3** (Left) illustrates the monitored power along the z-direction (light propagating direction), the light green line is the total power (summation of two branches), and the blue line is the power in one junction. The power starts to drop around  $4^\circ$  and gradually reduces while the angle increases. Therefore, the designed Y-junction angle is in the range of  $1-3^\circ$ .



**Figure 3.3** (Left) The XZ plan view of the simulated structure.  $\lambda_0=1550$  nm, splitting angle= $3^\circ$ . (Right) The total power and the power in one arm vs. the splitting angle.

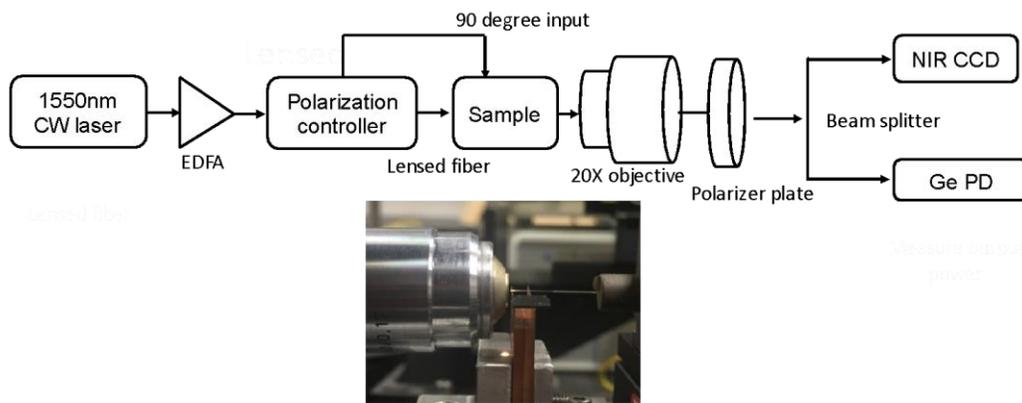
The GaN Y-junction splitter is fabricated through the following steps: A 2.5  $\mu\text{m}$  thick GaN is grown on a 2" single side polished (SSP) epi-ready grade sapphire wafer. The Y-junction is then patterned by electron beam lithography (EBL) with a negative E-beam resist, HSQ. The HSQ will convert into a  $\text{SiO}_2$ -like solid mask after the EBL writing and can be used as the mask for GaN dry etch. We perform a reactive-ion etching (RIE) only dry etch with a mixture of  $\text{Cl}_2$  and  $\text{BCl}_3$ . **Figure 3.4(a)** shows a 40 degree angle tilted view of the fabricated Y-junction splitter with a 3 degree splitting angle. To evaluate its optical properties, we diced the sample at its input and two outputs edges to couple with the lensed fiber. A focused-ion beam (FIB) polishing is applied to all three waveguide coupling facets (one input and two outputs) to reduce the fiber-to-chip coupling loss. **Figure 3.4(b)** compares the facets before and after the FIB polishing.



**Figure 3.4** (a) The 40 degree angle tilted SEM image of the GaN Y-junction splitter. (b) Comparison of the two output facets before and after the FIB polishing.

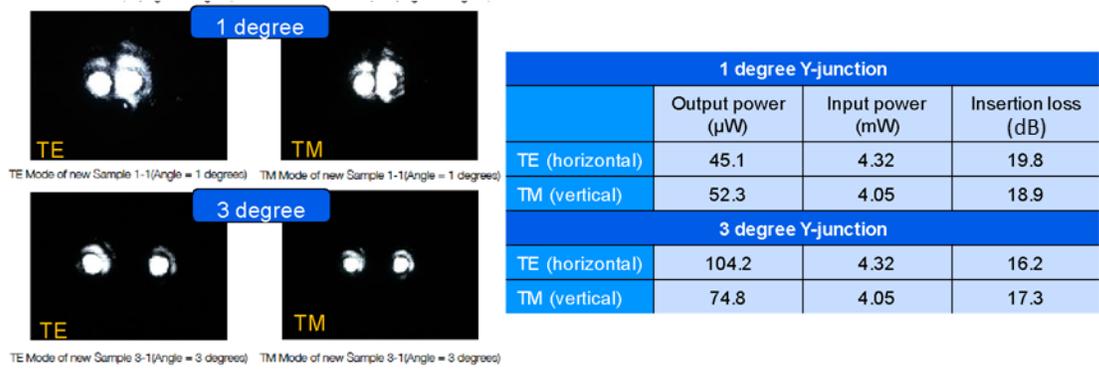
The Y-junction is mounted on an optical measurement setup (**Figure 3.5**) in our lab. The 1550 nm wavelength light from a CW tunable laser couples about 1mW optical power to the Erbium-doped fiber amplifier (EDFA), which leads to an output power in the 25 mW to 64 mW (14-18 dBm) range. The light went through the polarization controller before coupled into the splitter. The propagating light then split into two arms at the Y-junction

splitter, the output light is collected by the 20X objective lens focused at the output facets. We used a rotatable polarizer plate to select the TE/TM mode (which we can see at the near-Infrared CCD) and record the output power using a large area Ge photodetector. To assist the lensed fiber-to-splitter alignment, the  $\lambda_0=1550$  nm CW laser can be replaced by a 785 nm CW ruby laser to visualize the coupling at the input.



**Figure 3.5.** The optical measurement setup.

The optical measurement results are shown in **Figure 3.6**. Both  $1^0$  and  $3^0$  Y-junction showed similar mode profile and insertion loss. The insertion loss is the sum of fiber-to-chip coupling loss, propagation loss, Y-junction bending loss, and  $90^0$  bending loss. Based on the preliminary simulation, the Y-junction bending loss should be less than 0.05 dB at the splitting angle  $\leq 3^0$ . Further investigation is needed to understand the measured large insertion loss of this device.

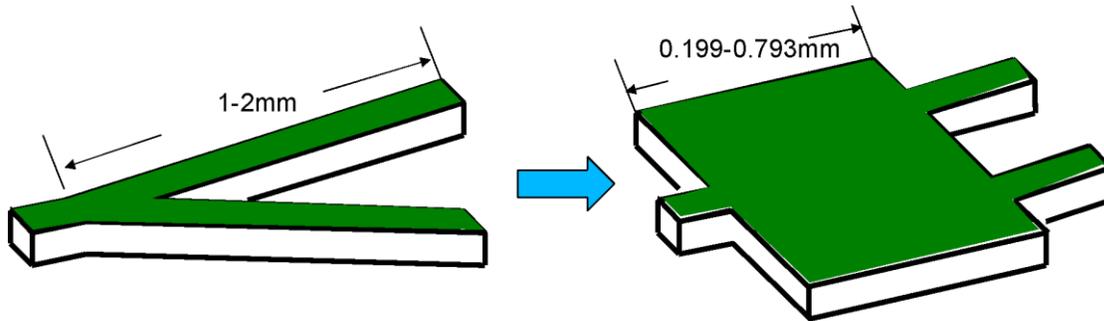


**Figure 3.6.** (Left) The TE/TM mode profile of  $1^\circ$  splitting angle and  $3^\circ$  splitting angle Y-junction. (Right) The summary table of TE/TM mode output power and insertion loss of  $1^\circ$  splitting angle and  $3^\circ$  splitting angles, respectively.

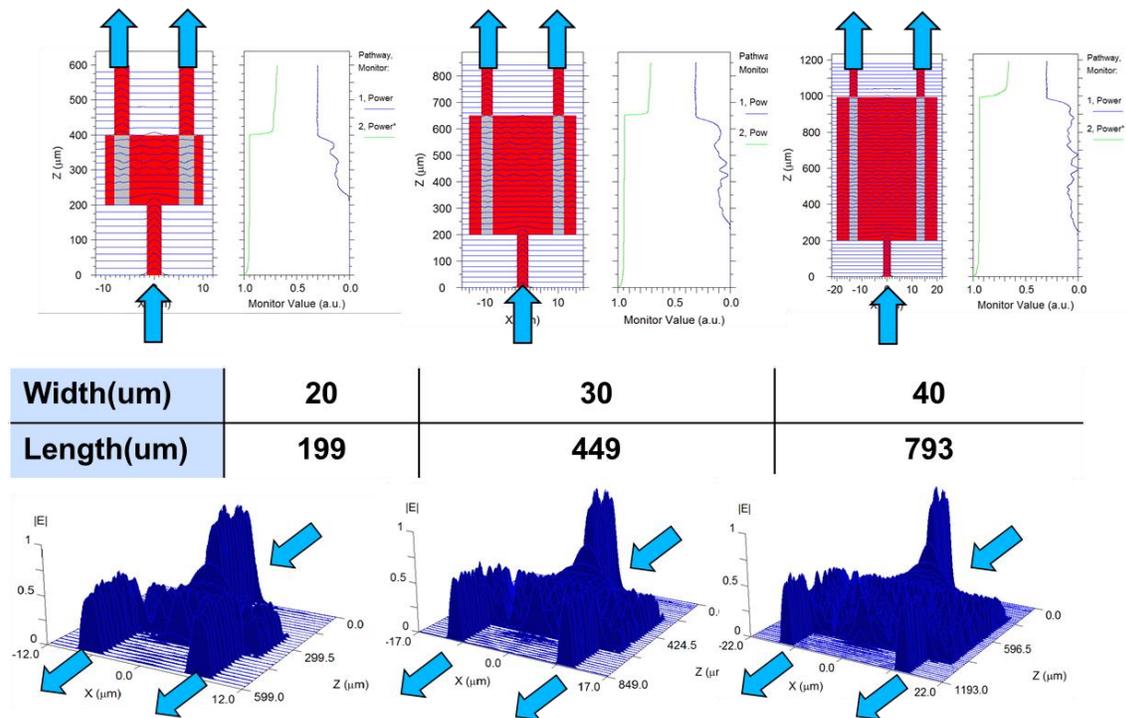
### 3.1.2 Multi-mode interferometer (MMI) beam splitter

Another kind of beam splitter is the Multi-mode interferometer (MMI). Consider the Y-junction beam splitter, the splitting angle is less than  $4^\circ$ . To have a sufficiently large spatial separation between the two arms for electrical isolation during modulation, the length of the Y-junction branch would be 1-2 mm. Since the GaN waveguide propagation loss is an order of magnitude higher than that of LiNbO<sub>3</sub> (GaN propagation loss of 3.4 dB/mm and 1.5 dB/mm are reported, respectively [32] [33]), we anticipate that, using an MMI instead of a Y-junction, the average splitter length can be reduced by a factor of three thus reduces the propagation loss (**Figure 3.7**). In **Figure 3.8**, we design three MMI couplers with three different widths: 20 μm, 30 μm, and 40 μm, and utilize R-soft CAD simulator based on Beam Propagation method (BPM) to find the optimized length to achieve the highest output power. To incorporate the MMI design into the modulator

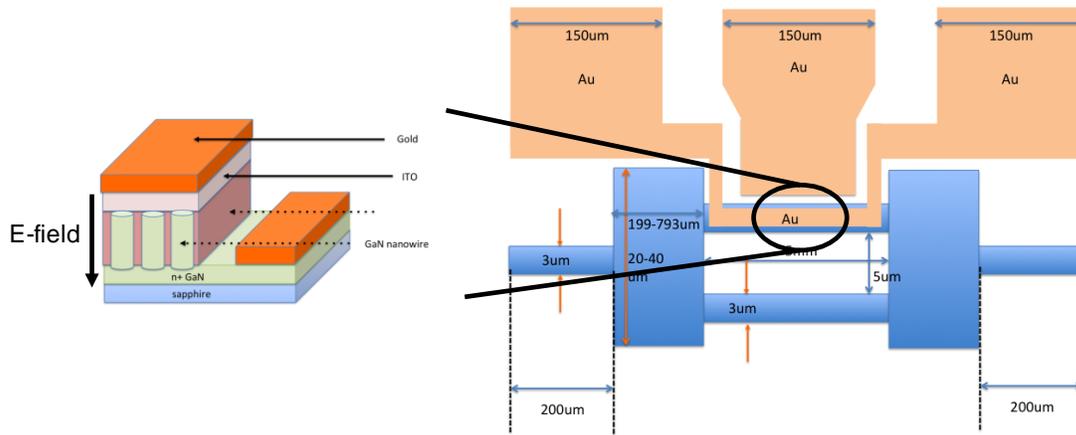
structure, **Figure 3.9** shows the integrated MMI as the beam splitter with the GaN nano-pillars arrayed waveguides.



**Figure 3.7** Comparison of the splitter length in a Y-junction and length of a MMI.



**Figure 3.8.** the R-soft Beam Prop simulation results of three different width/length combinations of MMI couplers.



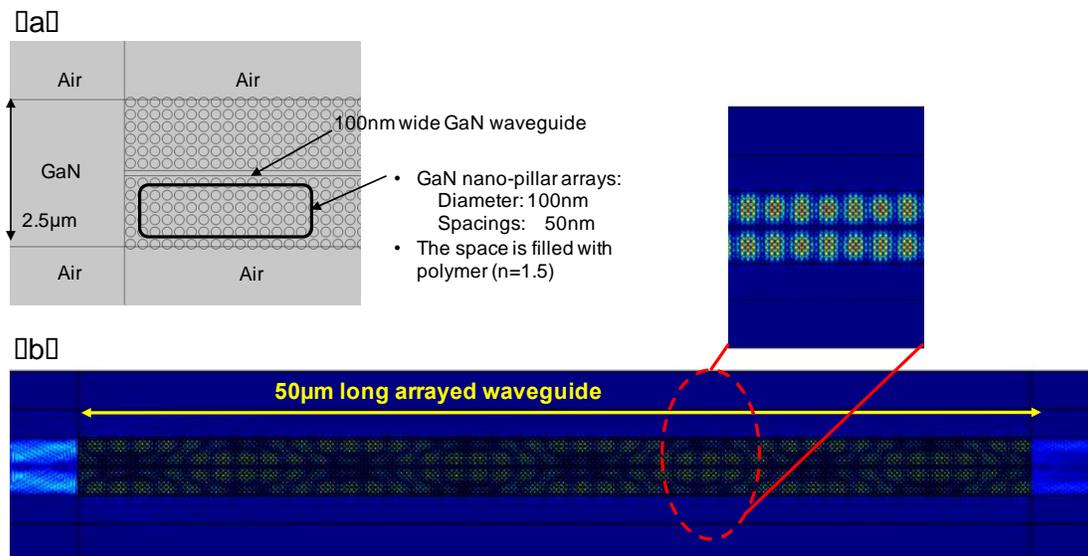
**Figure 3.9.** The design of GaN nano-pillars arrayed MZM using the MMI beam splitter.

## 3.2 GaN nano-pillars arrayed Mach-Zehnder modulator (MZM)

### 3.2.1 GaN nano-pillars arrayed waveguide simulation

This section presents the simulation, fabrication, and optical measurement results of GaN nano-pillars arrayed waveguide. The biggest concern of the GaN nano-pillars arrayed MZM is the propagation loss of the GaN nano-pillars arrayed waveguide. Because of the index mismatch between the GaN waveguide and the nano-pillars arrayed waveguide, it will have high light reflection at the interface. The purpose of the simulation is to design the GaN nano-pillar with proper individual pillar diameter, pillar-to-pillar spacing, and the cladding material refractive index to raise the effective refractive index of nano-pillars arrays region. We utilize the COMSOL simulator to realize the parameters just listed. We choose the HSQ as the cladding (filling-in) material which has a refractive index of 1.5. HSQ is used as the mask for nano-pillars array patterning and it converts into SiO<sub>2</sub> and fills in the spacing between nano-pillars after EBL writing. **Figure 3.10.** shows the simulation

result under the GaN nano-pillar diameter: 100 nm, pillar-to-pillar spacing: 50 nm. The 1550 nm center wavelength light originally is guided in a 2.5  $\mu\text{m}$  wide, 2.5  $\mu\text{m}$  high GaN waveguide before entering the nano-pillars array region. Subsequently the light propagates through a 50  $\mu\text{m}$  long arrayed waveguide region. It should be noted that we design a 100 nm wide GaN rectangular structure at the middle of the nano-pillars array region to assist light guiding.

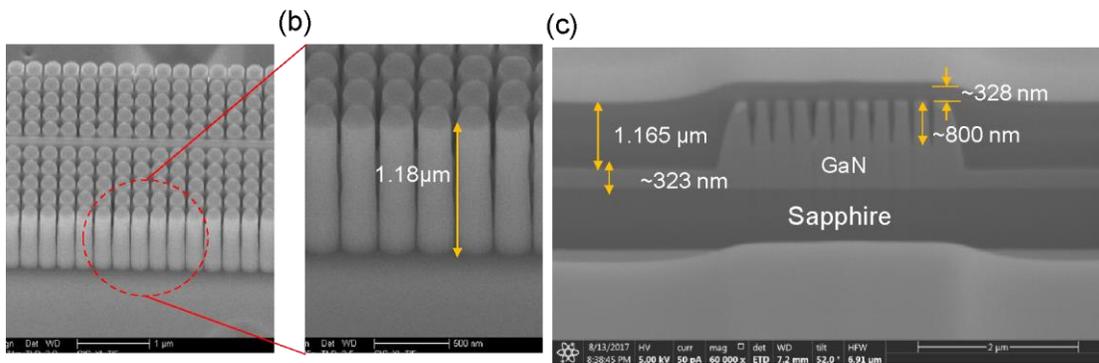


**Figure 3.10.** (a) The GaN nano-pillars arrayed waveguide design parameters for COMSOL simulation. (b) Using a 50  $\mu\text{m}$  long arrayed waveguide to test the light propagation.

### 3.2.2 GaN nano-pillars arrayed waveguide fabrication

The GaN nano-pillars arrayed waveguide pattern is based on the simulated parameters in Section 3.2.1. We first grew a layer of GaN on a 2" single side polished (SSP) sapphire. The EBL dose test and sample runs were done in CINT/ Sandia National Laboratories by another Ph.D. student, Renjie Chen in Prof. Shadi Dayeh's group at UCSD. We chose a

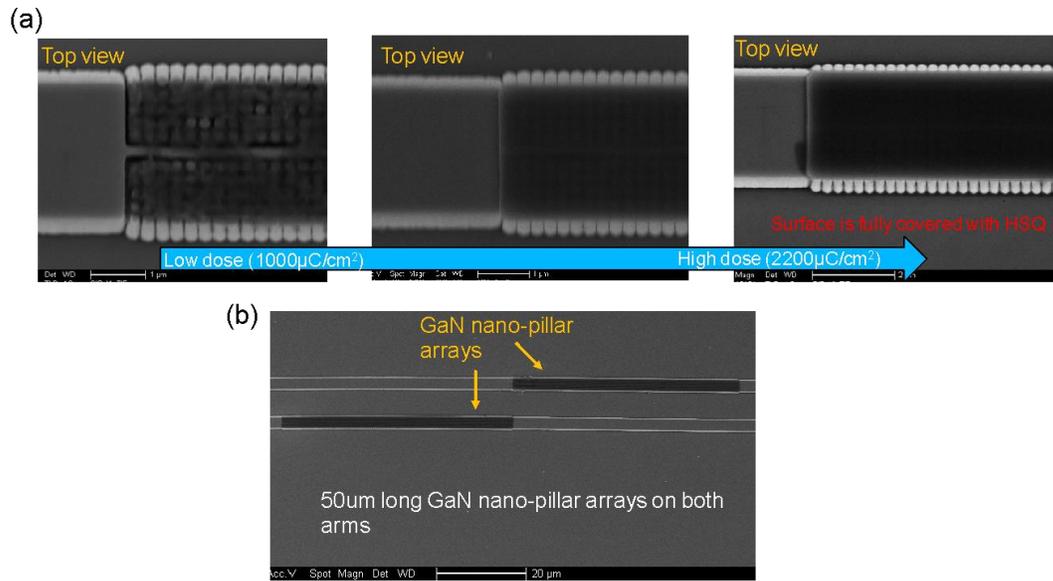
negative e-beam resist, HSQ, which was converted into a SiO<sub>2</sub>-like material after the EBL writing. The SiO<sub>2</sub>-like material acts as a dry etch mask in the GaN dry etch process. After dry etch, we achieved a 1.18 μm high GaN nano-pillars array. (**Figure 3.11-(a-b)**). Next, the SiO<sub>2</sub>-like HSQ mask was removed by BOE wet etch the sample was recoated with a new layer of HSQ. The purpose of recoating a new HSQ was to fill the spacing in the GaN nano-pillars arrayed region to increase the effective refractive index of the region. Also, it created a spacer between the top metal electrode and nano-pillars. **Figure 3.11(c)** shows the recoated HSQ fully fills the spacing of GaN nano-pillars arrayed region and keeps a ~328 nm spacing between the nano-pillars top and the air.



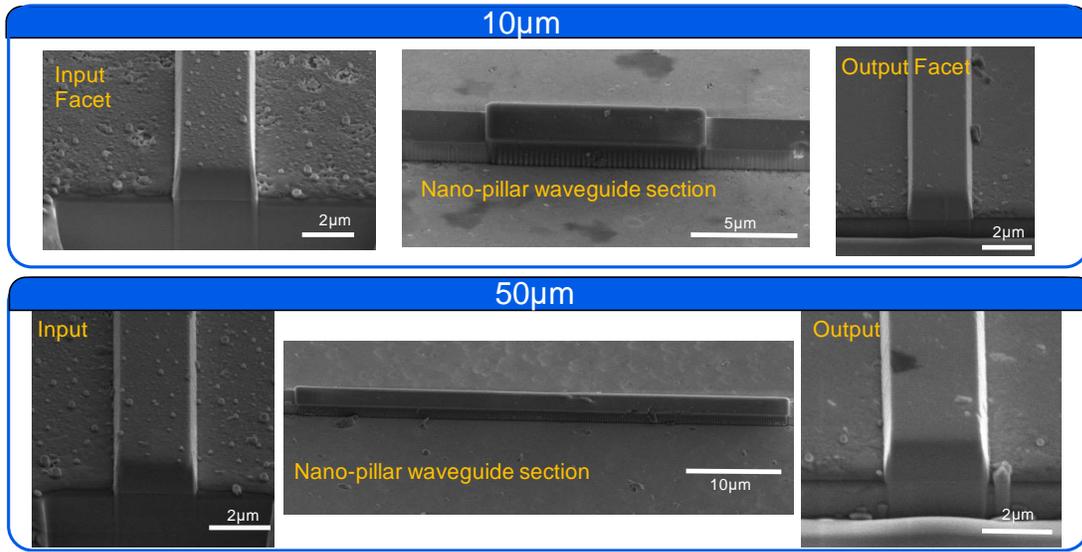
**Figure 3.11** (a) The 40 degree angle tilted SEM image of the GaN nano-pillars arrayed waveguide (b) The zoom in image to show the height of the GaN pillar is 1.18 μm (c) The cross-sectional SEM image of the GaN nano-pillars array which is coated with SiO<sub>2</sub>-like material.

Second EBL is written on the re-coated HSQ. **Figure 3.12** indicates the dose test result. When the dosage went beyond 2200 μC/cm<sup>2</sup>, the SiO<sub>2</sub>-like layer fully covered 50 μm long GaN nano-pillars arrayed waveguide at both arms. (**Figure 3.12(b)**). Notice that we design an asymmetrical nano-pillars arrayed waveguide such that one arm performs EO

modulation while the other arm serves as a reference. Both arms have nano-pillars array so that their propagation loss is maintained at the same level.



**Figure 3.12.** (a) The dose test result of the 2<sup>nd</sup> EBL writing. (b) The top view SEM image of the asymmetrical GaN nano-pillars arrayed waveguides on two arms.

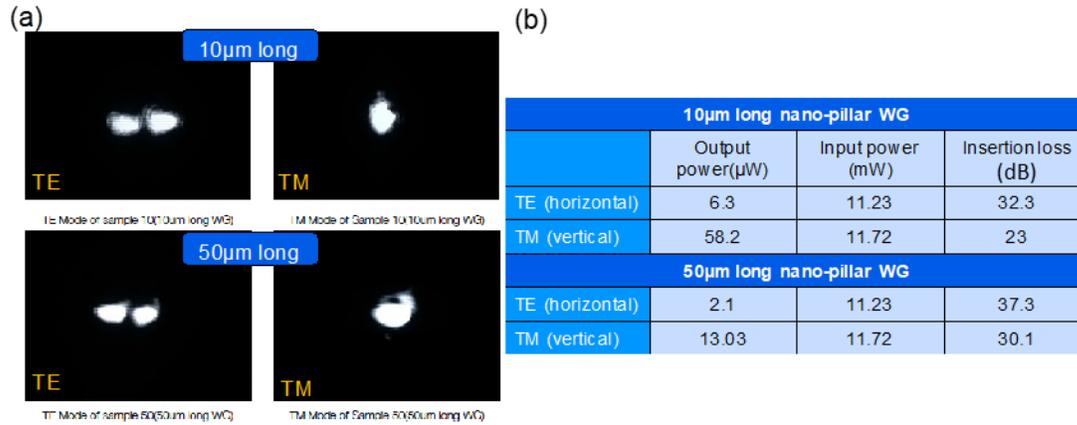


**Figure 3.13.** The 52 degree angle tilted SEM images of input facet, the GaN nano-pillars arrayed waveguides, and the output facet. (Upper) 10  $\mu\text{m}$  long of the nano-pillars arrayed section. (Lower) 50  $\mu\text{m}$  long of the nano-pillars arrayed section.

To reduce the lensed fiber-to-chip coupling loss, we used the focused-ion beam (FIB) to polish the input and output of 10  $\mu\text{m}$  and 50  $\mu\text{m}$  long GaN nano-pillars waveguides. All facets showed very clear contrast between the GaN layer and the Sapphire substrate. **(Figure 3.13)**

Last, we utilized the same optical measurement setup in **Figure 3.5** to evaluate the arrayed waveguides. Both 10  $\mu\text{m}$  and 50  $\mu\text{m}$  long GaN nano-pillars arrayed waveguides showed similar mode profile (**Figure 3.14-(a)**). This was the first time a GaN nano-pillars arrayed waveguide was fabricated, its optical mode profile is observed, and its insertion loss measured. Assuming the coupling loss was the same for these two nano-pillars arrayed

waveguides, the propagation loss of GaN nano-pillars arrayed waveguide was extracted to be 0.13 dB/ $\mu\text{m}$  (TE) and 0.18 dB/ $\mu\text{m}$  (TM).



**Figure 3.14** (a) The observed TE and TM mode profile from a 10  $\mu\text{m}$  (upper figure) and 50  $\mu\text{m}$  (lower figure) long GaN nano-pillars arrayed waveguide; (b) The measured input/output power and insertion loss of two different lengths of GaN nano-pillars arrayed waveguides.

### 3.3 Summary

For incorporating the GaN nano-pillars array in an EO modulator device, we design the scheme of GaN nano-pillars arrayed Mach-Zehnder modulator (MZM). Two kinds of beam splitters: Y-junction and MMI were examined by BPM simulation. We selected the Y-junction splitter design and fabricated two devices which have  $1^\circ$  and  $3^\circ$  branching angles respectively. The optical measurement result indicates the  $3^\circ$  branching angle splitter has a slightly lower insertion loss. For GaN nano-pillars arrayed waveguide, we simulated an arrayed waveguide with a narrow, centered GaN waveguide and the pillar-to-pillar spacing is filled with a  $\text{SiO}_2$ -like E-beam resist. Two different lengths (10  $\mu\text{m}$  and 50

$\mu\text{m}$ ) of the GaN nano-pillars arrayed waveguide were fabricated. Their TE/TM mode profiles were recorded, and their insertion loss and propagation loss were evaluated.

### **3.4 Acknowledgment**

This work is supported by the ONR-Multidisciplinary University Research Initiative (MURI) (grant number: N00014-13-1-0678). I would like to acknowledge the CINT/Sandia National Laboratories for E-beam lithography support, Dr. Renjie Chen, and Woojin Choi for the nano-pillars arrayed waveguide fabrication, all the UCSD Nano3 clean room staffs, and the fruitful discussion with Dr. Steve Pappert, Dr. CK Sun (VEO), Prof. Shadi Dayeh, Dr. Dingbo Chen (VEO), and Prof. Paul Yu.

# CHAPTER 4

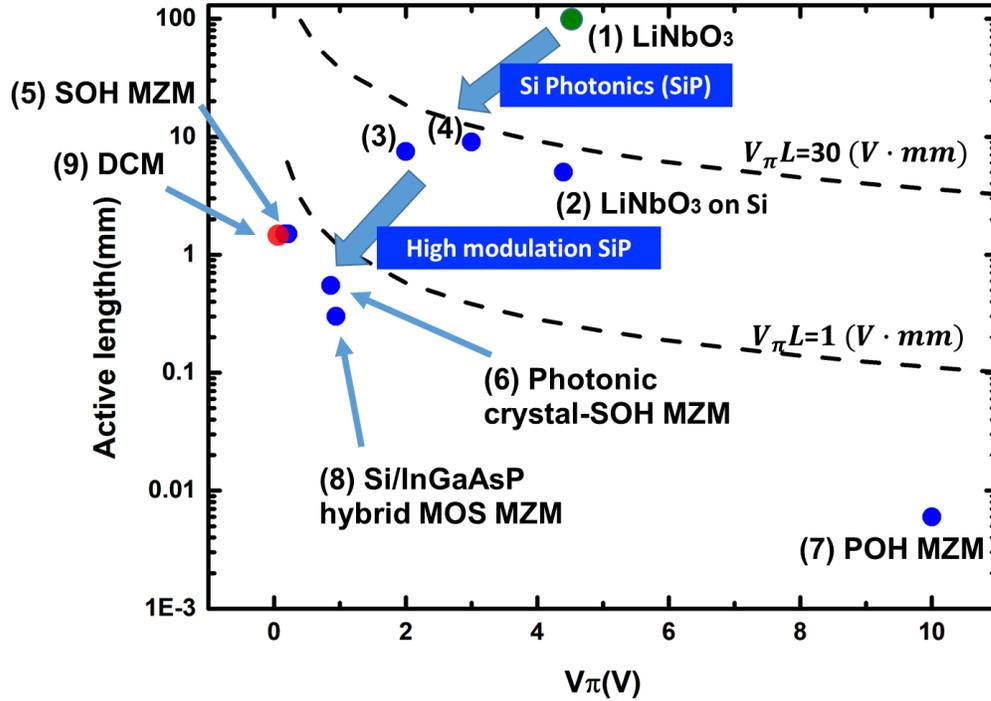
## NANO-SLOT CONDUCTIVE WAVEGUIDE OPTICAL MODULATOR- DESIGN, SIMULATION, AND PROOF OF PRINCIPLE

### 4.1 Introduction

Ultra-high speed (beyond 100 Gbps per wavelength), low power consumption optical interconnects are vital elements in future data centers [34] [35] and 5G network architectures [36]. Scaling information capacity in an energy efficient manner poses a severe challenge to network architects. A critical component within the optical interconnect that dictates the capacity and power consumption scaling is the optical transmitter using direct modulation or external modulation [37] [38] [39] [40]. Direct laser modulation techniques such as the current modulated Vertical-Cavity Surface-Emitting Laser (VCSEL) are currently limited to  $< 50$  GHz and appear to be near the end of their frequency scaling capability [38] [39] [40]. External modulation with an integrated optical modulator provides the most promising path for bandwidth and drive power improvements. Several types of external modulators have been used in the optical links and interconnects [41]. In past decades, traveling-wave  $\text{LiNbO}_3$  integrated optical modulators have been the standard for achieving high speed and low drive voltage in a low optical insertion loss device [42].

The LiNbO<sub>3</sub> device length requirements (> 10 cm) for low voltage operation inhibits this high-speed modulation platform for many large-scale data networking applications (**Figure 4.1, Point 1**). Recently, a LiNbO<sub>3</sub> modulator on Silicon substrate has been demonstrated but it too lacks the voltage-length product scaling ( $V_{\pi}L \sim 2.2\text{V}\cdot\text{cm}$ ) for it to be a serious future network candidate (**Figure 4.1, Point 2**). [43] Electro-absorption modulated lasers (EML) are currently the best available commercial solution to meet the need of > 100 Gbps optical interconnect [44] [45]. More recently, due to the growth of Silicon Photonics (SiP), pure-play foundries have built up its library for most passive and active photonic components, such as grating coupler, splitter, ridge waveguide, photo detector, and depletion-mode PN modulator [46] [47] [48]. Due to the absence of intrinsic Pockels effect in Si, Si-based optical interconnects with Silicon active layer rely on the plasma-dispersion effect and suffer weak phase-modulation efficiency in metal-oxide-semiconductor (MOS) junction [49] or forward [50]/reverse [51] [52] biased PN junction (**Figure 4.1, Points 3 and 4**). Depletion mode (reversed biased) modulators have been demonstrated up to 70 Gbps with band equalization, but the modulation efficiency is high with a voltage-length product of  $V_{\pi}L > 10\text{V}\cdot\text{mm}$  [53]. Currently, single- $\lambda$  25 Gbps SiP interconnects deliver 100 Gbps by employing PAM-4 signal formats [54]. Seeking an energy efficient transceiver solution to go beyond the single- $\lambda$  100 Gbps remains a key challenge. Several approaches have been reported. Silicon organic hybrid (SOH) MZMs enable  $V_{\pi}L$  modulation efficiency improvement (**Figure 4.1, Point 5**) by filling a nano-slot with a high EO coefficient ( $r_{33}$ ) chromophore [55]. To further improve the modulation efficiency, photonic crystal waveguide (PCW) MZM utilizing the slow-light effect [56] has demonstrated a  $V_{\pi}L$

of  $0.282\text{V}\cdot\text{mm}$  (**Figure 4.1, Point 6**), but the trade-off is high series resistance of the photonic crystal slab which limits its  $1/2\pi RC$  bandwidth. Plasmonic organic hybrid (POH) MZM shows extremely high modulation efficiency ( $V_\pi L$  of  $0.06\text{V}\cdot\text{mm}$ ), but the high propagation loss ( $\sim 125\text{ dB/mm}$ ) due to metallic absorption makes it difficult to bring down its  $V_\pi$  to sub-volt range (**Figure 4.1, Point 7**) [57]. In addition to the silicon-organic hybrid (SOH) MZM, Jae-Hoon Han *et al* reported a  $\text{Si}/\text{In}_{1-x}\text{Ga}_x\text{As}_y\text{P}_{1-y}$  hybrid MOS MZM design (**Figure 4.1, Point 8**). The low effective mass of the silicon hole,  $m_{\text{ch}}$ , and high electron mobility,  $\mu_e$ , of  $\text{In}_{1-x}\text{Ga}_x\text{As}_y\text{P}_{1-y}$  enable a device with 17 times higher  $\Delta n$ , and half of the optical absorption,  $\Delta\alpha$ , compared with Si-based MOS MZM. The reported  $V_\pi L$  of  $0.47\text{V}\cdot\text{mm}$  is an exceptional result [58].



**Figure 4.1.** Benchmarking recent developed optical modulators in terms of device active length and  $V_{\pi}$ . Note that the green dot stands for commercially available modulator product, blue dots stand for the modulator under academic research, and the red dot is our proposed nano-slot DCM.

In this chapter, we analyze a directional coupler modulator (DCM) proposed by CK Sun et al [59] [60]. DCM has a nano-slot (50-160 nm) between two conductive Si waveguides. With the improvement of modern microelectronic fabrication technology, mainly the development of high resolution lithography and accurate localized ion-implantation, we are able to fabricate this DCM structure. Ultra-short cross coupling length and sensitive EO polymer project a switching efficiency around  $0.21\text{V}\cdot\text{mm}$  (**Figure 4.1, point 9**), a noteworthy result compared with past DCM demonstrations.

## 4.2 Novel DCM operational principle and simulation results

Traditional DCMs suffered from high drive voltage in the past caused by wide cross-coupling region ( $\geq 3\mu\text{m}$ ) [61] and inefficient electrical to optical field confinement [62]. Due to more recent advancement in nano-wire silicon photonics, strong optical confinement is observed in the nano-slot (50 nm wide) silicon waveguide [63]. By reconditioning the optical input, this same nano-slot waveguide can be converted into cross-coupled optical waveguides having a nano-slot cross-coupling region, filled with EO sensitive polymer as is shown in **Figure 4.2**. This novel DCM structure can harvest both strong slot optical confinement and high electric field confinement, employing both doped silicon optical waveguides as two electrical contacts. Two adiabatically cross-coupled input bends are used to launch proper modes into the DCM waveguides. Optical switching between the two output ports can be achieved by changing the refractive index of the slot-filled EO polymer, influenced by a switching voltage  $V_\pi$  and its respective electric field applied across the slot region. Using a polymer that exhibits a strong  $r_{33}$  Pockels effect [64], an efficient refractive index change  $\Delta n_{slot}$  can be expressed as:

$$\Delta n_{slot} = \frac{-r_{33}n_0^3V}{2W_s} \quad \text{(Equation 4.1)}$$

where  $W_s$  is the slot width,  $V$  is the voltage across the nano-slot, and  $n_0$  is the polymer refractive index.

An ultra-short cross-coupling length  $L_c$  can be achieved in this novel silicon DCM by maximizing differences between the effective index  $N_s$  (fundamental symmetric mode) and  $N_a$  (first order anti-symmetric mode) at the given optical wavelength  $\lambda$ , and

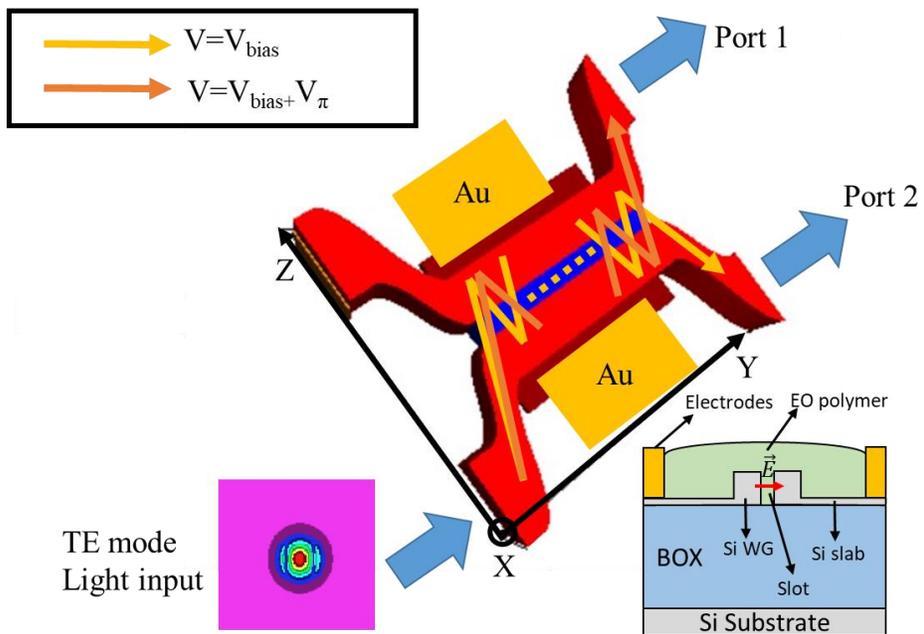
$$L_c = \frac{\lambda}{2(N_s - N_a)} \quad \text{(Equation 4.2)}$$

The effective indexes can be computed using numerical tools, such as R-Soft Beam Prop method [65], given a DCM geometry. With 260 nm silicon waveguide width, 330 nm height, 120 nm slot-width, 2  $\mu\text{m}$  thick buried oxide layer, 1.55  $\mu\text{m}$  TE optical input, and polymer cladding of 1.69 refractive index, **Figure 4.3** depicts dominant modal patterns and their corresponding  $N_s$  of 2.29 and  $N_a$  of 1.96. Two mode interference can create an ultra-short  $L_c$  in the proximity of 2  $\mu\text{m}$ .

Varying the effective indexes  $N_s$  and  $N_a$  through the Pockel's effect changes  $L_c$  [66], and the DCM switching voltage  $V_\pi$  can be derived through the condition,

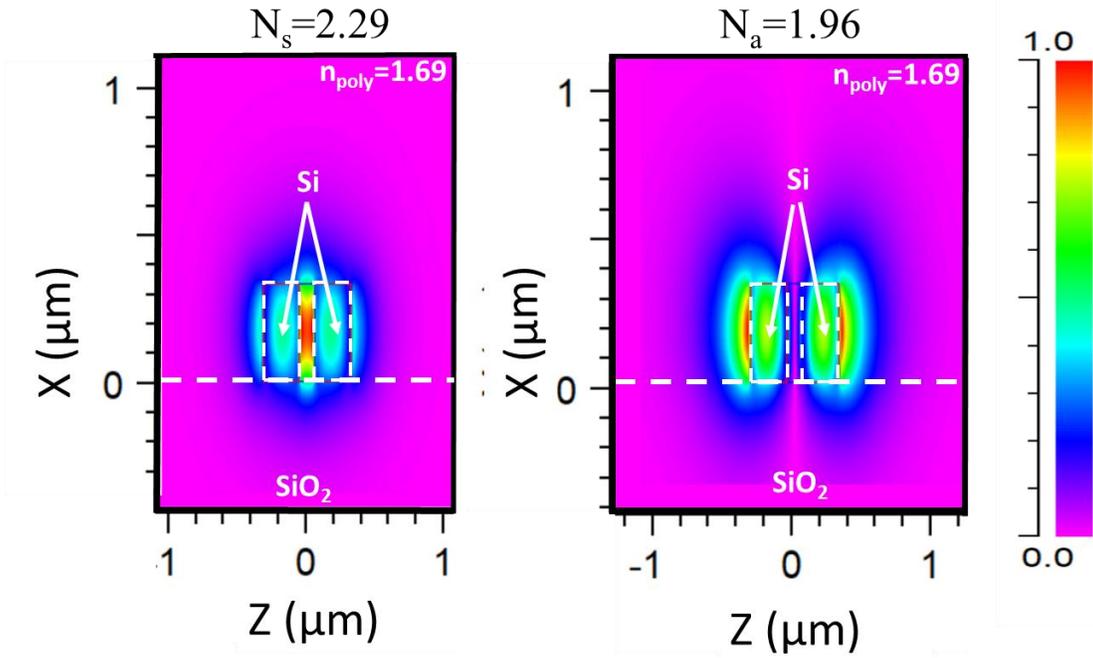
$$\left| \frac{L}{L_{c0}} - \frac{L}{L_{c1}} \right| = 1 \quad \text{(Equation 4.3)}$$

where  $L$  is the device length,  $L_{c0}$  is the coupling length when  $V$  is at  $V_{bias}$ , and  $L_{c1}$  is the coupling length when  $V = V_{bias} + V_\pi$ .



**Figure 4.2.** Schematic diagram of the nano-slot conductive waveguide DCM. Lower right is the cross-sectional view of the device.

$E_z$  mode profile



**Figure 4.3** An example of the fundamental symmetric mode, with index  $N_s$  (left) and 1<sup>st</sup> order anti-symmetric mode, with index  $N_a$  (right) at 260 nm waveguide width, 330 nm waveguide height, 120 nm slot width, and both nano-slot and surrounding are filled with a refractive index,  $n=1.69$  polymer.

The DCM switching efficiency ( $V_\pi L$ ) strongly depends on the slot width. Referring to **Figure 4.3**, by using waveguides as electrical contacts,  $V_\pi$  contributes primarily to the electric field change in the slot region. This creates an efficient change in  $N_s$  of the fundamental symmetric mode. On the other hand, little change in  $N_a$  of the anti-symmetric mode since it contains minimum energy in the slot region. Defining  $\gamma$  as the modal ratio number and setting  $\Delta N_s = \gamma \Delta N_a$ , the switching condition according to **Equation 4.2** and **4.3** can be expressed as

$$\left(1 - \frac{1}{\gamma}\right)\Delta N_s = \frac{\lambda}{2L} \quad \text{(Equation 4.4)}$$

Furthermore,  $\Delta N_s$  can be expressed as  $\sigma' \Delta n_{slot}$  where  $\sigma'$  is the optical mode confinement factor. Using **Equation 4.1**,  $V_\pi$  can be stated as:

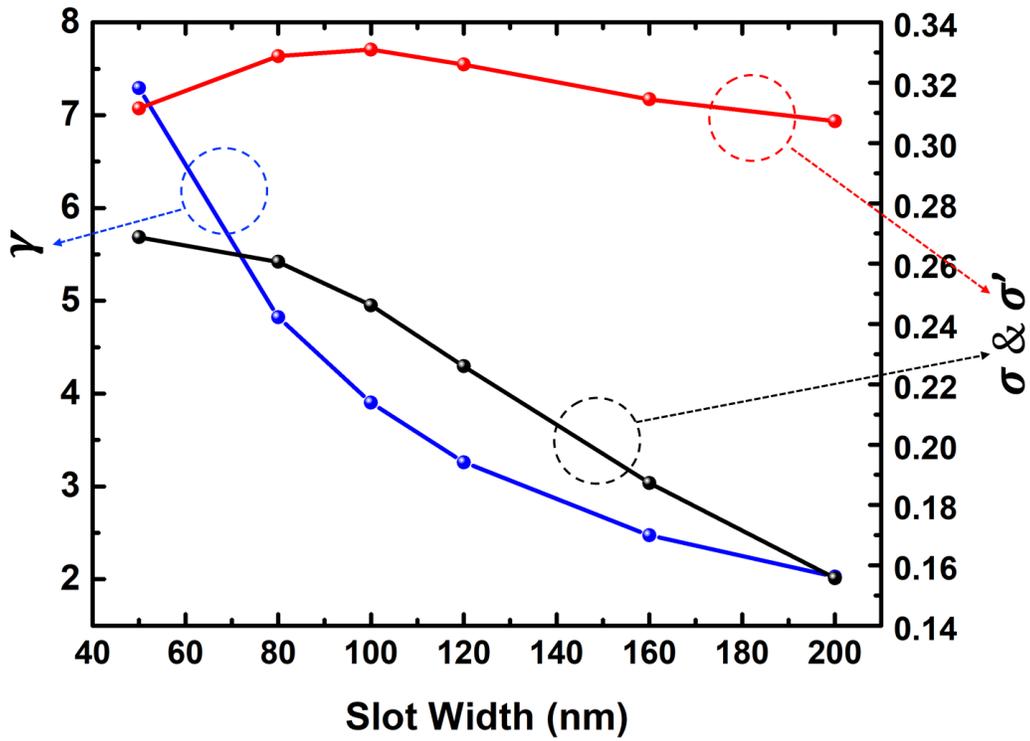
$$V_\pi = \frac{\lambda W_s}{2L r_{33} n_0^3 \sigma'} \left( \frac{\gamma}{\gamma - 1} \right) \quad \text{(Equation 4.5)}$$

Here we include a reduction of drive voltage by a factor of 2, assuming a differential signal is applied to the two contacts [67] [68]. The relationship of  $\sigma'$  and  $\gamma$  in **Equation 4.5** can be consolidated into an effective confinement factor  $\sigma$ , where  $V_\pi L$  can be calculated as

$$V_\pi L = \frac{\lambda W_s}{2 r_{33} n_0^3 \sigma} . \quad \text{(Equation 4.6)}$$

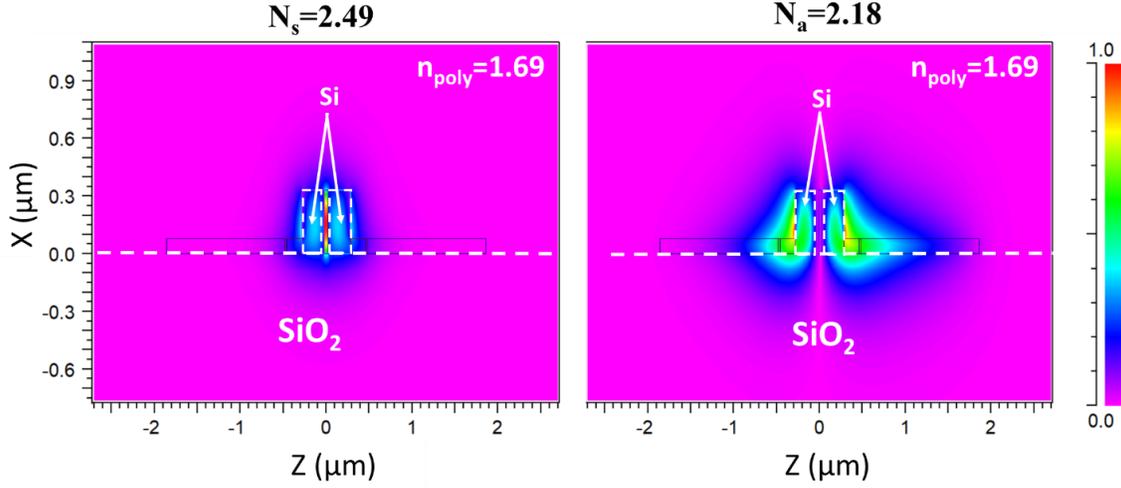
With  $W_s$  of 80 nm,  $r_{33}$  of 100 pm/V, and  $\sigma$  of 0.2, one can easily compute the switching efficiency of the DCM to be in the range of sub 1V·mm, and this is the highest reported DCM switching efficiency [61] [62].

For a given waveguide height, the effective confinement factor  $\sigma$  decreases with slot width increase. Primarily,  $\gamma$  degrades as 1<sup>st</sup> order asymmetric mode overlap increases in the slot region. **Figure 4.4** shows  $\gamma$ ,  $\sigma'$ , and  $\sigma$  at various slot width from 50 nm to 200 nm.



**Figure 4.4.** The effective modal number  $\gamma$  related to both  $N_s$  and  $N_a$ , the optical confinement factor  $\sigma'$ , and the effective confinement factor  $\sigma$ , computed as slot width varying from 50 nm-200 nm.

### $E_z$ mode profile



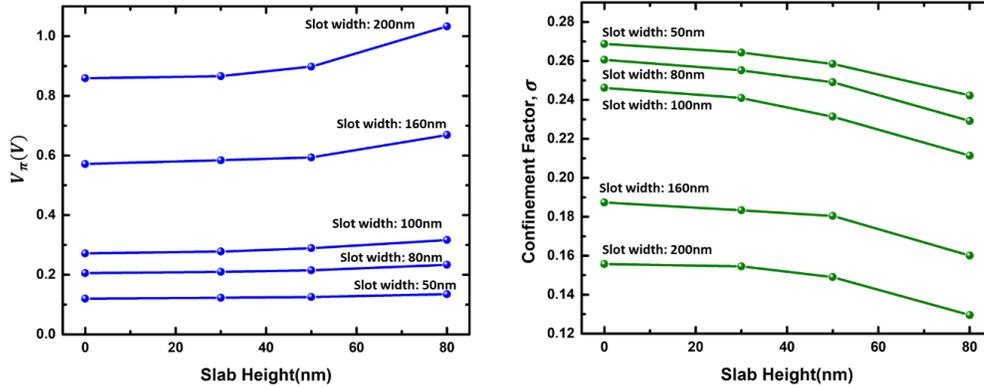
**Figure 4.5.** (Left) the fundamental symmetric mode profile, with index  $N_s$ . (Right) the 1<sup>st</sup> higher order anti-symmetric mode profile, with index  $N_a$ . the slab height is 80 nm.

It is observed that the highly doped silicon slabs used to connect the two conductive optical waveguides do affect  $L_c$ . Referencing **Equation 4.2** and **Figure 4.5**, both  $L_c$  and  $N_a$  grow rapidly with increasing slab height as the 1<sup>st</sup> order antisymmetric mode experiences higher indexes from the slab region, while less changes to  $N_s$  in the slot region. However, the effective confinement factor  $\sigma$  and the corresponding  $V_\pi$  are less impacted by the slab height increase. **Table 4.1** depicts computed  $\gamma$ ,  $\sigma'$ ,  $\sigma$ , and  $V_\pi$  of four DCMs with slab height ranging from 0 to 80 nm, using the same  $r_{33}$  of 160 pm/V,  $L$  of 1500  $\mu\text{m}$ , and  $W_s$  of 50 nm. Although **Table 4.1** exhibits a slight decrease of optical confinement  $\sigma'$ , its decrease is balanced by the increase of  $\gamma$ , when  $N_a$  is more influenced by the slab height and less influenced by the change of  $N_s$ . **Figure 4.6** summarizes both  $V_\pi$  and  $\sigma$  in 50 nm,

80 nm, 100 nm, 160 nm, and 200 nm slot width DCMs, each having four slab height variation of 0 nm, 30 nm, 50 nm, and 80 nm.

**Table 4.1.** Comparison of the  $\gamma$ ,  $\sigma'$ ,  $\sigma$ , and  $V_\pi$  of four same slot-width DCMs with slab height of 0, 30, 50, and 80 nm.  $L$  is 1500  $\mu\text{m}$ .

Slab Height(nm)	$\gamma(\frac{\Delta N_s}{\Delta N_a})(\text{a.u.})$	$\sigma'(\frac{\Delta N_s}{\Delta n_{slot}})(\text{a.u.})$	$\sigma(\sigma' \frac{\gamma-1}{\gamma})$	$V_\pi(\text{V})$
0	7.3	0.311	0.269	0.187
30	8.2	0.301	0.264	0.190
50	9.5	0.289	0.259	0.194
80	13.6	0.262	0.242	0.207



**Figure 4.6.** (Left) simulated  $V_\pi$  for five DCMs with varying slot width from 50 nm to 200 nm and varying slab heights of zero, 30 nm, 50 nm, and 80 nm. (Right) The overall confinement factor  $\sigma$ , corresponding to each  $V_\pi$ .

As explained above, the effectiveness of the DCM can be influenced by several parameters. Other than geometrical parameters, the EO sensitivity of the polymer plays an important role in achieving efficient  $V_\pi L$ . Although recent publications indicate that the

poling efficiency decreases in narrow slot widths [69], successful poling has been demonstrated with a slot width of 80 nm and a  $r_{33}$  of 160 pm/V [70] , and a  $r_{33}$  of ~390 pm/V ( $n_3^3 r_{33} = 2300$  pm/V) has been achieved in an 190 nm slot-width SOH MZM [71]. Here, we attempt to perform comparisons between DCM and SOH MZM, based on the same slot-width and same  $r_{33}$ . Understanding that there is a fundamental tradeoff between 3dB modulation bandwidth and  $V_\pi$ , we gauge modulator performance based on a figure-of-merit (FOM) defined as:

$$\text{FOM} = \frac{\text{Bandwidth (3dB)}}{V_\pi} \text{ (GHz/V)}. \quad \text{(Equation 4.7)}$$

For fair comparison in this paper, the 3dB bandwidth of the modulator is evaluated with unterminated lump element model which gives  $f_{3\text{dB}}=1/(2\pi RC_T)$  with  $R=50\Omega$  and  $C_T$  being the modulator capacitance. Using parallel plate dielectric capacitor model,  $C_T$  equals  $\epsilon_r \epsilon_0 \frac{H_s L}{W_s}$  where  $H_s$  is the waveguide height. Combining these parameters, the FOM can be expressed as:

$$\text{FOM} = \frac{1}{2\pi RC_T V_\pi} = \frac{r_{33} n_0^3 \sigma}{2\pi R K H_s \lambda}. \quad \text{(Equation 4.8)}$$

Here the factor  $K$  is used to differentiate DCM's waveguide capacitance from that of MZM which has two slot waveguides, thus, we assume  $K=2$  for SOH MZM and  $K=1$  for DCM. **Table 4.2** lists computed comparisons between a DCM and a SOH MZM, both structures having slot width of 190 nm, slab height of 70 nm,  $L$  of 1.5 mm, JRD1 polymer slot filling material,  $n_0$  of 1.81 at 1550 nm wavelength, and  $r_{33}$  of 390 pm/V. It is noted in our study

that some DCM FOM improvements can be made by trading the waveguide height with the effective confinement factor  $\sigma$ . Both DCM and SOH MZM predict FOM greater than 100 GHz/V, comparing to a 10 GHz/V FOM measured from a premium commercial silicon MZM, there remains a tenfold potential DCM improvement which silicon photonics can capitalize on.

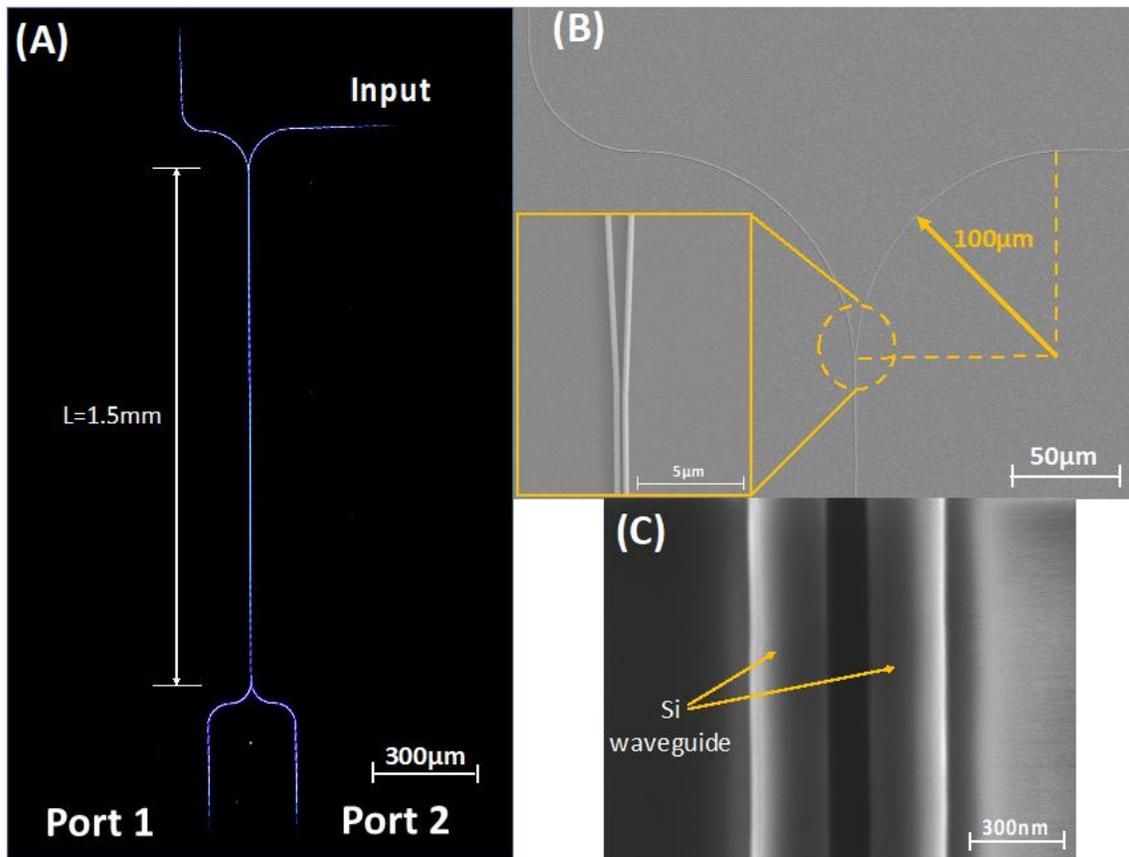
**Table 4.2.** Comparison list of DCM and SOH MZM of the same slot width and polymer filling

<b>Modulator type</b>	<b>DCM</b>	<b>SOH MZM</b>
<b>Waveguide height(nm)</b>	<b>500</b>	<b>220</b>
<b><math>K</math></b>	<b>1</b>	<b>2</b>
<b><math>\sigma</math></b>	<b>0.310</b>	<b>0.203</b>
<b><math>V_{\pi}</math> (V)</b>	<b>0.137</b>	<b>0.21</b>
<b>FOM (GHz/V)</b>	<b>202</b>	<b>150</b>

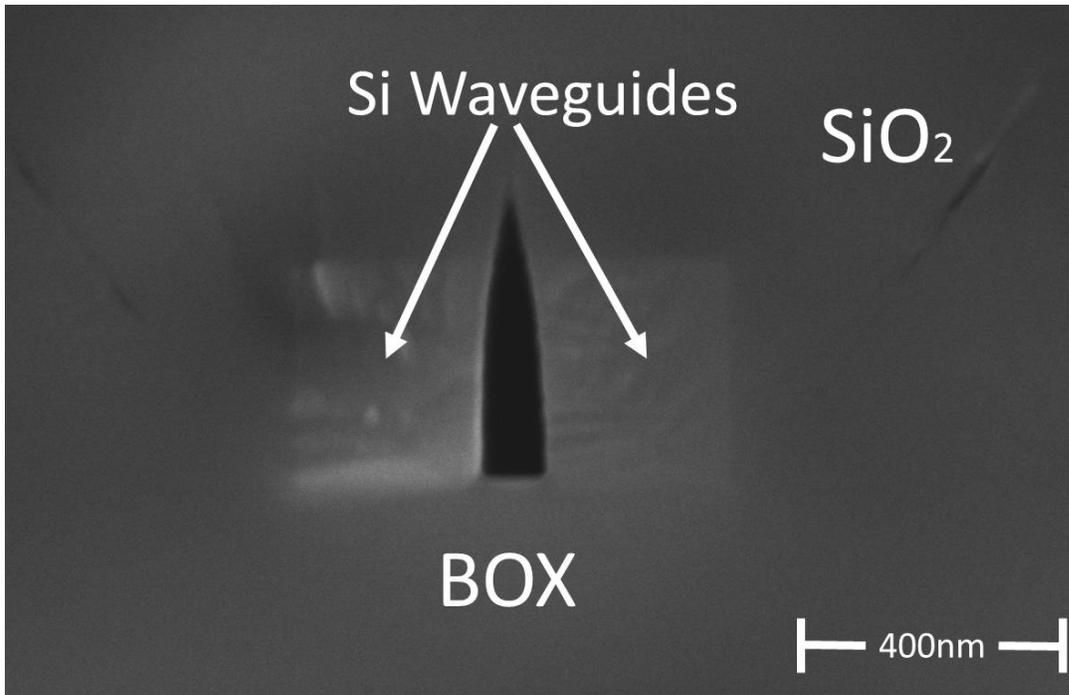
To further support the case for this DCM, it greatly simplifies the fabrication complexity compared to that of the SOI MZM which needs two multi-mode interferometer (MMI) splitters and four transformers at both input/output waveguides to divide/transform optical signal from silicon waveguide into slot-confined waveguides and vice versa. Careful balancing of optical loss and phase change between both arms is also required for the MZM to achieve good extinction ratio. Contrarily, the DCM only uses adiabatically cross-coupled bends at both input and output, and the output switching can be adjusted by bias voltage with relative low optical loss.

### 4.3 DCM device fabrication and preliminary measurement

Device proof of concept and ultimate demonstration is progressing in several stages. The first stage is passive optical characterization, presented in this chapter, and consists of fabricating a basic nano-slot DCM structure and characterizing its optical switching performance using optical wavelength scanning. The fabricated device is shown in **Figure 4.7(a)** and consists of three main sections, adiabatically cross-coupled S-bends (**Figure 4.7(b)**) at both input and output, a 1.5 mm long cross-coupled region (**Figure 4.7(c)**), and simple inverse-tapered mode size converters at both input and output. Fabrication begins with a 330 nm thick SOI wafer on 1  $\mu\text{m}$  buried oxide. The device is patterned by electron-beam lithography and followed by silicon dry etching to form the waveguides and the nano-slot. The cross-coupled waveguide width is  $\sim 280$  nm and the slot width is  $\sim 100$  nm. PECVD  $\text{SiO}_2$  is deposited on top of the whole structure, leaving an air slot (un-filled) between the two waveguides as shown in **Figure 4.8**.



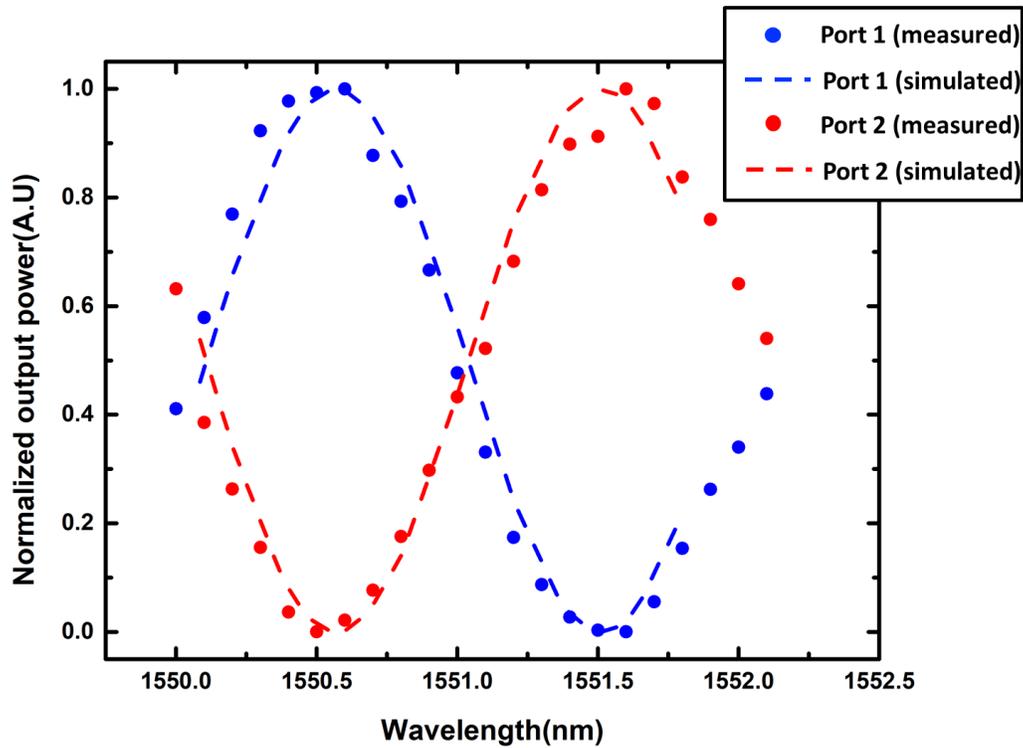
**Figure 4.7.** (A) Schematic of the DCM in dark field optical microscopy. (B) A top view SEM image of the input S-bends. (C) the top view SEM image of the two Si waveguides and the nano-slot.



**Figure 4.8.** A cross-sectional SEM image of an air-slot waveguides which are covered with 2.17  $\mu\text{m}$ -thick of  $\text{SiO}_2$ . The slot width is 80 nm.

The fabricated sample was tested at an optical bench to observe optical switching between two output ports by wavelength scanning from 1525 nm to 1575 nm. Light from a tunable external cavity laser was launched into the tapered input with polarization control at both input and output. The DCM was designed for TE mode operation, by scanning optical wavelength, optical switching between the two TE output ports can be clearly observed by a near infrared camera. The two TE outputs were measured separately by an optical power meter along with the scanned wavelength, displayed in **Figure 4.9**. The measured output power shows a peak-to-valley wavelength separation to be  $\sim 1$  nm. This measured wavelength separation is shorter than the derived value from **Equation 4.1** and **Equation 4.2**,  $2L_c^2(N_s - N_a)/L$ , due to the presence of the air slot. We have performed a Beam

Prop simulation to analyze the above fabricated sample and its wavelength dependency. Close match is obtained between the measured data and simulated data. This result gives us confidence that the DCM predicted performance in this paper can be achieved. Full DCM performance with polymer filled nano-slot will be reported at a later date.



**Figure 4.9.** Wavelength scan of the two output powers from the fabricated air-slot DCM. The blue dots are the normalized power from port 1 and the red dots from port 2. Dash lines represent corresponding simulation results.

#### 4.4 Summary

We investigate a nano-slot conductive waveguide directional coupler modulator (DCM) proposed by CK Sun et al. It projects a high modulator FOM ( $3\text{dB bandwidth}/V_{\pi}$ )

which is 35% better than the state-of-the-art SOH MZM and extremely low  $V_{\pi} = 0.14V$ . The projected switching efficiency of  $V_{\pi}L = 0.21 \text{ V}\cdot\text{mm}$  is also the best among all directional coupler modulators. To verify its operation, a 100 nm wide air-slot DCM is fabricated and tested. The device demonstrates strong wavelength dependency, the peak-to-valley wavelength separation is  $\sim 1 \text{ nm}$ , matching well with the simulation results.

## 4.5 Acknowledgment

Chapter 4 in full, is currently being prepared for submission for publication of the material. Pappert, Steve, Sun, CK, Chen, Dingbo, Yu, Paul K. L. The dissertation author was the primary investigator and author of this material. This chapter includes the nano-slot conductive waveguide directional coupler modulator(DCM). This work is done by Dr. Steve Pappert, Dr. CK Sun, Dr. Dingbo Chen, Kangwei Wang, and Prof. Paul Yu. I would like to acknowledge DARPA (W911NF-16-2-0152) and Office of Naval researcher (ONR) (contract N00014-18-I-2027) for partial support of this work. Also, I acknowledge Dr. CK Sun for the invention of the DCM concept according to Patent number: 9,500,929: "Vertical electro-optically coupled switch" (issued on November 22, 2016) and the patent: US 2018/0081253 A9). For the DCM fabrication, I acknowledge UCSD Nano3 electron beam lithography (EBL) specialist, Dr. Maribel Montero for the EBL writing and Dr. Xingyu Zhang (Acacia Communications Inc.) for all the fruitful discussion in DCM fabrication and EO polymer poling, Dr. CK sun, Dr. Steve Pappert, Dr. Dingbo Chen, and Prof. Paul Yu for giving me the guidance on the project goal.

# CHAPTER 5

## NANO-SLOT DIRECTIONAL COUPLER FABRICATION DEVELOPMENT

In Chapter 4, we introduce the DCM platform which can be an advanced modulator design which incorporates large  $r_{33}$  EO polymer, liquid crystal, or large EO coefficient inorganic materials, such as nano-pillars described in Chapter 3. In this chapter, I would summarize the fabrication development using university cleanroom facilities at the San Diego Nanotechnology Infrastructure (SDNI) facility located at the Qualcomm Institute (QI) at UCSD. I begin by introducing the key process steps (**Section 5.1**), followed by two different process flows which will be compared (**Section 5.2**). Then I explain the reason how we finalize our current process flow. During the fabrication process, we gradually optimize each step to make the DCM closer to a final prototype. Detail of the process optimization is presented in the **Section 5.3**. Last, in **Section 5.4**, the Beam Prop Method simulation results of the peak-to-valley separation for non-slab air-slot/polymer-slot is presented and the preliminary optical measurement of the 50 nm slab height DCM is summarized.

## 5.1 DCM process steps introduction

### 5.1.1 Diced wafer cleaning

At the SDNI facility, we dice 4 - 8 inches Silicon-on-Insulator (SOI) wafer into 1 cm<sup>2</sup> pieces to reduce the wafer cost. However, wafer dicing creates lots of Si particle debris. Therefore, the SOI wafer needs to be first coated with a thick layer of positive photoresist before dicing.

The DCM requires extremely low particles counts on the surface so as to avoid particle accumulation inside the slot later on. Traditional photoresist removal procedure doesn't meet the targeted particles counts.

We prepare 6 beakers includes: three beakers contain photoresist remover, one beaker contains D.I water, one beaker contains IPA, and one beaker contains acetone. The cleaning procedure is done by the following steps:

- (a) The first two beakers contain warm photoresist remover. Using the gravity to let the Si dust sink to the bottom of the beaker, the sample is immersed with the photoresist side down into the photoresist remover and move the sample gently in the horizontal direction. The photoresist remover dissolves the positive photoresist coating together with the Si debris which sink to the bottom of the beaker.
- (b) To minimize the Si debris from reaching back and stick on the sample surface, the sample is removed from the first resist remover solution and placed into second photoresist remover solution and the step (a) is repeated.
- (c) The sample is immersed into the third photoresist remover, DI wafer, IPA, and

acetone. Each solution has different solvent polarity [72]. The vertical sonication was performed by using a glass slide to fix the sample normal to the bottom of the beaker. Vertical sonication assists the release of any Si debris at the sample surface and prevents the Si sawdust from re-attaching the sample.

- (d) The last solution for vertical sonication is acetone. Due to the high evaporated property of acetone, the remaining acetone on the sample surface can be easily air-dried.

Step (a)-(d) are particularly designed for Si debris removal. From step (e), we use the standard wafer cleaning procedure to remove the metallic and organic contamination.

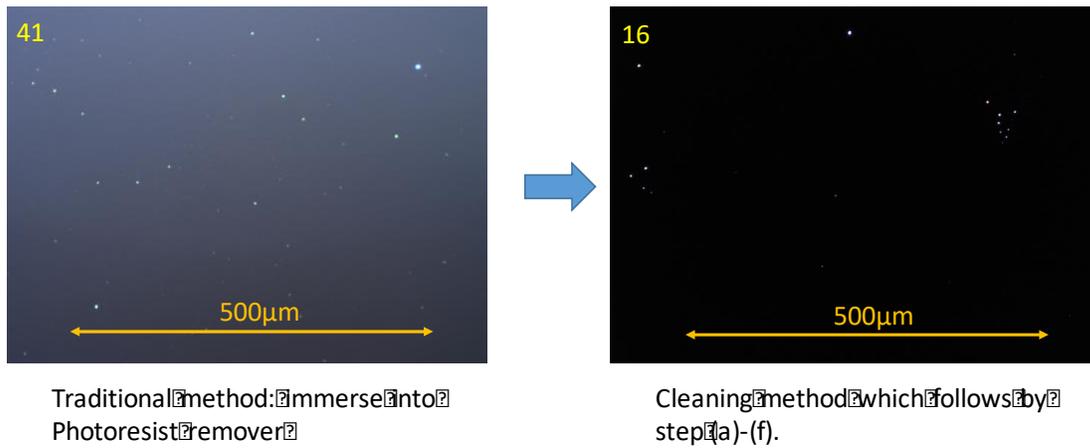
- (e) The sample is immersed in the Nanostrip solution (a commercial available reagent, which contains a fixed ratio of sulfuric acid (90%), Peroxymonosulfuric acid (5%), and Hydrogen peroxide (<1%) [73] it is a strong oxidant reagent which oxidizes organic contamination) which is heated to 70-80 °C to achieve high oxidizing strength, for a 15 min duration.

- (f) The sample is transferred to DI water for 30 s. in step (f), we mix prepare RCA1 and RCA2 solutions based on the chemical combination shown in **Table 5.1**. The cleaning sequence starts from the RCA1 and follows by each row in **Table 5.1**.

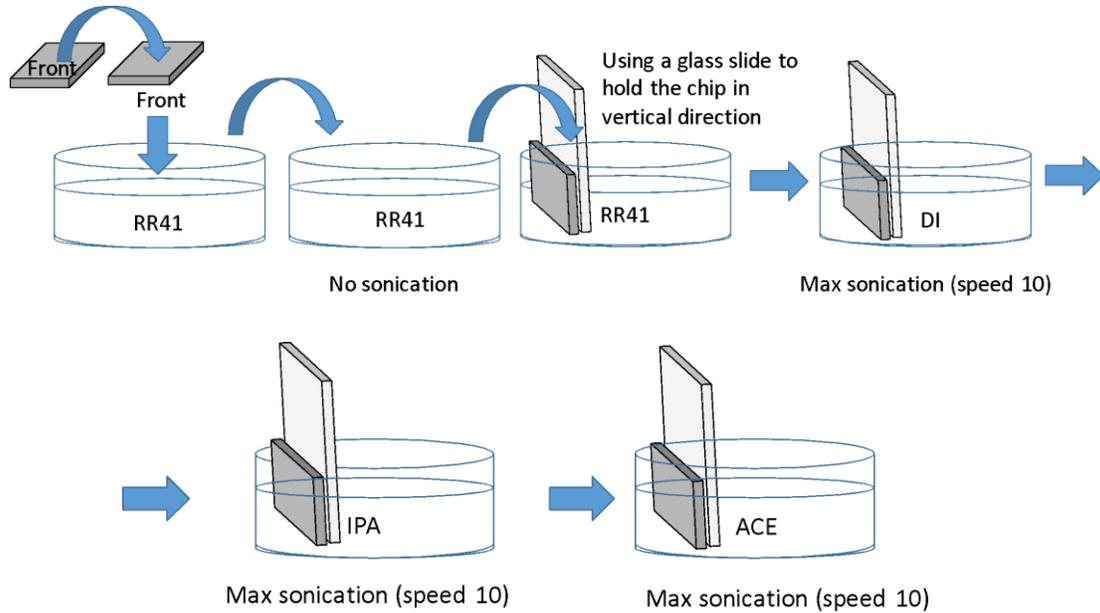
**Table 5.1.** Details of RCA 1 and RCA 2 wafer cleaning.

	Time	Purpose	Chemicals	Reaction
RCA 1 Solution 70 °C±5	10 min	Remove the organic contaminants	50ml H <sub>2</sub> O <sub>2</sub> 25ml NH <sub>4</sub> OH 250ml D.I water	H <sub>2</sub> O <sub>2</sub> + hydrocarbons → CO <sub>2</sub> +H <sub>2</sub> O.
10% HF	30 s	Remove SiO <sub>2</sub>	3.3ml HF 297ml D.I water	4HF+SiO <sub>2</sub> →SiF <sub>4</sub> +H <sub>2</sub> O
RCA 2 Solution 70 °C±5	10 min	Remove the metallic contaminants	63ml H <sub>2</sub> O <sub>2</sub> 31ml HCl 250ml D.I water	Metal + HCl → M <sup>+n</sup> +H <sub>2</sub>
10% HF	30 s	Remove SiO <sub>2</sub>	3.3ml HF 297ml D.I water	4HF+SiO <sub>2</sub> →SiF <sub>4</sub> +H <sub>2</sub> O

(g) The sample is inspected under an optical microscope under dark field with a 20X objective lens to do a particle count. Within a 500 μm<sup>2</sup> field of view, an acceptable particle count is less than 25. **(Figure 5.1)**



**Figure 5.1** The dark field optical microscopic images under a 20X objective lens.



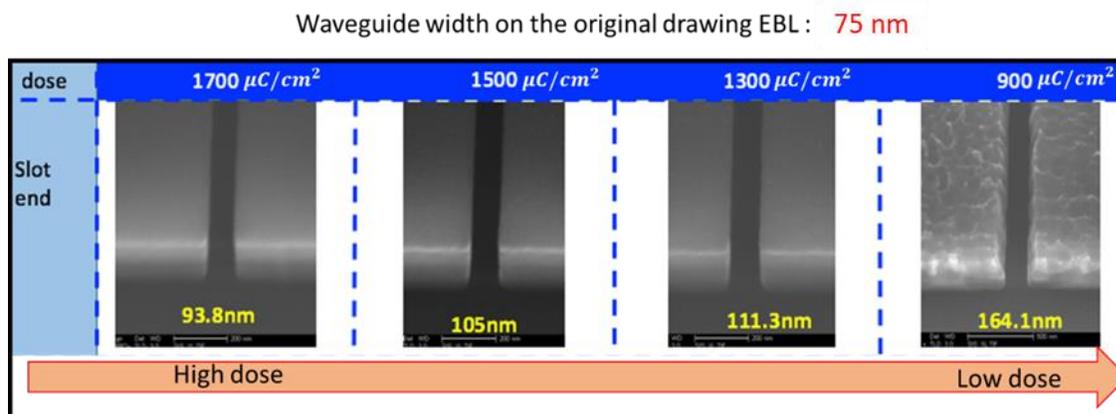
**Figure 5.2** A flow diagram of the cleaning steps for diced sample.

### 5.1.2 Electron beam lithography (EBL) for the formation of the DCM waveguides

All EBL writing is done by SDNI's EBL specialist, Dr. Maribel Montero. The EBL pattern writer is Vistec EBPG 5200, which offers a resolution of  $\sim 50$  nm. At the same applied voltage, we perform current dosage test to realize the best EBL writing parameter to form slot waveguides, S-bends, and inverted Si tapers. We select a negative EBL resist, XR-1541,6% (Dow Corning) to do the EBL patterning. Its selection is based upon: (a) The resist thickness is thin enough ( $\sim 113$  nm at 40s spinning time, and at a 3000 rpm spin-rate) to create a nano-slot which is 50-160 nm wide and 330 nm high, (b) it is a resist with Si-H-O bonding and therefore after the EBL writing, the resist will convert into  $\text{SiO}_2$ -like

material which can be used as a dry etch mask, (c) its refractive index ( $n=1.45$  at  $\lambda=1550$  nm) is appropriate as the Si slot waveguides cladding material.

**Figure 5.3** shows an example of the slot width versus electron current dosage. We can observe the E-beam resist surface quality and the Si sidewall quality after the dry etching. All samples are written on the sample wafer, and the Si dry etch is performed at the same time. The original slot width from the EBL drawing is 75 nm. As the dosage reduces, the slot width is widened. The dosage can go even higher since we have not seen the cross-linking of the e-beam resist. Notice that as the dosage increases, more electrons back reflect from the substrate into the e-beam resist at the nano-slot. This means the e-beam resist at the slot also converts into a  $\text{SiO}_2$ -like material and acts as a Si dry etch mask. Consequently, the un-etched Si remains in the slot. At a  $900 \mu\text{C}/\text{cm}^2$ , the XR1541 film has not been fully converted into  $\text{SiO}_2$ -like material. The original XR1541 film is not a strong dry etch mask, the SEM shows the Si surface is damaged at low dose, and the slot wide wall quality is poor.



**Figure 5.3.** the dose test result of an EBL pattern with a 75 nm separation.

### 5.1.3 Silicon dry etch

To pattern the full structure including Silicon slot waveguides, S-bends, and input/output inverted Si tapers, a precise control of the Si dry etch rate is essential. At the slot waveguides section, under-etching will result in a thin layer of Si remaining in the slot, which will lead to a current leakage during the poling process. On the other hand, an over-etching of the top Si will result in an undercut at the Buried oxide (BOX). At the Si taper tip, the tip width is 50-100 nm, severe undercut will result in the collapse of the Si taper. We utilize Oxford instruments, P-100 dry etcher [2] to perform the Si dry etch. The reactant gaseous affluent include 25 sccm of SF<sub>6</sub> and 50 sccm of C<sub>4</sub>F<sub>8</sub>. This combination yields a 5 to 1 ratio of etching selectivity between crystal Si and the native oxide. The etcher is set at a pressure of 15 mTorr; reactive ion etching (RIE) power of 30 W; inductively coupled plasma (ICP) of 1200 W, and the gas affluent above. The calibrated Si etch rate is 3.6 nm/s, and that for the native oxide is 0.5-0.6 nm/s. The native oxide thickness (~1-2 nm) is reported from M. Morita *et al*'s work [74]. The film thicknesses are measured by Filmetrics with a fitting accuracy better than 97% [75].

### 5.1.4 Electro-optic (EO) polymer: Poling station, device design, and EO polymer

We divide the Electro-optic (EO) polymer handling in three stages:

- (1) EO polymer thin film poling;
- (2) Silicon slot EO polymer filling and poling test;
- (3) Nano-slot conductive waveguide-DCM EO polymer poling.

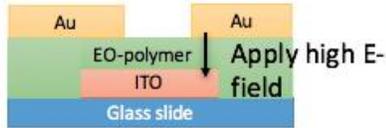
To successfully pole the Nano-slot-conductive waveguides-directional coupler modulator (NSC-DCM), we must suppress the leakage current under the poling E-field in the range of 150-200 V/um. The leakage current originates from the polymer itself and the nano-slot waveguides sidewall roughness. We design two device structures to investigate each leakage pathway. In **Figure 5.4 (Left)**, the electro-optic (EO) polymer thin film is designed for testing the leakage current originates from the EO polymer material itself. First, a high E-field (150-200 V/um) in the vertical direction is applied to the EO polymer. Second, we gradually bring up the temperature of the polymer to its glass transition temperature ( $T_g$ ). Leakage current is monitored and recorded during this process. Second, we design a nano-slot structure for the poling test. In **Figure 5.4 (Right)**, the SEM images show the nano-slot structure at the end of the device and also the sidewall roughness at the middle of the nano-slot. Compared to NC-DCM, the poling-test structure does not have the dual waveguides so as to reduce the fabrication complexity.

1. EO polymer thin film:

a. Test device :

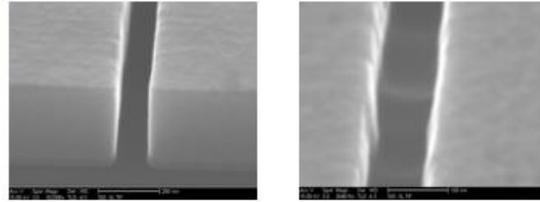


b. Cross section :

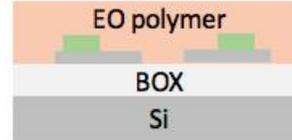


2. Nano-slot structure:

a. SEM of the Nano-slot:



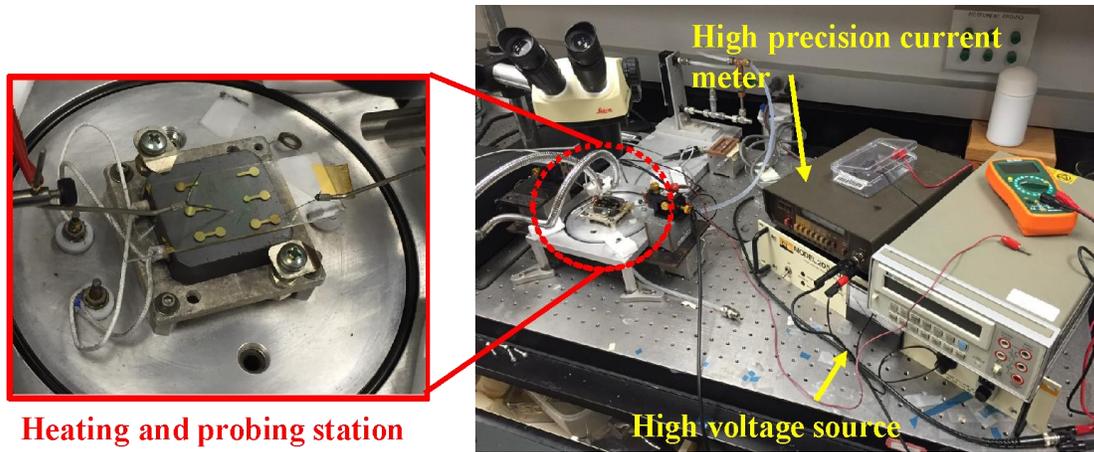
b. Cross section of the final device will be:



**Figure 5.4-**(1a) the top view and (1b) the illustrated picture of cross-sectional view of the EO polymer thin film. (2a) the SEM images of the nano-slot device. The left image is at the device end; the right is at the middle of the nano-slot; (2b) the schematic cross-sectional view of the nano-slot poling test device.

We assemble the EO polymer poling station (**Figure 5.5**). The poling system includes:

- (a) High voltage source: capable of delivering up to 3,000 V.
- (b) Current meter: capable of measuring down to nA scale.
- (c) Heating station: device is placed on a temperature controllable graphite holder.

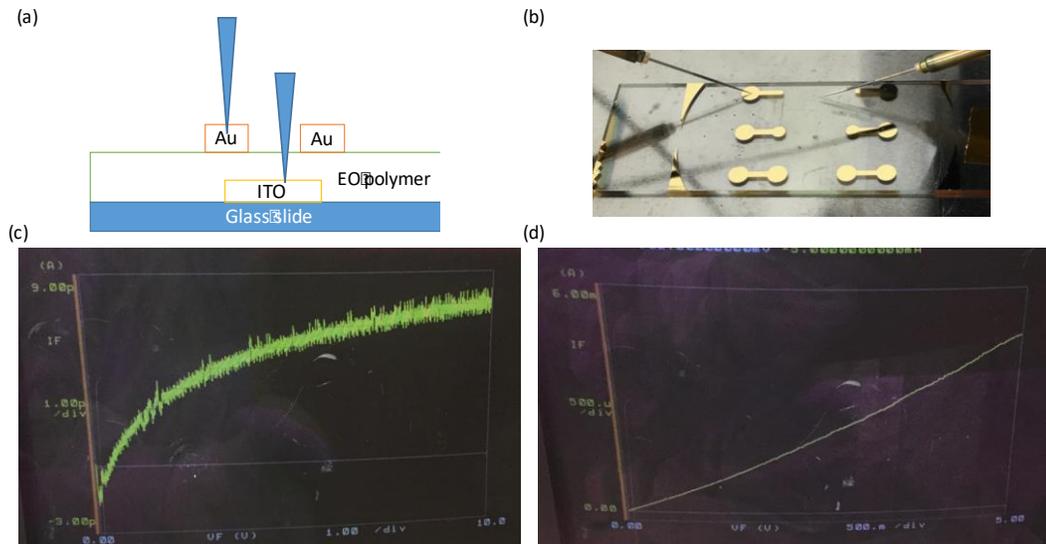


**Figure 5.5.** The EO polymer poling station setup

#### ***5.1.4-1 EO polymer thin film device fabrication***

The device configuration is shown in **Figure 5.6(a)**. A 50 nm thick of ITO is sputtered by Denton Discovery 18 on a glass slide followed by annealing on a 150 °C hot plate for 2 min to increase the conductivity of the ITO layer. The 6.1 w.t. % polymer solution is spin-coated on a ITO/glass slide at a 1200 rpm spin rate for 120 s to receive a 2 μm thick polymer film. The EO polymer thin film then is baked at 130 °C for 1 hour in a nitrogen ambient oven to remove the solvent, Dibromomethane (DBM). Finally, 150 nm thick gold and 5 nm thick Ti are deposited on top of the EO polymer thin film via sputtering using a shadow meshed mask. **Figure 5.6 (b)** showed the final thin film device. It should be noted that e-beam evaporation is not recommended for the top metal deposition. Compared with sputtering, e-beam evaporation is operated at a relatively high temperature and results in a stronger metal bombardment to the electro-optic polymer. The metal using e-beam evaporation will penetrate the EO polymer and generate a leakage pathway. **Figure**

**5.6(c-d)** indicate the leakage current level comparison with same thickness of top contact metal stacks but using different metal deposition facility. For sputtered metal, when the device is biased at +10V, the leakage current is  $< 9$  pA. In contrast, for e-beam evaporated metal, when the device is biased at +5 V, the leakage current is  $\sim 4.5$  mA.



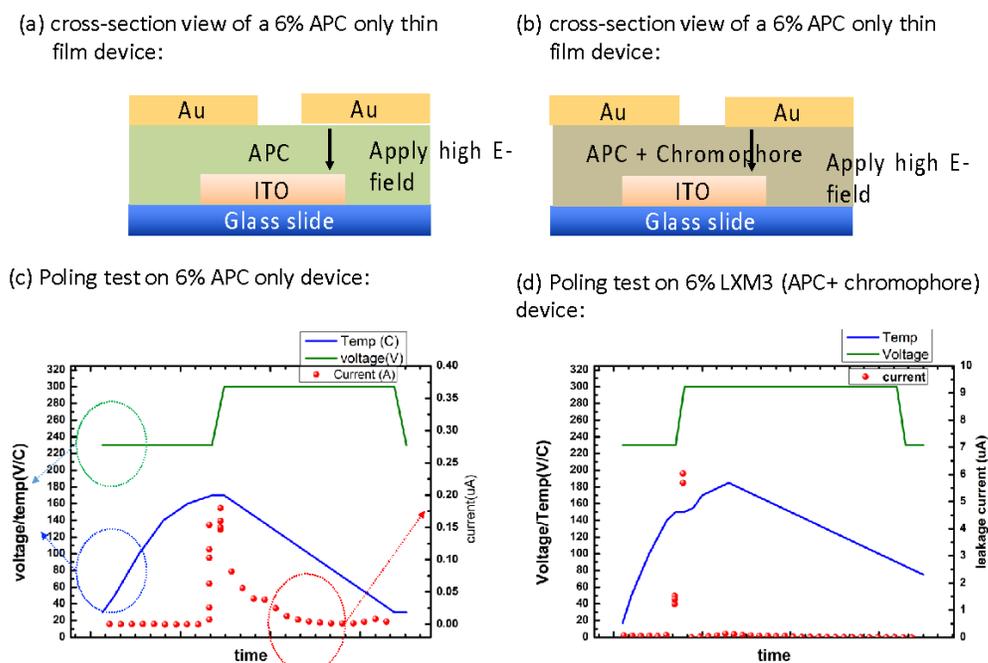
**Figure 5.6:** (a) the cross-sectional view of the thin film device (b) the photograph of the fabricated thin film device. (c) the leakage current test result with sputtered metal stacks. (d) the leakage current test on the same structure, but with e-beam evaporator to deposit the same thicknesses of Ti and Au;

### 5.1.4-2 EO polymer thin film device poling

The EO polymer thin film is poled by our home-built poling system (**Figure 5.5**). Our preliminary poling test is performed in an air ambient. In the future, the poling system will be housed in a nitrogen gloves box to avoid moisture induced current leakage. The high voltage source is capable to deliver up to 3,000 V, and the leakage current is monitored

by a nanoampere current meter. The EO polymer thin film is placed on a graphite heating that is resistively heated.

Polymer solution is prepared by mixing chromophores and amorphous polycarbonate (APC) in a 1:1 ratio with dibromomethane (DBM). We prepare two poling thin films: 1. APC only. APC acts as the host material to effect chromophore-to-chromophore separation. 2. Chromophore mixed with APC in a 1:1 ratio. These two thin films provide important information of how chromophore affects the leak current. The results (see **Figure 5.7(c-d)**) from both devices show abruptly leakage current increased when the temperature reach  $T_g$ . And once we turn off the heater to cool down the device, the leakage current drops. The results are in the same leakage current level as the published paper [5]. More importantly, the chromophore mixed with the APC device performs 30 times higher leakage current than the APC only device. This implies the chromophore and APC mixture generates more leakage paths at  $T_g$ .



**Figure 5.7** (a-b) the cross-section of the 6 wt.% amorphous poly-carbonate (APC) only and the 6 wt.% chromophore mixed with APC, respectively. (c). the poling result of a 6 wt.% APC only device. (d) the poling result of a 6 wt.% chromophore mixed with APC.

### 5.1.4-3 EO polymer in the nano-slot structure

The nano-slot poling test device structure is shown in **Figure 5.8** and has a 120 nm slot width. The fabrication process details for this poling test structure is as follows. The fabrication procedure starts with a SOI wafer with the top 330 nm thick Si device lightly p-type doped. The 120 nm wide Si slot and the 3  $\mu\text{m}$  wide Si pad is patterned by E-beam lithography (EBL) followed by Si dry etching (RIE and ICP), as described earlier in this chapter. **Figure 5.8 (Left)** show the SEM images of the top view and 90<sup>0</sup> cross-sectional view of the nano-slot poling device. The ion-implantation with Phosphorous ions is applied at an energy of 92 keV and dose of  $1.05 \times 10^{15} \text{ cm}^{-2}$  to yield a phosphorous concentration of  $1 \times 10^{20} \text{ cm}^{-2}$  in the Si pad. Rapid thermal annealing (RTA) at 1000 <sup>0</sup>C for 20 s in a nitrogen

ambient is used to activate the implanted dopants. This followed by 3 min of Oxygen descum and a 40 s Buffer-oxide-etchant (BOE) immersion to fully removed the remaining XR1541. Next, 50 nm thick gold electrodes with 5 nm thick chromium adhesion layers are sputtering in the contact region patterned by conventional photolithography, followed by a lift-off. **Figure 5.8 (Right)** shows the top view and 45<sup>0</sup> tilted view SEM images of the fabricated device. The tilted view confirms the gold electrodes are connected to the Si pads. In parallel, we fabricate another sample using an identical process flow to test the polymer filling. **Figure 5.8 (middle)** shows the cross-sectional SEM image of the EO polymer fills into a 120 nm wide nano-slot. No void is observed in the slot. The poling system setup has been described in **Figure 5.5** and the setup is tested with the EO polymer thin film device. According to the literature [76], the slot poling device needs to sustain an applied E-field of 100-200 V/ $\mu\text{m}$  with low leakage current (less than 10 nA/m<sup>2</sup>) at the glass transition temperature of the polymer, T<sub>g</sub>, which is 160-170 °C. First, the device is tested in an E-field of 150 V/ $\mu\text{m}$  and the leakage current is peaked 7.6nA at 175 °C. **Figure 5.9 (Left)** show the poling E-field, temperature, and leakage current profile. Lastly, the device is tested under the E-field of 200 V/ $\mu\text{m}$ . The highest leakage current is 10.8 nA at 190 °C. No breakdown occurs during both poling tests. After the device cool down to room temperature, we confirm that the device remains intact.

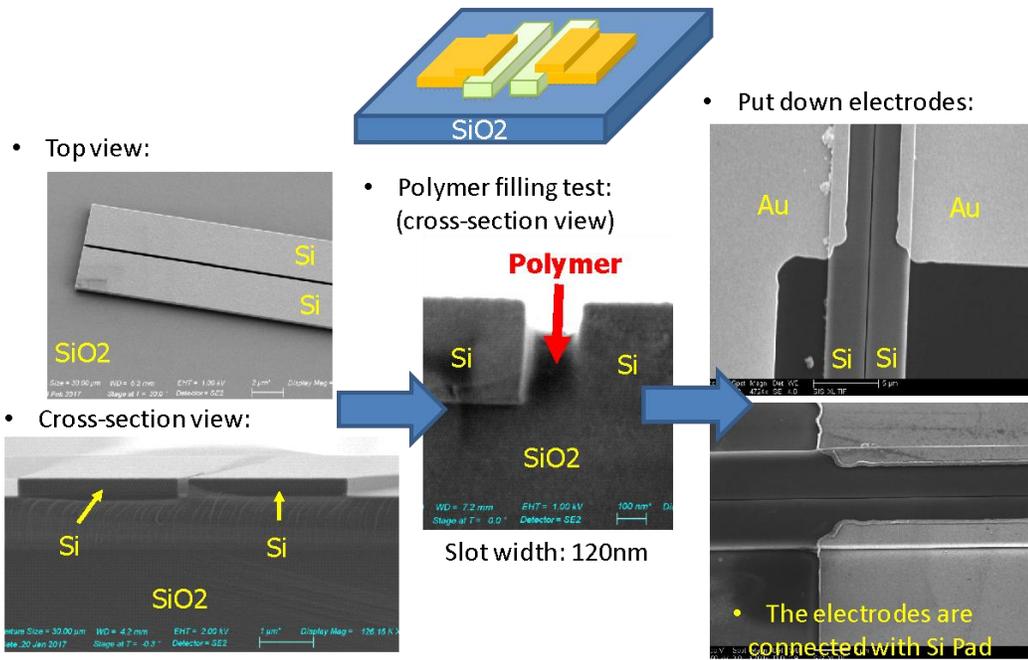


Figure 5.8. Polymer filled Si nano-slot poling test structure with 120 nm slot width.

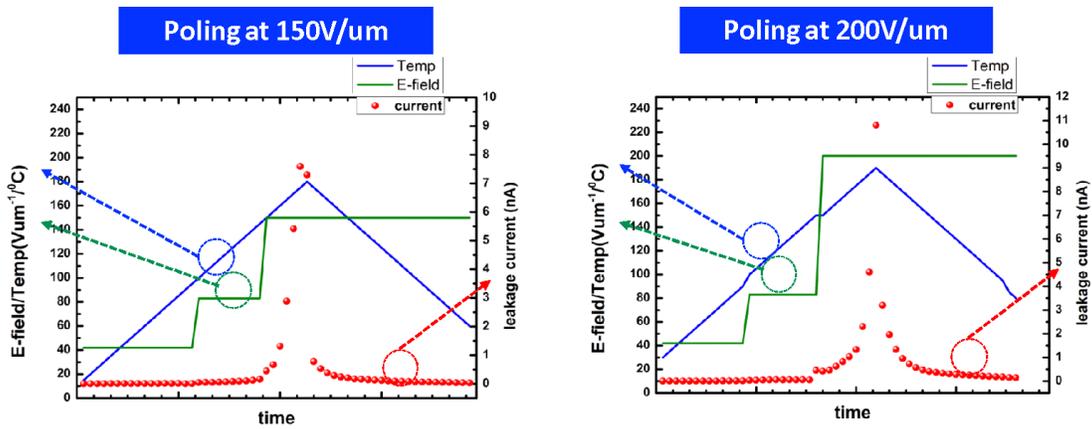
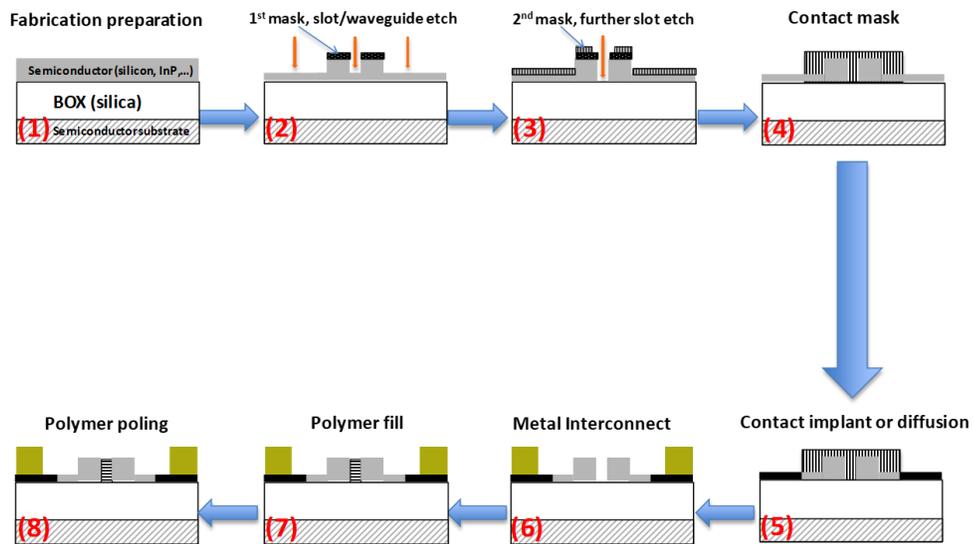


Figure 5.9. Poling measurements of polymer filled Si nano-slot test structure.

## 5.2. DCM fabrication process flow comparison

At the very beginning of the DCM fabrication design, we only construct the process flow of the slot waveguides active region. The process includes 8 steps as shown in **Figure 5.10**. However, we need an additional edge coupler to couple light from the tunable laser into the DCM waveguides. To simplify the fabrication process, a horizontal strip of SiO<sub>2</sub> cladding layer on top of a 200 μm long inverted Si taper is depicted as the initial mode-size converter (MSC). To merge the active region and the mode-size converter region into a new process flow, we design two different process flows: 1. Slot first, MSC last process. 2. Slot last, MSC first process. The comparison of the two process flows is listed in **Table 5.2**. We prefer the latter process flow because it ensures that the slot remains uncontaminated before the EO polymer spin coating.

### • Strongly Coupled DCM Device Fabrication



**Figure 5.10:** first version on the DCM process flow without having the MSC.

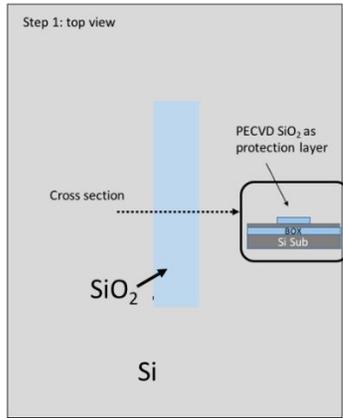
**Table 5.2.** The comparison of the pros and cons between “Slot first, MSC last” and “Slot last, MSC first” process flows.

Process flow	Pros	Cons
Slot first, MSC last	<ol style="list-style-type: none"> <li>1. Less prorogation loss through the joint waveguide.</li> <li>2. Lower risk in the fab process</li> </ol>	<ol style="list-style-type: none"> <li>1. Contaminated slot.</li> <li>2. Need precise control of thick SiO<sub>2</sub> removal in the slot</li> </ol>
Slot last, MSC first	<ol style="list-style-type: none"> <li>1. Uncontaminated Si slot for polymer filling</li> </ol>	<ol style="list-style-type: none"> <li>1. High process complexity. Need more time on process development.</li> <li>2. Optical loss at the joint section.</li> </ol>

The “Slot last, MSC first” process flow includes 9 steps (**Figure 5-11**): 1. SiO<sub>2</sub> protection layer formation. 2. Si taper formation. 3. SiO<sub>2</sub> protection layer removal. 4. Mode size converter formation. 5. Si nano-slot formation. 6. Si slab formation and slot etched-through. 7. Dual ion-implantation. 8. Metal contact formation and EO polymer filling. 9. EO polymer poling and device modulation measurement.

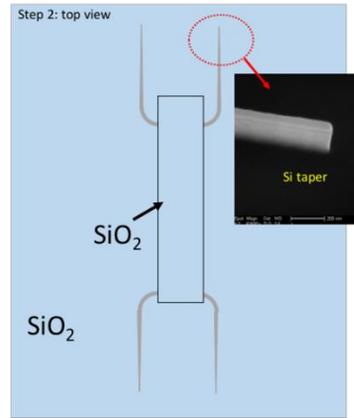
**1. Put a SiO<sub>2</sub> protection layer on a SOI wafer:**

- Process: PECVD  
SiO<sub>2</sub> → Photo litho → SiO<sub>2</sub>  
dry etch



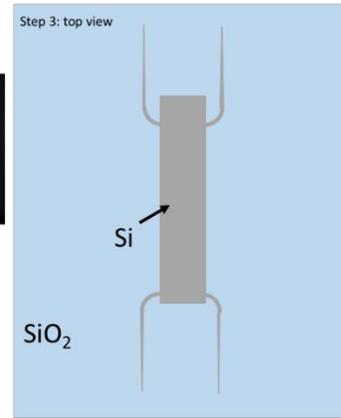
**2. Si taper formation:**

- Process: Si taper EBL  
→ Si dry etch



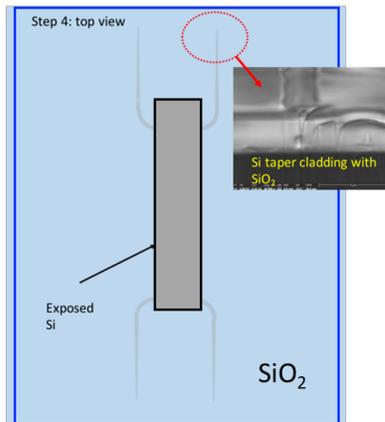
**3. SiO<sub>2</sub> protection layer removal**

- Process: BOE wet etch



**4. Mode size converter formation:**

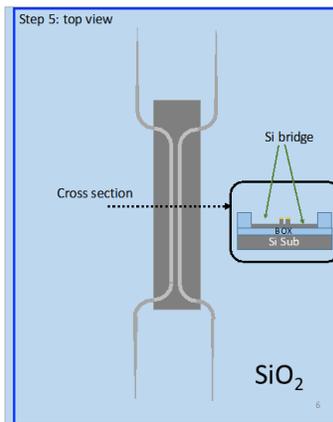
- Process: 2.2 μm thick PECVD SiO<sub>2</sub> → Photo litho → SiO<sub>2</sub> dry etch



**5. Si Slot formation:**

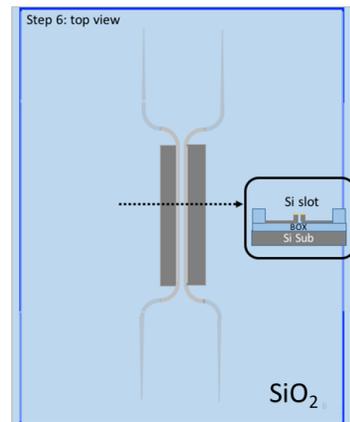
- Process: Si slot EBL → Si dry etch

Note: define slot and form Si bridges



**6. Si Slot etch through:**

- Process: Si WG & bridges EBL → Si dry etch → 1<sup>st</sup> ion-implantation (1E18cm<sup>-3</sup>)



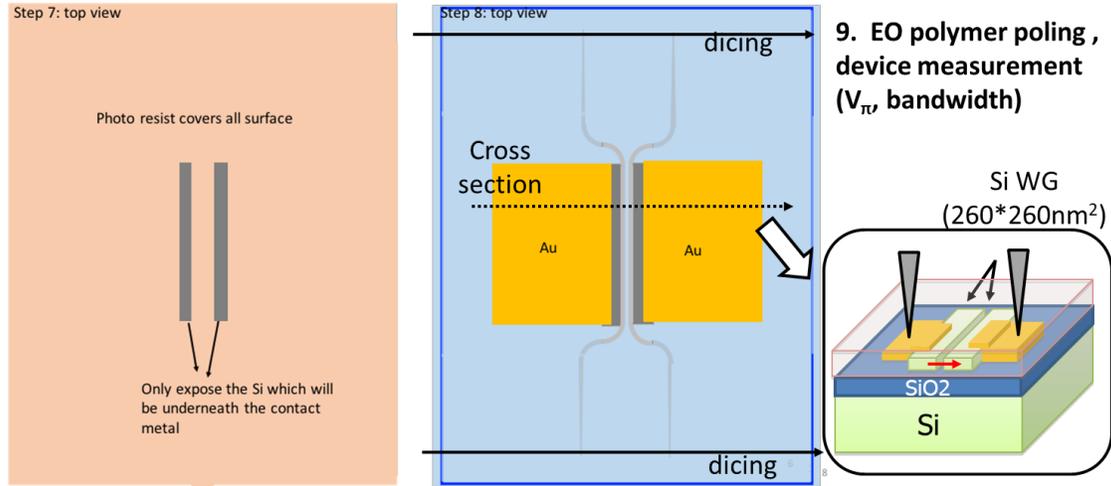
**Figure 5.11.** Process flow of “Slot last, MSC first”

**7. 2<sup>nd</sup> ion-implantation for Ohmic contact**

- Process: Photo litho → ion-implantation ( $>1E20cm^{-3}$ )

**8. Contact metal formation & EO polymer filling**

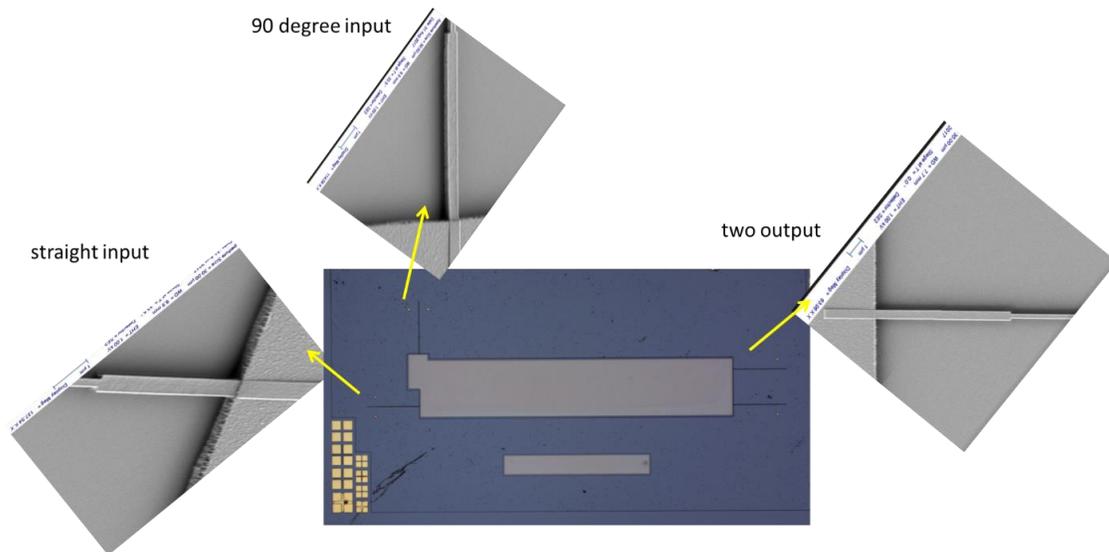
- Process: photo litho → E-beam evaporated Cr/ Au → lift off → annealing → EO polymer spin coating → baking → sample dicing → FIB polish.



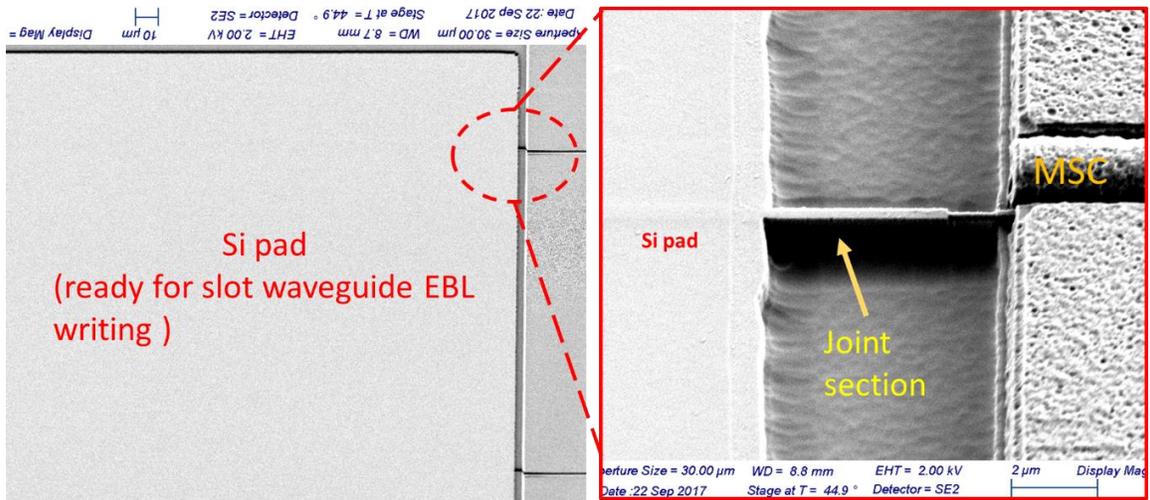
**Figure 5.11.** Process flow of “Slot last, MSC first” (continued)

A key design consideration for the “Slot last, MSC first” process flow is the use of a SiO<sub>2</sub> protection layer to cover the slot waveguides region. After forming the MSC, we open the active region using SiO<sub>2</sub> dry etch followed by EBL writing to form the nano slot waveguide. To make the whole Si waveguide connected from end-to-end (from input MSC to slot waveguides to the output MSC), we design a joint section to connect the MCS and the slot waveguides (**Figure 5.12**). The joint section is 80 nm wider than the actual Silicon waveguide width (260 nm) and therefore eases the EBL alignment for the slot waveguides EBL writing. Step 5 (**Figure 5.11**) in the “Slot last, MSC first” process flow is the critical step. After forming the MSC, we protect the MSC region and open the active region for the slot waveguide EBL writing. (**Figure 5.13**). The EBL writing followed by an Si dry etch is alright for most of the slot waveguides region which includes the 1500 μm long slot

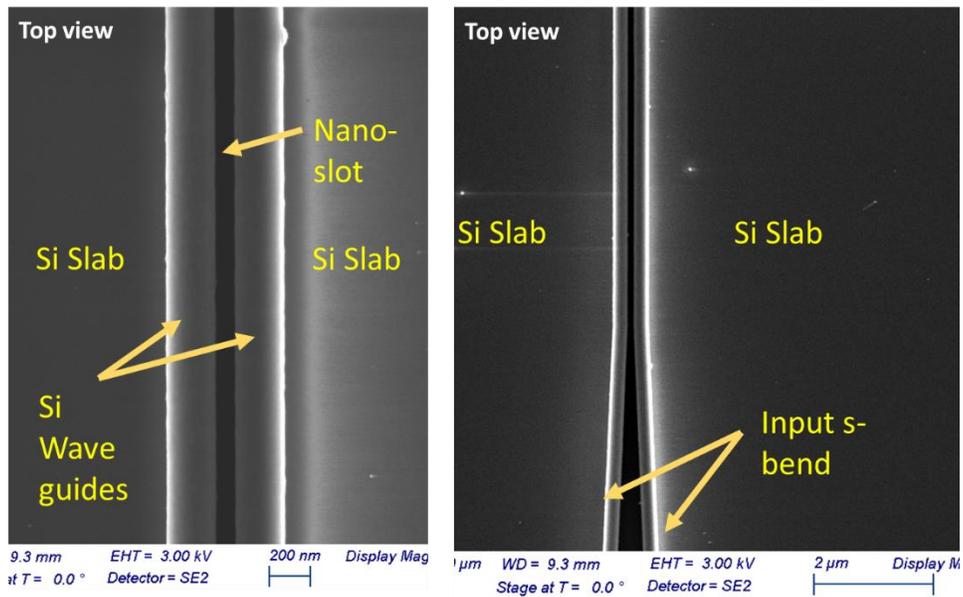
waveguides and input/output S-bends (**Figure 5.14**), but obviously there is no E-beam resist covered on the joint region and at the end of the Si pad (**Figure 5.15**). It is because the height of the joint waveguide is 330 nm, but the thickness of the E-beam resist (XR1541, 6 wt.%) is only 113 nm. After the wafer is coated with E-beam resist, there is no E-beam resist remain on the joint waveguide and the Si pad edge. No matter how accurate the EBL alignment is, the “Slot last, MSC first” approach is not a workable flow at this moment for making a DCM due to a disconnected Si waveguide at the joint waveguide section.



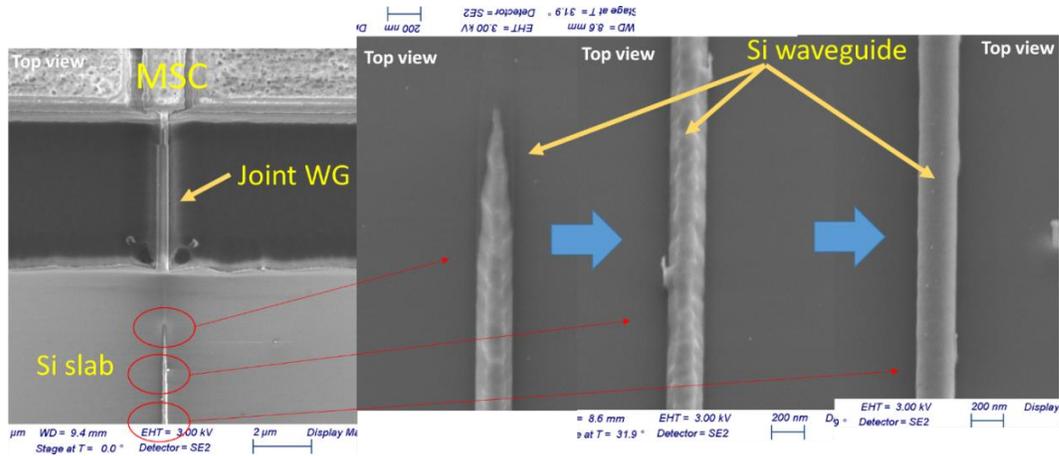
**Figure 5.12:** The step 3: SiO<sub>2</sub> protection removal of the “Slot last, MSC first” process flow.



**Figure 5.13:** The step 5 of the “Slot last, MSC first” process flow.



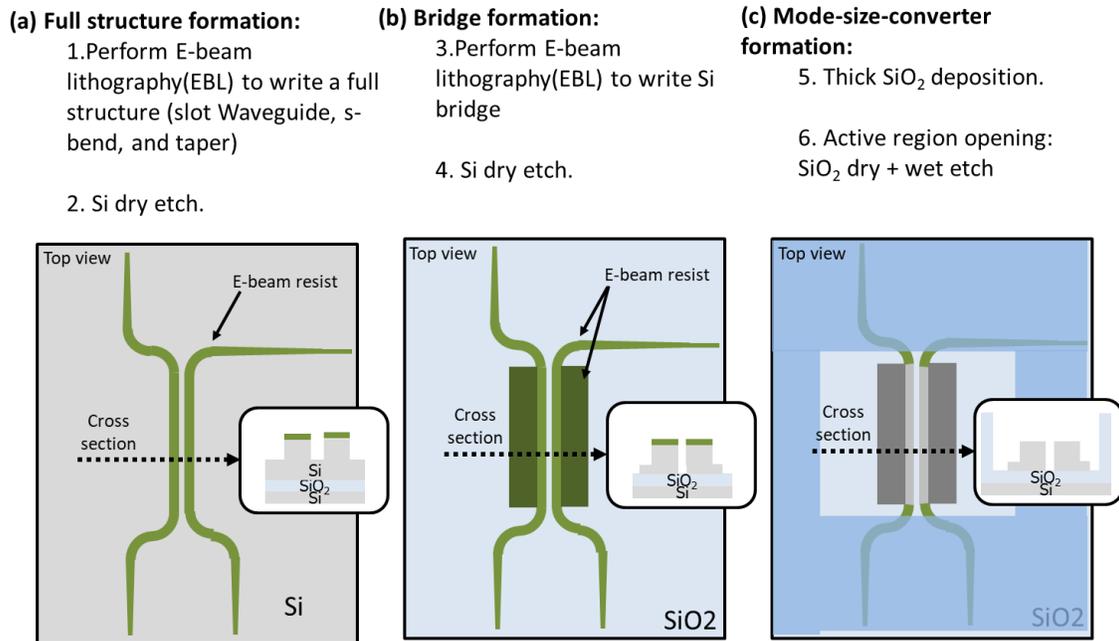
**Figure 5.14.** Top view SEM images at the middle of the slot waveguides and the input S-bend region in step 5: slot formation.



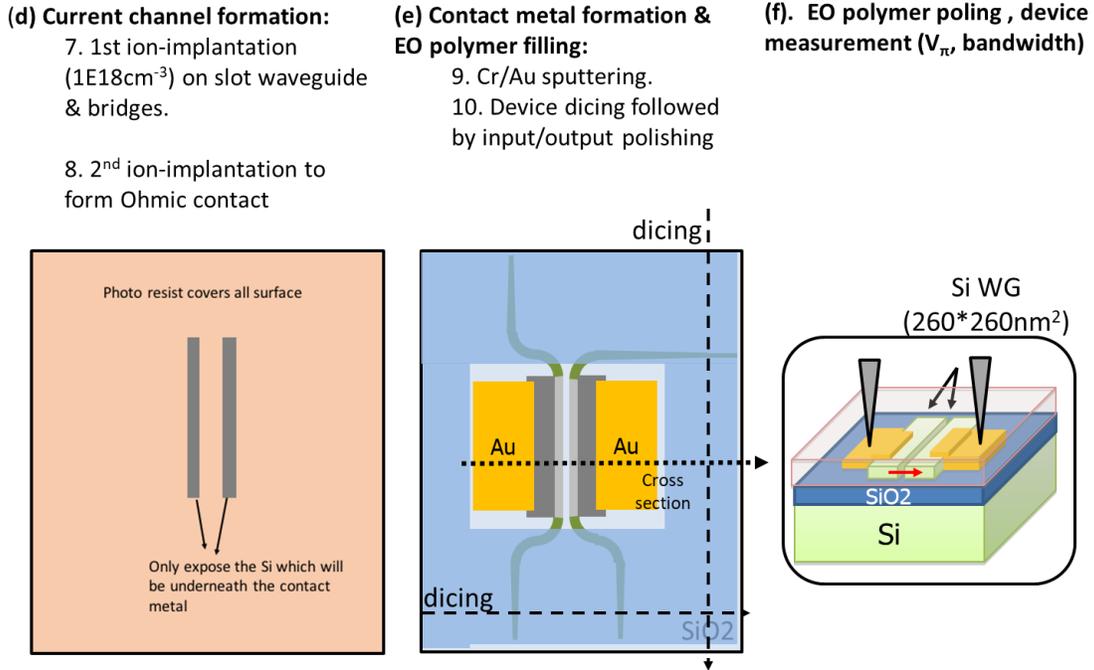
**Figure 5.15.** The top view SEM images of the edge of the middle Si pad and the joint waveguide region.

The process flow for the DCM using the “Slot first, MSC last” approach is depicted in **Figure 5.16**. The process starts with an EBL writing on 1cm<sup>2</sup> extremely low particle count SOI wafer (the wafer cleaning procedure is the same as that in section 5.5.1), followed by a Si dry etch. The Si dry etch determines the height of the Si slabs (Step (a)). The 2<sup>nd</sup> EBL step patterns the Si slabs region followed by a short Si dry etch to form the slabs. At this same step, the nano-slot is fully etched through (Step (b)). A 2.17 μm thick SiO<sub>2</sub> is deposited on the whole wafer to form the MSC. Next, we pattern the MSC region with a 300 nm of Cr by photolithography, metal deposition, and lift off. The Cr layer acts as the SiO<sub>2</sub> dry etch mask to protect the MSC. This is followed by opening the slot waveguide active region by SiO<sub>2</sub> dry etch (Step (c)). Once the slot waveguides region is fully exposed after ~1-hour SiO<sub>2</sub> dry etch, the wafer will be sent out for its 1<sup>st</sup> ion implantation to bring up the whole DCM doping level to 5×10<sup>17</sup> cm<sup>-3</sup>, n-type. A 2<sup>nd</sup> ion implantation is performed on the opened area of the two Si slabs (Step (d)). It further

increases the doping level at the Ohmic n-contact regions to  $>1 \times 10^{20} \text{ cm}^{-3}$ . After the photoresist removal, a  $1000 \text{ }^\circ\text{C}$ , 10 s of rapid thermal annealing (RTA) activates the dopant and recover the Si crystallinity. Metal contacts consist 300 nm of Au and 10 nm of Cr are formed by the photolithography, Au and Cr sputtering, and lift-off. The device is then coated with a  $2 \text{ }\mu\text{m}$  thick EO polymer and baked it in a nitrogen ambient for 1 hour at  $130 \text{ }^\circ\text{C}$  (same procedure as described in **Section 5.1.4-1**). Next, the wafer is diced at its input and output MSC end. The device underwent the poling process described in **Section 5.1.4-2**. The last step before modulation measurement is the input/output facets polishing. The polishing is done by focused-ion-beam (FIB). It produces to mirror-like facets at both input and output.



**Figure 5.16.** The “slot first, MSC last” process flow



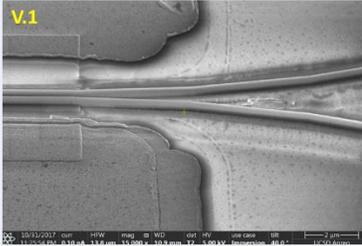
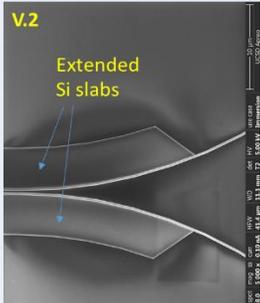
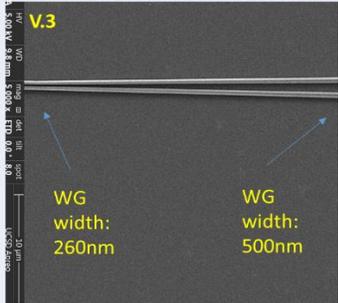
**Figure 5.16.** The “slot first, MSC last” process flow (continued)

### 5.3 The “Slot first, Mode-size converter last” process flow optimization

#### 5.3.1 Input S-bend optimization

Dual input/output S-bend is perhaps one of the most important regions in a DCM. It determines the extinction ratio of the modulation transfer curve. In our process development, we design three versions of the input/output S-bend to meet the goals of (1) high extinction ratio, and (2) low propagation loss and bending loss. It should be noted that the design of input S-bend not only deals with the dual waveguides, but also the Si slabs attached to the dual waveguides. **Figure 5.17** summarizes the three versions of the S-bend of the DCM. Version 1 has a bending radius of  $50\ \mu\text{m}$ , has no Si slab extended out from

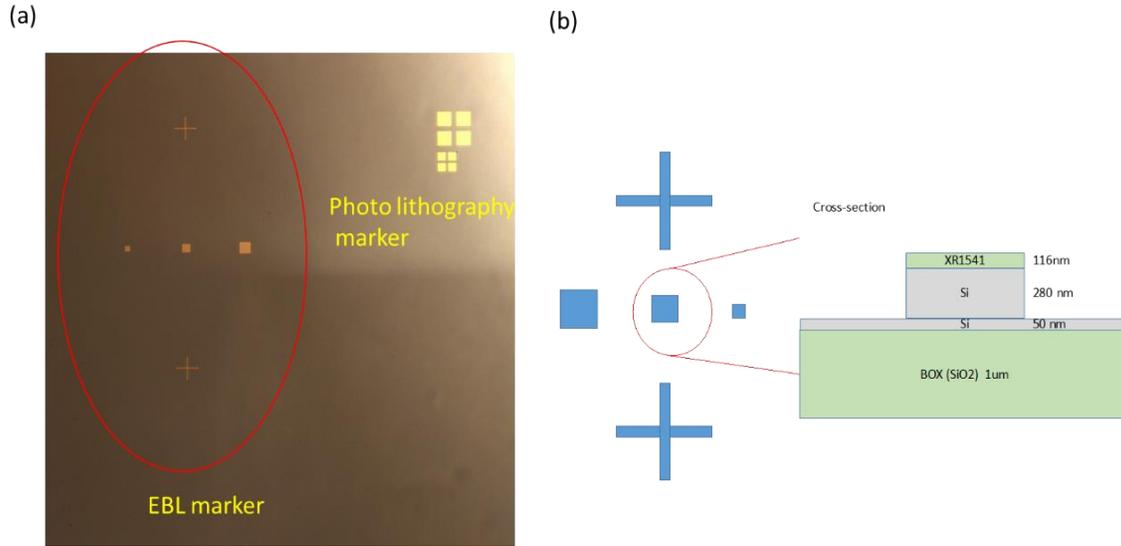
the slot waveguides, and no taper Si waveguide design (the S-bend waveguide width is 260 nm from end to end). In version 2, the Si slabs extends out from the active region to avoid the optical scattering by the slabs as light enters the active slot waveguides. Also, within a 20  $\mu\text{m}$  from the slot waveguides region, the bending radius is 100  $\mu\text{m}$ . This design ensures the incident light starts first cross-coupling before entering the active region (based on Beam Prop simulation). The rest of S-bend remains to be 50  $\mu\text{m}$  in bending radius to lower the propagation loss. The (last) version 3 is the tapered S-bend design. The end-point of the S-bend, which attaches to the MSC, has a waveguide width of 500 nm. In the S-bend region, the waveguide width gradually reduces from 500 nm to 260 nm then continues into the slot waveguides active region. This design reduces the propagation loss between the MSC to the S-bend.

Version	1	2	3
S-bend radius( $\mu\text{m}$ )	50	100 $\mu\text{m}$ (within 20 $\mu\text{m}$ to the active region). 50 $\mu\text{m}$ for the rest of s-bend	100 $\mu\text{m}$
Si slab extension	No	Yes (extend 20 $\mu\text{m}$ out from active region)	Yes (extend 20 $\mu\text{m}$ out from active region)
Taper design	No (same waveguide width)	No	Yes (260nm-500nm waveguide width)
			

**Figure 5.17** Three versions of the dual input/output S-bend of the DCM.

### 5.3.2 Particle counts reduction and reduction of process steps

During the process development, we suffer from high particle count on the wafer. In **Section 5.1.1**, we present the wafer cleaning procedure to minimize the Si debris, but this does not guarantee the wafer can remain low in particle count all the way till the last stage or at least till the nano-slot formation stage. Therefore, we re-examine the process flow to eliminate the number of steps so as to reduce the chance of particle contamination. First, an additional benefit of applying the “Slot first, MSC last” process is the whole structure includes: slot waveguides, taper S-bend, and the inverted Si taper is formed in single step of the process. However, before the first EBL writing (**Figure 5-16, step (a)**), we must create alignment markers for the following EBL and photolithography. In the first version the alignment marker is made of metals (150 nm thick of Au on top of 5 nm thick of Cr) (**Figure 5-18(a)**). It requires additional EBL, metal deposition by e-beam evaporator, and lift-off to generate those high contrast, inert metallic marker. Unfortunately, this step creates extra particles and leads to a low yield in the subsequent slot waveguides EBL writing. We run an experiment to test the marker recognition on the EBL writer and merge the metallic formation step (step 0) into the 1<sup>st</sup> EBL writing step (**Figure 5-16(a)**), which means, instead of forming high contrast metallic marker, we rely on the marker consisted of a 113 nm tall of SiO<sub>2</sub> on a 280 nm thick Si (**Figure 5-18(b)**). the new marker still gives enough contrast recognizable by the EBL writer.



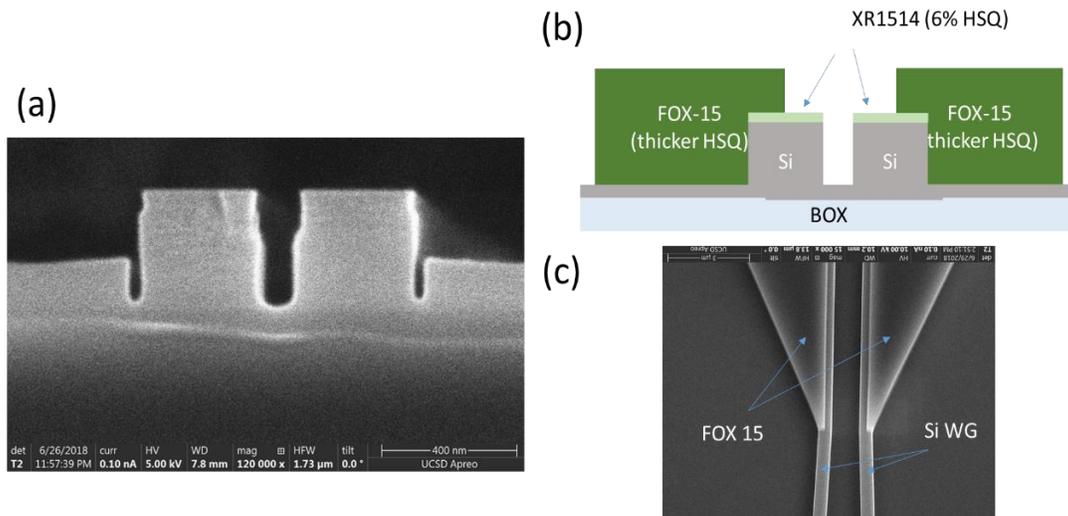
**Figure 5.18.** (a) The metallic EBL and photolithography alignment marks (b) the SiO<sub>2</sub>-like/Si markers.

### 5.3.3 EBL for Si slabs formation optimization (Step (b))

In the original “Slot first, MSC last” process flow (**Figure 5.16**), the 1<sup>st</sup> EBL: slot formation and 2<sup>nd</sup> EBL: slab formation and slot etch through both use the XR-1541, 6% (a diluted solution of HSQ) as the e-beam resist and the dry etch mask after the e-beam writing. A thin layer of XR1541 (113-116 nm in height) enables the 1<sup>st</sup> EBL followed by a Si dry etch to achieve 50-200 nm wide nano-slot. Its slot width to resist height (aspect ratio) is ~1:2). In our experiment, it is not recommended to apply XR-1541, 6% as the e-beam resist for the 2<sup>nd</sup> EBL. The thin XR-1541 would not fully cover the sidewall of Si waveguides and since the Si dry etch is not isotropic. The exposed Si sidewall will suffer from lateral Si dry etch the subsequent vertical etch through the Si slab (**Figure 5.19. (a)**). This creates a “short” circuit in the DCM. We replace the XR-1541 with a thicker e-beam resist: FOX-15 (**Figure 5.19(b)**). At a 4000-5000 rpm spin rate, the FOX-15 offers a film

thickness of 550-600 nm, which fully covers the entire sidewall of the Si waveguides.

**Figure 5.19(c)** depicts the top view SEM of the DCM input taper S-bend. The FOX-15 also converts into a SiO<sub>2</sub>-like layer and forms the pattern of the Si slab as well as covers half of the Si waveguide.



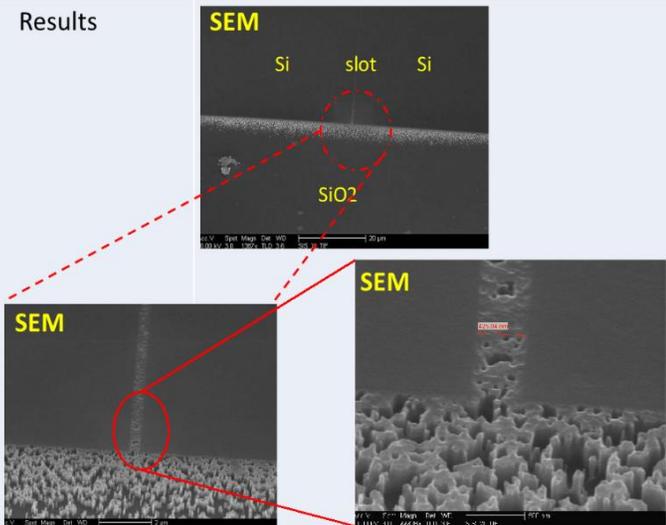
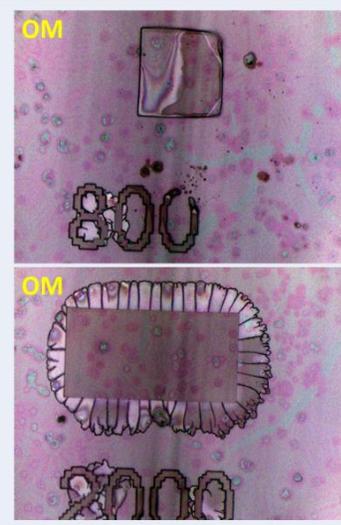
**Figure 5.19.** (a) The cross-sectional SEM image of the DCM which suffers from over-etching of the Si slabs. (b) The cross-sectional picture to illustrate the use of the FOX-15 to protect the slabs and the Si waveguides sidewall. (c) The top view SEM image of the input taper S-bend.

### 5.3.4 2<sup>nd</sup> ion implantation blocking mask optimization (Step (d))

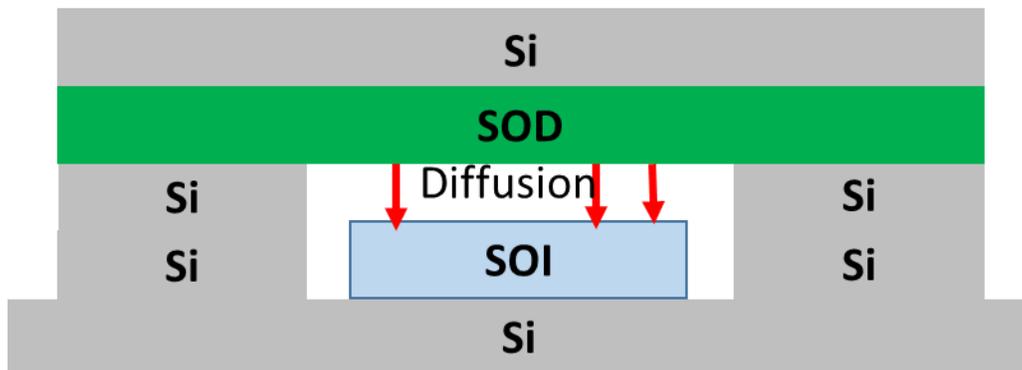
In **Figure 5.16 (Step (d))**, we apply ion-implantation blocking mask to selectively increase the dopant concentration of the slab region to  $\sim 1 \times 10^{20} \text{ cm}^{-3}$ , n-type. This region will form an Ohmic contact with Au/Cr in Step (e). For higher bandwidth DMC, we would like to put the two metallic contacts as close as possible to reduce the series resistance,  $R_s$ .

In other words, the opening of the ion implantation blocking mask would also prefer to be as close as possible. On the other hand, the two electrodes cannot be too close to the slot waveguides. Otherwise, the metallic absorption will increase the propagation loss (which occurs in the plasmonic organic hybrid (POH) modulator). In our first design, the blocking mask opening is only 1  $\mu\text{m}$  away from the slot waveguides and leads to the total separation between two mask openings to be 2.62  $\mu\text{m}$  (1  $\mu\text{m}$  + 260 nm of Si waveguide width + 100 nm of slot width + 260 nm of Si waveguide width + 1  $\mu\text{m}$ ). We decided to use EBL to have an accurate control to form the ion-implantation blocking mask. In **Figure 5.20**, the top view SEM images (middle column) show the extremely high electron scattering during the EBL writing on the SOI wafer which had been ion-implanted before. The scattering converts the E-beam resist, HSQ inside the nano-slot into  $\text{SiO}_2$ -like material which becomes a micro dry etch mask. Notice that the SOI wafer had gone through 1000  $^\circ\text{C}$ , 20 s RTA annealing to activate the dopants and repair the Si crystal damages. Another approach to enhance the top Si doping concentration is to use the spin-on-dopant (SOD) (**Figure 5.20, right**). The SOD solution first spin-coated on a Si wafer then placed on top of the SOI wafer. The separation between the SOI and the SOD coated wafer is 500  $\mu\text{m}$  (**Figure 5.21**). Placing the two wafers topside on topside in close proximity in the furnace then heating up to 650  $^\circ\text{C}$  for 5 min, the sheet resistivity,  $R_{\text{sq}}$  is measured at 64.5  $\Omega/\text{sq}$ . Even though the SOD method causes less damage to the top Si layer on SOI wafer, unfortunately, we still observe high EBL e-scattering. This concludes that the EBL writing is very sensitive to the Si surface quality. At SDNI facility, we rely on e-beam lithography (EBL) to provide the sub-nanometer nano-patterning instead of using deep UV lithography. This

can limit the 3dB bandwidth of the DCM since we can now only utilize conventional photolithography (UV light wavelength: 365 nm) and the resolution would be  $> 2 \mu\text{m}$ .

Method to enhance top Si doping level	Ion implantation	Spin-on-dopant (SOD)
Sheet resistivity, $R_{sq}$ ( $\Omega/\text{sq}$ )	17.1 (corresponding to $>1 \times 10^{20} \text{cm}^{-3}$ )	64.5
Results		

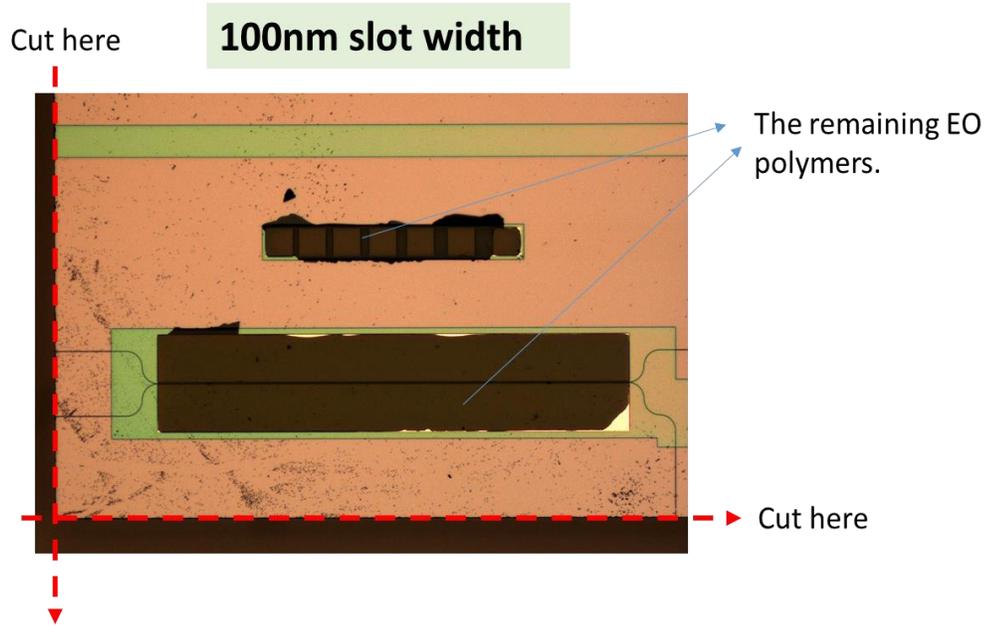
**Figure 5.20.** Comparison of the EBL results between using ion-implantation and spin-on-dopant (SOD) to enhance the wafer doping level.



**Figure 5.21.** A schematic cross-sectional view to illustrate the dopant diffusion from the SOD layer into the top Si layer of SOI during annealing.

### 5.3.5 EO polymer adhesion (step 8)

The EO polymer, LXM3, is prepared inside the fume hood at a 6.1 wt.% with dibromomethane (DBM). The mixture is then filtered with the 2  $\mu\text{m}$  porous diameter disk plate filter before coating on the DCM. At 2000 rpm spin rate and 2 min spin time, a 2  $\mu\text{m}$  thick of the LXM3 film results. The wafer is then soft-baked in a nitrogen ambient oven set at 130  $^{\circ}\text{C}$  for 1 hour to get rid of air bubbles inside the thin film. However, we find that the EO polymer has poor adhesion to  $\text{SiO}_2$  (The surface of Mode-size converter and the surrounding are both  $\text{SiO}_2$ ). Unfortunately, the DCM does not allow applying adhesion promoter before the EO polymer coating since it will affect the EO polymer poling and the final  $r_{33}$ . **Figure 5.22** shows the optical microscope image after the dicing at the input and output of the DCM. It indicates that the EO polymer has better sticking coefficient with the Au electrode but has poor adhesion with the  $\text{SiO}_2$ . This makes it uncertain about whether the EO polymer has filled in the nano-slot or it just floats on top of the nano-slot. Therefore, the DCM needs to be diced before the EO polymer spin-coating and re-design the separation between the DCMs to have sufficient area for wafer handling after the wafer dicing.



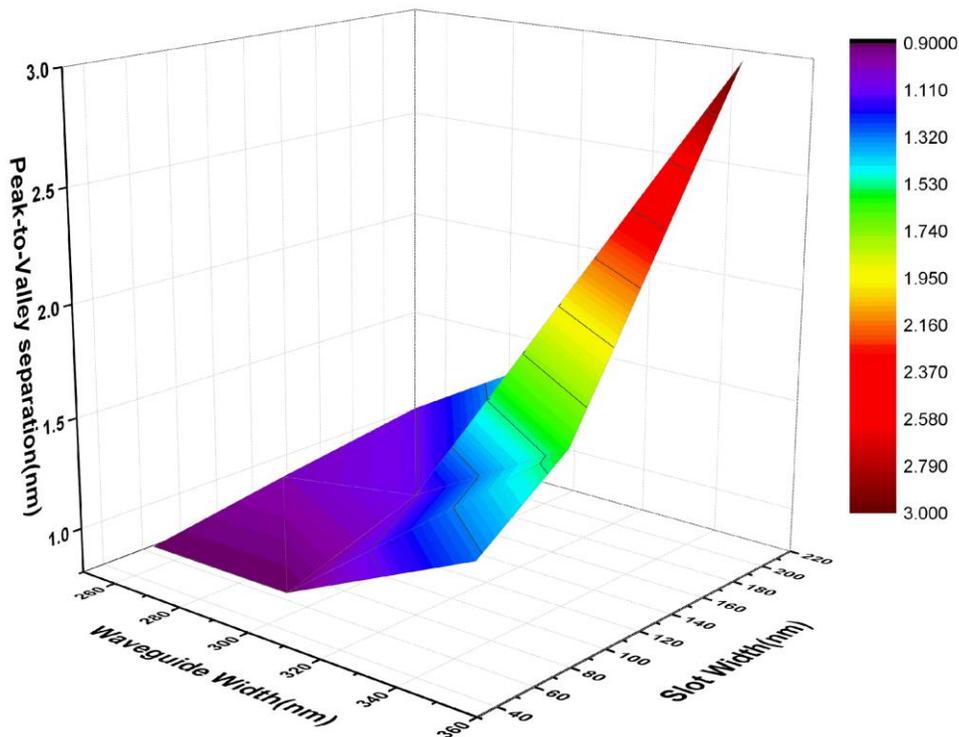
**Figure 5.22.** The optical microscopic image of the full DCM device spin-coated with a layer of EO polymer then cut the input/output facet with a blade.

## 5.4 Optical measurement

All passive optical measurements are using the setup shown in **Figure 4.13**. To tackle the final DCM modulation, we split the development in three stages:

**Stage 1.** Demonstrate passive wavelength dependence characteristic in an air-slot as described in chapter 4-section 4.2c. In this stage, we start to fabricate a simplified DCM without the Si slabs. We then apply the dual EBL and dual Si dry etch to generate the Si slab DCM structure. **Figure 5.23** shows the BPM simulation result of wavelength dependence characteristics for the air-slot, no-slab DCM. The nano-slot width ranges from 75 nm - 200 nm and the waveguide width ranges from 260 nm - 350 nm. For high

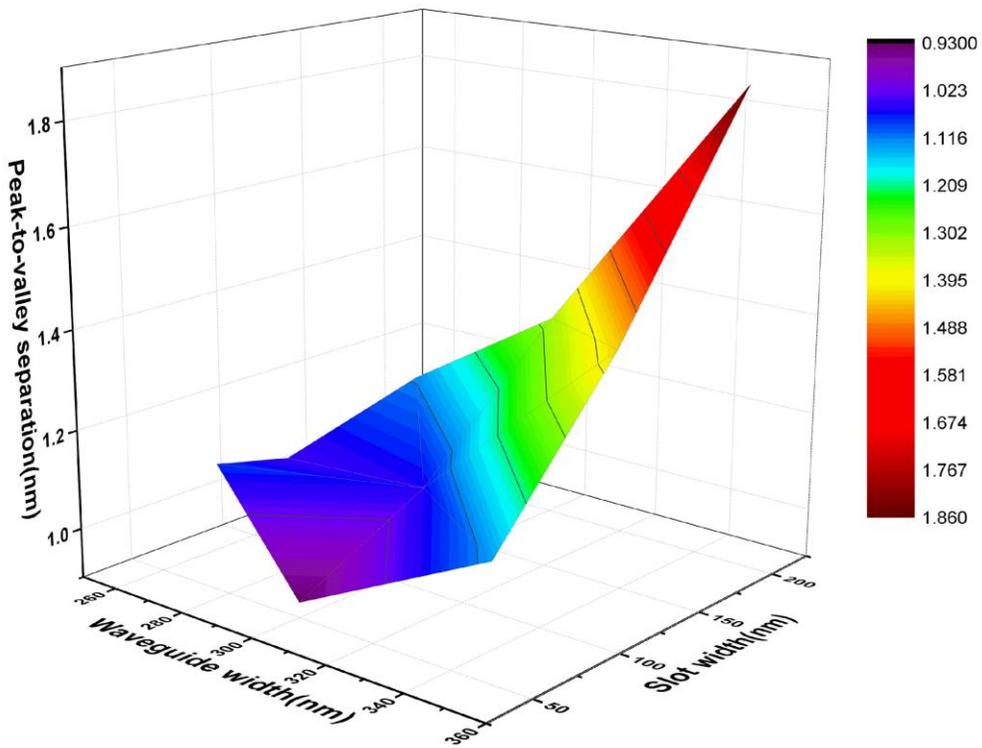
modulation efficiency DCM structure that has a narrow slot and narrow waveguide, the peak-to-valley separation is simulated to be  $<1$  nm (purple area). At this area, the peak-to-valley separation in wavelength cannot provide the actual physical parameter of the fabricated DCM, but once you take the top view SEM image of the DCM, the simulation can give you an idea of the peak-to-valley separation.



**Figure 5.23.** The BPM simulation result of the simplified air-slot, non-slab DCM.

**Stage 2.** Demonstrate passive wavelength dependence characteristics in a DCM which has EO polymer fills in the nano-slot. To achieve this stage, the fabrication process ends at Step (c) (**Figure 5.16**) which opens the slot waveguide region. The wavelength dependence characteristics, that is, the peak-to-valley separation will change due to the change of both

the refractive index of the material inside the slot and cladding. **Figure 5.24** indicates the peak-to-valley separation of a no-slab DCM and the EO polymer fills in the nano-slot and the cladding ( $n=1.69$ ). The slot width and the waveguide width ranges are same as those shown in **Figure 5.23**. The simulation indicates that the change of the peak-to-valley separation is not as large as the air-slot no-slab DCM. It is because the air-slot is a strong coupled DCM (larger difference between its fundamental mode and higher order mode), but the polymer filled slot DCM is a weakly coupled DCM. It should be kept in mind that the wavelength dependence relies on the Silicon refractive index difference at different incident wavelengths. Therefore, the change of the  $N_s$  and  $N_a$  is in the same level where the slot index modulation mostly change the  $N_s$ . To sum up, the wavelength dependence measurement is not ideal for the DCM which had been filled with EO polymer due to the small peak-to-valley separation.

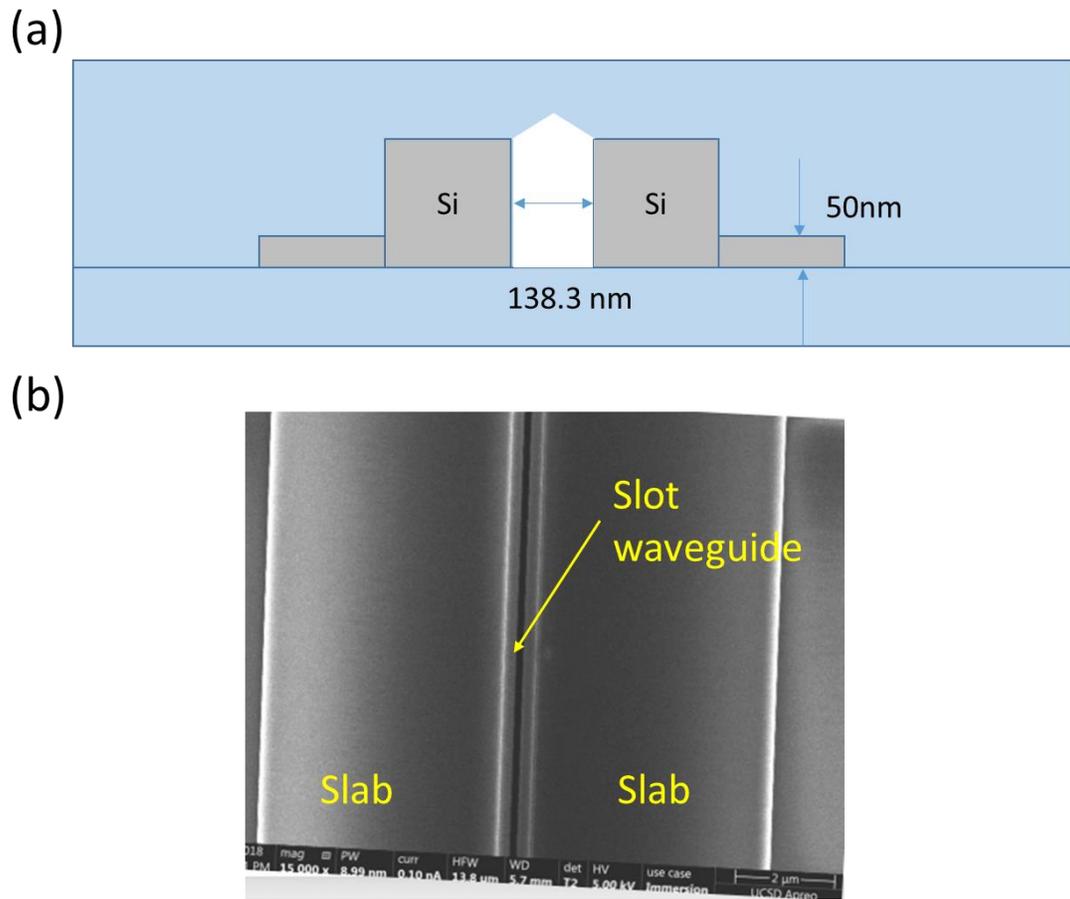


**Figure 5.24.** The BPM simulation result of the polymer-slot, no-slab DCM. (polymer refractive index: 1.69)

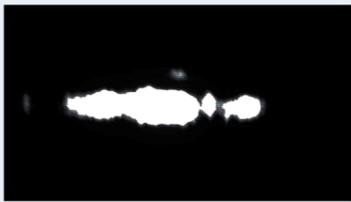
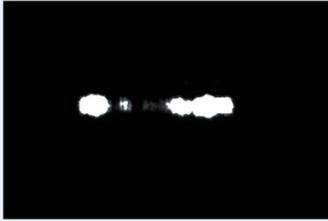
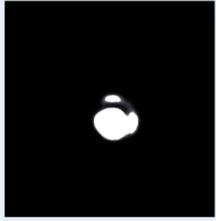
Stage 3. Optical measurement. The last stage of the optical measurement requires the fabrication process is completed all the way to the last step. The EO polymer needs to be poled and the DCM has dual slabs and the doping level is as shown in chapter 4. We applied the drive voltage,  $V$ , and monitor the output power modulation as  $V$  changes.

Follow the fabrication process flow shown in **Figure 5.16**, we have successfully measured more than 5 no-slab air-slot DCM and two 50 nm slab air-slot DCM. In **Figure 4.15**, the no-slab air-slot DCM indicates the peak-to-valley separation perfectly matches

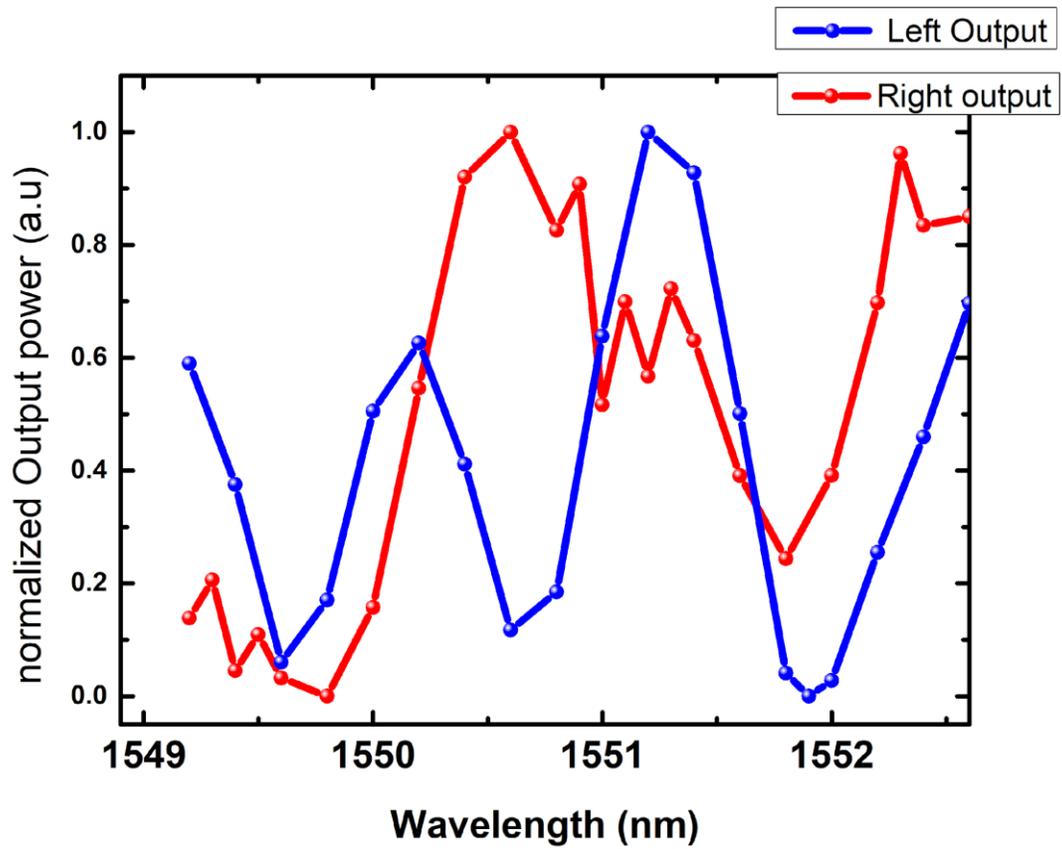
with that from the BPM simulation. **Figure 5.25(a)** illustrates the cross-sectional profile of the air-slot DCM with 50 nm slab height and **Figure 5.25(b)** shows the top-view SEM image of the nano-slot DCM structure with the Si slab. The waveguide width is 267 nm. We fabricate two identical DCMs with Si slabs to confirm the reproducibility of the mode observation and the wavelength dependence characteristics. The TE mode observation of both DCM are summarized in **Figure 5.26**. Both left and right output show nearly circular single mode profile. At the same focal length of the objective lens, when moving the objective lens from the position where we observe the single mode profile of the light coming out from the left output to the right output, we can always record the flat and long mode profile at the middle (slot waveguides region). We believe the middle mode is the higher order slab mode. In addition, both DCMs with 50 nm height slab have wavelength dependence in both TE and TM mode. The TE wavelength dependence are respectively shown in **Figure 5.27** and **Figure 5.28** for the two DCMs with slab. The average peak-to-valley separation is  $\sim 0.7$  nm.



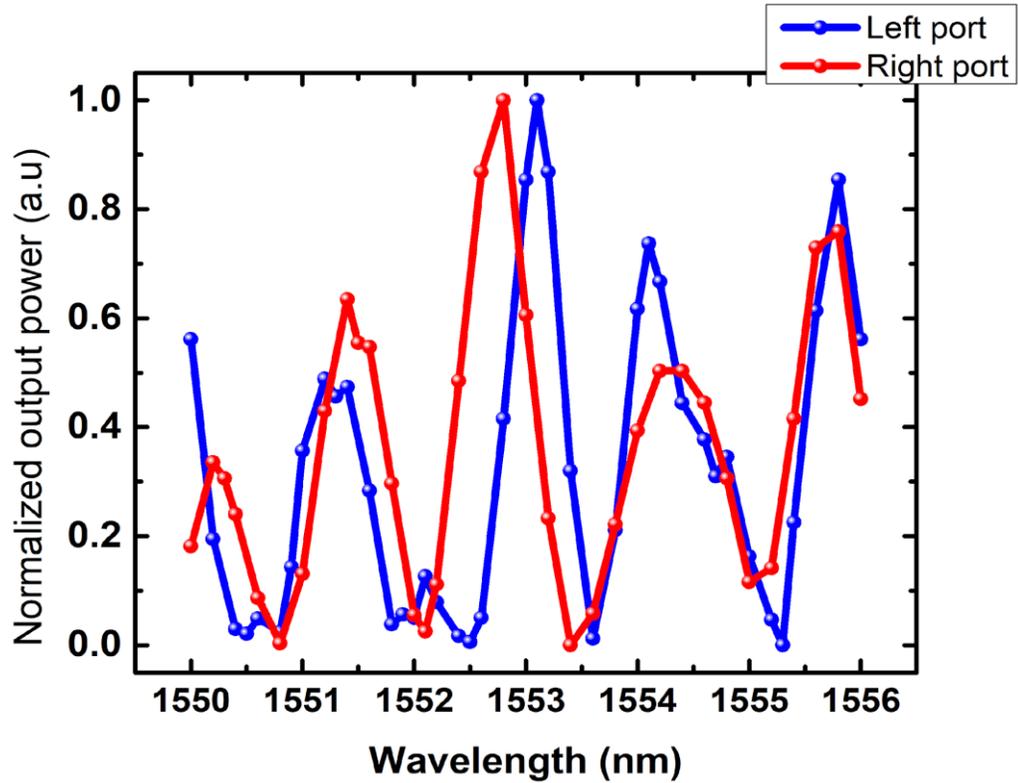
**Figure 5.25.** (a) the cross-sectional picture to illustrate an air-slot, 50 nm slab DCM. (b) The top-view SEM image of the 50 nm slab height DCM structure.

Sample #	24-1		
Position	Left output	Middle (same focus)	Right output
Observed mode			
Sample #	24-2		
Observed mode			

**Figure 5.26.** The TE mode profiles of two identical 50 nm slab height, air-slot DCMs.



**Figure 5.27.** The wavelength scanning measurement of sample 24-1, TE mode, with a 50 nm slab height, and air-slot.



**Figure 5.28.** The wavelength scanning measurement of sample 24-2, TE mode, with 50 nm slab height, and air-slot.

## 5.5 Conclusion

The process development of DCM involves EO polymer handling, process flow development and optimization. We design two checkpoints in the DCM fabrication which separately include optical measurement in air-slot and polymer-slot to evaluate the fabricated device for meeting the DCM device geometry. The rest of process optimization will be presented in the Chapter 6- future plan.

# CHAPTER 6

## CONCLUSION AND FUTURE WORK

### 6.1 Summary of accomplishments in this dissertation

Optical modulator is the key component in optical transceivers. Three key factors of optical modulators: bandwidth,  $V_\pi$ , and insertion loss, determine its application in digital communication (Datacom and Telcom) and analog communication, such as antenna remoting. Among all three factors, bandwidth is the most critical factor and need to be improved in near term. In this dissertation, we focus on the modulator design and new material to respond to the need of high speed, low  $V_\pi$ , and low insertion loss optical modulator. First, investigating new electro-optic material is a long-term goal as high EO coefficient material offers low  $V_\pi$ , short active length, which leads to high bandwidth. In this dissertation, we have demonstrated the enhancement of second harmonic susceptibility in single GaN nano-pillar and show

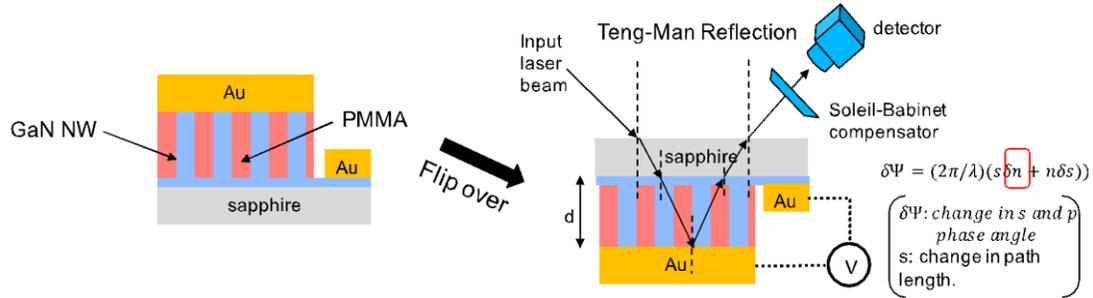
its strong potential for forming a Mach Zehnder modulator (MZM) as a semiconductor based MZM to replace commercially available LiNbO<sub>3</sub> MZM. We also fabricate the GaN nano-pillars array for incorporation into the MZM. We design the Y-junction splitter and experimentally investigated the insertion loss and evaluated the propagation loss of the GaN nano-pillars arrayed waveguide. In this dissertation, a novel modulator platform for

high  $r_{33}$  material is investigated. The nano-slot conductive waveguide directional coupler modulator (DCM) takes advantages of a strong E-field in the nano-slot, and high optical confinement in the nano-slot. We achieve a simulated figure-of-merit (3dB bandwidth/ $V_{\pi}$ ) of 202 GHz/V at  $50\Omega$  termination by BPM simulation. The  $V_{\pi}L$  is below 0.21 V·mm, which is more than an order of magnitude lower than the reversed biased PN junction Silicon MZM. To realize this DCM, we investigate the fabrication processes including the process flow, adiabatic S-bend, and Si slab extension design. Using air-slot DCM, power switching between the dual outputs is demonstrated when the incident wavelength is scanned. The strong wavelength dependence (peak-valley separation is  $\sim 1$  nm) verifies the strong cross-coupling characteristic of the DCM. The extinction ratio is  $\sim 10$  dB.

## **6.2 Future plan on GaN nano-pillars arrayed MZM**

So far, we had demonstrated the potential of utilizing GaN nano-pillars array to form a MZM device with high EO coefficient. To complete the device, we first need to reduce the GaN nano-pillars arrayed waveguide insertion loss. For propagation loss, it can be improved by smoothening the sidewall of a GaN ridge waveguide with wet chemical polishing etch. Also, we could reduce the light coupling loss by making less index mismatch between the GaN waveguide and the nano-pillars arrayed waveguide. Last, measuring second harmonic susceptibility of GaN nano-pillars is an indirect method, albeit convenient. To measure a new material's EO coefficient, Teng-Man reflection method

would be a better approach [77]. It measures the EO polymer thin film phase change from the EO effect directly. (**Figure 6.1**)



**Figure 6.1** Schematic of Teng-Man reflection method.

### 6.3 Future work of DCM

Since the nano-slot directional coupler modulator (DCM) project has not been completed, several tasks need to be developed to finish the device. I mainly separate them into two aspects: 1. Modulator active region design, and 2. fiber-to-chip coupling design. In this section, the simulation results based on mode analysis using Beam Prop simulator and the published LXM3 (commercially available EO polymer) will be presented with predictions on what would be the  $V_\pi$  of the on-going EO polymer-filled DCM.

#### 6.3.1 Modulator active region design

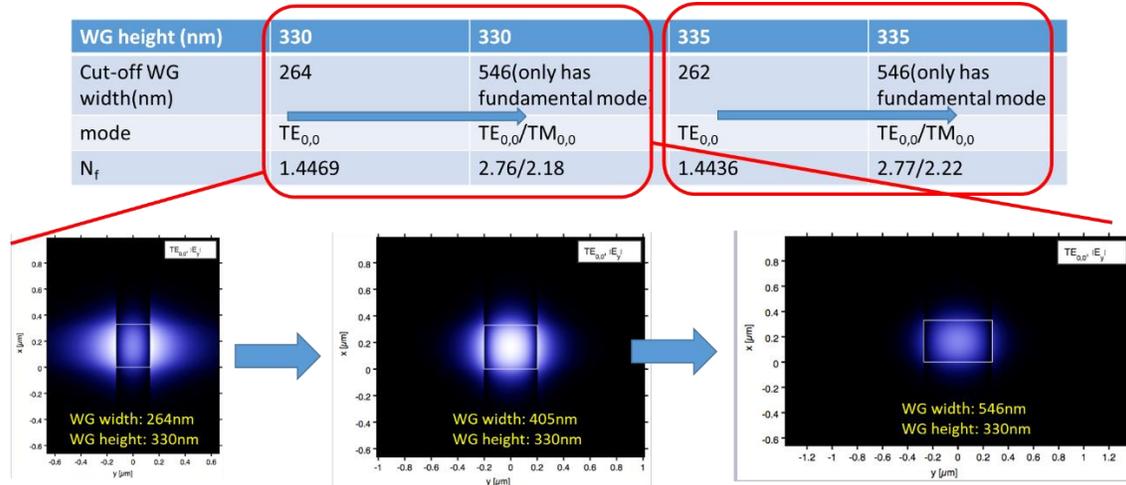
##### (a) Establishing in-line dry etch monitoring

Our goal is to demonstrate the DCM strongly cross-coupled characteristic by measuring its  $V_\pi$  (single ended, at near DC frequency) and then compare with the

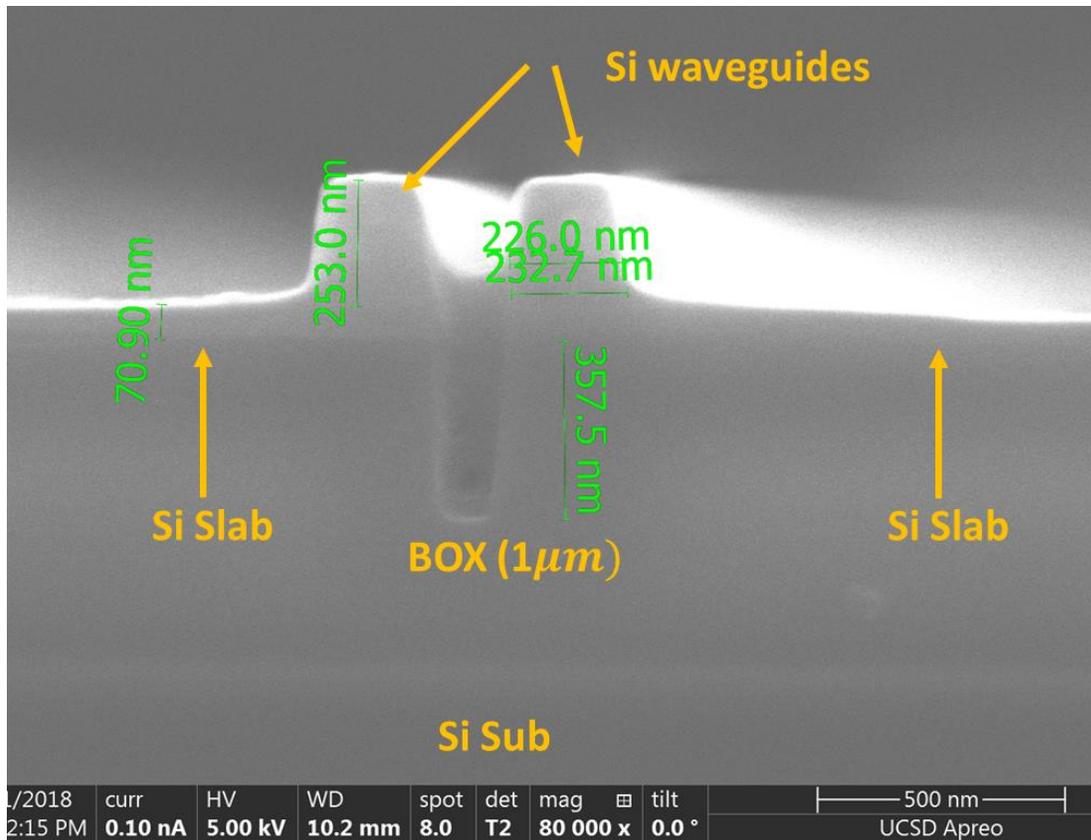
simulation results. Utilizing the 2-D multilayer waveguide mode solver variational effective index approximation [78], for a 330-335 nm tall Si waveguide, the minimum waveguide width is ~260 nm for supporting the fundamental mode (**Figure 6.2**). It should be noted that the cladding layer in the simulation is LXM3, which has a refractive index of 1.69. However, due to the variation of the Si and SiO<sub>2</sub> dry etching rates and the lack of in-line in-situ etch rate monitoring, we must set the working waveguide width to be larger than the cut-off width, even though the cut-off waveguide width may achieve the lowest  $V_{\pi}$ .

**Figure 6.3** shows the cross-sectional SEM image of the cladding SiO<sub>2</sub> which has been over-etched. It can be seen that the BOX under the slot is over-etched by ~358 nm. Even though an over-etched of BOX region under the slot will not affect the cross-coupling behavior much, but the Ar and CHF<sub>3</sub> used in SiO<sub>2</sub> dry etch recipe will still etch Si slightly since their dry etch rates are in the ratio of 19.6: 1 (etch rate of SiO<sub>2</sub> is 34.6 nm/min; etch rate of Si is 1.77 nm/min). This Si dry etch is more anisotropic. Therefore, the Si waveguides not only becomes shorter, but also reduces its waveguide width and it becomes narrower than the cut-off width. Off-line SiO<sub>2</sub> dry etch monitoring by taking cross-sectional SEM to check the remaining SiO<sub>2</sub> thickness is not reliable since the etch rate varies daily except the etch rate can be consistent for a back-to-back run on the same day. The best in-line monitor (non-destructive) would be incorporating a monitor pad on the same wafer. The alternative way is to use dummy sample then calibrate the thickness correlation between the dummy wafer and the actual wafer with DCM structure. Three equipment are available for in-line dry etch monitor: Profilometer, Ellipsometer, and

Filmatic, which calibrate film thickness by fitting the refractive light at different wavelengths with respect to film refractive index and thickness.



**Figure 6.2** Simulation results and modal profiles from “2-D multilayer waveguide mode solver variational effective index approximation,” for DCM waveguides with dimensions shown.

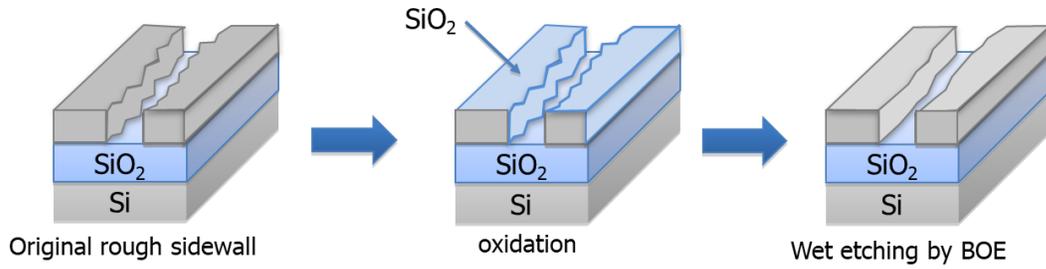


**Figure 6.3.** The cross-sectional SEM showing DCM structure with over-etched SiO<sub>2</sub> region. The Si waveguide width becomes below the cut-off width (~260 nm).

### (b) Reduction of Si waveguide/slot sidewall roughness

The sidewall roughness of Si waveguide and the roughness in the slot affect the propagation loss. More important, a smooth sidewall in the nano-slot is key to suppress leakage current during the poling of the EO polymer. We had investigated the sidewall roughness reduction using the “Cyclic oxidation etching” (COE) approach [79] [80]. In **Figure 6.4**, the wafer starts from a rough Si sidewall (right after Si dry etch) and the Si is subjected to oxidation in a furnace to form a thin layer of dry oxide. Last, the sample is

immersed in BOE for a short time to removal the SiO<sub>2</sub>. Due to the uneven SiO<sub>2</sub> oxidation rate at the sharp edges and at the smooth, flat surface, the sidewall roughness improves after a cycle of the COE. **Figure 6.5** indicates the roughness improvement after a cycle of the CEO. All RMS, average, and range are measured by the AFM.



**Figure 6.4.** Illustration of the Cyclic oxidation etching process

	RMS (nm)	Avg (nm)	Range (nm)
Ref Silicon	1.68	4.75	9.44
After dry etch 180s	4.18	10.34	26.81
thermal oxide, oxide removal	2.91	4.74	12.16

**Figure 6.5** The comparison in terms of the RMS, average, and the range of the reference silicon wafer, wafer after Si dry etch, and the wafer which had gone through a cycle of COE.

### 6.3.2 Fiber-to-chip coupling loss reduction

The key region of the DCM is the active waveguide region which has the light bouncing back and forth between two identical waveguides achieving very low  $V_{\pi}L$  and high bandwidth. However, this device also needs to meet the criteria of low insertion loss. The 1-D confinement mode-size converter suffers a  $\sim 15$  dB per facet coupling loss due to the incident light has no confinement in the horizontal direction. 2D SiON mode-size converter (MSC) will be one of the solutions to reduce the coupling loss not only because the additional confinement in horizontal direction but only SiON has higher refractive index,  $n=1.6-1.7$ , than  $\text{SiO}_2$ . This is important to better couple to the fiber mode than the  $\text{SiO}_2$  cladded mode-size converter. [81]

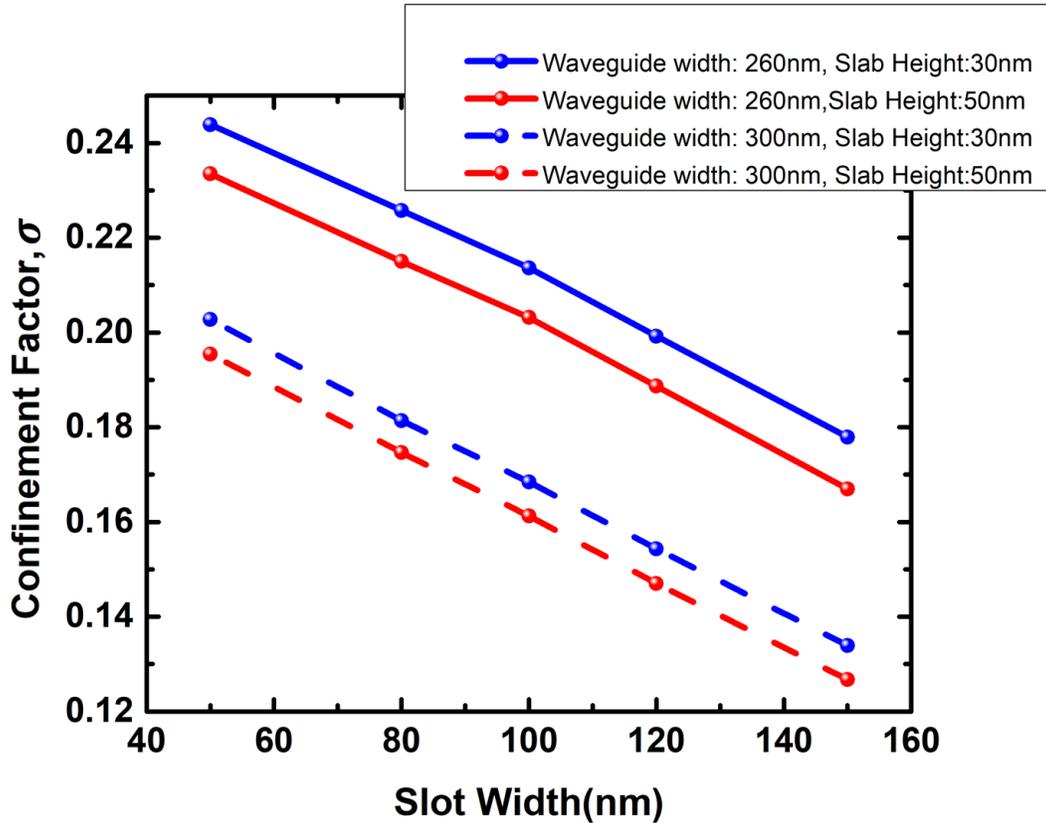
### 6.4 BPM simulation results of on-going DCM modulation performance

Due to limited number of suppliers who would provide SOI wafers for Si photonics applications (top Si layer thickness needs to be 220-330 nm), the more readily available SOI wafer has a top Si layer which is 250 nm thick. We perform a simulation for a 250 nm tall, 260-300 nm wide slot Si-waveguides. The slot is filled with LXM3, and the actual  $r_{33}$  for different DCMs slot width is referred to a published paper which shows the  $r_{33}$  value varies with slot width, [82] as summarized in **Table 6.1**. The confinement factor  $\sigma$ , for the respective DCMs are shown in **Figure 6.6**. As described in **Section 6.3.1(a)**, due to the dry etch rate variation from the dry etcher in our clean room facilities, it is difficult to control the slab height to exactly 30 nm. The simulation yields  $\sigma$  and  $V_{\pi}$  of DCMs in 30 nm and 50

nm slab height for the fabrication reference. In the DCM waveguides previously analyzed in **Section 6.3.1(a)**, we notice that the best waveguide width is the cut-off width for the fundamental mode. In the present case, the cut-off width is 260 nm. Since the Si dry etch (**Figure 5.16 step (a)&(b)**) and SiO<sub>2</sub> dry etch (**Figure 5.16 step (c)**) both show slow Si lateral etching, to be practical, we start the fabrication with a wider waveguide width to prevent the final waveguide width is reduced below the cut-off width. Therefore, the simulation includes two different Si waveguides width. Waveguide width of 260 nm gives the best  $\sigma$  and  $V_{\pi}$  of the DCM, and the experimental devices, meeting the device goals ( $\sigma$  and  $V_{\pi}$ ) should have the waveguide width within the range of 260 nm to 300 nm.

**Table 6.1.** The  $r_{33}$  at different slot widths. [82]

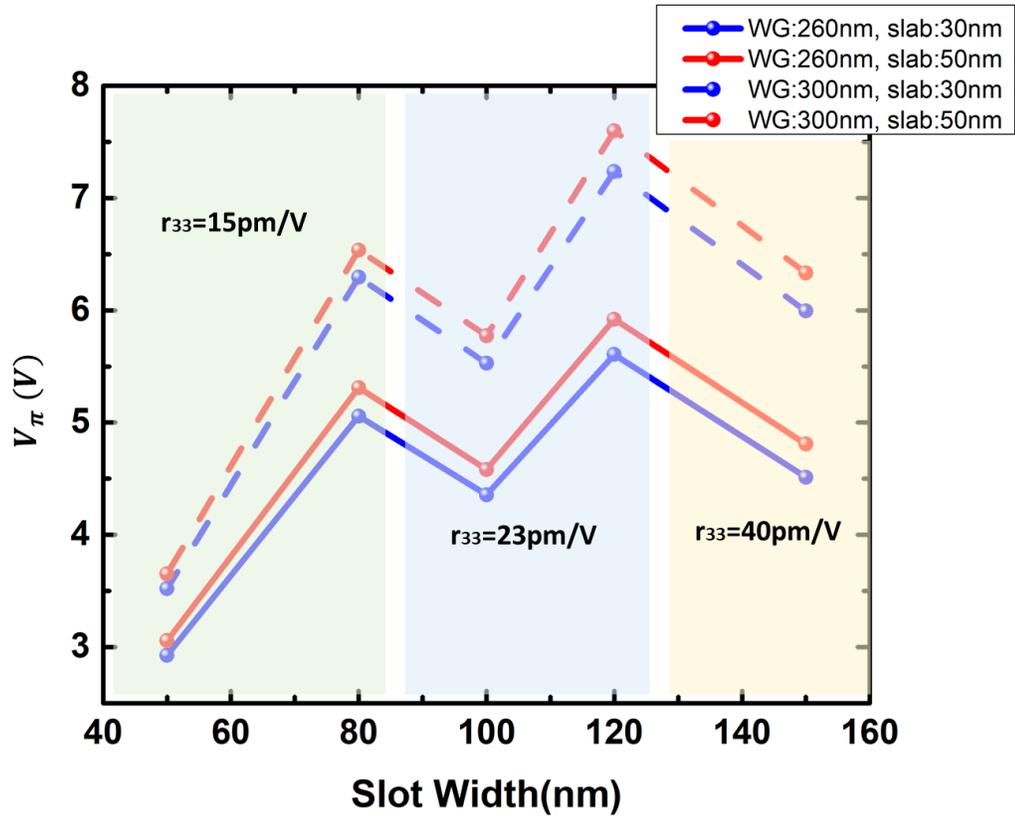
	$r_{33}$ (bulk at 1310 nm)	$r_{33}$ (in device at 1550 nm) slot width 60-80 nm	$r_{33}$ (in device at 1550 nm) slot width 100-120 nm	$r_{33}$ (in device at 1550 nm) slot width > 150 nm
GigOptix LXM3	86 °C	15 pm/V	23 pm/V	40 pm/V



**Figure 6.6** The confinement factor  $\sigma$ , of the 30 nm and 50 nm slab height DCM. The slot width ranges from 50 nm to 150 nm.

In **Figure 6.6**, the simulation is based on the optical geometry given as: Si waveguide width is 260 nm or 300 nm; waveguide height is 250 nm; slot width variations are 50, 80, 100, 120, and 150 nm; refractive index in the slot and in the cladding is 1.69. The confinement factor  $\sigma$ , does not degrade much as the slab height increases from 30 nm to 50 nm. The reason had been explained in the discussion of **Table 4.2**. This gives us a wider process window to build the device. **Figure 6.7** presents the calculated  $V_{\pi}$  in the following conditions: slot width in the range 50-200 nm; slab height is 30 nm or 50 nm. The

calculation is based on **Equation 4.7** with the reported  $r_{33}$  for different slot widths (**Table 6.1**) and  $\sigma$  (**Figure 6.6**). Even though the  $\sigma$  decreases as the slot width expands, but the actual device  $r_{33}$  is enhanced due to the higher poling efficiency at wider slot. Based upon these simulation results, I would recommend the DCM with 150 nm slot width and that would give an upper bound (for waveguide width of 300 nm and slab height of 50 nm) for  $V_{\pi}$  as 6.3V. It should be noted that the  $V_{\pi}$  is calculated with the single ended configuration, not the push-pull (differential driver) configuration. Last, the main reason for simulating the actual DCM parameter is not only for predicting the outcome performance, but also for ensuring  $V_{\pi}$  is below the poling voltage (20V). Therefore, researchers can observe the full power switching from one port to the other port at  $V_{\pi}$  without the concern that the DCM may breakdown or induce a high leakage during the measurement.



**Figure 6.7.** Calculated  $V_\pi$  for DCMs with the slab height of 30 nm and 50 nm versus the slot width which ranges from 50 nm to 150 nm. The rest of optical geometry in the simulation: the Si waveguide height is 250 nm; the refractive index in the nano-slot and in the cladding is 1.69 (LXM3).

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