Title
A 4-MHz, 256-Channel Readout ASIC for Column-Parallel CCDs With 78.7-dB Dynamic Range

Journal
IEEE Transactions on Nuclear Science, 67(5)

ISSN
0018-9499

Authors
Grace, CR
Denes, P
Fong, E
et al.

Publication Date
2020-05-01

DOI
10.1109/tns.2020.2980769

Peer reviewed

A 4 MHz, 256-Channel Readout ASIC for Column-Parallel CCDs with 78.7-dB Dynamic Range

C.R. Grace, *Senior Member, IEEE*, P. Denes, *Member, IEEE*, E. Fong, *Member, IEEE*, A. Goldschmidt, and A. Papadopoulou, *Member, IEEE*

***Abstract*— A 256-channel readout Application Specific Integrated Circuit (ASIC) called the Very High-Speed Analog Sampling Engine, or VASE, intended for the readout of Column-Parallel Charge-Coupled Devices (CP-CCDs), is presented. Each channel employs a charge-sensitive amplifier and a first-order dual-gain sigma-delta Analog-to-Digital Converter (ADC) that acts as the front end of an Extended Counting ADC. The Extended Counting ADC directly implements Correlated Multiple-Sampling as part of its operation. To reduce the noise due to input capacitance and to ensure a compact camera, the VASE input bonding pads are pitch matched to the CP-CCD to allow chip-to-chip bonding with minimal parasitic capacitance. The chip is designed in a modular way with each 16 input channels sharing a single differential analog output and digital serializer. VASE, with a die area of 38.1 mm^2 and fabricated in 180 nm CMOS technology, achieves 22 e$^-$ Equivalent Noise Charge (ENC) and a dynamic range of 190 ke$^-$ (78.7 dB) at a 4 MHz pixel rate (corresponding to a frame rate of 32 kfps when a 256 by 256 pixel sensor is read out on both sides) while dissipating 10.1 mW per channel. The prototype has been used to successfully image X-ray diffraction at a soft X-ray synchrotron.**

Index Terms—Mixed-Signal IC Design; Charge-Coupled Devices; Analog-to-Digital Conversion; Correlated Double Sampling

I. Introduction

The Very Low-Noise Analog Sampling Engine (VASE) is a custom mixed-signal integrated circuit intended for the readout of Column-Parallel Charge-Coupled Devices (CP-CCDs). Fast, 2-D soft X-ray detectors are valuable tools in instrumenting both Synchrotron-based and Free-Electron Laser-based soft X-ray sources. Low-noise readout is important to successfully image samples with low-energy X-rays, and high speed is important to be able to image evolving, dynamic processes. These requirements typically trade off directly and to provide both simultaneously requires re-thinking the typical CCD readout system.

In a conventional voltage-mode CCD, charge is shifted row-by-row into a serial shift register. The serial register then shifts charge onto a floating diffusion connected the gate of an output source follower, as shown in the top schematic in Fig. 1. For each pixel, the floating diffusion is reset (and read) and then signal charge is transferred to the floating diffusion (and read) [1]. This is an inherently slow process. To speed up the readout of the CCD, multiple horizontal shift registers and source-follower buffers can be added. However, the source follower buffer, while effective and nearly universal in CCD design, requires area in layout, which limits the number of columns that can be read out in parallel [2], particularly in CCDs implemented in processes optimized for fully-depleted CCDs, as they are not optimized for fine line lithography and therefore their design rules are typically several generations behind CMOS processes [3].

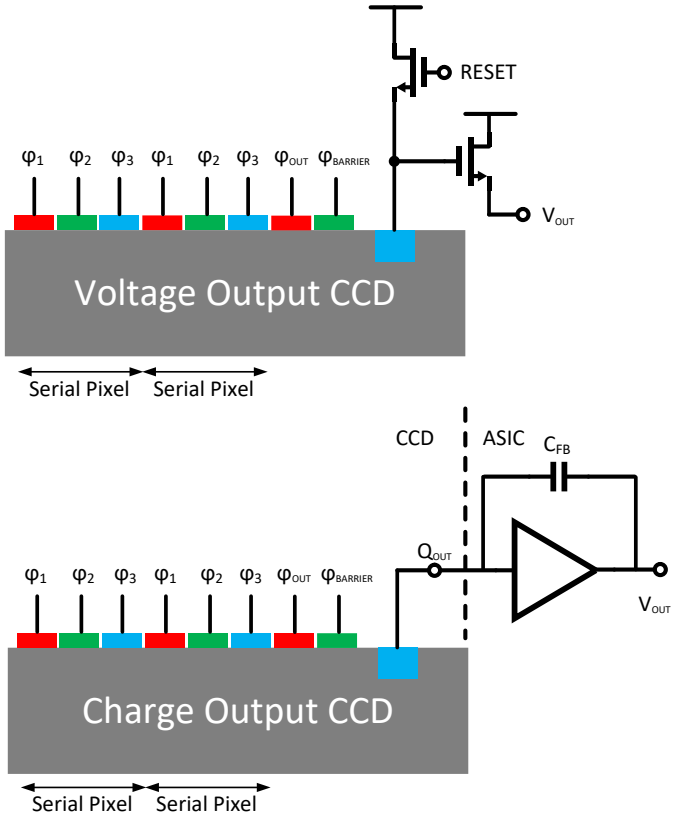

Fig. 1. Comparison of voltage output and charge output CCDs.

Some CCDs optimized for soft X-ray detection, such as the well-known pnCCD [4], are able to fit column-level source followers on the same die as the CCD. However, the pnCCD reported in [4] reads out 1024 rows at a maximum frame rate of 200 Hz, giving a pixel rate of 204.8 kHz, which limits the range of dynamic processes that can be captured. To increase the speed in fabrication processes in which it is not possible to design sufficiently fast source followers that fit within the column width, the horizontal shift register and output amplifier can be removed and the columns can shift their output charge directly off the CCD. In contrast to a voltage-input amplifier, this requires a charge-sensitive amplifier to provide the low input impedance needed for the charge transfer. In the bottom

Manuscript received December 2, 2019. This work was supported by the U.S. Department of Energy under Contract No. DE-AC02-05CH11231.

The authors are with the Lawrence Berkeley National Laboratory, Berkeley, CA, 94720, USA (email crgrace@lbl.gov).

schematic of Fig. 1, the source follower buffer and reset switch are removed and the charge is directly shifted off the CCD and converted to the voltage domain by a charge-sensitive amplifier that, in this case, is not on the same die as the CCD. By obviating the source follower buffers, each column can be read out in parallel, greatly increasing frame rate for a given pixel rate. The output diffusion is then reset between each pixel read by the readout ASIC rather than by a switch internal to the CCD. An early version of the CP-CCD concept was reported in [5], however its associated readout ASIC had a much lower dynamic range (approximately 5 bits) and was clocked at 1 MHz, so is not suitable for this application.

An example camera system using a CP-CCD is shown in Fig 2. A 256 by 256 pixel CP-CCD is read out by a number of readout channels equal to the number of CP-CCD columns. The CP-CCD is clocked such the two halves of the CP-CCD are clocked out in opposite directions, so each readout ASIC instruments 128 rows and 256 columns, further increasing the readout speed. These readout channels are then multiplexed to a smaller number of digitizers and the digital data stream is finally sent to a Data Acquisition System (DAQ).

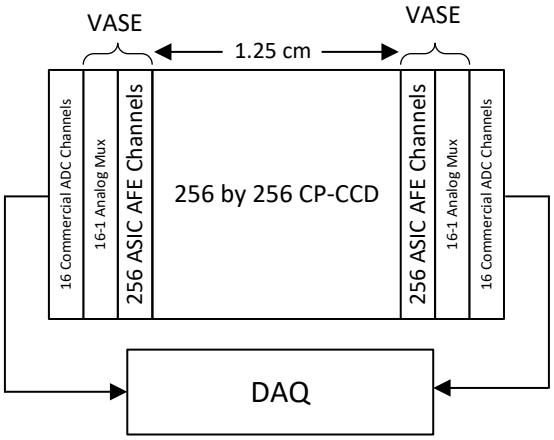

Fig. 2. Example camera system using CP-CCD and VASE.

Due to practical design constraints, the number of readout channels that can be comfortably implemented on a single die is limited to about 256. Extending the number of channels in a system beyond this level requires that the readout ASICs are buttable on the top and bottom. To accommodate some dead area where the chips are butted, the ASIC bonding pad pitch channel pitch is 4 µm less than channel pitch. Process design rules mandate that all pads on the input side of the chip be allocated to CP-CCD signal connections. One consequence of this pad partitioning is that power connections to the ASIC can only be made on the readout side of the chip. This severely constrains the power that can be dissipated in the channels as the input side of the channels is physically remote from needed power and ground connections. To enable low-noise readout, the capacitance at the input of the readout ASIC should be minimized. This can be done by pitch matching the readout ASIC channels to the CP-CCD output columns and directly bonding the output pads of the CP-CCD to the input pads of the ASIC. In this work we report on the VASE ASIC, a highly integrated data acquisition chip that enables a CP-CCD to provide 2-D soft X-ray imaging with high speed and low noise.

II. VASE Design Considerations

A. Chip Architecture

VASE is intended to read out high dynamic-range CCDs. A straightforward approach to the readout of high dynamic-range CCDs would be to include a high dynamic-range ADC in each channel. The specific CCD that VASE is intended to instrument is operated with a dynamic range of approximately 16 bits. Because of severe power constraints, however, it is impractical to implement a 16-bit ADC directly in the readout channel. Fortunately, we can take advantage of photon statistics to relax the constraints on the ADC. Simply put, the variance of photon energy is proportional to the square root of the number of incident photons because photon arrival can be modeled as a Poisson process [6]. Therefore, lower resolution is required in bright conditions (i.e. a larger LSB is acceptable) than when in low light conditions. In other words, while VASE should be able to accommodate input charge spanning a 16-bit dynamic range, it does not need to provide full 16-bit resolution across the entire dynamic range.

A conceptual block diagram of the VASE prototype ASIC is shown in Fig 3. This block diagram is meant to convey the concept of a floating-point front end, not to indicate how the channels are actually implemented. The low resolution MSB ADC and the higher-resolution LSB ADC together comprise an Extended Counting ADC [7]. An Extended Counting ADC is a technique that combines a sigma-delta modulator to convert the most significant bits (called the MSB ADC here) with a higher-speed ADC (such as a SAR ADC) to convert the least significant bits (called the LSB ADC here) [8]. The low-resolution ADC digitizes the analog residue from the sigma-delta. In this way, the Extended Counting ADC reuses the input range of the LSB ADC to extend the overall ADC's dynamic range by an amount depending on the resolution of the MSB ADC. An Extended Counting ADC behaves in a similar way to a numerical floating-point system, in that the dynamic range is enhanced and the resolution is reduced as the magnitude is increased.

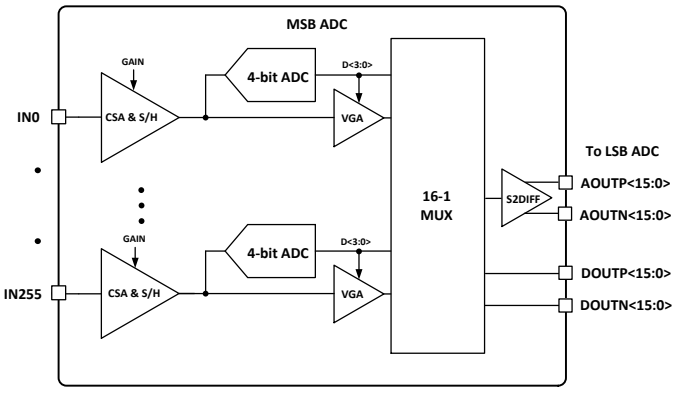

Fig. 3. Conceptual block diagram of VASE.

Each channel has a charge-sensitive amplifier (CSA) as the front end to acquire the signal from the CP-CCD and convert it to a voltage. The CSA output is then digitized using the low-resolution MSB ADC which gives information on the magnitude of the input signal. The variable gain amplifier (VGA) amplifies the CSA output and this residue is then

digitized again by the higher-resolution LSB ADC. The MSB ADC automatically selects a front-end gain prior to the LSB ADC. The resultant gain-setting bits are combined with the linear ADC bits from the LSB ADC to give the final composite ADC output.

By combining the MSBs and the LSBs, a wider dynamic range can be digitized but the maximum resolution is limited by the resolution of the LSB ADC.

B. Sigma-Delta-Based Correlated Multiple Sampling

Besides digitization, the CP-CCD readout channels require a correlated double sampling (CDS) function to reduce reset noise generated in the CSA. In CDS, the reset level of the CP-CCD is first acquired and then the reset plus signal is acquired. By subtracting the two samples, the reset noise is canceled. While CDS eliminates reset noise and other low-frequency noise sources (for example flicker noise) it increases the thermal noise contribution of the front end because the output thermal noise of the front-end amplifier is uncorrelated from sample to sample. To overcome this limitation, the Correlated Multiple Sampling (CMS) technique has been developed extensively [9, 10]. CMS is conceptually an extension of the CDS technique. By increasing the number of samples of both the reset level and the signal level, the thermal noise is reduced by $\sqrt{N}$ (at the expense of speed). CMS is typically implemented using an integrator that can sum a plurality of reset samples and a plurality of signal samples. These integrated signals can then be subtracted in either the analog or digital domain to eliminate low-frequency noise and reduce high-frequency noise [11].

While CMS is effective in reducing thermal noise, it can be impractical to implement directly because of the headroom requirements of the analog integrator. This dynamic range problem can be addressed by adding a comparator. Here, when the limit of the dynamic range of the integrator is reached, the comparator is triggered and the integrator output is reset. By keeping track of how many times the comparator is triggered in an acquisition, the effective channel gain is increased while the issue of integrator headroom is circumvented [12].

This key idea can be extended to sigma-delta modulation by introducing a reconfigurable modulator. The modulator uses a non-inverting integrator for reset, and an inverting integrator for signal. Therefore, the required subtraction happens automatically. Moreover, the modulator digital outputs can be filtered to provide the MSBs. In case the CP-CCD charge injection is small enough that it does not need to be cancelled, then the modulator can be operated in a traditional sigma-delta mode, further lowering the noise (by doubling the oversampling ratio).

The concept of oversampling a CSA output can be counterintuitive, especially when hard reset is used. In this case, the reset switch generates a noise power of kT/C_{FB} on the feedback capacitor (where C_{FB} is the CSA feedback capacitor). This noise is canceled using the CMS algorithm (analogous to how CDS cancels kTC noise in image sensors). Oversampling works here because while the sampled noise is fixed, the CSA continuously generates thermal noise across samples, even after it has settled. It is this CSA-generated thermal noise that is primarily reduced by $\sqrt{N}$ by the sigma-delta loop.

C. VASE Channel

In VASE, the required CMS function is merged with the front-end of the Extended Counting ADC by using sigma-delta modulation [13]. The sigma-delta modulator implements a 3-bit MSB ADC that provides 2 effective bits because of the CMS subtraction inherent to the modulation. In addition, another bit is provided by parallel modulator (see below). Four front-end gain settings provide another 2 bits of dynamic range. An off-chip commercial 12-bit ADC digitizes the analog LSB reside output from the sigma-delta modulator. The 12-bit LSB ADC output is combined with the 4-bits digitized on VASE (2 from the modulator, 1 from the parallel modulator scheme, and 2 from the gain settings) to make a composite 16-bit ADC word. Parasitic capacitance in the CSA limited the size of the gain steps, giving an effective dynamic range of about 14 bits.

A simplified block diagram of the channel used in VASE is shown in Fig. 4. The CP-CCD column output is connected to the charge-sensitive amplifier (labeled CSA). The signal charge from the CP-CCD in integrated and converted into a voltage by the CSA. After the CSA, the signal is presented to a first-order, reconfigurable sigma-delta modulator. The sigma-delta modulator embodies both the ADC and VGA functions of the MSB ADC in Fig 3. The modulator oversamples the output of the CSA, reducing noise, and filters the comparator outputs to generate the digital MSB ADC output. The analog residue of the sigma-delta modulator is then sent off-chip for fine digitization by the LSB ADC. Each block of 16 VASE channels includes a shared analog buffer (which interfaces the VASE ADC residue to a commercial ADC that is used as the Extended Counting ADC backend) and a high-speed digital serial interface which transmits the MSBs generated by the sigma-delta ADCs off chip. The sigma-delta loop in the VASE channel simplifies the system by making the subtraction of the reset level from the signal level inherent to the operation of the modulator. In other words, there is no need for a dedicated CMS circuit here because the function is embedded in the operation of the sigma-delta modulator.

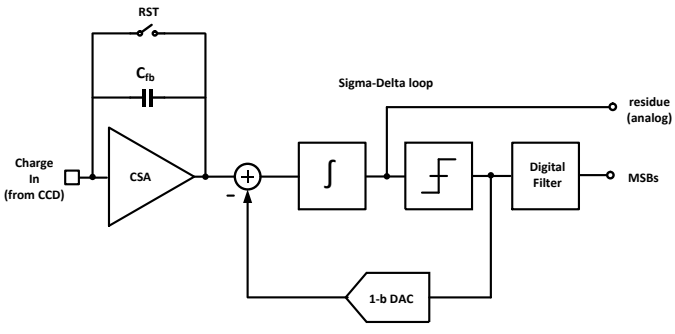

Fig. 4. Simplified block diagram of VASE channel. The CMS is implemented as part of the ADC function by oversampling the CSA output using the modulator and reconfiguring the modulator in the middle of the cycle to cancel reset noise.

D. Reconfigurable Sigma-Delta Modulator

The basic idea of the reconfigurable sigma-delta modulator is to integrate the reset level in one direction and then integrate the reset plus signal level in the opposite direction, canceling the reset noise. This is done by reconfiguring the operation of the modulator in the time between the reset and the arrival of signal. A simplified schematic of the reconfigurable sigma-delta modulator along with its timing diagram is shown in Figure 5.

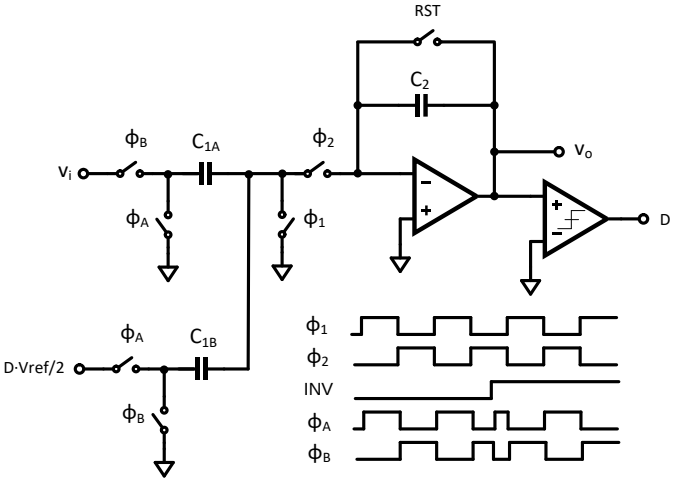

Fig. 5. Reconfigurable sigma-delta Modulator with timing diagram.

The modulator can be configured as either an inverting or non-inverting modulator based on the settings for the clocks φ_A and φ_B. When the control signal INV is low, φ_A and φ_B are equal to φ_1 and φ_2, respectively and the modulator uses a non-inverting integrator. When INV is high, φ_A and φ_B switch connections and the modulator now uses an inverting integrator. By integrating the reset level in one direction, then reconfiguring the modulator before integrating the signal level, the signal samples are subtracted from the reset level samples. In this way, the CMS is implemented inherently by the sigma-delta modulator without the need for an explicit subtractor circuit that would dissipate additional power and generate noise.

The sigma-delta modulator can be operated at different oversample ratios and speeds. When VASE is operated at 4 MHz, the sigma-delta oversamples by a factor of 8. Because the modulator is reconfigured to halfway through a conversion in order to implement the CMS subtraction, the effective oversampling ratio is 4. The modulator itself is first order, so it is inherently stable [12].

E. Parallel Sigma-Delta Modulators

To add an additional bit of dynamic range to VASE, there are two parallel sigma-delta modulators in each channel. One modulator has a gain G times larger than the other. The outputs of both modulators are monitored and if the high-gain modulator saturates, the low-gain modulator's output is used, otherwise the output of the high-gain modulator is used. This is shown schematically in Fig. 6.

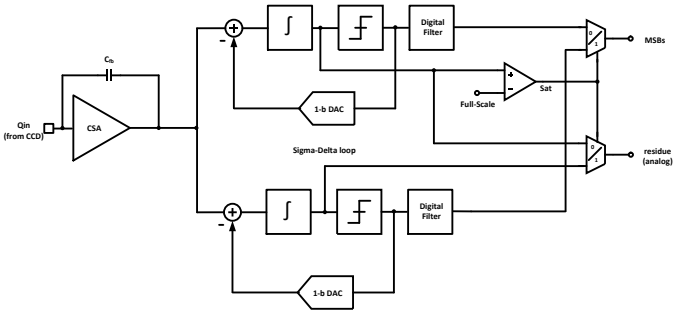

Fig. 6. Parallel sigma-delta modulators used to add additional bit to dynamic range.

F. Modulator Analysis

The VASE sigma-delta modulator can be operated in three modes: CMS, inverting sigma-delta, and non-inverting sigma-delta. Expressions for the LSB residue and the modulator analog input estimate after M samples are given below. Derivations for these expressions are in the Appendix. The various equations are summarized in Table 1.

TABLE I. SUMMARY OF MODULATOR EXPRESSIONS

Equation	Description
1	MSBs in CMS mode
2	LSB analog output in CMS mode
3	Derived modulator input in CMS mode
4	LSB analog output in inverting output
5	Derived modulator input in inverting mode
6	LSB analog output in non-inverting mode
7	Derived modulator input in non-inverting mode

These equations should be used to determine the VASE sigma-delta analog voltage input (CSA output) given a LSB and MSB output. This can be useful in reconstructing the input waveform from the output data. To refer the modulator input to the VASE charge-domain input, divide by the CSA gain. The symbols are defined in Table 2.

TABLE II. SYMBOLS USED IN MODULATOR EXPRESSIONS

Symbol	Description	Note
V_o	Modulator LSB output	
V_i	Modulator analog input	
V_r	Modulator analog input (CCD reset level)	
V_s	Modulator analog input (CCD signal level)	Only used in CMS mode
ΔV_{ref}	Reference voltage (full reference range is +/-	Size of modulator correction packet

Symbol	Description	Note
	ΔV_{ref})	
M	Oversampling ratio	
G	Modulator gain	M is one half in CMS mode because two inputs processed
N	Number of effective output bits	1 for low-gain modulator, 2 for high-gain modulator
D_F	Final digital output (DR + DS) where DR and DS are the digital filter output for the reset and signal digitizations, respectively	CMS = 3 Inverting or noninverting = 4

In CMS mode, the digital MSBs are calculated using

$$D_F = TRUNC\left\{\frac{(v_r - v_s) + 2\Delta V_{ref}}{2^{-(N-1)}}\right\} + 2^{(N-2)} \quad (1)$$

The LSB output of the modulator is

$$v_o = \frac{GM}{2}(v_r - v_s) + (M - D_F)\Delta V_{ref} + V_{cm} \quad (2)$$

The CP-CCD input corresponding to the modulator LSB output is

$$(v_r - v_s) = \frac{2(v_o - V_{cm} - (M - D_F)\Delta V_{ref})}{GM} \quad (3)$$

When VASE is configured to operate in inverting mode (CMS is not used, so an additional effective bit is available) the LSB output is

$$v_o = -\frac{1}{2}\left(Mv_i - (M - 2D)\Delta V_{ref}\right) + V_{cm} \quad (4)$$

And the corresponding analog input is

$$v_i = \frac{-2(v_o - V_{cm}) + (M - 2D)\Delta V_{ref}}{M} \quad (5)$$

When VASE is configured to operate in non-inverting mode (CMS is not used, so an additional effective bit is available) the LSB output is

$$v_o = \frac{1}{2}\left(Mv_i + (M - 2D)\Delta V_{ref}\right) + V_{cm} \quad (6)$$

And the corresponding analog input is then

$$v_i = \frac{2(v_o - V_{cm}) - (M - 2D)\Delta V_{ref}}{M} \quad (7)$$

In both the inverting and non-inverting mode the MSBs are simply the filter modulator decisions D.

G. Crosstalk

The crosstalk in VASE should be as low as practical. This is done by ensuring the effective input capacitance of the preamplifier is much larger than the parasitic coupling capacitance between channels. In this way, charge will preferentially flow to the preamp input virtual ground rather than to neighboring channels.

A schematic illustrating the origin of crosstalk in VASE is shown in Fig. 7. The CP-CCD and VASE use pads that are staggered in a complementary way, simplifying chip-to-chip bonding.

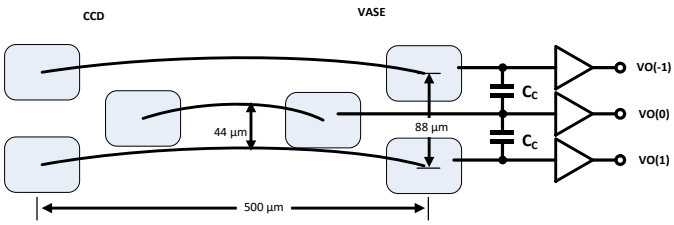

Fig. 7. Pad structure of CP-CCD and VASE, showing origins of crosstalk.

The crosstalk in a charge sensitive readout array is approximately C_C/C_{in} here C_C is the lumped coupling capacitance between channels and C_{in} is the effective input capacitance of the readout amplifier ($C_{in} \approx C_F(1+A)$, where C_F is the CSA feedback capacitor and A is the open loop gain of the CSA) [14].

There are two main contributors to C_C. The first, and dominant, contributor is the mutual capacitance of the bondwires. As previously described, the CP-CCD output and VASE input pads are staggered giving a 44 µm effective pitch for bonding (the CP-CCD and VASE channels themselves have a 48 µm pitch). The CP-CCD and VASE are connected together using bondwires which have a mutual capacitance that allows a signal in one channel to appear in adjacent channels. The second contributor to crosstalk is the parasitic routing capacitance internal to VASE.

The parasitic routing capacitance can be estimated using software extraction of the layout. The bondwire capacitance can be estimated using the equation for capacitance of parallel wires [15] and is

$$C_{C,bondwire} = \frac{\pi \varepsilon l}{ln\left(\frac{d}{2a} + \sqrt{\frac{d^2}{4a^2} - 1}\right)} \quad (8)$$

In Eq 8, ε is the dielectric constant, l is the length of the wires, d is the distance between the wires, and a is the wire thickness. Assuming a bondwire thickness of 0.8 mil and a distance between bondwires of 44 µm (about 1.75 mils), the coupling capacitance is 64.7 fF/mm. In the case of the longer

wires, and neglecting shielding effects of the inner bondwire, the coupling capacitance is 19.6 fF/mm.

The channel-to-channel parasitic capacitance internal to VASE varies due to channel wiring specifics but has a worst case of approximately 20 fF to adjacent channels. The coupling to channels once removed internal to VASE is negligible. Therefore, given these assumptions, the maximum coupling capacitance for adjacent channels is 40 fF and the coupling capacitance to channels once removed is about 10 fF.

Given the minimum feedback capacitance of 5 fF and the simulated open-loop gain of about 700, the minimum expected C_{in} = 5fF(1+700) = 3.5 pF. The ratio of C_c to C_{in} for adjacent channels is then 40/3500 or about 1%, giving an expected crosstalk of the same order-of-magnitude.

III. *Prototype*

A photograph of VASE glued to a PCB and directly bonded to a CP-CCD is shown in Fig. 8. The channel inputs are arrayed along the bottom of VASE and the LSB analog output and MSB ADC bits leave along the top of the die. The 256-channel VASE prototype measures 12.3 mm by 3.1 mm. The capacitance seen by each VASE channel is approximately 100 fF (including CP-CCD and VASE bonding pads and the bond wire).

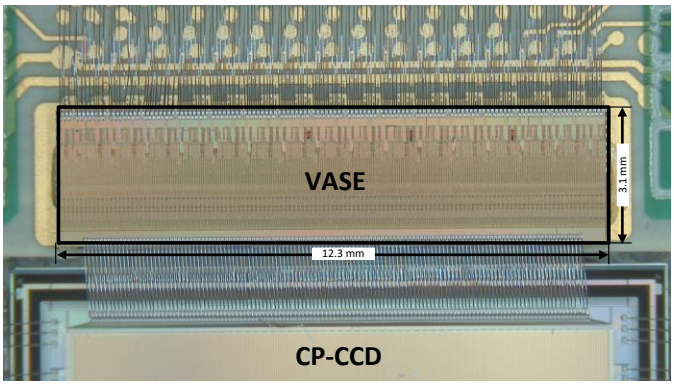

Fig. 8. VASE die bonded directly to CP-CCD. The bonding pitch is 44 µm.

The 256-channels in VASE are organized into 16 distinct 16-channel modules. The layout of a single 16-channel module is shown in Fig. 9. The analog outputs of the modulators are sent off chip using class A/B line drivers [16] and the digital outputs are sent off chip using a shift-register based serializer and LVDS digital drivers [17]. To synchronize the analog and digital data streams, VASE also includes a test mode where known analog and digital patterns are sent. The CSA uses a traditional folded-cascode design [18] and the sigma-delta modulators use single-ended versions of the class A/B op amp used in the line driver to save power. The capacitors in the sigma-delta modulators are implemented using Metal-Insulator-Metal structures. The small feedback capacitance required in the CSA is implemented using a custom finger capacitor realized using interconnect metals [19].

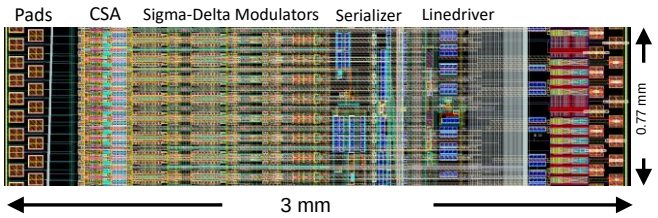

Fig. 9. Layout of a 16-channel VASE module.

IV. Measured Results

A photograph of the test PCB that corresponds to the diagram in Fig. 2 is shown in Fig 10. A 256 by 256 pixel prototype CP-CCD (the square die in the center) is read out on both sides by VASE ASICs (the skinny chips on the left and right of the CP-CCD which implement the MSB ADCs and the CMS function) and commercial 12-bit ADCs (the larger packaged chips on each side that implement the LSB ADCs).

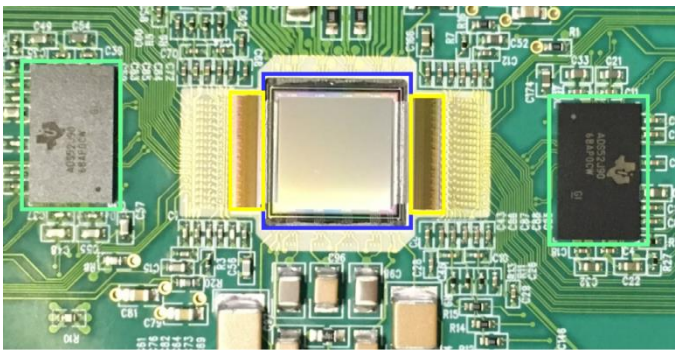
Fig. 10. System evaluation PCB.

The full test stand is shown in Fig 11. The camera head attached to the vacuum chamber sitting on the bench is connected to a stack of programmable power supplies that provide power for the high-speed CP-CCD and VASE clocking.

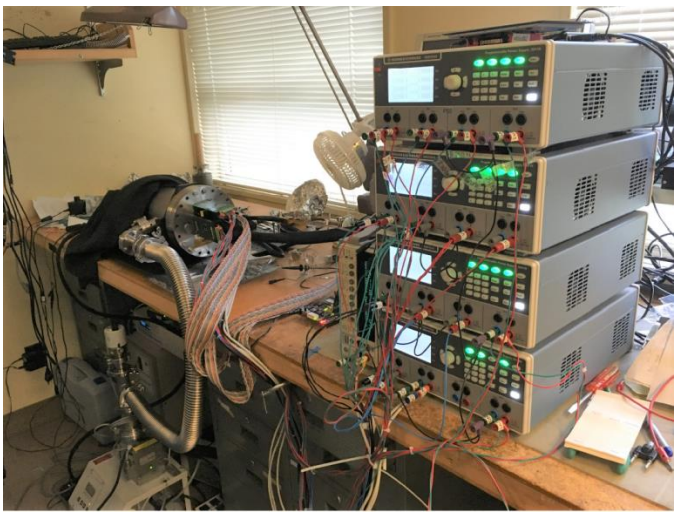
Fig. 11. Camera system test stand.

The measured input-referred noise is shown in Fig. 12 for an idle VASE channel in its maximum gain configuration. In this measurement, the input was left floating and the variance in the dc output was recorded using a high-resolution (16-bit)

ADC [20]. The LSB to e^- conversion was done using a neighboring channel connected to an injection capacitor. The rms deviation is about 22 e^- (without input capacitive loading).

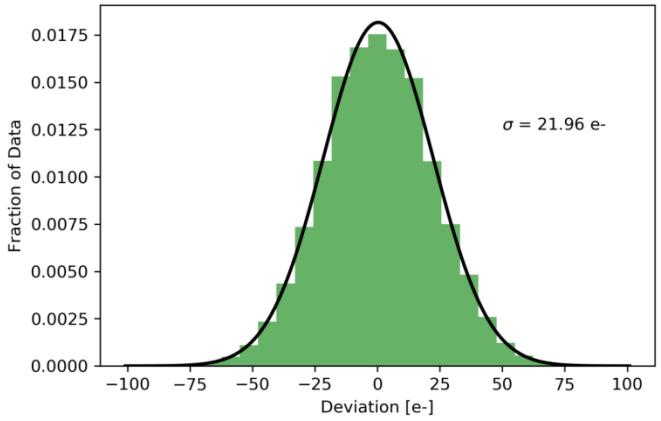

Fig. 12. VASE measured noise. Input is left floating.

A reconstructed transfer function measured using the high-gain sigma-delta setting (only a single sigma-delta is used in this measurement for clarity) is shown in Fig. 13. The sigma-delta bits (MSBs) are combined with the digitized residue to generate the curves. The four plotted gains correspond to different gain settings for the CSA. During stand-alone VASE testing, a 16-bit ADC was used to implement the LSB ADC. To model the intended 12-bit LSB ADC, we only used part of the ADC dynamic range. This, combined with the MSBs, gives the range of values in the y-axis which covers approximately 14 bits when scaled (25000 16-bit codes → 3125 12-bit codes * 2 for additional sigma-delta modulator * ~2 to account for CSA gain settings gives a value of about 12500, which is approximately 14 bits). The VASE front end is biased such it can respond to relatively small inputs of negative polarity, and this accounts for the x-axis in the plot including negative injected charge. VASE responds to negative charge in all gain settings, but the input dynamic range is small in those cases. The dynamic range when the CSA is configured for minimum gain is approximately 70 ke^-. This is combined with the low-gain sigma-delta setting (dynamic range of 120 ke^-) to give an overall dynamic range of about 190 ke^-.

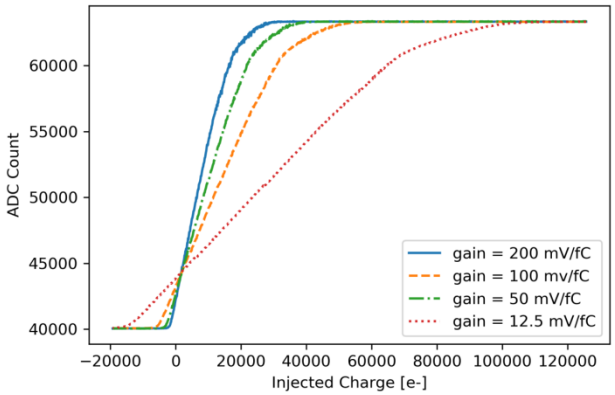

Fig. 13. Measured VASE transfer function.

The VASE noise breakdown in high-gain configuration is shown in Fig. 14. The noise is dominated by the sigma-delta modulator (54.5%) and the CSA (28.1%). This is due to power dissipation considerations (the achievable g_m in the modulator amplifiers and the CSA is limited) and due to the requirement to accommodate large charge inputs in the CSA even in high-gain mode (which limits the maximum CSA gain).

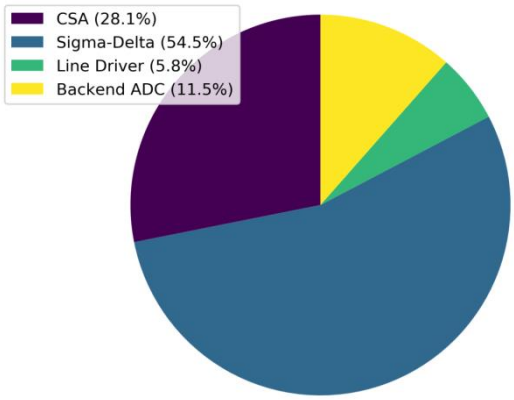

Fig.14. VASE noise breakdown when configured for maximum gain.

VASE is intended to be operated in a controlled environment and therefore good performance across temperature is not a key requirement. VASE has been operated at room temperature and also at -10 °C to read out a cooled CP-CCD. No significant functionality differences were observed between these temperatures.

The maximum pixel readout rate of VASE was measured to be 4 MHz. When data is clocked in from the CP-CCD at faster rates, the noise performance and linearity degrade quickly, indicating op amp settling errors. This measured maximum pixel rate differed by at most about 10% across channels. Performance was relatively uniform at lower pixel readout rates.

The channel-to-channel gain mismatch was low. While the absolute gain varies by approximately 10% from chip to chip, within a chip the channel-to-channel gain mismatch is dominated by capacitor mismatch which is expected to be better than a few percent and was consistent with observations.

The camera shown in Fig. 10 has been tested at several light sources. A ptychography test sample imaged at 850 eV at the Advanced Light Source at Lawrence Berkeley National Laboratory is shown in Fig. 15. The camera demonstrates no hot columns and shows good noise performance.

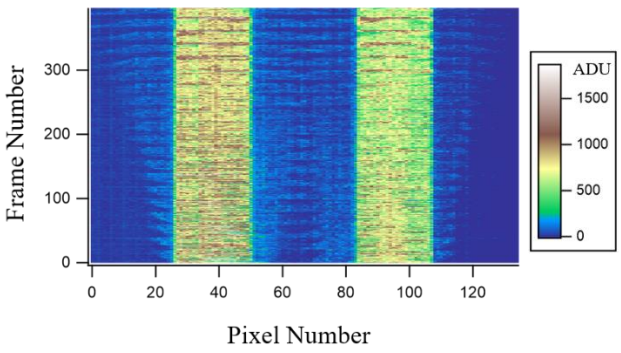

Fig.15. Ptychography test image at 850 eV. This is a projection of a slice through a ptychographic image stack. The image is banded because this is a projection of a toroid. The x-axis is the pixel number (position in 48 µm units) and each point on the y-axis is a slice through an image in the movie. The color scale is in ADC count units (ADU), with 6 ADU corresponding to one incident photon. This image was made using a 256 by 256 pixel CP-CCD that was read out in 256 µs by VASE. The variations between lines contain the information.

A Figure of Merit (FoM) for Analog-to-Digital Converters for image sensors (including the CDS function) is proposed in [21] that takes into account various relevant factors such as dynamic range, channel conversion time, power consumption, and area. The proposed FoM is

$$FoM = \frac{P \cdot ConvTime \cdot A}{10^{\frac{(DR_{dB}-1.76)}{10}}} \left[\frac{fJ \cdot \mu m^2}{conv.-step}\right]$$

where P is the per-channel power, ConvTime is the ADC conversion time (including extra functions like CDS), A is the area of the ADC and dB is the dynamic range of the channel (not simply the full-scale of the ADC). For VASE, the calculated FoM (including the power dissipation of the off-chip LSB ADC) is approximately 2.9 pJ · µm^2 / conv.-step, which compares favorably to other reported ADCs when extrapolated to the high pixel rate achieved with VASE.

The measured results of VASE are summarized in Table III.

TABLE III. MEASURED RESULTS

VASE Performance: 1.8 V and 25 °C		
	Value	Units
CMOS Technology	180	nm
Number of Channels	256	
Channel Pitch	48	µm
Maximum Pixel Rate	4	MHz
Equivalent Noise Charge (max gain)	22	e$^-$
Channel Gain (Maximum)	200	mV/fC
Maximum Input Signal	190	ke$^-$
Dynamic Range	78.7	dB
Crosstalk	-60	dB
Power Dissipation (per channel)	10.1	mW

VASE Performance: 1.8 V and 25 °C		
	Value	Units
Die Area	38.1	mm^2

V. CONCLUSION

A 256-channel CP-CCD readout ASIC called VASE is presented. VASE is pitch matched with the CP-CCD to allow direct wire bonding between the CP-CCD and VASE, lowering noise and reducing the physical size of the camera. The maximum channel rate is 4 MHz, corresponding to a frame rate of 32 kframes/sec when a 256 by 256 pixel sensor is read out on both sides. The use of an Extended Counting ADC with embedded CMS functionality partitions the ADC function between multiple chips allowing for system-level optimization. The readout ASIC achieves 22 e$^-$ ENC at 25 °C when configured for maximum gain (200 mV/fC) and a dynamic range of 78.7 dB.

VI. APPENDIX

In this appendix, Eq. (2) is derived. Assuming equal-valued input capacitors (i.e. we assume the modulator gain is 1 without loss of generality), the time-domain response of the modulator in Fig. 5 during one clock cycle is

$$V_o[n+1] = V_o[n] + \frac{V_i}{2} - \frac{V_{DAC}}{2} + V_{cm} \quad (9)$$

Here, $V_{DAC} = -\Delta V_{ref}$ when D = 0 and $V_{DAC} = \Delta V_{ref}$ when D = 1. Also, $\Delta V_{ref} = V_{ref}/2$. Therefore, $V_{DAC} = (2D-1)\Delta V_{ref}$.

Plugging this into the above we have,

$$V_o[n+1] = V_o[n] + \frac{V_i}{2} - \frac{(2D-1)}{2}\Delta V_{ref} + V_{cm} \quad (10)$$

Now,

$$V_o[M] = \sum_0^{M-1} V_o[n] = \frac{MV_i}{2} - \frac{M(2D-1)}{2}\Delta V_{ref} + V_{cm} \quad (11)$$

After M samples, the modulator is then switched from non-inverting to inverting and $V_o[M]$ becomes the initial condition for the inverting modulator so we have

$$V_o[2M] = \frac{1}{2}\left(MV_r + (M - D_R)\Delta V_{ref}\right) - \frac{1}{2}\left(MV_s + (M - D_S)\Delta V_{ref}\right) + V_{cm} \quad (12)$$

Here, V_r is the reset input from the CP-CCD (sampled when the modulator is in non-inverting mode) and V_s is the signal input from the CP-CCD (sampled when the modulator is in inverting mode). Simplifying, we have:

$$V_o[2M] = \frac{M}{2}\left((V_r - V_s)\right) + (M - D_F)\Delta V_{ref} + V_{cm} \quad (13)$$

where D_F is the sum of the digital outputs of the filter during both modes. This can be rearranged to solve for the input signal ($V_r - V_s$).

$$(v_r - v_s) = \frac{2(v_o - V_{cm} - (M - D_F)\Delta V_{ref})}{M} \quad (14)$$

The high-gain mode output is then:

$$V_o[2M] = \frac{GM}{2}\big((V_r - V_s)\big) + (M - D_F)\Delta V_{ref} + V_{cm} \quad (15)$$

Here, G is the ratio of the gain of the high-gain modulator to the low-gain modulator.

REFERENCES

[1] J. Janesick, *Scientific Charge Coupled Devices*, Bellingham, WA, SPIE-Press, 2001

[2] P. Denes, D. Doering, H. A. Padmore, J.-P. Walder, and J. Weizeorick, "A fast, direct x-ray detection charge-coupled device," *Rev. Sci. Instrum*. 80, 2009.

[3] R. J. Stover, M. Wei, D. K. Gilmore, S. E. Holland, D. E. Groom, W. W. Moses, S. Perlmutter, G. Goldhaber, C. R. Pennypacker, N. W. Wang, and N. Palaio, "High-Performance CCD on High-Resistivity Silicon," Proc. SPIE. 3505, 1998.

[4] Struder, L. et al., "Large-Format, high-speed, X-ray pnCCDs Combined with Electron and Ion Imaging Spectrometers in a Multipurpose Chamber for Experiments at 4th Generation Light Sources," Nucl. Instr. and Meth. A 614, 2010, pp. 483-496

[5] C. Damerell, "CCD-based Vertex Detectors," Nucl. Instr. and Meth. A 541, 2005, pp. 178-188

[6] J. Janesick, *Photon Transfer*, Bellingham, WA, SPIE-Press, 2007

[7] C. Jansson, "A High-Resolution, Compact, and Low-Power ADC Suitable for Array Implementation in Standard CMOS," *IEEE Trans. Circuits Syst.*, vol. 32, no. 11 pp. 904-912, Nov. 1995

[8] P. Rombouts, W. De Wilde, and L. Weyten, "A 13.5-b 1.2-V Micropower Extended Counting A/D Converter," *IEEE J. Solid-State Circuits*, vol. 36 no. 2, pp. 176–183, Feb. 2001.

[9] A.M. Fowler, and I. Gatley, "Demonstration of an Algorithm for Read-Noise Reduction in Infrared Arrays," *Astrophysical Journal Letters*, vol. 353, p. 33 April 1990

[10] S. Suh, S. Itoh, S. Aoyama, and S. Kawahito, "Column-Parallel Correlated Multiple Sampling Circuits for CMOS Image Sensors and Their Noise Reduction Effects," *Sensors*, vol. 10, no. 10, pp. 9139-9154, 2010

[11] N. Kawai and S. Kawahito, "Noise Analysis of High-Gain, Low-Noise Column Readout Circuits for CMOS Image Sensors," *IEEE. Trans. Electron Devices*, vol. 51, no. 2, pp. 185-194, Feb. 2002

[12] M-W. Seo, S-H. Suh, et al., "A Low-Noise High Intrascene Dynamic Range CMOS Image Sensor with a 13 to 19b Variable Resolution Column-Parallel Folding-Integration/Cyclic ADC," *IEEE J. Solid-State Circuits*, vol. 47, no. 1, pp. 272–283, Jan. 2012.

[13] R. Schreier, and G. Temes, *Understanding Delta-Sigma Modulators*, New York, Wiley 2004

[14] H. Spieler; *Semiconductor Detector Systems*, Oxford, Oxford University Press, 2005

[15] J.D. Jackson, *Classical Electrodynamics*, New York: Wiley, 1998

[16] D.M. Monticelli, "A Quad CMOS Single-Supply Op Amp with Rail-to-Rail Output Swing," *IEEE J. Solid-State Circuits*, vol. 21, no. 6, pp. 1026–1034, Dec. 1986.

[17] R.J. Baker, *CMOS Circuit Design, Layout, and Simulation*, New York: Wiley-IEEE Press, 2010

[18] A. Boni, A. Pierazzi, and D. Vecchi, "LVDS I/O Interface for Gb/s-per-pin Operation in 0.35-µm CMOS," *IEEE J. Solid-State Circuits*, vol. 36, no. 4, pp. 706–711, April 2001.

[19] T.H. Lee, *The Design of Radio Frequency Integrated Circuits*, New York: Cambridge University Press, 2003

[20] M. Burns and G.W. Roberts, *An Introduction to Mixed-Signal IC Test and Measurement*, New York: Oxford University Press, 2001

[21] M. Kwon and B. Murmann, "A New Figure of Merit Equation for Analog-to-Digital Converters in CMOS Image Sensors", *Proc. Int. Symp. Circuits Syst.*, Florence, Italy, 2018