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Fabrication and Characterization of Silicon Microwire Neural Electrode Arrays on
Flexible Substrates

A Thesis submitted in partial satisfaction of the requirements for the degree of
Master of Science

in

Electrical and Computer Engineering

by

Farid Azzazy

Committee in charge:

      Professor Shadi Dayeh, Chair
      Professor Gert Cauwenberghs
      Professor Vikash Gilja

2014

The Thesis of Farid Azzazy is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

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<div align="right">Chair</div>

University of California, San Diego

2014

DEDICATION

I would like to dedicate this thesis to science.

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ABSTRACT OF THE THESIS

Fabrication and Characterization of Silicon Microwire Neural Electrode Arrays on
Flexible Substrates

by

Farid Azzazy

Master of Science in Electrical and Computer Engineering

University of California San Diego, 2014

Professor Shadi Dayeh, Chair

Neuroprosthetic devices are widely employed in clinical and research settings. However, most of these devices suffer from diminishing device performance over time, likely due to the reactive tissue response of the central nervous system and scarring to biological tissue from the implantation procedure. In an effort to minimize acute tissue trauma while maintaining high spatial resolution, this thesis presents a novel miniaturized neural implant device capable of recording high-density neural signals from cortical tissue with penetrating silicon microwire sensing elements on a flexible conformable substrate.

In addition to reduced tissue scarring, it is possible to improve on current commercially available neural probe designs by reducing the mechanical property mismatch between the electrode interface and neural tissue. Neural electrodes fabricated on flexible substrates have received an increase in attention in recent years; however, these designs offer moderate spatial resolution because signals are typically recorded from the surface of neural tissue in thin film style electrode designs.

The MEA presented in this thesis is fabricated by a hybrid integration technology that takes advantage of both rigid penetrating pillars, similar yet smaller than commercially available technology, and is fabricated on thin film polyimide substrates. The thin film polyimide substrate allows for the electrode to make intimate contact with surrounding cortical tissue around sulci and gyri of the brain, and the silicon microwire sensing elements, which penetrate into the

cortex, enable this MEA to have the potential for the best spatial resolution. The impedance of these MEAs was characterized and found to be in the range of a few hundred kilohms making them suitable for both local field potentials and single unit recordings.

Chapter 1: Introduction

Neuroscientists have long been interested in recording and stimulating various regions of the brain to better understand neural connectivity and decrypt the signal transport of neuronal tissue. Recent advances in neurotechnology have allowed for higher spatiotemporal resolution[1] of recording and stimulating multi-electrode arrays (MEA's) allowing for breakthroughs in brain mapping, diagnosing neurological disease, and controlling prosthetic devices.[2]

Various electrode arrays are currently used in achieving said goals, including electroencephalography (EEG),[3] electrocorticography (ECoG),[4] Utah electrodes,[5] Neuronexus probes developed at the University of Michigan,[6] as well as various other novel technologies currently being researched [7,8]. These various technologies have different degrees of invasiveness and spatial resolution, and depending on the specific application, can be used to collect various types of brain signals.

1.1 Current Technology

Perhaps the least invasive neural recording modality is the EEG electrode. EEG electrodes are advantageous due to their ability to collect signals from the scalp; however, they suffer from poor spatial resolution and are limited in their ability to determine neural activity below the topmost layers of the brain. While EEG may be one of the oldest[9] and widely used methods for observing brain

activity, firing patterns of individual neurons cannot be discriminated from EEG data.[10] Even though high-density recording cannot be collected with EEG electrodes, they have been a key element in diagnosing and treating epilepsy patients due to their ease of use and ability to localize epileptic zones.[11]
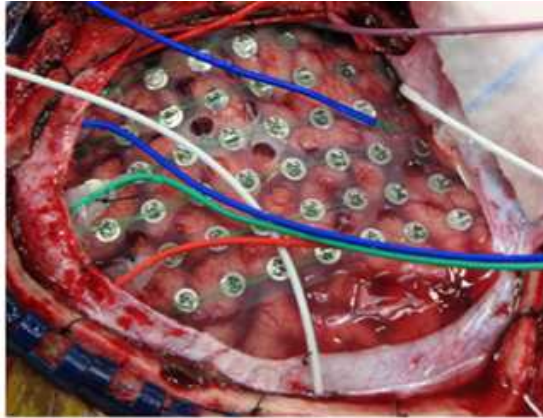
Figure 1.1: An ECoG electrode implanted on a human brain's surface [14]

ECoG electrodes have a much greater spatial resolution than EEG electrodes, though they are much more invasive because they record directly from the surface of the cortex. This greatly enhances the fidelity of the recorded signal because the skull and intermediary tissue no longer stand between the electrode and brain, thus providing access to non-attenuated signals and higher signal-to-noise ratios. Furthermore, ECoG electrodes can be fabricated with thin film technology to achieve intimate contact with the gyri and sulci of the brain. When designed with thin plastic substrates such as polyimide under about 10 µm, the thin film can be flexible enough to conform intimately to the surrounding tissue.[12] ECoG electrodes typically involve the recording of local field potentials

from groups of neurons and cannot resolve single unit activity due to their large electrode pitch, which is usually on the order of about 1 cm.[13]

Penetrating microelectrode array designs, such as Utah electrodes and Michigan probes, are capable of much greater spatial resolution than EEG or ECoG by penetrating into the cortical tissue vs. recording and stimulating from the surface of the brain tissue. However, these electrodes suffer from a large mechanical mismatch with surrounding tissue due to them being fabricated from rigid materials such as silicon. Devices such as these have received significant attention in recent years because of their ability to discriminate single unit activity as well as local field potentials.[15]
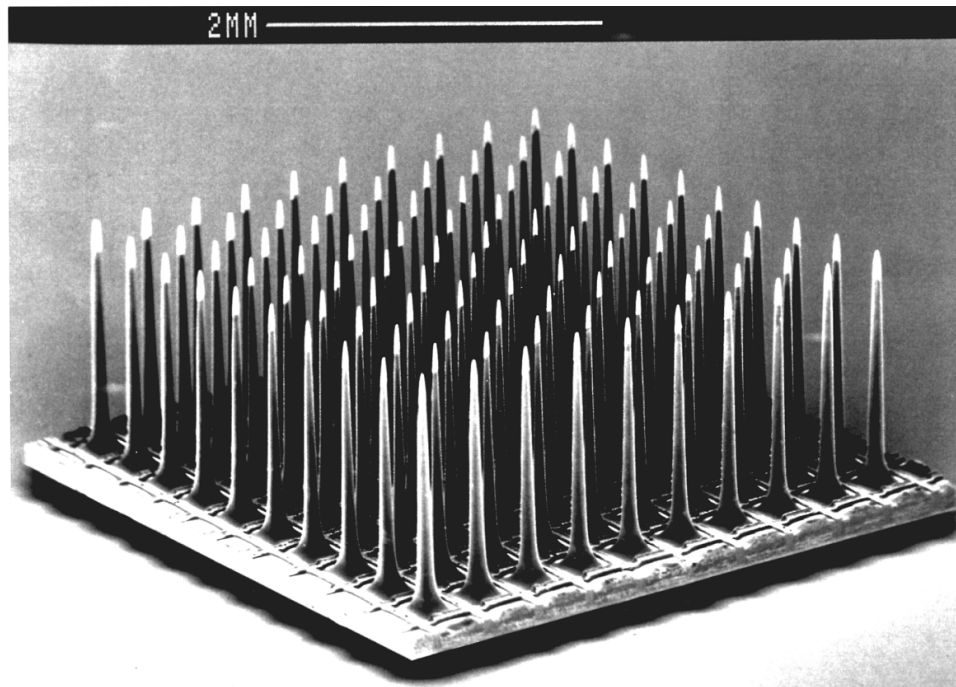
Figure 1.2: A 10x10 array of the Utah microelectrode[16]
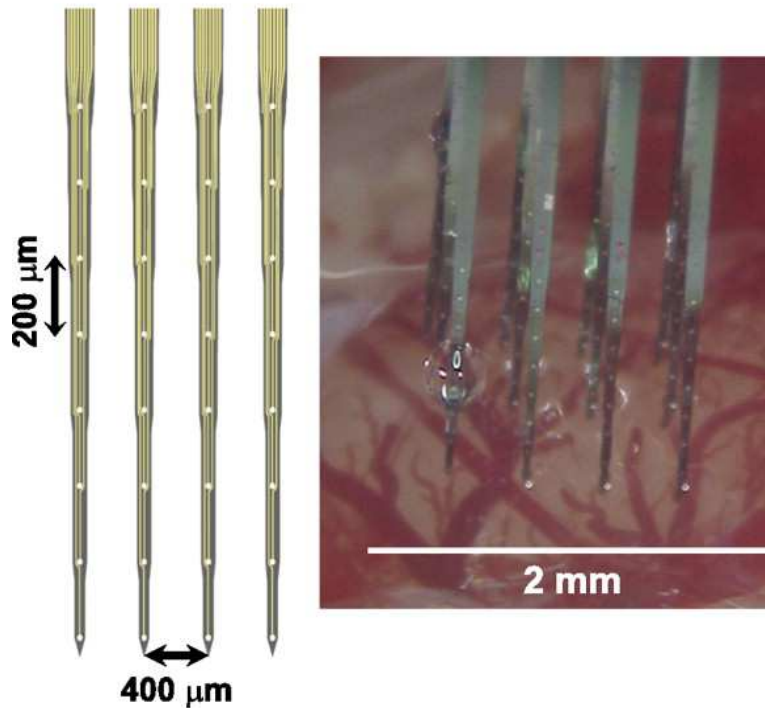
Figure 1.3: An array of four custom Neuronexus (Michigan style probes) microelectrodes inserted into a Wistar rat [17]

The mechanical property mismatch between neural tissue and rigid probes is great, which in turn causes tissue damage around the penetration site and elicits a neural response to the foreign body.[18] The mechanical property mismatch can be reduced when flexible probes are used, but implantation procedure becomes difficult if the electrode is too flaccid. Novel technologies, such as parylene based neural probes developed at the University of Southern California,[7] are flexible enough to have similar mechanical properties as cortical tissue, however spatial resolution on these devices is not optimal. Fabrication of

these devices often involves manual processing steps making this process difficult to scale into large-scale manufacturing.

1.2 Motivation

While efforts have been made to make microelectrode devices more flexible,[19,20] these devices often times have few recording sites or are not thin enough to conform intimately to the surface of the brain. Additionally, these devices focus mainly on improved flexibility of the microelectrode design, and do not address improvements in spatial resolution which is necessary for understanding collective neural activity and for achieving higher resolution in prosthetic implants.
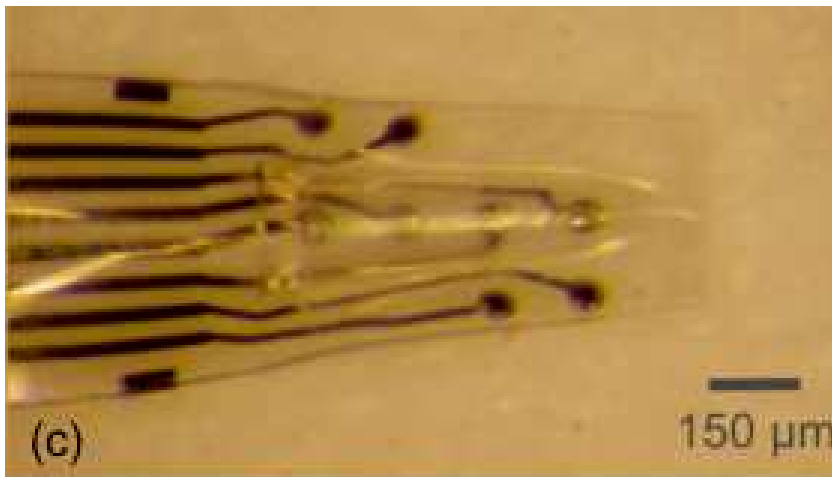
Figure 1.4 Flexible parylene sheath neural electrode [7]

It is then of great interest to develop a thin film neural recording modality that can conform to the surface of cortical tissue while at the same time penetrate into the cortical column but such devices have not been utilized prior to this work.

Fabricating such devices is challenging because penetrating pillar like structures must be heterogeneously integrated onto thin film plastic substrates and are required to be integrated with metallic electrode leads at high spatial resolution. It is of further interest for such a device to be designed with CMOS compatible processing so that fabrication can be transitioned for large scale commercial manufacturing.

Presented in this thesis is a manufacturing method and impedance characterization of a novel neural probe design. The MEA presented here utilizes penetrating microwires and is fabricated on an ultrathin polyimide substrate in a CMOS compatible process where silicon microwires are used as the sensing element. This design heterogeneously integrates silicon microwires onto the polyimide substrate in an etch-back process. The novelty of the design has led to the filing of a provisional patent disclosure through UCSD's tech transfer office. Additionally, the spatial resolution of the presented design has electrode spacing's of about one order of magnitude less than commercially available Utah or Neuronexus probes.

1.3 Thesis Outline

The outline of the thesis is as follows:

Chapter 2 gives an overview of the design consideration and fabrication steps involved in producing neural probes on flexible substrates. Design

considerations including etch back processing, double side alignments, electrode lead passivation, metal coating of microwires, and wafer bonding are discussed.

Chapter 3 reviews basic electrochemical impedance spectroscopy (EIS). EIS results of the neural probes are shown in this chapter as well and optimization of probe impedance to meet single unit recording requirements.

Chapter 4 gives a summary of the thesis, possible improvements of the design, and an outlook of the research.

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Chapter 2: Silicon microwires on flexible substrates; design and fabrication

2.1: Introduction

Fabricating silicon wires on flexible substrates poses many challenges. Commonly used microfabrication techniques such as dry etching, annealing, and photolithography are extremely difficult to perform when thin plastic substrates are used, such as polyimide, due to chemical and thermal stability. Furthermore, the mechanical stability of flexible substrates with thicknesses that are less than ten micrometers poses further challenges making simple fabrication techniques such as photolithography or dry etching difficult. Penetrating microwires must also be properly aligned onto thin film substrates; however, performing photolithography with pillar structures already defined can be challenging as well. Various microfabrication techniques heterogeneously integrated into a unique process flow are discussed in this chapter.
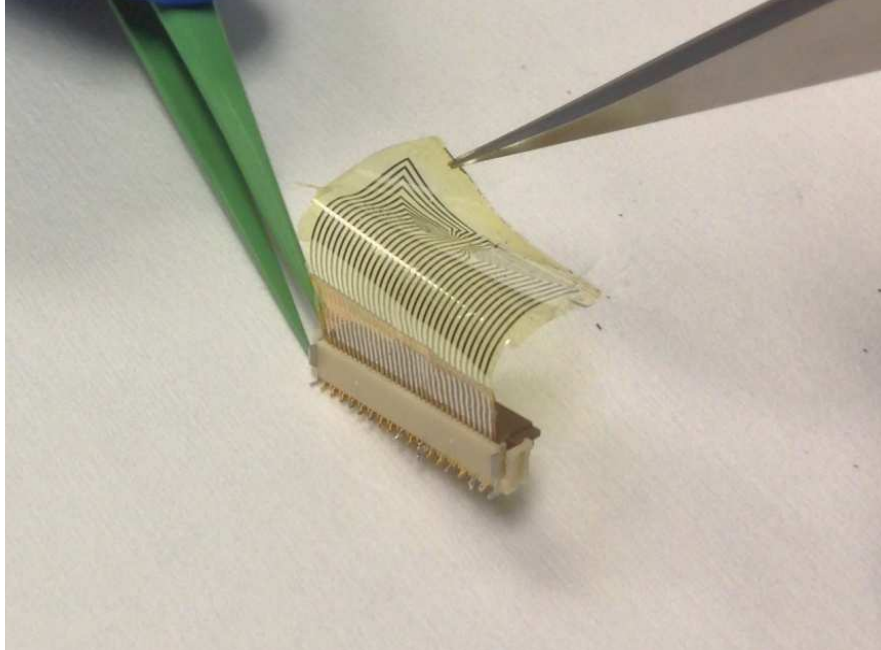
Figure 2.1: A completed device with square packed arrays flexed with tweezers connected to a zero insertion force clipper

2.2: Design Considerations

Numerous design elements must be considered in fabricating such a device. The design presented in this thesis is fabricated in a unique process flow with several processing steps that differentiate it from previous works; namely, a double side aligned, etch back process in which silicon pillars are dry etched onto a pre-patterned polyimide substrate in a monolithic integration approach. This is the first design that utilizes a double side aligned process for defining silicon microwires onto flexible substrates. Additionally, this process allows one to further scale down the dimension and spacing of the silicon microwires. The process flow discussed in the following sections was used to fabricate MEA's

with linearly spaced arrays and square packed arrays. Center-to-center spacing as low as 25 µm between silicon microwires was successfully implemented in the square packed array design. Silicon microwire pitch as high as 8:1 was successfully implemented in an electrochemically functional device as well.

The multiple electrode array presented in this thesis comprises a thin flexible substrate with encapsulated metal leads and silicon microwires coated with platinum. Metal is exposed in two regions of the substrate: at the edge of the electrode where a commercially available zero insertion force clip is used as an adapter to connect to measurement devices such as electrochemistry impedance and neurophysiology equipment, and at the base of the silicon microwires to allow electrical access between the metal leads, microwire sensing element, and zero insertion force clip. The silicon microwires are coated in metal to reduce electrochemical impedance in solution.

Electrode leads must be either passivated or encapsulated in a manner that isolates the metal lines from being in electrical contact with brain tissue. This can be achieved by depositing an insulating film such as SiO_2 or SiN on the device surface late in the process flow, after microwires are defined.[1] While this method may be effective in some designs, depositing a thin film of oxide or nitride will cause mechanical stress on the flexible substrate, which may cause the substrate to curl or buckle. The final device thickness of the MEA is so thin that even small amounts of tension or compression can be significant; therefore, oxide or nitride passivation films were avoided.

Access vias are instead patterned into the passivation layer early in the process, granting electrical access to the silicon wafer through the backside of the device. The passivation layer is made of polyimide, the same material as the flexible substrate, thus minimizing the mechanical stress mismatch between differing materials.

The use of plastic substrates such as polyimide further constrains processing implementations. Flexible plastic substrates cannot be annealed at high temperatures, prohibiting solid state bonding and CVD growth of silicon microwires. Furthermore, there exists a thermal coefficient mismatch between silicon and polyimide. As an alternative, low temperature adhesive bonding techniques utilizing spin-on polymers such as photoresist or polyimide are used instead of solid-state bonding. Microwires are not grown in the presented MEA, but are rather etched back onto pre-patterned flexible substrates. Additionally, polyimide is not etch-selective to strong acids, so aggressive cleaning solutions such as piranha or RCA must be used before the polyimide substrate is spun coat onto the device. Moreover, wet etching is limited to weak acids so dry etching must be implemented in a majority of the processes.

The materials chosen for metal lines must be selected carefully as well. Metals that make a good ohmic contact to silicon must be used as the seeding layer; however, metals must also have good etch selectivity because the surface of some metal will be exposed later in the processing during silicon microwire

etching and could be attacked risking electrical discontinuity between the silicon microwires and connection pads.
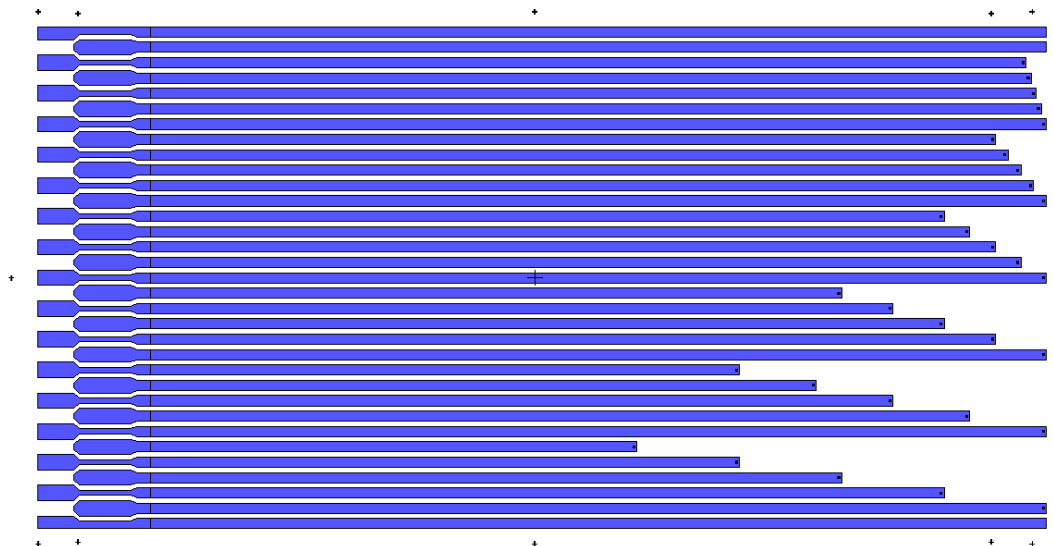
Figure 2.2: Mask design showing a schematic of linearly spaced electrodes. The mask is designed to have 6 arrays with varying electrode spacing (100 µm – 1500 µm)
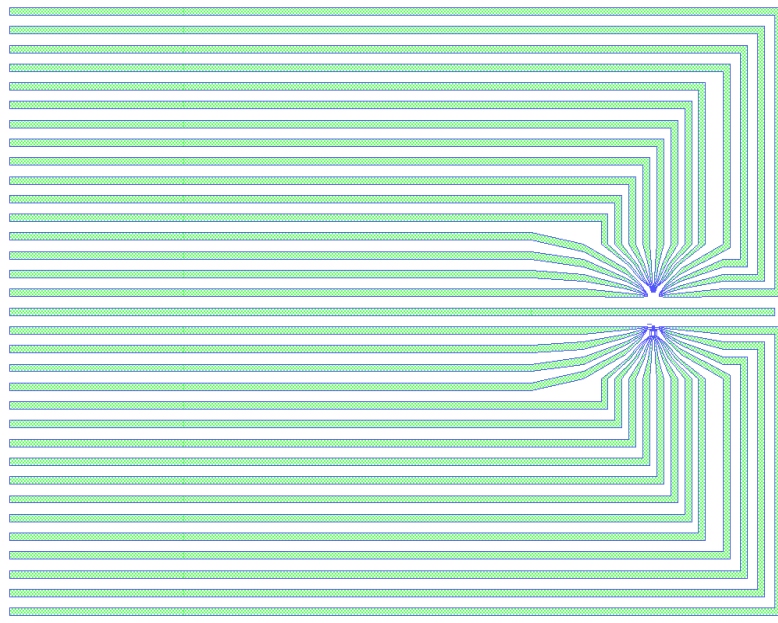
Figure 2.3: Mask design schematic of square packed electrodes. The mask is designed to have two 4X4 arrays. Top array have 20 µm wide access vias and 50 µm pillar-to pillar spacing while lower array has 17 µm wide access vias and 25 µm pillar-to-pillar spacing

Two distinct design implementations were fabricated using this unique process flow, linearly spaced arrays and square packed arrays, demonstrating the adaptability of this fabrication method. Although only two geometries were fabricated using this method, various layouts can be easily manipulated for a variety of applications that require different shapes and dimensions.

2.3: Process Flow

The process flow is summarized in the following two figures. The subsequent chapters provide a more in depth analysis of key processing steps.

A) Fabrication begins with a clean <111> silicon substrate

B) Two spin coats of PI-2610 are applied

C) 20 nm of sacrificial titanium is deposited by electron beam deposition

D) Access vias are patterned into the titanium film by photolithography and dry etched in Ar/SF$_6$ plasma

E) The exposed polyimide is dry etched in O$_2$ plasma

Figure 2.4: Process Flow demonstrating steps of the fabrication process

F) The sacrificial titanium is removed in HF

G) Electrode lines are patterned by photolithography and a 20/80 nm titanium/nickel stack is deposited by electron beam deposition

H) Before the photoresist is lifted off, 300 nm of titanium is sputtered completing the electrode lines

I) The device is flipped and a 500 nm nickel etch mask is double side aligned to the top side of the device

Figure 2.4: Process flow, continued

J) The metal lines are then encapsulated with four spin coats of PI-2610, completing the flexible substrate

K) The device is adhesively bonded to a carrier wafer using NR9-6000 photoresist

L) Silicon microwires are dry etched in SF_6/C_4F_8 plasma

Figure 2.4: Process flow, continued

M) PMMA is spun coat onto the device surface, and 50 nm platinum is sputtered to coat the microwires

N) The deice is soaked in acetone releasing it from the carrier wafer and lifting off the PMMA layer

Figure 2.4: Process flow, continued

2.4: Lead passivation

Fabrication of the MEA begins with a clean <111> silicon substrate. Commonly used cleaning solutions such as piranha followed an HF dip are appropriate for cleaning the Si substrate and are used here. Ultimately, the height of the silicon microwires is determined by the initial thickness of the silicon wafer being used, which is optimally about 70-100 µm. When the starting thickness of the silicon substrate is too thick, etching back silicon microwires

becomes more difficult. Longer etch times result in less repeatability between etching runs, and the etch mask must be made thicker to resist the long exposure to the plasma etchant. When silicon substrates are too thin, devices break easily during fabrication and the yield becomes quite low.

The silicon substrate will eventually be etched back in later processing steps onto a pre-patterned flexible substrate; therefore, fabrication begins with patterning access vias on the backside of the substrate. Passivating electrode leads towards the end of the device fabrication is difficult due to the presence of freestanding silicon microwires; therefore passivating leads early in the process flow is preferred.

Once the Si wafer is cleaned, polyimide is spun-coat on the backside of the silicon wafer, which will serve as the passivation layer. In the present design, PI-2610 manufactured by HD Microsystems is used throughout the fabrication process. PI-2610 is baked at 170℃ for five minutes on a hot plate, and then cured at 300℃ for thirty minutes in a furnace. One spin coat of PI-2610 is about 2.5 microns after curing, and multiple spin coats can be applied to achieve the desired passivation layer thickness. Two spin coats of PI-2610 are used as the passivation layer resulting in a PI thickness of about 5 microns. The passivation layer accounts for about one third of the ultimate thin film flexible substrate thickness.

Access vias are then etched into the polyimide layer revealing the Si substrate. This is achieved in multiple processing steps. First, a thin sacrificial Ti

layer of about 20 nm is deposited on top of the polyimide by electron beam deposition, shown in figure 2.4c.

Photolithography is then performed to pattern access vias on the Ti surface. The sacrificial Ti is selectively etched in Ar/SF_6 based plasma to open access to the PI passivation layer below. O_2 plasma is then used to selectively etch the uncovered PI and photoresist thus exposing Si in predefined regions, shown in 2.4d-e.

With the access vias patterned into the PI film, an HF dip is used to etch away the sacrificial Ti layer leaving access vias patterned into the PI passivation layer, shown in figure 2.4f. This enables electrical connectivity to predefined regions of silicon in later metallization steps, while the rest of the metal line is passivated by polyimide.

2.5: Metallization

The metal lines of the MEA comprise a metal stack of titanium and nickel. Photolithography is first used to pattern the electrode lines followed by an HF dip to remove native oxide from the exposed silicon regions. A 20 nm titanium layer followed by 80 nm of nickel are deposited by electron beam deposition onto the patterned passivation layer shown in figure 2.4g.

300 nm of titanium is then sputtered to complete metallization, shown in figure 2.4h. It is necessary to sandwich 80 nm of nickel in between the titanium layers because titanium will be attacked later in the process flow by SF_6 plasma

during the silicon microwire etching process. The 80 nm nickel layer protects the sputtered Ti layer beneath it. The 20 nm titanium layer is used as the seeding layer because it creates a more ohmic contact with n-type silicon than nickel. Sputtering is used instead of electron beam deposition so that titanium is deposited on the sidewalls of the passivation layer, ensuring an electrical connection between the discontinuous metal layers on the surface of the Si substrate at the bottom of the via and on the surface of the polyimide layer.

2.6: Double side alignment

Once metal lines are patterned on the backside of the die, a double side photolithography is performed on the top-side of the device to define an etch mask. The double side alignment process allows one to align and expose patterns on the top-side of the substrate to alignment markers or features on the bottom-side, shown in figure 2.4i. 500 nm of Ni is then deposited and lifted off on the top-side of the die. This nickel etch mask is used later in the process flow for etching silicon microwires.

A double side photolithography alignment is an essential step in the processing. Silicon wires are eventually etched back onto the pre-patterned flexible substrate; therefore, a precise double side alignment is crucial because misaligned silicon microwires will act like an open circuit due to the polyimide passivation. Furthermore, the double sided alignment of the silicon microwire etch mask allows for the patterning and passivation of electrode leads prior to defining 3D structures on the MEA. This allows one to do most of the

photolithography and metal deposition as well as passivation before etching the delicate silicon microwires.

The current design was implemented with two different types of layouts, linearly spaced arrays and square packed arrays. The accuracy of the double side alignment was greatly improved when square packed arrays were implemented because the alignment of the etch mask was less sensitive to rotation misalignments. Furthermore, higher density silicon microwires could be defined in 4x4 arrays rather than linearly spaced arrays with spacing's as low as 25 μm being successfully implemented.

2.7: Wafer Bonding

The next step in the microfabrication process involves encapsulating the metal leads and bonding the die to a temporary carrier wafer, shown in figure 2.4j-k. After etching the silicon microwires, the electrode will consist of freestanding silicon microwires on a thin flexible substrate. Handling the thin electrode array is quite difficult because the polyimide substrate flexes and bends quite easily. The temporary carrier wafer allows one to more easily handle the electrode in the final processing steps before completing device fabrication. It is also necessary to encapsulate the leads before etching the silicon microwires because processing on the back-side of the device must be completed before defining the pillar structures.

Two different materials were studied as intermediary adhesive bonding materials, polyimide and photoresist. Because the carrier wafer is bonding directly to the backside of the flexible substrate, polyimide was the first material to be investigated as an intermediary adhesive bonding layer. Air bubbles and poor bond strength associated with polyimide bonding led to investigations of other bonding materials. Ultimately, photoresist was chosen as the adhesive bonding material between the carrier wafer and the device.

In the initial experiments, PI-2610 was utilized as the adhesive bonding layer between the carrier wafer and device. First, metal leads were encapsulated with two spin coats of PI-2610 and soft baled at 170^0 for five minutes. One spin coat of PI-2610 was applied to a Si/SiO_2 carrier wafer, and an additional spin coat of PI-2610 was applied to the backside of the device. The two substrates were brought into contact before the polyimide was soft baked. With the two wafers in contact, pressure was manually applied with tweezers on a hot plate at 170^0 for five minutes and then cured at 300^0 C for thirty minutes, concluding the wafer bonding process. The device was lifted off from the carrier by soaking in dilute HF solution for several hours; thus removing the SiO_2 layer, which released the carrier wafer from the device. This process is shown below in figure 2.5a-c.

A) The metal lines are then encapsulated with two spin coats of PI-2610 and soft baked

B) A third spin coat of PI-2610 is applied to the device, and a single spin coat is applied to the carrier wafer

C) The two substrates are brought into contact, and soft baked on a heat plate at 170° under pressure
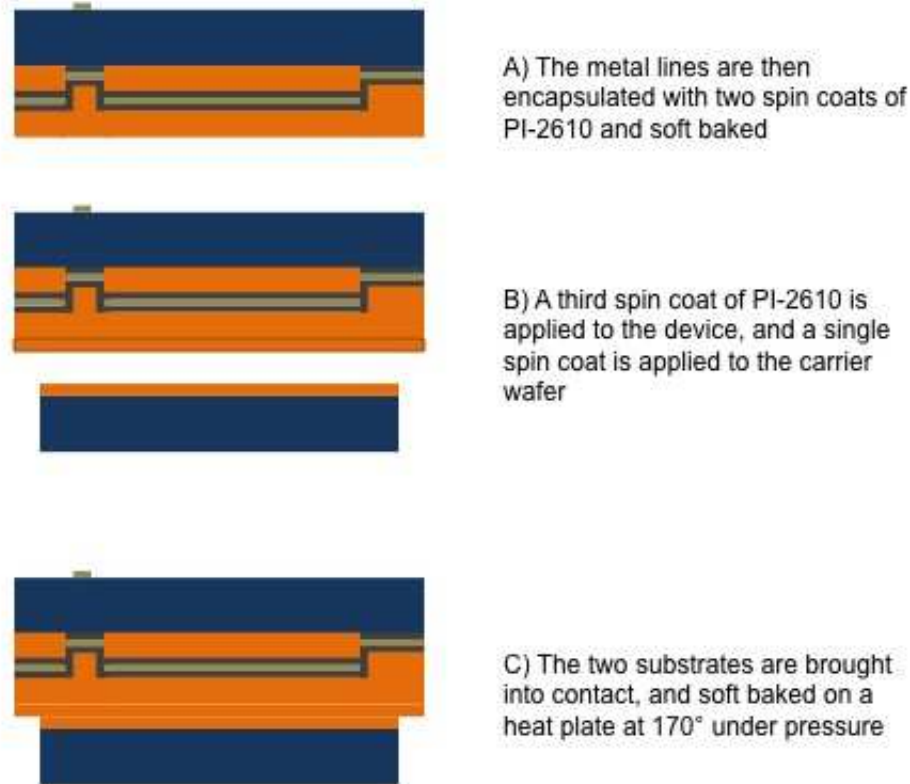
Figure 2.5: Process flow demonstrating the polyimide bonding method

After etching back the silicon microwires, several problems with this bonding method could be observed. Many tiny air pockets would form between the polyimide bonding layers. Additionally, large air pockets would bubble causing discontinuities in the flexible substrate. This was likely due to out-gassing during the soft bake at 170^0. Similar results utilizing PI-2610 as an adhesive bonding candidate were found to be in agreement with these findings.[2]

While the devices utilizing this bonding method were functional, the process could still be further optimized. In an effort to minimize outgassing issues, other intermediary bonding candidates were investigated.

Polyimide-2610 is resistant to weak acids and commonly used solvents such as IPA and acetone; however, due to the poor bonding results, photoresist NR9 was investigated. Photoresist is not as chemically resistant as polyimide, but initial bonding results showed photoresist as a superior bonding candidate over PI-2610. Intimate contact between the carrier wafer and device could be achieved using a similar bonding technique.

With this technique, four spin coats of PI-2610 were applied to the backside of the device to encapsulate the metal leads, soft baked at 170° for five minutes, and cured at 300° for thirty minutes in a furnace. One spin coat of NR9-6000 photoresist was applied to the carrier wafer, and the device and carrier were brought into contact and subsequently soft baked at 150° on a hot plate with pressure applied with tweezers.

Little to no out-gassing was observed when using NR9 photoresist and the intermediary adhesive layer. Smooth continuous films of polyimide were observed following the silicon microwire etch. Although the adhesive bond formed by the photoresist perhaps does not exhibit the most resistive bond, adhesion between the device and the carrier was sufficient to carry out the rest of the processing steps in the electrode fabrication.

2.8: Etch back processing

The next phase in the device fabrication is dry etching the silicon microwires. SF_6/C_4F_8 based RIE/ICP plasma was used to etch through the silicon substrate, shown in figure 2.4l. Optimal results were found when the silicon microwires were etched slowly with low powered plasmas, with etching rates of about 300 nm/min. Increasing the etch rate of the process causes poor pillar morphology, with often times unrepeatable results. It was found that increasing the etch rate causes a less anisotropic etch, with silicon microwires often time being attacked from the sides of the wires.

During the dry etch, the nickel etch mask does get attacked by the SF_6 plasma. The nickel is resistant to the etch plasma for about an hour and a half etching before nickel starts getting attacked, and is completely removed after about three hours of exposure to the SF_6/C_4F_8 plasma. While it is important for the etch mask to resist the ICP plasma for several hours during the etching process, it can be advantageous if nickel is slightly consumed during this process. This allows for silicon microwires forming into points at the wire tips, which is preferred when the electrode is to be used as an implant.

Towards the end of the microwire etching, small portions of exposed titanium are attacked by the SF_6. The dimensions of the nickel etch mask are smaller than the access vias causing the exposed titanium to be attacked. This would normally cause the device to be open circuited but the sandwiched nickel layer protects the underlying titanium.

It is preferable for the silicon microwires to have a reverse taper, or be pointier at the tip and wider at the base. Unfortunately, it is difficult to achieve this result with the current process flow and the silicon wires do have a slight taper at the base. Square patterns are defined when the etch mask is patterned; however by the time the silicon is fully etched back, microwires take on a more circular shape.
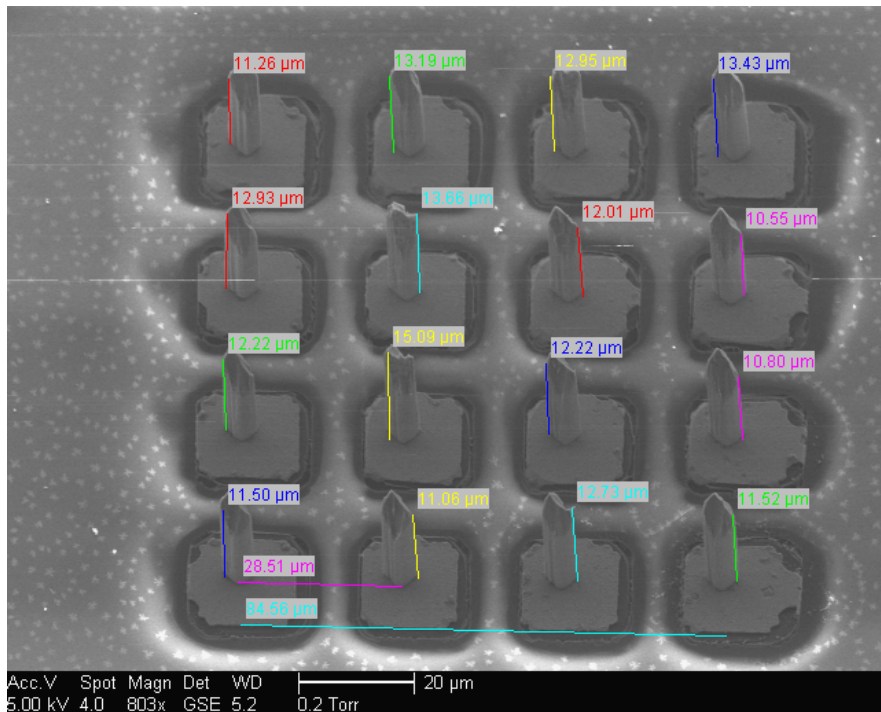

Figure 2.6: (Top) Tilted-view scanning electron microscope etch results of 4x4 square packed arrays of silicon microwires showing pointed microwire tips. SEM micrographs were taken at a 45⁰ angle. (Bottom) Zoom in view of SEM micrograph.
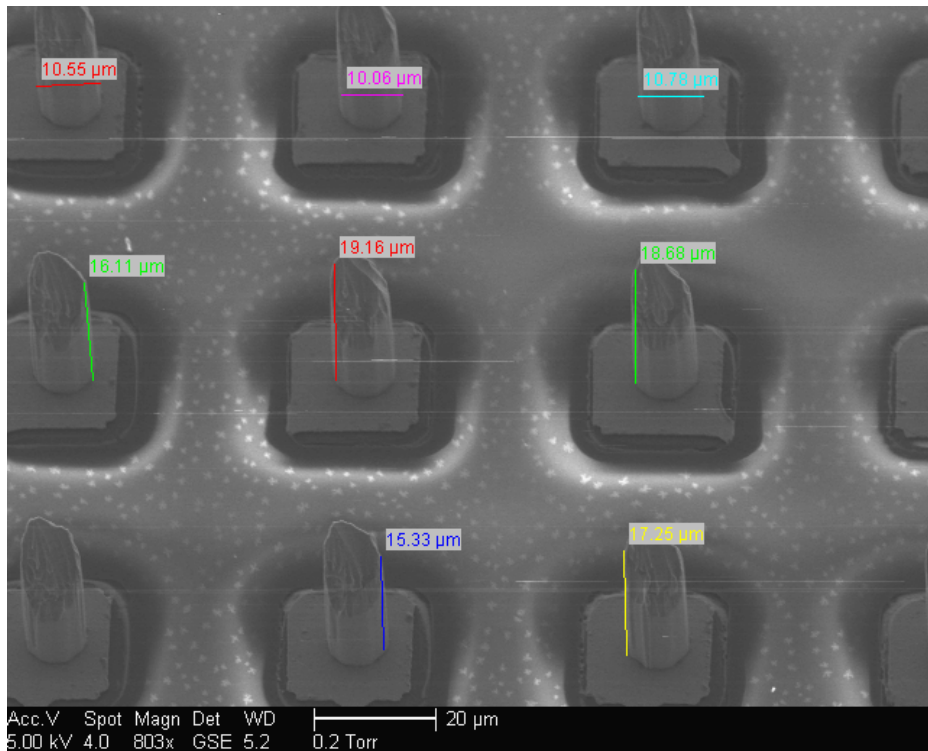
Figure 2.6: SEM micrographs, continued

The etch back process can be scaled down to smaller dimensions as well. While there are some constraints to the limit that the silicon microwires of actual devices can be scaled down to, the following SEM micrograph demonstrates that pillars of pitch greater than 8:1 with pillar diameter less than three microns can be achieved. This result suggests the silicon microwire etching will not constrain scaling the device down further.
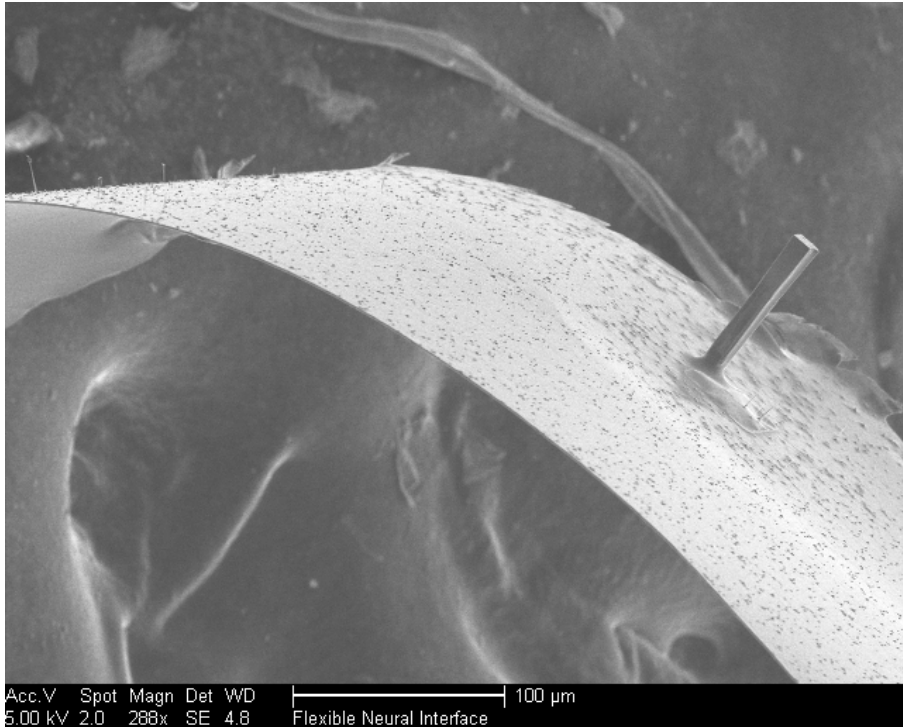
Figure 2.7: SEM image of a single electrode lead cut out from a linearly spaced array of electrodes

2.9: Metal coating of silicon microwires

The final step in device fabrication is coating the silicon microwires with metal. The metal coating of the silicon wires ensures low electrochemical impedance in solution, which will be discussed further in the next chapter.

At this point in the device fabrication, the electrodes are quite delicate because of the free-standing silicon microwires, making metal deposition difficult. A sacrificial PMMA A series resist was first applied to the surface of the device, exposing only the silicon microwires. Various metal deposition techniques were attempted, some with limited success, and were later lifted off in acetone. The

acetone soak also separated the finalized thin flexible device from the temporary carrier substrate and suspended it in solution, shown in figure 2.4m-n.

At first, electron beam deposition was used to deposit a metal film on one-side of the silicon microwires. Electron beam deposition is directional, so to achieve microwire sidewall coating, the device was loaded in the electron beam deposition chamber at an angle, shown in figure 2.8 below. Depositing metal by electron beam deposition often times led to difficulty lifting off the PMMA layer and results were difficult to repeat. EIS characterization of devices with this method of microwire coating resulted in shorts between different electrode leads.
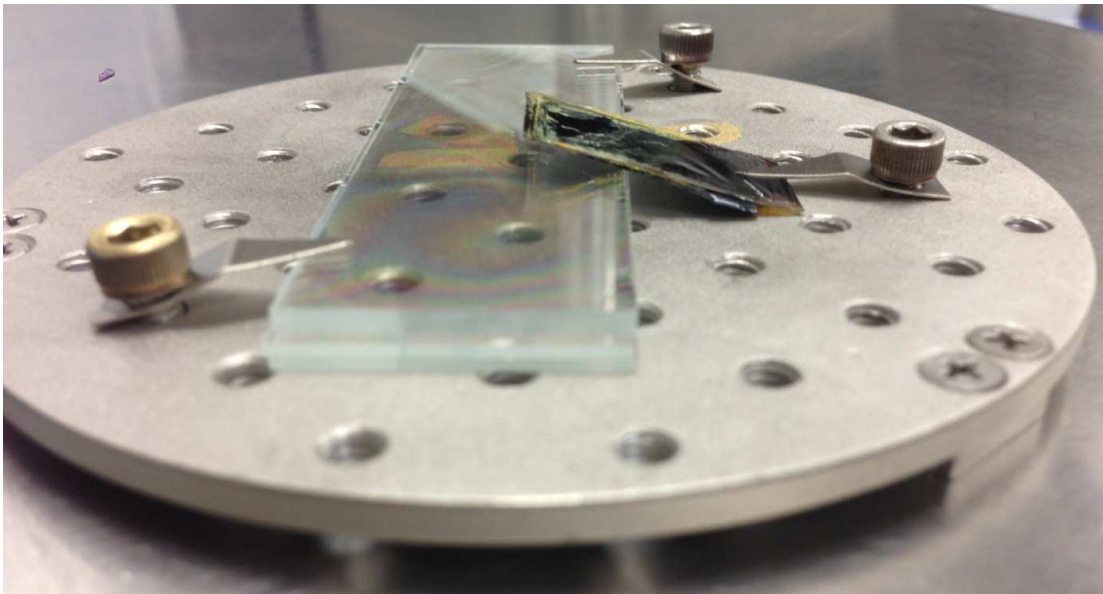

Figure 2.8: Device loaded onto electron beam deposition chuck at an angle, to achieve microwire sidewall metal coating

Ultimately, a sputter deposition was used to deposit 50 nm of platinum onto the microwire sidewalls. This method of coating metal onto the microwires resulted in the lowest impedance of devices.
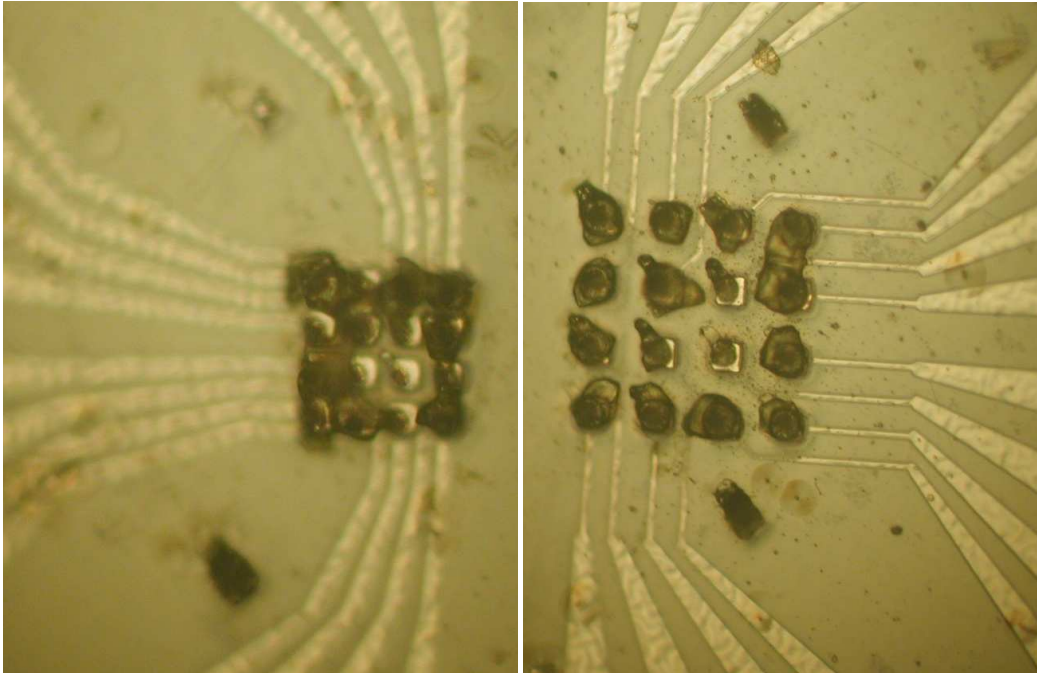

Figure 2.9: Optical micrograph of a completed device. Densely packed arrays with 25 µm pitch (left) and 50 µm pitch (right)

Sources

[1] Akifumi Fujishiro, Hidekazu Kaneko, Takahiro Kawashima, Makoto Ishida & Takeshi Kawano, In vivo neuronal action potential recordings via three-dimensional microscale needle-electrode arrays, Scientific Reports, 4:4868

[2] Frank Niklaus, Peter Enoksson, Edvard Kälvesten and Göran Stemme, Low temperature full wafer adhesive bonding, Journal of micromechanics and microengineering, Vol 11, No 2

Chapter 3: Electrochemical impedance spectroscopy theory and characterization

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3.1: Electrochemical impedance spectroscopy theory

It is often of interest to study the electrical behavior of electrodes in solution. This type of study enables one to analyze the impedance of the electrode in an environment similar to that in tissue for in vivo implants. The impedance of the electrode will ultimately determine the types of neural signals that can be recorded by the electrode. AC signal excitation in solution over a wide range of frequencies gives a complete characterization of the electrodes' impedance.

An interface is formed when the electrode and physiological medium come into contact with each other, where a combination of charge transport processes may occur. These charge transport processes can be either reversible non-Faradaic processes where no electrons are injected into the electrolyte solution and charged species are merely redistributed, or non-reversible Faradaic processes where electrons are injected into the solution by a redox reaction.[1]
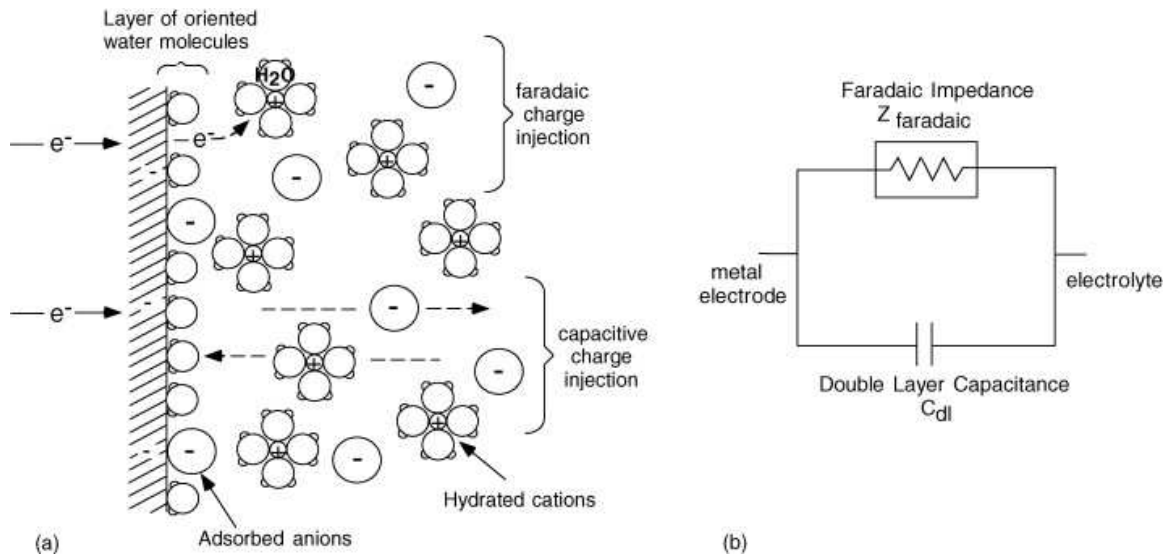
Figure 3.1: Illustration showing Faradaic processes (top-left) and non-Faradaic processes (bottom-left) at the electrode electrolyte interface, and a two-element equivalent circuit model of charge transfer mechanisms.[1]

When the electrode and electrolyte are at different potentials, a double layer of charge forms at the interface, known as the double layer capacitance. This capacitance tends to dominate the overall device impedance at lower frequencies where the mass transport regime is dominant. Impedance due to the double layer capacitance can be greatly reduced when porous electrode coatings are used.[2] There exists some additional charge that can be injected from the electrode to the solution or vice versa in Faradaic processes. This impedance is known as the charge transfer resistance, or Faradaic resistance.[3]

Often times, many processes and charge transfer mechanisms may occur during electrochemistry impedance measurements; however, the simple circuit model shown in the figure above can be used as a starting point to better

understand the mechanisms of charge flow in electrode impedance measurements.

3.2: EIS characterization

Potentiostatic EIS measurements were used to study the electrochemical impedance of the electrode in a 1X phosphate buffered saline solution. This solution emulates in vivo physiological conditions for the purpose of electrochemistry experiments. A small AC potential, which is kept constant, hence potentiostatic, is applied to the electrochemical cell and then current is measured through the electrode. A three-electrode cell was used for all measurements with an Ag/AgCl reference electrode, stainless steel counter electrode, and a functional device as the working electrode.
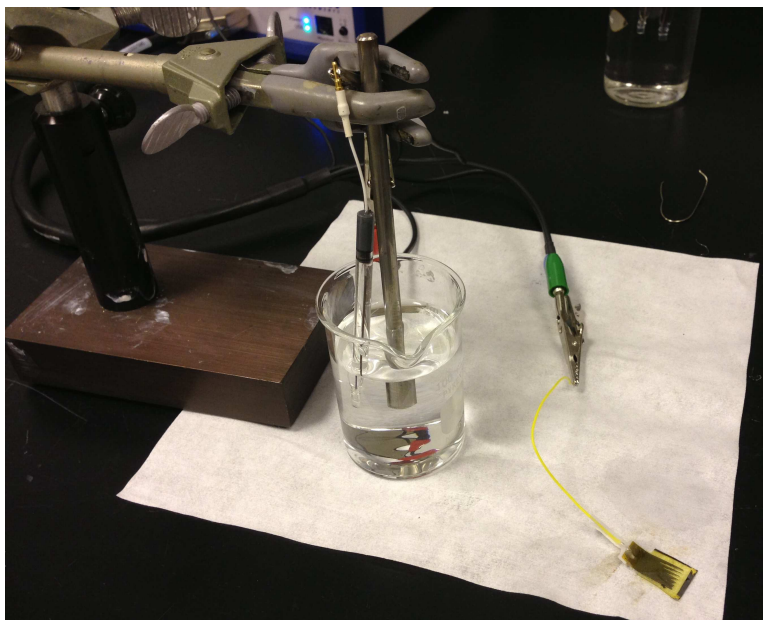

Figure 3.2: Three-electrode cell used for electrochemical impedance spectroscopy measurements

The device under test is a 32-channel electrode with silicon microwires coated in platinum, and twenty-four runs were taken on distinct leads. Graph 3.1 shows a histogram of the device impedance at 1 kHz for the 24 different channels under test.

Graph 3.1: Histogram of device impedance tested for 24 distinct channels
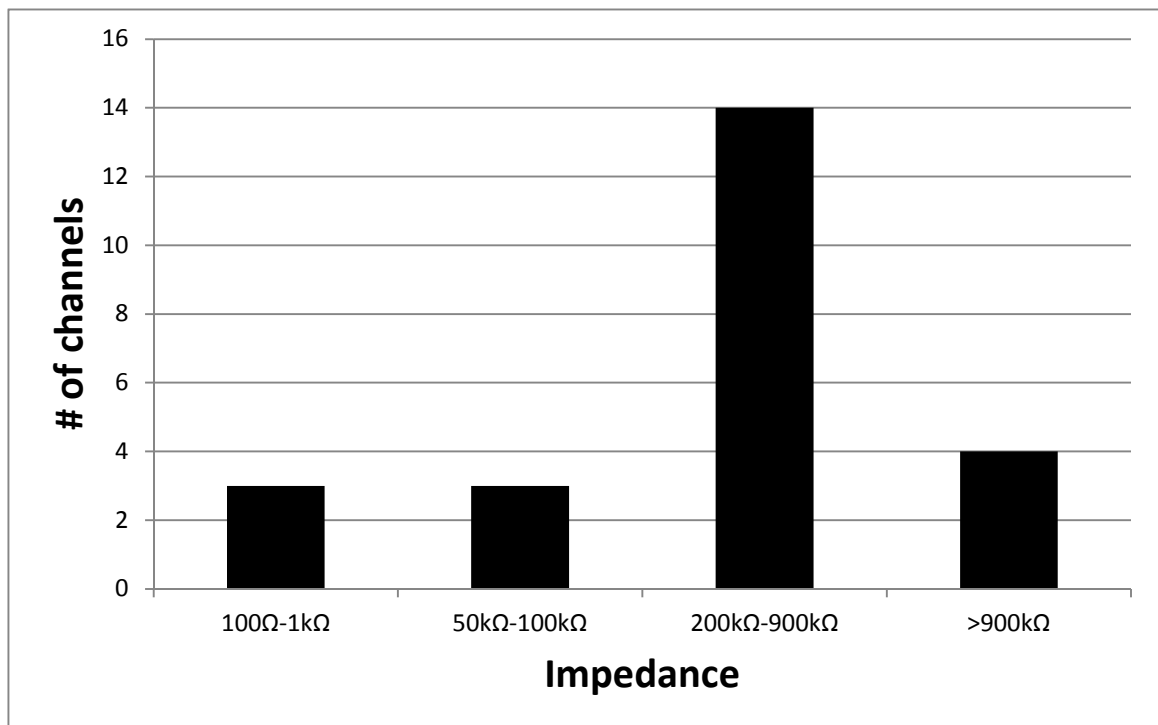
EIS curves of the platinum coated neural electrodes showed large variations in both impedance vs. frequency and phase vs. frequency across the 24 channels under test. This large discrepancy between leads is likely due to physical imperfections of the device itself caused by fabrication; however, over 50% of the tested channels showed impedances between 200-900 kΩ. These

channels demonstrated the most reliable, repeatable measurements of the neural electrode, and data from these channels was used in further analysis of impedance measurements.

Some channels exhibited erratic phase and high impedances, which is characteristic of an open circuit. Open circuits may be caused by poor electrical connection between the silicon microwire and metal lead below, or even from discontinuous metal layers between the access via and zero insertion force clip. Some other leads exhibited uncharacteristically low impedances, which is typical of shorted leads. Short-circuited electrodes may have continuous platinum films connecting multiple electrodes together, or the low impedance may be due to some exposed metal drawing current through the lead. In either case, these results are characteristic of poorly fabricated electrodes, and these channels are not suitable for reliable neural recordings.

Graph 3.2 and 3.3 show impedance and phase data over several decades of frequencies of the 14 functional channels. The average impedance and phase of the 14 channels was calculated with error bars is showing the min and max values measured at that frequency. The device shows impedances at 1kHz to be between 200-900kHz, which is suitable for single unit recording in neural tissue.[4] The phase of the impedance curve hovers between about -55 to -75 degrees, suggesting the impedance of the device is dominated by capacitance, likely due to the double layer effect discussed earlier in this chapter. The large variations in

phase may have arisen due to wires being manually soldered at the zero insertion force adapter to connect the device to EIS instrumentation.

Graph 3.2: Magnitude of impedance vs. frequency plot for platinum coated neural electrodes
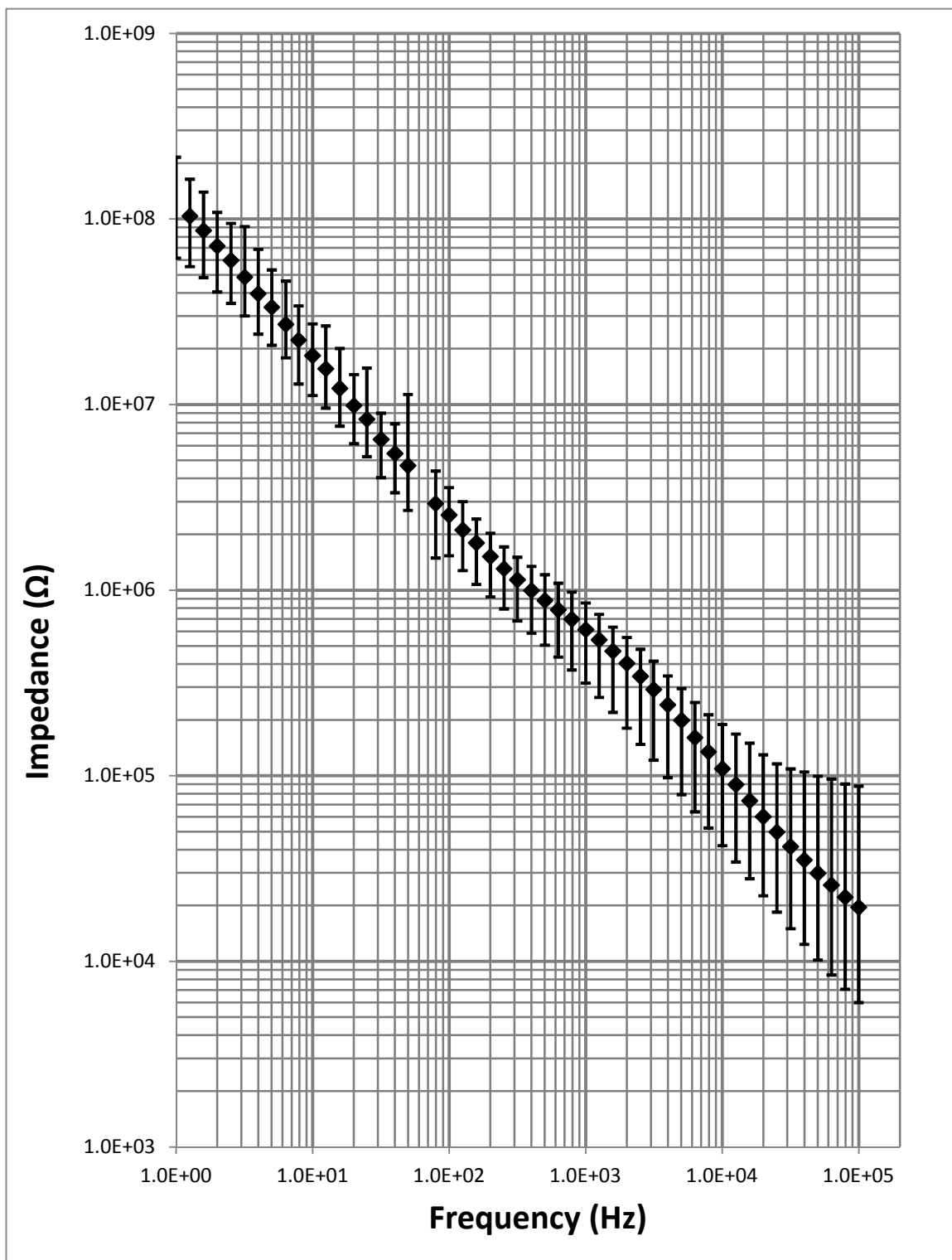
Graph 3.3: Phase vs. frequency plot for platinum coated neural electrodes
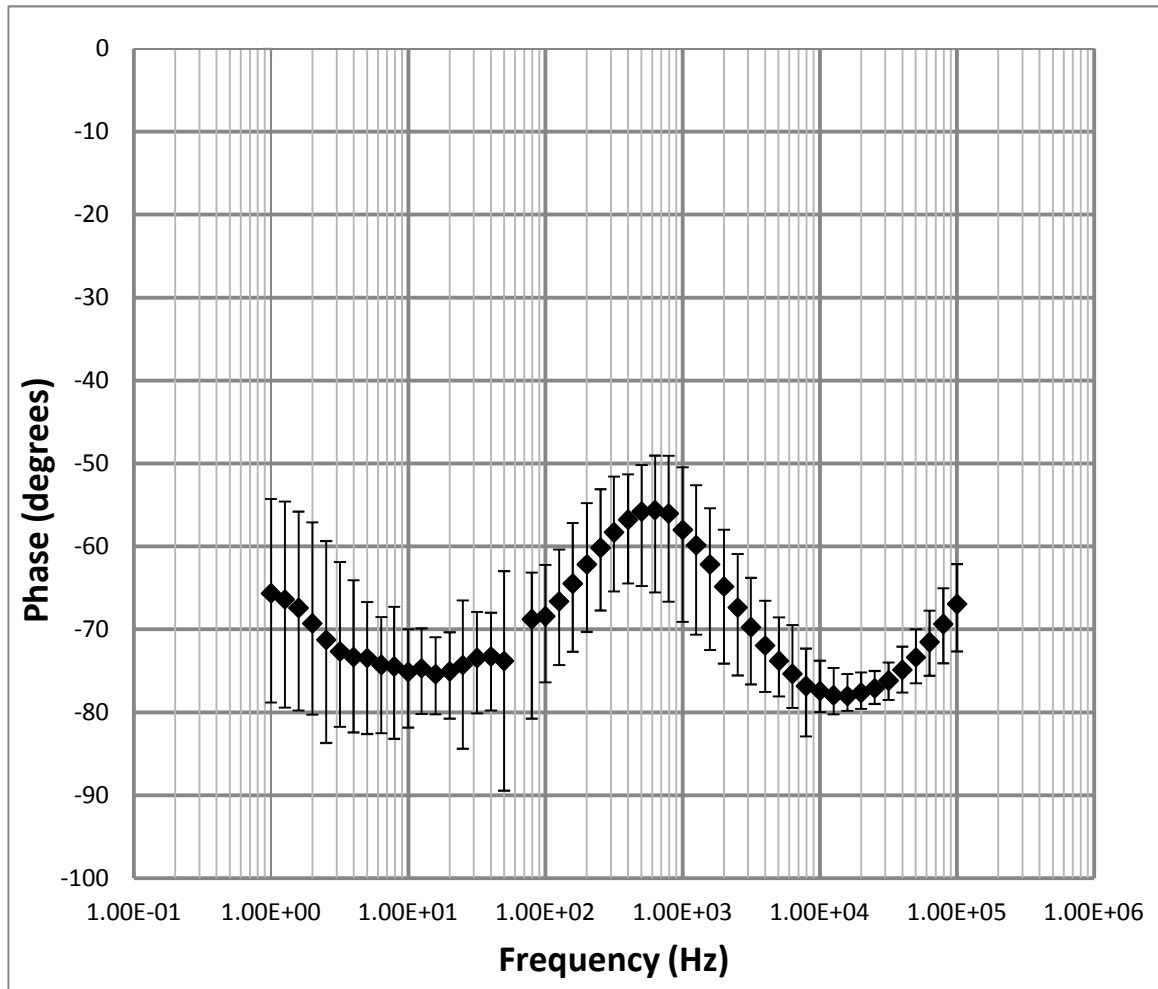
Graph 3.4 shows a Nyquist plot of the device under test, with the data point taken at 1kHz plotted in red. The linear nature of the Nyquist data from this device again suggests that non-Faradaic processes, namely the double layer capacitance, dominate charge transfer at the electrode-electrolyte interface.[3]

Graph 3.4: Nyquist curve of the platinum coated neural electrode. Impedance at

1kHz is in red.
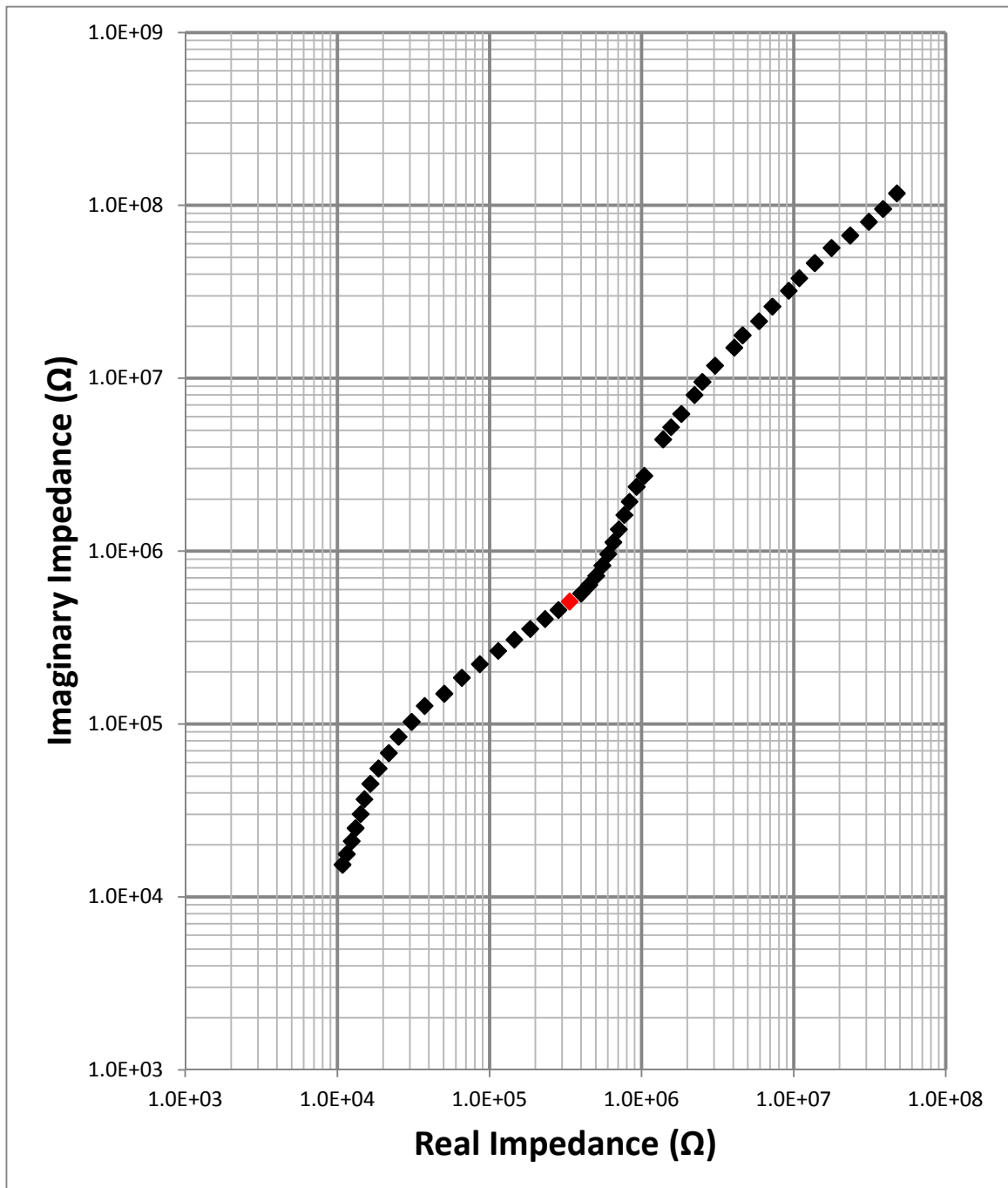
Graph 3.5 shows impedance data from a device not coated with metal plotted against a device with platinum coated silicon microwires, demonstrating a reduction in impedance after the metal coating. Silicon microwires were initially left uncoated, but exhibited impedances too high for single unit recordings. Final efforts were made to optimize the impedance as much as possible, including adding a metal coating step to the end of the process flow. The impedance of the device dropped about one order of magnitude with the metal coating treatment.

Because the impedance of the platinum coated device is dominated mainly by the double layer capacitance, it is believed that further reductions of impedance can be achieved by using coatings with effectively high surface area, such as platinum black.[5] While platinum black has proven to be a viable candidate as a coating for neural electrodes, further efforts must be made to increase the long-term durability of the coatings before electrodes utilizing this material can be used in a chronic implant.[6]

Graph 3.5: Optimization of electrode impedance using platinum coating of silicon microwires.
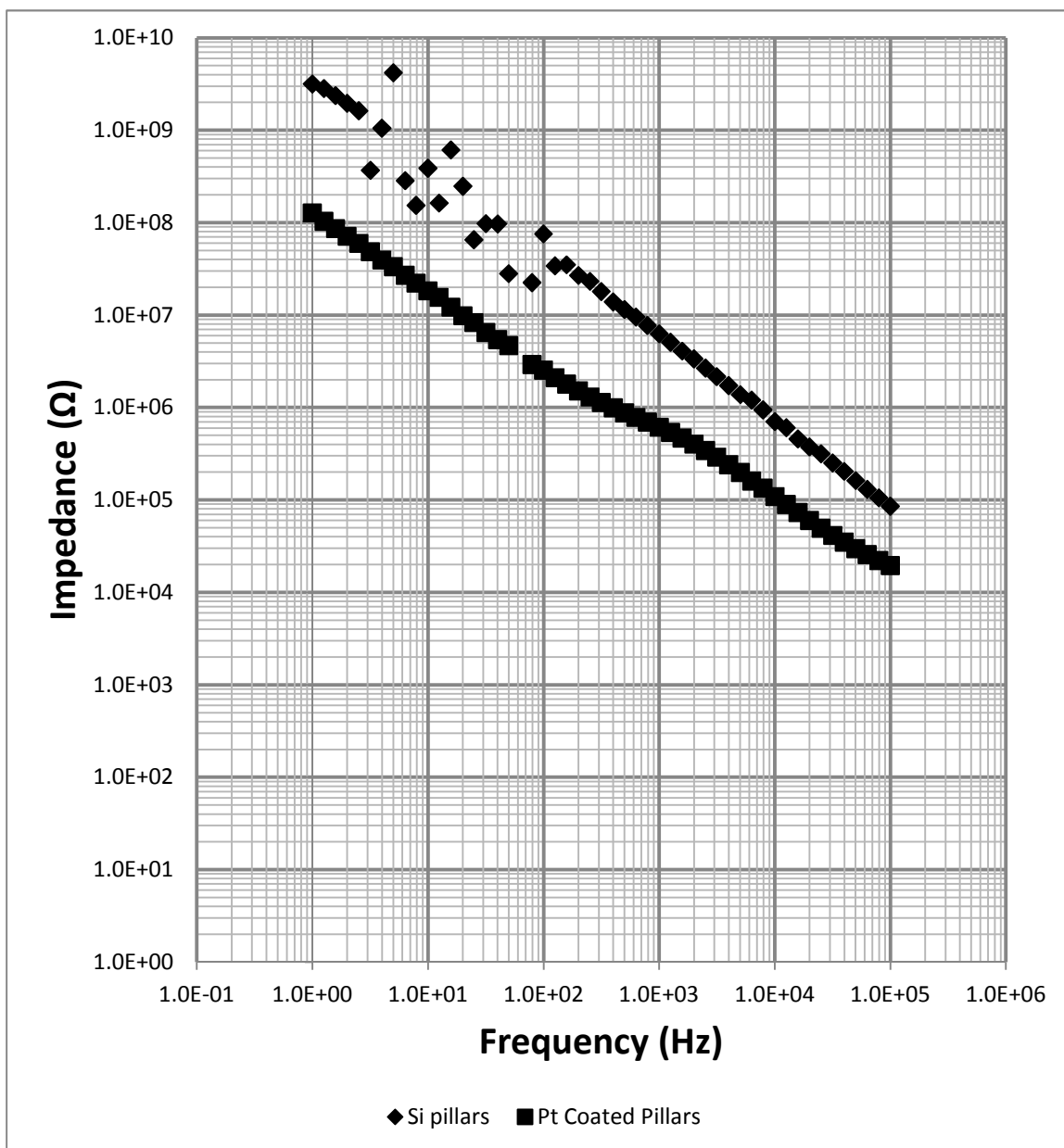
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[1] Daniel Merril, Marom Boksom, John Jeffreys, Electrical stimulation of excitable tissue: design of efficacious and safe protocols, Journal of Neuroscience Methods, Volume 141, Issue 2, 171-198, 2005

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[3] E.T. McAdams, A. Lackermeiser, J.A. McLaughlin, D. Macken, The linear and non-linear electrical properties of the electrode-electrolyte interface, Biosensors and Bioelectronics, Volume 10 Issues 1-2, 1995

[4] Akifumi Fujishiro, Hidekazu Kaneko, Takahiro Kawashima, Makoto Ishida & Takeshi Kawano, In vivo neuronal action potential recordings via three-dimensional microscale needle-electrode arrays, Scientific Reports, 4:4868

[5] Carl Marrese, Preparation of strongly adgerent platinum black coatings, Analytical Chemistry, volume 59, 217-218, 1987

[6] Sharanya Desai, John Rolston, Liang Guo, Steve Potter, Improving impedance of implantable microwire multi-electrode arrays by ultrasonic electroplating of durable platinum black, Frontiers in Neuroengineering, Volume 3, number 5, 2010

Chapter 4: Summary and future work

4.1: Summary of the thesis

The fabrication and electrical impedance characterization of metal-coated silicon microwires etched back onto pre-patterned polyimide substrates was investigated in this thesis. The 4x4 neural electrode design presented here has the highest density of sensing elements of any neural electrode of its kind to date. The key improvement of prior art of this design is the integration etched back penetrating microwires onto ultrathin conformable substrates.

Many design elements were considered and several difficulties including low process temperatures, and limited wet chemical processing were overcome. Furthermore, the neural electrode was fabricated in a highly parallelizable CMOS compatible process flow, which could be scaled up for commercial manufacturing.

EIS characterization of the neural electrode showed these devices had low enough impedance, on the order of a few hundreds of kilohms, to be used for single unit action potential measurements. Over one half of the electrode leads tested showed repeatable, reliable measurements.

4.2: Research outlook and possible improvements

Most of the work in this thesis has been dedicated to the design and fabrication of the neural electrode. The realization of this device however is only the first step towards a much broader research goal. Further testing on pillar coatings can be investigated, to perhaps further reduce the device impedance in solution. Iridium oxide coatings have yet to be studied and may offer an alternative to platinum as a microwire coating. In addition, neurophysiology tests must be performed on the neural electrode before design elements such as microwire dimension and spacing can be further optimized. Furthermore, mechanical stress tests can be performed on the neural electrode and conformality studies can be performed either on cortical tissue or tissue phantoms. Moreover, an electrode such as this one may be used not only as a neural interface, but as a retinal interface as well. This thesis shows some promising fabrication results and opens the door for several different exciting lines of research.