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The Electromechanical Responses of Suspended Graphene Ribbons for Electrostatic Discharge Applications

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The Electromechanical Responses of Suspended Graphene Ribbons for Electrostatic Discharge Applications

A dissertation submitted in partial satisfaction of the

requirements for the degree Doctor of Philosophy

in Materials Science and Engineering

by

Wei Zhang

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ABSTRACT OF THE DISSERTATION

The Electromechanical Responses of Suspended Graphene Ribbons

for Electrostatic Discharge Applications

by

Wei Zhang

Doctor of Philosophy in Materials Science and Engineering

University of California, Los Angeles, 2015

Professor Ya-Hong Xie, Chair

This dissertation presents a novel suspended graphene ribbon device for electrostatic discharge (ESD) applications. The device structure is proposed and fabricated after careful design considerations. Compared to the conventional ESD devices such as diodes, bipolar junction transistors (BJTs), and metal-oxide-semiconductor field-effect transistors (MOSFETs), the proposed device structure is believed to render several advantages including zero leakage, low parasitic effects, fast response, and high current carrying capability, etc. A process flow is developed for higher yield and reliability of the suspended graphene ribbon device which is very delicate in nature. Direct current (DC) and transmission-line pulse test (TLP) measurements are carried out to investigate the switch-on behavior of the device which is crucial for ESD protection. DC measurement with a different configuration is used to characterize the mechanical shape evolution of

the graphene ribbon upon biasing. Finite Element Simulations are also conducted to verify the experimental results, which are in good agreements. Furthermore, the breakdown properties of graphene ribbons are tested using TLP. It is found that graphene has a better current drivability compared to copper wires which is widely used as interconnects in integrated circuits (ICs). Also, bi-layer graphene has a higher breakdown current than monolayer graphene which indicates that multilayer graphene should be superior in current discharging. Last, Ab inito calculations are carried out to study the growth mechanism of multilayer graphene which is needed for graphene homo-epitaxy with precise control. It is found that a carbon cluster with six carbon atoms has the smallest kinetic barrier thus largest surface diffusivity during surface diffusion. So it is believed to be the most favorable diffusing species for graphene homo-epitaxy.

The dissertation of Wei Zhang is approved.

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1. Wei Zhang, Xinke Yu, Erica Cahyadi, Ya-Hong Xie, and Christian Ratsch, Appl. Phys. Lett. 105, 221607 (2014).

2. Wei Zhang, Biyun L. Jackson, Ke Sun et al., International Journal of Photoenergy, Volume 2015, Article ID 253296 (2015).

3. Wei Zhang, Peichi Liu, Biyun Jackson, Tianshu Sun et al., J. Appl. Phys. 113, 144908 (2013).

4. Ke Sun, Wei Zhang, Biyun Li, Jae Young Lee et al., IEEE Trans. Nanotechnol. 11, 999 (2012).

5. Wei Zhang, Qi Chen, Ming Xia, Rui Ma et al., invited paper accepted by 11th International Conference on ASIC (ASICON 2015).

6. Pu Wang, Wei Zhang, Owen Liang, Marcos Pantoja, Jens Katzer, Thomas Schroeder, and Ya-Hong Xie, ACS Nano 6, 6244 (2012).

7. Pu Wang, Owen Liang, Wei Zhang, Thomas Schroeder, and Ya-Hong Xie, Adv. Mater. 25, 4918 (2013).

Chapter 1. Introduction

1.1. ESD event and test models

Electrostatic discharge (ESD) is probably familiar to everyone since one could hardly not experience some kind of ESD events in our daily lives. When two objects with different potential are brought into close proximity, transfer of electrostatic charges between two objects occurs. This process is called electrostatic discharge. The ESD event interested to semiconductor ICs is generally referred to the ones with very short duration of about 150 ns, which generates very high current and voltage transients, up to a few tens of Amperes and kilovolts. Such fast and large ESD transients may cause severe damages to ICs [1, 2]. Fig. 1.1 shows an example image of an ESD damaged chip. In order to protect ICs from ESD damage, and electronic on-chip component, often called ESD device, is always designed and built.

The ESD protection performance level, often regarded as ESD robustness, is determined by the ESD failure threshold voltage of an IC part, normally called ESDV in units of volts or kilovolts. In order to estimate the ESDV level of an IC part, or to specify its ESD rating on data sheet, one needs to test the IC part by stressing the device under test (DUT) with emulated ESD zaps, a procedure called ESD zapping. To obtain reliable ESD zapping results, it is extremely critical to be able to generate reproducible ESD transients using an ESD tester satisfying accepted ESD specifications. Many ESD test models have been developed such as Human Body Model (HBM), Machine Model (MM), and Charged Device Model (CDM), etc. These model are designed to mimic different ESD environment by producing ESD transients capacitively, inductively, or both. [1]

Though the ESD models mentioned above have their specific features, such as peak current, parasitic resistance, discharge resistance, etc., they share one feature in common: the test methods are destructive. In other words, the results provided by these test methods only tell us the failure ESD threshold voltage level, but offer no information about the possible failure mechanism. Apparently the failure mechanism is very crucial for the design and improvement of ESD devices. In order to obtain such important information, a Transmission-line-pulsing (TLP) model is raised up. The principle of TLP testing is as follows. A piece of transmission line cable is precharged to a certain voltage level, then discharges into the DUT through another transmission line cable with constant matching resistance of 50 Ohm. By doing this, a stable square waveform is generated to stress the DUT. The typical set up and equivalent circuit is shown in Fig. 1.2. The instantaneous current and voltage data (I-V curve) is obtained by probing the current and voltage of the DUT using oscilloscopes. The voltage level is incrementally stepped up so that one can obtain an I-V curve of the DUT under increasingly stressing until the breakdown point is reached which is characterized by an abrupt drop of current as shown in Fig. 1.3. Usually a time duration (t_d) of 100 ns and a rise time (t_r) of 10 ns are used in the TLP testing to match with HBM model. [1]

Fig. 1.4 shows a BARTH Model 4002 TLP tester used in the study for graphene device testing.

1.2. ESD protection mechanisms

There are mainly two ESD failure mechanisms: thermal damage and dielectric rupture. These are caused by very high transient current and electric field generated by

ESD pulse. The principle of the on-chip ESD protection is to safely discharge the high current via low impedance path and to clamp the voltage to a sufficiently low level which won't damage the core circuit of ICs. There are two methods to realize the purpose mentioned above as shown in Fig. 1.5. Fig. 1.5 (a) depicts the first solution that a simple turn-on I-V characteristics is used to dump the high current via a low resistance path. The ESD device is turned on at V_{t1} which is the trigger voltage. This voltage needs to be lower than the breakdown voltage of core circuit of IC to clamp the voltage to a safe level, while it should be higher than the normal operation voltage of IC to avoid accidental turn-on which will affect normal operation. The second option is illustrated in Fig. 1.5 (b). Similarly the ESD device is turned on at V_{t1} and driven into a snapback region. The snapback region is characterized by a low holding voltage (V_h) and current (I_h) and a low impedance path. This snapback characteristic is very beneficial to ESD protection because it clamps the voltage to a lower safe level which leave more space in the design window. A second breakdown represents the ESD protection level of the ESD device meaning beyond which voltage or current level the ESD device will breakdown [1]. In the following sections, the conventional ESD devices are discussed.

1.2.1. Diode as ESD device

It should be straightforward that a diode can be used as a ESD device which falls into the first category as shown in Fig. 1.5 (a). It worth noting that single forward diode is usually not used as ESD protection device due to its low forward turn-on voltage (~0.7 V). A string of diodes can be used instead to increase the turn-on voltage. In reality however, a reverse connected diode (Zener diode) is usually used. The turn-on voltage is

determined by the reverse breakdown voltage. It is well known that reverse breakdown is caused by avalanche multiplication, or impact ionization which is reversible, so the ESD device can be used repeatedly without malfunction.

There is always a trade-off between the ESD protection level and parasitic capacitance. Usually large-area ESD structure renders higher robustness, i.e. higher breakdown current and voltage, but meanwhile the ESD-induced parasitic effects will also be pronounced which is a killing factor of mixed-signal and RF ICs. As a consequence, a figure of merit (FOM) is often used to evaluate the performance of ESD devices:

$$FOM = I_{t2}/C_{ESD} \qquad \textit{Equation 1.1}$$

where I_{t2} and C_{ESD} are the second breakdown current and ESD-induced parasitic capacitance, respectively.

Due to the structure simplicity, diodes typically have low on-resistance (R_{on}) and small C_{ESD} (comes from junction capacitance and diffusion capacitance of diodes), which gives diodes the largest FOM of ~20 mA/fF among all traditional ESD devices[3]. Also, diodes consume least chip area compared to other ESD devices. Moreover, the response time of diodes is pretty fast usually less than 10 ns. This is determined by the turn-on time of diodes which is further dependent on its transit time and saturation velocity since for a ESD device, it is usually operates under high electric filed. However, the main problem of diodes is their large leakage which is intolerant with the scaling down of ICs.

1.2.2. Bipolar junction transistor as ESD device

A bipolar junction transistor (BJT) can also be used as an ESD protection device. It typically works in the snapback mode as mentioned in Fig. 1.5 (b). The ESD protection circuit is shown in Fig. 1.6. The scheme shown in Fig. 1.6 (a) is an simplest example: since the collector and emitter of the bipolar junction transistor are reversely biased, it is normally in off state. When an positive ESD event happens, the base potential V_B needs to be raised to turn on the bipolar junction transistor where a low resistance path is formed to discharge the current. In practice, Fig. 1.6 (b) shows the connection often used in the design of bipolar junction transistor ESD configuration. When an ESD pulse appears at the I/O pad, since V_B is zero biased, the collector is reversely biased and breakdown. So avalanche multiplication takes place and current of collector junction passes through resistor R. This will build up the potential of V_B which keeps increasing until the emitter junction is turned on. Once the bipolar junction transistor is turned on, a low resistance path is formed so V_c starts to decrease and the bipolar junction transistor works in the snapback region and the voltage is clamped to a low level of V_h.

Fig. 1.7 shows the cross-section of a bipolar junction transistor and its parasitic C_{ESD} model. The base-collector capacitance (C_{cb}) and collector-substrate capacitance ($C_{c\text{-}sub}$) dominate the total C_{ESD} where C_{be} doesn't play much role. Apparently due to bipolar junction transistor's complexity in device structure, it has a larger C_{ESD} than diodes. Therefore, the FOM for bipolar junction transistors is usually smaller than diodes. On the other hand, the response time for bipolar junction transistor is longer than diodes because it has a reverse breakdown and potential accumulation process. But compared to diodes, bipolar junction transistors have the advantages of lower leakage current and snapback

behavior. The snapback depth and V_h are directly related to impact ionization, base width, BJT current gain, and resistance in the path.

1.2.3. Metal-oxide-semiconductor field-effect transistor as ESD device

Typically the metal-oxide-semiconductor field-effect transistor (MOSFET) is connected as illustrated in Fig. 1.8 to work as an ESD protection device. This structure is called grounded-gate n-channel MOSFET (ggNMOS) in which the drain (D) is connected to the I/O pad and the gate (G), source (S), and body (B) are shortened together to ground. This unique connection is used to minimize the leakage current [1]. When a positive ESD pulse comes to the I/O pad, the DB junction is reversely biased to its breakdown. Then avalanche multiplication happens and generates electro-hole pairs. Hole current flows into the body and build up a potential aross BS via parasitic resistance R. Therefore, BS junction is biased positively. With the increase of V_R, BS junction will be eventually turned on which turns on the lateral DBS transistor. What happens next is same as a BJT discussed in previous section.

The parasitic C_{ESD} model of a ggNMOS is shown in Fig. 1.9. In the configuration shown in Fig. 1.8, the gate-source overlap capacitance (C_{gs}), BS junction capacitance (C_{sb}), body to guard ring and substrate capacitances ($C_{b\text{-}nw}$ and $C_{b\text{-}sub}$) are negligible because they are under forward or zero bias in operation. As a result, C_{ESD} is dominant by gate-drain overlap capacitance (C_{gd}) and DB capacitance (C_{db}). Similar to BJT, due to ggNOS's structure complexity, the FOM is usually smaller than diodes and its response time is long. But it is highly compatible to CMOS technologies besides the advantages of lower leakage current and snapback behavior.

1.3. New challenges for ESD devices

While the traditional ESD protection configurations still dominate in IC designs, as the feature size of ICs keeps on decreasing according to Moore's Law, the demand for novel ESD devices becomes more and more urgent. The challenges of current ESD solutions include: (1) As mentioned in previous sections, traditional ESD solutions utilize diodes, BJTs, and MOSFETs which are very leaky inherently. For example, the typical leakage current for a 2.5 kV classic ggNMOS ESD device is ~100 nA which is intolerable to advanced ICs at sub-45nm nodes [1]. Nowadays, the concept of high-efficiency and low-power IC is of great importance which requires low stand-by power consumption. So it is obvious a novel ESD device with low leakage is needed. (2) The ESD event always comes with high current and voltage surges, which generates ultra large amount of heat. This unique characteristic of ESD event inevitably requires the structure to be superior in electrical and thermal conductivity. Modern electronics require more robust ESD protection meaning larger ESD size for less heat generation and better dissipation. Using conventional ESD structures, typically 25%-50% of the chip area is consumed by ESD protection circuit. This causes layout problem, excessive ESD parasitic, and also larger leakage. Novel ESD device structure and interconnect material are needed to replace the currently used copper wires. (3) Advanced ESD protection standards require fast response time of ESD devices in the range of 10^{-10}~10^{-9} seconds. Simple diodes usually may meet this requirement but it is the leakiest one among traditional ESD devices. BJTs and MOSFETs typically has a response time ~10 ns due to their structure complexity compared to diodes. (4) The parasitic capacitance (C_{ESD}) and

noise issues also become more severe with the shrinking dimensions of ICs. CESD for conventional ESD devices are typically 0.1~1 pF. This will critically affect the performance of mixed signal and RF ICs. High performance ESD solution with low parasitic effects is highly demanded.

Given that the traditional ESD devices cannot meet the demands of modern ESD protection, an innovative ESD device structure needs to be developed for modern high-efficiency and low-power ICs.

1.4. A graphene-based innovative ESD protection approach

According to the challenges of traditional ESD devices, first of all, a new material is needed for interconnects to replace current copper wires for better electrical and thermal conductivity. This is very crucial for the robustness of ESD device and reliable device performance and life time. Graphene, as a two-dimensional material with extremely good electrical, thermal conductivity, and mechanical strength is viewed as an excellent candidate [4-6]. Due to the high electrical conductivity of graphene which comes from its high mobility, if graphene ribbons (GRs) are used as interconnects, the heat generation will be tremendously reduced. Combined with graphene's excellent thermal conductivity, the heat dissipation problem is also resolved. And graphene is known as the hardest material in the world with strong mechanical strength, it guarantees the robustness of the device. Second, a novel ESD device structure needs to be developed. In this work, an electromechanical suspended GR ESD device structure is proposed. By using the proposed device structure, low leakage (ideally zero leakage) and high response

time can be promised. Detailed device structure will be discussed in the following chapters.

1.5. Dissertation outline

In this work, the focus is mainly on the design, fabrication, and characterization of an innovative electromechanical suspended GR ESD device. The content of this dissertation is listed as follows.

Chapter 2 of this dissertation gives an overview of graphene, including its properties, synthesis, characterization, and applications.

Chapter 3 presents in details about the structure, design considerations, fabrication, characterization, and electrical measurements of the proposed electromechanical suspended GR ESD device.

Chapter 4 reports the ab initio calculations of kinetic barriers of graphene homo-epitaxy. This study is carried out to investigate the growth mechanism of multilayer graphene.

Chapter 5 summarizes the dissertation and discuss possible future directions of the work discussed in this dissertation.

1.6. Figures

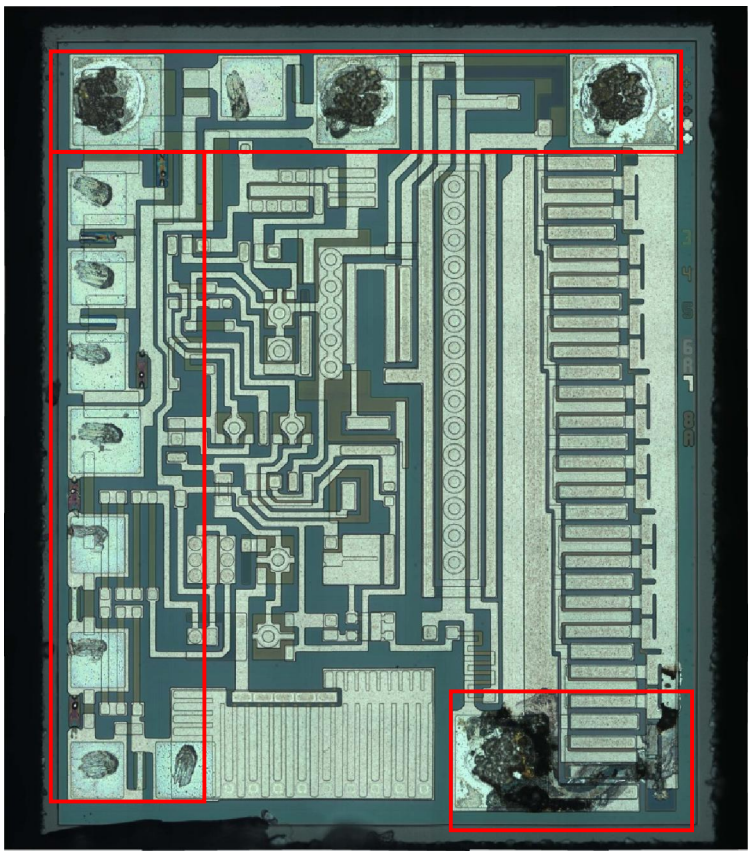


Fig. 1.1 An image of a chip after ESD damage (taken from web).

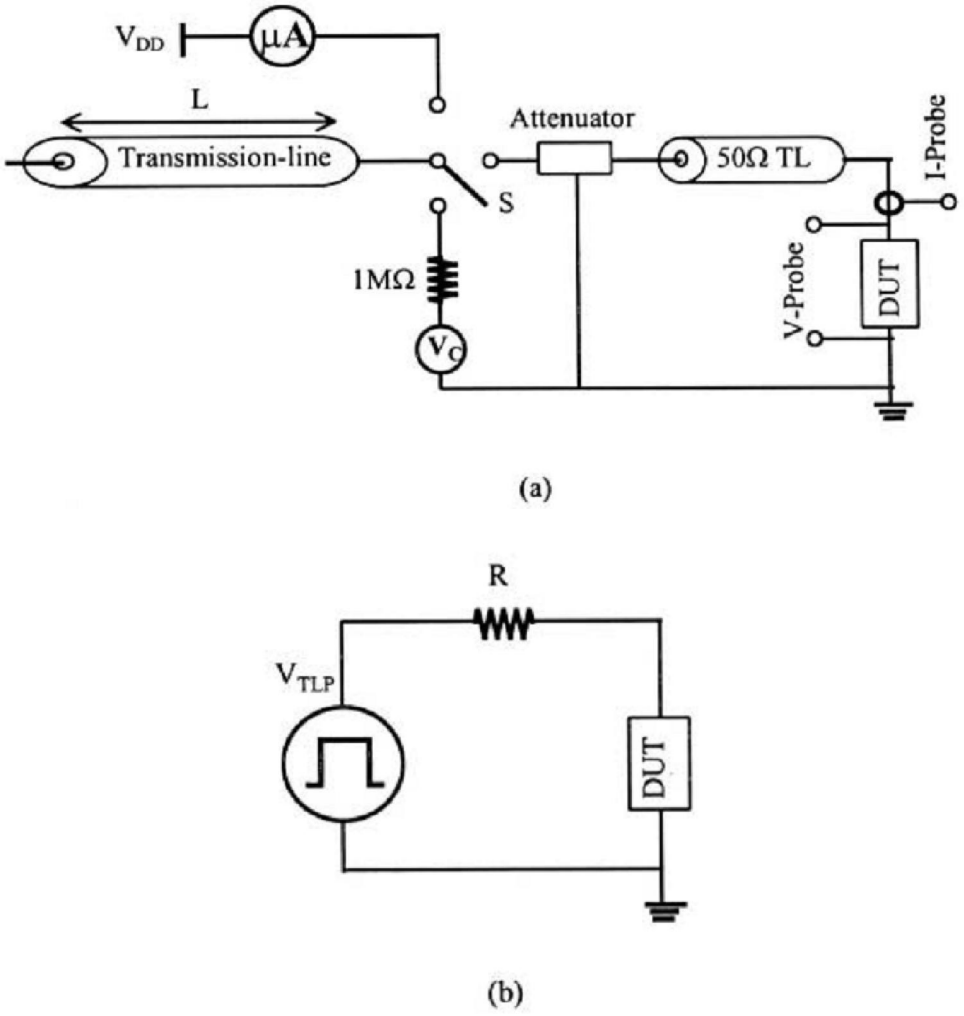


Fig. 1.2 (a) A typical TLP set-up; (b) the equivalent circuit. (After [1])

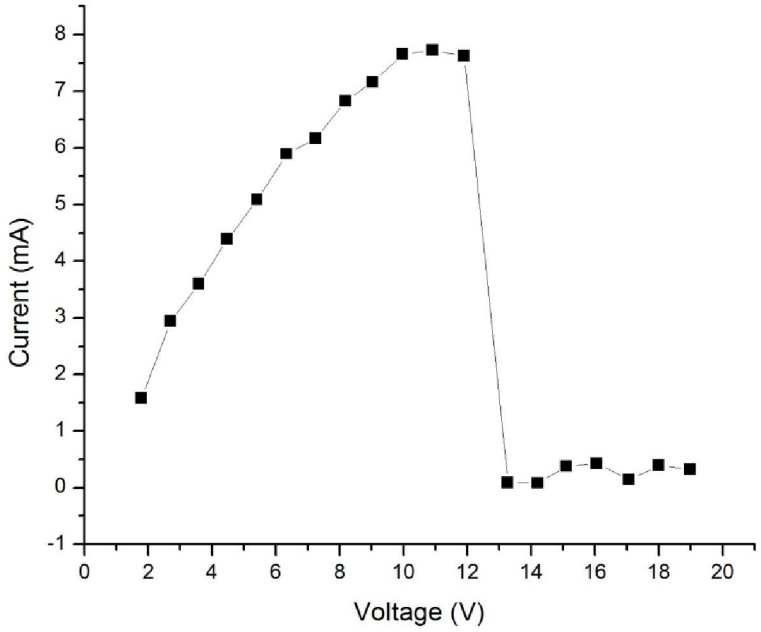


Fig. 1.3 A typical TLP breakdown I-V curve.

Fig. 1.4 A BARTH Model 4002 TLP tester used in the testing.

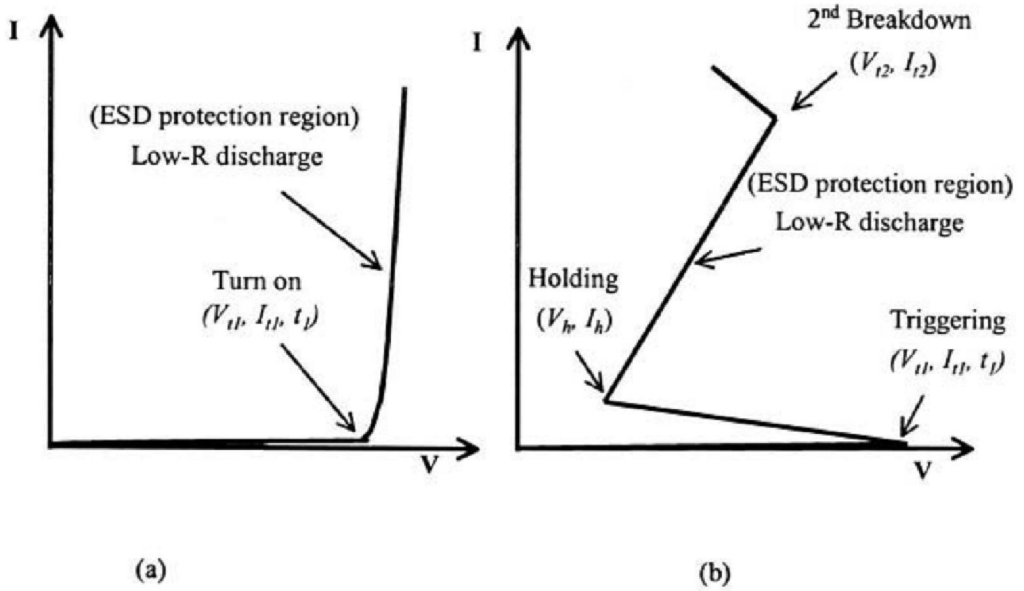


Fig. 1.5 Two typical I-V characteristics for ESD protection solution: (a) simple turn-on and (b) snapback. (After [1])

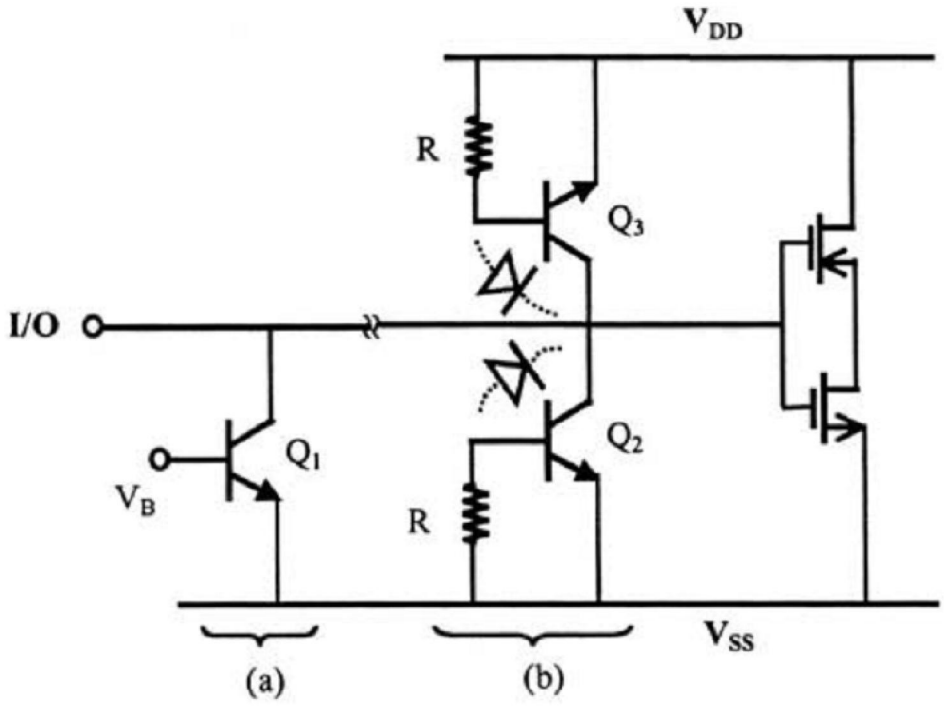


Fig. 1.6 Typical ESD protection scheme using BJTs. (After [1])

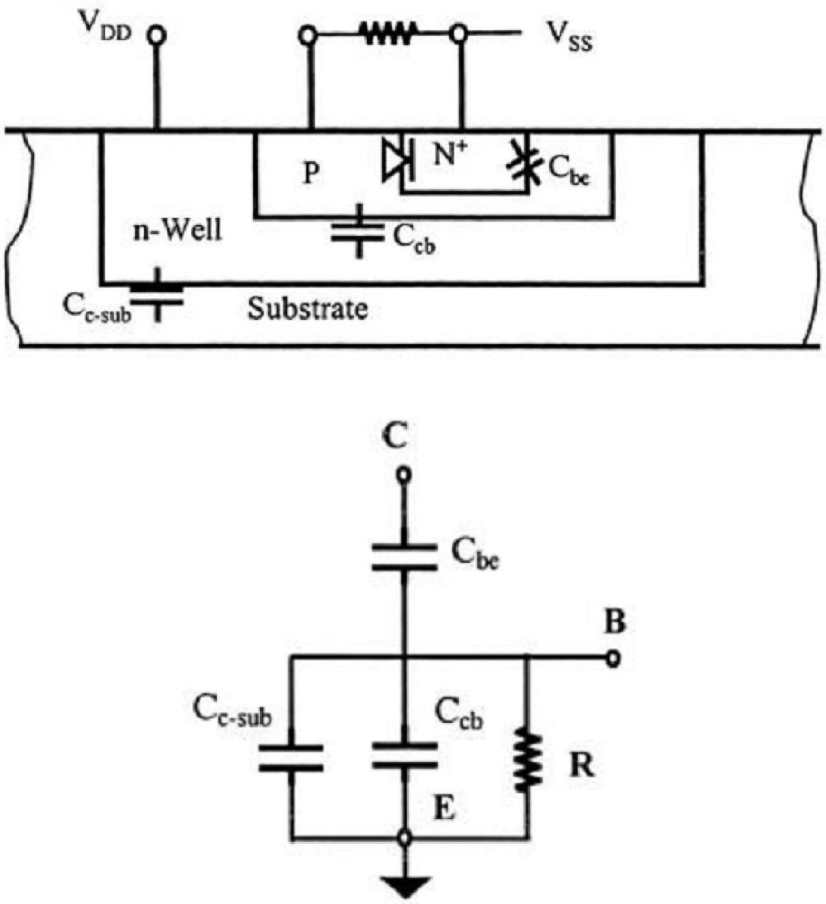


Fig. 1.7 A cross-section of a BJT and its parasitic C_{ESD} model. (After [1])

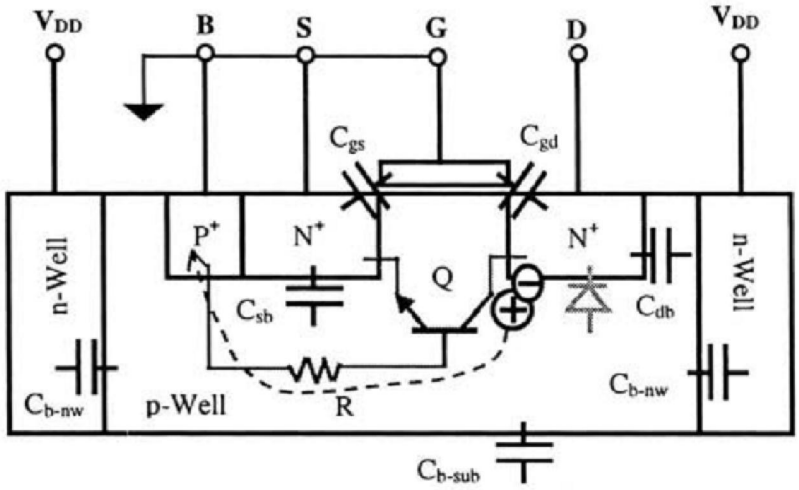


Fig. 1.8 Typical configuration of ggNMOS for ESD protection. (After [1])

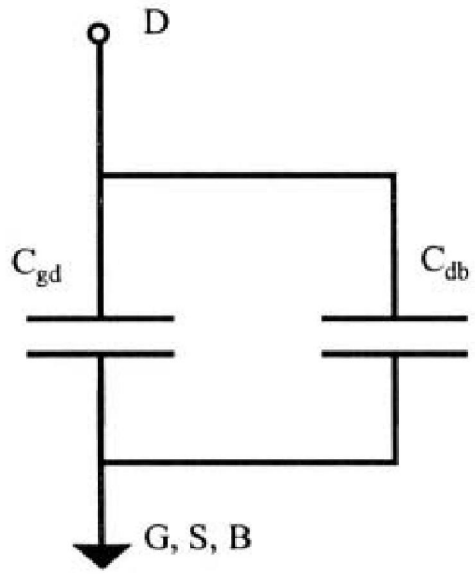


Fig. 1.9 A parasitic C_{ESD} model for ggNMOS. (After [1])

1.7. Reference

1. Albert Z. H. Wang, On-Chip ESD Protection for Integrated Circuits, Boston, Kluwer Academic Publishers, 2002.
2. Dangelmayer, G. T., ESD Program Management, Boston, Kluwer Academic Publishers, 1999.
3. Sami Hyvonen, and Elyse Rosenbaum, Electrical Overstress/Electrostatic Discharge Symposium, 1-9 (2005).
4. K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, and A. A. Firsov, Science, 306, 666 (2004).
5. Y. Zhang, Y. -W. Tan, H. L. Stormer, and P. Kim, Nature, 438, 201 (2005).
6. Y. M. Lin, C. Dimitrakopoulos, K. A. Jenkins, D. B. Farmer, H. Y. Chiu, A. Grill, and P. Avouris, Science, 327, 662 (2010).

Chapter 2. Overview of graphene

2.1. Basics about graphene

Graphene is a two-dimensional crystalline material consisting of carbon atoms with a honeycomb lattice structure. It is the building block of graphite which is comprised of large number of layers of graphene stacking together with specific order by van der Waals forces. There are many allotropes of carbon such as graphene, graphite, carbon nanotubes, and fullerenes, etc., which are shown in Fig. 2.1 (a)-(d). Graphene is one of the most unique one with excellent electrical, thermal, and mechanical properties, thus draws tremendous attentions in the past decade since it is first found by K. S. Novoselov et al. in 2004 [1-3]. As mentioned in the last section of Chapter 1, these excellent properties of graphene guarantee it to be a suitable candidate for ESD applications.

As shown in Fig. 2.1 (a), graphene has a lattice structure of carbon atoms arranging in a two-dimensional hexagon shape. The carbon atoms are bonded to its nearest neighbors by a very strong sp^2 covalent bond. This is the origin of the excellent mechanical strength of graphene. The carbon-carbon bonding length is about 1.42 Å. Each carbon atom shares a π bond with its three nearest neighbors resulting in a band of filled π orbital (valence band) and a band of empty π^* orbital (conduction band). Figs. 2.1 (e) and (f) depict the lattice structure of graphene in real space and its unit cell in reciprocal space. The two points K and K' at the corners of the graphene Brillouin zone (BZ) are of particular importance for the electronic properties of graphene. These two points are named as Dirac points. Fig. 2.2 shows the electronic band structure of

graphene, in which we can see the Dirac points are where the valence and conduction bands meet. The linear dispersion relationship is also drawn in Fig. 2.2 known as Dirac cone. This can be described by the equation

$$E = \hbar v_F k \qquad \textit{Equation 2.1}$$

where $\hbar = h/2\pi$ is the reduced Planck constant, $v_F = 10^8$ cm/s is the Fermi velocity in graphene. This linear relationship is one of the most unique characteristic of graphene which indicates that the mobility of electrons and holes equal to each other. [4]

2.2. Band structure and density of states of graphene

As mentioned above, the band structure and density of states (DOS) of graphene are of great importance since they determines the electronic properties of graphene. Since its first discovery in 2004, many efforts have been made to calculate the band structure and DOS of pristine graphene, disordered graphene, and doped graphene, in which most of them use tight-binding approach [4-8]. In this section, ab initio calculations are used to study the band structure and DOS of pristine and defective monolayer and bilayer graphene.

2.2.1. Band structure of monolayer and bilayer pristine graphene

The calculations are based on DFT as implemented in the Fritz Haber Institute ab initio molecular simulations package (FHI-AIMS) [9-11]. This is an all-electron full potential DFT code that uses numeric atom centered orbitals as its basis set. Details about the DFT calculations will be discussed in Chapter 4. The convergence of the results has

been carefully tested with respect to the system size, the basis set, and the density of the numerical integration mesh.

Fig. 2.3 shows the lattice structure and band structure of pristine monolayer graphene. As can be seen from Fig. 2.3 (b), near the Fermi level (E_F) around Dirac point (K), the E-k dispersion relationship is linear as discussed in previous sections. Similarly, Fig. 2.4 shows the lattice structure and band structure of pristine bilayer graphene. The two graphene layers are in A-B stacking which is one of the common stacking orders. Obviously the band structure of bilayer graphene is different from that of the monolayer graphene but the conduction and valence bands touch together at K point. This indicates that the bilayer graphene is also semi-metallic like monolayer graphene, which is consistent with the conclusions in the literature [12, 13].

2.2.2. DOS of pristine and defective monolayer and bilayer graphene

Ab initio calculations are also conducted to visualize the DOS of monolayer and bilayer graphene in pristine and defective forms.

Figs. 2.5 (a) and (b) show the calculated DOS of pristine monolayer and bilayer graphene, respectively. Apparently, both of them have zero value of DOS at Dirac point (Fermi level) indicating their semi-metallic characteristics which agrees with the band structure calculations and literature [12, 13].

Vacancies and grain boundaries are two types of defects commonly existed in graphene. Their presence in the graphene lattice disturbs the periodic lattice structure thus the band structure and DOS will be affected as well. As a result, the electrical properties of graphene will also be altered. In principle, the defective regions act as scattering

centers for charge carriers which will reduce the mobility and thus electrical conductivity. Figs. 2.6 (a) and (b) show the lattice structure of a defective graphene with a vacancy, and its corresponding DOS. The defective region in Fig. 2.6 (a) is colored as red which represents a vacancy with one carbon atom missing. It can be clearly seen from Fig. 2.6 (b) that there are three major bumps near Fermi level which are absent in pristine graphene. As discussed above, these bumps come from the defective regions in graphene which break the lattice structure periodicity. Figs. 2.7 (a) and (b) show the lattice structure of a defective graphene with a grain boundary, and its corresponding DOS. The carbon atoms at grain boundaries form pentagons and octagons instead hexagons. Similarly in the DOS shown in Fig. 2.7 (b), due to the disturbance of periodic lattice structure there is a huge peak near Fermi level and several small bumps. Therefore, it can be concluded that defects in graphene will form scattering centers which is not desired to make use of the excellent electrical properties of graphene. According to the discussions above, it is obvious that any form of defects such as point defects, grain boundaries will deteriorate the electrical conductivity by reducing the charge carrier mobility which is not desired for ESD applications. So the synthesis of graphene with least number of defects is the first step for a successful graphene based ESD device.

2.3. Synthesis of graphene

The work trying to synthesize monolayer graphene first starts in 1975 by B. Lang et al [1]. This is done by direct deposition of carbon on four platinum crystal faces. However, the formed sheets were not conclusively studied due to the inconsistency of the films. Since the first discovery of graphene in 2004, various of methods of synthesis of

graphene are developed and polished, which mainly include mechanical exfoliation, chemical vapor deposition (CVD) on metals, plasma enhanced CVD techniques, and thermal decomposition of SiC, etc [15]. In this section, these synthesis methods are briefly reviewed.

2.3.1. Mechanical exfoliation

It is well known that graphite consists of many layers of graphene stacking together by van der Waals force. Therefore, theoretically it is possible to obtain monolayer graphene by mechanical exfoliation of highly pure and ordered graphite sheet. After decades of exploration, it is difficult to get monolayer graphene though many efforts have been spent [16]. This is eventually realized by Novoselov el al. in 2004 [1]. In his work, a commercial highly oriented pyrolytic graphite (HOPG) was used. HOPG mesas were first prepared by O_2 plasma etching, followed by pressed against a wet 1 μm thick photoresist on glass surface. The substrate is then baked on hotplate after which the mesas became attached to the photoresist layer. Using scotch tape, graphite flakes can be peeled off repeatedly off the mesas. After many times of peeling off, the rest of the mesas was soaked in the acetone solution together with the substrate. So the photoresist would be resolved and the left-over flakes were released and floating in the solution. A Si wafer was then dipped into the solution to scoop for the flakes and washed in DI and propanol. The last step was ultrasonic cleaning in propanol, which would remove most of thick flakes. In the end, thin flakes were found to attach strongly to SiO_2 surface due to van der Waals force. Fig. 2.8 shows a multilayer graphene flake on SiO_2 substrate sample prepared by this technique. [1]

The mechanical exfoliation technique provides a simple way to obtain high-quality monolayer and multilayer graphene through a relatively clean process. The as-fabricated graphene usually render good electrical and mechanical properties, thus is still used by many researchers. However, the downside of this method is also obvious. It is impossible to get large area continuous graphene flakes with desired thickness. Therefore, this method can be hardly used for mass production of graphene, but is probably only limited to research purposes.

2.3.2 CVD growth of graphene on metals

Monolayer and multilayer graphene can be grown using CVD technique. The basic idea is to use gaseous precursors containing carbons to grow graphene on metal surfaces. The metals act as catalytic surfaces or media for the surface segregation of carbon atoms dissolved in the bulk of the metal. A lot of works have been done to study the CVD growth on metals, such as Ni, Cu, Fe, Pt, Pd, and Co, etc [17-21]. Among them, Ni and Cu are two metals most people use nowadays, but the growth mechanisms of them are different.

During the CVD growth of graphene on Ni, CH_4 and H_2 mixture gases are used as carbon source. At growth temperature higher than 1000 ^oC, CH_4 gas decomposes at the surface of Ni and individual carbon atoms appear. These carbon atoms will diffuse into the Ni bulk due to concentration gradient and form a solid solution. After the high temperature process, the growth temperature starts to decrease, during which the carbon atoms dissolved in the Ni bulk will begin to diffuse out and segregate at the surface of Ni. Crystalline films of multilayer graphene are formed. The number of layers of the film is

determined by the growth parameters including CH_4 flux, temperature, pressure, growth time, etc. [22-25]

Due to the very low solubility of carbon in Cu (less than 0.001 atom% at 1000 ^oC), the carbon source can only decompose at the surface of Cu to form carbon atoms. Therefore, the process of CVD graphene growth on Cu is a purely surface-mediated process in which Cu serves as an catalyst. Because of this, this process is self-limiting since after the growth of first layer of graphene no exposed Cu surface is available any more [26]. Therefore, compared to the graphene growth on Ni, the growth on Cu is easier to control. Fig. 2.9 shows a sample of large area monolayer graphene domain grown on Cu [27].

Apparently, after the growth of graphene, it is important to transfer graphene to other arbitrary substrates to make devices. A lot of efforts have been made to develop a clean and reliable transfer technique. The transfer techniques using PDMS and PMMA are two methods mainly adopted by researchers [28-30]. Fig. 2.10 shows the process flow of transferring graphene from Cu foil using PDMS. Since the adhesion between PMMA and graphene is stronger than that between Cu foil and graphene, graphene will be attached to PDMS after the removal of Cu foil physically or chemically. Then the PDMS/graphene layer is transferred to the desired substrate and the PDMS is dissolved in a solution of TBAF: NMP (mixing ratio of 10: 1) at room temperature for 24 hours [28]. Fig. 2.11 illustrates the process flow by PMMA. The wet process is usually used so briefly discussed here. A PMMA layer is first spun onto the graphene on Cu foil sample. Then the sample is dipped in the Cu etching solution ($FeCl_3$ or CuCl) to remove the Cu foil. The graphene/PMMA layer is now floating on the solution surface due to surface

tension. This layer is then transferred to DI water a few times to clean off. The desired substrate is then dipped into the ending clean DI to scoop up the floating layer and leave it to dry in air. After the sample is completely dried off, the top PMMA layer is removed by soaking in acetone.

2.3.3. Plasma enhanced chemical vapor deposition techniques

The usage of plasma enhanced chemical vapor deposition (PECVD) to produce graphene is a relatively straightforward and simple technique, thus many research groups start their studies since the first successful report in 2004 [31-36].

Similar to the CVD growth on metals, a gas mixture of CH_4 and H_2 is used as precursors. The synthesis can be on a variety of substrates (e.g. Si, SiO_2, Al_2O_3, etc.) without any surface preparation or catalyst. According to Zhu et al. [34], the growth mechanism is as follows: gas species from CH_4 diffuse around the substrate surface and find energy favored sites to deposit while the atomic hydrogen attacks and etches away carbon species. Growth conditions are tuned to balance these two processes to get monolayer or multilayer graphene.

PECVD method provides a simple way to synthesis graphene with arbitrary thickness on any type of substrate. However, more efforts should be made to improve its controllability over the thickness of the as-grown graphene layer. Also, the uniformity of the synthesized graphene should be better engineered.

2.3.4. Thermal decomposition of SiC

In this technique, graphene is synthesized by thermal decomposition of SiC and graphene forms at the surface of SiC surface. Fig. 2.13 shows the process steps. The SiC substrate is first annealed at 750 ^{o}C in small Si flux to remove the surface contamination and form a Si-rich surface. This is followed by high temperature annealing at 1150 ^{o}C then 1280 ^{o}C to decompose SiC. In this step, Si atoms desorb from the surface, and the C atoms left behind would form bonds and eventually monolayer or few-layer graphene.

Similar to the PECVD method, the thermal decomposition of SiC technique looks attractive due to its simplicity. However, before it can be adopted for industry production, better controllability of the film thickness and reproducibility are the issues to be solved. Also, the cost is high since SiC substrates are costly.

2.4. Applications of graphene

Due to its attractive properties in electrical, thermal, and mechanical aspects, graphene has drawn attentions in wide range of applications including transparent electrodes, field effect transistors, field emission, and graphene based sensors, etc. In this section, the applications of graphene is briefly reviewed.

2.4.1. Transparent electrodes

Since graphene is a one atomic layer material with high transparency (monolayer graphene only absorbs 2.3% of white light [38]), it is believed to be an excellent candidate for transparent electrode applications of solar cells, LCD displays, etc [39-41]. Compared to the widely used ITO as transparent conductive coatings, graphene has better conductivity, flexibility, mechanical strength, and meanwhile it is less costly.

2.4.2. Field effect transistors

Graphene is expected to be used in field effect transistors (FETs) due to its extremely high electron and hole mobilities and perfect ballistic transport properties [1]. However, the semi-metal characteristic of graphene, i.e. zero band gap makes it unsuitable to make FET devices. It is found that graphene nanoribbons (GNRs) provide tunable band gaps with high carrier mobility and switch speed which is perfect for FETs [42-46]. Although many reports have demonstrated the excellent performance of GNR based FETs, difficulties including processing, doping, graphene quality issues still remain. This requires more efforts to improve in order to realize commercial logic devices.

2.4.3. Field emission

Field emission (FE) is the emission of electrons induced by an electrostatic field. The most common context is field emission from a solid surface or tip into vacuum. The sharper the tip is, the larger the FE enhancement factor [47]. Monolayer for few-layer graphene can be used to cover the tip surface to improve the field enhancement. Many research groups have reported their works of making FE devices with graphene [48-50].

2.4.4. Graphene based sensors

One of the most promising applications of graphene is in sensors. The utilization of graphene in sensors typically use the change of graphene's electrical conductivity as an indication to sense the change of environment.

The electrical conductivity of graphene is very sensitive to doping and strain. If certain gas or bio molecules are absorbed on the graphene surface, the electrical conductivity of graphene will change accordingly because the absorbents will act as donors or acceptors. Through careful design of the device, relationship between the concentration of detected gases or molecules and the electrical conductivity of graphene can be found, thus the device can be used as sensors [51-53]. One the other hand, the electrical conductivity of graphene is very sensitive to strains [54]. Microelectromechanical system (MEMS) devices with suspending GR element or graphene/polymer hybrid platforms can be used for pressure sensing applications [55, 56]. Due to the strain induced by bending or pressure change, the electrical conductivity of graphene can be measured then mapped to pressure.

2.5. Graphene for ESD protection

It has been mentioned that the excellent properties of graphene make it a wonderful candidate for ESD protection applications, i.e. high electrical conductivity for less heat generation and fast high current discharge during the ESD event, high thermal conductivity for quick heat dissipation, and strong mechanical strength for device rigidity. All these superior properties of graphene guarantee a robust and reliable graphene based ESD protection device with long life time. However, similar to the issues with graphene based FETs, the zero band gap of graphene makes it hard to be used in ESD protection device because the switch-on behavior is the crux of the ESD protection operation. GNR structures with an finite band gap can be considered but this type of device will inevitably

suffer from leakage issues like the traditional ESD devices. Therefore, a novel device structure is needed to realize a graphene-based ESD protection device.

2.6. Figures

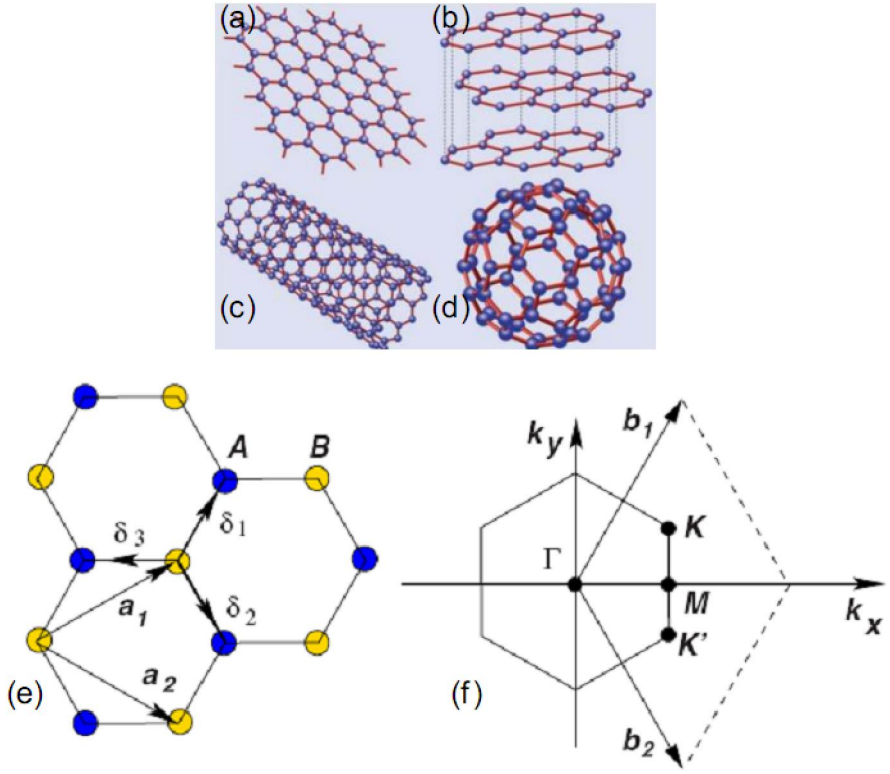


Fig. 2.1 Allotropes of carbon including (a) graphene, (b) graphite, (c) carbon nanotubes, and (d) fullerenes; (e) The hexagonal lattice structure of graphene in real space; (f) Brillouin zone (BZ) with Dirac points located at K and K'. (After [4])

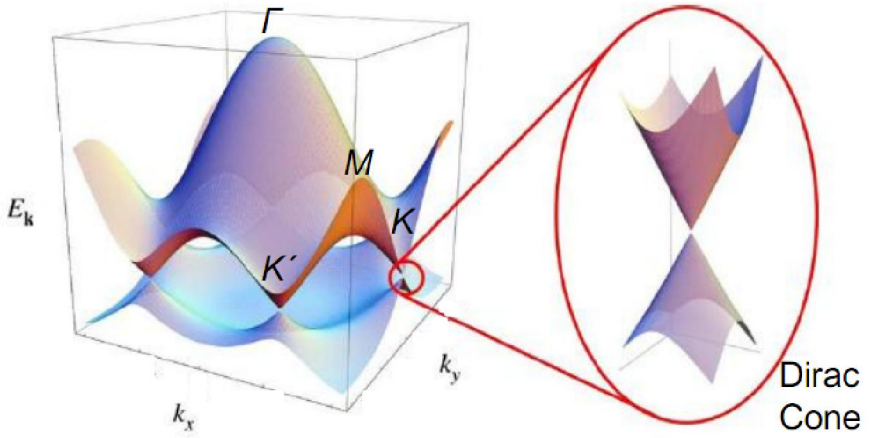


Fig. 2.2 Band structure of graphene with Dirac points (K and K') and a linear E-k dispersion relationship commonly named as Dirac cone.

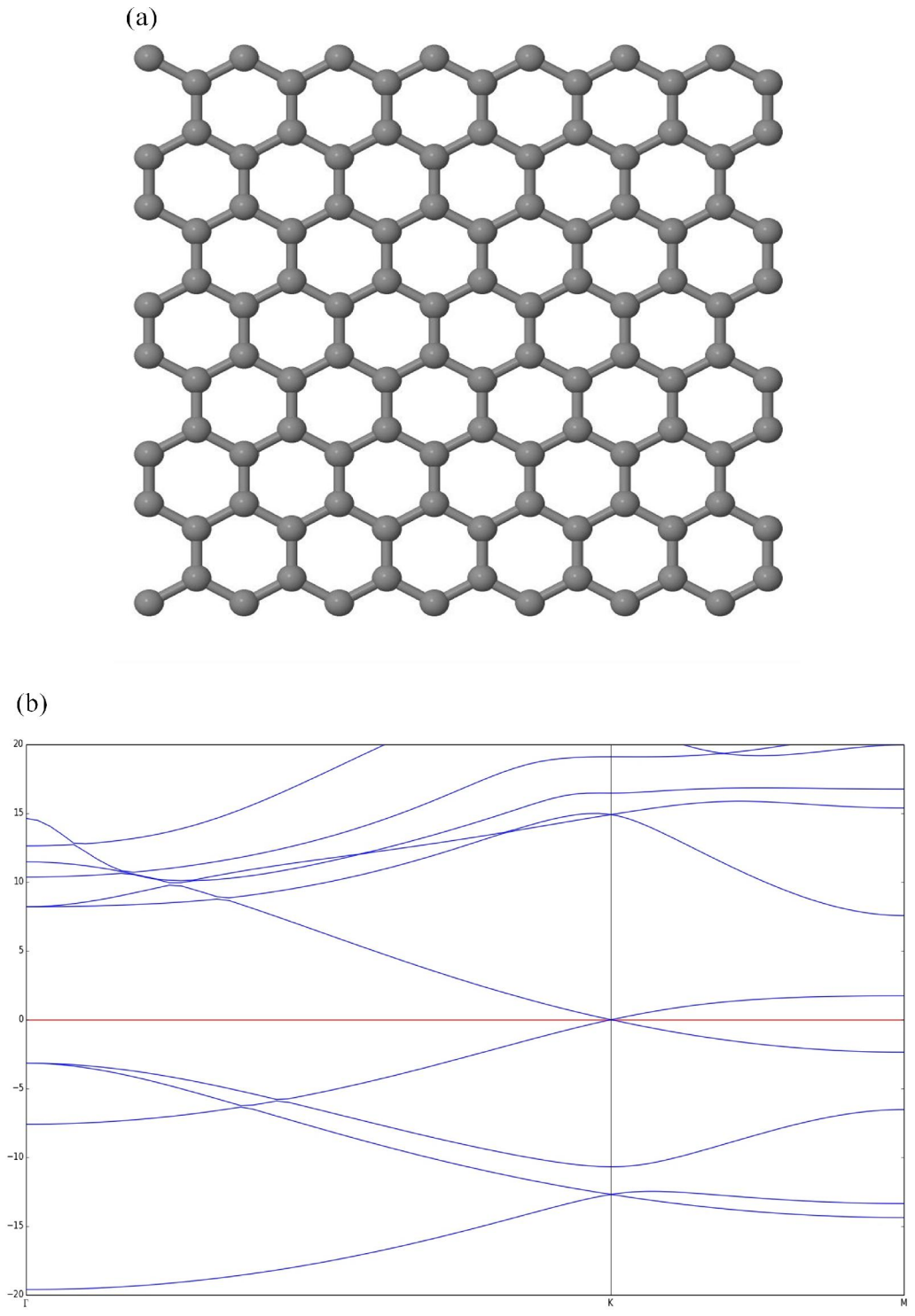
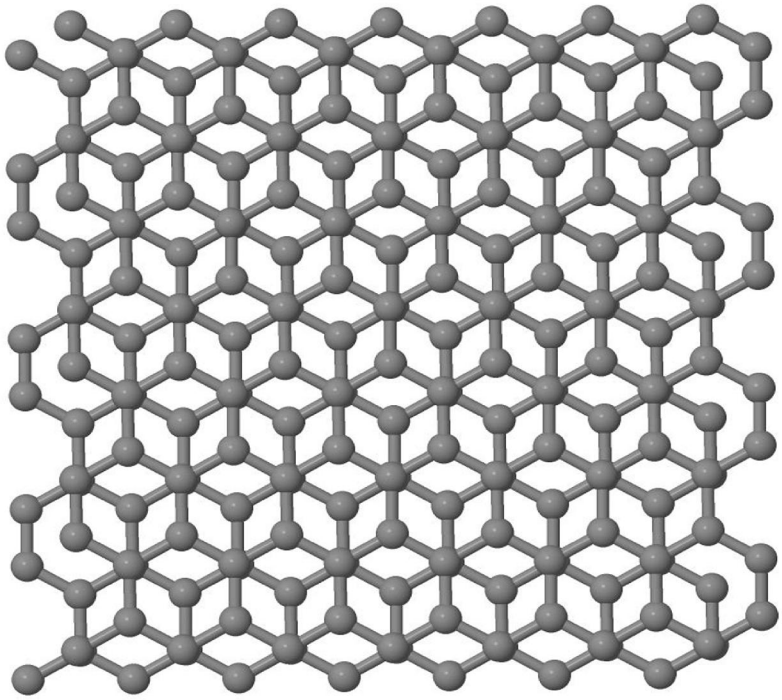


Fig. 2.3 Lattice structure of monolayer pristine graphene (a) and its band structure (b).

(a)



(b)

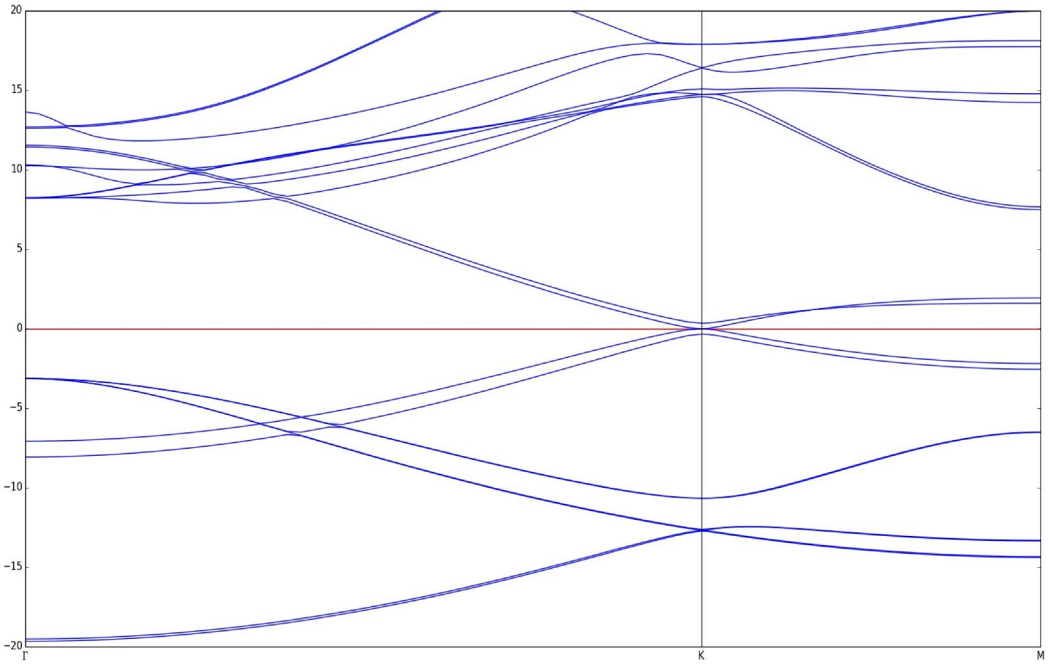


Fig. 2.4 Lattice structure of bilayer pristine graphene (a) and its band structure (b).

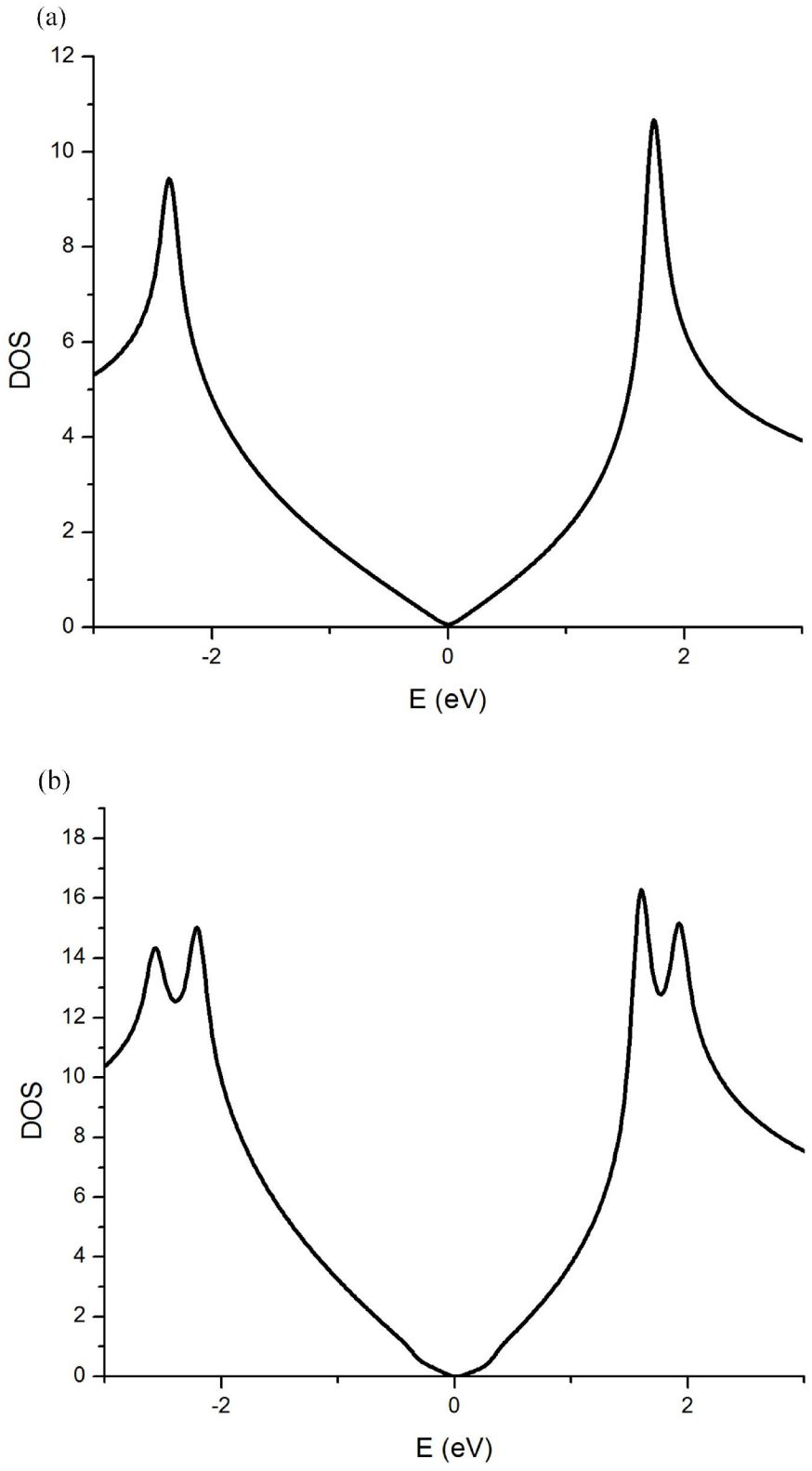


Fig. 2.5 DOS of (a) pristine monolayer graphene, and (b) bilayer graphene.

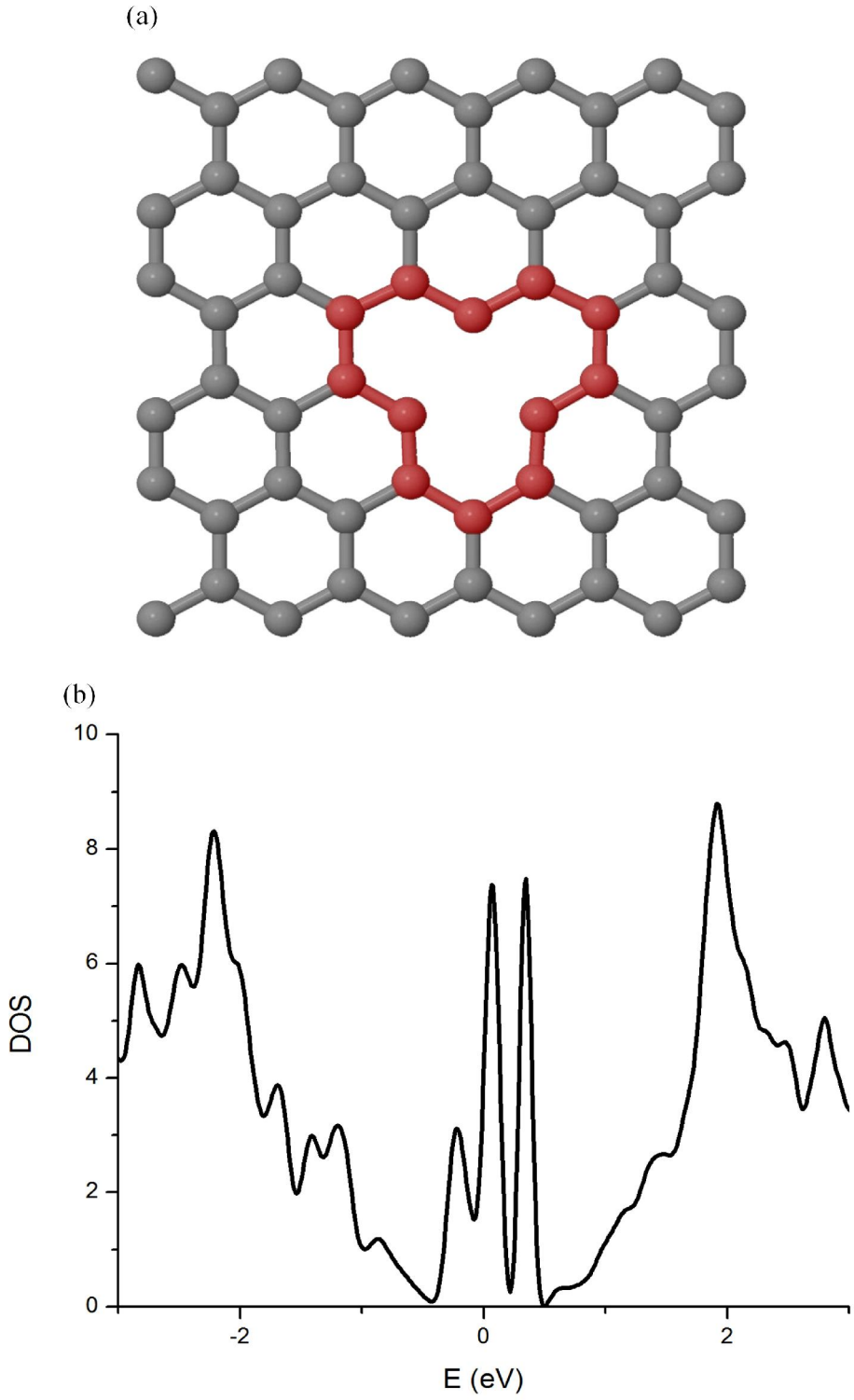


Fig. 2.6 (a) Lattice structure of defective graphene with a vacancy, and (b) its corresponding DOS.

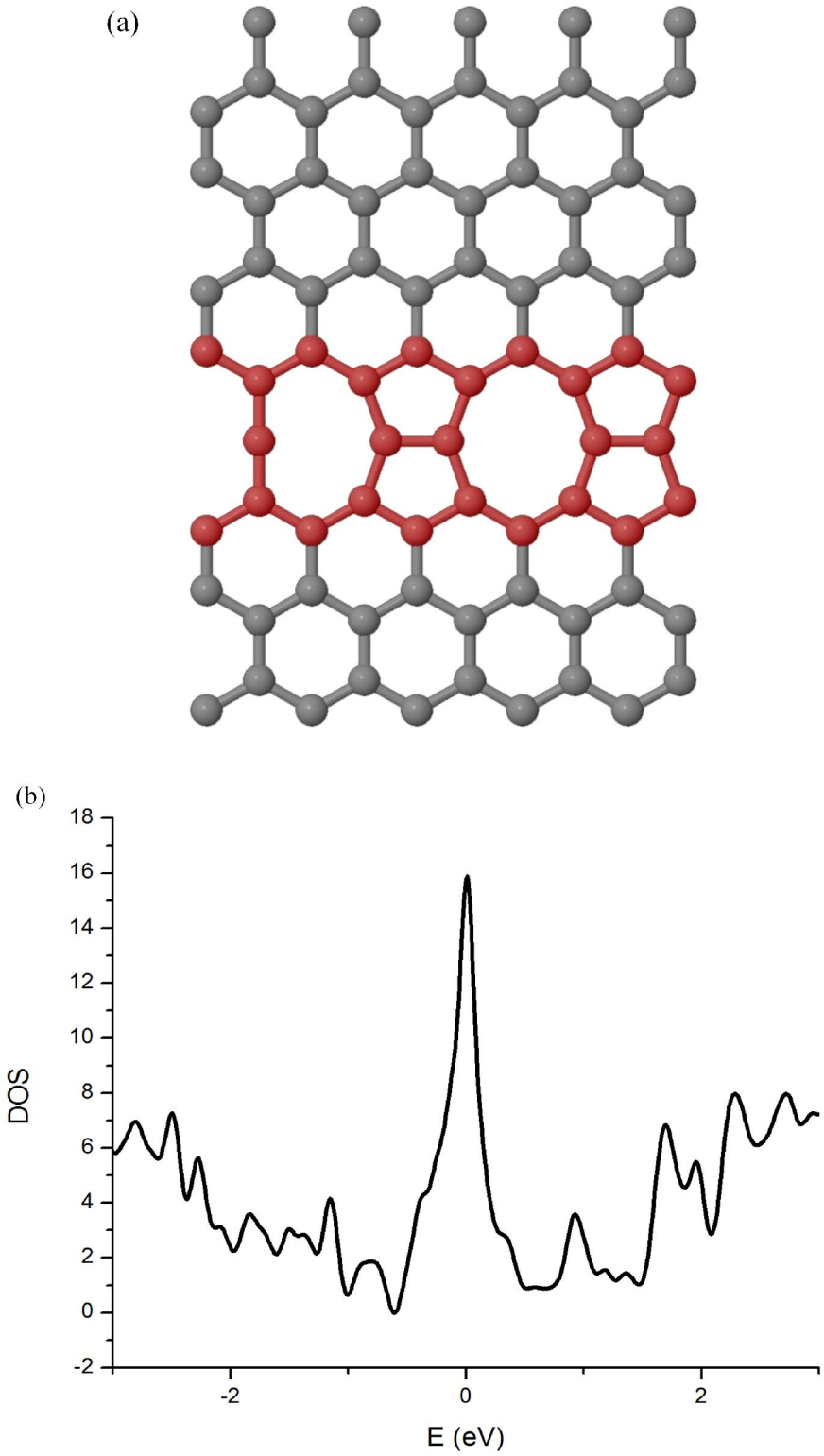


Fig. 2.7 (a) Lattice structure of defective graphene with a vacancy, and (b) its corresponding DOS.

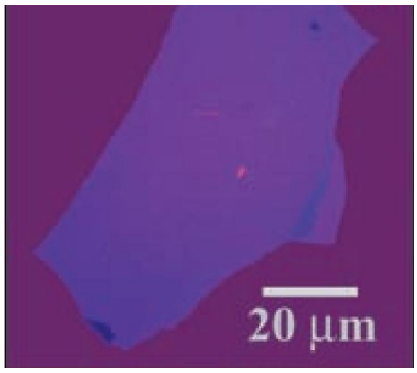


Fig. 2.8 A multilayer graphene flake prepared by mechanical exfoliation technique. (After [1])

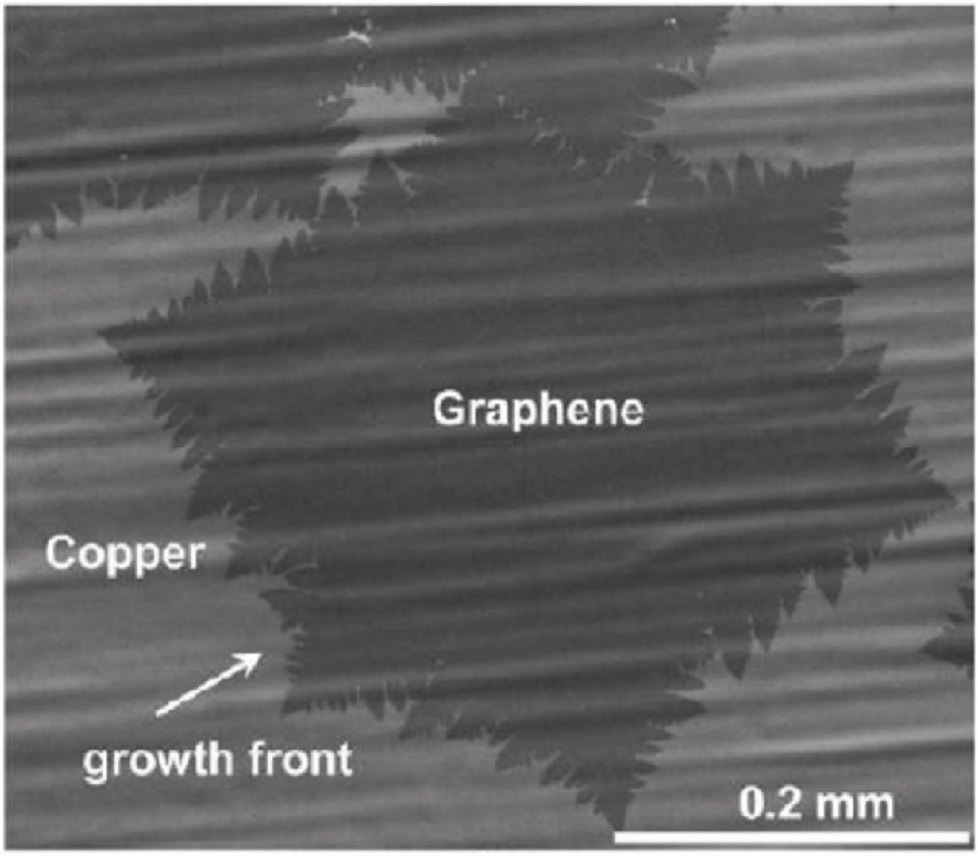


Fig. 2.9 CVD monolayer graphene grown on Cu. (After [27])

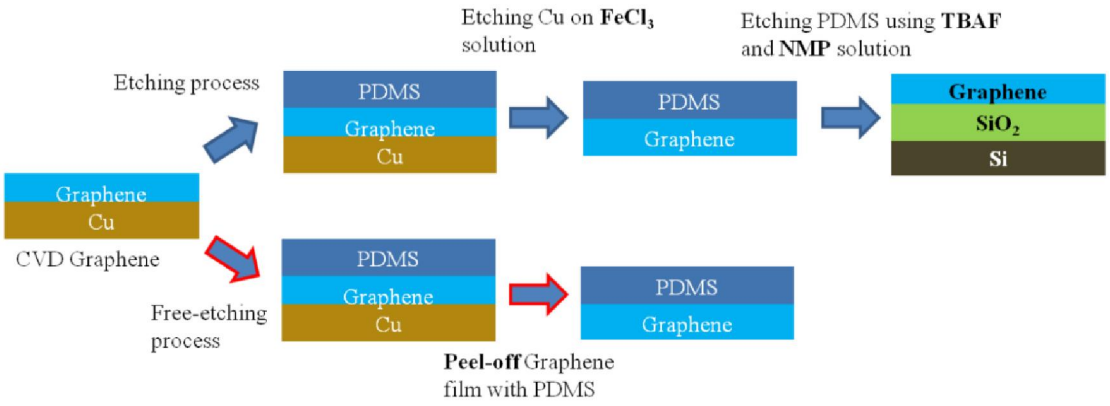


Fig. 2.10 Schematic diagram of the processes used for transferring graphene from copper foils to target substrates using PDMS. (After [28])

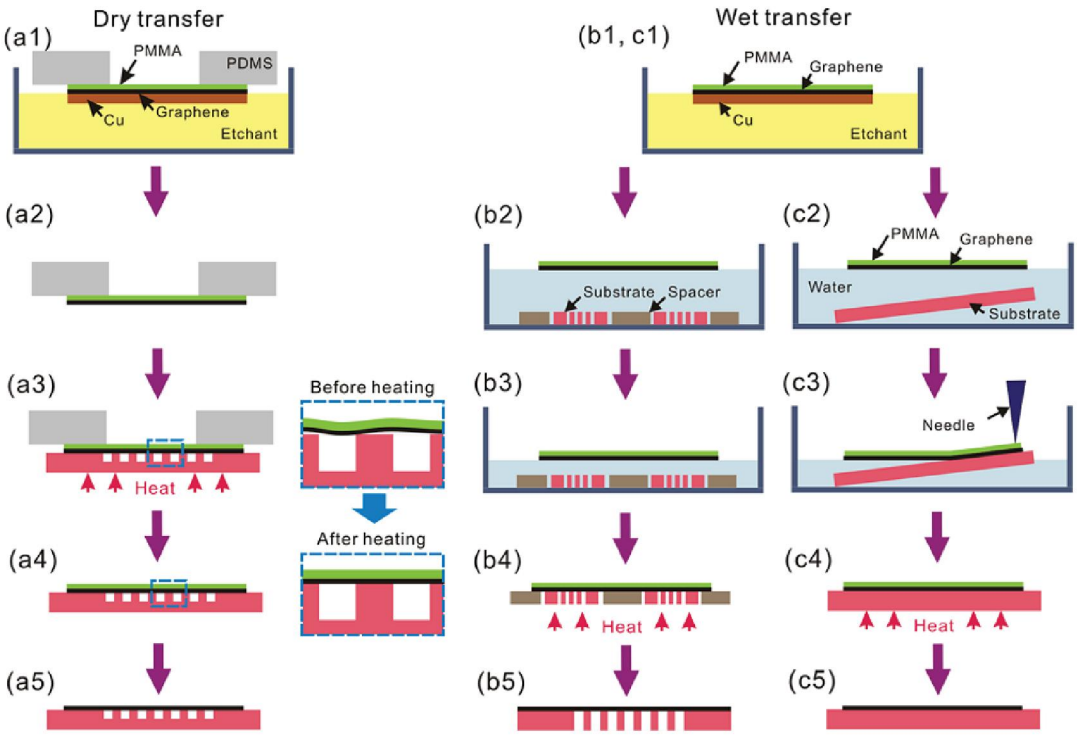


Fig. 2.11 Schematic diagram of the processes used for transferring graphene from copper foils to target substrates using PMMA. (After [30])

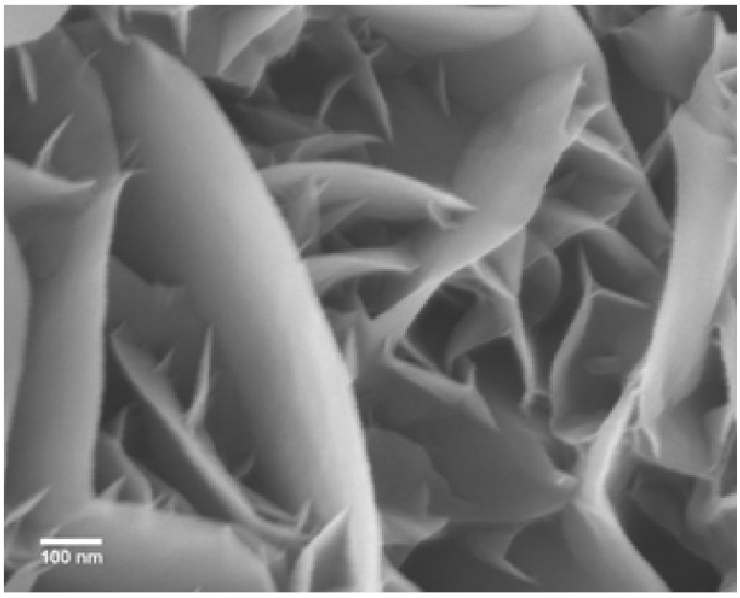


Fig. 2.12 SEM image of multilayer graphene grown on Si by PECVD method. (After [36])

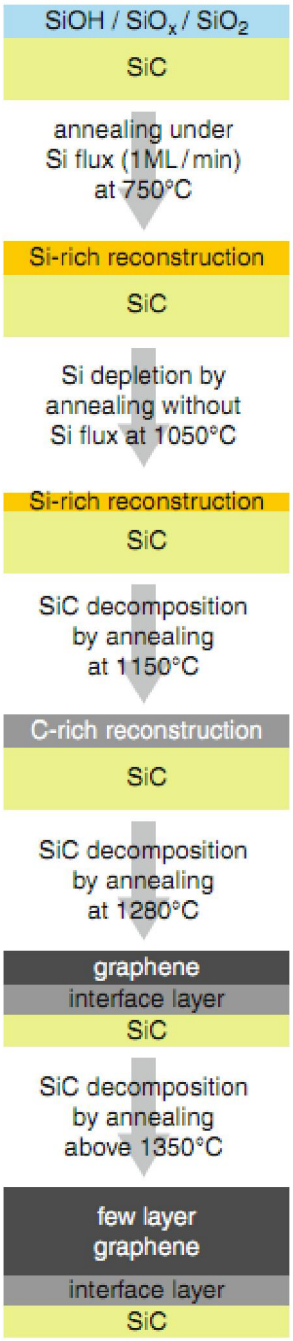


Fig. 2.13 Process flow of graphene synthesis using thermal decomposition of SiC method. (After [37])

2.7. Reference

1. K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, and A. A. Firsov, Science, 306, 666 (2004).
2. Y. Zhang, Y. -W. Tan, H. L. Stormer, and P. Kim, Nature, 438, 201 (2005).
3. Y. M. Lin, C. Dimitrakopoulos, K. A. Jenkins, D. B. Farmer, H. Y. Chiu, A. Grill, and P. Avouris, Science, 327, 662 (2010).
4. A. H. Castro Neto, F. Guinea, N. M. R. Peres, K. S. Novoselov, and A. K. Geim, Reviews of Modern Physics, 81, 109 (2009).
5. Aziz N. Mina, Attia A. Awadallah, Adel H. Phillips, and Riham R. Ahmed, Journal of Physics: Conference Series, 343, 012076 (2012).
6. Davood Fathi, Journal of Nanotechnology, 2011, 471241 (2011).
7. Alessandro Cresti, Norbert Nemec, Blanca Biel, Gabriel Niebler, Francois Triozon, Gianaurelio Cuniberti, and Stephan Roche, Nano Research, 1, 361 (2008).
8. S. Reich, J. Maultzsch, C. Thomsen, and P. Ordejon, Physical Review B, 66, 035412 (2002).
9. V. Blum, R. Gehrke, F. Hanke, P. Havu, V. Havu, X. Ren, K. Reuter, and M. Scheffler, Computer Physics Communications, 180, 2175 (2009).
10. J. P. Perdew, K. Burke, and M. Ernzerhof, Physical Review Letters, 77, 3865 (1996).
11. A. Tkatchenko, and M. Scheffler, Physical Review Letters, 102, 073005 (2009).
12. McCann E., and Falko V. I., Physical Review Letters, 96, 086805 (2006).

13. Yuliang Mao, G Malcolm Stocks, and Jianxin Zhong, New Journal of Physics, 12, 033046 (2010).
14. B. Lang, Surface Science, 53, 317 (1975).
15. Wonbong Choi , Indranil Lahiri , Raghunandan Seelaboyina, and Yong Soo Kang, Critical Reviews in Solid State and Materials Sciences, 35, 71 (2010).
16. L. M. Viculis, J. J. Mack, and R. B. Kaner, Science, 299, 1361 (2003).
17. Shelton J. C., Patil H. R., and Blakely J. M., Surface Science, 43, 493 (1974).
18. Grabke H. J., Paulitschke W., Tauber G., Viefhaus H., Surface Science, 63, 377 (1977).
19. Hamilton, J. C., and Blakely, J. M., Surface Science, 91, 119 (1980).
20. A. N. Obraztsov, E. A. Obraztsova, A. V. Tyurnina, and A. A. Zolotukhin, Carbon, 45, 2017 (2007).
21. Xuesong Li, Weiwei Cai, Jinho An, Seyoung Kim, Junghyo Nah, Dongxing Yang, Richard Piner, Aruna Velamakanni, Inhwa Jung, Emanuel Tutuc, Sanjay K. Banerjee, Luigi Colombo, Rodney S. Ruoff, Science, 324, 1312 (2009).
22. Phaedon Avouris, and Christos Dimitrakopoulos, Materials Today, 15, 86 (2012).
23. Yi Zhang, Lewis Gomez, Fumiaki N. Ishikawa, Anuj Madaria, Koungmin Ryu, Chuan Wang, Alexander Badmaev, and Chongwu Zhou, Physical Chemistry Letters, 1, 3101 (2010).
24. Qingkai Yu, Jie Lian, Sujitra Siriponglert, Hao Li, Yong P. Chen, and Shin-Shem Pei, Applied Physics Letters, 93, 113103 (2008).
25. Alfonso Reina, Xiaoting Jia, John Ho, Daniel Nezich, Hyungbin Son, Vladimir Bulovic, Mildred S. Dresselhaus, and Jing Kong, Nano Letters, 9, 30 (2009).

26. Shanshan Chen, Weiwei Cai, Richard D. Piner, Ji Won Suk, Yaping Wu, Yujie Ren, Junyong Kang, and Rodney S. Ruoff, Nano Letters, 11, 3519 (2011).
27. Xuesong Li, Carl W. Magnuson, Archana Venugopal, Rudolf M. Tromp, James B. Hannon, Eric M. Vogel, Luigi Colombo, and Rodney S. Ruoff, Journal of the American Chemistry Society, 133, 2816 (2011).
28. P. J. Ko, H. Takahashi, S. Koide, H. Sakai, T. V. Thu, H. Okada, and A. Sandhu, Journal of Physics: Conference Series, 433, 012002 (2013).
29. Donglin Ma, Yanfeng Zhang, Mengxi Liu, Qingqing Ji, Teng Gao, Yu Zhang, and Zhongfan Liu, Nano Research, 6, 671 (2013).
30. Ji Won Suk, Alexander Kitt, Carl W. Magnuson, Yufeng Hao, Samir Ahmed, Jinho An, Anna K. Swan, Bennett B. Goldberg, and Rodney S. Ruoff, ACS Nano, 5, 6916 (2011).
31. J. J. Wang, M. Y. Zhu, R. A. Outlaw, X. Zhao, D. M. Manos, and B. C. Holoway, Applied Physics Letters, 85, 1265 (2004).
32. J. J. Wang, M. Y. Zhu, R. A. Outlaw, X. Zhao, D. M. Manos, and B. C. Holoway, Carbon, 42, 2867 (2004).
33. M. Hiramatsu, K. Shiji, H. Amano, and M. Hori, Applied Physics Letters, 84, 4708 (2004).
34. M. Zhu, J.Wang, B. C. Holloway, R. A. Outlaw, X. Zhao, K. Hou, V. Shutthanandan, and D. M. Manos, Carbon, 45, 2229 (2007).
35. C. Wang, S. Yang, Q. Wang, Z. Wang, and J. Zhang, Nanotechnology, 19, 225709 (2008).

36. A. Malesevic, R. Kemps, L. Zhang, R. Erni, G.van Tendeloo, A. Vanhulsel, and C. van Haesendonck, Journal of Optoelectronics and Advanced Materials, 10, 2052 (2008).
37. W. Choyke, H. Matsunami, G. Pensl, Recent Major Advances in SiC, Springer Scientific, Berlin, Heidelberg, New York, 2003.
38. R. R. Nair, P. Blake, A. N. Grigorenko, K. S. Novoselov, T. J. Booth, T. Stauber, N.M. R. Peres, and A. K. Geim, Science, 320, 1308 (2008).
39. Keun Soo Kim, Yue Zhao, Houk Jang, Sang Yoon Lee, Jong Min Kim, Kwang S. Kim, Jong-Hyun Ahn, Philip Kim, Jae-Young Choi, and Byung Hee Hong, Nature, 457, 706 (2009).
40. J. Wu, H. A. Becerril, Z. Bao, Z. Liu, Y. Chen, and P. Peumans, Applied Physics Letters, 92, 263302 (2008).
41. X. Wang, L. Zhi, and K. Mullen, Nano Letters, 8, 323 (2008).
42. V. Barone, O. Hod, and G. E. Scuseria, Nano Letters, 6, 2748 (2006).
43. D. A. Areshkin, D. Gunlycke, and C. T.White, Nano Letters, 7, 204 (2007).
44. Y. W. Son, M. L. Cohen, and S. G. Louie, Pysical Review Letters, 97, 216803 (2006).
45. K. Nakada, M. Fujita, G. Dresslhaus, and M. S. Dresselhaus, Physical Review B, 54, 17954 (1996).
46. M. Y. Han, B. Ozyilmaz, Y. B. Zhang, and P. Kim, Physical Review Letters, 98, 206805 (2007).

47. Ke Sun, Wei Zhang, Biyun Li, Jae Young Lee, Ya-Hong Xie, Thomas Schroeder, Jens Katzer, Xinyu Wei, and Thomas P. Russell, IEEE Transactions on Nanotechnoloty, 11, 999 (2012).
48. Z. S. Wu, S. Pei, W. Ren, D. Tang, L. Gao, B. Liu, F. Li, C. Liu, and H. M. Cheng, Advanced Materials, 21, 1756 (2009).
49. G. Eda, H. E. Unalan, N. Rupesinghe, G. A. J. Amartunga, and M. Chhowalla, Applied Physics Letters, 93, 233502 (2008).
50. S. Watcharotone, R. S. Ruoff, and F. H. Read, Physics Procedia, 1, 71 (2008).
51. C. Shan, H. Yang, J. Song, D. Han, A. Ivaska, and L. Niu, Analytical Chemistry, 81, 2378 (2009).
52. J. D. Fowler,M. J. Allen, V. C. Tung, Y. Yang, R. B. Kaner, and B. H. Weiller, ACS Nano, 3, 201 (2009).
53. S. Alwarappan, A. Erdem, C. Liu, and C. Z. Li, Journal of Physical Chemistry C, 113, 8853 (2009).
54. Xue-Wen Fu, Zhi-Min Liao, Jian-Xin Zhou, Yang-Bo Zhou, Han-Chun Wu, Rui Zhang, Guangyin Jing, Jun Xu, Xiaosong Wu, Wanlin Guo, and Dapeng Yu, Applied Physics Letters 99, 213107 (2011).
55. Xiao Li, Rujing Zhang, Wenjian Yu, Kunlin Wang, Jinquan Wei, Dehai Wu, Anyuan Cao, Zhihong Li, Yao Cheng, Quanshui Zheng, Rodney S. Ruoff, and Hongwei Zhu, Scientific Reports, 2, 870 (2012).
56. A.D. Smith, S. Vaziri, A. Delin, M. Ostling, and M.C. Lemme, Ultimate Integration on Silicon (ULIS), 21 (2012).

Chapter 3. A Novel Electromechanical Suspended Graphene Ribbon Electrostatic Discharge Device

3.1. Device structure and working mechanism

As mentioned in previous chapters, an innovative graphene-based electromechanical device structure is needed for next generation ESD protection. The proposed device structure is shown in Fig. 3.1 (a). The graphene ribbon (GR) is suspended on the $Si_3N_4/SiO_2/Si$ trenched substrate. The Si substrate is heavily doped. When GR is in its original suspending position, there is no conducting path between the top and back metal pad, and the device is in "OFF" state. When a bias is applied to the device, the GR will be pulled towards the bottom by the electrostatic force. If the mechanical restoring force is strong enough to balance the electrostatic force, the GR can bend and stay stable in an equilibrium position. If the bias is large enough, the GR will be pulled down and collapse with the bottom heavily doped Si, thus a conducting path is formed and the device is in "ON" state [Fig. 3.1 (b)]. The bias which can pull the GR down is the trigger voltage of the ESD device. The inset of Fig. 3.1 (b) shows the expected working I-V curve of the device. Since there is no touching between GR and Si bottom before the device is turned on, zero leakage can be realized in principle.

As an ESD device, the FOM (I_{t2}/C_{ESD}) of the proposed device structure needs to be reviewed. Compared to the conventional ESD devices, the parameters are simple and straightforward here: I_{t2} is the breakdown current of GR, while C_{ESD} is the capacitance between GR and Si substrate. It will be discussed in section 3.7 that for a device made of monolayer GR (L=9 μm, W=5 μm, d= 1 μm), I_{t2} is ~10 mA. As to the parasitic

capacitance C_{ESD}, it can be calculated as follows: $C_{ESD}= \varepsilon A/d= 8.854x\ 10^{-12}x\ 9x\ 10^{-6}x\ 5x\ 10^{-6}/\ 1x10^{-6}= 0.39$ fF. Therefore, the proposed device FOM= 10/0.39= 26 mA/fF, which is comparable to the best performance of conventional ESD devices. It is worth noting that I_{t2} can be further increased by appropriate doping and/or using multilayer graphene to improve the current carrying capability. Moreover, appropriate IC packaging techniques may keep the device away from oxygen environment which is believed to delay the breakdown of graphene. Details will be discussed in section 3.7.

During the pulling down process of GR, there exists a critical voltage ($V_{pull\text{-}in}$) beyond which no stable state is present for the GR to stay in, i.e. the electrostatic force and mechanical restoring force can never balance beyond this point. The corresponding position of GR is called the critical position which is about one third of the trench depth as shown in Fig. 3.2 (a). When $V_{pull\text{-}in}$ is reached, GR is bent to the critical position. If the bias keeps increasing, the GR will be suddenly pulled down and collapse with the trench bottom. This is called pull-in phenomenon. The physics behind this pull-in can be explained by force balance analysis. It's easy to understand that the mechanical restoring force F_M is proportional to -d (d is the trench depth), while the electrostatic force F_E is proportional to $1/d^2$. This relationship can be seen in Fig. 3.2 (b). At low voltage level, there are two points of intersection between the two curves. But while one of these two equilibrium states is stable, the other one is unstable. Increasing voltage may result in new equilibrium states. At pull-in, the two curves intersect at one point referred to as pull-in state which is meta-stable. For voltages higher than $V_{pull\text{-}in}$, there is no intersect between the two curves so no equilibrium state is present [1, 2].

3.2. Device fabrication

The process flow for fabricating the suspended GR ESD device is shown in Fig. 3.3. First, thermal SiO_2 with desired thickness is grown on heavily doped Si substrate. Second, thin layer of LPCVD Si_3N_4 is grown on top of SiO_2 to form a hard mask for the final HF vapor etching. This is followed by thermal annealing at 1100 ^oC in air for 1 hour to release the residue strain at the interface [Fig. 3.3 (a)]. This step is very crucial because in the final step of HF vapor etching, the residue strain will render ultra fast etching rate of HF vapor at interface, which will lead to Si_3N_4 layer being peeled off. Third, photolithography and plasma etching are used to etch away the Si_3N_4 in the area where trenches will be formed in the end [Fig. 3.3 (b)]. Then CVD grown graphene is transferred onto the trenched substrate and patterned into individual GRs by photolithography and O_2 plasma etching [Fig. 3.3 (c)]. It is worth mentioning that during the drying off after graphene transfer, due to the high surface tension of water, graphene will be dragged down and form good contact with the trenched surface. If Si_3N_4 layer is too thick, graphene may be partially suspended or even cracking will form during this step. Both of these two situations will result in device failure. Next, the metal pads consisting of Ti/Pd/Au (0.5/30/50 nm) are deposited by e-beam evaporation and lift-off processes [Fig. 3.3 (d)]. At last, HF vapor etching (HFVE) is used to etch away the exposed SiO_2 layer to release the suspended GR structure [Fig. 3.3 (e)].

Compared to other existing processing methods to make suspended GR structures [3-6], the process flow we use is more reliable and thus the device fabrication yield is higher: (i) in the conventional fabrication techniques, there is no mask to protect SiO_2 area which is not supposed to be etched during BOE etching, and due to the fast etching

in between graphene/SiO_2 interface, the device structure became quite unreliable. We use Si_3N_4 as a hard mask to protect the non-affected area, and since the etching rate of Si_3N_4 is negligibly slow, the uncertainty caused by fast interface etching is resolved; (ii) HF vapor etching is used instead of BOE etching. As graphene is a mono-atomic layer two dimensional material, it is not easy to make suspending structures without breaking. The survival rate of the devices is usually not high due to the liquid turbulent environment and large surface tension of water [5, 6]. And critical point dryer needs to be used which adds another level of complexity to the process. In the contrary, HF vapor etching is much simpler to handle and there is no liquid involved in the process which prevents GR from breaking during the release process.

An AMMT HF vapor etching system is used for the SiO_2 etching. In vapor etching, HF vapor is generated by evaporation at room temperature and react with the exposed "to be etched" surface. The reactions between HF and SiO_2 are as follows:

$$SiO_2 + 2H_2O \rightarrow Si(OH)_4 \; Si(OH)_4 + 4HF \rightarrow SiF_4 + 4H_2O$$

The etching product SiF_4 is a volatile compound and will desorb easily from the surface. It can be seen from the reactions above, water is involved on both sides of the reactions. Therefore, in order to avoid water from concentrating on the surface to damage the suspended GR structure, the wafer is slightly heated to evaporate excess wafer. However, too much heating will evaporate all the water from the surface, and no water is available for the reaction to proceed. As a result, the etching rate drops quickly as the wafer heating temperature increases. So careful optimization of the etching temperature is very critical for the HFVE process to be successful. A etching temperature of 15^{o}C is used in the fabrication process. Also, it is worth noting that there is an "incubation time" of the

HFVE process, i.e. during the beginning ~19 minutes, there is negligible etching taking place at the SiO_2 surface, which is probably due to the lack of the presence of water on the surface. After this incubation time, enough water is accumulated and etching rate begins to ramp up very quickly and can reach as high as 160 nm/min. The etching rate curve is shown in Fig. 3.4.

Fig. 3.5 shows SEM image of the suspended GR ESD device as fabricated.

3.3. Direct current characterization

Direct current (DC) electrical measurements are conducted to characterize the device performance. Different test set-ups are used to visualize different aspects of the device behavior. In this section, the results using two DC measurement methods are discussed. Finite Element Simulations are also carried out using COMSOL to compare with the experimental results.

3.3.1. Two-terminal direct current measurement

The "switch-on" behavior is the crux of any ESD device. In order to visualize this behavior of the proposed suspended GR ESD device, two-terminal DC measurement is conducted. The measurement scheme is same as Fig. 3.1 (a). As can be seen in the figure, a bias is applied between GR and heavily doped Si substrate which is the back gate. As has been discussed in the previous section, as the bias increases, GR will be bent and eventually collapse and touch the bottom at $V_{pull\text{-}in}$. A conducting path is then formed from the graphene/Si contact. Therefore, $V_{pull\text{-}in}$ is the trigger voltage of the device.

Devices with different dimensions are fabricated and measured to study the effect of device geometry. The trench depth (d= 350/550/850 nm) and length of GR (L= 7/10/15/20 μm) are taken as two variables to see their effect on the trigger voltage. Fig. 3.6 shows the turn-on behavior of devices with different trench depths. GR length of the tested devices is fixed at 20 μm. The current compliance is set to be 0.1 mA to avoid the device from breaking down. A sharp turn-on behavior can be clearly seen from the I-V curves for all devices which is desired for an ESD device. The turn-on voltages are about 3.9, 7.8, and 16 V for d= 350/550/850 nm respectively, from which we may extract the relationship of $V_{pull\text{-}in} \propto d^{3/2}$, which is consistent with literature [7]. Similarly, Fig. 3.7 shows the turn-on behavior of devices with different GR lengths. The trench depth of the tested devices is fixed at 350 nm. The turn-on voltages are about 3.9, 7.2, 15.2, and 30 V for L= 7/10/15/20 μm respectively. We can extract the relationship of $V_{pull\text{-}in} \propto 1/L^2$, which also agrees with the reported works [3, 7].

If same measurements were repeated one the same device, similar turn-on behavior can be observed but with a decreasing trigger voltage. This pointed out two things: (1) GR will not stick to the bottom after the bias is gone. This is because the mechanical restoring force is dragging it back. This also tells us that the Si_3N_4 layer cannot be too thick, otherwise, after graphene transfer the graphene layer will not form good contact with the trenched surface during the drying off process due to the mechanical restoring force and will be partially suspended as mentioned in section 3.2. (2) The decreasing trigger voltage may be a potential reliability problem for the proposed device. This might be due to slight sliding of GR towards the bottom, plastic deformation

of GR, or crack formation due to poor GR quality. More research should be done to find out the reasons.

From the results above, we may conclude that the proposed suspended GR ESD device may work as a switch with tunable turn-on voltage and sharp turn-on property, which are very crucial for ESD devices. More discussions on trigger voltage will be made in the following sections.

3.3.2. Three-terminal direct current measurement

The turn-on behavior of the suspended GR ESD device has been discussed in the previous section to show the feasibility of the proposed device structure. However, detailed information about the device behavior during bias increase cannot be learnt from two-terminal DC measurement. Therefore, another measurement method is used to study the mechanical shape evolution of GR when increasing bias is applied. The three-terminal DC measurement set up is shown in Fig. 3.8. The purpose of this measurement is to measure the resistance (R) change of GR with increasing back gate bias (V), from which the bias induced charge (ΔQ), the capacitance (C) change, and the bending information of GR can be calculated and extracted. The lateral bias is kept at 5 mV to measure the R of GR. As oppose to the device for two-terminal measurement, there is a thin 50 nm SiO_2 layer intentionally left at the bottom of the trench in order to measure the R of GR after GR is pulled down to the bottom and collapse with heavily doped Si substrate. Since the GR is typically p-doped, when a positive back gate bias is applied, R should increase with increasing V, whereas when a reverse negative back gate bias is applied, R should decrease. The position change of Fermi level is indicated in Fig. 3.9.

COMSOL simulations are carried out to compare with the measurement results. Three pre-defined models in COMSOL Finite Element Simulation package are used in the simulations, which are electrostatic, solid mechanics, and moving mesh models. In the electrostatic model, poisson's equation and equations of Maxwell stress tensor are used to calculate the electrostatic force applied on GR. The mechanical restoring force and shape evolution of GR is taken care of by the solid mechanics model. Since the system is moving all the time due to the deformation of GR, moving mesh model is needed for appropriate meshing for the simulation.

Fig. 3.10 (a) shows the change of R with increasing V (positive back gate bias) for a device with L=20 μm and d= 300 nm. As mentioned before, since GR is pre-p type doped, with increasing positive bias on Si substrate, the Fermi level of GR goes up and R increases slowly. At a certain voltage value, R increases abruptly which indicates the pull-in of GR. The voltage is the $V_{pull\text{-}in}$ which is slightly smaller than the $V_{pull\text{-}in}$ measured from the two-terminal measurement due to the smaller trench depth. The bias induced charge and capacitance of GR can be calculated by the equations as follows:

$$Q = L^2/(R\mu) \qquad \textit{Equation 3.1}$$

$$C = \Delta Q/\Delta V \qquad \textit{Equation 3.2}$$

where L is the length of GR, μ is the mobility of GR. The calculated and simulated results of change of ΔQ and C with increasing V are shown in Fig. 3.10 (b) and (c). Similar to the change of R, ΔQ and C increase slowly at small voltage values then suddenly increase abruptly at $V_{pull\text{-}in}$ indicating that pull-in happens. Since GR is pulled in and collapsed with trench bottom, the gap between GR and Si substrate reaches minimum at this moment. The capacitance reaches its peak value and keeps fixed since then. The

maximum calculated and simulated capacitance are consistent with the value calculated from the geometry of the device. It can be clearly seen from Fig. 3.10 (b) and (c) that the experimental and simulation results fit very well which verify the solidity of the results. On the other hand , if a negative back gate bias is applied instead of positive, R would decrease slowly first then abruptly at $V_{pull\text{-}in}$. ΔQ and C can also calculated using the same method. The change of R, ΔQ, and C with negative back gate bias is shown in Fig. 3.11, which is similar to Fig. 3.10.

Devices with dimensions of L=20 μm, d= 500 nm, and L=20 μm, d= 2 μm are also tested using the same measurement method. The results are similar so not shown here. It worth noting that for the device with trench depth of 2 μm, the trench is so deep that the GR will break at $V_{pull\text{-}in}$ where R increases dramatically [Fig. 3.12 (a)]. But before the breakage, the discussions on shape evolution of GR previously still hold [Fig. 3.12 (b)]. Calculated from the geometry, the average strain on GR after pull-in is ~20% which is smaller than the maximum strain limit of graphene (25%) [8]. So the breakage of GR may be due to non-perfect graphene or non-uniform strain distribution. The COMSOL simulation result reveals that the strain distribution on GR is indeed non-uniform and strain concentrates at the edge regions which is shown in Fig. 3.13 (a). Fig. 3.13 (b) shows the SEM image of GR after test. It can be clearly seen that the breakage happens at the edge region highlighted by red circle.

3.4. Transmission line pulse measurement

Besides the direct current measurements, transmission line pulse (TLP) measurement is also carried out to test the switch behavior of the suspended GR ESD

device. It is of great importance that the proposed device structure can still turn on under TLP testing because an ESD transient is more appropriate to emulate an actual electrostatic shock. According to HBM, an ESD event is characterized by a constant charge discharge via a transient surge but not a constant voltage provided by DC. The rise time (t_r) and duration time (t_d) are critical parameters in TLP to match with HBM. The measurement scheme is same as shown in Fig. 3.1 (a) except that TLP (t_r=10 nm, t_d=100 nm) is used as input instead of DC for HBM emulation.

Devices with fixed trench depth (d=350 nm) and various GR lengths are tested. The results are shown in Fig. 3.14. Similar to the two-terminal DC measurement results, we can see sharp turn-on behavior of the device. The turn-on voltages are about 4, 9, 19 V for L= 20, 15, 10 μm, respectively, which is close to the DC measured $V_{pull\text{-}in}$.

In order to test out the reliability of the device, same measurement is done on an same device for more than 30 times. The device performs similarly without showing device damage. However, similar to the DC measurements, trigger voltage tends to decrease after several times of repeats. More research should be done to study and resolve this reliability problem.

3.5. Key parameters for the design of ESD device

For ESD devices, trigger voltage and response time are two key parameters. In order for the ESD device to work properly as a protection for the core circuit of IC, these two parameters must be designed carefully to match the requirement. In this section, the design of the dimensions of the suspended GR ESD device is discussed based on them.

3.5.1. Trigger voltage

As is know from the previous discussions, the trigger voltage of the suspended GR device is the pull-in voltage of the GR. The pull-in voltage follows the relationship below [7, 9]:

$$V_{pull-in} \sim \sqrt{\frac{Ed^3h^3}{L^4\varepsilon_0}} \qquad \textit{Equation 3.3}$$

where E is the Young's modulus of graphene (1TPa), d is the trench depth, h is the thickness of graphene, L is the length of GR, ε_0 is the vacuum permittivity. As a rule of thumb, the trigger voltage should be designed to be smaller than the breakdown voltage of the core circuit of the IC, so that when a ESD surge comes in, the ESD device can clamp the voltage to a safe level for protection.

3.5.2. Response time

Another key parameter for ESD device is response time (t_r). In order to protect the core circuit, the ESD device must response ultra fast to an ESD event. Modern ESD function requires the response time to be on the order of 10^{-10}~10^{-9} seconds. The response time of the suspended GR device can be calculated from the equations as follows [10]:

$$t_r = 3.67\ (V_{pull\text{-}in}/V_{op}f_0) \qquad \textit{Equation 3.4}$$

$$f_0 = 1.03\sqrt{\frac{E}{\rho}}\frac{h}{L^2} \qquad \textit{Equation 3.5}$$

where V_{op} is the operation voltage, f_0 is the resonance frequency of GR, E is the Young's modulus of graphene, ρ is the density of graphene, h is the thickness of graphene, L is the length of GR. In Equation 3.4, response time t_r is scaled by the factor of $V_{pull\text{-}in}/V_{op}$. This is because the operation of the ESD device is not like a normal oscillator with time constant of $1/f_0$. The GR collapses at the bottom under V_{op} which should be larger than $V_{pull\text{-}in}$. Larger V_{op} renders larger electrostatic force on GR thus larger acceleration, and the moving distance of GR is fixed which is the trench depth. So a faster response time

can be obtained if the device is working under larger V_{op}. It can be seen from the equation that since graphene has ultra large E and small ρ, it is an excellent candidate for making fast response device. The number of graphene layer and length of GR can be designed to meet the requirement of response time. Theoretically, for a monolayer graphene, a GR length of 300 nm may render a response time of ~10^{-9} s.

3.6. Considerations on quantum capacitance

We all know how to calculate the capacitance of a parallel plate capacitor which is made of two parallel metal plates with a layer of dielectric in between. But if one makes a parallel plate capacitor where one or both of the plates has a low density of states, then the capacitance is not given by the normal formula for parallel plate capacitors. Instead, the capacitance is lower, as if there was another capacitor in series. This second capacitance, related to the density of states of the plates, is the quantum capacitance. Since the two capacitance is in series, the smaller one will be dominant in the total capacitance [11].

For perfect monolayer graphene without impurities or defects, the quantum capacitance can be calculated by [12]:

$$C_Q = \frac{2e^2 k_B T}{\pi(\hbar v_F)^2} \ln[2(1+\cosh\frac{eV_{ch}}{k_B T})] \qquad \textit{Equation 3.6}$$

where $V_{ch}= E_F/e$ is the potential of graphene, e is the electron charge, k_B is the Boltzmann constant, T is temperature, ħ is the reduced plank constant, v_F is the Fermi velocity of graphene. When $eV_{ch} >> kT$, the above equation can be reduced to [13]:

$$C_Q \approx e^2 \frac{2}{\pi} \frac{eV_{ch}}{(\hbar v_F)^2} = \frac{2e^2}{\hbar v_F \sqrt{\pi}} \sqrt{n} \qquad \textit{Equation 3.7}$$

where n is the charge carrier density. There are several important information worth noting from the equations above: 1) the quantum capacitance has a minimum value at the Dirac point, and 2) the minimum value is close to zero (0.8 μF/cm^2 thermal induced), 3) it increases linearly with V_{ch} with a slope of 23 μF/cm^2/V.

If we assume the extreme situation, the minimum quantum capacitance could possibly be 0.8 μF/cm^2, which means the trench depth needs to be smaller than 2 nm for the quantum capacitance to be non-negligible. However, in the real case, the graphene is never perfect but with some defects making the quantum capacitance even larger. Therefore, the quantum capacitance is orders of magnitude larger than the normal capacitance, and since the smaller capacitance is dominant in the total capacitance, the quantum capacitance effect can be disregarded.

3.7. Breakdown properties of GR

As the key material for ESD device, the breakdown properties of GR need to be investigated. In this section, systematic characterization and statistical analysis of CVD grown-graphene by transient TLP testing with different splits of GR dimensions are discussed.

The test device structure is shown in Fig. 3.15. The test devices are fabricated on thermally oxidized Si wafers with SiO_2 thickness of 300 nm. Monolayer and bilayer graphene are grown on copper foil via CVD and transferred onto the SiO_2/Si substrates. The quality and number of layers of graphene were examined by Raman [14] as shown in

Fig. 3.16. Conventional photolithography and O_2 plasma etching are used to pattern graphene into individual GR test devices. The metal pads consisting of Ti/Pd/Au (0.5/30/50 nm) are deposited by e-beam evaporation and lift-off processes. In order to study the effect of GR dimensions on TLP breakdown behaviors, test device splits with different GR dimensions are designed and fabricated as summarized in Table 3.1. Length (L= 9/12/22/30/50 μm) and width (W= 3/5/10 μm) of GR and number of graphene layers (monolayer/bilayer) are designed as test parameters. The GR robustness is determined by the maximum sustainable critical current (I_C, converted to critical current density, J_C) where GR wire is broken and I_C drops abruptly to zero as shown in Fig. 3.17 (a). We speculate the ESD breakdown procedures being: the failure starts at one spot with locally highest resistivity such as defects, grain boundaries, and contaminations, etc. When J_C is reached, breakdown happens with the presence of oxygen due to thermal energy accumulation, after which breakdown spreads near the breakdown spot due to further conductivity loss. A failure signature of an open line will be eventually formed across the width of a GR as shown in Fig. 3.17 (b), which is readily observed for all GR samples after breakdown.

Fig. 3.18 depicts the TLP I-V curves for monolayer and bilayer GR samples. It clearly shows that bilayer GR have much higher maximum current than monolayer GR indicating that both graphene layers of bilayer GR are contributing to ESD conduction. However, J_C for bilayer sample (2.27×10^8 A/cm^2) is smaller than monolayer sample (3.34×10^8 A/cm^2), which is likely due to more defects associated with bilayer graphene. However, these critical current density values are much higher than that of copper wires (~10^7 A/cm^2) which demonstrates the superiority of GR. Since the breakdown of GR is

due to the reaction between oxygen and carbon atoms in graphene after Joule heating accumulation, it is believed that through appropriate device packaging technique, J_C can be further increased [15, 16]. However, it should be noticed that the breakdown current of monolayer graphene is in the order of several milliamperes, which is way smaller than the huge breakdown current (typically 0.1~5 A) a conventional ESD device can discharge. More study should be carried out before the proposed device can be utilized in real ESD applications.

Fig. 3.19 presents the change of breakdown voltage V_C and current density J_C with varying GR lengths while keeping GR width constant (W=5 μm) for bilayer GR samples. V_C increases monotonically with L, while J_C, expected to be constant for homogeneous GR quality, degrades as L increases. This is possibly attributed to more defects (mainly grain boundaries) in longer GRs since typical grain size for CVD-grown graphene is known to be ~10 μm [17]. Fig. 3.20 shows the trend of breakdown current I_C and current density J_C with varying GR widths for same GR length (L=22 μm) bilayer samples. It can be seen that I_C increases linearly with increasing W, while J_C keeps nearly constant, which is different from the results shown in Fig. 3.19. This is expected because the variation of GR width (3-10 μm) is much smaller than that of GR length (9-50 μm), and 3-10 μm is within the range of one graphene grain domain, thus the number of defects in GR doesn't vary too much.

3.8. Figures

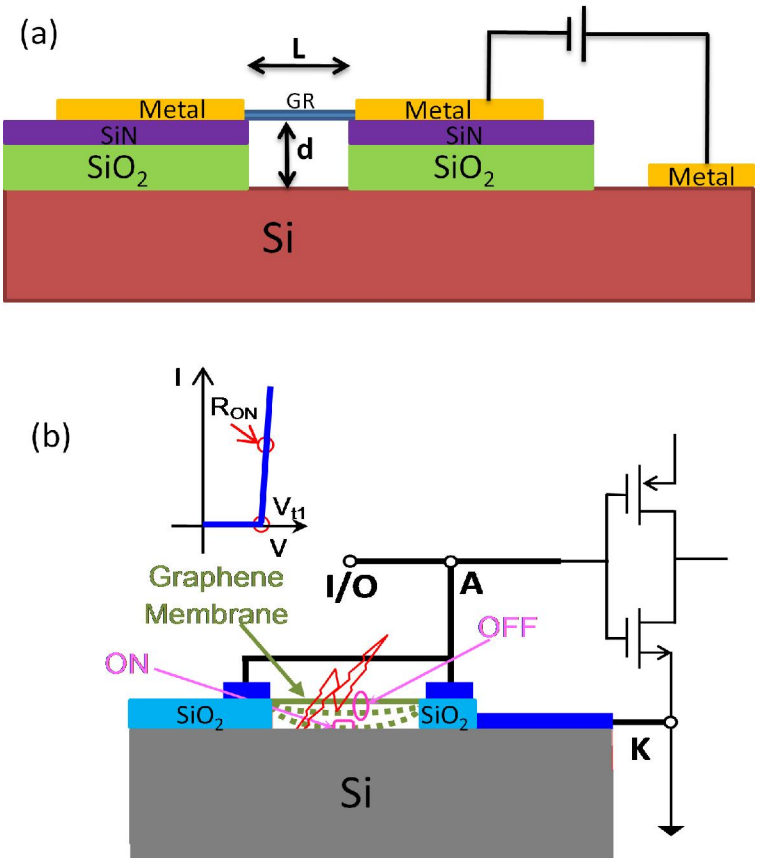


Fig. 3.1 (a) Proposed device structure; (b) "OFF" and "ON" state of the device under bias, inset shows the expected I-V curve.

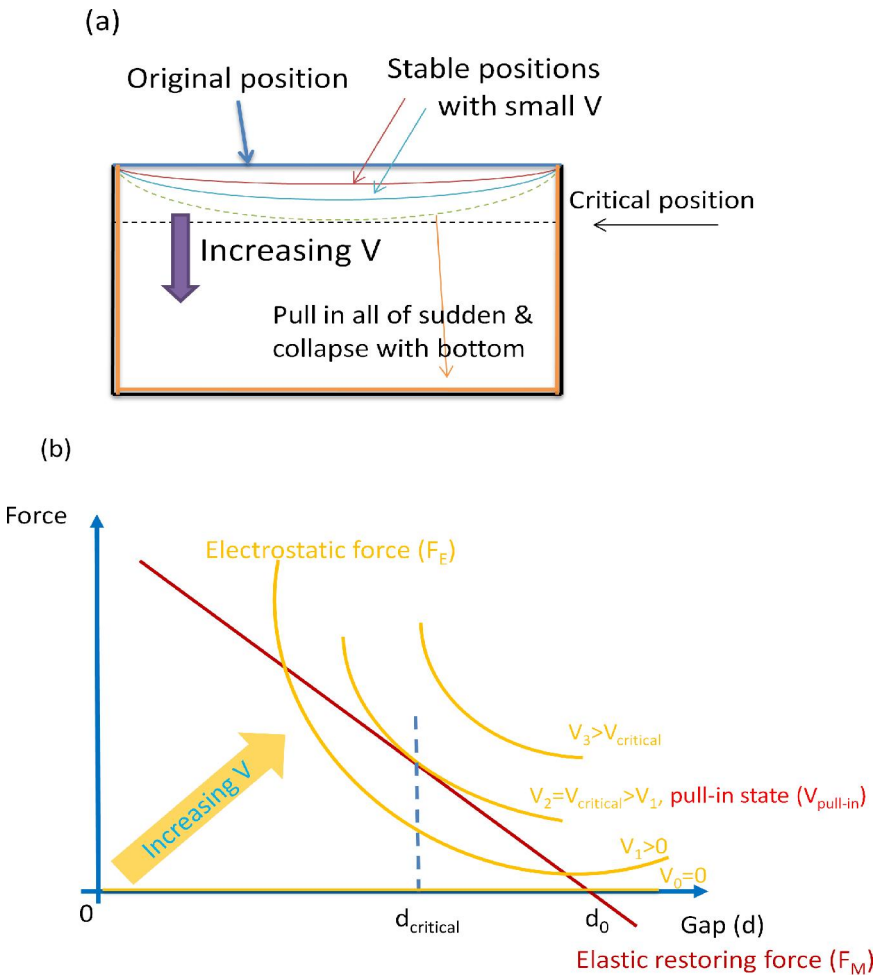


Fig. 3.2 (a) shape evolution of GR under increasing bias; (b) force balance between mechanical restoring force and electrostatic force.

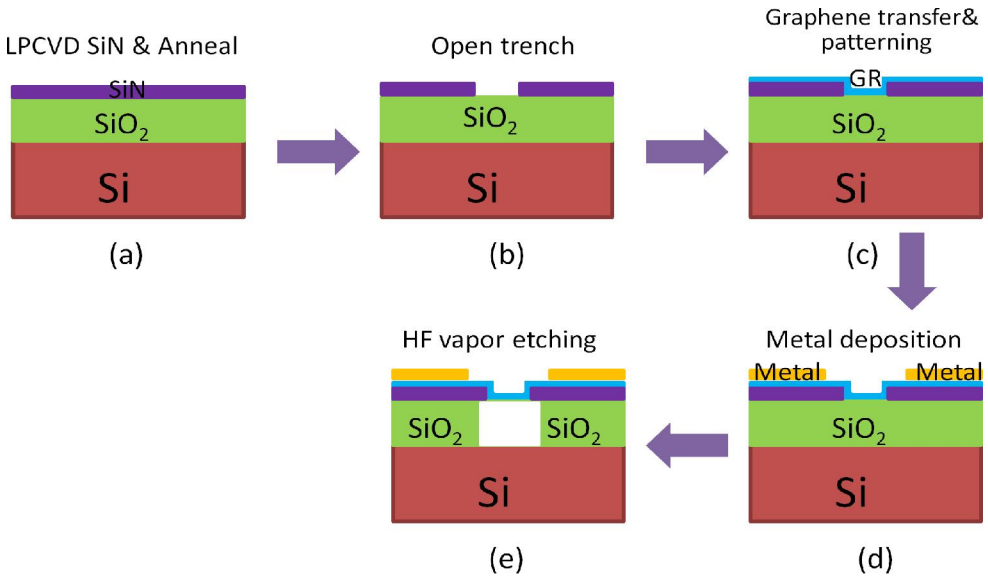


Fig. 3.3 Process flow of the device fabrication.

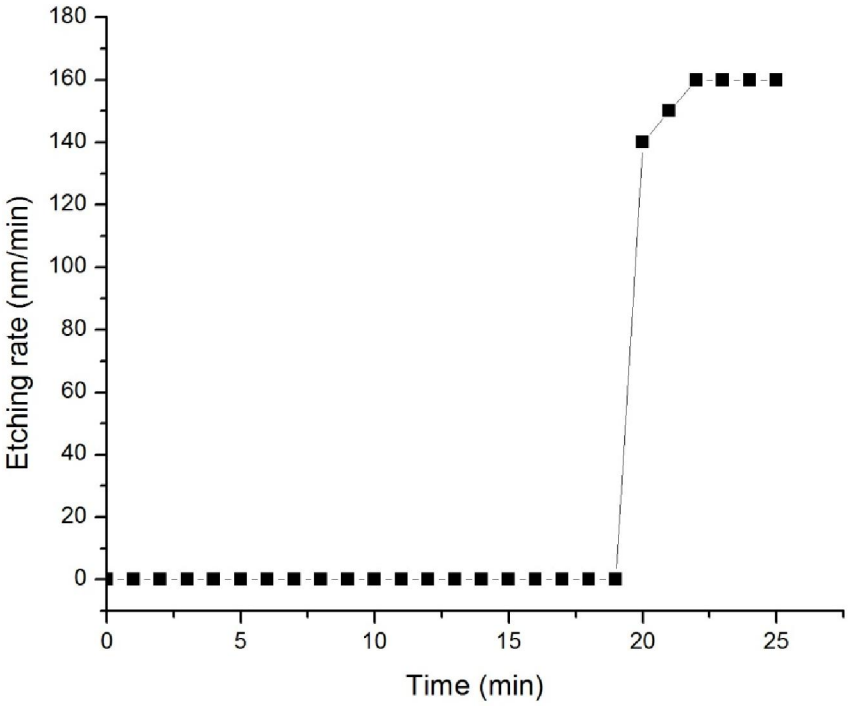


Fig. 3.4 SiO_2 etching rate of HFVE at 15^{o}C.

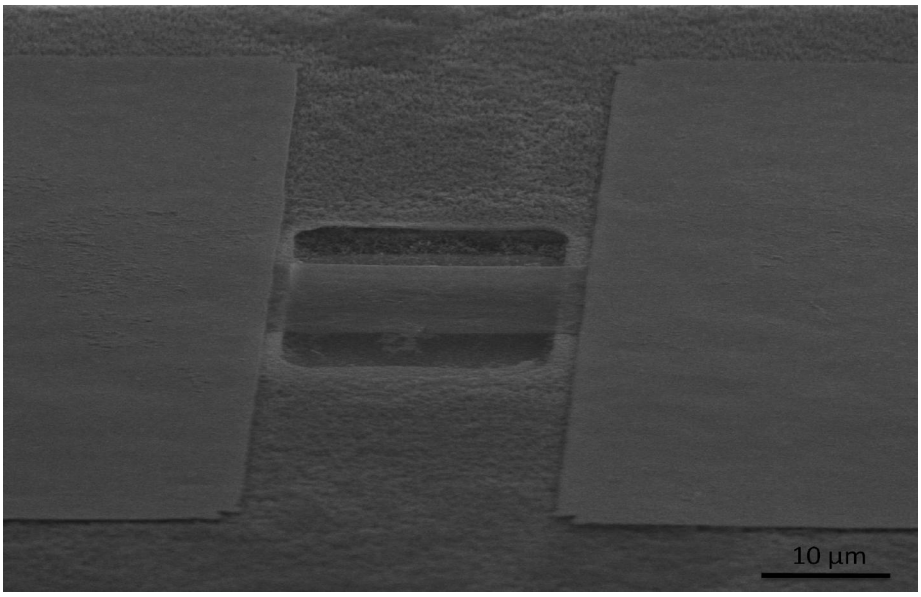


Fig. 3.5 SEM image of as fabricated suspended GR ESD device.

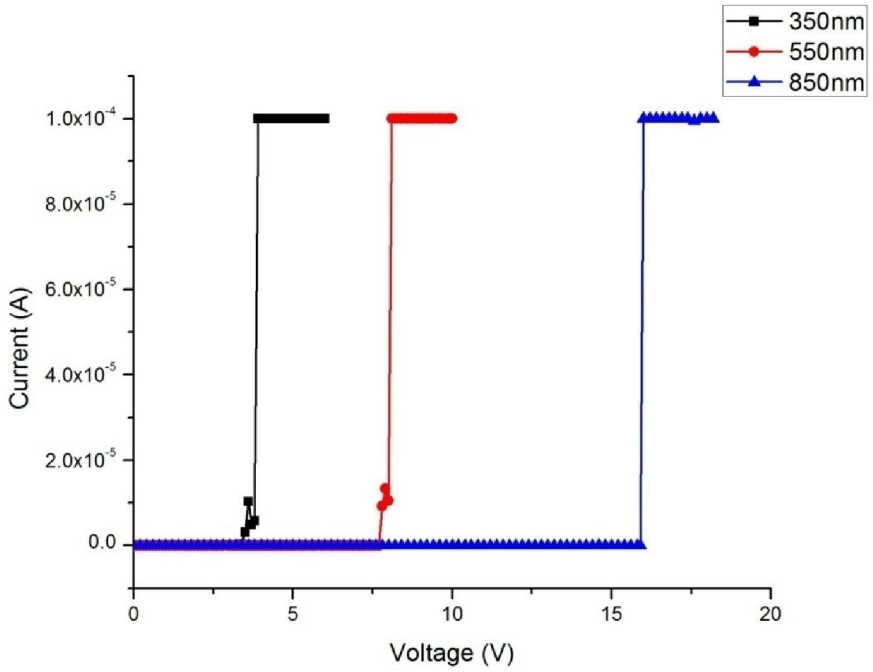


Fig. 3.6 Two-terminal DC measurement showing the turn-on behavior of suspended GR ESD devices with different trench depths.

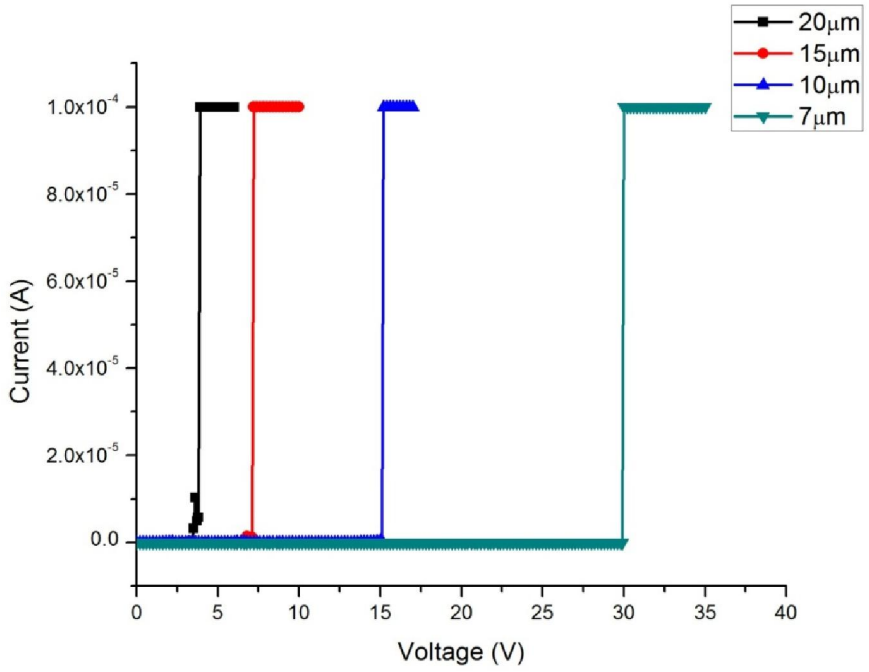


Fig. 3.7 Two-terminal DC measurement showing the turn-on behavior of suspended GR ESD devices with different GR lengths.

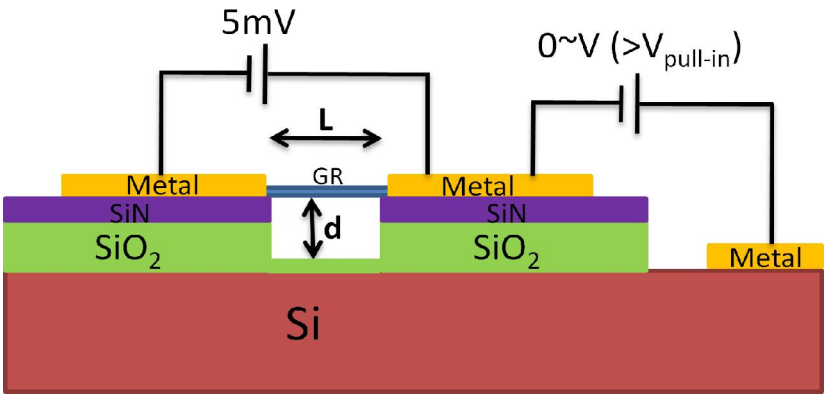


Fig. 3.8 Measurement scheme of three-terminal measurement.

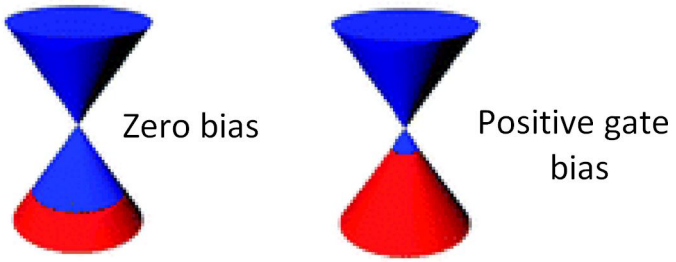
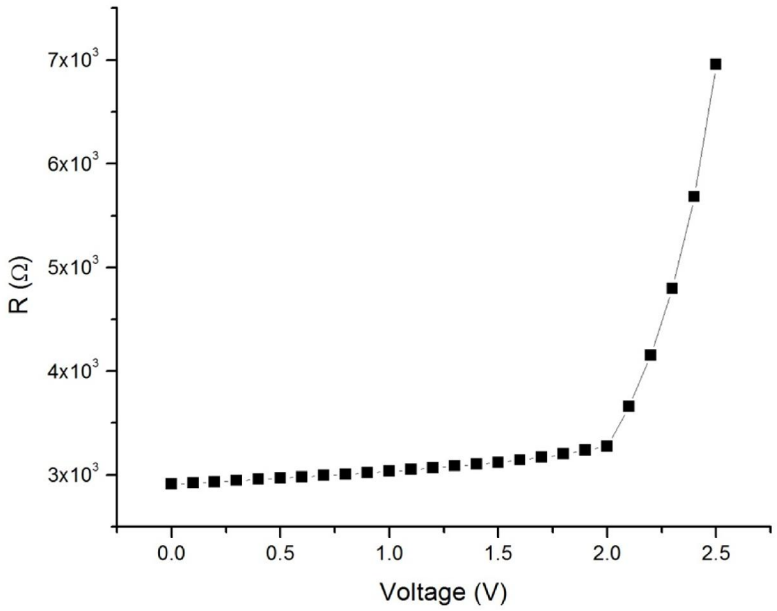
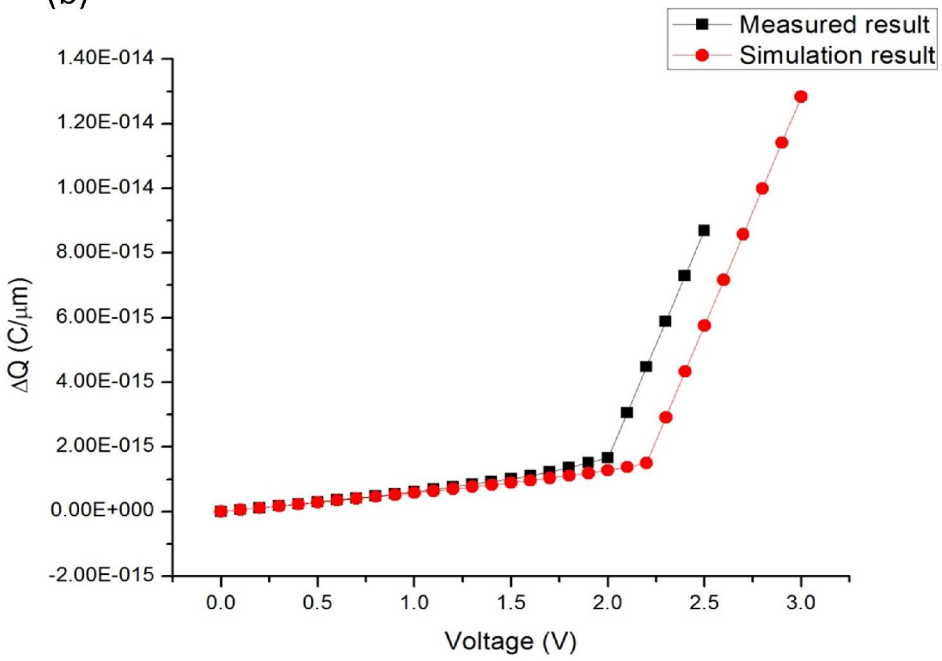


Fig. 3.9 The change of position of Fermi level with bias.

(a)


7x10^3
6x10^3
5x10^3
4x10^3
3x10^3
R (Ω)
0.0
0.5
1.0
1.5
2.0
2.5
Voltage (V)

(b)


Measured result
Simulation result
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1.20E-014
1.00E-014
8.00E-015
6.00E-015
4.00E-015
2.00E-015
0.00E+000
-2.00E-015
ΔQ (C/μm)
0.0
0.5
1.0
1.5
2.0
2.5
3.0
Voltage (V)

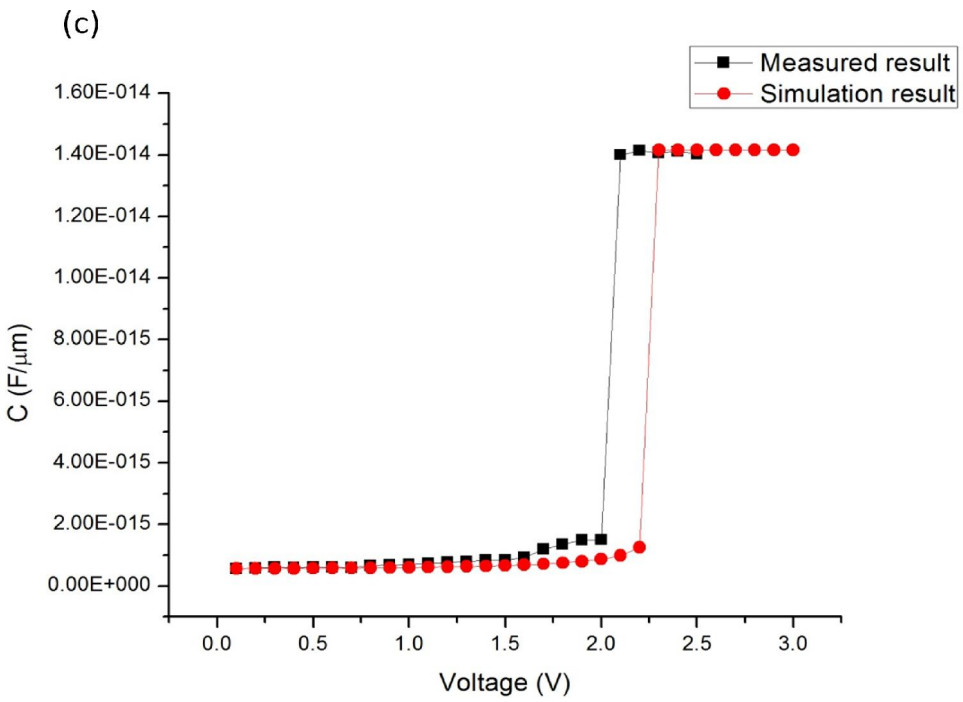
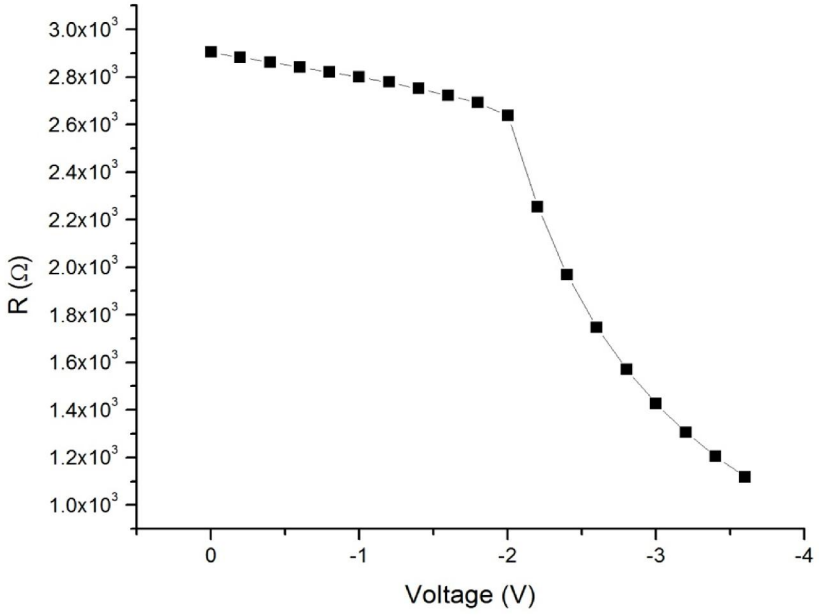
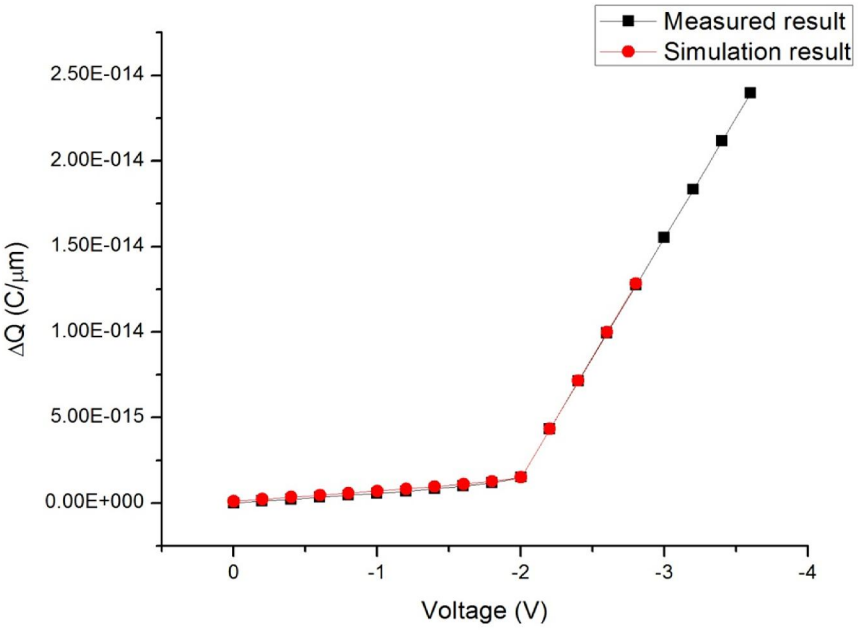


Fig. 3.10 Three-terminal DC measurement and simulation results (positive back gate bias, L= 20 μm, d= 300 nm) of the change trend of (a) R, (b) ΔQ, and (c) C with increasing V.

(a)


3.0x10^3
2.8x10^3
2.6x10^3
2.4x10^3
2.2x10^3
2.0x10^3
1.8x10^3
1.6x10^3
1.4x10^3
1.2x10^3
1.0x10^3
R (Ω)
0
-1
-2
-3
-4
Voltage (V)

(b)


Measured result
Simulation result
2.50E-014
2.00E-014
1.50E-014
1.00E-014
5.00E-015
0.00E+000
ΔQ (C/μm)
0
-1
-2
-3
-4
Voltage (V)

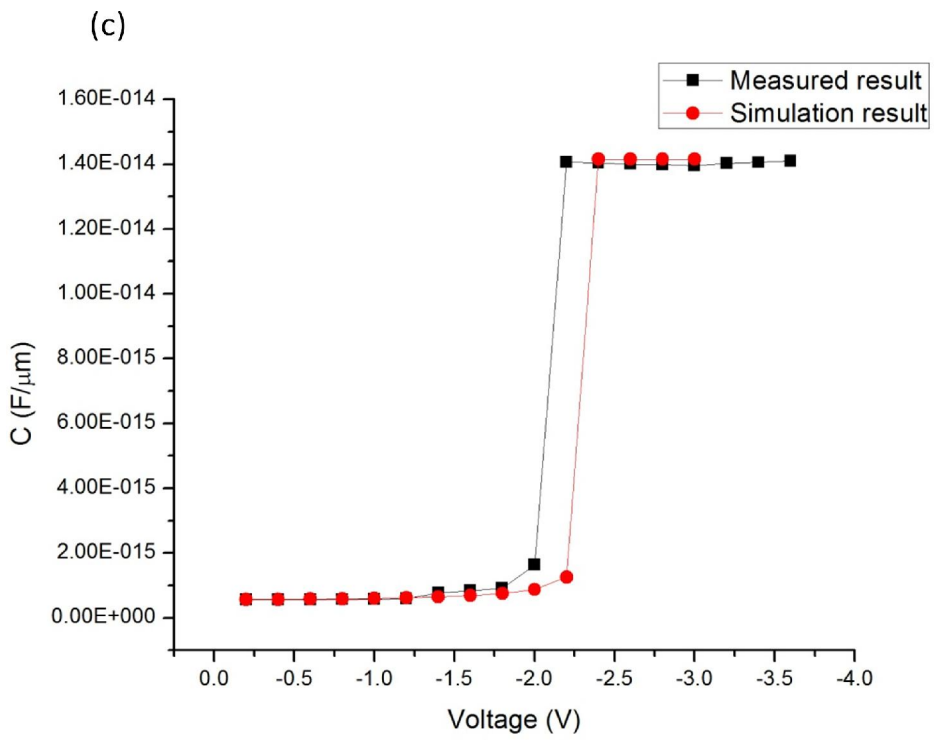


Fig. 3.11 Three-terminal DC measurement and simulation results (negative back gate bias, L= 20 μm, d= 300 nm) of the change trend of (a) R, (b) ΔQ, and (c) C with increasing V.

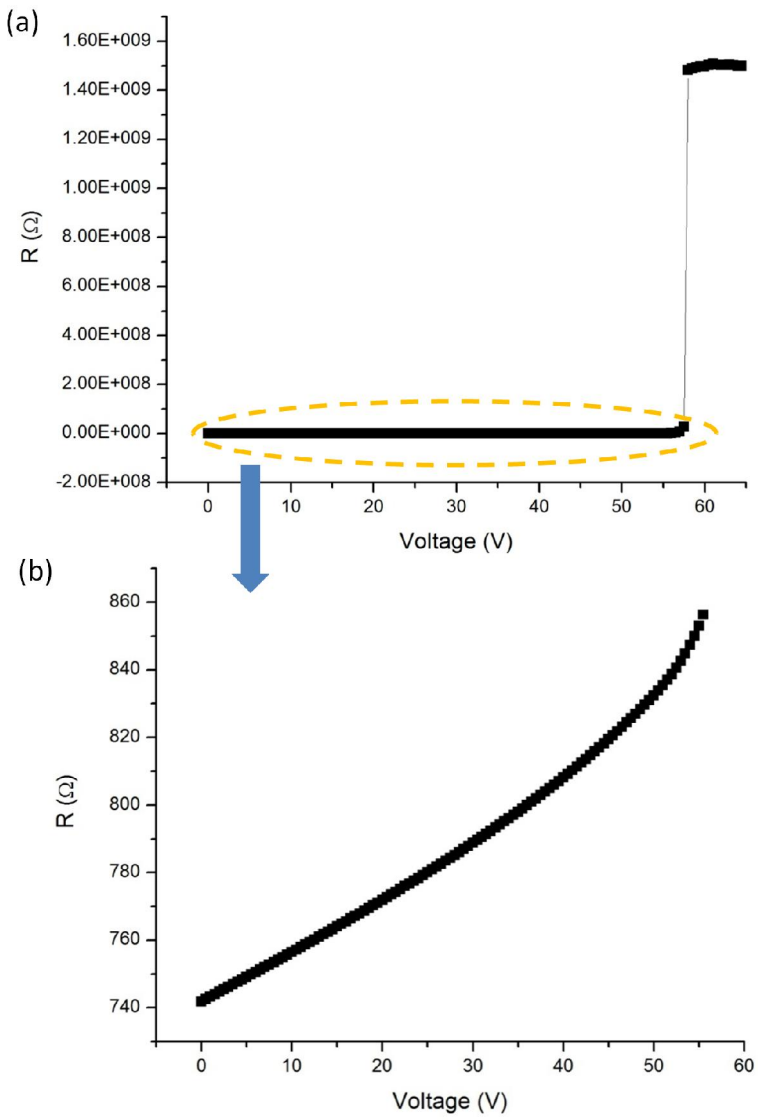


Fig. 3.12 (a) Three-terminal DC measurement (positive back gate bias, L= 20 µm, d= 2 µm) of the change of R; (b) enlarged curve of the circled section of (a).

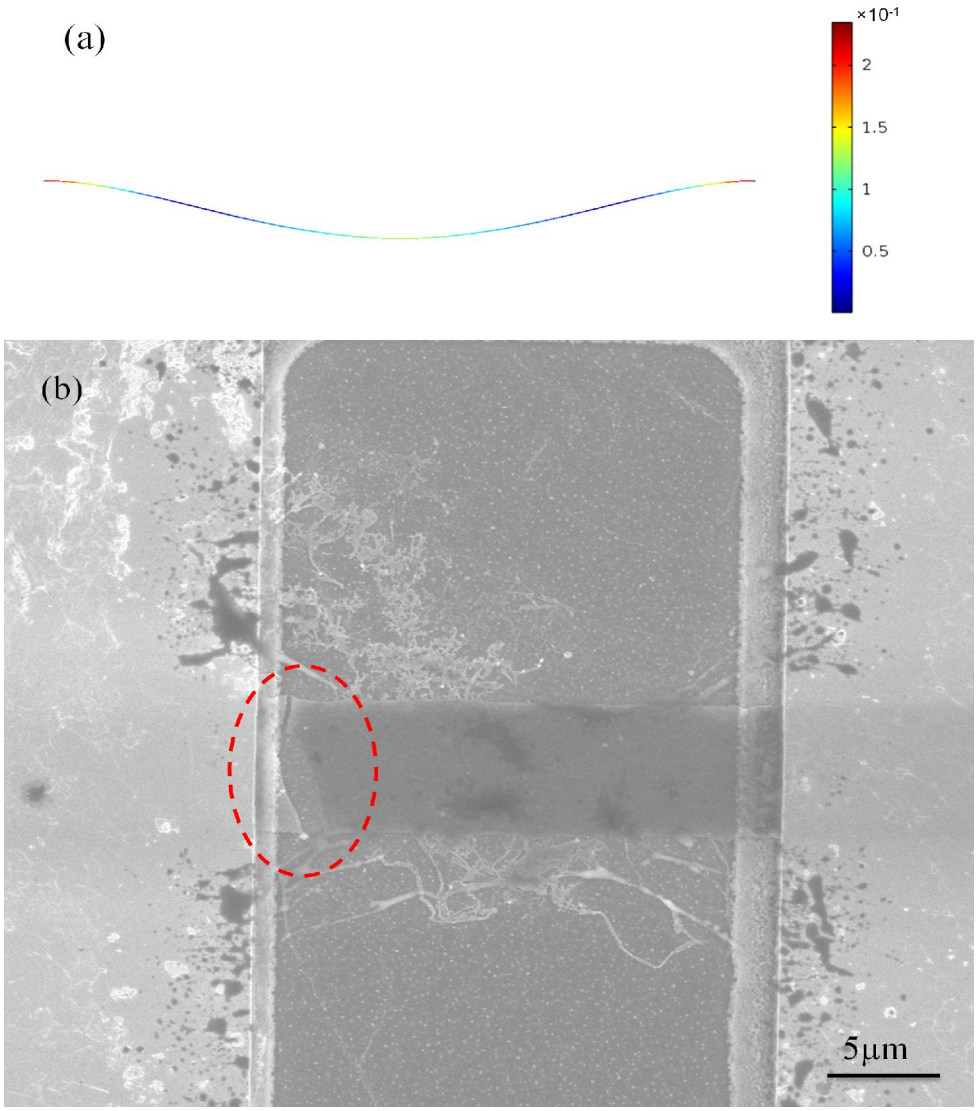


Fig. 3.13 (a) COMSOL simulation of strain distribution on GR; (b) SEM image of a broken GR after test showing the breakage at edge region.

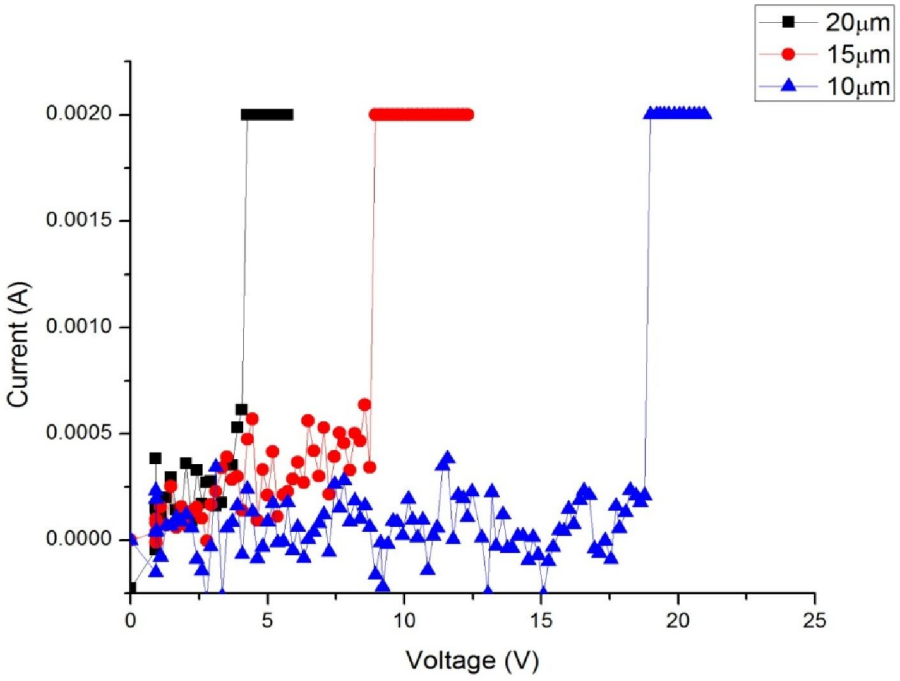


Fig. 3.14 TLP testing showing the turn-on behavior of suspended GR ESD devices with different GR lengths.

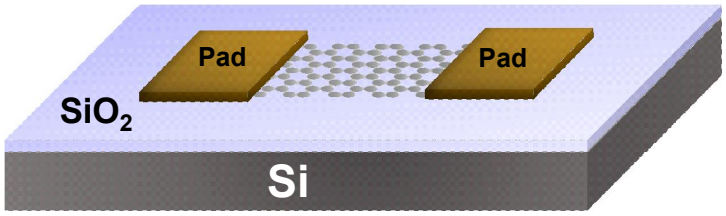


Fig. 3.15 Test device structure for TLP testing.

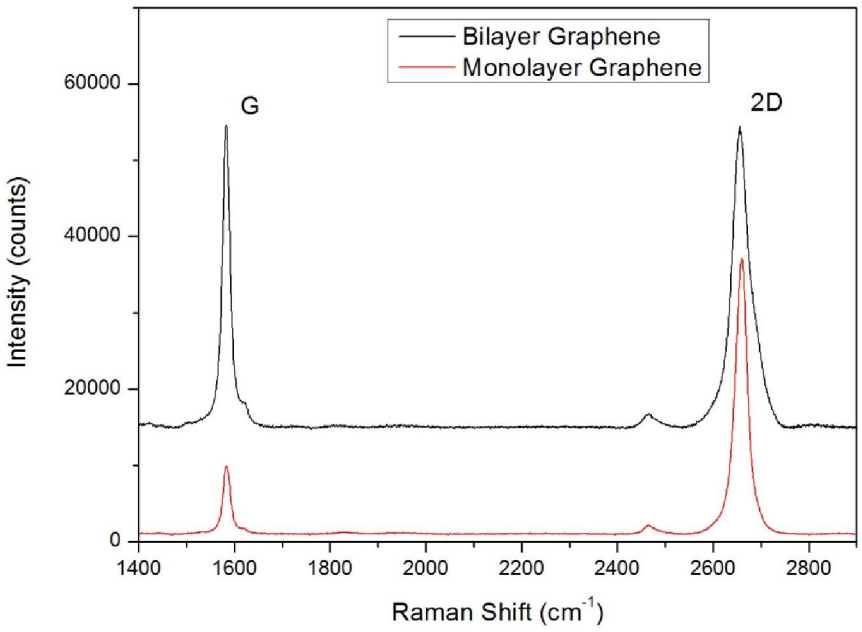


Fig. 3.16 Raman spectra of sample monolayer and bilayer graphene on SiO_2/Si substrate.

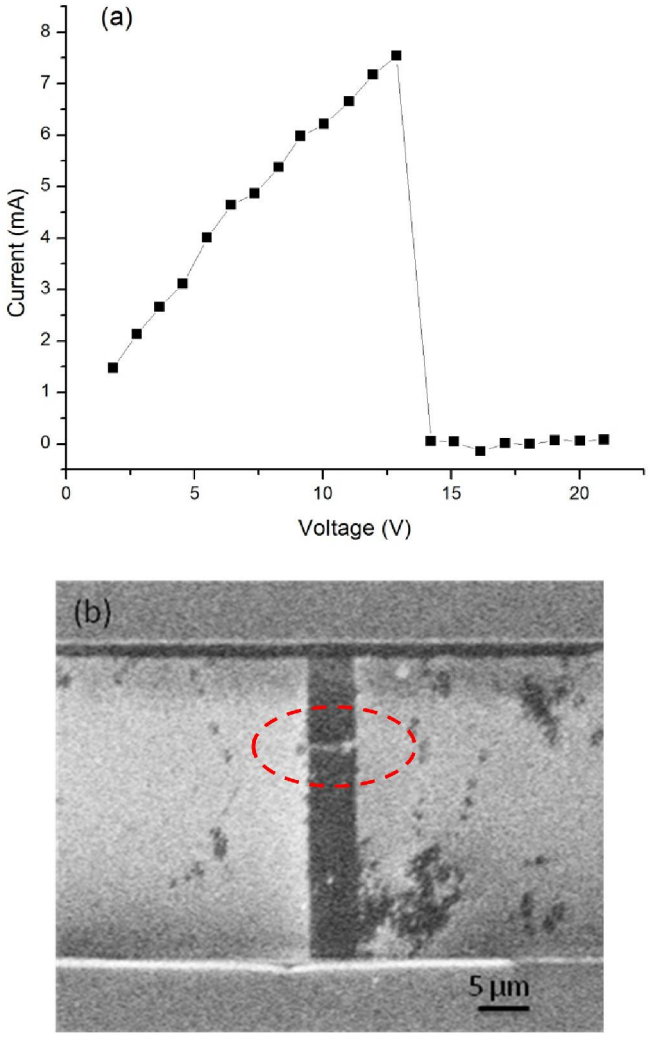


Fig. 3.17 (a) Typical transient I-V characteristics for a bilayer GR sample (L=12 µm, W=5 µm) under TLP stressing with t_d=100 nm, t_r=10 nm; (b) SEM image of a device with broken GR after breakdown, failure signature of a open line is circled.

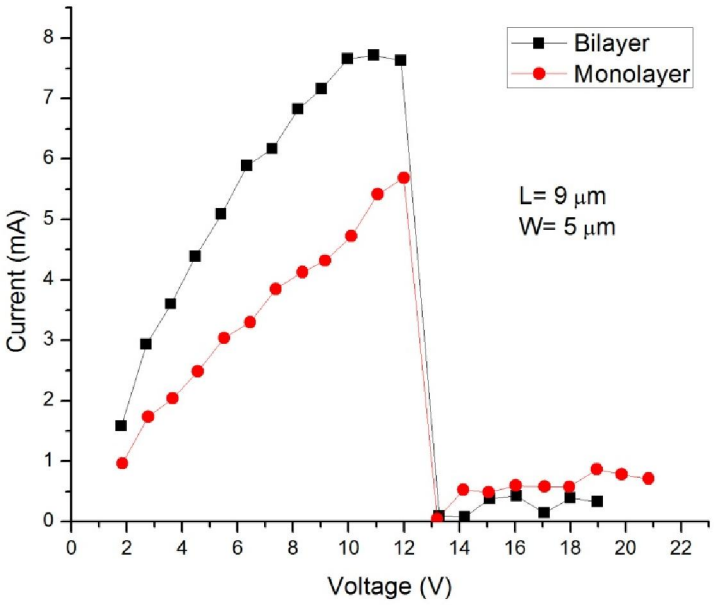


Fig. 3.18 TLP I-V curve for monlayer and bilayer GR samples showing better current carrying capability for bilayer GR, yet higher J_C for monolayer GR.

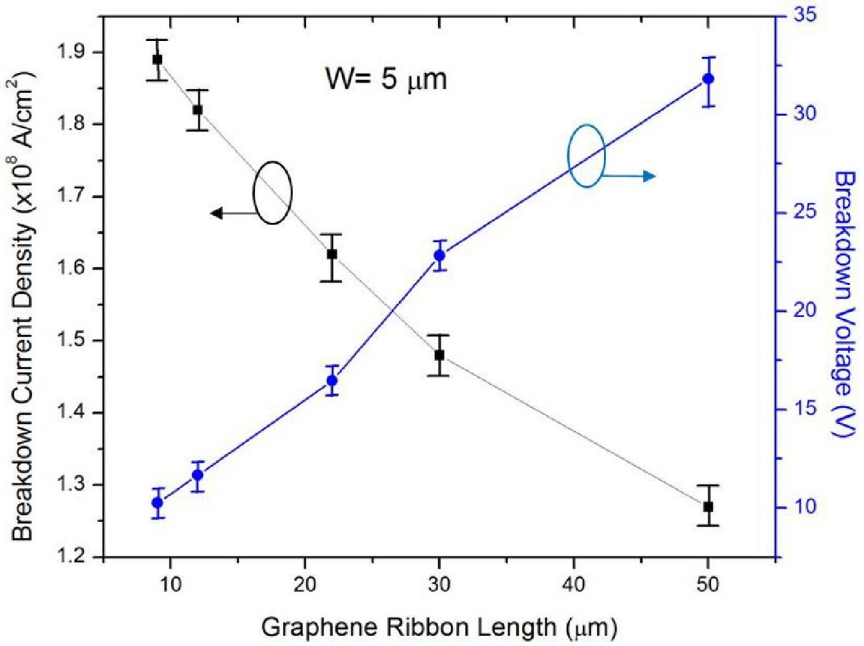


Fig. 3.19 TLP breakdown current density J_C and breakdown voltage V_C for various bilayer GR lengths (L), W= 5 μm. Trends for other GR width devices are similar.

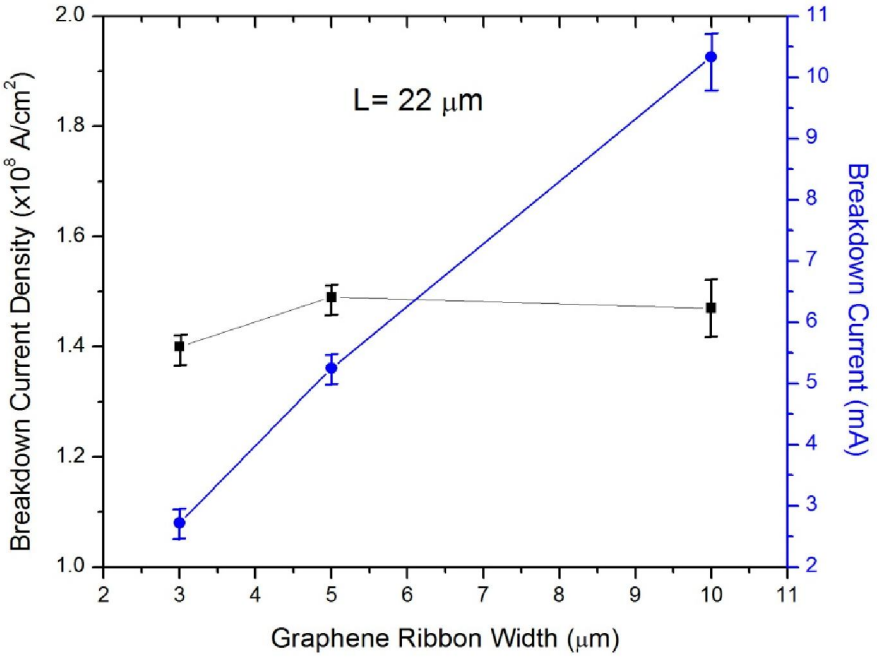


Fig. 3.20 TLP breakdown current density J_C and breakdown current I_C for various bilayer GR widths (W), L= 22 μm. Trends for other GR length devices are similar.

3.9. Tables

GR Wire Sample Splits			
Layers	L (μm)	W (μm)	Sample size
Mono-/Bilayer	9	3 / 5 /10	>2000
	12		
	22		
	30		
	50		

Table 3.1 Test device splits of different GR dimensions.

3.10. Reference

1. Ofir Bochobza-Degani, and Yael Nemirovsky, Sensors and Actuators A, 97-98, 569 (2002).
2. Anurekha Sharma, and P. J. George, Sensors and Actuators A, 141, 376 (2008).
3. Sung Min Kim, Emil B. Song, Sejoon Lee, Sunae Seo, David H. Seo, Yongha Hwang, R. Candler, and Kang L. Wang, Applied Physics Letters, 99, 023103 (2011).
4. K.I. Bolotin, K.J. Sikes, Z. Jiang, M. Klima, G. Fudenberg, J. Hone, P. Kim, and H.L. Stormer, Solid State Communications, 146, 351 (2008).
5. Chun Ning Lau, Wenzhong Bao, and Jairo Velasco Jr., Materialstoday, 15, 238 (2012).
6. Xu Du, Ivan Skachko, Anthony Barker, and Eva Y. Andrei, Nature Nanotechnology, 3, 491 (2008).
7. Peng Li, Zheng You, Greg Haugstad, and Tianhong Cui, Applied Physics Letters, 98, 253105 (2011).
8. Giulio Cocco, Emiliano Cadelano, and Luciano Colombo, Physical Review B, 81, 241412 (2010).
9. Anurekha Sharma, and P.J. George, Sensors and Actuators A, 141, 376 (2008).
10. Jeremy B. Muldavin, and Gabriel M. Rebeiz, IEEE International Microwave Symposium Digest, 3, 2119 (2001).
11. Serge Luryi, Applied Physics Letters, 52, 501 (1988).
12. Tian Fang, Aniruddha Konar, Huili Xing, and Debdeep Jena, Applied Physics Letters, 91, 092109 (2007).

13. A. Das, S. Pisana, B. Chakraborty, S. Piscanec, S. K. Saha, U. V. Waghmare, K. S. Novoselov, H. R. Krishnamurthy, A. K. Geim, A. C. Ferrari, and A. K. Sood, Nature Nanotechnology, 3, 210 (2008).
14. Zhenhua Ni, Yingying Wang, Ting Yu, and Zexiang Shen, Nano Research, 1, 273 (2008).
15. Xiangyu Chen, David H. Seo, Sunae Seo, Hyunjong Chung, and H.-S. Philip Wong, IEEE Electron Device Letters, 33, 1604 (2012).
16. Chang Goo Kang, Sang Kyung Lee, Young Gon Lee, Hyeon Jun Hwang, Chunhum Cho, Sung Kwan Lim, Jinseong Heo, Hyun-Jong Chung, Heejun Yang, Sunae Seo, and Byoung Hun Lee, IEEE Electron Device Letters, 32, 1591 (2011).
17. X. Li, C. W. Magnuson, A. Venugopal, J. An, J. Suk, B. Han, M. Borysiak, W. Cai, A. Velamakanni, Y. Zhu, L. Fu, E. M. Vogel, E. Voelkl, L. Colombo, and R. S. Ruoff, Nano Letters, 10, 4328 (2010).

Chapter 4. Ab initio calculations for multilayer graphene growth

4.1. Motivation for the calculations

Multilayer graphene (MLG) consisting of two or more layers of graphene is of interest for various applications including transparent electrodes for organic devices [1, 2], solar cells [3], field-effect transistors [4], field emission displays [5], photo-detectors [6], and highly efficient thermal interface materials [7]. It has also been discussed previously that for the proposed suspended GR ESD device, MLG will render advantages such as higher current drivability, faster response time, and stronger mechanical strength, etc. The crux of MLG fabrication is the growth dynamics of graphene homo-epitaxy. This dynamic process is expected to be fundamentally different between 2-dimensional materials (also known as van der Waals materials) and their 3-dimensional counterparts for which there exists an extensive knowledge base. Different techniques have been used to fabricate MLG including low-temperature chemical vapor deposition on Ni catalyst [3], microwave plasma enhanced chemical vapor deposition [5, 8] and transferring and stacking large-area CVD-grown graphene mono-layers [9]. However to date, no proven approach allows for precise control of the number of layers presumably due to the lack of fundamental understanding of the dynamics of epitaxy. It has been mentioned that MLG will benefit the suspended GR ESD device performance, and controllability of the number of layers is of great importance because the graphene film thickness is relevant to the trigger voltage and response time of the ESD device. Therefore, it is critical to study the growth mechanism of MLG to guide its controllable growth. In this chapter, the

results of an ab initio study of various plausible modes of graphene epitaxy over graphene surfaces using density-functional theory (DFT) are discussed.

4.2. DFT calculations

In principle, the quantum mechanical wavefunction contains all the information of a given system. The wavefunction of a system can be obtained by solving the Schrodinger equations, and the allowed energy states of the system can be determined. However, the Schrodinger equation cannot be solved for a many-body system. Therefore, a set of approximations need to be made in order to get an approximation solution for the Schrodinger equation of a many-body system. This method is called Density Functional Theory (DFT) developed by Hohenberg and Kohn (1964) and Kohn and Sham (1965). A functional is a function of a function. Hohenberg and Kohn proved that the total energy, including exchange and correlation, of an electron gas is a unique functional of the electron density. The minimum value of the total-energy functional is the ground-state energy of the system, and the density that yields this minimum value is the exact single-particle ground-state density. Kohn and Sham then showed how it is possible, formally, to replace the many-electron problem by an exactly equivalent set of self-consistent one-electron equations. Therefore, if we know the electron density functional which can be derived by a one-election Schrodinger equation, we know the total energy of our system. Basically, DFT calculations are based on pseudopotentials, a plane-wave basis set, and a supercell geometry. It allows a description of the many-body electronic ground state in terms of sigle-particle equations and an effective potential. The effective potential is comprised of the ionic potential due to the atomic cores, the Hartree potential describing

the electrostatic electron-electron interaction, and the exchange-correlation potential that takes into account the many-body effects. [10-12]

4.3. Calculation methods

The calculations are based on DFT as implemented in the Fritz Haber Institute ab initio molecular simulations package (FHI-AIMS) [13]. This is an all-electron full potential DFT code that uses numeric atom centered orbitals as its basis set. We have used the parameters as they are implemented in FHI-AIMS in the default setting "light" which has radial s, p, and d characters with an overall cutoff radius of 5 Å and a Hartree potential expansion up to l=4. The accuracy of the total energy is tested to be within 0.01 eV compared with that obtained using the default setting "tight" (overall cutoff radius of 6 Å and l=6) [13]. We use the Perdew-Burke-Ernzerhof (PBE) approximation of the generalized gradient approximation (GGA) for the exchange-correlation functional [14]. It is a well-known problem that inter-layer graphitic bonding due to van der Waals (vdW) forces is not properly described within the standard DFT framework. This is most dramatic for graphite where the DFT-GGA results yield a slight repulsion of around 10~20meV per atom between individual carbon sheets. We therefore use the Tkatchenko-Scheffler method [15] to include vdW interactions in the DFT calculations. The graphene lattice constant is calculated to be 2.465 Å in good agreement with previous results [16]. To model the diffusion of carbon atoms or clusters on monolayer graphene, we use a 17.25 Å x 17.08 Å graphene supercell (7-hexagon wide in the x-direction and 8-hexagon wide in the y-direction) comprising of 112 carbon atoms with a vacuum region of 50 Å in the z-direction. A 4 x 4 x 1 k-point grid is used for the calculations. The convergence of

the results has been carefully tested with respect to the system size, the basis set, and the density of the (numerical) integration mesh.

4.4 Calculation results

4.4.1. Diffusion of a carbon adatom

First, we investigate the diffusion of individual carbon adatoms on monolayer graphene. The preferred adsorption sites are the bridge sites about 1.89 Å above the graphene plane with an adsorption energy of -2.70 eV. It is shown as position A in Fig. 4.1 (a). The absorption energy ΔE_a of a carbon adatom on monolayer graphene is defined as:

$$\Delta E_a = E_{total} - E_g - E_c \qquad \textit{Equation 4.1}$$

where E_{total} is the total DFT energy of the carbon adatom-graphene system, and E_g and E_c are the total DFT energies of an isolated graphene monolayer and an isolated carbon adatom, respectively. All of the energies mentioned above are negative in value. In order to diffuse across the graphene surface, a carbon adatom has to cross the transition site shown as position T in Fig. 4.1 (a). The nudged elastic band method (NEB) is used to find the minimum energy path (MEP) and the transition site [17, 18]. The diffusion barrier for an adatom to hop along the path indicated in Fig. 4.1 (a) is about 0.48 eV. Figs. 4.1 (b) and (c) show the side view of site A and T. The corresponding electron density difference plots are shown in Figs. 4.1 (d) and (e). They are obtained by subtracting the electron densities of individual carbon atoms (no interaction among each other) sitting in the same positions as the adatom-graphene system from that of the adatom-graphene

system. Therefore, they represent a net change of the electron densities from which the bonding information [white part in Fig. 4.1 (d) and (e)] of the adatom-graphene system can be extracted. It can be seen from Fig. 4.1 (d) at the adsorption site A, that the carbon adatom forms covalent bonds with two neighboring atoms in the graphene layer underneath. This accounts for the strong interaction between the carbon adatom and the graphene layer, and thus the larger adsorption energy and diffusion barrier compared to other carbon clusters of bigger sizes diffusing on graphene. Details will be discussed in the following sections.

4.4.2. Diffusion of carbon dimers, tetramers and hexagons

We continue to study the diffusion of carbon dimers, trimers, tetramers, pentamers, and hexagons. For each cluster size, more than 10 plausible configurations have been tested to find the most preferred configuration and adsorption site. Trimers and pentamers behave in a similar fashion as dimers and tetramers within the accuracy of the calculation and are excluded here for brevity. Figs. 4.2 (a)-(c) show these configurations of the diffusing species at the adsorption sites and the bonding information obtained in the same way as discussed previously. The adsorption energies per carbon atom of dimers, tetramers and hexagons are -5.47 eV, -6.91 eV, and -7.27 eV, respectively. The absorption energy ΔE_a can be defined as:

$$\Delta E_a = E_{total} - E_g - nE_c \qquad \textit{Equation 4.2}$$

where E_{total} is the total energy of the carbon cluster-graphene system, n is the number of carbon atoms in the cluster, and E_g and E_c are the total energies of an isolated graphene monolayer and an isolated carbon adatom, respectively. Since the adsorption energy per

atom decreases as the size of cluster becomes bigger, it is energetically favorable for the carbon atoms to stick together and form clusters instead of standing alone as individual adatoms. As can be seen from Figs. 4.2 (a)-(c), dimers and tetramers prefer to sit upright at the bridge site about 1.88 Å and 1.81 Å above the graphene layer whereas hexagons prefer to lay flat floating about 3.25Å above the graphene layer. Dimers and tetramers form covalent bonds with the neighboring two atoms of the graphene layer in a similar way as an individual carbon adatom. The diffusion barriers for dimers and tetramers are about 0.25 eV and 0.35 eV respectively, both smaller than the barrier for an individual carbon adatom. On the other hand, there are no covalent bonds formed between hexagons and graphene and only vdW forces are present. The bonding energy between hexagons and graphene is quite small being about 80 meV per atom, which results in a very small diffusion barrier of about 6 meV. This means that compared to an individual carbon adatoms, dimers or tetramers, hexagons are much more mobile and may move more freely on the graphene surface. It is instructive to compare these diffusion barrier values to that of Si adatoms diffusing on Si (100) surfaces which is about 1 eV [19]. This suggests that all carbon species from monomers to other clusters diffusing on the graphene surfaces are much faster than Si adatoms on Si (001) surfaces. Therefore, we expect that during the homo-epitaxy of graphene, the islands grown will be much larger and much further separated than in the case of Si on Si (001) at the same growth temperature.

4.4.3. Diffusion of carbon clusters of larger sizes

At least 5 plausible configurations have been tested to find the most preferred configuration and adsorption sites for several cluster sizes larger than 6 carbon atoms. When the number of carbon atoms in the cluster is larger than 6, the clusters tend to form flat rings floating over graphene surface, as shown in Figs. 4.3 (a) and (b). When the size of the cluster reaches 13 carbon atoms or more, a flat and compact graphene-like configuration can be formed above the graphene surface as shown in Figs. 4.3 (c)-(e). Like hexagons, no covalent bonds are formed between clusters and graphene with only vdW forces present. We plot the adsorption energies per atom for the clusters of different configurations as a function of number of atoms in Fig. 4.4. The adsorption energies per atom for flat ring configurations first drop sharply with increasing cluster size and reach a minimum at the size of about 54 carbon atoms. Then it goes up, presumably approaching -6.56 eV which is the adsorption energy per atom for an infinite carbon atom string. The adsorption energy per atom for graphene-like configurations slowly approaches the binding energy per atom for a full graphene layer, which we have calculated as -9.23 eV per atom (in AB stacking). Compared to flat ring configurations, the compact graphene-like configuration is less energetically favored until the size of cluster increases to about 24 carbon atoms. However, we speculate that due to the kinetic limitations, clusters of size less than 24 carbon atoms might also form metastable graphene-like configurations. The kinetic pathway for the transition from flat ring configuration to graphene-like configurations is not yet known. When considering surface diffusion of carbon clusters, it is important to keep in mind the fundamental difference between islands/clusters of carbon over graphene surface and those of 3-dimensional crystals such as Si over Si surface. The former is more mobile than individual carbon adatoms whereas the latter is

stationary for all practical purposes. By far, majority of the total adsorption energy of ΔE_a comes from the C-C bonds in the plane of the island/cluster. The strong C-C bonds within individual island/cluster imply their very low "2-dimensional vapor pressures". In other words, the carbon adatom density in the presence of graphene islands in equilibrium is expected to be orders of magnitude lower than that of Si adatoms in the presence of Si 2-dimensional islands at comparable temperatures. The surface diffusion barriers shown in Fig. 4.5 are typically less than 10% of ΔEa. This is one of the unique characteristics of van der Waals materials. The surface diffusion barrier height increases nearly linearly with increasing cluster size. This is because each carbon atom in the cluster contributes to the total vdW force which is the origin of the energy barrier. Therefore, the carbon clusters will eventually become immobile again with increasing size of the clusters. To put things in perspective, we know from Fig. 4.5 that the diffusion barrier of graphene islands/clusters on a graphene surface approaches that of individual Si adatoms on Si (001) surface only when the cluster size reaches about 200. This means that on pristine graphene surfaces, one would expect that epitaxial growth of a second layer of graphene can be carried out at much lower substrate temperatures than for 3-dimensional crystals.

4.5. Discussions

Based on the calculation results presented above, we believe that the growth mode for graphene homoepitaxy is completely different from the established conventional growths modes for 3-dimensional bulk materials. For the epitaxy of 3-dimensional materials, single adatoms are typically the fastest moving entities on the surface. They collide and interact with one another to form clusters. When a critical size is reached

stochastically, a cluster becomes thermodynamically stable and acts as a sink for additional adatoms in the island nucleation/coalescence mode of growths. Alternatively, adatoms diffuse along the surface until encountering an existing step edge where they incorporate in the step-flow growth mode. However, for epitaxial growths of vdW materials such as graphene on graphene, the process appears to be that monomers and small clusters are relatively stationary on the surface because of the covalent bonds they form with the underlying graphene, whereas clusters of size 6 or more diffuse freely on the graphene surface and incorporate smaller clusters and adatoms along the way. The process continues with these large clusters experiencing growth in size while losing mobility. Therefore, we propose that growth of graphene proceeds rather differently, depending on the size and nature of the species that are being deposited. Specifically, we believe that one can design experiments such that either (i) adatoms are deposited onto the surface, or (ii) small clusters such as hexagons are the deposited species. The anticipated kinetics of these two modes of growths is rather different, as will be discussed in the following. It should be emphasized that the results presented here assume a pristine graphene surface while in practice graphene surfaces, especially the CVD grown graphene surfaces, are likely to suffer from inevitable contamination leading potentially to significantly impeded surface diffusion.

4.5.1. Single atoms as carbon source

First, let us assume that the species used for deposition are single adatoms [20]. In that case, the adatoms are rather immobile, and the density of these adatoms increases essentially linearly with time. The formation of clusters begins only when the density of

these adatoms becomes rather high and the probability of the collisions of multiple adatoms becomes significant during the growths. As the sizes of individual clusters grow, they become increasingly mobile. They become levitated when their sizes grow to at least 6 carbon atoms, and the mobility for surface diffusion reaches its peak. They will diffuse along the surface and incorporate the relatively immobile adatoms, while growing in size. With the increase of their sizes, they also slow down and eventually become as immobile as the adatoms.

4.5.2. Hexagon rings as carbon source

When hexagons are deposited on the graphene surface [21, 22], these hexagons are very mobile, and essentially float on the surface. These hexagons collide and coalesce into larger graphene-like clusters and then slow down. Due to the large diffusion length of the hexagons, one could expect large area and high quality graphene homoepitaxy with large grains at low growth temperatures. But we note that defects of grain boundaries may occur during coalescence for the following two reasons: (a) AA stacking and AB stacking are degenerate; (b) smaller building blocks such as monomers or dimers that are needed to fill in voids are absent.

These consequences need to be verified by carefully planned experimental studies. They also point to methods for optimizing the growths of precisely controlled bilayer graphene. We propose to design experiments that use benzene as a source of diffusing species based on the fact that hexagons are very mobile. Other 2-dimensional van der Waals materials may follow similar growth mode as graphene which needs to be further verified.

In summary, small carbon clusters are much more mobile than individual carbon adatoms on graphene surfaces. Due to the large diffusion length of carbon clusters, it is possible to conduct graphene epitaxial growth over graphene surfaces at low growth temperatures. Beyond a certain size of the cluster (24 atoms), a graphene-like structure is energetically preferred compared to a flat ring structure. Our results indicate that the growth mode of graphene homoepitaxy is totally different from the 3-dimensional bulk materials, and growth proceeds rather differently, depending on the size and nature of the species that are being deposited. [23]

4.6. Figures

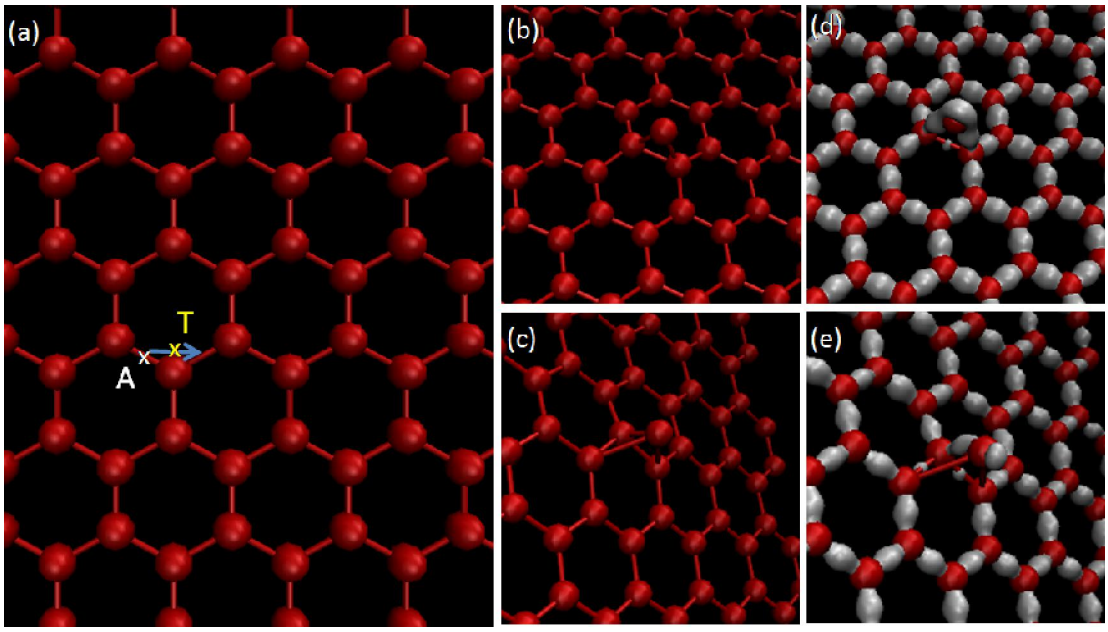


Fig. 4.1 .(a) Adsorption site (A) and transition site (T) for a carbon adatom on graphene, (b)side view of adsorption site, (c) side view of transition site, and the corresponding electron density difference plots (d) and (e).

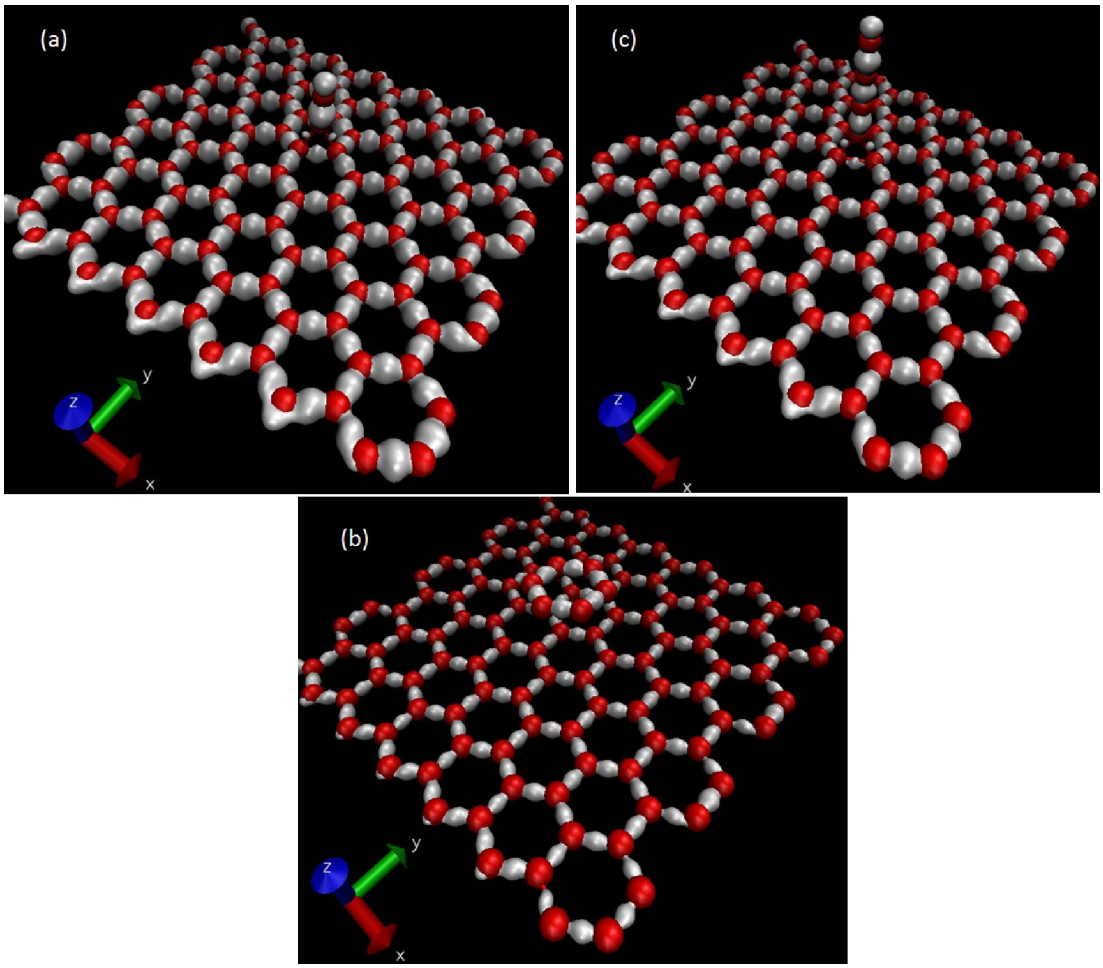


Fig. 4.2 The electron density difference plots showing the most preferred configurations with bonding information for (a) dimer, (b) tetramer, and (c) hexagon.

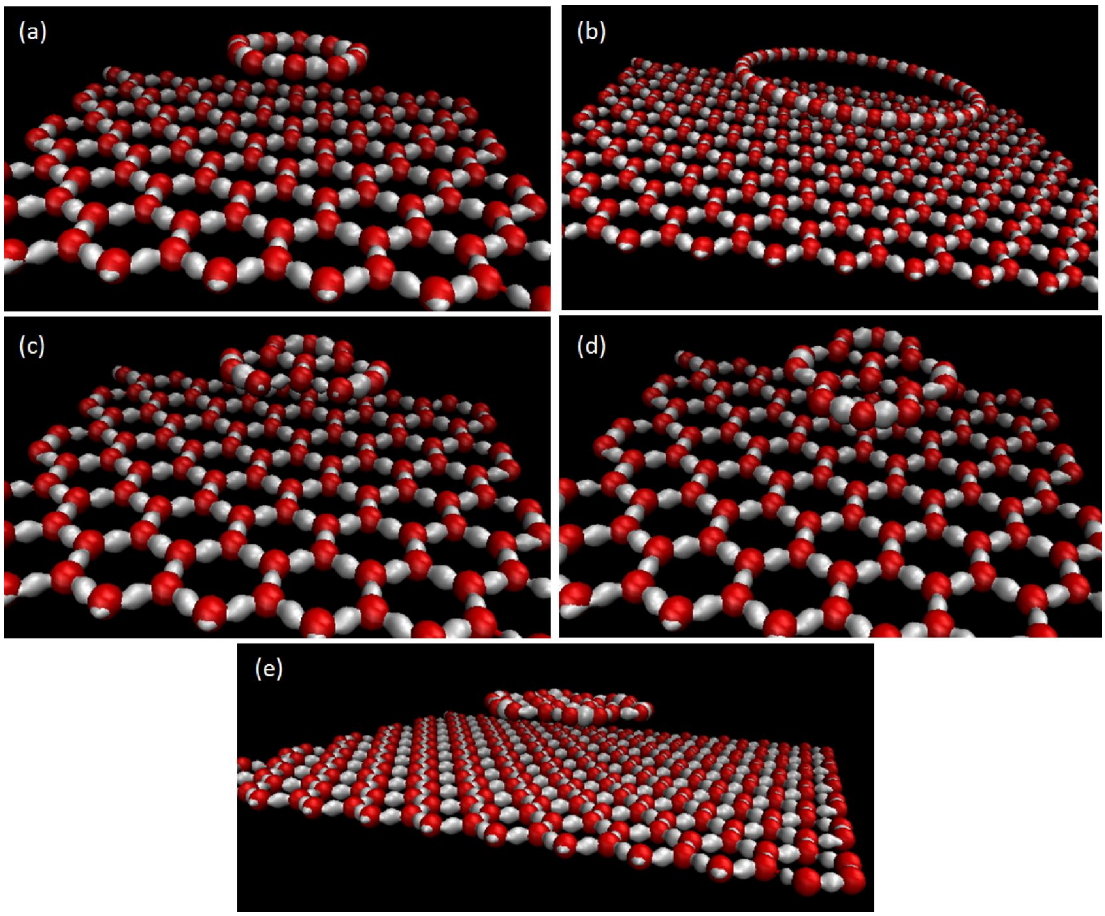


Fig. 4.3 Stable flat ring configurations for (a) 10 carbon atoms, and (b) 30 carbon atoms; stable compact graphen-like configurations for (c) 13 carbon atoms, (d) 16 carbon atoms, and (e) 24 carbon atoms.

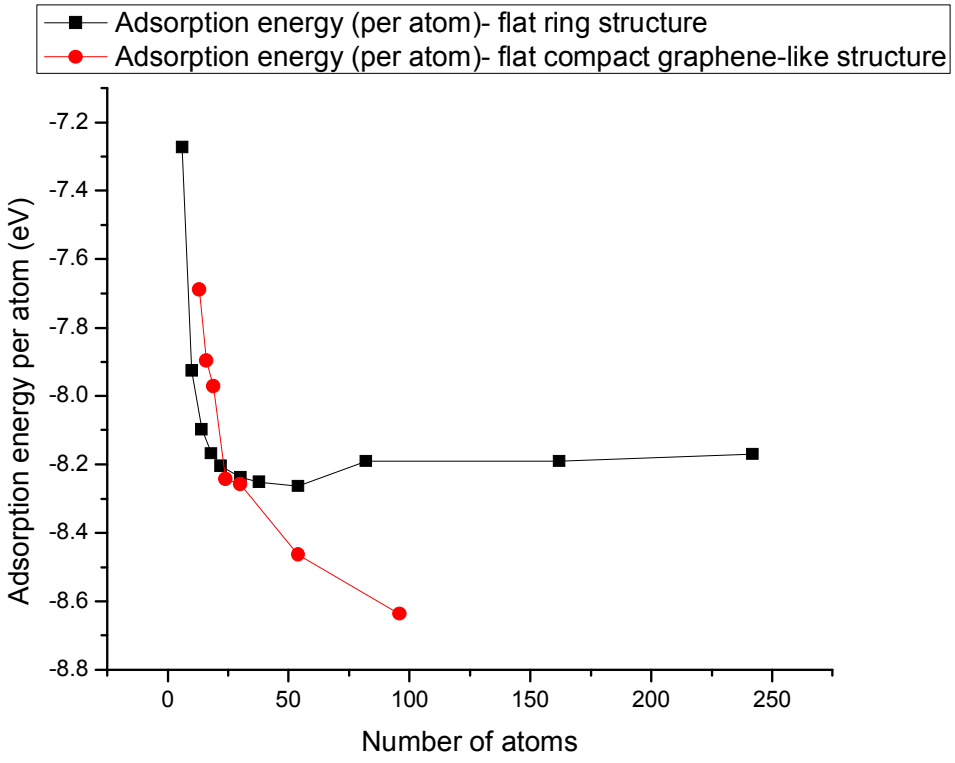


Fig. 4.4 Adsorption energies per atom as a function of number of atoms.

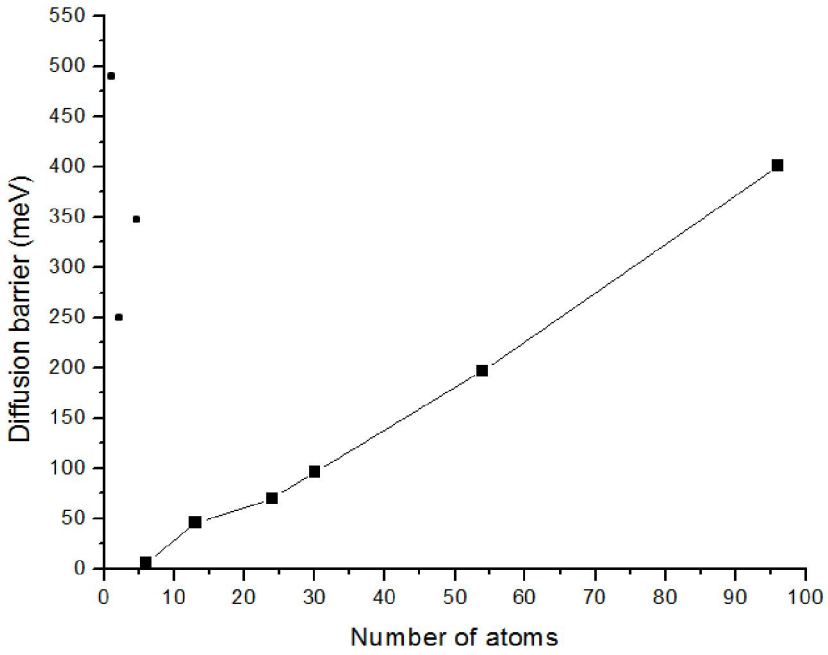


Fig. 4.5 Diffusion barriers for graphene-like clusters as a function of number of atoms. Also shown are the diffusion barriers for single carbon atoms, dimers, and tetramers.

4.7. Reference

1. Y. Ji, S. Lee, B. Cho, S. Song, and T. Lee, ACS Nano, 5, 5995 (2011).
2. Y. Yi, W. M. Choi, B. Son, J. W. Kim, and S. J. Kang, Carbon, 49, 4936 (2011).
3. T. Cui, R. Lv, Z.-H. Huang, H. Zhu, Y. Jia, S. Chen, K. Wang, D. Wu, and F. Kang, Nanoscale Research Letters, 7, 453 (2012).
4. Y. Sui and J. Appenzeller, Nano Letters, 9, 2973 (2009).
5. J. H. Deng, B. Yu, G. Z. Li, X. G. Hou, M. L. Zhao, D. J. Li, R. T. Zheng, and G. A. Cheng, Nanoscale, 5, 12388 (2013).
6. R. J. Sun, Y. Zhang, K. Li, C. Hui, K. He, X. C. Ma, and F. Liu, Applied Physics Letters, 103, 013106 (2013).
7. K. M. F. Shahil, and A. A. Balandin, Nano Letters, 12, 861 (2012).
8. M. Zhu, J. Wang, B. C. Holloway, R. A. Outlaw, X. Zhao, K. Hou, V. Shutthanandan, and D. Manos, Carbon, 45, 2229 (2007).
9. T. Yu, C. Kim, and B. Yu, "Highly Conductive 3D Nano-Carbon: Stacked Multilayer Graphene System with Interlayer Decoupling", arXiv:1103.4567 (2011).
10. M. C. Payne, M. P. Teter, D. C. Ailan, T. A. Arias, and J. D. Joannopouios, Reviews of Modern Physics, 64, 1045 (1992).
11. Chris G. Van de Walle, and Jorg Neugebauer, Journal of Applied Physics, 95, 3851 (2004).
12. P. Hohenberg, and W. Kohn, Physical Review, 136, B864 (1964).
13. V. Blum, R. Gehrke, F. Hanke, P. Havu, V. Havu, X. Ren, K. Reuter, and M. Scheffler, Computer Physics Communications, 180, 2175 (2009).

14. J. P. Perdew, K. Burke, and M. Ernzerhof, Physical Review Letters, 77, 3865 (1996).
15. A. Tkatchenko, and M. Scheffler, Physical Review Letters, 102, 073005 (2009).
16. L. Xian, and M. Y. Chou, Journal of Physics D: Applied Physics, 45, 455309 (2012).
17. K. W. Jacobsen, H. Jonsson, and G. Mills, "Nudged elastic band method for finding minimum energy paths of transitions," in Classical and Quantum Dynamics in Condensed Phase Simulations, edited by B. J. Berne, G. Ciccotti, and D. F. Coker (World Scientific, Singapore, 1998), p. 385.
18. G. Henkelman, and H. Jonsson, Journal of Chemical Physics, 113, 9978 (2000).
19. Q.-M. Zhang, C. Roland, P. Boguslawski, and J. Bernholc, Physical Review Letters, 75, 101 (1995).
20. G. Lippert, J. Dabrowski, M. C. Lemme, C. M. Marcus, O. Seifarth, and G. Lupina, Physica Status Solidi (b), 248, 2619 (2011).
21. G.-P. Dai, P. H. Cooke, and S. Deng, Chem. Physical Letters, 531, 193 (2012).
22. Z. Li, P. Wu, C. Wang, X. Fan, W. Zhang, X. Zhai, C. Zeng, Z. Li, J. Yang, and J. Hou, ACS Nano, 5, 3385 (2011).
23. Wei Zhang, Xinke Yu, Erica Cahyadi, Ya-Hong Xie, and Christian Ratsch, Applied Physics Letters, 105, 221607 (2014).

Chapter 5. Conclusion and future directions

5.1. Conclusion

Due to the challenges of the traditional ESD devices such as high leakage, high parasitic effects, slow response, large cost of IC area due to low electrical conductivity and heat dissipation efficiency, etc., novel interconnect material and ESD protection device and structure need to be developed. Graphene, due to its excellent electrical and thermal conductivity and strong mechanical strength, is a perfect candidate for the ESD application. First of all, it can replace copper wires as interconnects of IC, which can largely reduce the area cost of ESD structures due to its high electrical and thermal conductivity. This can help resolve the layout problem as well. By doing this, parasitic effects can also be minimized. Second, a novel electromechanical suspended GR ESD device is proposed based on the utilization of graphene's great mechanical strength, extremely high Young's modulus, and ultra light density. Compared to traditional ESD devices, the proposed suspended GR device is verified to have very low leakage due to its mechanical switch characteristic. And through careful design of the device dimensions, it can render ultra fast response time to meet the requirement of modern ESD 10^{-10}~10^{-9} s.

The proposed suspended GR ESD device is realized by careful design of the device dimensions and a new fabrication processing flow is developed. The new fabrication technique especially the usage of Si_3N_4 hard mask and HF vapor etching environment make the device fabrication more reliable with a high yield. Both direct current and transmission line pulse testing are conducted to demonstrate the turn-on behavior of the suspended GR device which indicate the feasibility of the proposed

device to be used for ESD protection. Three-terminal direct current measurements combined with COMSOL Finite Element Simulations are also carried out to study the mechanical shape evolution of GR under bias. Transmission line pulse testing for non-suspended GR device as interconnects is done to investigate the ESD robustness of GR. Monolayer and bilayer graphene both have higher breakdown current densities (3.34 x 10^8 A/cm^2 and 2.27 x 10^8 A/cm^2 respectively) than copper wires (~10^7 A/cm^2). Thicker graphene with more number of layers can provide better current drivability.

Ab initio calculations are carried out to study the growth mechanism of multilayer graphene. It is found that small carbon clusters are much more mobile than individual carbon adatoms on graphene surfaces. Due to the large diffusion length of carbon clusters, it is possible to conduct graphene epitaxial growth over graphene surfaces at low growth temperatures. Beyond a certain size of the cluster (24 atoms), a graphene-like structure is energetically preferred compared to a flat ring structure. The results indicate that the growth mode of graphene homoepitaxy is totally different from the 3-dimensional bulk materials, and growth proceeds rather differently, depending on the size and nature of the species that are being deposited.

5.2. Future directions

The proposed suspended GR ESD device have been successfully fabricated and measured. However, there are still some aspects to be discovered before this novel device structure can be utilized in ICs. In this section, some possible future directions are pointed out.

5.2.1. Device fabrication optimization

It has been mentioned that by using the developed process flow discussed in Chapter 3, higher reliability and yield can be obtained. However, there is still room for improvement.

First of all, graphene is transferred on an nonflat surface with Si_3N_4 trenches. Since the transfer process is in water environment, graphene will occasionally crack in the trench regions due to surface tension upon drying. This happens more often when the Si_3N_4 layer becomes thicker because there is more room for stretching GR thus rendering more stain on it. Also, graphene may not form good conformal contact with the trenched surface and become partially suspended if the mechanical restoring force is too large. This will harm the fabrication yield because the partially suspended regions would tend to be damaged during the subsequent processing steps. On the other hand Si_3N_4 layer cannot be too thin as well. Because otherwise, it won't be able to protect SiO_2 underneath during HFVE. Therefore, the optimization of the thickness of Si_3N_4 is necessary to achieve higher yield of workable devices.

Second, the CVD grown graphene quality and cleanness need to be further improved. It has been found that in some batches of graphene on Cu foil samples, the graphene film is not continuous or full of cracks, which will harm the yield of the subsequent device fabrication. Moreover, large amount of dark residues presumably to be carbon, PMMA, or Cu residues can be found in the transferred graphene. This will probably affect the performance of the suspended GR device in mainly two aspects: (i) The sites with residues will become defective spots where breakdown tends to happen first, which deteriorates the life time and reliability of the device; (ii) If the residues are in

the suspended GR region, the trigger voltage and response time will be largely affected. This renders uncertainty and uncontrollability of the device performance. Therefore, both the growth and transfer steps need to be improved to obtain better quality graphene.

Last, the exposed Si surface can be covered by Au, graphene or any other conducting films in order to prevent the oxidation. Otherwise, the surface contact between graphene and oxide would render a large contact resistance which is undesired for charge dumping.

5.2.2. Multilayer graphene

It has been mentioned that the graphene film thickness (h) is a key parameter for the suspended GR device since it affects both the trigger voltage and response time. Theoretically, thicker graphene film renders higher trigger voltage ($V_{trigger} \sim h^{3/2}$) and faster response time ($t_r \sim 1/h$). This can be studied and verified in future's experiments. Furthermore, in principle faster response time is desired and required by modern ESD protection standards, and it can be realized by using thicker graphene film. However, the trigger voltage will increase simultaneously. So careful design on the device parameters is very important which has be elaborated in Chapter 3. In order to realize the device design, well controlled growth of graphene is needed to get precise idea about the exact number of graphene layers to be used in the device fabrication. Therefore, experiments on graphene growth need to be done based on the ab initio calculation results discussed in Chapter 4 to further study the mechanism of graphene homo-epitaxy experimentally.

5.2.3. Reliability problem

As mentioned in Chapter 3, the trigger voltage tends to decrease if the device is turned on repeatedly. This may indicate a reliability problem that needs to be resolved. There may be presumably three causes for this problem: (1) sliding of GR towards the trench bottom; (2) plastic deformation of GR; (3) partial breakage of GR. Fig. 5.1 shows the SEM image of GR taking after the device is turned on for 5 times. The trigger voltage decreases from ~4 V to ~3.5 V. We may clearly see there is a slight bending of GR towards the bottom which should be the cause of decreased trigger voltage. However, more studies need to be conducted to find out if this is due to sliding, plastic deformation or any other possible reasons.

5.2.4. Snapback

As mentioned in Chapter 1, the snapback behavior is an important effect that may clamp the voltage to a safer level and provide better protection on ICs. However, the proposed suspended GR device doesn't have this property as is. Further research may be carried out to seek for possibilities of adding in this element or any other enhancement of the current device structure.

5.2.5. Current drivability

The breakdown current for monolayer graphene is tested to be in the order of several milliamperes per micrometer width. Although the current drivability may be improved by using multilayer graphene, appropriate doping, packaging, etc., which has be discussed in Chapter 3, compared to the huge current level in actual ESD event, more studies should still be done to further push the limit of graphene and seek for other

possibilities. There is still a long way to go before the proposed device structure can be utilized in real ESD applications.

5.2.5. Integration of proposed ESD device into ICs

The demonstration of the proposed suspended GR ESD device is not the end but a fresh start. The ultimate goal is to integrate the ESD device structure into ICs. In order to do this, simulations on a higher circuit level need to be done to develop the ESD circuit models. After this, design of practical device parameters and actual integration can be conducted to demonstrate the feasibility of utilizing the proposed ESD device structure in ICs.

5.3. Figures

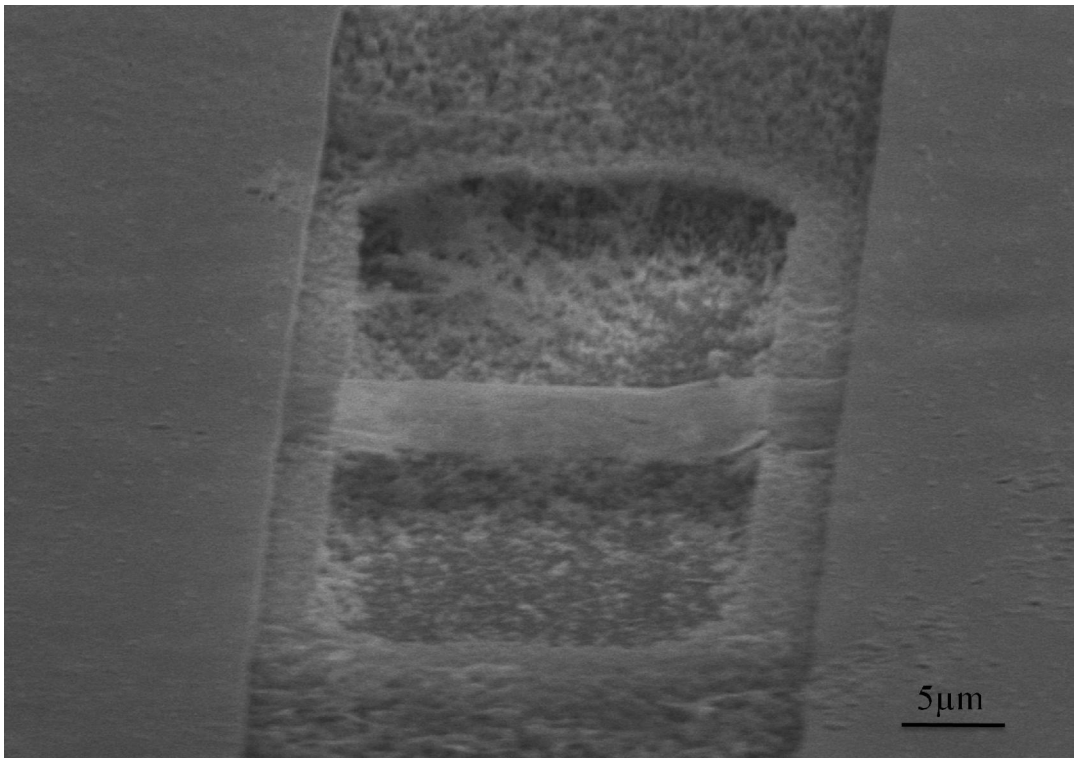


Fig. 5.1 SEM image showing possible sliding of GR after 5 times of device turn-on.