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Journal
Journal of Applied Physics, 108

Author
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Publication Date
2010

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Comparison of methods to quantify interface trap densities at dielectric/III-V semiconductor interfaces

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(Received 8 September 2010; accepted 23 October 2010; published online 16 December 2010)

Methods to extract trap densities at high-permittivity (k) dielectric/III-V semiconductor interfaces and their distribution in the semiconductor band gap are compared. The conductance method, the Berglund intergral, the Castagné–Vapaille (high-low frequency), and Terman methods are applied to admittance measurements from metal oxide semiconductor capacitors (MOSCAPs) with high-k/$In_{0.53}Ga_{0.47}As$ interfaces with different interface trap densities. The results are discussed in the context of the specifics of the $In_{0.53}Ga_{0.47}As$ band structure. The influence of different conduction band approximations for determining the ideal capacitance-voltage (CV) characteristics and those of the MOSCAP parameters on the extracted interface trap density are investigated. The origins of discrepancies in the interface trap densities determined from the different methods are discussed. Commonly observed features in the CV characteristics of high-k/$In_{0.53}Ga_{0.47}As$ interfaces are interpreted and guidelines are developed to obtain reliable estimates for interface trap densities and the degree of Fermi level (un)pinning for high-k/$In_{0.53}Ga_{0.47}As$ interfaces. © *2010 American Institute of Physics*. [doi:10.1063/1.3520431]

I. INTRODUCTION

The scaling of Si-based metal-oxide-semiconductor field-effect transistors (MOSFETs) is approaching limitations that are determined by the properties of the materials that are currently employed in these devices. One potential solution that would allow further scaling is to replace Si with alternative semiconductor channel materials. In particular, III-V semiconductors, such as (In,Ga)As solid solutions, have a lower electron effective mass than Si, allowing for high electron mobilities, and are thus of great interest for n-channel MOSFETs. Although the low electron effective mass is also accompanied by a low conduction band density of states (DOS), the increase in mobility overcompensates the resulting effective decrease in capacitance density.[1] The small band gap of In-rich (In,Ga)As solid solutions reduces the band bending required to populate the channel with carriers, allowing for lower operating voltages and less power dissipation. $In_{0.53}Ga_{0.47}As$ is of particular interest because it is lattice matched to InP substrates and to $In_{0.48}Al_{0.52}As$, which can be used as a back barrier to confine the electrons in the channel.[2]

To realize MOSFETs with III-V channels, suitable gate dielectrics must be developed, which must (i) form a stable interface within the thermal budget of the transistor fabrication process, (ii) possess a high dielectric constant and sufficient band offsets with the semiconductor conduction band to allow for scaling and low gate leakage, and (iii) have a low interface trap state density (D_{it}). While many high dielectric constant (k) dielectrics meet criteria (i) and (ii), achieving criterion (iii) has been proven to be extremely challenging. High interface trap densities cause inefficient Fermi level response or even Fermi level pinning, preventing control over the charge carriers in the channel and the realization of MOSFETs with good sub-threshold slopes and high drive currents. Unlike Si, III-V semiconductors do not possess high-quality native oxides with good stability, low leakage, and high breakdown fields. In addition, the III-V semiconductor surface itself may be prone to high D_{it}. Vacancies, antisite defects, or incomplete dimerization of the III-V surface can result in unsaturated bonds and form electrically active traps[3–5] that may be present even before high-k dielectric growth or are generated during the deposition.

Methods capable of quantifying D_{it}, the trap level energy position and the degree of Fermi level (un)pinning are critical in the development of high-quality high-k/III-V interfaces. For III-V devices, in particular, the characterization of metal-oxide-semiconductor capacitor (MOSCAP) structures is important as it is often impractical to fabricate full MOSFETs. The transistor fabrication process itself may introduce additional issues that should be addressed separately from the initial optimization of the high-k/III-V interface.[2] Methods to determine the D_{it} of dielectric/semiconductor interfaces using MOSCAP structures were developed for SiO_2/Si interfaces as far back as the 1960s.[6] Several factors, however, make the interpretation of the admittance response of high-k/III-V MOSCAPs in terms of D_{it} less straightforward than for Si. Specifically, the low conductance band DOS and different band gaps result in very different minority carrier response times. Furthermore, interfaces typically have very high D_{it}, with an energy distribution that is different from that of interfaces with Si.[7] As summarized in Table I for high-k/$In_{0.53}Ga_{0.47}As$ interfaces, many different methods have been employed, such as interpretation of shifts in the

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TABLE I. Summary of high-k/$In_{0.53}Ga_{0.47}As$ interface trap densities (D_{it}) reported in the literature. Unless indicated otherwise, the D_{it} was determined at room temperature. The acronyms in the table are defined as follows. ALD: atomic layer deposition, MBD: molecular beam deposition, PDA: postdeposition anneal, ICL: interface control layer, FG: forming gas, HV: high vacuum, UHV: ultrahigh vacuum, VB: valence band, CB: conduction band, BG: band gap, MG: midgap, ϕ_m: gate metal work function, $\Delta\psi_s$: surface potential swing. If the Berglund analysis was applied to a quasistatic CV measurement, this is indicated as BLQS, whereas if it was applied to a low-frequency curve this is indicated as BLA, respectively.

Semiconductor doping	High-k/ deposition method	Comments	D_{it} analysis method	D_{it} ($cm^{-2}\ eV^{-1}$) $\Delta\psi_s$ (eV)	Refs.
n/p-type $2\times10^{17}\ cm^{-3}$	Al_2O_3 ALD	$(NH_4)_2$ PDA:FG	Conductance	1×10^{12} (CB edge) 7×10^{12} (~MG) 2×10^{13} (VB edge)	8 and 9
				5×10^{12} (~MG) 3×10^{13} (VB edge)	
			Quasistatic CV	1.1 eV (total)	
n/p-type $5\times10^{16}\ cm^{-3}$	Al_2O_3 ALD_3	Fast transfer RTA 650 °C	Conductance	3×10^{12} (upper BG)	10
			Charge pumping	1×10^{12} (upper BG) 3×10^{11} (lower BG)	
			BLQS	1.0 eV total	
n/p-type $1\times10^{17}\ cm^{-3}$	Al_2O_3 ALD	As decap in FG/HV	BLA (5 kHz, 110 °C)	0.5 eV–1.1 eV	11 and 12
		PDA FG	Sensitivity to gate metal ϕ_m	0.7 eV after FG	
n/p-type $2\times10^{17}\ cm^{-3}$	Al_2O_3 ALD_3	$(NH_4)_2$ PDA FG (10% H_2)	Conductance	2×10^{13} (~MG) 3×10^{13} (VB edge)	13
p-type $1\times10^{17}\ cm^{-3}$	Al_2O_3 ALD	NH_3 native oxide etch	Castagné–Vapaille	1.4×10^{12} (~MG)	14
n-type $5\times10^{16}\ cm^{-3}$	Al_2O_3 ALD	Sulfur passivation PDA N_2	Conductance	1×10^{12} (~MG)	15
	Al_2O_3 ALD	As decap in UHV	Conductance	4×10^{12} (~MG)	
n-type $\sim3\times10^{18}\ cm^{-3}$	$LaAlO_3$ MBD		Conductance	1.5×10^{12} (~MG)	16
			Terman		
n-type $4\times10^{17}\ cm^{-3}$	HfO_2 ALD	No treatment/HCl, $(NH_4)_2S$, FG PDA	Conductance	$\geq1\times10^{13}$	17 and 18
n-type $5\times10^{17}\ cm^{-3}$	HfO_2 ALD	Self-cleaning	Terman	2×10^{12} (CB edge) 1×10^{12} (~MG) $>10^{13}$ (VB edge)	19
n-type $5\times10^{17}\ cm^{-3}$	HfO_2 ALD	FG PDA	Terman	2×10^{12} (midgap)	20
n/p-type $1\times10^{17}\ cm^{-3}$	HfO_2 MBD	As decap in UHV (2×4) reconstr. PDA N_2	Conductance	5×10^{11} (CB edge) $>10^{13}$ (~MG) 1×10^{12} (VB edge)	21
n-type $1\times10^{17}\ cm^{-3}$	ZrO_2 ALD	As decap in UHV (2×4) reconstr. PDA N_2	BLA (50 kHz, 72 °C)	>0.7 eV	22
			Sensitivity to gate metal ϕ_m		
n/p-type $3\times10^{17}\ cm^{-3}$	ZrO_2 ALD	PDA NH_3	Sensitivity to gate metal ϕ_m	$>10^{13}$ (~MG) 2×10^{12} (150 K)	23
n/p-type	ZrO_2 ALD	$LaAlO_3$ ICL	Conductance	10^{12} (MG 150 K)	24
		Al_2O_3 ICL		10^{12} (MG 150 K)	
n-type $1.7\times10^{17}\ cm^{-3}$	Si ICL, oxidation		Terman	3×10^{12} (~MG) 0.65 eV	25
n-type $1\times10^{16}\ cm^{-3}$	Si ICL, nitridation	PDA	Conductance BLQS	3×10^{11} (~MG) 0.65 eV	26

capacitance-voltage (CV) curves with gate metal work function,[11,23] the combined high-low frequency capacitance (Castagné–Vapaille) method,[14] the Terman (high-frequency capacitance) method,[16,19,20] the Berglund integral,[11,12,27] the conductance method,[8,10,13,15–18,21,24,28] and the Fermi level efficiency method.[29] As can be seen from Table I, reported D_{it} values differ by several orders of magnitude, ranging from low-$10^{11}\ cm^{-2}\ eV^{-1}$ to exceeding $10^{13}\ cm^{-2}\ eV^{-1}$. The wide range of reported D_{it} values is particularly confusing because the admittance responses appear often remarkably similar even with different surface preparation techniques, deposition methods, and interface passivation schemes. The discrepancies in the D_{it} values extracted from the same device using different methods can exceed half an order of magnitude.[8–10,13] There is substantial variation in the reported D_{it} even when similar sample preparation and D_{it} extraction methods were used.[9,13]

The goal of this paper is to compare the most commonly used methods, identify potential pitfalls and develop reliable and robust guidelines for the quantification of D_{it} of high-k/III-V interfaces. We use full impedance measurements of MOSCAPs of HfO_2/$In_{0.53}Ga_{0.47}As$ interfaces as examples, which are evaluated as a function of temperature for both n- and p-type channels (the sample details can be found in the Appendix). The examples are selected to represent different degrees of Fermi level (un)pinning and different D_{it}, to the extend that is currently possible. The underlying physical mechanisms giving rise to the different observed characteristics are not within the scope of this paper and will be covered elsewhere. Although the paper focuses on interfaces with $In_{0.53}Ga_{0.47}As$ as the channel, the conclusions and methodology can be applied to other III-V channels, provided that the appropriate modifications are made to account for the different semiconductor band structure.

The paper is organized as follows. In Sec. II, we discuss different methods to quantify D_{it} at high-k/$In_{0.53}Ga_{0.47}As$ in-

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terfaces, specifically, conductance (Sec. II A) and capacitance based methods (Sec. II B). Because the application of the conductance method to high-k/III-V interfaces has been discussed extensively in the literature,[28–30] it is treated somewhat more briefly here. We discuss the calculation of the theoretical, ideal (i.e., with no D_{it}) CV curve for interfaces with III-V semiconductors, as is needed for the CV-based methods (Sec. II B 2). Part of this Section is based in work published previously[31] but is included here for completeness and comparison. A main focus of Sec. II is then to compare the D_{it} values obtained by the different methods and to discuss the origins of differences in the extracted D_{it}. In Sec. III we discuss the implication of the results for commonly observed features in the CV characteristics of high-k/III-V MOSCAPs. Finally, in Sec. IV, we develop a methodology for the characterization of high-k/$In_{0.53}Ga_{0.47}As$ interfaces to obtain reliable estimates of D_{it} and Fermi level response.

II. METHODS TO DETERMINE THE D_{it} AT HIGH-k/InGaAs INTERFACES

Impedance measurements of MOSCAPs as a function of voltage, frequency, and temperature of high-k/semiconductor interfaces contain contributions from D_{it} that can be extracted in different ways. Figure 1(a) shows a schematic energy band diagram of a n-type MOSCAP in depletion. A dc gate bias, V_g, is applied to the metal gate and a small amplitude (~25 mV) ac signal with frequency f (typically between 1 MHz and 100 Hz) is superimposed. The gate bias induces a space charge and band bending, ψ_s, which determines the Fermi level position at the interface. The ac signal causes a periodic change in band bending and the Fermi level at the interface oscillates around the energy level position determined by the gate bias. Traps with energy levels that are located in proximity of the Fermi level can change their occupancy, provided that their response time τ is small so that they can follow the ac signal. CV and conductance-voltage (GV) curves are obtained by slowly sweeping the dc bias. Figure 1(b) shows an equivalent circuit model for a MOSCAP with interface trap states in depletion, which includes the gate oxide capacitance, C_{ox}, the semiconductor capacitance, $C_{dos}(\omega,\psi_s)$ and a series resistance, R_s. The interface trap density contributes an equivalent parallel interface trap capacitance, $C_{it}(\omega,\psi_s)$, and equivalent parallel conductance $G_p(\omega,\psi_s)$, respectively.[32] The frequency dependence is related to the characteristic trap response time, $\tau=2\pi/\omega$, where ω is the angular frequency ($\omega=2\pi f$). The trap response time is given by the Shockley–Read–Hall statistics of capture and emission rates:[13,33–35]

$$\tau=\frac{\exp[\Delta E/k_BT]}{\sigma v_{th}D_{dos}},\tag{1}$$

where ΔE is the energy difference between trap level E_T and majority carrier band edges (E_{CB} or E_{VB}, respectively), σ the capture cross section of the trap, v_{th} the average thermal velocity of the majority carriers, D_{dos} the effective DOS of the majority carrier band, k_B the Boltzmann constant, and T the temperature. The band bending ψ_s controls the interface trap level position E_T with respect to the bulk Fermi level E_F

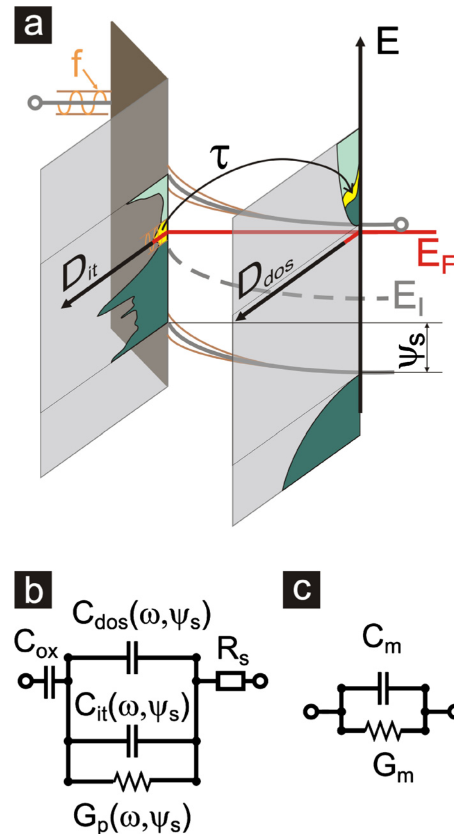

FIG. 1. (Color online) (a) Schematic showing the energy bands of an n-type MOSCAP in depletion. A dc gate bias V_g and a small ac signal of frequency f are applied, causing a band bending ψ_s in the semiconductor and an interface trap response with time constant τ. Also shown are the conduction and valence band DOS, D_{dos}, an arbitrary interface trap density distribution, the Fermi level E_F and the intrinsic level E_I. (b) Equivalent circuit of the MOSCAP in depletion, showing the oxide capacitance C_{ox}, the semiconductor capacitance $C_{dos}(\omega,\psi_s)$, the equivalent parallel interface trap capacitance $C_{it}(\omega,\psi_s)$, the equivalent parallel interface trap conductance $G_p(\omega,\psi_s)$ and a series resistance R_s. (c) Equivalent circuit of the impedance analyzer with measured capacitance C_m and conductance G_m.

and thus the trap occupancy. The interface trap capacitance is related to the interface trap density by $C_{it}=qD_{it}$, where q is the elemental charge, as long as D_{it} does not vary rapidly with energy level position.[6] The circuit model shown in Fig. 1(b) assumes that the minority carrier contribution is negligible. Modeling the measured admittance using the equivalent circuit shown in Fig. 1(b) is usually sufficient for the purpose of analyzing the D_{it} response of high-k/$In_{0.53}Ga_{0.47}As$ interfaces for which the admittance is governed by majority carrier response (see below). Figure 1(c) shows the equivalent circuit of the impedance analyzer with the measured capacitance, C_m, and conductance, G_m, that have to be corrected for series resistance R_s, which is determined from the measured accumulation impedance:[6]

$$R_s=\frac{G_{m,a}}{G_{m,a}^2+\omega^2C_{m,a}^2}.\tag{2}$$

The corrected capacitance and equivalent parallel conductance are then:

$$C_c=\frac{(G_m^2+\omega^2C_m^2)C_m}{[G_m-(G_m^2+\omega^2C_m^2)R_s]^2+\omega^2C_m^2},\tag{3a}$$

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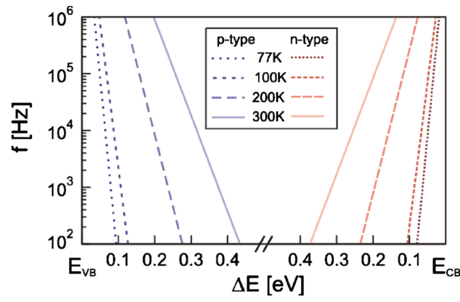

FIG. 2. (Color online) Characteristic trap frequency f calculated from Eq. (1) using a capture cross section $\sigma = 1\times10^{-16}$ cm^2 and values for average thermal velocity and the band DOS given in Table II. Here, ΔE is the energy difference between trap level E_T and the majority carrier band edges, E_{VB} or E_{CB}, respectively.

$$G_c = \frac{(G_m^2 + \omega^2 C_m^2)[G_m - (G_m^2 + \omega^2 C_m^2)R_s]}{[G_m - (G_m^2 + \omega^2 C_m^2)R_s]^2 + \omega^2 C_m^2}. \tag{3b}$$

All data shown below were corrected for series resistance and the measured total capacitance C_{tot} and measured conductance G_m always refer to the corrected values, C_c and G_c, respectively.

A. Conductance method

1. Basic principles

The conductance method is based on analyzing the loss that is caused by the change in the trap level charge state. Both the interface trap density, D_{it}, and the trap level energy position, E_T, are determined as follows. The equivalent parallel conductance G_p is related to the measured impedance by:

$$G_p = \frac{\omega^2 C_{ox}^2 G_m}{G_m^2 + \omega^2 (C_{ox} - C_m)^2}. \tag{4}$$

Interface traps in the proximity of Fermi level can change their occupancy. Their frequency dependent response depends on the trap time constant given by Eq. (1). Maximum loss occurs when interface traps are in resonance with the applied ac signal ($\omega\tau=1$). Assuming that surface potential fluctuations can be neglected, the D_{it} is estimated from the normalized parallel conductance peak, $(G_p/\omega)_{max}$:[6]

$$D_{it} \approx \frac{2.5}{Aq}\left(\frac{G_p}{\omega}\right)_{max}, \tag{5}$$

where A is the device area. To assign the trap level an energy position E_T in the band gap, the band bending-gate voltage relationship has to be determined, as described in Sec. II B 2. Alternatively, E_T can determined from the frequency at which G_p/ω is maximal and applying Eq. (1).[13,29] Figure 2 shows trap level position calculated from Eq. (1) using the values for the average thermal velocity and the band DOS for $In_{0.53}Ga_{0.47}As$ given in Table II and a capture cross section $\sigma = 1\times10^{-16}$ cm^2.[37] Given typical measurement frequencies between 100 Hz and 1 MHz, the D_{it} closer to the band edges (for $In_{0.53}Ga_{0.47}As$ channels) could then potentially probed by measuring the impedance at lower temperatures.[13,35] This will increase the trap response time and shift the resonance frequency back into the experimentally available frequency range. The limitations of this approach will be discussed below. The determination of E_T using Eq. (1) assumes a constant capture cross section σ that is independent of trap type and position in the band gap, which may not be the case. For GaAs σ can vary over orders of magnitude from 10^{-12} to 10^{-16} cm^2.[38] Data for σ of $In_{0.53}Ga_{0.47}As$ are scarce. Deep level transient spectroscopy measurements reported values in the range from 7×10^{-15} to 5×10^{-17} cm^2.[39–42] It should be noted, however, that E_T is relatively insensitive to errors in σ results, i.e., ~60 meV per decade error in σ at room temperature, with the error even smaller at lower temperatures.[13]

TABLE II. Average thermal velocity $v_{th} = \sqrt{3k_B T/m^*}$ and majority band DOS $D_{dos} = 2(2\pi m^* k_B T/h^2)^{3/2}$ for the calculation of trap response time τ. Electron and hole effective masses for $In_{0.53}Ga_{0.47}As$ were taken from Ref. 36.

	n-type		*p*-type	
T (K)	v_{th} (cm/s)	D_{dos} (cm^{-3})	v_{th} (cm/s)	D_{dos} (cm^{-3})
300	5.6×10^7	2.2×10^{17}	1.7×10^7	7.8×10^{18}
200	4.6×10^7	1.2×10^{17}	1.4×10^7	4.3×10^{18}
100	3.3×10^7	4.3×10^{16}	1.0×10^7	1.5×10^{18}
77	2.9×10^7	2.9×10^{16}	8.7×10^6	1.0×10^{18}

2. Extraction of interface properties from the conductance method

The main advantage of the conductance method is that the D_{it} can be determined directly from the experiment, using Eq. (5). Furthermore, the efficiency of band bending and Fermi level movement with gate bias can also be observed directly; they are correlated with the shift in the frequency of the maximum of the normalized conductance peak as a function of gate bias.[29] As an example, Fig. 3 shows conductance maps of thick (~35 nm) $HfO_2/In_{0.53}Ga_{0.47}As$ MOSCAPs that were annealed in nitrogen, on both p- and n-type $In_{0.53}Ga_{0.47}As$, respectively, at temperatures between 100 and 300 K. These maps show the magnitude of the normalized parallel conductance $(G_p/\omega)/Aq$ (see color scale) as a function of ac frequency f and the gate voltage V_g. The D_{it} is estimated by multiplying the peak value, $[(G_p/\omega)/Aq]_{max}$ (see contour lines) with a factor of ~2.5 [see Eq. (5)]. By tracing the maximum, $[(G_p/\omega)/Aq]_{max}$, across the maps, a measure of the degree of band bending in response to an applied gate voltage is obtained.[29] Specifically if $[(G_p/\omega)/Aq]_{max}$ moves vertically across the map the band bending is efficient. In contrast, the frequency shift with gate bias is negligible if the Fermi level is pinned or if the semiconductor is in weak inversion. For the MOSCAP shown in Fig. 3, the conductance is large and band bending is not efficient at 300 K. The conductance peak maximum does not move to frequencies less than 500 Hz for p-type and 2 kHz for n-type, respectively. Comparing these frequencies with Fig. 2, it can be seen that the Fermi level at the interface cannot be moved into the midgap energy range, i.e., into the region of 0.4 eV above the valence band or to below 0.3 eV below the conduction band edge, respectively. It should be noted that if the capture cross section, σ, is significantly

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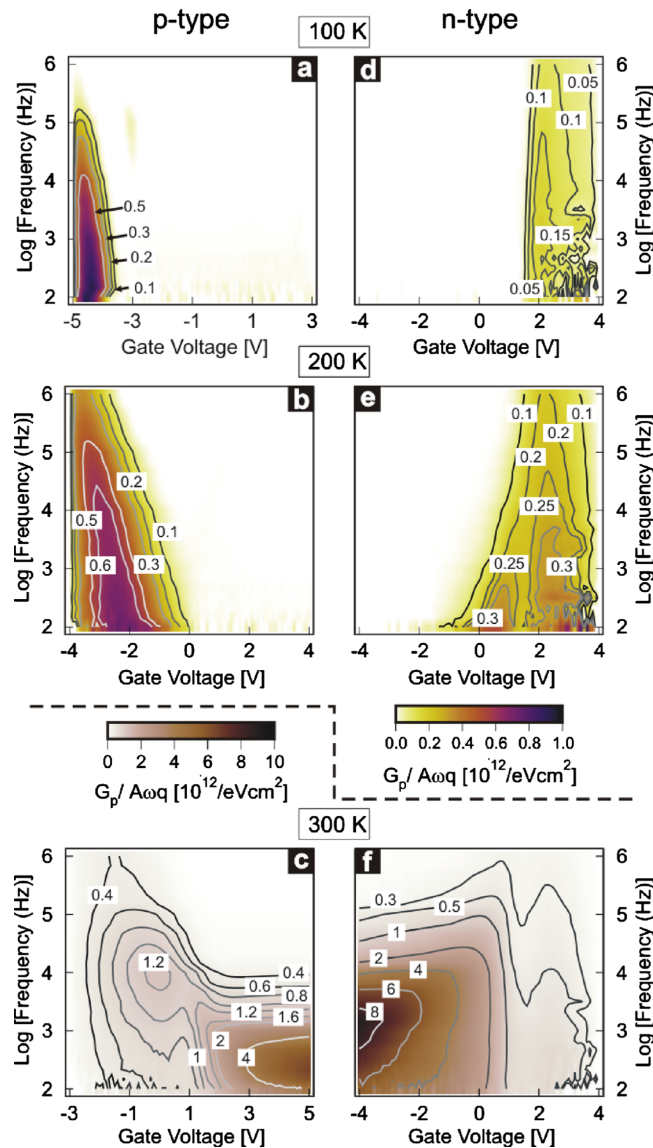

FIG. 3. (Color online) Map of the normalized parallel conductance, $(G_p/\omega)/Aq$, as a function of gate bias V_g and frequency f measured at 300 K, 200 K, and 100 K for MOSCAPs with HfO_2 on n- (right column) and p-type (left column) $In_{0.53}Ga_{0.47}As$, respectively. The HfO_2 film was about 30 nm thick and was annealed in nitrogen after deposition. The scale bars can be used to extract the $(G_p/\omega)/Aq$ peak values, which are also given at the contour lines in the maps. Note the two different scale bars for the low temperature (100 K and 200 K) and 300 K measurements, respectively.

smaller than what was assumed here ($\sigma=10^{-16}$ cm^2), as recent measurements indicate,[43] then the midgap region over which the Fermi level is moved would become even smaller. The conductance maps are very similar to those obtained for MOSCAPs with other dielectrics, such as $Al_2O_3/In_{0.53}Ga_{0.47}As$.[44]

For comparison, Fig. 4 shows a conductance map for a *forming gas* annealed n-type MOSCAP with a thinner (~9 nm) HfO_2/n-$In_{0.53}Ga_{0.47}As$ MOSCAP measured at 300 K. Here the conductance peak moves to different frequencies with gate bias, showing that the conductance method is indeed sensitive to changes in the degree of Fermi level pinning. The Fermi level moves efficiently between about 0.15 to 0.3 eV below the conduction band.

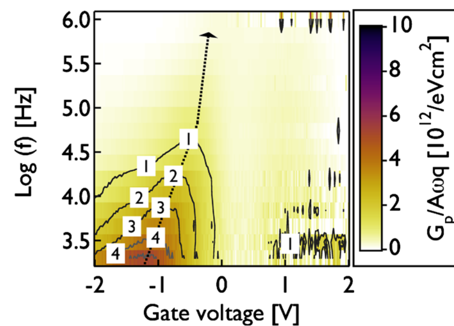

FIG. 4. (Color online) Normalized parallel conductance, $(G_p/\omega)/Aq$, as a function of gate voltage and frequency f measured at 300 K for a 9 nm HfO_2/n-$In_{0.53}Ga_{0.47}As$ MOSCAP that was forming gas annealed. The scale bar can be used to extract the $(G_p/\omega)/Aq$ peak values, which are also given at the contour lines in the map. The dotted-line arrow is a guide to the eye to trace the position of the $(G_p/\omega)/Aq$ maximum in the depletion region.

3. Issues and limitations

A serious potential issue of the conductance method when applied to high-k/III-V interfaces is that the standard conductance method, as developed in textbooks for Si interfaces,[6] is based on an expression of the parallel conductance derived by Lehovec.[32] This expression assumes that the D_{it} and capture cross section are independent of energy, which is a good approximation for Si. If these conditions are not satisfied the conductance peak due to interface traps may exhibit a strong asymmetry, which limits the applicability of the conductance method, as discussed in Ref. 6. The fact that a strong asymmetry of the conductance peak as a function of frequency is often observed at high-k/III-V interfaces indicates that the standard conductance method may have to be revised to take into account the nonuniform D_{it} distribution of high-k/III-V interfaces.

A limitation of the conductance method that has already been pointed out in the literature is that it cannot provide quantitative estimates of the D_{it} for interfaces with a large D_{it}, i.e., typical high-k/III-V interfaces. Specifically, if the interface trap capacitance is larger than oxide capacitance, i.e., $C_{ox}<qD_{it}$, the measured impedance is dominated by the oxide capacitance and the D_{it} is underestimated.[28,45] Finally, for $4C_{ox}<qD_{it}$ the extracted parallel conductance becomes insensitive to D_{it}.[28,29,45] For example, the $[(G_p/\omega)/Aq]_{max}$ values measured at 300 K for the n-MOSCAP annealed in nitrogen shown in Fig. 3 give a maximum D_{it} near midgap of $\sim 2\times10^{13}$ cm^{-2} eV^{-1}. For the MOSCAP annealed in forming gas a maximum D_{it} of $\sim 10^{13}$ cm^{-2} eV^{-1} is obtained (Fig. 4). This appears to be a small change, particularly considering the large difference in Fermi level movement observed for the two MOSCAPs. However, for the MOSCAP shown in Fig. 3, $4C_{ox}<qD_{it}$ and the extracted D_{it} is at best a lower bound. For the gate stack shown in Fig. 4, $C_{ox}>qD_{it}$ and the D_{it} estimate should be more reliable.

Disadvantages of the conductance method also include the sensitivity of the results to C_{ox}, which must be determined from an independent measurement. In contrast to Si, using the accumulation capacitance to estimate C_{ox} is not possible for n-type channels, because of the low conduction band DOS of III-V semiconductors (see Sec. II B). If C_{ox} is *overestimated*, the estimates for G_p/ω will be too low [see

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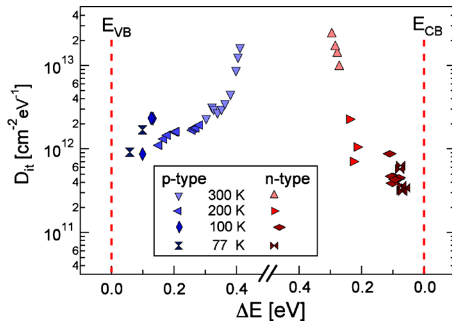

FIG. 5. (Color online) $HfO_2/In_{0.53}Ga_{0.47}As$ interface trap distribution as determined from conductance maps shown in Fig. 3. Here, ΔE is the energy difference between trap level E_T and the majority carrier band edges, E_{VB} or E_{CB}, respectively.

Eq. (4)]. The D_{it} will be *underestimated* and the $[(G_p/\omega)/Aq]_{max}$ peak position shifts toward smaller frequencies, causing the band bending to be *overestimated*.

Additional sources of error in determining the D_{it} from the conductance method include the onset of weak inversion.[28] In weak inversion, the conductance increases due to the contribution of minority carrier generation-recombination.[28] Assigning the measured conductance solely to interface trap response causes the D_{it} to be overestimated. As will be discussed in Sec. III, weak or strong inversion is not typically observed for high-$k/In_{0.53}Ga_{0.47}As$ interfaces and the effect of minority carrier generation on D_{it} extraction will not be discussed here.

The factor of 2.5 in Eq. (5) implies a negligible lateral variation in the surface potential.[46] Neglecting the effect of band bending fluctuations D_{it} analysis may cause the D_{it} extracted from the conductance method to be underestimated.

We next discuss the use of low-temperature conductance measurements[13,21,24,44] to obtain D_{it} values closer to the band edges for $In_{0.53}Ga_{0.47}As$ channels. As seen from Fig. 2, the D_{it} closer to the band edges could potentially be probed by measuring the impedance at lower temperatures. Figure 3 shows that the conductance values decrease dramatically at lower temperatures, in particular for the *n*-type sample. The trace of the conductance peak maximum in these maps becomes more vertical with decreasing temperature and narrows, which could be interpreted as a decrease in D_{it} from midgap toward the band edges. Figure 5 shows the D_{it} values as a function of their position in the band gap, as extracted from the conductance maps shown in Fig. 3 and using Fig. 2 to assign the trap level position in the band gap. Closer to the band edges D_{it} appears to decrease by more than an order of magnitude, to 1×10^{12} cm^{-2} eV^{-1} and 5×10^{11} cm^{-2} eV^{-1} near valence band and conduction bands, respectively. Similar D_{it} distributions, with sharp drop near the band edges have been reported in the literature for other high-*k*/III-V interfaces using the conductance method.[35,44] However, the low-temperature measurements do not account for the entire D_{it} that responded at room temperature. For example, a freezing of D_{it} response was reported in low-temperature charge pumping measurement for high-$k/In_{0.53}Ga_{0.47}As$ gate stacks.[24] Traps that are filled at low temperature may remain in their charged state, causing *CV* curves to appear steeper[47,48] and will not contribute to the measured loss. At lower temperatures the thermal broadening of the Fermi–Dirac distribution is reduced. As the trap states that contribute to the loss measured in the conductance method are located in close proximity of the Fermi level within the thermal broadening, there are fewer traps responding at lower temperature, thus the total D_{it} appears reduced. We conclude here, based on the experimental observations, that the conductance method is not suited to provide reliable estimate of the D_{it} near the band edges for high-$k/In_{0.53}Ga_{0.47}As$ gate stacks.

B. Capacitance-voltage based methods

1. Basic principles

The total capacitance of the MOS structure [see Fig. 1(b)] is given by:

$$\frac{1}{C_{tot}} = \frac{1}{C_{ox}} + \frac{1}{C_{it}+C_{dos}}. \quad (6)$$

The D_{it} can then be determined from C_{it} if C_{dos} and C_{ox} are known. "low-frequency" *CV* methods are based on measuring the total capacitance, C_{tot}^{lf}, at frequencies that are sufficiently low so that all traps can follow the ac signal. By ramping the gate bias slowly and measuring the displacement current ("quasistatic measurement"), the interface traps are in equilibrium with the applied ac voltage ($C_{it}=qD_{it}$), yielding:[6]

$$D_{it} = \frac{1}{q}\left(\frac{C_{ox}C_{tot}^{lf}}{C_{ox}-C_{tot}^{lf}} - C_{dos}\right). \quad (7)$$

C_{ox} can be determined experimentally from a thickness series and $C_{dos}(\psi_s)$ from a *CV* curve measured at sufficiently high frequencies C_{tot}^{hf}, so that interface trap can *not* follow the ac signal ($C_{it}=0$). The semiconductor capacitance is then given by $C_{dos}^{-1}=C_{tot}^{hf-1}-C_{ox}^{-1}$. Using the total capacitance from both high and low frequency measurements, the D_{it} can be obtained (Castagné–Vapaille method):[49]

$$D_{it}(V_g) = \frac{C_{ox}}{q}\left(\frac{C_{tot}^{lf}}{C_{ox}-C_{tot}^{lf}} - \frac{C_{tot}^{hf}}{C_{ox}-C_{tot}^{hf}}\right). \quad (8)$$

To determine the trap level position the band bending as a function of the gate voltage is needed, as described in Sec. II B 2. Alternatively the bend bending has sometimes been calculated using the Berglund integral:[50]

$$\psi_s = \psi_s^0 + \int_{V_g^0}^{V_g}\left(1 - \frac{C_{tot}^{lf}(V_g)}{C_{ox}}\right)dV_g, \quad (9)$$

where ψ_s^0 corresponds to the band bending at V_g^0. It is important to choose a gate voltage V_g^0 at which band bending does not strongly vary with bias, such as in accumulation or inversion, to reduce offsets in the band bending gate voltage dependence. As will be discussed below (Sec. II B 2), for III-V semiconductors there is considerable band bending in accumulation as the Fermi level resides within the conduction band. This makes the utility of the Berglund method for interfaces with III-V semiconductors questionable.

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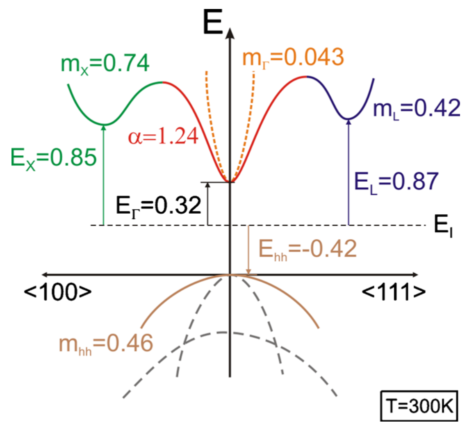

FIG. 6. (Color online) Schematic band structure of $In_{0.53}Ga_{0.47}As$ using the parameters from Ref. 36 for $T=300$ K. The minimum energies of the conduction band valleys are given in eV with respect to the intrinsic energy level E_I located 0.42 eV above the valence band maximum. The effective DOS masses m^* are given in units of the free electron mass and the nonparabolicity parameter α of the Γ valley is in units of per electron volt. The index indicates the conduction band valley location. For the valence band only the heavy hole band was included in the *CV* modeling.

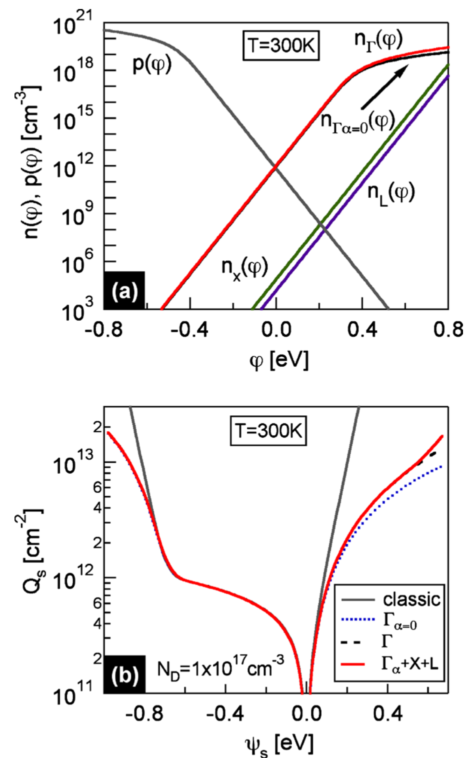

FIG. 7. (Color online) (a) Electron (n) and hole (p) concentration as a function of semiconductor potential $\varphi=(E_F-E_I)/q$, at $T=300$ K calculated from Eqs. (12) and (13) using different approximations for the semiconductor band structure. The subscripts indicate for which valley the charge carrier concentration is shown. The parabolic Γ-valley approximation is labeled with a subscript $\alpha=0$. (b) Semiconductor sheet charge Q_s as a function of band bending ψ_s for n-type $In_{0.53}Ga_{0.47}As$ ($N_D=10^{17}$ cm^{-3}, $\varepsilon_s=13.9$, $T=300$ K) calculated from Eq. (14) using different band structure approximations. The "classical" result using Boltzmann approximation is shown for comparison.

The D_{it} can also be obtained from a high frequency *CV* curve (Terman method). The total capacitance is measured at sufficiently high frequencies to not contain any ac contribution from interface traps. The only influence of interface traps on the *CV* curve is a stretch-out with gate bias, because the trap occupancy changes with gate bias. The stretch-out ($d\psi_s/dV_g$) is quantified by comparison with an ideal *CV* curve, and yields:[51]

$$D_{it}(\psi_s) = \frac{C_{ox}}{q}\left[\left(\frac{d\psi_s}{dV_g}\right)^{-1} - 1\right] - C_{dos}(\psi_s). \tag{10}$$

A prerequisite for the *CV*-based methods is that the measured low frequency and high frequency *CV* curves are indeed true low and high frequency *CV* curves. That is, all traps should contribute to C_{tot}^{lf}, whereas C_{tot}^{hf} should not contain any ac trap contribution; otherwise the D_{it} extraction is erroneous.

Most importantly, *CV* methods require a realistic model of the semiconductor to calculate the theoretical *CV* curve. Because of the differences in the electronic structure, approximations that work well for Si are not applicable to high-k/III-V interfaces. To further discuss D_{it} extraction from *CV* measurements, modeling of the theoretical *CV* curve is described first (Sec. II B 2), using high-$k/In_{0.53}Ga_{0.47}As$ MOSCAPs as the example.

2. Theoretical CV characteristics of high-k/In$_{0.53}$Ga$_{0.47}$As MOSCAPs

For interfaces with Si, theoretical *CV* curves are normally calculated using a charge carrier density at the semiconductor surface that is described by a Boltzmann distribution function,[6] referred to in the following as the "classical" approximation. It is valid only when the semiconductor Fermi level remains within the band gap for all applied gate biases. $In_{0.53}Ga_{0.47}As$ has a small electron effective mass, m^*, and thus a small conduction band DOS. For large C_{ox}, the electric field applied to the semiconductor becomes large and the Fermi level moves deep into the conduction band, calling the classical approximation into question. Additionally, the nonparabolicity of the lowest conduction band valley (Γ) and the population of the higher lying conduction band valleys, X and L, have to be taken into account. The nonparabolicity is described by a parameter α, defined as $\alpha=(1-m^*)^2/E_g$.[52] Figure 6 shows a schematic of the band structure of $In_{0.53}Ga_{0.47}As$ using the parameters given in Ref. 36 at $T=300$ K. For the valence band a single, parabolic band approximation is sufficient because of the large split-off energy and the larger DOS. We next describe an approach to model the theoretical *CV* curve for high-$k/In_{0.53}Ga_{0.47}As$ MOSCAPs that takes these considerations into account.

The ideal semiconductor capacitance is modeled by assuming a semi-infinite, semiconductor with constant doping concentration. The interface is located at $x=0$. Charge quantization effects have been shown to be negligible and are not included here.[53] It is further assumed that the DOS does not change upon applying an electric field and the gate bias only affects the band bending in the semiconductor. The electrostatic potential is defined as $\varphi(x)=(E_F-E_I)/q$, where E_F is the Fermi level and E_I the intrinsic energy level in the semiconductor, and is related to the charge density $\rho(x)$ by the one-dimensional Poisson equation:

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$$\frac{d^2\varphi(x)}{dx^2} = -\frac{\rho(x)}{\varepsilon_s} = -\frac{q\{p[\varphi(x)] - n[\varphi(x)] + N_D - N_A\}}{\varepsilon_s}, \tag{11}$$

where N_D and N_A are the charge densities from donors and acceptors, respectively, and ε_s is the dielectric constant of the semiconductor. The charge densities of the mobile carriers, denoted $n[\varphi(x)]$ for electrons and $p[\varphi(x)]$ for holes, depend on the electrostatic potential. The electron density in the Γ valley is given by:[54]

$$n_\Gamma[\varphi(x)] = \frac{4}{\sqrt{\pi}}\left(\frac{2\pi k_B T m_\Gamma^*}{h^2}\right)^{3/2} \times \int_0^\infty \frac{\sqrt{\eta_\Gamma}(1+\alpha\eta_\Gamma)(1+2\alpha\eta_\Gamma)}{\exp\left[\eta_\Gamma - \frac{q\varphi(x)}{k_B T} + \delta_\Gamma\right] + 1} d\eta_\Gamma. \tag{12}$$

Here, $\eta_\Gamma = (E - E_\Gamma)/k_B T$ is the normalized electron kinetic energy, and $\delta_\Gamma = (E_\Gamma - E_I)/k_B T$ the reduced energy band offset with respect to the intrinsic level E_I. In the parabolic band approximation $(\alpha \to 0)$ Eq. (12) reduces to:

$$n_i[\varphi(x)] = \frac{4}{\sqrt{\pi}}\left(\frac{2\pi k_B T m_i^*}{h^2}\right)^{3/2} \times \int_0^\infty \frac{\sqrt{\eta_i}}{\exp\left[\eta_i - \frac{q\varphi(x)}{k_B T} + \delta_i\right] + 1} d\eta_i, \tag{13}$$

where the subscript $i = \mathrm{X,L}$ refers to the higher lying conduction band valleys. Summation over all valleys gives the total electron density in the conduction band $n[\varphi(x)] = \Sigma_{i=\Gamma,X,L} n_i[\varphi(x)]$. For the hole density, $p[\varphi(x)]$, the corresponding expression is used. The electric field at the semiconductor surface, $E[\varphi(x=0)]$, is obtained by integrating Eq. (11). Applying Gauss's law yields the total charge Q_s per unit area in the semiconductor:

$$Q_s(\psi_s) = \varepsilon_s E[\varphi(x=0)] = -\mathrm{Sign}(\psi_s)\sqrt{2\int_{\varphi_b}^{\varphi_b+\psi_s} - q\varepsilon_s\{N_D - N_A + p[\varphi(x)] - n[\varphi(x)]\}d\varphi(x)}, \tag{14}$$

where $\psi_s = \varphi_s - \varphi_b$ is the total band bending in the semiconductor, representing the potential difference at the semiconductor surface φ_s with respect to the bulk potential φ_b.

Figure 7(a) shows the carrier concentration as a function of semiconductor potential φ, i.e., Fermi level position E_F with respect to the intrinsic energy level E_I, calculated from Eqs. (12) and (13) at $T = 300$ K. The population density in the higher lying valleys is much smaller compared to the Γ valley. The carrier concentration in the X valley is larger than in the L valley because it has a slightly lower energy and smaller energy dispersion. Larger electron concentrations are obtained in the Γ valley when taking the nonparabolicity into account. The difference between parabolic and nonparabolic approximations increases as the Fermi level moves deeper into the conduction band. The semiconductor charge, Q_s, calculated from Eq. (14) for n-type $In_{0.53}Ga_{0.47}As$ ($N_D = 10^{17}$ cm^{-3}, $\varepsilon_s = 13.9$, $T = 300$ K) using different band structure approximations is shown in Fig. 7(b). For a nonparabolic Γ valley Q_s increases more rapidly with band bending. The population of higher lying valleys is only relevant for a positive band bending larger than 0.4 eV. A negative band bending of $\psi_s < -0.6$ eV is needed to form an inversion layer. The result using the Boltzmann distribution is also shown in Fig. 7(b). It can be seen that using the Boltzmann distribution causes the semiconductor carrier concentration to be overestimated in accumulation and inversion. Thus, as has also been pointed out in the literature,[8,53,55,56] the classical approach is not applicable for small effective mass semiconductors such as $In_{0.53}Ga_{0.47}As$.

The ideal semiconductor capacitance $C_{dos}(\psi_s)$ is directly calculated by differentiating Eq. (14) with respect to ψ_s:

$$C_{dos}(\psi_s) = -\frac{dQ_s(\psi_s)}{d\psi_s}. \tag{15}$$

The gate voltage causing the band bending ψ_s is calculated from:

$$V_g = \psi_s + \Delta\phi_{ms} - \frac{Q_s(\psi_s)}{C_{ox}}, \tag{16}$$

where $\Delta\varphi_{ms}$ is the work function difference between gate metal and semiconductor.[6] Figure 8 shows total capacitance and band bending of an ideal ($C_{it} = 0$) n-MOSCAP for the different conduction band models, calculated from Eqs. (6), (15), and (16) for a donor concentration $N_D = 1 \times 10^{17}$ cm^{-3} and an equivalent oxide thickness (EOT) of 3 nm ($C_{ox} = 1.15$ μF/cm^2) at $T = 300$ K. The ideal high frequency CV curve in inversion is shown as well, which was calculated following Ref. 57 by taking the ac inversion layer polarization effect into account. In depletion, high frequency and low frequency capacitance are in good agreement. The results using the classical approximation are also shown. The different models agree in depletion because the semiconductor charge is governed by the immobile donors and not affected by the details of the band structure. In contrast, they predict very different CV characteristics in accumulation.[53,56,58] The classical CV curve does not reveal the asymmetry due to the difference in the DOS of valence and conduction bands, respectively. The parabolic Γ valley approximation underestimates the increase in semiconductor charge with band bend-

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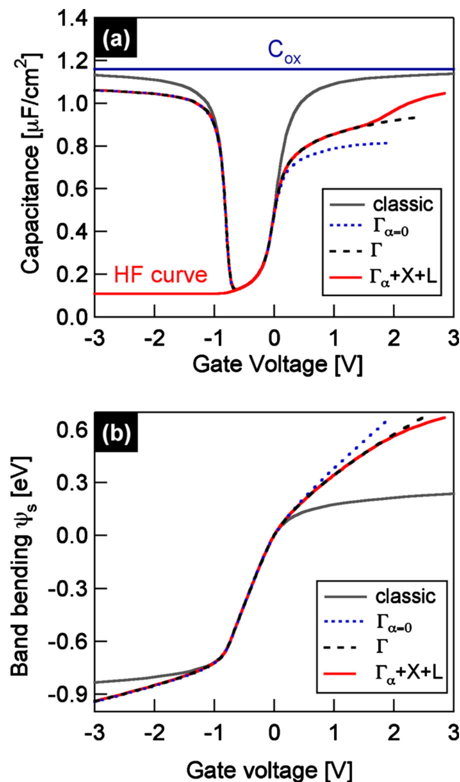

FIG. 8. (Color online) (a) *CV* and (b) band bending of an ideal *n*-MOSCAP with a donor concentration $N_D = 1\times10^{17}$ cm^{-3} and an oxide capacitance $C_{ox} = 1.15$ μF/cm^2, calculated using different approximations for the band structure.

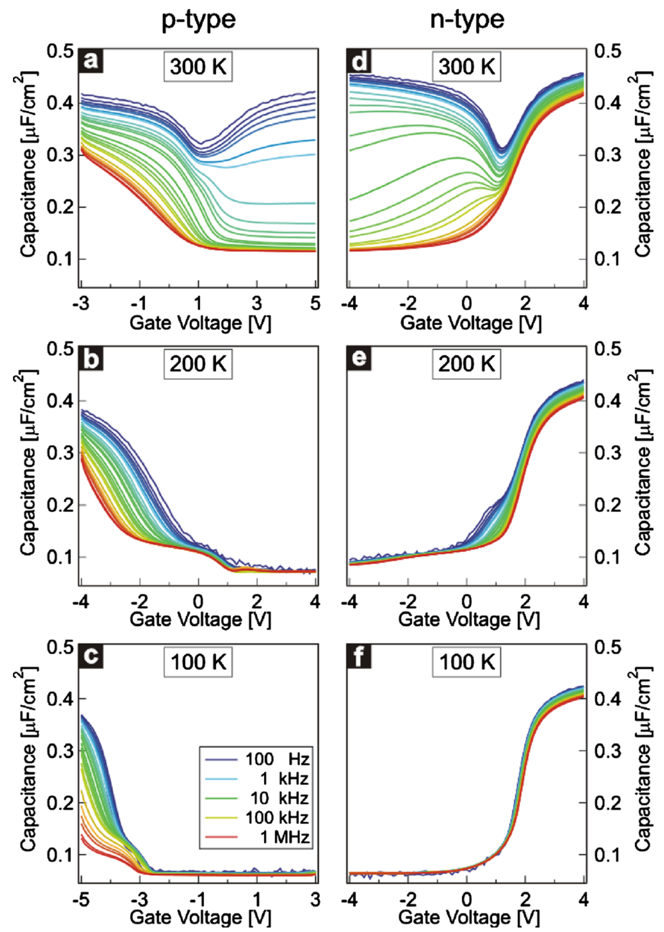

FIG. 9. (Color online) Frequency-dependent *CV* characteristics measured at 300 K, 200 K, and 100 K for MOSCAPs with HfO_2 on *n*- (right column) and *p*-type (left column) $In_{0.53}Ga_{0.47}As$, respectively. The HfO_2 film was about 30 nm thick and was annealed in nitrogen after deposition. The conductance data of this MOSCAP are shown in Fig. 3.

ing and thus the semiconductor capacitance, causing the asymmetry in the *CV* to be overestimated. At a gate bias of 1 V, C_{dos} is 25% lower compared to the nonparabolic case. The upturn of the capacitance for gate voltages exceeding 1.5 V, at a band bending $\psi_s > 0.4$ eV, is due to the population of the higher lying conduction band valleys. In accumulation, band bending [Fig. 8(b)] is slightly overestimated in the parabolic case and strongly underestimated using the classical approach.

3. Extraction of interface properties from capacitance-based methods

To discuss the *CV*-based methods and the information that can be extracted, experimental results from two differently treated $HfO_2/In_{0.53}Ga_{0.47}As$ MOSCAPs are shown in Figs. 9–11. We discuss their *CV* characteristics qualitatively first, before quantitatively determining band bending and D_{it} using *CV*-based methods.

Figure 9 shows *CV* curves of a MOSCAP with a thick (35 nm) HfO_2 film on *n*- and *p*-type $In_{0.53}Ga_{0.47}As$, respectively, measured at temperatures between 300 K and 100 K (the conductance results for this MOSCAP are shown in Fig. 3). For *p*-type, the semiconductor never reaches accumulation. At room temperature and positive gate bias the capacitance does not change with gate voltage, i.e., the MOSCAP appears to be fully depleted; however, the minimum capacitance for the doping level (1×10^{17} cm^{-3}) in the semiconductor ($C_{min} = 0.1$ μF/cm^2) is *not* reached. At 300 K, pronounced frequency dispersion is seen at positive bias, which is completely suppressed at lower temperature. The *CV* curves shift to more negative gate bias with decreasing temperature. The horizontal shift can be explained with the shift in the Fermi level closer to the valence band at lower temperatures. If the D_{it} near the valence band is high, then larger negative gate biases are needed at lower temperatures for the same band bending in the semiconductor to compensate the charge due the interface traps, causing a horizontal shift in the *CV*. The very large shift indicates a high D_{it} close to the valence band edge. For the *n*-type MOSCAPs, accumulation is achieved at positive gate bias. At negative gate voltages ($V_g < -1$ V) the total capacitance of the 1 MHz curve does not change with gate bias; however, the theoretical minimum capacitance is again not reached. The increase in capacitance with decreasing frequency at negative bias seen at 300 K is completely suppressed at 200 K and below. Furthermore, the minimum capacitance measured at these temperatures is lower than the theoretical value. It is likely that at low temperatures, some traps do not respond to the ac signal or dc sweep. The MOS structure cannot maintain thermal equilibrium with the gate bias because traps do not change their charge state. To maintain charge neutrality majority carriers are depleted beyond the maximum carrier depletion width, driving the semiconductor into deep depletion. The effect of

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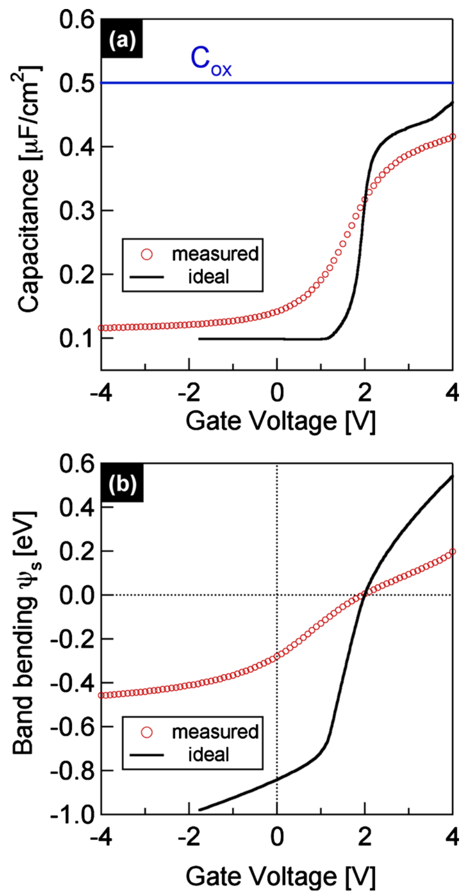

FIG. 10. (Color online) (a) Comparison of the experimental 300 K/1 MHz *CV* of the *n*-type $HfO_2/In_{0.53}Ga_{0.47}As$ MOSCAP shown in Fig. 9 with a calculated ideal high frequency *CV*. The oxide capacitance, C_{ox}, is also shown. (b) Experimental band bending ψ_s vs gate voltage V_g as determined by the Terman method. The ideal band bending is shown for comparison.

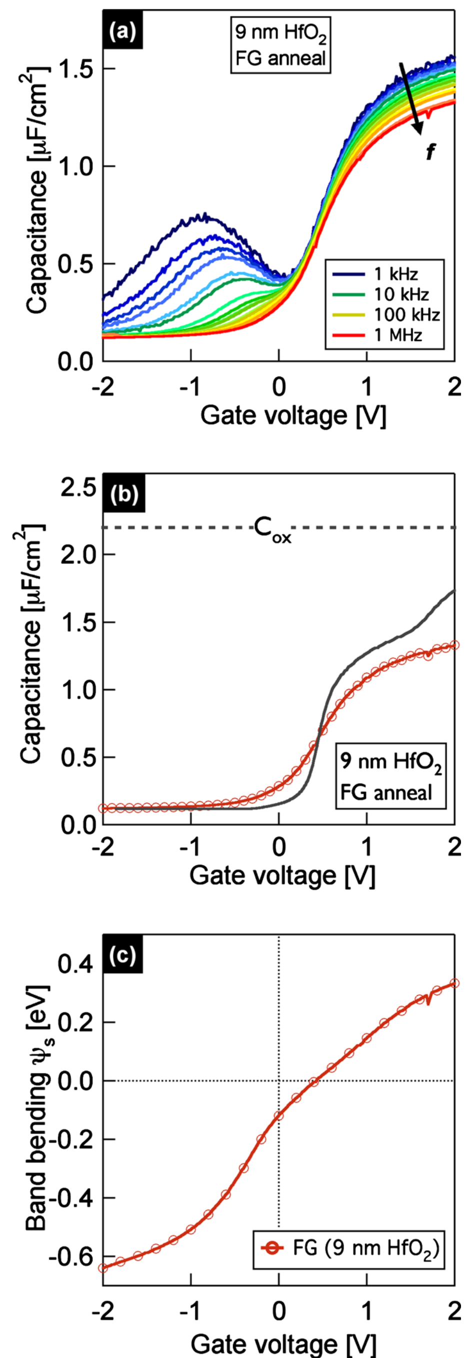

FIG. 11. (Color online) (a) Frequency-dependent *CV* characteristics of a 9-nm-thick HfO_2/n-type $In_{0.53}Ga_{0.47}As$ MOSCAPs at 300 K that was forming gas annealed after MOSCAP fabrication. The conductance data of this MOSCAP are shown in Fig. 4. (b) Comparison of the experimental 1 MHz *CV* (symbols) measured at 300 K with a calculated ideal high frequency *CV* (solid line). The oxide capacitance, C_{ox}, is also shown. (c) Experimental band bending ψ_s vs gate voltage V_g as determined by the Terman method.

a progressively freezing trap response with decreasing temperature that was noted in the conductance measurements (Fig. 3) is thus also evident in the *CV*. In addition, the *CV* is less stretched out in depletion and the frequency dispersion is reduced. In contrast to the *p*-type MOSCAP, the horizontal shift in the *CV* with temperature is negligible for the *n*-type MOSCAP and indicates that the D_{it} is smaller near the conduction band edge than toward the valence band edge. Many published *CV* curves of *n*-type high-$k/In_{0.53}Ga_{0.47}As$ MOSCAPs look qualitatively similar to the ones shown here. The upturn in capacitance in the depletion region with decreasing frequency has sometimes been interpreted as an indication of the onset of inversion. However, as will be discussed in Sec. III, the response is due to a high midgap D_{it}, rather than due to true or weak inversion.

Figure 10 shows a comparison of the measured 1 MHz (300 K) *CV* curve with the ideal high frequency *CV* curve and the extracted band bending, as determined using the Terman method. The theoretical *CV* curve was calculated from Eqs. (6), (15), and (16) and accounts for the finite conduction band DOS, the nonparabolicity of the Γ-band and the occupation of higher lying valleys in the conduction band, as described in Sec. II B 2. The oxide capacitance density, C_{ox}, is also shown, which is higher than the capacitance in accumulation because of the finite DOS in the conduction band. A gate voltage change from −1 to −4 V moves the Fermi level by less than 0.1 eV. The Fermi level is effectively pinned and the minimum capacitance is not reached.

For comparison, Fig. 11(a) shows the *CV* characteristics of a forming gas annealed n-$In_{0.53}Ga_{0.47}As$ MOSCAP with a thin (9 nm) HfO_2 film measured at room temperature (the conductance data for this MOSCAP is shown in Fig. 4). Compared to the *CV* of the nitrogen-annealed MOSCAP shown in Fig. 9, the frequency dispersion in depletion and

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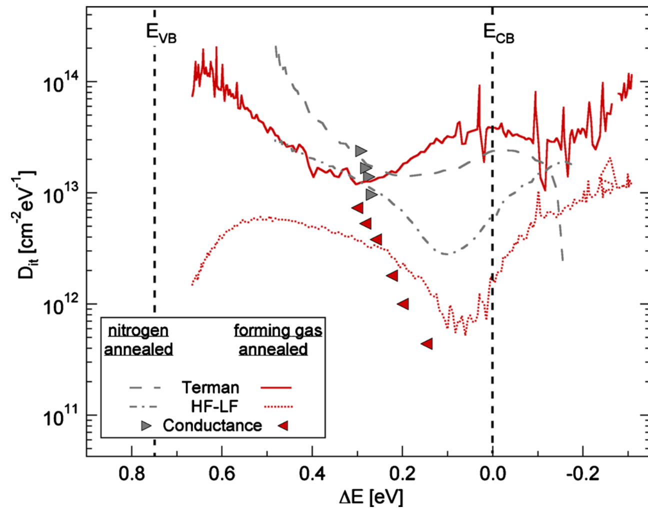

FIG. 12. (Color online) Comparison of $HfO_2/In_{0.53}Ga_{0.47}As$ interface trap distributions determined using the Terman method from the *n*-type MOSCAPs with nitrogen annealed, 30 nm HfO_2 (also see Figs. 3, 9, and 10) and forming gas annealed 9 nm HfO_2 (also see Figs. 4 and 11). Also shown are for comparison the results from room temperature conductance measurements and from the Castagné–Vapaille (high-low frequency) method.

the *CV* stretch-out are smaller, the rise in the capacitance at negative bias with decreasing frequency is largely suppressed, and the depletion capacitance is close to its theoretical value (0.119 $\mu F/cm^2$ for a semiconductor doping of 10^{17} cm^{-3}). The fact that the forming gas annealed stack reaches the ideal depletion capacitance indicates efficient band bending. Figures 11(b) and 11(c) show a comparison of the modeled and 1 MHz experimental *CV* and the extracted band bending, respectively, for the forming gas annealed MOSCAP. The band bending exceeds half the band gap of $In_{0.53}Ga_{0.47}As$ at the maximum applied negative voltage, indicating an unpinned Fermi level that is not impeded by the midgap D_{it} (note that the conductance method, discussed in Sec. II A 2, indicated a reduced midgap D_{it} for this MOSCAP).

Figure 12 shows the D_{it} distribution for the two $HfO_2/n\text{-}In_{0.53}Ga_{0.47}As$ MOSCAPs (nitrogen and forming gas annealed, respectively) extracted from the 1 MHz *CV* curve measured at 300 K using the Terman method. The energy distribution of the trap levels is assigned from the calculations. The flat band capacitance, $C_{fb}=3.17\times10^{-7}$ F/cm^2, corresponds to $\Delta E=25$ meV, the Fermi level position in bulk ($N_D=1\times10^{17}$ cm^{-3}). In addition, D_{it} values calculated from the Castagne–Vapaille method are also shown which were extracted using 1 MHz curve and the 100 Hz and 1 kHz curve for the nitrogen and forming gas annealed stacks, respectively. Furthermore, the results from the room temperature conductance method are also shown. A larger band bending is obtained from the Terman method compared to the conductance method, which can be due to two possible reasons. First, the capture cross section σ used in the conductance method may be too small. However, this would not be consistent with interface trap response times determined recently from small signal response analysis of $LaAlO_3/In_{0.53}Ga_{0.47}As$ MOSFETs corresponded of $\sigma\sim1\times10^{-18}$ cm^2,[43] i.e., even smaller than the value used here. Another reason might be an overestimation of band bending by the Terman method due to relatively slow charge trapping/detrapping in the dielectric, which are not taken accounted for in the analysis.

The D_{it} obtained from the Terman method for the nitrogen annealed stack is larger than what is obtained from the conductance method. This discrepancy is largely attributed to the inaccuracy of the conductance method for stacks with high D_{it}, as discussed above. The minimum D_{it} from the Terman method is 2×10^{13} cm^{-2} eV^{-1}. The D_{it} distribution shows a peak near midgap, where the D_{it} exceeds 10^{14} cm^{-2} eV^{-1}. For the forming gas annealed stack, with a C_{ox} of 2.2 $\mu F/cm^2$, the midgap D_{it} values obtained from conductance should provide reliable values, because for this stack $C_{ox}>qD_{it}$. However, the minimum D_{it} of 1.14×10^{13} eV^{-1} cm^{-2} for the forming gas annealed stack extracted by the Terman method is still higher than the highest D_{it} from the conductance method. The D_{it} determined by the conductance method only probes fast interface traps with short response times, whereas the Terman method is also sensitive to slow traps that contribute to the stretch-out and can be located at the interface or even in the dielectric. The apparent upturn in D_{it} near the valence band is an artifact of the Terman method: as the slope of the *CV* curve decreases in depletion, uncertainties in D_{it} extraction are too large to yield reliable results.

4. Issues and limitations of CV-based methods

a. Berglund integral. Because there is considerable band bending when the Fermi level resides inside the conduction band the Berglund integral [Eq. (9)] to determine band bending becomes intractable. The band bending in accumulation contributes to the total band bending determined from the Berglund method and has to be subtracted if the Fermi level movement **inside** the band gap is to be reported. Calculations, such as discussed in Sec. II B 2, are required to relate gate voltage to band bending in accumulation. It is concluded here that the Berglund method is not suited for high-*k*/III-V interfaces, in particular those with a small EOT.

b. High-low frequency (Castagné–Vapaille) method. Figure 12 also shows the D_{it} values obtained from the Castagné–Vapaille method, which has also been used in the literature.[14] The D_{it} values were smaller than those obtained using the Terman method. The likely reason for the underestimate is that neither the 100 Hz or the 1 MHz *CV* are true low and high frequency curves, respectively. As traps close to the band edge respond first, the ac contribution of interface traps reduces the apparent stretch-out of the measured curve and the D_{it} will be underestimated due to the increase in slope of the measured *CV* curve.

c. Terman method. Potential sources of error in the D_{it} extraction using the Terman method are the two input parameters needed to calculate the ideal *CV* curve, namely the dopant concentration and the oxide capacitance. The effect of any errors in N_D and C_{ox} on the extracted D_{it} are shown in Fig. 13. A *CV* curve with $N_D=1.5\times10^{17}$ cm^{-3} and a uniform $D_{it}=5\times10^{12}$ cm^{-2} eV^{-1} is calculated and taken here to represent a measured curve. Figures 13(a) and 13(b) show the extracted D_{it} and band bending using a correct C_{ox} but dif-

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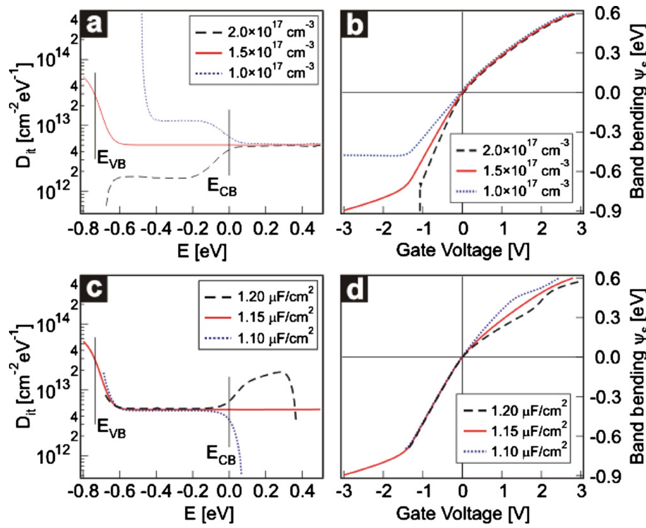

FIG. 13. (Color online) Errors in the (a) extracted D_{it} and (b) band bending ψ_s determined from the Terman method caused by using a semiconductor dopant concentration that deviates from the actual value in the calculation of the ideal *CV* curve. Errors in the (c) extracted D_{it} and (d) band bending ψ_s determined from the Terman method caused by using a oxide capacitance that deviates from the actual value in the calculation of the ideal *CV* curve.

ferent, incorrect dopant concentrations. For the correct dopant concentration the correct D_{it} is obtained, even at large negative band bending, where the slope of the *CV* curve is small. In inversion, where the slope of the high-frequency *CV* curve is zero, the Terman method is not applicable anymore because the inverse stretch-out $(d\psi_s/dV_g)^{-1}$ diverges and along with it the apparent D_{it}. If an erroneously too low value is taken for the dopant concentration, the extracted D_{it} is too high and the extracted band bending suggests Fermi level pinning. Conversely, if an erroneously too high value is taken for the dopant concentration,[16] then the D_{it} is underestimated because the calculated ideal *CV* curve is more stretched out. For a dopant concentration that is 30% lower than its actual value, D_{it} will be underestimated by a factor of three. Figures 13(c) and 13(d) show the extracted D_{it} and band bending for different (correct and incorrect) C_{ox}. The effect on D_{it} is very small. In accumulation the deviations are larger, because C_{dos} is larger than C_{ox}. Too large C_{ox} values overestimate D_{it} inside the conduction band and underestimate band bending.

III. IMPLICATIONS FOR TYPICAL CHARACTERISTICS OF HIGH-*k*/InGaAs MOSCAPs

In addition to providing estimates of D_{it} and band bending, the methods discussed above can explain the origin of certain *CV* characteristics that are widely observed for high-k/$In_{0.53}Ga_{0.47}As$ interfaces at room temperature (and high-*k*/GaAs interfaces at elevated temperatures). These characteristics are often independent of the particular high-*k* but can change with post-deposition processing (see examples in Sec. II). In particular, at negative biases and room temperature *n*-MOSCAPs with $In_{0.53}Ga_{0.47}As$ often show: (i) either a constant but higher than ideal (as calculated from the doping concentration) minimum capacitance measured at 1 MHz or a decreasing slope even at the maximum applied negative gate bias and (ii) an increase in capacitance with decreasing frequencies at negative bias (see Fig. 9). There are two possible explanations for these features. The first, suggested frequently in the literature,[10,11,13,16,44] explains the upturn of capacitance at negative bias with minority carrier (true or weak inversion) response. Minority carriers are expected at higher frequencies for $In_{0.53}Ga_{0.47}As$ than Si, due to the faster generation-recombination rates. The observed increase in parallel conductance at negative biases (for *n*-MOSCAPs) would then be due to generation-recombination loss through bulk traps and the conductance peak should not move with gate bias, as is frequently observed. This would not explain why the minimum capacitance is higher than what is calculated from the doping concentration but this could possibly be explained with a dopant concentration that differs from the nominal concentration (though it is unlikely that this would be the case for *all* MOSCAPs). The second possible explanation is that Fermi level is effectively pinned around midgap due to a high D_{it}. In this case, the semiconductor is never fully depleted even at the largest negative gate bias, and the ideal minimum capacitance is only approached but not reached. A finite slope of the 1 MHz curve (as seen, for example, for ZrO_2 dielectrics[22,23]) is found if the band bending still weakly responds to changes in the gate voltage, i.e., the Fermi level is not completely pinned. The upturn of capacitance at negative gate bias is then due to a strongly frequency and temperature dependent midgap interface trap response, causing an associated increase in parallel conductance.[18,28,30,34] The conductance peak due to interface traps moves only if the Fermi level is not pinned at midgap.

The admittance response of these two scenarios is very similar.[28] The activation energy for minority carrier generation is $E_g/2$ or E_g, depending on whether it is dominated by generation-recombination in the depletion region or drift-diffusion from the back contact, respectively. At lower temperatures the generation-recombination mechanism governs the inversion response due to the smaller activation energy. Because the interface trap response of traps located around midgap will also have an activation energy of $\Delta E = E_g/2$ [see Eq. (1)] the admittance response is similar to the one of minority carriers generated via generation-recombination. For interfaces with Si, minority carrier response is only observed at 10 Hz or lower. However, the minority carrier response time τ_R of $In_{0.53}Ga_{0.47}As$ is about four orders of magnitude shorter, because $\tau_R \propto \tau_T/n_i$, where the intrinsic carrier concentration n_i is two orders of magnitude larger and smaller minority carrier life time τ_T than in Si. Inversion may thus be observed already at kHz frequencies for interfaces with $In_{0.53}Ga_{0.47}As$. Despite this, the methods discussed in Sec. II clearly show that minority (inversion) response is *not* the origin of the characteristics described above; rather, that the *CV* characteristics point to a strong midgap D_{it} response as the origin. Specifically:

- To explain typical discrepancies between the measured and ideal minimum (depletion) capacitance (such as shown in Fig. 10) with errors in the dopant concentra-

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tion, a concentration that is 50% greater than the nominal concentration would be required. Such errors are much higher than typical uncertainties in doping of III-V semiconductors, typically no greater than 10%.

- If minority carrier generation is the origin for the upturn in capacitance with decreasing frequency of *n*-MOSCAPs at negative biases, then the measured capacitance should be independent of gate bias for all frequencies. Instead, typical *CV* curves show a "hump" at negative biases and low frequencies, which is characteristic for interface trap response.[30]
- The band bending of *n*-MOSCAPs that show the very strong frequency dispersion at negative gate biases is not sufficient to cause inversion (see Fig. 10). Inversion occurs when the Fermi level at the interface resides sufficiently close to the valence band edge. For example, for $In_{0.53}Ga_{0.47}As$ with a typical donor concentration of $N_D=1\times10^{17}$ cm^{-3} a total band bending of -0.6 eV is needed at room temperature to cause inversion (see Fig. 7). As can be seen from the example shown in Fig. 10, the band bending is typically much smaller, in particular for the stacks that show the strong frequency dispersion in depletion.
- Forming gas annealed *n*-MOSCAPs, such as shown in Fig. 11 and in the literature[12] show a much reduced frequency dispersion at negative biases. In these stacks, the conductance peak maximum shifts in frequency with gate voltage at negative bias, indicating an efficient Fermi level movement in the kHz frequency regime (Fig. 4). The frequency response of the conductance peak with gate bias unambiguously excludes bulk trap loss as the origin of the conductance peak.

In summary, a pronounced midgap D_{it} response can explain all details of the admittance measurements at room temperature, whereas the behavior is not consistent with inversion. A large D_{it} located near midgap can effectively pin the Fermi level and cause an increase in capacitance upturn at negative bias with decrease in frequency and a parallel conductance peak, which does not shift in frequency with gate bias. The semiconductor is not fully depleted and the minimum capacitance is not reached. A finite slope of the 1 MHz curve is found in cases where the band bending still weakly responds to gate voltage changes.

There are still several remaining open questions regarding the *CV* characteristics of MOSCAPs with $In_{0.53}Ga_{0.47}As$. One concerns the forming gas annealed stacks that show sufficient band bending to, in principle, achieve inversion (see Fig. 11) but do not show an inversion response even at kilohertz frequencies. This may indicate that the rough estimate of the minority carrier response time for $In_{0.53}Ga_{0.47}As$ is not correct and lower measurement frequencies may be needed. A second question concerns the strong frequency dispersion seen in accumulation of *n*-MOSCAPs, the origin of which is still under debate.[12,43]

IV. GUIDELINES TO OBTAIN RELIABLE ESTIMATES OF D_{IT} AND FERMI LEVEL RESPONSE FROM MOSCAP STUDIES

The quantification of D_{it} at high-*k*/III-V interfaces is not as straight-forward as for interfaces with Si. For $In_{0.53}Ga_{0.47}As$ in particular, a small conduction band DOS, the small band gap and a relatively high D_{it} at midgap make the interpretation of analysis methods that have worked well for Si more difficult. Features in the *CV* can easily be misinterpreted. Here we summarize potential pitfalls that can result in claims of too low D_{it}, too large band bending and Fermi level unpinning at high-$k/In_{0.53}Ga_{0.47}As$ interfaces:

- Demonstrating flat band voltage shifts in *CV* as a function of metal gate work function is not sufficient to establish an unpinned Fermi level. For *n*-type substrates with a dopant concentration in the range of 10^{16}–mid-10^{17} cm^{-3} and typical metal work functions the Fermi level is in the conduction band or upper half of the band gap range at zero gate bias, where the *CV* is either insensitive to D_{it} or where the D_{it} is low, respectively. Flat band voltage shifts with gate metal work function are observed for III-V MOSCAPs that show a large midgap D_{it} response.[11,22,23]
- The Berglund integral greatly overestimates semiconductor band bending because the Fermi level can move deep into the conduction band due to the small conduction band DOS. It impossible to anchor the band bending gate voltage relationship without calculations of the ideal *CV*.
- Using low temperature conductance data to probe D_{it} close to the band edges results in underestimates of the D_{it} due to trap response freeze-out.
- The room temperature conductance method does not give reliable values for the midgap D_{it} for MOSCAPs with a large D_{it}, for which $C_{ox} < qD_{it}$.[28,29] The estimated D_{it} for such MOSCAPs may be orders of magnitude too small.
- *CV* curves *cannot* be calculated classically. The error that is introduced by using the classical (Boltzmann) approximation increases for highly scaled dielectrics.[20] Fermi level (un)pinning cannot be established and band bending is overestimated. The parabolic band approximation of the conduction band gives an apparently high acceptor D_{it} in the conduction band because it underestimates the change in semiconductor charge with band bending, which is then attributed to an interface trap density.

In the following we propose a set of guidelines to report reliable D_{it} values that can provide evidence for efficient Fermi level movement across the band gap for high-$k/In_{0.53}Ga_{0.47}As$ interfaces:

- The dopant concentration and oxide capacitance should be determined independently, as they are needed in conductance and capacitance based methods. The dopant concentration should *not* be determined from the minimum capacitance[20] or slope of the 1 MHz curve.[16]

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- To establish that the Fermi level is *not* effectively pinned at midgap, it should be shown that the high-frequency *CV* curve reaches the ideal depletion capacitance determined by the doping level.
- The room temperature parallel conductance should show a frequency-dependent shift in the conductance peak maximum with gate voltage. If the conductance peak maximum shifts to frequencies that are less than 2 kHz for *n*-MOSCAPs it is indicative that the Fermi level can be moved into the lower part of the band gap.
- The room temperature conductance method gives reasonable estimates of the *fast* D_{it} around midgap, if $C_{ox} > qD_{it}$.
- The ideal *CV* curve must be calculated taking into account the low conduction band DOS and the nonparabolicity of the Γ valley. The Terman method gives both slow and fast traps and provides reliable values of midgap D_{it}. If the contribution from slow traps is small and extracted D_{it} values should agree quantitatively with results from the conductance method (if $C_{ox} > qD_{it}$). The fact that the *CV* is not a true high-frequency curve affects mostly the D_{it} near the band edges.
- Measured low frequency *CV* curves should reflect the asymmetry of the conduction and valence band DOS, especially for highly scaled oxide capacitances and compound semiconductors with higher indium content. Large interface trap densities close to the conduction band edge can obscure the asymmetry.
- If true inversion is claimed it should be shown that the experimentally achieved bend bending is sufficient to achieve inversion. Measurements of the inversion conductance as a function of temperature should be used to show that minority carrier generation transitions from generation/recombination in the depletion layer to drift-diffusion with an activation energy that corresponds to the band gap (i.e., not half the band gap).

Further reduction in D_{it} at high-*k*/III-V interface is critical for the improvement of the transconductance and subthreshold slopes of surface channel III-V MOSFETs. The authors hope that the guidelines developed above aid in developing high-quality high-k/$In_{0.53}Ga_{0.47}As$ interfaces.

ACKNOWLEDGMENTS

The authors thank Jeff Huang of SEMATECH helping with some of the measurements. R.E.-H. also thanks Oliver Bierwagen for valuable discussions. The authors thank funding from the Semiconductor Research Corporation through the Nonclassical CMOS Research Center (Task ID 1437.005). R.E.-H. acknowledges support from the Alexander-von-Humboldt Foundation through a Feodor–Lynen fellowship. This work made use of the UCSB Nanofabrication Facility, a part of the NSF-funded NNIN network.

APPENDIX: SAMPLE DETAILS

HfO_2 films were grown on lattice matched *n*-(Si: 1×10^{17} cm^{-3}) or *p*-doped (Be: 1×10^{17} cm^{-3}) $In_{0.53}Ga_{0.47}As$ films on n^+ and p^+ (001) InP wafers using methods that have been described in detail elsewhere.[21,22,59] The $In_{0.53}Ga_{0.47}As$ doping concentration was within 10% of the targeted value. The dielectric constant was determined independently form a thickness series. The "nitrogen-annealed" samples were annealed immediately after deposition for 30 min at 300 °C in nitrogen and then MOSCAPs were fabricated using Pt electrodes. MOSCAPs of the forming-gas annealed samples were fabricated before annealing. The anneal was performed in forming gas (95% of N_2 and 5% of H_2) for 50 min at 400 °C, as described elsewhere.[59]

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