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Publication Date
1969-04-01

Submitted to Nuclear Instruments and
Methods

UCRL-18850
Preprint
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April 1969

AEC Contract No. W-7405-eng-48

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AN INEXPENSIVE GAIN STABILIZER CONTROLLED BY A TIME-SHARED COMPUTER*

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ABSTRACT

An electronic pulse amplifier is described for automatic gain correction in high-resolution high-rate pulse-height analysis systems. The circuit gain is controlled by a PDP-7 computer devoting less than 4 ms per second of its time to provide gain correction signals for up to 8 amplifiers.

Necessary control voltages are developed in the computer's CRT display circuits and transferred to a "sample and hold" circuit associated with each gain stabilizer. Gain control is accomplished by adjusting the gate voltage of an FET which shunts a small fraction of the total signal.

In pulse-height analysis systems using a computer, the computer can replace the digital electronics, particularly since gain shifts that require correction occur quite slowly. The computer is used to trim the gain periodically so as to maintain a calibration peak at a constant position.

The computer-controlled gain adjustment could be done by driving a potentiometer, but small hunting motions would lead to serious wear and a short life for the potentiometer. A better scheme would be to store a digital code in a flip-flop register and convert the digital output to an analog voltage that controls the gain of a variable-gain amplifier.

A much less expensive alternative,which is the subject of this paper, is available with many computer systems that have CRT displays. Such a display requires a high-quality digital-to-analog converter which can also be used to provide the precisely adjustable voltage level to control one or more gain stabilizers. However, the CRT display must remain available for its normal uses at the same time.

A scheme that has been used successfully to time-share the computer and CRT display circuitry for gain stabilization is illustrated in fig. 1. Every second or so, a digital number corresponding to the desired gain setting is loaded into the digital register whose output controls the CRT vertical deflection. The resultant voltage signal to the CRT deflection amplifier is fed in parallel to an analog "sample and hold" storage unit* (see fig. 2). A computer-generated

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* The storage unit used is a stripped-down version of one developed for use as the stretcher in an ADC for pulse height analysis3).

pulse then gates the voltage into the analog store, and the computer and CRT are free for other operations. A gain correction of 1% or 2% normally represents the full control range, and the analog store drifts by less than 0.01% of its full scale per second, representing an error in gain due to drift in the analog store of less than 0.0002% if the store is refreshed once per second. Thus the analog store need only be refreshed every few seconds.

It should be noted that a number of stretchers can readily be controlled from one CRT, allowing several amplifier gains or other analog functions to be controlled. For example, we have used a second stretcher to control the threshold voltage of a biased amplifier so that both threshold and gain drift can be corrected, using two stretchers and one variable gain amplifier.

The requirement that the computer refresh the stretcher setting as often as once per second presents no difficulty in an on-line data system in which data are being continuously stored in the computer. If, for example, the computer is halted, the gain might drift, but no data would normally be taken during this interval. When the computer is restarted, the gain is instantly restored to the position held when the halt occurred, and gain correction for any intervening changes is carried out rapidly.

The machine-language computer program to control as many as eight independent stabilizers is relatively simple, requiring less than 130 words in a PDP-7 computer. This program is started once per second by a real-time clock in the computer and requires less than 0.5 ms of computer time for each gain stabilizer in operation.

III. CONTROLLED GAIN AMPLIFIER

The controlled gain amplifier is shown schematically in fig. 3. The FET (Q3) operating with close to zero volts between source and drain behaves as a nearly linear resistor of about 2000 ohms when the gate voltage is held at about -2 V with respect to ground.

Since the FET acts as a linear resistor only for small signals, the controlled-gain unit is placed between preamplifier and main amplifier, where signal amplitude is much less than 1 V. About 3% of this signal is allowed to appear across the FET so the small-signal condition across the FET is satisfied. The small fraction of the signal appearing across the FET determines the gain control range, which is about 1% with the component values of fig. 3. Since the drift observed in a well-designed pulse-height analysis system, under practical experimental conditions, is generally less than 0.1%, the 1% range of gain correction represents a reasonable choice; a wider range of control could lead to significant nonlinearity of gain with pulse height, because of the nonlinearity of the FET for large signals.

IV. HIGH-RATE EFFECTS

At high rates, the average preamplifier output voltage level may undergo significant fluctuations due to pile-up of the pulses which have a long "tail" at this point in the system. Preamplifiers and amplifiers are usually designed to give constant gain in spite of these fluctuations. Therefore, the gain of the controlled-gain unit must also be made insensitive to the fluctuations.

To accomplish this result we have differentiated the signal which appears in the FET gain controlled section of the unit on a 30 μs time constant. Since the pile-up effects are negligible at normal rates with this differentiation, the average voltage level across the FET is sensibly constant, and rate effects on the gain are negligible.

The presence of a 30-μs differentiation alone would degrade the overall system response at high counting rates. This results in the need for an extra pole-zero cancellation network. To accomplish this an integrator network is needed; the parallel 30-μs integrator seen in fig. 3 is for this purpose. Compensation is not precise, due to the gain changes in the ac path produced by the FET, but it is adequate for practical purposes.

Even assuming perfectly stable circuitry, some broadening of peak width must result from use of a gain stabilizer, because the gain will be adjusted unnecessarily as successive pulses fall randomly in either the upper or lower half of the reference peak. This effect can be made small by making the increments of gain small. Ladd and Kennedy2) find that the peak broadening will be of the same order as the smallest increment of gain that can be applied by the gain controller. The computer can further reduce the broadening effect by changing the gain only when a statistically significant difference in count rate is detected. Our computer program merely ignores the least significant bit of the count rate. At present, no experimentally significant improvement could be obtained by more complex procedures.

V. PERFORMANCE

The insertion of the controlled gain amplifier in a high-performance pulse-height analysis system[4)] produced line broadening of less than 0.1 channel at count rates up to 15000/sec, and caused no measurable system nonlinearity.

Drift in peak position over a period of several hours was as much as 5 channels in 4000 before insertion of the gain control, but too small to be detected while the gain control was operating.

FOOTNOTE AND REFERENCES

* This work was carried out as part of the research program of the Nuclear Chemistry Division of the Lawrence Radiation Laboratory, University of California, which is supported by U.S. Atomic Energy Commission Contract W-7405-eng-48.

1. H. DeWaard, Stabilizing Scintillation Spectrometers with Counting Rate Difference Feedback, Nucleonics 13 [7] (1955) 36.
2. J. A. Ladd and J. M. Kennedy, A Digital Spectrum Stabilizer for Pulse Analyzing Systems, AECL Report No. 1417, Dec. 1961.
3. L. B. Robinson, F. Gin and F. S. Goulding, A High-Speed 4096-Channel Analog-Digital-Converter for Pulse Height Analysis, Nucl. Instr. and Meth. 62 (1968) 237.
4. F. S. Goulding, D. A. Landis and R. H. Pehl, The Design and Performance of a High-Resolution High-Rate Amplifier System for Nuclear Spectroscopy, UCRL-17560, May 1967.

FIGURE CAPTIONS

Fig. 1. Computer-controlled gain-stabilizing system. The computer program detects gain changes by testing a peak in the spectrum, and the gain of the controlled Gain Amp is adjusted by the computer to compensate for any change.

Fig. 2. Sample and Hold Circuit used for gain stabilizer system. The one-shot circuit Q18, Q19, Q20 opens the input gate Q2 ... Q3 for 10 μs to charge C3. The output level drifts by only about 1 mV per second after the gate is closed.

Fig. 3. Variable-Gain Inverting Pulse Amplifier. The FET Q3 acts as a resistive shunt; changes in control voltage change its effective resistance in a range centering on 2 KΩ.

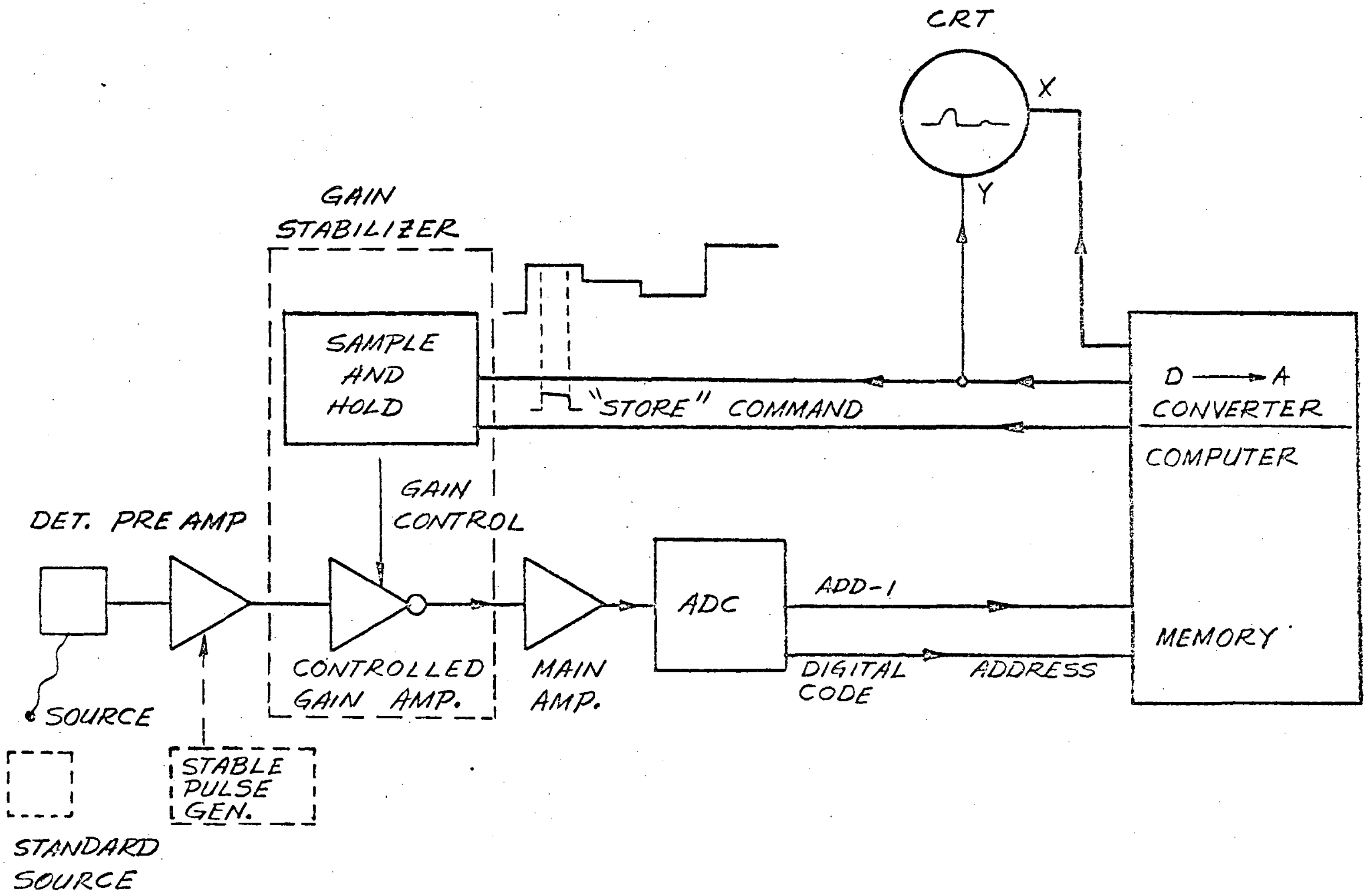

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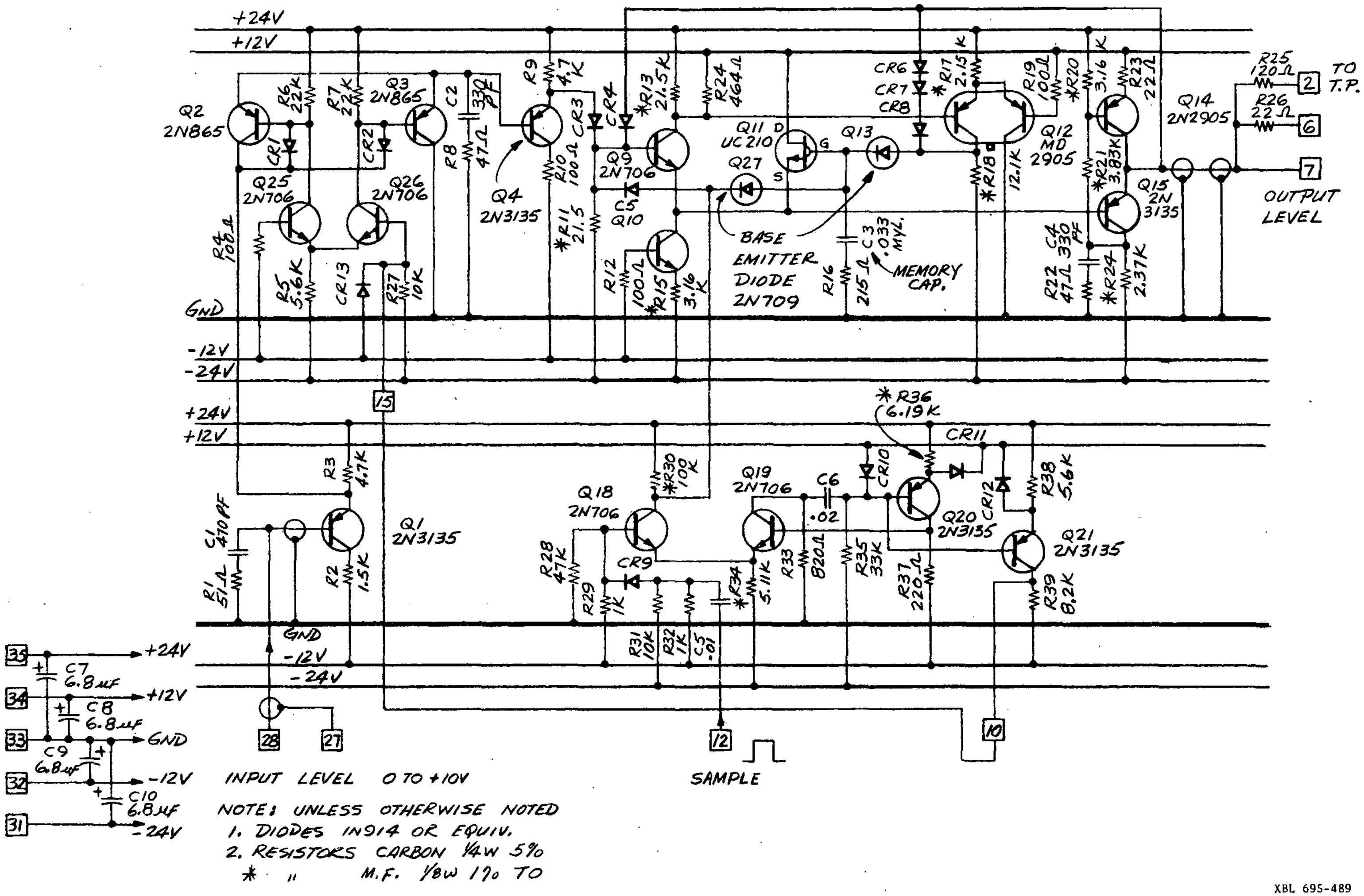
Fig. 1. Computer-Controlled Gain-Stabilizing System.



INPUT LEVEL 0 TO +10V

NOTE: UNLESS OTHERWISE NOTED
1. DIODES IN914 OR EQUIV.
2. RESISTORS CARBON 1/4W 5%
* " M.F. 1/8W 1% TO

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Fig. 2. Sample-And-Hold Circuit

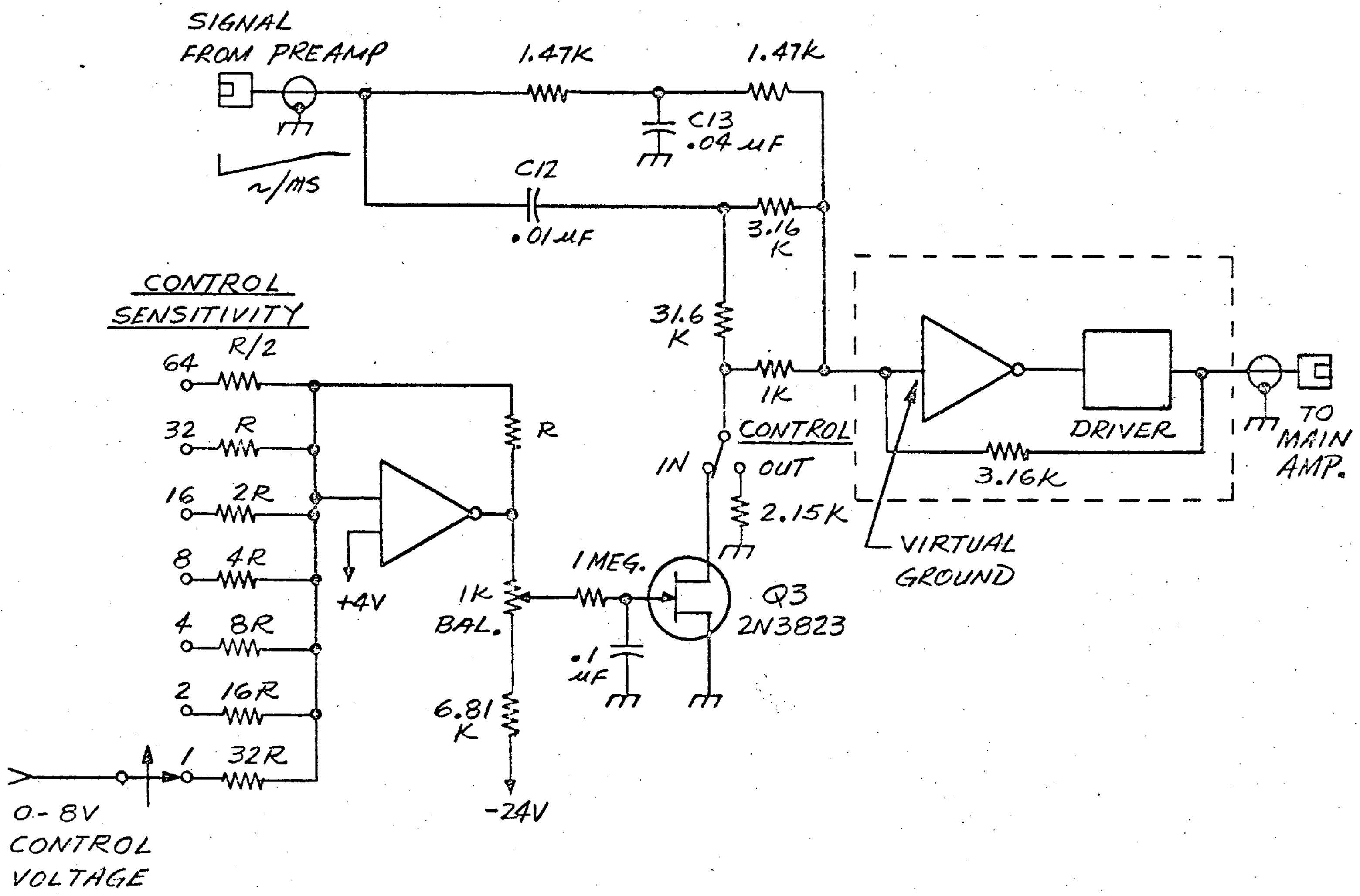

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Fig. 3. Variable-Gain Inverting Pulse-Amplifier.

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