University of California
Santa Barbara

Blocker and Multipath Tolerant, Full-Duplex Receivers using RF Code-Domain Signal Processing

A dissertation submitted in partial satisfaction
of the requirements for the degree

Doctor of Philosophy
in
Electrical and Computer Engineering

by

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December 2020

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Acknowledgements

I would like to thank God for His unlimited blessings on me.

I would like also to express my gratitude to Professor James Buckwalter for supervising my Ph.D. Thesis. It was a great honor for me to work under his supervision. Without his great help and concern, I would not have been able to accomplish a lot of things during the Ph.D. period.

I would also like to thank the Ph.D. committee members: Professor Mark Rodwell, Professor Upamanyu Madhow, and Professor Clint Schow. The discussions with committee members during both the screening and qualifying exams broadened my perspective on many research topics. I am also especially grateful to Professor Rodwell for the multiple recommendation letters he agreed to write for me.

I would like to acknowledge all my colleagues at the RF and mixed-signal integrated systems laboratory at UCSB. They made my Ph.D. at UCSB enjoyable and full of fun, besides the great technical discussions I had with them. Thanks to Navid Hosseinzadeh, Kang Ning, Mayank Singh, Luis Valenzuela, Everett O'Malley, Ghazal Movaghar, Rohit Karnaty, Jeff Chien, Andrea Arias, Jonathan Tao, Shu-Ming Chang, and Eythan Lam. In particular, I would like to mention the contributions of Hussam AlShammary and Cameron Hill who worked with me for more than 4 years on the same research project.

The Egyptian graduate students at the ECE department at UCSB were extremely helpful and supportive. Thanks to Ahmed Samir, Ali Farid, Belal Salama, Mohamed El-Motaz, Ahmed ElShafiy, Mohamed Wahba, and Islam Hashem. I had a lot of fun moments and memories with them. Also, I would like to thank Ghassan Aburqayeq and Wael Taha.

Finally, I would like to thank my parents and family for their unlimited support that can not be described by any words.

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Publications

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J.1 **A. Hamza**, H. AlShammary, C. Hill, and J. Buckwalter, "A Full-Duplex Rake Receiver Using RF Code-Domain Signal Processing for Multipath Environments," submitted to *IEEE Journal of Solid-State Circuits (JSSC)*.

J.2 **A. Hamza**, A. Nagulu, A. Davidson, J. Tao, C. Hill, H. AlShammary, H. Krishaswamy, and J. Buckwalter, "A Code-Domain, In-Band, Full-Duplex Wireless Communication Link with Greater than 100 dB Rejection," accepted to *IEEE Transaction on Microwave Theory and Techniques (TMTT)*.

J.3 **A. Hamza**, C. Hill, H. AlShammary, and J. Buckwalter, "A Multi-band, High-Order Notch Filter for TX Leakage Suppression in FDD Receivers," accepted to *IEEE Solid-State Circuits Letters (SSC-L)*.

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Abstract

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by

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Full-Duplex (FD) communications allow the concurrent operation of the transmitter (TX) and receiver (RX) of a radio frequency (RF) transceiver at the same frequency channel offering multiple advantages for wireless communications such as increased bandwidth efficiency. However, the RX of an FD node should tolerate high TX self-interference (TX SI) power levels ($\sim$ 30 dBm) while detecting small desired RX signals ($\sim$ -100 dBm). The required dynamic range (DR) is addressed through a variety of TX SI rejection techniques in the RF, analog, and digital domains.

This thesis presents an RF code-domain signal processing technique that increases the achieved rejection for FD radios. FD DR is enhanced by assigning orthogonal PN codes to the TX and RX signals of an FD transceiver and performing code correlation in the RF domain through code selective filters. RF code-domain signal processing increases the achieved TX-SI rejection by >50 dB along with enhancing the RX linearity by >20 dB while providing 9 dB SNR improvement in multipath environments.

The thesis reports various CMOS chip implementations of the proposed RF code-domain signal processing approach including code pass and code notch filters, a reconfigurable multi-band/high-order notch filter, a high-rejection code-domain receiver, and a 3-finger multipath tolerant rake RX. Moreover, the thesis presents an FD link demonstration combining the proposed code-domain approach with circulators and digital SI cancellation for a complete node evaluation with >100 dB TX SI rejection.

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Chapter 1

Introduction

1.1 Full-Duplex Wireless

Wireless spectrum is a scarce resource given the tremendous increase in wireless devices and their increasing data rate requirements. Generally, wireless resources are shared between wireless terminals using time division duplexing (TDD) techniques, or frequency division duplexing (FDD) techniques.

As demonstrated in Fig. 1.1, TDD allocates different time slots for the transmitter (TX) and receiver (RX) of a wireless transceiver. The full channel capacity alternates between the TX and RX to avoid desensitizing the RX with the TX signal which is orders of magnitude higher. FDD operates by allocating different frequency channels to

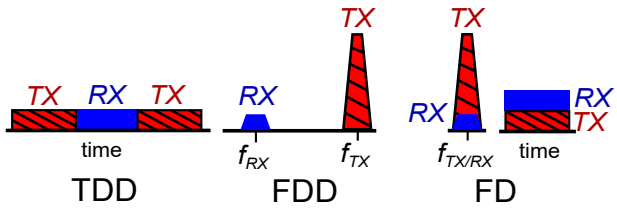


Figure 1.1: Time division duplexing vs frequency division duplexing vs full-duplex.

both the TX and RX and uses duplexers and high-selectivity filters at the RF front-end to overcome the desensitization problem. Full-duplex (FD), also known as simultaneous transmit and receive (STAR), aims to increase the bandwidth (BW) efficiency of wireless systems by allowing the TX and RX concurrent operation in the same wireless channel.

In addition to enhanced BW efficiency (nearly 2x), FD offers other benefits in upper network layers such as the medium access control (MAC) layer [1, 2]. One of the main challenges of FD transceivers is addressing the extreme dynamic range (DR) difference between the TX and RX signals. The TX signal could be in the range of ∼30 dBm while the RX signal could be as small as ∼-100 dBm. Simultaneous operation of the TX and RX in the same channel requires bringing the TX self-interference (TX SI) signal down to the RX sensitivity level.

1.2 Techniques for Self-Interference Rejection in FD Transceivers

Different TX SI cancellation and rejection techniques were previously proposed to handle the required dynamic range difference between the TX and RX signals. These techniques can be categorized into 4 categories namely, antenna domain, radio frequency (RF) domain, analog (or baseband (BB) domain), and digital cancellation. The different FD techniques are summarized in Fig. 1.2 and a comprehensive survey of these techniques can be found in [3, 4].

Antenna-based TX SI rejection techniques achieve rejection through isolation at the antenna interface. Prior work has exhibited using two or more antennas with spatial separation, orthogonally polarized antennas, antenna arrays, or a relay antenna with wave traps [2, 5–12]. One of the main challenges in these techniques is the form factor of

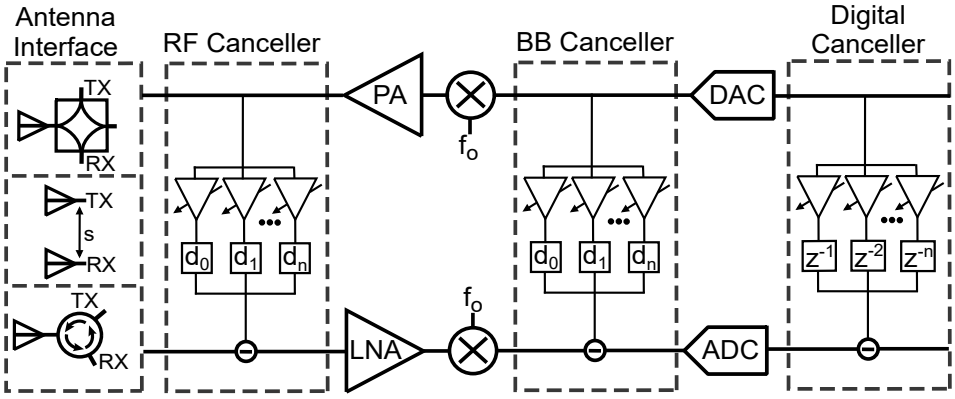


Figure 1.2: Different TX SI rejection techniques in FD transceivers including antenna interface rejection, RF cancellation, baseband cancellation, and digital cancellation. A combination of these techniques can be used to achieve the required rejection.

the FD transceiver. Multiple antennas occupy a large area overhead given the required antenna separation making them unsuitable for mobile devices. Otherwise; magnetic circulators [13–17], electrically balanced duplexers (EBD) [18–21], or compact CMOS circulators [22–26] can be used in a single antenna FD transceiver. An EBD reduces the FD transceiver from factor at the expense of at least 3-dB TX power loss penalty reducing the TX efficiency. The 3-dB TX power loss penalty can be overcome by using a circulator instead of the EBD. Magnetic circulators still occupy a large area overhead making non-magnetic CMOS circulators the most feasible option for compact FD transceivers. However, CMOS circulators have less linearity compared to magnetic ones limiting the achievable TX power level.

RF rejection operates by injecting a replica TX signal to the RX and cancelling it at the low noise amplifier (LNA) [7, 9, 10, 13, 15, 16, 25]. RF cancellers use tunable delays/phase-shifters and tunable gain elements to emulate the SI channel response between the TX and RX in a time or frequency-domain approach. Analog cancellation operates similarly in the BB section after frequency down-conversion by the mixer and is effective when the SI does not generate significant in-band (IB) distortion [27, 28]. Emulating the SI channel between the TX and RX with high accuracy is one of the

main challenges in high-rejection RF/analog cancellers. The SI channel is characterized by having large delay spreads due to multipath and environmental reflections. A high-rejection time-domain canceller requires long delay lines with small delay resolution to achieve a good approximation of the SI channel which is challenging and ultimately results in non-compact designs that are not compatible with CMOS integration. Moreover, the SI channel is dynamic requiring adaptive RF filters for frequency-domain cancellers increasing their design challenges and power/area overhead.

Digital self-interference cancellation (SIC) exploits the computational-scaling available from complementary metal-oxide-silicon (CMOS) and operates by estimating the SI channel using digital signal processing (DSP) techniques to cancel the residual TX SI to the RX noise floor [7, 11–17, 25]. Employing a non-linear channel estimation algorithm in the digital domain cancels the IB distortion along with the fundamental TX SI and requires high DR analog-to-digital converters (ADC) with high sampling rates for effective cancellation.

1.3 FD Link Budget

Handling 27 dBm TX power levels in FD transceivers requires a careful analysis of the link budget of the transceiver and how to assign the required rejection to the different SI cancellation domains. The minimum detectable signal (MDS) in an FD transceiver is either limited by the RX sensitivity (P_{sens}) or the residual TX SI ($P_{TX,SI}$) after cancellation techniques have been applied.

$$MDS = \max\{P_{sens}, P_{TX,SI}\} + SNR, \tag{1.1}$$

Table 1.1: Full-duplex link parameters

P_{TX}	BW	SNR	NF	Link Margin	G_{ant}
27 dBm	10 MHz	15 dB	9 dB	15 dB	2.5 dB

where

$$P_{sens} = -174dBm/Hz + 10\log_{10}(BW) + NF, \tag{1.2}$$

given the signal bandwidth (BW), RX noise figure (NF), and the desired signal-to-noise ratio (SNR). The TX SI is the difference between the TX power (P_{TX}) and the sum of the RF, BB, and digital rejection, i.e.

$$P_{TX,SI} = P_{TX} - \Sigma REJ. \tag{1.3}$$

The system gain (G_{SYS}) is therefore given by

$$G_{SYS} = P_{TX} + 2G_{ant} - (MDS + L_M), \tag{1.4}$$

where G_{ant} is the TX and RX antenna gains and L_M is the link margin for fading, multi-path losses, and other propagation non-idealities. For link parameters with conventional FD approaches shown in Table 1.1 and Fig. 1.3, P_{sens} and $P_{TX,SI}$ are calculated to be -95 dBm and -73 dBm, respectively. Therefore, the FD link is SI limited, and the system gain is restricted to 75 dB, corresponding to a distance of 135 m at 1 GHz as calculated by the Friis equation for free-space propagation.

Although watt-level circulators and EBDs have been reported [18, 19, 24, 26], the TX power of complete FD systems is limited to around 10 dBm output power [23, 25] due to limited SI rejection. At least 20-30 dB of additional rejection is demanded to handle a 27 dBm TX. This extra SI rejection will eventually increase the FD link gain even if it demands an extra 4-5 dB NF penalty.

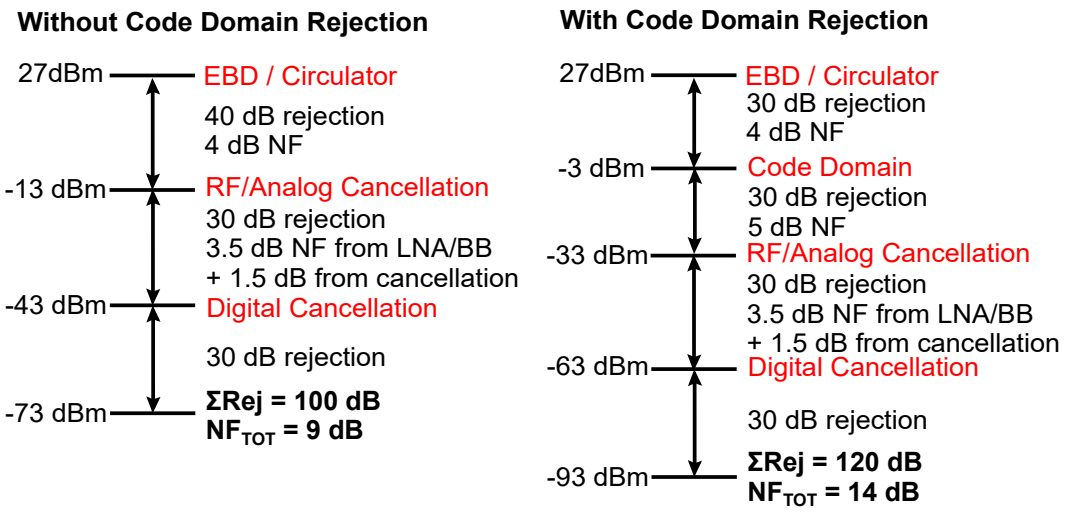


Figure 1.3: Link budget comparison for an FD communication system.

1.4 RF Code-Domain Signal Processing

This thesis presents a code-domain (CD) FD technique that employs the orthogonality between pseudo-noise (PN) codes to reject the TX signal at the RF domain. The proposed code-domain RX for SI rejection is shown in Fig. 1.4. A PN code of length M is applied to the TX signal and spreads the signal BW over $M \cdot BW$. The code length is determined by the number of simultaneous channel users and directly increases the spreading bandwidth for a given BW. The code-domain RX operates by correlating the desired signal against a matching PN code (PN_{RX}) while rejecting the TX signal out of the signal band due to its orthogonal PN code (PN_{TX}).

Code-division multiple access (CDMA) techniques were previously used in the IS-95 and wideband CMDA (WCDMA) standards [29–32] where the signal processing and PN correlation were done using digital signal processing (DSP). Moreover, the TX operates in a different frequency channel with respect to that of the RX in CDMA (similar to FDD) to relax the ADC DR requirements. Performing the PN code correlation and signal processing in the RF domain increases the achieved rejection in the RF domain

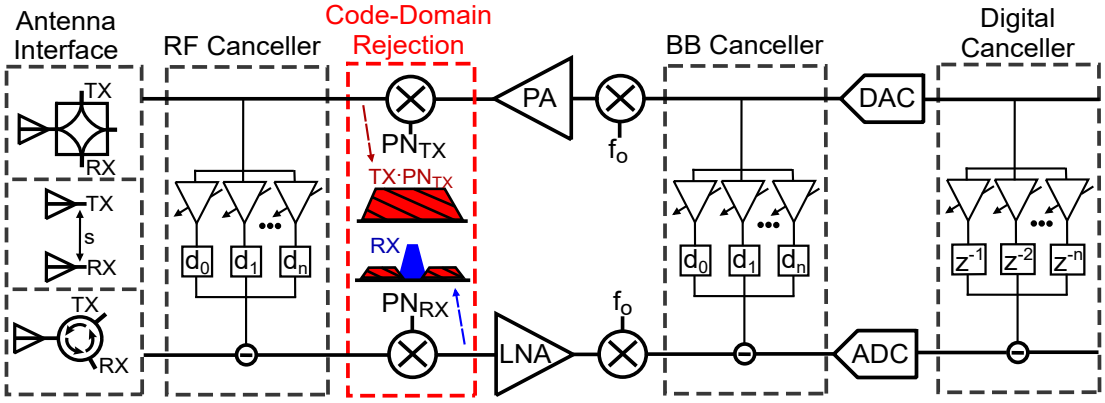


Figure 1.4: Proposed CD FD technique in conjunction with prior TX SI rejection techniques.

allowing FD communications along with relaxing the ADC power requirements. First, the ADC DR is reduced by the extra SI rejection in the RF domain. Second, the ADC only samples the signal BW instead of the spread BW reducing the ADC sampling frequency. Both of these advantages lower the power consumption compared to DSP. Using the same parameters in Fig. 1.3, the DR of the ADC is reduced by 20 dB or 3.32 lower effective number of bits for the same link performance by using RF code-domain rejection. For a data rate of 6.25 Mbps and a chip rate of 100 MChips/sec, the corresponding sampling frequency of the ADC is 6.25 MHz and 100 MHz with and without the RF code-domain rejection respectively. The 20 dB decrease in the ADC DR and 16-fold decrease in sampling frequency result in a 160-fold reduction in the ADC power consumption (this increases to 1280-fold when 128 length codes are used) assuming that the ADCs have the same figure of merit.

Along with removing the additional DR and BW requirements in the ADC by implementing the signal correlation in the RF front-end, RF code-domain signal processing also maintains compatibility with other in-band FD (IBFD) techniques. When combined with other TX SI techniques such as circulators, RF cancellation, and digital SIC, as shown in Fig. 1.3, the total SIC can theoretically exceed 120 dB. If the proposed

code-domain signal processing provides an additional 30 dB of TX SI rejection, P_{sens} and $P_{TX,SI}$ are calculated to be -90 dBm and -93 dBm, respectively, using the link parameters in Table 1.1.[1] As a result, the system is no longer SI-limited since the system gain is 92 dB corresponding to a range of 950 m at 1 GHz.

However, RF CD signal processing entails some challenges for the RF front-end circuitry. The DR, power handling, and linearity of the RX must be improved to tolerate TX SI. Advances in CMOS device technology provide support to high-speed, high-linearity CMOS switches allowing RF CD signal processing with little power and NF overhead. Also, N-path filtering techniques allow high-quality factor (Q) RF filters with high power handling [33, 34]. N-path filters utilize CMOS switches and capacitors to perform RF filtering using the impedance translation property of the $1/N$ duty cycle clock pulses of the N-path filter switches, resulting in linear, low-loss, high-Q RF filtering that is compatible with chip integration. This high-Q RF filtering relaxes the RX power handling by rejecting the residual TX signal which is spread by the RX PN code (PN_{RX}) out of the signal BW.

Moreover, RF CD rejection overcomes some of the challenges of previous SI cancellation techniques as PN codes are resilient to the SI channel multipath propagation effects due to PN code orthogonality for any lag. Also, spreading the RF spectrum with PN codes is advantageous with respect to the required circulator linearity allowing higher TX power levels compared to the prior art.

1.5 Dissertation Organization

The introduction discussed the importance of FD communications and the need for more rejection to achieve reliable, long-range FD links that can handle higher TX power

[1] It is assumed that the circulator/EBD isolation drops by 10 dB due to the wider bandwidth needed with the code-domain approach.

levels. The remainder of the thesis focuses on the proposed CD SI rejection technique and discusses various chip implementations for the proposed technique. While the thesis focuses mainly on the implementation of the RX side of the transceiver, it also gives a brief overview of some of the encountered challenges when implementing the circulator and TX code modulator of the complete FD transceiver.

Chapter 2 discusses the implementation of N-path bandpass and bandstop (notch) filters. The N-path filters are modified to perform code selectivity in addition to frequency selectivity. The chapter also discusses a reconfigurable, multi-band, high-order notch filter architecture that can be reconfigured to different operating modes offering greater programmability allowing its usage in software-defined radios (SDR) and carrier aggregation (CA) applications.

Chapter 3 investigates the design of a CD FD RX. The CD FD RX uses code-pass and code-notch filters at the RF front-end to allow high SI rejection. The front-end CD filters are followed by an LNA with N-path feedback for amplification, filtering, and frequency down-conversion. Finally, harmonic BB recombination circuitry generates the I and Q BB outputs.

Chapter 4 presents the design of a multipath-tolerant, blocker-tolerant rake RX. The rake receiver employs the orthogonality properties of PN codes to offer TX SI rejection and tolerance to multipath propagation effects and frequency selective fading present in practical wireless channels. The rake RX consists of 3 fingers, each synchronized to a delayed version of the RX PN code to capture multipath signal components and enhance SNR by about 9 dB.

Chapter 5 demonstrates the experimentation of a complete FD transceiver node. The FD transceiver uses a non-magnetic CMOS circulator, TX and RX code correlators, and digital SIC to achieve high TX SI rejection. The implemented FD node leverages these different techniques to achieve an overall rejection that is around 104 dB bringing the

TX signal from 20 dBm to the noise floor of the RX at -85 dBm.

Finally, future work and directions are discussed in chapter 6 including the integration of the previously discussed techniques in an integrated CMOS transceiver and the extension of the proposed CD FD technique to millimeter-wave bands where the available BW is much higher compared to RF frequencies allowing high symbol rates and chip rates.

1.6 Permissions and Attributions

Chapter 2

N-path Bandpass and Bandstop Filters and their Application to CD FD Receivers

This chapter presents a series code-selective bandpass filter (CS BPF) for FD communication. The CS BPF passes the desired signal in a frequency band only when the signal is tagged with a PN code that matches the code at the filter. This approach is shown to reject TX SI in the same band as the desired RX signal. The coded TX signal is orthogonal through appropriate code selection from a codebook and the PN sequence spreads the signal energy outside the filter BW.

Then, the chapter discusses a reconfigurable bandstop filter (BSF) - notch filter - that can be reconfigured to improve rejection while offering high power handling. The notch filter uses a series N-path notch filter in conjunction with an impedance-transformed shunt N-path filter to improve the TX rejection or notch concurrent bands. Applying

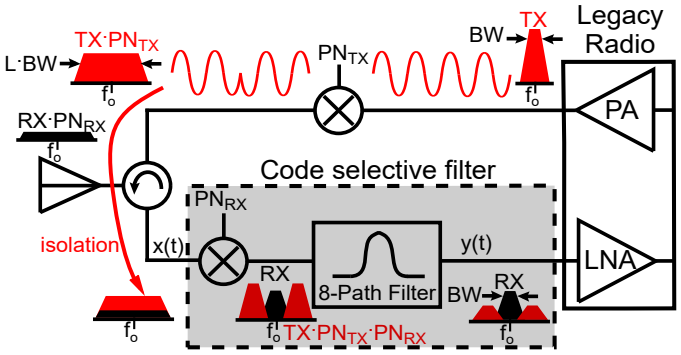


Figure 2.1: Concept of RF code-domain signal processing for TX SI rejection.

the TX PN codes to the notch filter in conjunction with the RX coded CS BPF improves the achieved rejection beyond that of the standalone CS BPF.

2.1 Code-Selective Bandpass Filters (CS BPF)

The dynamic range (DR) of an FD RX is improved by rejecting the TX SI before the LNA. An alternative approach uses direct sequence spread spectrum (DSSS) techniques to spread the TX SI to separate it from the desired signal directly at the antenna as shown in Fig. 2.1. This approach performs the code-domain signal processing at the antenna and does not require significant radio redesign. N-path filters have been recently used to implement RF TX SI rejection for FD transceivers [28, 43–46]. In [28, 43], an N-path-based circulator was demonstrated at the antenna to reject the TX SI signal. In [44], FD operation was demonstrated by injecting a replica TX signal through an N-path filter and adjusting its gain and phase to cancel the TX SI.

A code-domain approach was shown in [45, 46], where in [45] an LNA with N-path feedback was used to select the desired PN coded input to achieve SI rejection and in [46] a combination of a duplexer and a code modulator were used to achieve SI rejection. Compared to the work in [45], this work has the advantage that it is transparent at the antenna interface and can be used directly with a legacy radio without requiring any

changes in the radio design. In [46], the 51 dB of rejection was obtained mainly from the duplexer while the code modulation only offered 20 dB of rejection as there was no filtering in the RF path. This work also includes on-chip code generation compared to previous work where PN codes were applied off-chip.

The presented CD BPF uses RF DSSS techniques implemented at the antenna interface to reject the TX SI signal without demanding large receive bandwidth to process signals at baseband which would require a high-speed ADC. A series CS BPF is designed and implemented based on modulating a series N-path filter with PN codes to select the desired RX signal modulated by the same code as the filter while rejecting the SI signal modulated by an orthogonal code. The next sections introduce the CS BPF and explain its principle of operation, discuss the implementation of the filter, and finally present the measurement results of the proposed CS BPF.

2.2 N-path CS BPF Operation

A CS filter produces the desired response, either bandpass or band-reject, for signals that fall into the BW of the filter and are modulated with a PN code. In the case of an FD system, shown in Fig. 2.1, both the desired RX and undesired TX signals are tagged with a unique, orthogonal PN sequence.

$$x(t) = RX(t) \cdot PN_{RX}(t) + TX(t) \cdot PN_{TX}(t) \tag{2.1}$$

The PN signal has length L and chip period T_c. At the RX, strong TX SI is eliminated by modulating the RX signal with an orthogonal PN sequence. Under ideal circumstances,

$$y(t) = \int_0^{LT_c} PN_{RX} \cdot x(t)dt \approx L \cdot RX(t) + REJ \cdot TX(t) \tag{2.2}$$

The approximation recognizes that the processed signal consists of two components: a de-spread RX signal that is increased due to the processing gain (PG) of the PN signal processing and a rejected TX signal that is spread outside the RF BW by the product of the two orthogonal PN codes. Since the latter component is out-of-band due to orthogonality between the PN_{RX} and PN_{TX} codes, it must be filtered so that only the recovered RX signal remains. The rejection (REJ) of the CS BPF depends on the cross-correlation between the two orthogonal PN codes (PN_{RX} and PN_{TX}). To remove the spread channel components, a BPF is placed in the RF path passing only the desired de-spread RX signal as shown in Fig. 2.1. The BPF BW is much smaller than the DSSS BW at the filter input. The proposed scheme demands a BPF with low insertion loss (IL) and high linearity. Recent work on N-path filters has demonstrated the ability to produce high-quality factor (Q) responses centered around the RF carrier frequency that can be tuned with the local oscillator (LO) [33, 34, 47]. Both the spreading and filtering operations are performed in a single CS BPF that operates as a code-domain RF correlator.

2.3 N-path CS BPF Implementation

The proposed CS BPF, illustrated in Fig. 2.2, modifies a series N-path filter by applying the PN sequence to the first set of switches. The 8-path filter uses the 2-port N-path filter architecture to increase the filter rejection compared to the shunt N-path version [48].

The first set of switches modulate the RF signal by a PN code modulated on top of the $1/N$ duty-cycle clocks with two parallel switches. When the PN code is 1, the upper pair of switches are enabled and the RF signal passes through the switch. When the PN code is 0, the lower pair of switches are enabled reversing the phase of the input RF

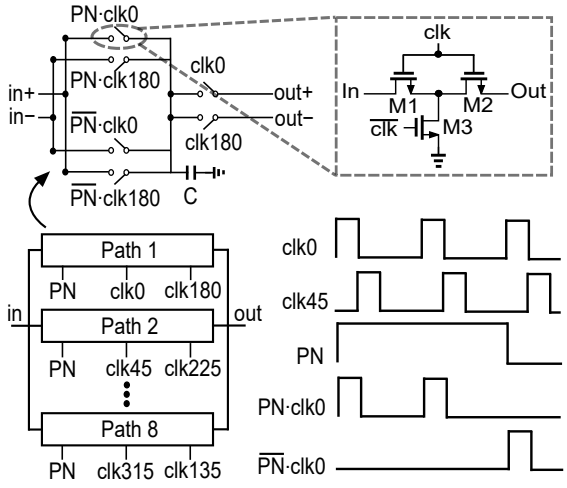


Figure 2.2: Schematic of the series 8-path CSF.

signal (multiplying it by -1). Therefore, the filter de-spreads the input signal when it is tagged with a matched PN code within the N-path BW. Meanwhile, the filter spreads any other TX SI or jammers outside the N-path BW to reject these signals.

Each switch is implemented as a series-shunt-series switch to improve linearity for thin-oxide devices. The series switches (W/L=25μm/40nm) are controlled by 12.5% duty cycle clock pulses while the shunt switch (W/L=2μm/40nm) is controlled by 87.5% duty cycle clock pulses. A large blocker can degrade the filter rejection by turning on the switches of the N-path filter. The shunt switch prevents the blocker from affecting the second series switch (M2) connected to the N-path capacitor protecting the voltage stored on it. Simulations indicate that the series-shunt-series switch provides a 3 dB and 3.5 dB increase in the third-order intercept point (IIP3) and 1-dB compression point (P1dB) respectively.

The schematic of the CSF chip is shown in Fig. 2.3 and consists of an 8-path CS BPF, a frequency divider to generate the 12.5% duty cycle non-overlapping clock pulses driving the filter switches, a 16-length Walsh code generator, switches control circuitry multiplying the generated Walsh code by the clock pulses, and source follower output

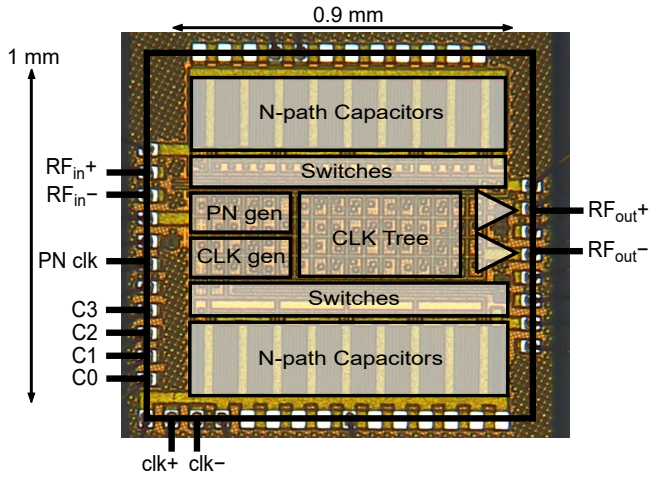


Figure 2.3: CSF chip schematic and die microphotograph in 45-nm CMOS SOI.

buffers driving 50 Ω loads.

2.4 N-path CS BPF Measurements

The CS BPF was implemented in a 45-nm complementary metal-oxide-semiconductor (CMOS) silicon-on-insulator (SOI) process. It occupies an active area of $1 \times 0.9\ mm^2$ as shown in Fig. 2.3. The measured $S21$ of the filter in a 50 Ω environment when PN operation is shut off is shown in Fig. 2.4 and compared to simulation (dashed). The CS BPF is tuned from 300 MHz to 675 MHz and consumes 28.2 mA at 500 MHz from a 1-V supply. The IL of the filter ranges from 1.8 dB to 7.5 dB across the tuning range and

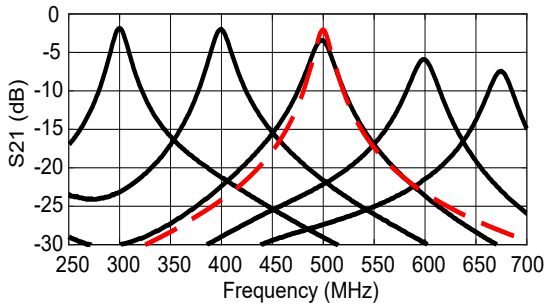


Figure 2.4: Measured $S21$ of the 8-path filter (simulation in dashed line).

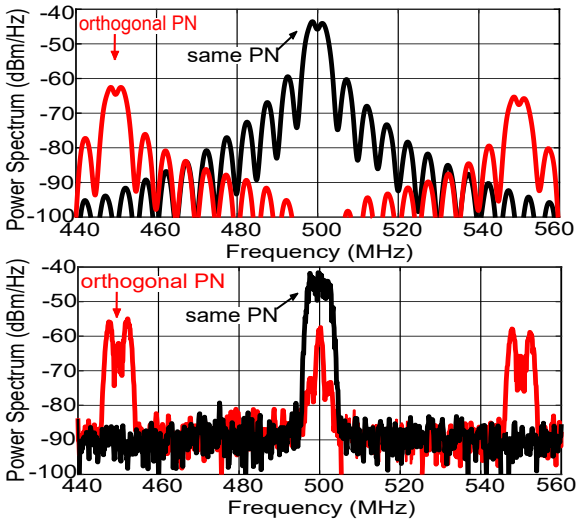


Figure 2.5: Simulated (up) and measured (down) output spectrum of the CS BPF.

the 3-dB signal BW is 20 MHz.

The filter code rejection was measured by applying an RF carrier modulated by a 5 MSymbol/sec Gaussian pulse shaped binary phase-shift keying (BPSK) random data modulated by a 100 Mchip/sec PN code to the filter. The output power was measured for both cases where the filter is modulated by the same PN code and orthogonal PN code to that of the input. The synchronization between the input RF signal and on-chip generated Walsh codes was done by delaying the PN clock using an off-chip programmable delay line until both codes are aligned. The simulated and measured output spectrum for matched and unmatched codes are shown in Fig. 2.5 and illustrate how the filter spreads the orthogonal input out of the filter BW allowing the rejection of the TX SI. The CS BPF average rejection is 23.2 dB over 10 MHz (the signal BW). The out-of-band (OOB) signal can be easily attenuated by additional filtering in the receiver chain.

The rejection is limited by reciprocal mixing and LO leakage and can be enhanced to approach simulations (>40 dB) by improving the clock circuitry and its phase noise as will be demonstrated in later chapters [49]. The measured LO leakage was around -55 dBm while the NF was 7.2 dB at 500 MHz and was degraded by 1 dB for a -25 dBm

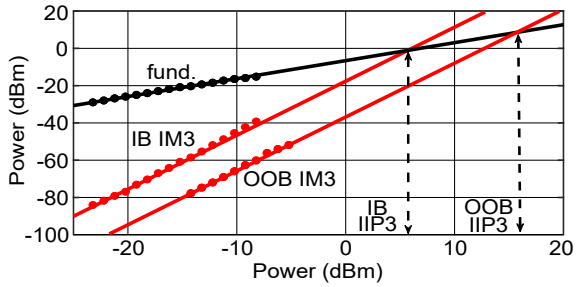


Figure 2.6: Measured in-band and out-of-band IIP3 of the filter.

blocker. Simulations indicate that the NF is improved to 5.4 dB by improving the rise and fall times of the clock pulses at the expense of 50% increase in the power consumption of the filter.

The linearity of the filter was characterized at 500 MHz without PN code modulation. The in-band (IB) IIP3 of the filter is +6.3 dBm at an offset frequency of 6 MHz, while the OOB IIP3 is +15.7 dBm at an offset frequency of 100 MHz as shown in Fig. 2.6. The measured blocker 1-dB compression point is 2 dBm for an IB blocker at an offset frequency of 10 MHz and 5 dBm for an OOB blocker at 100 MHz offset as shown in Fig. 2.7. Table 2.1 summarizes the achieved performance of the proposed CS BPF and how it compares with previously reported FD systems.

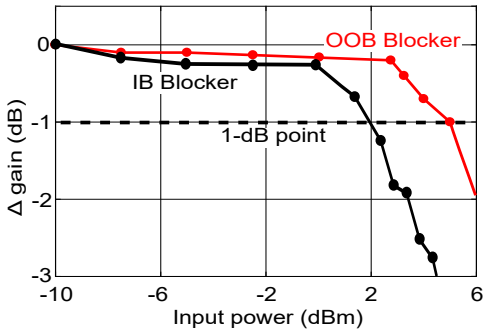


Figure 2.7: Measured in-band and out-of-band blocker 1-dB compression point.

Table 2.1: CS BPF performance summary and comparison

	[28]	[43]	[45]	[46]	This work
Architecture	Circulator & BB rej.	Circulator	Code-domain	Duplexer & Code-domain	Code-domain
Technology	65 nm	65 nm	65 nm	45 nm	45 nm
Freq. [GHz]	0.6-0.8	0.6-0.975	0.3-1.4	1.1-2.5	0.3-0.675
IIP3 (IB)	-33 dBm*	-18.4 dBm*	-26 dBm*	-	6.3 dBm
IIP3 (OOB)	19 dBm*	15.4 dBm*	-	-	15.7 dBm
BW	12 MHz	20 MHz	1 MHz	1 MHz	10 MHz
NF	10.9 dB*	8 dB*	4.9 dB*	4.2 dB**	7.2 dB
Power	159 mW*	108 mW*	36 mW*	50 mW*	28.2 mW
Active Area	1.4 mm^2	0.94 mm^2	0.31 mm^2	1.4 mm^2	0.9 mm^2
SI Rejection	42 dB	40 dB	38.5 dB	51 dB***	23.2 dB

*receiver, **at LNA i/p, ***41 dB from duplexer

2.5 Improving Rejection using CS Notch Filters

The previous sections demonstrated a CS BPF which showed good TX SI rejection performance using Walsh codes. To reject TX SI, only a short PN code is required. To handle U users, an $M > U$ length code should be selected. To increase M, either the spread-spectrum bandwidth is increased or the signal bandwidth is reduced. Although, Walsh codes provide excellent rejection; a practical system could not rely on using Walsh codes only due to difficulty in synchronization due to repetitive nature, limited processing gain, and ease of jamming with un-coded blockers. Also, they require all transmitters and receivers to be synchronized for orthogonality (meaning that 4 codes should be synchronized, two at each transceiver). A practical system would need to have good rejection while using any family of PN codes to be able to serve multiple users. This can be achieved by the addition of the TX notch filter.

The rejection over the signal BW of the code-domain RX equals PG when used with a long random PN sequence and it can be increased beyond PG by the CS notch filter. Fig. 2.8 shows the effect of the notch filter BW on the rejection and IL for random PN codes with varying code length at a fixed chip rate of 128 Mchips/sec. Without the notch filter, the rejection is 21.8 dB, 17.3 dB, and 14.2 dB for 128, 64, and 32 length codes respectively (≈PG). Increasing the notch BW increases the achieved rejection at

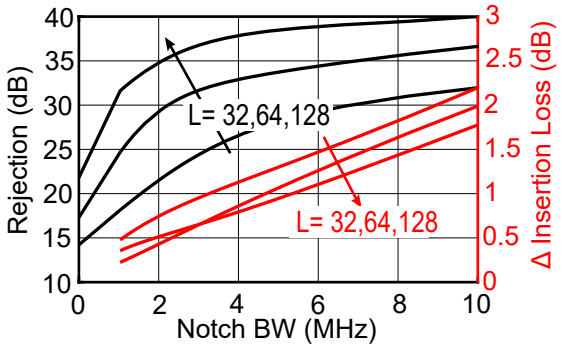


Figure 2.8: Effect of notch filter and code length on rejection (black) and IL (red) from system level simulations.

the expense of a slight increase in IL.

Simulations indicate an optimal trade-off occurs for a notch filter BW that is around 3 MHz. The 3-MHz notch filter increases the rejection to 36.8 dB, 31.7 dB, and 24.4 dB with an extra IL of 0.6 dB, 0.7 dB, and 1 dB for 128, 64, and 32 length codes respectively. So, the notch filter is effective in increasing the rejection beyond the PG of the used codes and this is more profound with higher length PN codes where the rejection increases by 15 dB with a 0.6 dB increase in IL for 128-length codes. It is worth mentioning that the notch filter also increases the rejection of Walsh codes allowing them to achieve better rejection.

The next sections present the design and implementation of a reconfigurable notch filter that can be configured into different modes of operation and the next chapter discusses the application of the notch filter in a CD FD RX in conjunction with the CS BPF presented earlier.

2.6 Reconfigurable Notch Filters

N-path filters are candidates for reconfigurable filters to support multi-band or software-defined radios (SDR) where the operating frequency, BW, and linearity of the RF front-

end can be easily programmed. While prior research has been devoted to reconfigurable bandpass N-path filtering to demonstrate high-order response (4^{th}, 6^{th}, and 13^{th} order) [50–52], and concurrent multiband reception for carrier aggregation (CA) applications [53], less research has focused on the need for high-order notch filters. Additionally, an uplink CA multi-band transceiver might suffer from multiple TX leakage signals operating at peak output powers in different frequency bands.

The following sections present a reconfigurable notch filter for TX leakage suppression which can be reconfigured to improve rejection while offering high power handling. The notch filter uses a series N-path notch filter in conjunction with an impedance-transformed shunt N-path bandpass filter to improve the TX rejection or notch concurrent bands. The TX notch filter can be reconfigured as a dual notch (DN) filter to suppress two different TX bands, or as a high-order (HO) notch filter suppressing a main TX by more than 50 dB, or as a single notch for low power (LP) consumption depending on the transceiver operation. Each of these modes is frequency tunable offering greater flexibility for the transceiver programmability. The notch filter can be placed between the duplexer and LNA in a multi-standard transceiver to avoid desensitizing the LNA with large TX leakage. It is worth mentioning that the power overhead of the notch filter is minor compared to that of the preceding PA (>1 Watt) such that the overall transceiver power consumption is still dominated by the PA.

2.7 Proposed Notch Filter Architecture

N-path notch filters can be implemented in either a series [54] or an impedance-transformed shunt [55] filter topology. Series N-path notch filters translate a high-pass RC response at DC to the RF frequency determined by the non-overlapping LO pulses of the N-path switches. Shunt N-path notch filters employ impedance transformation to

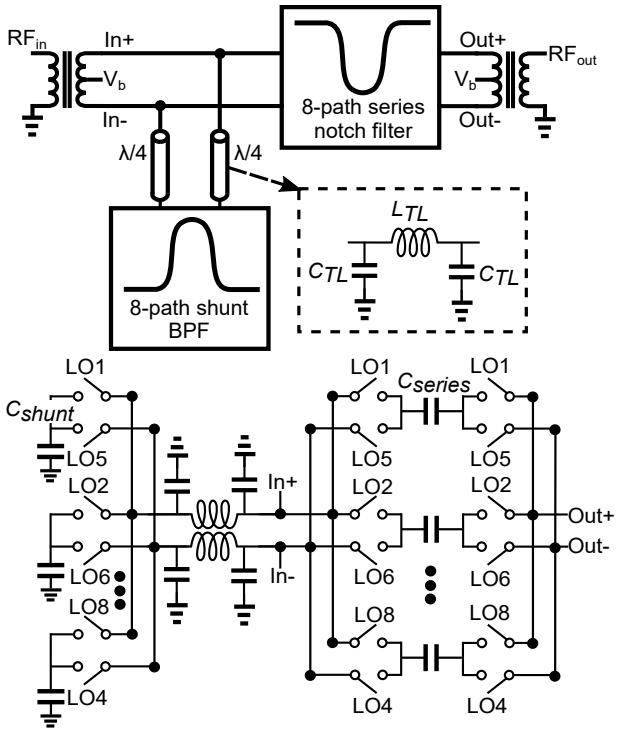


Figure 2.9: Proposed reconfigurable notch filter using a series notch N-path filter and an impedance transformed shunt bandpass N-path filter.

transform the bandpass N-path response to a notch response using quarter-wave ($\lambda/4$) transmission lines (TL). Utilizing a cascade of the series and shunt notch filters produces the proposed reconfigurable notch filter shown in Fig. 2.9.

The input impedance of a shunt N-path BPF is [34]:

$$Z_{in,sh}(\omega) = R_{sw} + [(R_{sw} + R_s)\frac{N\gamma}{1 - N\gamma}]//\gamma Z_{BB}(\omega - \omega_o), \tag{2.3}$$

where R_{sw} is the switch resistance, R_s is the source impedance, γ is a harmonic scaling factor given by $\frac{N}{\pi^2}sin^2(\frac{\pi}{N})$ derived in [56], N is the number of paths, and Z_{BB} is baseband capacitance impedance translated to RF at ω_o. The input impedance is high around the clock frequency of the N-path switches resulting in a bandpass response. A $\lambda/4$ TL

transforms the shunt filter input impedance to be:

$$\widetilde{Z_{in,sh}}(\omega) = \frac{Z_o^2}{R_{sw} + [(R_{sw} + R_s)\frac{N\gamma}{1-N\gamma}]//\gamma Z_{BB}(\omega - \omega_o)}, \tag{2.4}$$

where Z_o is the characteristic impedance of the TL. As such, the input impedance around ω_o is low instead due to the impedance inversion of the TL. Similarly, the input impedance of a series N-path notch filter is given by:

$$Z_{in,ser}(\omega) = 2R_{sw} + R_L + [(2R_{sw} + R_s + R_L)\frac{N\gamma}{1-N\gamma}]//\gamma Z_{BB}(\omega - \omega_o), \tag{2.5}$$

where R_L is the load impedance of the filter.

The rejection of the series and shunt filters can be derived using the equivalent circuit model in Fig. 2.10a and 2.10b [54]. The model simplifies the N-path filter impedance around the clock frequency and at far frequencies based on (2.4) and (2.5). Assuming $R_s = Z_o$, the rejection of both filters is given by:

$$REJ = \frac{1}{1-N\gamma} = \frac{\pi^2}{\pi^2 - N^2 sin^2(\pi/N)}, \tag{2.6}$$

where REJ is the difference between the IL and notch depth of the filter. This results in 26 dB of rejection for 8-path filters independent of the switch resistance for a 1^{st} order approximation.

High-order filtering is realized by cascading two different notch filters architectures. In contrast to cascading series N-path filters which only increases the IL of the cascaded filter without improving the achieved rejection due to charge sharing between the N-path capacitors [51], the $\lambda/4$ TL isolates the shunt and series filters. At the clock frequency, the inverted shunt filter creates a short that shunts the input while the series filter presents an open to the load thus improving the achieved rejection. At larger frequency offsets, the

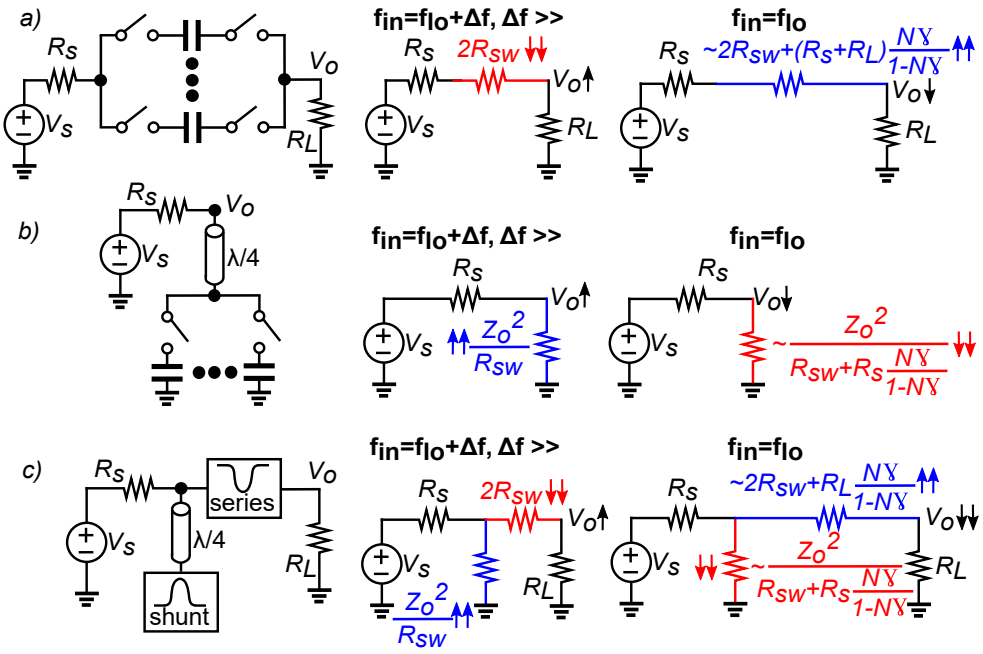


Figure 2.10: Model for calculating the rejection of the notch filter. a) Series Notch filter, b) Shunt impedance-inverted notch filter, c) High-order notch filter.

impedance transformation presents an effective open circuit shunt to the input allowing nearly the same IL of a single series filter. The rejection is derived using the circuit model of Fig. 2.10c[1].

$$REJ_{HO} \approx \frac{R_L}{R_L + R_S + 2R_{sw}} \left(\frac{\pi^2}{\pi^2 - N^2 sin^2(\pi/N)}\right)^2. \tag{2.7}$$

The rejection reaches 45 dB for 8-path filters using an R_{sw} of 5 Ω demonstrating the improvement of the proposed filter compared to standalone filters.

The impedance inverted shunt filter is controlled independently from the series notch filter to realize arbitrary notch relationships. Depending on the clock frequency, Fig. 2.11 summarizes different modes of operation. In the dual-notch (DN) mode, each filter is clocked at a different clock frequency resulting in two notches suppressing TX leakages

[1]For $f_{in} = f_{lo}$ in Fig. 2.10c, the impedance seen from the source side is shorted by the small impedance of the shunt filter and thus is not included in the impedance expression of the series filter.

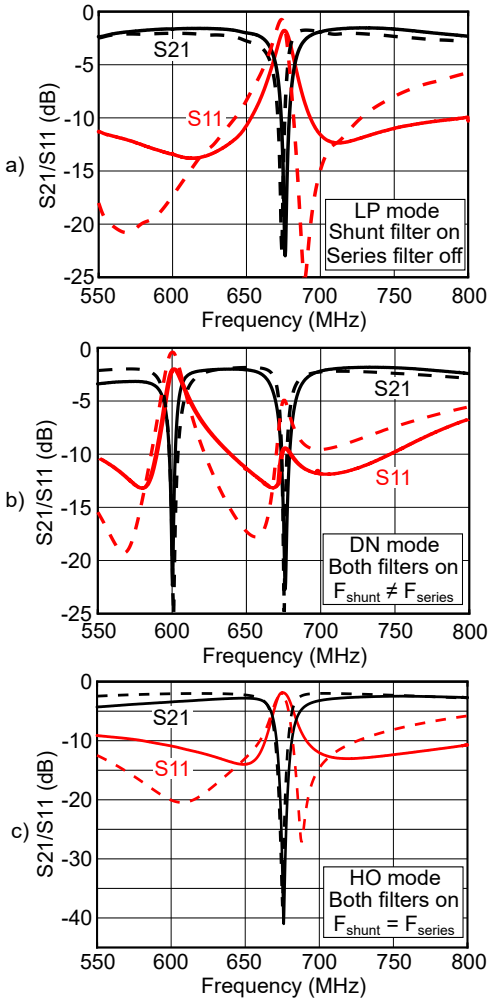


Figure 2.11: Different modes of the reconfigurable notch filter (simulations in dashed line and measurements in solid line). a) LP mode, b) DN mode, c) HO mode.

at two distinct bands. In the high-order (HO) notch mode, both filters are clocked at the same frequency resulting in deeper notch depth compared to a single notch filter. Finally, the shunt filter is turned on while turning off the series filter (clocked at a few MHz such that the power consumption is reduced and the response due to higher harmonics would not affect the IL in the desired tuning range) allowing a single notch in the desired tuning range with reduced power consumption in the low-power (LP) mode. The shunt filter is activated in the LP mode as it consumes nearly half the power of the series filter due to the reduced number of switches reducing the dynamic power of the clock generation.

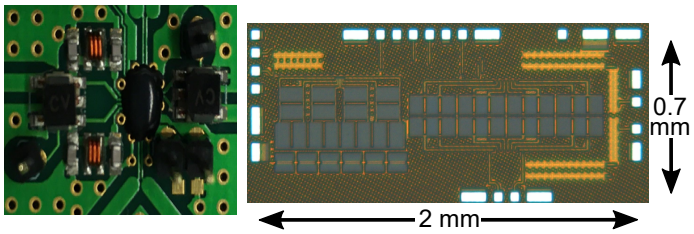


Figure 2.12: Assembled board of the filter with CLC TL and chip micrograph in 45-nm RFSOI process.

2.8 Notch Filter Implementation

Both filters are implemented as 8-path filters for improved rejection and IL. The switches are implemented as transmission gate switches for increased power handling. The NMOS and PMOS switches have W/L of 40μm/40nm and 62.4μm/40nm with threshold voltages of 0.26 V and 0.27 V, respectively. The switches were designed wide enough to avoid degrading the on-state resistance and IL of the filter. The series filter has a unit capacitance of 62.5 pF while the shunt filter has a unit capacitance of 50 pF. The capacitors are implemented using high-density, high-Q metal-insulator-metal (MIM) capacitors. The N-path capacitors dominate the chip area due to the targeted 5 MHz BW for the notches and the area can be reduced significantly for wider BW according to the system's specifications. The chip also includes the clock generation network for the 12.5% duty cycle complementary non-overlapping clock pulses for the 8-path switches with a simulated phase noise of -160.3 dBc/Hz at 1 MHz offset and -165 dBc/Hz at 10 MHz offset at 0.75 GHz.

The $\lambda/4$ transmission lines for the shunt filter impedance transformation were implemented on-board using lumped CLC π-section as shown in Fig. 2.9. A CLC π-network with a single inductor, an 8.1 nH air core inductor with a Q of 130, was selected to allow the same biasing voltage for the series and shunt switches while using the minimum number of inductors as compared to LCL π-network and CLC/LCL T-networks. Simulations

indicate that using an on-chip inductor with a Q of 10 is still a feasible option and only degrades IL by 0.5 dB and rejection by <5 dB in the HO mode. Besides higher Q, board inductors have the advantage of simpler band tunability by changing the assembled inductor compared to the on-chip counterpart. However, On-chip CLC networks might be preferable at higher frequencies at the expense of higher power consumption for the non-overlapping clock generation.

The chip is implemented in a 45-nm CMOS SOI process and the chip micrograph is shown in Fig. 2.12 occupying an active area of 1.4 mm^2. The measurements were performed on a chip-on-board assembly of the notch filter.

2.9 Notch Filter Measurements

2.9.1 Small Signal Measurements

Fig. 2.11 illustrates the measured $S21$ in the three different modes showing the rejection of the LP, DN, and HO notch modes. S-parameters were measured across the tuning range for the three different modes. The measured $S21$ in the LP mode is shown in Fig. 2.13 (left plot) where the IL ranges from 1.2 dB to 1.7 dB and the notch depth ranges from 18.3 dB to 23.4 dB. The shunt notch filter is tunable from 0.55 GHz to 0.8 GHz limited by the tuning range of the $\lambda/4$ impedance transformation but the center frequency can be varied by changing the inductance and capacitance values of the on-board CLC π-network according to the desired operating frequency range. The rejection is >10 dB across at least 5 MHz BW across the tuning range. The power consumption ranges from 11.9 mW to 15.3 mW at 1-V supply across the tuning range in the LP mode.

Similarly, the measured $S21$ in the DN mode is illustrated in Fig. 2.13 (middle plot) where the shunt filter is fixed at 0.675 GHz and the series filter center frequency is tuned.

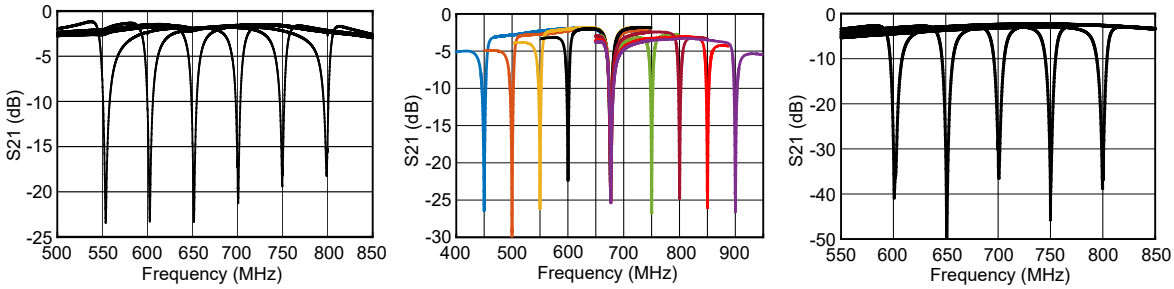


Figure 2.13: Measured $S21$ in different modes of the reconfigurable notch filter across the tuning range. (Left) LP mode tuned from 0.55 GHz to 0.8 GHz. (Middle) DN mode with the shunt filter at 0.675 GHz and the series filter tuned from 0.45 GHz to 0.9 GHz. (Right) HO mode tuned from 0.6 GHz to 0.8 GHz.

The series filter can be tuned between 0.2 GHz and 1.2 GHz where the IL around the center frequency of the $\lambda/4$ impedance transformation is small but degrades for far off frequencies. Thus, the DN mode tuning range is limited from 0.45 GHz to 0.9 GHz to minimize the IL across the whole tuning range. The measured IL ranges between 1.8 dB and 3.3 dB as shown in Fig. 2.13. The depth of the series notch ranges between 22.4 dB and 32.9 dB while that of the shunt notch ranges between 21.5 dB and 25.4 dB. The rejection for both notches is >10 dB across around 5 MHz BW. The power consumption in the DN mode depends on the operating frequency of both the series and shunt filters and ranges between 34.4 mW and 40.7 mW when the shunt filter is clocked at 0.675 GHz and the series filter is tuned between 0.45 GHz and 0.9 GHz.

Finally, the measured $S21$ in the HO notch mode is shown in Fig. 2.13 (right plot) where the filter is tunable from 0.6 GHz to 0.8 GHz. The tuning range is slightly smaller than that of the LP mode shunt filter to guarantee a rejection >35 dB across the whole tuning range. The IL ranges from 2.3 to 2.9 dB and the peak notch depth is >50 dB at the center frequency of $\lambda/4$ TL at 0.65 GHz. The rejection is > 20 dB and 10 dB across a BW of about 5 MHz and 10 MHz respectively in the HO notch mode. The power consumption in the HO notch mode ranges from 33.7 mW to 43.9 mW across the tuning range where both filters have the same clock frequency.

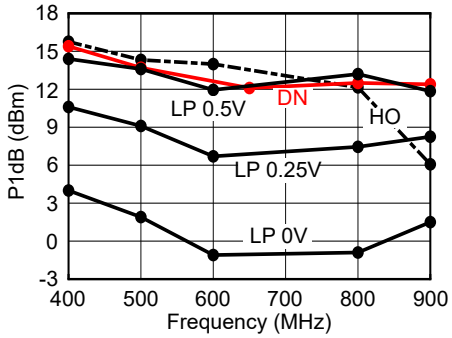


Figure 2.14: Measured P1dB across the tuning range in different modes.

2.9.2 Compression, Linearity and NF Measurements

The 1-dB compression point (P1dB) was measured in the different operating modes of the proposed notch filter. The P1dB compression point exceeds 12 dBm across most of the tuning range as shown in Fig. 2.14 with a peak P1dB of 15.8 dBm in the HO notch mode due to the linearized transmission gate switches. Fig. 2.14 demonstrates the benefit of the transmission gate switches by plotting the P1dB in the LP mode as a function of the RF bias voltage (drain/source voltage of the switches) where the P1dB increases at 0.5 V ($V_{DD}/2$). Similarly, the linearity of the notch filter was characterized in the three different modes. The IIP3 of the notch filter ranges between 11.8 dBm and 15 dBm across the tuning range in the different modes as shown in Fig. 2.15. The notch rejection was also measured versus the jammer power in the HO notch mode as shown in Fig. 2.16. The notch depth degraded by 1 dB for a 6 dBm jammer power and the filter maintained >30 dB of rejection till ∼10 dBm jammers.

The NF of the notch filter was measured in the three operating modes. The NF was measured by tuning the filter to different center frequencies and the minimum NF across the band at each frequency is reported. The measured NF is plotted in Fig. 2.15 where the minimum NF ranges between 3 dB and 5 dB when the notch filter is tuned between 550 MHz and 750 MHz. The minimum NF in each of the three modes is 3 dB, 3.25 dB,

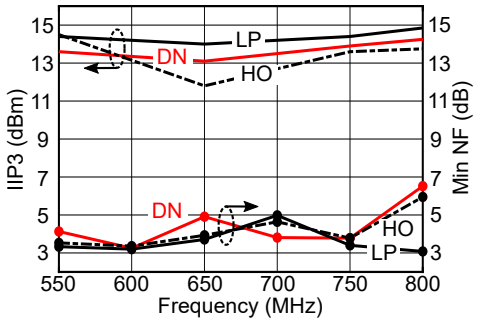


Figure 2.15: Measured IIP3 and NF across the tuning range in different modes.

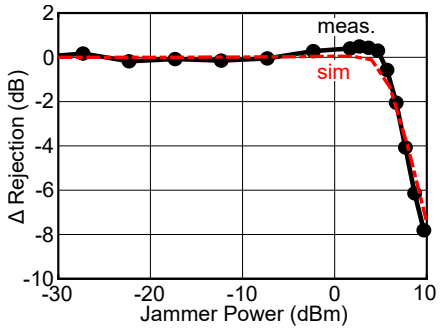


Figure 2.16: Notch rejection versus jammer power in the HO notch mode at 0.7 GHz.

and 3.36 dB for the LP, DN, and HO modes respectively. The NF increases to 6.5 dB and 6 dB in the DN and HO modes at 800 MHz LO frequency. This NF degradation is attributed to the increased rise and fall times of the series filter clock pulses as this was not observed in the LP mode where the series filter is turned off. This can be overcome by increasing the power consumption of the series filter clock drivers to maintain switching speed at higher frequencies. LO leakage was measured in the different operating modes. The LO leakage is less than -60 dBm across the whole tuning range for each mode.

Table 2.2 summarizes the performance of the proposed notch filter and compares the measured results with the state-of-the-art for N-path based passive notch filters. To the authors' knowledge, this is the 1^{st} reconfigurable notch filter covering multiple bands simultaneously as well as providing high-order notch response. The proposed cascaded shunt/series notch filter achieves one of the highest rejections (>50 dB) in the HO mode

Table 2.2: Reconfigurable notch filter performance summary and comparison

	ISSCC12 [54]	IMS18 [55]	ISSCC20 [57]	This Work		
				LP	DN	HO
Topology	Series Notch	$\lambda/4$ Inv. Shunt Notch	Neg. Trans-Res. Notch	Series Notch + $\lambda/4$ Inverted Shunt Notch		
Tech. (nm)	65	45	65	45		
Freq. (GHz)	0.1-1.2	0.9-1.1	0.2-1	0.55-0.8	0.45-0.9	0.6-0.8
N-Paths	8	4	4	8		
Power (mW)	3.5-30	6.18	7.2-13.2	11.9-15.3	34.4-40.7	33.7-43.9
IL (dB)	1.4-2.8	2.4	0.8-3.5	1.2-1.7	1.8-3.3	2.3-2.9
Rej. (dB)	21-24	20-23	45->50	18.3-23.4	21.5-32.9	36.6->50
NF (dB)	1.6-2.5	4-5	1-4	3-5		
P1dB (dBm)	6	NR	5-7	11.9-14.4	12.1-15.4	6.1-15.8
IIP3 (dBm)	>17	22.6	17-21.5	14.4-15	13.1-15	11.8-14.5
Area (mm^2)	0.87	1.77	0.18	1.4		

while having the highest P1dB compression point.

2.10 Conclusion

This chapter presented a series CS BPF for FD communication. The CS BPF achieves a TX SI rejection of 23.2 dB over a 10 MHz BW using on-chip generated Walsh codes. The measured results show 15.7 dBm OOB IIP3 and 6.3 dBm IB IIP3 at 1-V supply in a 45-nm CMOS SOI process. The CS BPF operates from 300 MHz to 675 MHz and consumes 28.2 mA from a 1-V supply at 500 MHz.

A high performance, reconfigurable, multiband notch filter was also presented in the chapter. The 4^{th}-order notch provides >40 dB rejection for a single TX channel. In the dual-notch mode, the notches can be tuned to two different TX channels. Finally, a low-power single notch mode provides >20 dB rejection with low power consumption. The filter is implemented in a 45-nm CMOS SOI process and consumes between 11.9 and 43.9 mW at 1-V supply in the different modes across a tuning range from 0.45 to 0.9 GHz while providing a peak rejection >50 dB and P_{1dB} as high as 15.8 dBm.

Chapter 3

A High-Rejection Code-Domain Full-Duplex Receiver

As demonstrated in the previous chapter, code-domain signal processing techniques implemented in the RF domain enable FD and STAR applications. With direct sequence spread spectrum (DSSS) techniques and RF correlators, the TX SI is separated from the RX signal at the antenna interface. The processing gain inherent in the code-domain approach increases the TX SI rejection in the RF domain to relax the filtering and linearity requirements of the RX. This chapter expands on the previous chapter to demonstrate a code-domain RX with 52 dB of TX SI rejection. The RX employs a TX code-notch and an RX code-pass filter operating at the same center frequency to increase the achieved rejection.

First, the chapter analyzes the different properties of high-rejection RF code-domain filters. Then, it presents the circuit details of the RX including the code-pass and code-notch filters in a 45-nm CMOS SOI process. Finally, measurement results and an over-the-air (OTA) 2x2 FD link demonstration are presented.

3.1 Code-Domain FD RX Properties

This section presents a detailed analysis of the properties of the proposed CD FD RX. First, it gives a brief overview of previous FD RX implementations and the challenges that the proposed RX tries to overcome. Then, the PN modulated N-Path code-pass and code-notch filters transfer functions are derived and the properties of different PN code families are discussed. Next, useful observations regarding the rejection, linearity, harmonic folding, LO leakage, and spurious-free dynamic range (SFDR) of PN-modulated N-path filters are discussed.

3.1.1 Comparison with Previous Receivers

FD techniques allow the concurrent operation of the TX and RX. A common challenge for FD communications is the rejection of a strong TX signal so that it does not desensitize the RX. Prior TX SI rejection techniques were recently proposed to support FD operation as shown in Fig. 3.1, including CMOS circulators [22–24, 58], electrically-balanced duplexers (EBD) [18, 19, 59] and cancellation in the RF, analog, and digital domains [22, 59]. Up to 100 dB of TX SI rejection has been achieved from a combination of these techniques. Nevertheless, additional rejection is required to tolerate average TX power levels as high as 27 dBm.

As demonstrated in the previous chapter, code-domain techniques are another alternative for implementing FD transceivers [35, 46, 60]. By allocating orthogonal PN codes to the TX and RX signals, the RX signal is distinguished from the TX signal allowing their co-existence at the same RF band. The TX SI rejection achieved in the RF domain relaxes the linearity requirements of the RF RX.

Also, wireless transceivers operate in congested environments where the scarce RF spectrum is shared among different devices. Previous FD receivers [18, 19, 22–24, 58, 59]

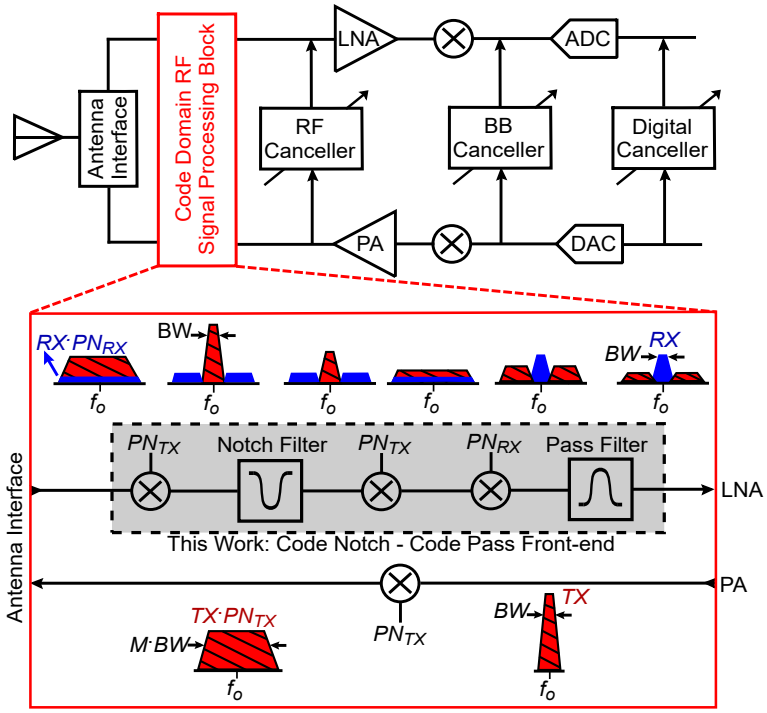


Figure 3.1: Proposed RF code-domain signal processing for TX SI rejection.

focused on rejecting the main TX SI from the co-existing TX. However, any co-located nearby blocker could degrade the RX sensitivity. An RF filter is required at the RF front-end to operate without being susceptible to co-located blockers. This RF filter is usually implemented on board using a surface acoustic wave (SAW) filter for improved rejection and this increases the area and cost overhead of the RX. Compared to prior FD techniques, the proposed CD RX has the extra advantage of blocker tolerance due to PN codes spreading. Thus, it can reject the main TX SI as well as other blockers. The proposed code-domain approach trades lower signal BW for increased interference tolerance as other blockers are spread out-of-band (OOB) by the PN code correlation.

Recently, N-path filters were proposed to replace SAW filters at the RF interface of frequency division duplex (FDD) receivers [33,47,51,61–67]. However, a SAW-less N-path RX suffers from limited OOB rejection compared to SAW filters requiring the use of high-order filters at the expense of increased power consumption and NF. Moreover, N-path

filters suffer from LO leakage and harmonic folding issues which can be as problematic as SI in FD systems. Code-modulated N-path filters provide RF signal processing to support FD transceivers along with relaxing the LO leakage and folding problems with comparable power and NF to high-order N-path filters [51,66,67] as demonstrated in the following sections.

3.1.2 Proposed CD FD RX Architecture

The proposed code-domain RX for SI rejection is shown in Fig. 3.1. A PN code of length M is applied to the TX signal and spreads the signal BW over $M \cdot BW$. The code length is determined by the number of simultaneous channel users and directly increases the spreading bandwidth for a given BW. TX signal spreading can be done either before the power amplifier (PA) [46] or after the PA using high-power, low-loss modulators [68, 69]. The DSSS TX signal is distributed to a shared antenna with a circulator or an EBD. Imperfect isolation allows some TX SI to leak into the RX signal path and overwhelm the desired RX signal. The code-domain RX operates by correlating the desired signal against a matching PN code (PN_{RX}) while rejecting the TX signal out of the signal band due to its orthogonal PN code (PN_{TX}). The proposed approach uses two code-domain N-path filters to eliminate the TX SI. First, a code-notch filter (CNF) identifies the TX signal and notches it within the signal BW. Second, a code-pass filter (CPF) identifies the RX signal and passes it while rejecting the residual TX signal.

For code-domain signal processing, the input signal is first multiplied by the TX PN code (PN_{TX}) to de-spread the TX signal and filter the signal energy through a CNF. Meanwhile, the RX signal is spread out of the notch filter bandwidth with minimal IL. Next, the notch filter output is re-multiplied by the TX PN code (PN_{TX}) to restore the RX signal. Finally, the RX signal is de-spread through multiplication by the RX PN

code (PN_{RX}) and it passes to the LNA after filtering by a bandpass filter (BPF). The BPF also rejects the residual TX signal which is spread by the RX PN code (PN_{RX}) out of the BPF BW.

Although the addition of the TX notch filter increases the IL, it increases the SI rejection and therefore the link gain. It also does not increase the synchronization complexity compared to prior code-domain receivers [46,60] as the TX PN code is known in advance and its generation can be shared between the TX and RX.

3.1.3 Interference Tolerance for CD FD Receivers

An additional challenge in FD systems is tolerating not only the TX SI but also other sources of in-band interference. Although many FD receiver proposals cancel the TX SI using a priori knowledge of the TX signal, other nearby in-band blockers will severely limit the RX sensitivity. Otherwise, the FD radio must be frequency duplexed with respect to other transmitters reducing spectral efficiency and requiring narrowband filters.

RF code-domain signal processing has the advantage of being robust to noise and interference [29–31]. The received signal $r(t)$ in a multi-user FD wireless system consists of multiple signal components; a desired signal $s(t)$ modulated by a unique code $PN_s(t)$, K in-band blockers $b_k(t)$, and noise $n(t)$ from the wireless channel (neglecting the TX SI for now).

$$r(t) = PN_s(t)s(t) + \sum_{k=1}^{K} b_k(t) + n(t). \tag{3.1}$$

The code-domain filter correlates the received signal with the desired code $PN_s(t)$

and the output $y(t)$ is

$$y(t) = PN_s(t) \times r(t) = s(t) + PN_s(t) \sum_{k=1}^{K} b_k(t) + n(t). \tag{3.2}$$

The desired signal is de-spread at the RX while blockers are spread OOB by the PN code, and the additive white Gaussian noise (AWGN) is unaffected when multiplied by a long PN code. Without loss of generality, it can be assumed that the signal has a total power P_S and is spread uniformly across the spread spectrum bandwidth (BW_{ss}) with a power spectral density (PSD) of P_S/BW_{ss} after multiplication by the PN code, the blockers have a total power of P_B and this power is distributed uniformly across the spread BW as well after multiplication by the PN code, and AWGN has a noise power density of $N_o/2$.

The signal to interference and noise ratio ($SINR$) over the spread BW at the input of the RX is

$$SINR_i = \frac{\int_{BW_{ss}} \frac{P_S}{BW_{ss}} df}{P_B + \int_{BW_{ss}} \frac{N_o}{2} df} = \frac{P_S}{P_B + \frac{N_o}{2} BW_{ss}}, \tag{3.3}$$

while at the output of the receiver, the $SINR$ over the signal bandwidth (BW_{sig}) is

$$SINR_o = \frac{P_S}{\int_{BW_{sig}} (\frac{P_B}{BW_{ss}} + \frac{N_o}{2}) df} = \frac{P_S}{P_B \frac{BW_{sig}}{BW_{ss}} + \frac{N_o}{2} BW_{sig}}. \tag{3.4}$$

Therefore, the improvement in $SINR$ due to code-domain signal processing is given by the ratio between $SINR_o$ and $SINR_i$.

$$SINR_{imp} = 10log_{10} \frac{SINR_o}{SINR_i} = 10log_{10} \frac{BW_{ss}}{BW_{sig}} = PG, \tag{3.5}$$

where PG is the processing gain $10 \log_{10} M$; M is the used code length. For a code length of 128, the PG is 21 dB and the spreading of the blockers relaxes the filtering

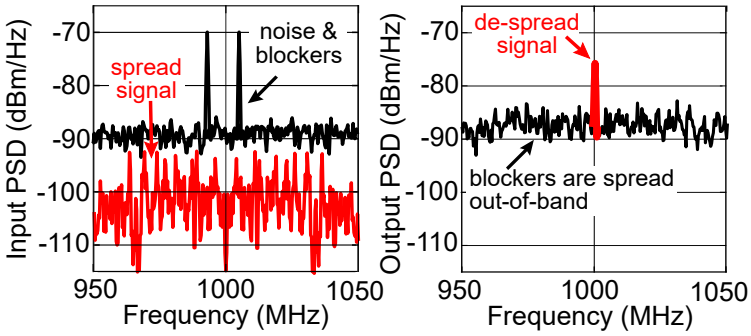


Figure 3.2: Simulated desired RX signal (red), noise and in-band blockers (black) before and after code-domain signal processing demonstrating noise and blocker tolerance.

requirements of N-path filters. Fig. 3.2 plots a simulated spectrum at the input of an RX including the desired signal spread by a 128-length PN code along with AWGN with an input SNR of -11 dB and two in-band blockers at 5 MHz and 7 MHz offset from the center frequency with a signal to interference ratio (SIR) of -9 dB. The output spectrum indicates the desired signal is received correctly with an output SNR and SIR of +9.5 dB and +12.5 dB respectively. The code-domain RX is robust to detect signals below the noise and interference levels with an $SINR$ improvement given by the PG.

3.1.4 Code-Pass and Code-Notch Filter Transfer Functions

Modulating the N-path filter by PN codes generates a frequency response associated with the spectral characteristics of the PN codes. The transfer function of a band-pass N-path filter can be analyzed around integer multiples of the clock frequency ($k\omega_{LO}$) using the approach described in [62] by substituting the baseband capacitor C_{BB} by $N \cdot C_{BB}$ and calculating the transfer function of an RC filter connected to a source resistance R_s. Multiplying this transfer function by the Fourier coefficients of the clock pulses accounts for the frequency conversion at the input and output switches. Finally,

shifting the transfer function around ($k\omega_{LO}$).

$$H_{N,BP}(\omega) = sinc^2(\frac{k\pi}{N})\frac{1}{j(\omega - k\omega_{LO})NR_sC_{BB} + 1}, \tag{3.6}$$

where k is an odd integer for a differential architecture.

The PN-modulated N-path is modeled by adding a PN modulator ahead of the N-path switches resulting in mixing the N-path frequency response with the spectral components of the PN code. Assuming a PN code of length M and chip period T_{chip}, the PN code is periodic with a period $M \cdot T_{chip}$ described as a Fourier series expansion.

$$PN(t) = \sum_{m=-\infty}^{\infty} c_m e^{j\frac{2\pi m}{MT_{chip}}} = \sum_{m=-\infty}^{\infty} c_m e^{j\frac{m\omega_{chip}}{M}}, \tag{3.7}$$

where c_m is the Fourier coefficient of the m^{th} harmonic. Therefore, the output voltage of the code-domain filter is

$$v_{out,BP}(t) = [v_{in}(t) \times PN(t)] * h_{N,BP}(t), \tag{3.8}$$

where $h_{N,BP}(t)$ is the impulse response of the N-path filter and $*$ denotes convolution operation. Using the Fourier transform properties, the output in frequency domain is

$$V_{out,BP}(\omega) = \sum_{m=-\infty}^{\infty} c_m V_{in}(\omega - \frac{m\omega_{chip}}{M})H_{N,BP}(\omega). \tag{3.9}$$

This equation illustrates the frequency translations occurring in a code-modulated N-path filter through mixing of the input spectrum with the spectral components of the PN code. Fig. 3.3 compares the simulated conversion gain of the input spectrum across the spread bandwidth at 1 GHz using a 16-length Walsh code. Only the input spectrum at the specific harmonic content determined by the PN code will be mixed to 1 GHz at

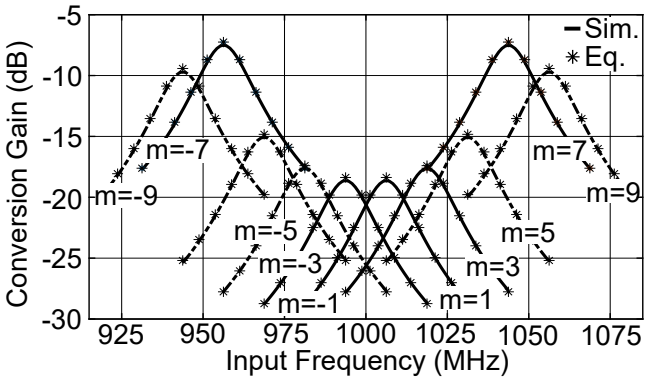


Figure 3.3: Conversion gain of PN-modulated BP N-path filter using Walsh 10.

the filter output while other frequencies are mixed OOB and rejected.

Similarly, the output of a PN-coded N-path notch filter is

$$\begin{aligned} V_{out,notch}(\omega) &= \sum_{m=-\infty}^{\infty} c_m V_{in}(\omega - \frac{m\omega_{chip}}{M}) H_{N,notch}(\omega) \\ &= \sum_{m=-\infty}^{\infty} c_m V_{in}(\omega - \frac{m\omega_{chip}}{M})(1 - H_{N,BP}(\omega)), \end{aligned} \tag{3.10}$$

where $H_{N,notch}(\omega)$ is the N-path notch transfer function, which is $1 - H_{N,BP}(\omega)$ [70]. Fig. 3.4 plots the simulated notch response using a Walsh code and compares with (3.10). Only the input spectrum at the specific PN code spectral components lies inside the notch while other orthogonal harmonics will be spread out of the notch. By comparing the response in Fig. 3.3 and Fig. 3.4 for the BPF and notch filter, the peaks of the bandpass response lies at different frequencies compared to the notches due to different used codes and code orthogonality.

3.1.5 PN Codes for RF CD Signal Processing

Different families of PN codes can be proposed for the RF code-domain RX [29–31]. An ideal PN code for CDMA systems should have the following values for its

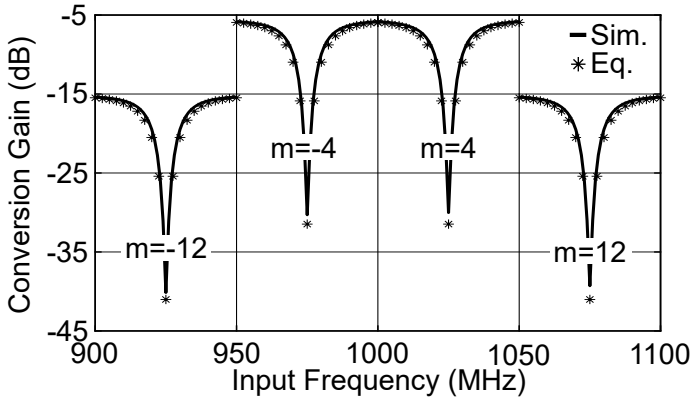


Figure 3.4: Conversion gain of PN-modulated notch N-path filter using Walsh 5.

normalized auto-correlation $R_{xx}[i] = \frac{1}{M}\sum_{k=0}^{M-1} x[k]x[k+i] = \delta[i]$ and cross-correlation $R_{xy}[i] = \frac{1}{M}\sum_{k=0}^{M-1} x[k]y[k+i] = 0, \forall x \neq y$. A single peak for the auto-correlation allows synchronization while the cross-correlation with other PN codes is zero for any time lag for rejection as shown in Fig. 3.5. Although no PN code has these ideal properties, some PN codes can approximate these ideal characteristics.

M-sequence

R_{xx} is either 1 or -1/M which guides synchronization. However, R_{xy} may take large values which degrades their use for TX rejection.

Gold Codes

Generated by XORing two pairs of preferred m-sequences of the same length. The resulting sequence has an R_{xy} that is bounded to 3 values making it better for rejection compared to m-sequence at the expense of worse R_{xx}.

Walsh Codes

An M-length Walsh code is constructed with

$$W_2 = \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix}; W_{2^k} = \begin{bmatrix} W_{2^{k-1}} & W_{2^{k-1}} \\ W_{2^{k-1}} & -W_{2^{k-1}} \end{bmatrix}, \tag{3.11}$$

where $k = \log_2(M)$. Walsh codes have zero R_{xy} making them ideal for rejection. However, R_{xx} has many peaks due to their periodic properties resulting in bad synchronization and spreading efficiency (Walsh codes spread most of the signal at a small number of specific harmonics).

A practical system uses a combination of different codes for multi-user operation. For example, CDMA uses long PN codes, short PN codes, and Walsh codes as described in [32].

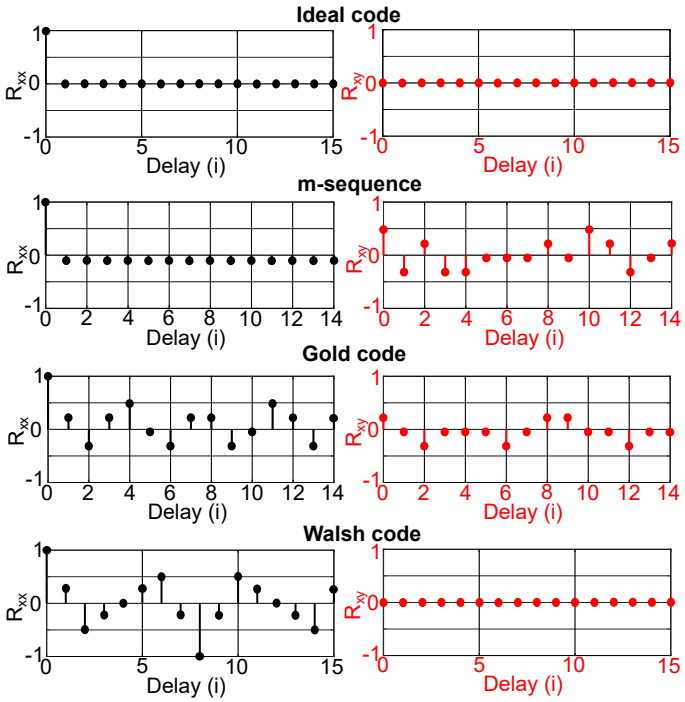


Figure 3.5: Auto-correlation (black) and cross-correlation (red) properties of ideal codes, m-sequence, Gold codes, and Walsh codes.

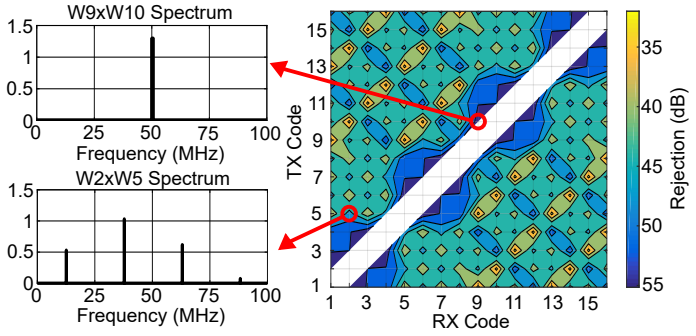


Figure 3.6: Simulated rejection for different Walsh code pairs.

3.1.6 *RC*-limited Rejection in RF Correlators

As described in the previous section, Walsh codes have ideal rejection properties due to their orthogonality. However, *RC*-limited integration in N-path filters limits the actual rejection. Fig. 3.6 shows the simulated rejection for combinations of 16-length Walsh codes and how the rejection changes based on inter-code interference (ICI).

The ICI is caused by residual correlation energy that remains during the next code correlation and can be explained by inspecting the time-domain waveforms of the product of different Walsh code pairs. Without loss of generality, we consider the following code sequences [1, 1, -1, -1, -1, -1, 1, 1] and [1, -1, -1, 1, 1, -1, -1, 1] which represent the product of different 8-length Walsh code pairs. Both sequences are balanced sequences with no DC content.[1]

Passing these two sequences to an RC filter results in the following output waveforms as shown in Fig. 3.7.[2] A careful observation of the output over one symbol period reveals that it has DC content compared to the ideal integrator output with no DC. This can be attributed to the exponential charging/discharging of the RC filter and dependence on the initial capacitor voltage value. This behavior is more detrimental with amplitude-

[1]These sequences are the product of the following code pairs (2,8) and (2,3). Any Walsh code with any length can be used and the used codes were just selected as a general illustration.

[2]The problem is analyzed in BB for simplicity but the same can be applied at RF frequencies.

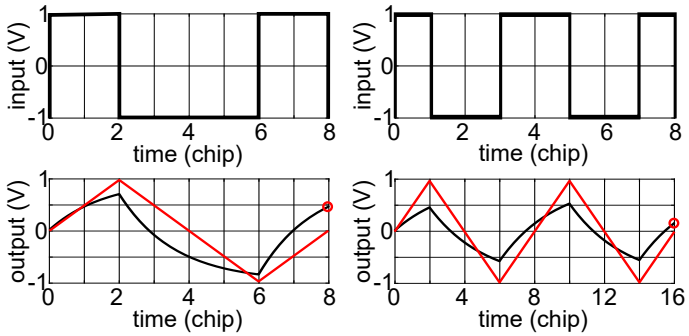


Figure 3.7: Response of an RC filter (black) and ideal integrator (red) to different Walsh codes. Final value of RC filtered signal is highlighted as a non-zero leading to DC content and rejection limitations. Faster transitions reduce this effect as shown for the right code.

modulated symbols as the capacitor voltage at the end of each symbol will depend on the transmitted symbol amplitude causing ISI.

RC limited correlators degrade the rejection compared to ideal correlators. But, this effect is less profound with some codes compared to others. For example, the 2^{nd} sequence has more transitions compared to the 1^{st} one resulting in smaller DC content. This can be explained by noting that $e^{-t/\tau} \approx 1 - t/\tau$ when τ is large relative to the transition time causing the non-ideal integrator to approach the ideal linear behavior.

Consequently, selecting optimum code pairs reduces ICI as shown in Fig. 3.6 for the (9,10) code pair compared to the (2,5) code pair. The product of the (9,10) code pair produces a square wave with a period equals to double the chip rate (waveform with the highest frequency content). This decreases the charging/discharging time relative to the RC time constant of the filter and the RC filter response approaches that of an ideal integrator. The map in Fig. 3.6 indicates that 16-length codes can achieve rejection between 35 and 55 dB and shows the existence of 8 optimum code pairs. The number of optimum code pairs can be increased by using longer length codes.

3.1.7 Linearity Improvement in CD Receivers

The PN-modulated N-path filter response can be modeled as a nonlinear system consisting of PN multiplication and a weakly nonlinear filter,

$$V_{out,BP}(t) = \sum_{k=1}^{3} \alpha_k [v_{in}(t) \times PN_f(t)]^k, \tag{3.12}$$

assuming that the differential filter cancels the second-order contribution and noting that $PN^3 = PN$,

$$V_{out,BP}(t) = PN_f(t) \sum_{k=1}^{2} \alpha_{2k-1} v_{in}(t)^{2k-1}. \tag{3.13}$$

For a 2-tone PN-coded input to the PN-modulated filter, i.e. $V_{in}(t) = PN_{in} \times [cos(\omega_1 t) + cos(\omega_2 t)]$, the third-order intermodulation (IM3) tone at the output can be written as $V_{IM3}(t) = \frac{3}{4}\alpha_3 PN_{in} PN_f cos((2\omega_1 - \omega_2)t)$.

When the input PN code is matched to the filter PN code, i.e. $PN_{in} = PN_f$, the IIP3 is the same as that of an unmodulated N-path filter $IIP3_{N-path} = \sqrt{\frac{4}{3}|\frac{\alpha_1}{\alpha_3}|}$. Alternatively, when the input and filter codes are different, i.e. $PN_{in} \neq PN_f$, the IM3 tones are spread OOB by the product of the orthogonal codes relaxing the linearity requirements of the system. For a random M-length PN code, the IIP3 is $IIP3_{PN} = 10log_{10}(M) + IIP3_{N-Path}$ which indicates improvement by the PG of the PN code.

3.1.8 Harmonic Folding in CD N-path filters

N-path filters suffer from harmonic folding when blockers located at $(N \pm 1)f_{LO}$ fold back to the RF band around f_{LO} due to the harmonic contents of the $1/N$ duty cycle clock pulses. The attenuation for the strongest harmonic folding term is approximated as $20log_{10}(N-1)$ [34, 71]. Harmonic folding can be reduced by increasing N of the filter at the expense of power consumption [72] or by adding a low-pass pre-filter deteriorating

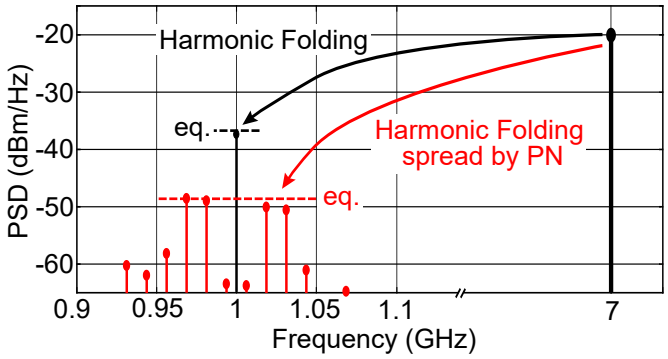


Figure 3.8: Simulated harmonic folding improvement with PN codes.

the IL and NF.

The PN-modulated N-path relaxes the problem of harmonic folding as any blocker at $(N \pm 1)f_{LO}$ that is down-converted to f_{LO} will be spread out of the desired RF band by the PN code of the code-domain front-end. For an M-length PN code, the harmonic folding attenuation is increased by the PG of the PN codes to $20log_{10}(N-1)+10log_{10}(M)$. Fig. 3.8 shows the simulated spectrum of an 8-path filter for an input at 7 GHz which is folded back to 1 GHz. Code-domain signal processing increased the attenuation for harmonic folding content from 17.4 dB to 28.6 dB using a 16-length PN code.

3.1.9 LO Leakage in CD N-path filters

While LO leakage is a challenge in traditional N-path filters, PN-modulated N-path filters reduce the LO leakage power as the N-path switches are modulated by PN codes which spread the LO leakage out of the signal BW [73]. Measurements of LO leakage with and without PN codes are discussed in Section 3.3.

3.1.10 SFDR of the CD RX

The previous sections have explained the trade-offs between code length, IL, interference tolerance, SI rejection, and linearity for CD receivers. SFDR captures these trade-

offs and presents a measure for comparing the proposed approach. We have demonstrated that blocker tolerance and linearity improves with the PG at the expense of IL and NF. The SFDR of an RX applying code-domain signal processing is expressed as

$$SFDR_{CD} = SFDR_{RX} + 10log_{10}(\frac{1}{|R_{in,CP}(0)|}) + \frac{Notch\ Rej.}{1 - 10log_{10}(\frac{1}{|R_{in,CN}(0)|})}, \tag{3.14}$$

where $SFDR_{RX}$ is the SFDR of the RX after the CD front-end. The SFDR depends on the code correlation with both the CPF represented by the $R_{in,CP}$ term and the CNF represented by the $R_{in,CN}$ term. The 1^{st} term represents the PG of the CPF, and the 2^{nd} term represents the notch rejection which increases SFDR for inputs matched to the notch filter while slightly increasing IL for other unmatched inputs. The PG increases more quickly than the IL as demonstrated in Fig. 2.8 and, the net benefit is an SFDR improvement.

3.2 Code-Domain RX Implementation

The proposed RX consists of two filters: a CNF followed by a CPF. The code-domain filters are followed by an LNA with N-path feedback for amplification and frequency down-conversion. Finally, the N-path feedback capacitors are sampled by harmonic recombination g_m cells to generate I and Q baseband (BB) outputs. The chip also includes frequency dividers to generate the non-overlapping clock pulses for the N-path filters and digital logic for PN code generation. The chip schematic is shown in Fig. 3.9 and this section describes the design of the RX different blocks.

3.2.1 Code-Notch and Code-Pass Filters Design

The CNF and CPF are 8-path filters to decrease the IL of the RX front-end. The switches are 50 μm width thin-oxide NMOS transistors (L = 40 nm) for low power consumption. The switch resistance is simulated to be 5 Ω. The N-path filter switches are modulated by the PN codes to perform modulation as well as filtering reducing the number of cascaded switches and IL of the filters. The upper pair of switches is enabled when the PN code is 1 and the RF signal passes as it is, while the lower pair is enabled when the PN code is 0 reversing the phase of the input RF signal. The schematic of the switch and the accompanying digital control gates are shown in the left of Fig. 3.9.

The notch filter capacitance is 37.5 pF to achieve more than 15 dB of rejection across 3 MHz BW and the BPF capacitance is 20 pF for 22 MHz BW. Consequently, the notch BW was designed to be much smaller than the bandpass BW to avoid degrading the IL of the desired RX signal. Both capacitances are implemented using high-quality factor MIM capacitors with minimum back-plate parasitic capacitance which is a major advantage of the used SOI process.

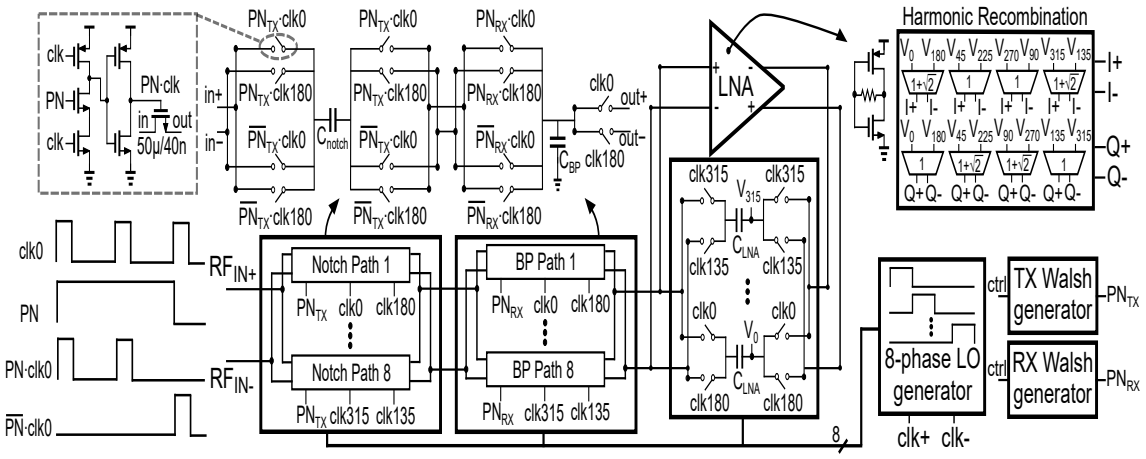


Figure 3.9: Schematic of the CD RX.

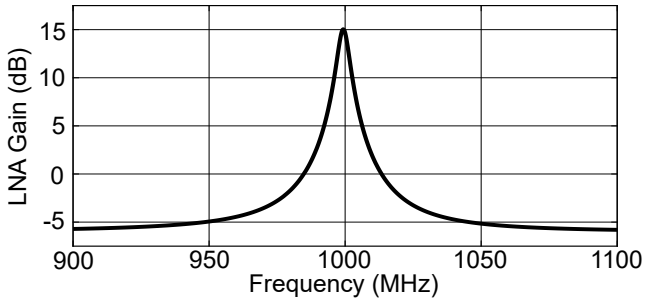


Figure 3.10: Simulated gain of the LNA with N-path feedback.

3.2.2 LNA and Baseband Amplifier Design

The filters are loaded by an LNA with N-path feedback [63]. The LNA is designed as a pseudo-differential self-biased gain stage. The NMOS transistor has a W/L of 50 μm / 56 nm while the PMOS transistor has a W/L of 72 μm / 56 nm. The LNA 8-path feedback switches are 25 μm width thin-oxide NMOS transistors (L = 40 nm). The LNA switches are smaller in size compared to the front-end N-path filters as the LNA gain allows achieving smaller equivalent switch resistance with larger switches due to feedback reducing the RX power consumption. Increasing the value of the feedback resistor of the LNA increases its input impedance which decreases the IL of the front-end filters leading to a better NF at the expense of degrading the LNA linearity. The feedback resistor was designed to be 3 KΩ as a tradeoff between NF and linearity.

The LNA characteristics at 1 GHz is simulated in Fig. 3.10. The LNA with N-path feedback has 15 dB of gain, a BW of 5 MHz using 20 pF MIM capacitors. It offers 20 dB of rejection for OOB signals while consuming 13.5 mA at 1-V supply.

Finally, the LNA N-path capacitors are sampled by weighted harmonic recombination g_m cells to get the I and Q BB outputs. Differential PMOS g_m cells convert the N-path capacitor voltages to currents which are summed at a shared NMOS differential load. The weights for the g_m cells are the same as described in [63]. The BB section uses thick oxide devices (L = 472 nm) at 1.8-V supply to increase linearity and decrease flicker

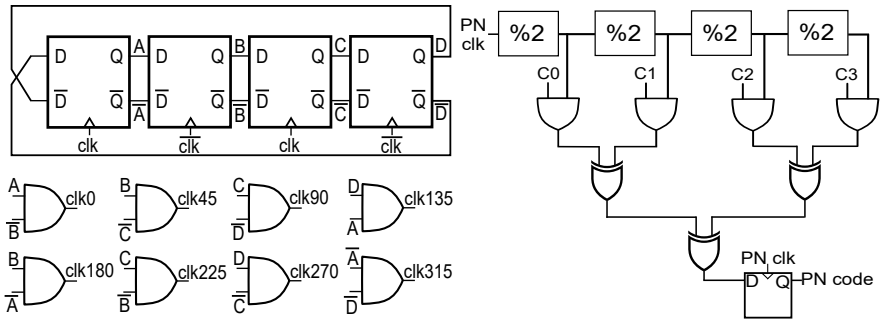


Figure 3.11: Schematic of the clock divider and 16-length Walsh code generator.

noise. The BB section has a gain of 30 dB and consumes 4.9 mA at 1.8-V supply.

3.2.3 Clock and PN Generation

The RX contains a divide-by-4 frequency divider followed by AND gates to generate the 12.5% duty cycle pulses for the N-path switches. The schematic of the clock generation circuit is shown in Fig. 3.11. The divider uses differential flip-flops for fast, low-power operation as described in [63]. The dividers have a phase noise of -160.5 dBc/Hz at 1 MHz offset at 1 GHz output frequency and consumes 4.6 mA at 1-V supply.

The RX also includes logic gates for 16-length Walsh PN code generation [29] as shown in Fig. 3.11. All the logic gates are static CMOS for low power consumption. Simulations indicate that the PN generation logic consumes 0.1 mA at 100 MChips/sec from a 1-V supply and was tested to operate till a chip rate of 250 MChips/sec. Besides the advantage of a fully integrated chip, having on-chip PN generation demonstrates the feasibility of synchronizing the on-chip generated PN codes with the modulated RF signal from the arbitrary waveform generator (AWG). Details about how synchronization was performed are given in the measurements section.

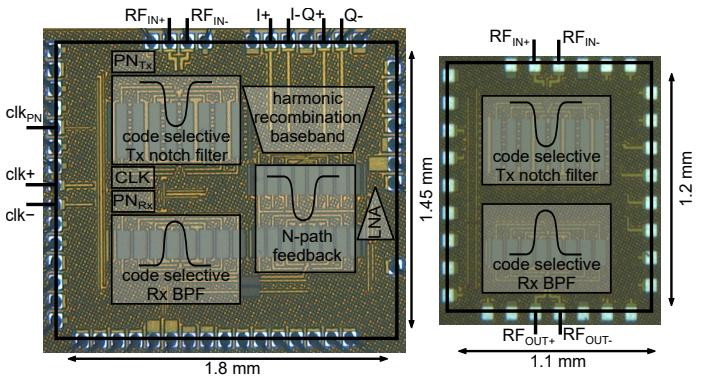


Figure 3.12: Chip micrograph of the code-domain RX (left) and filters breakout (right) in 45-nm CMOS SOI.

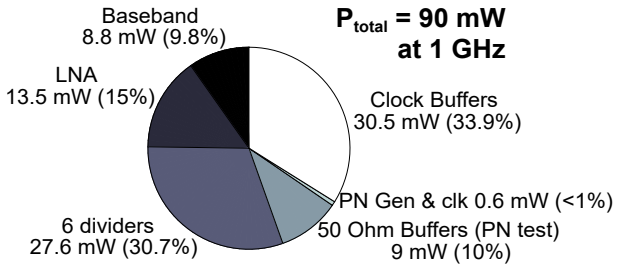


Figure 3.13: Power distribution among different RX blocks at 1 GHz.

3.3 Code-Domain RX Measurement Results

The code-domain RX is implemented in a 45-nm CMOS SOI process and the chip micrograph is shown in Fig. 3.12. The RX chip occupies an area of 2.6 mm^2 while a standalone filters breakout occupies an area of 1.3 mm^2. The chip is tested nominally at 1 GHz and the DC power consumption is 90 mW of which 40 mW are consumed in the code-domain filters. The power consumption among the different blocks of the RX at 1 GHz is shown in Fig. 3.13 and increases from 50 mW at 0.25 GHz to 103 mW at 1.25 GHz.

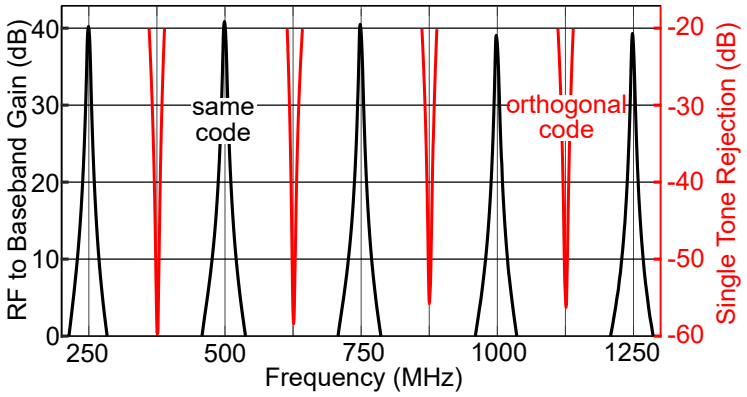


Figure 3.14: Conversion gain and rejection as a function of RF frequency.

3.3.1 Small Signal Measurements

The RX tunes from 0.25 GHz to 1.25 GHz. The conversion gain and single tone rejection are plotted in Fig. 3.14. The conversion gain was measured to characterize the CP mode by applying an unmodulated single tone while bypassing the notch filter. The RX has a gain of 39 dB at 1 GHz. The rejection was measured in CN mode by applying an unmodulated single tone while the notch filter has no code applied and the BPF has a PN code applied (Walsh 1) to spread the rejected signal OOB. The rejection is calculated as the integrated output power across the spread BW in the CN mode relative to the output power in the CP mode. The peak single tone rejection at 1 GHz is 55 dB and is more than 30 dB across 15 MHz BW.

The S-parameters of the code-domain filters were measured from a standalone break-out. The measured $S21$ in CP and CN modes across the tuning range are shown in Fig. 3.15. The IL of the cascaded filters is 5 dB at 500 MHz and increases to 6.5 dB at 1 GHz due to increased rise/fall time in the clock pulses. At 500 MHz, Fig. 3.16 plots the simulated (dashed) and measured (solid) $S21$ and $S11$ in CP and CN modes at 250 Mchip/sec PN rate. The BW of filters in CP mode is 22 MHz at 50 Mchip/sec PN rate and increases to 64 MHz at 250 Mchip/sec. The notch depth is 29.4 dB and more than

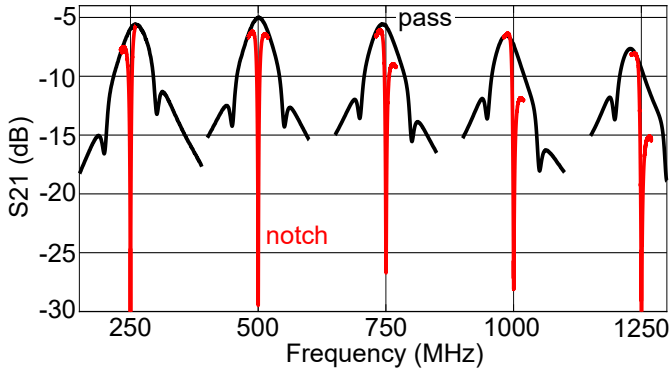


Figure 3.15: Measured $S21$ in CP and CN modes across the tuning range.

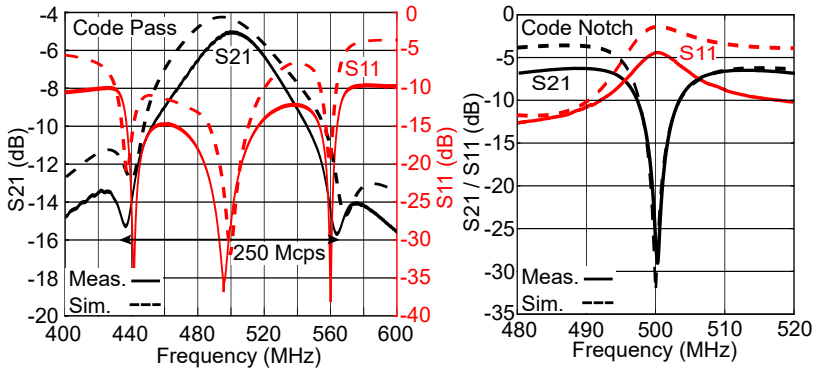


Figure 3.16: Measured (solid) and simulated (dashed) $S21$ and $S11$ in CP and CN modes at 500 MHz.

15 dB for a 3 MHz BW.

3.3.2 Linearity and NF Measurements

The linearity was characterized at RF and BB outputs without applying PN codes for a fair comparison with other receivers. In CP mode, the linearity was measured by applying two tones at f_{in}-Δf and f_{in}-2×Δf such that the IM3 tone would be at f_{in} which was 998 MHz and the offset frequency Δf was varied for in-band (IB) and OOB frequencies. The IIP3 of the filters is 3 dBm at 0.5 MHz offset frequency and increases to 13.6 dBm at 80 MHz offset frequency. While the entire RX IIP3 at 39 dB of gain is -22.1 dBm at 0.5 MHz offset and increases to 9.1 dBm at 80 MHz offset. The IIP3

measurements in CP mode are summarized in Fig 3.17.

Similarly, the IIP3 was measured in CN mode by applying two tones lying inside the notch filter at 999 MHz and 1000.5 MHz and observing the IM3 tone at 2 MHz at BB output. The IIP3 in CN mode is 19.1 dBm as shown in Fig. 3.18.

The 1-dB compression point (P1dB) of the RX is -6.7 dBm in CP mode as shown in Fig. 3.19. Also, the blocker 1-dB compression point (B1dB) for an IB orthogonal blocker was measured by applying a blocker modulated by the notch filter code while simultaneously receiving a signal modulated by the pass filter code and increasing the blocker power till the desired signal compresses by 1-dB. The B1dB compression point of the RX is -6.1 dBm as shown in Fig. 3.19.

Measurements indicate no difference in the compression point between the CP and CN modes due to the power handling of the switches of the CN filter. While PN modulation improves the RX linearity, it does not affect compression. While IIP3 is characterized under small-signal conditions, compression is determined by the large-signal voltage swing at the switches which is not affected by PN modulation as it is a constant envelop modulation. The compression point of the code-domain front-end can be increased to exceed 10 dBm by using thick oxide switches as in [47, 64] at the expense of power consumption. Since the RX is usually proceeded by a circulator or an EBD as an antenna

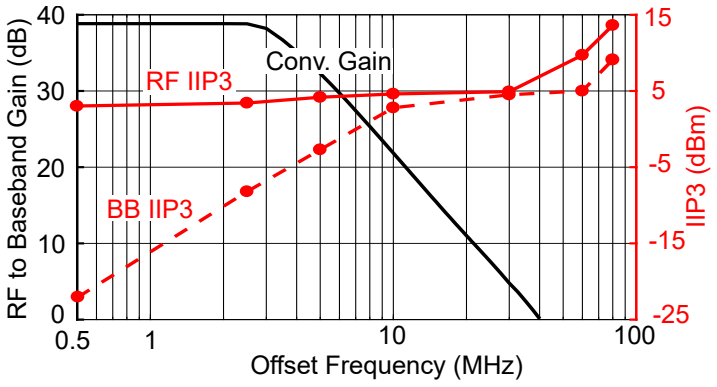


Figure 3.17: Measured conversion gain and IIP3 in CP mode.

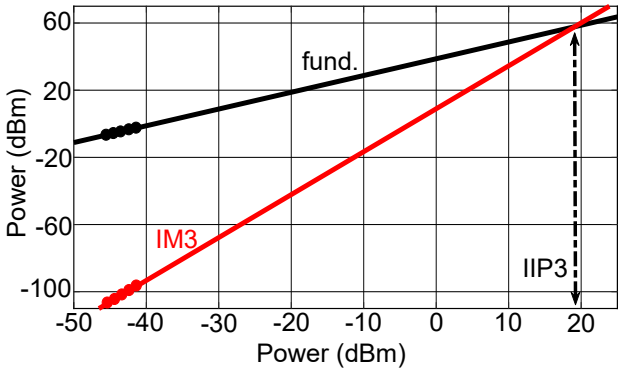


Figure 3.18: Measured IIP3 at BB in CN mode.

interface in FD applications, the power handling of the system is determined by the power handling of these blocks which can be more than 25 dBm [19,24] while offering more than 35 dB of isolation. A co-design of the antenna interface and the code-domain filters would determine the optimum power handling of the code-domain filters without a significant increase in power consumption.

The NF of both the standalone filters and the entire RX were measured at 500 MHz in Fig. 3.20. The filters have an NF of 5 dB while the entire RX has an NF of 9.35 dB.

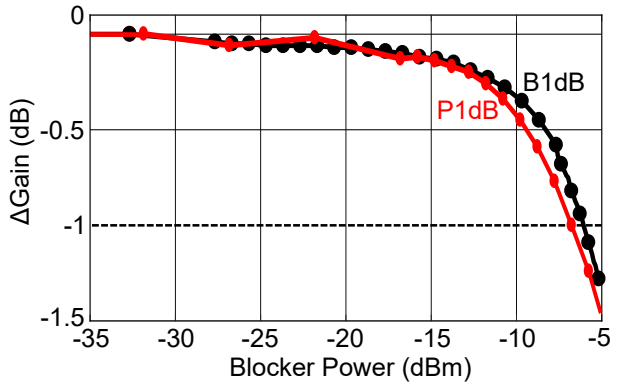


Figure 3.19: Measured 1-dB and IB blocker 1-dB compression points of the CD RX.

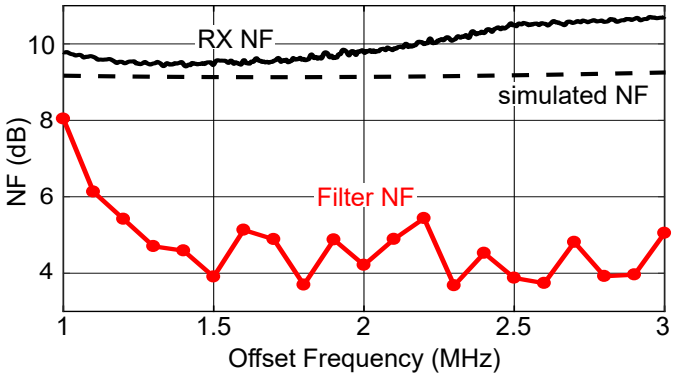


Figure 3.20: Measured NF at 0.5 GHz (simulation in dashed line).

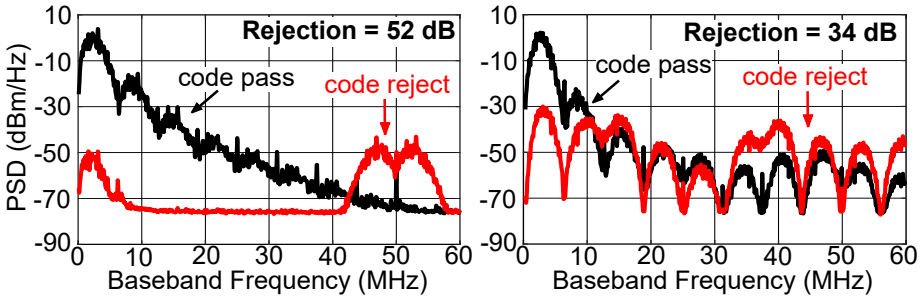


Figure 3.21: Measured rejection for different 16-length Walsh code pairs.

3.3.3 Rejection Measurements

The rejection was measured by applying an RF carrier modulated by a 6.25 MS/sec BPSK random data modulated by a 100 Mchip/sec PN Walsh code to the RX through an AWG. The output power is measured for both cases where the RX CP and CN filters are modulated by the combinations of matching and orthogonal PN codes. The RX achieves 52 dB rejection over the signal BW for a 6.25 MS/sec signal modulated by a 100 Mchip/sec Walsh PN code at 1 GHz RF frequency as shown in Fig. 3.21. As discussed in Section 3.2, the rejection depends on the cross-correlation between the pair of TX and RX codes. The measured rejection ranges from 52 dB for the (9,10) code pair to 34 dB for the (2,5) code pair across the signal BW as shown in Fig. 3.21 which agrees with the simulated behavior discussed in Fig. 3.6.

Synchronization was achieved using an external programmable coaxial delay line to synchronize the RF modulated input to the on-chip generated Walsh codes. The resolution of the programmable delay is 2.5 ns which is used as coarse tuning while sub-ns fine-tuning is done through the AWG. A similar approach can be implemented on-chip by sampling the PN clock by a shift register clocked with the N-path frequency dividers clock and selecting the required delayed sampled PN clock with a multiplexer.

Fig. 3.22 shows the measured synchronization profile indicating peak auto-correlation at the correct chip delay. Generally, the proposed RX does not require the CP filter to be synchronized with the CN filter. However, some codes like Walsh codes require that for improved rejection.

3.3.4 Harmonic Folding and LO Leakage Measurements

Harmonic folding was measured by tuning the LO to 225 MHz such that the first folding content is at 1.575 GHz. The lowest center frequency was selected so that the folding frequency is within the balun bandwidth. A modulated input was applied at 1.575 GHz and the output at 225 MHz was observed for both cases where the filter had no PN code and when it was modulated by a 16-length Walsh code. The harmonic folding is spread out of the signal BW by the PN code and is improved by 38.4 dB across the

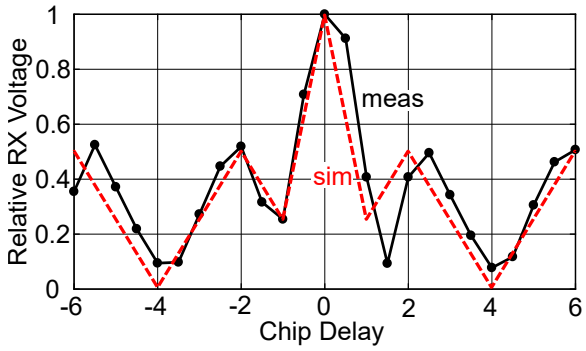


Figure 3.22: Measured and simulated synchronization profile using Walsh code.

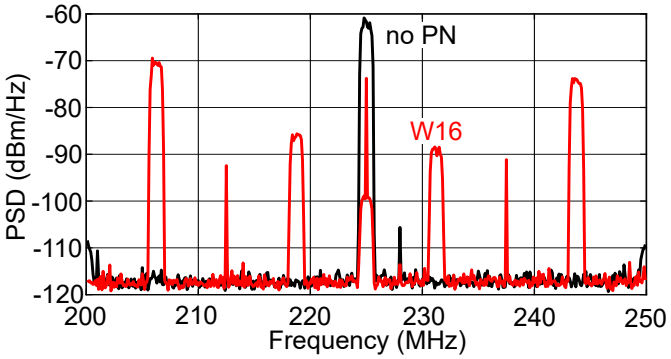


Figure 3.23: Measured harmonic folding from 1.575 GHz to 225 MHz with and without PN codes.

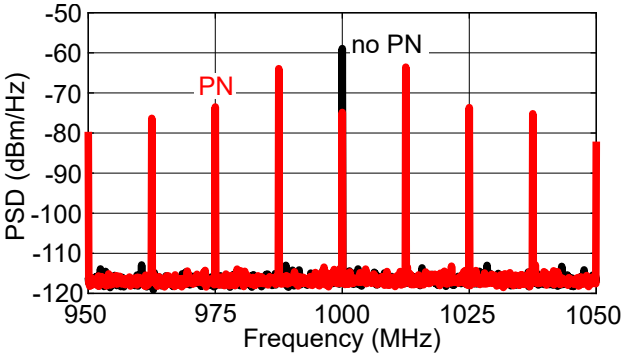


Figure 3.24: Measured LO leakage with and without PN codes.

signal BW as shown in Fig. 3.23.

Similarly, Fig. 3.24 compares the measured LO leakage at the output of the notch filter with and without PN codes. LO leakage is improved from -59 dBm to -75 dBm and is spread OOB and thus can be filtered in BB when PN codes are used.

3.3.5 Over-the-air STAR Demonstration

The prototype RFIC was tested in an over-the-air (OTA) STAR link with 2 simultaneous TX and RX (2x2) at 900 MHz. The OTA demonstration is shown in Fig. 3.25. The code-domain filters were added at the RF interface of a universal software radio peripherals (USRP) [74] to demonstrate compatibility with legacy radios. Two ISM-band antennas (VERT900) [75] were used along with a CentricRF (CF1020) circulator [76].

Minicircuits amplifiers (ZKL-2R7) [77] were added after the TX of the USRPs to boost the output power and reduce the USRP internal leakage and Minicircuits modulators (ZMQ-1050) [78] were used to perform TX PN modulation.

Off-the-shelf modulators were used for TX modulation for simplicity and to demonstrate system feasibility. A practical system would use lower-loss, high-power TX modulators as those described in [68, 69]. These modulators use device stacking to handle up to 34 dBm of TX power with a minimal IL of 1.5 dB at 1 GHz and have a 46% fractional BW. Another viable approach would be using the modulators before a wideband PA achieving similar performance.

The measured isolation of the circulator was 11 dB at 900 MHz when loaded by the antennas as shown in Fig. 3.26 which limited the TX power from each USRP to 5 dBm so as not to exceed the B1-dB of the filters. The 5 dBm power level is sufficient for measuring over several meters between the USRPs. The TX power and, consequently, range between the two radios can be increased by using a higher isolation circulator. The measured RX power level at the input of the USRP was -40 dBm while the TX SI power at the input of the filters was -6 dBm as shown in Fig. 3.25.

In the 2x2 OTA link, one USRP was programmed to transmit a quadrature phase-shift keying (QPSK) signal modulated by a Walsh PN code after the PA while the other USRP was programmed to transmit quadrature amplitude modulation (16-QAM) data modulated by a different Walsh PN code. The data rate of the USRP was 0.5 Mbit/sec

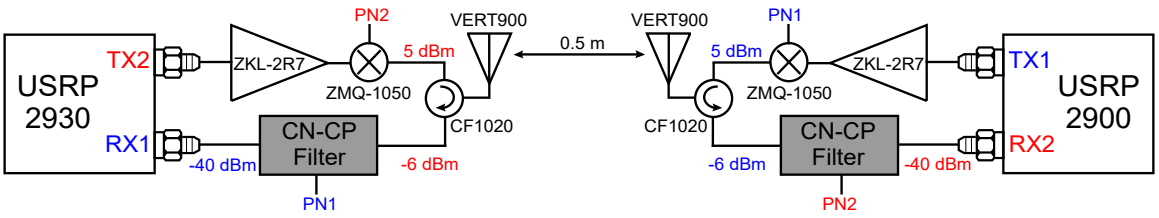


Figure 3.25: Wireless STAR demo setup.

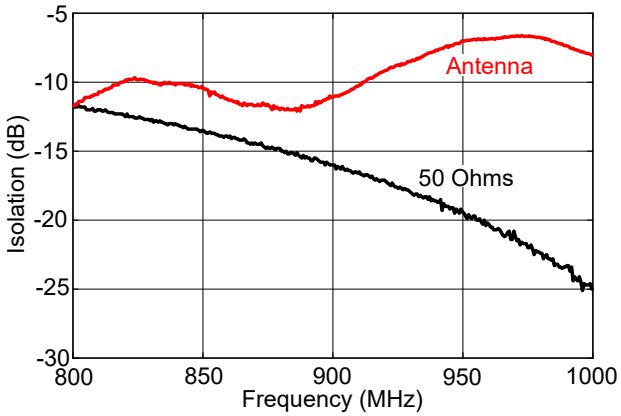


Figure 3.26: Measured circulator isolation with 50 Ω and antenna.

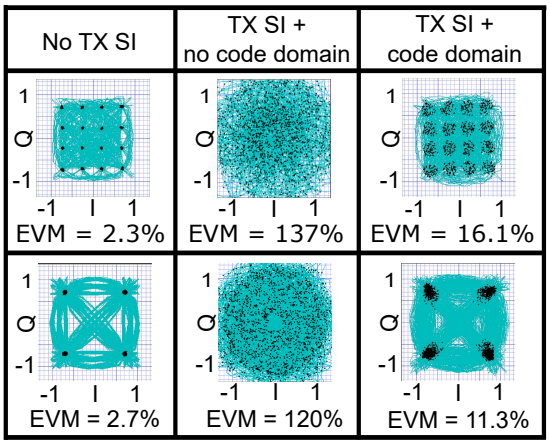


Figure 3.27: Measured EVM of the USRPs at different cases: no TX SI (left), TX SI without PN modulation (middle), and TX SI with PN modulation (right).

while the PN rate was 32 Mchip/sec. Fig. 3.27 plots the measured error vector magnitude (EVM) under different cases. The EVM in the absence of SI was around 2.5% (left plots). After enabling the TX and introducing SI without the code-domain signal processing, the EVM degrades significantly and the constellation can not be recovered (middle plots). Finally, the code-domain filters are enabled and the EVM can be recovered after turning both the TX SI and the PN code modulation on (right plots). The measured EVM was around 14% illustrating the ability to simultaneously transmit and receive signals at the same center frequency using the proposed RF CD signal processing.

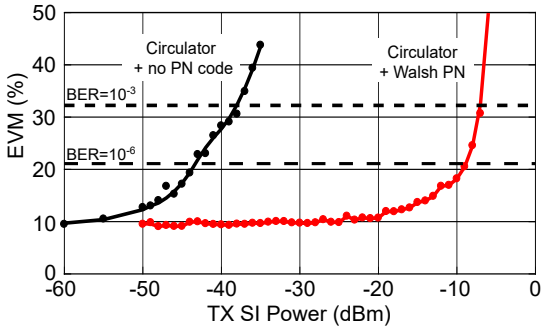


Figure 3.28: Measured EVM for different TX SI power level while receiving a -50 dBm QPSK RF signal.

Another demonstration was done where one of the USRPs was receiving a -50 dBm QPSK RF signal while sweeping the TX SI power and recording the EVM of the received signal. The same experiment was repeated: i) using the circulator isolation without PN modulation, ii) using the circulator, and spreading the TX SI with a Walsh code.

The TX SI power level where the EVM reached 21.1% and 32.5% corresponding to a bit error rate (BER) of 10^{-6} and 10^{-3} was measured for each of the previous cases [79]. The TX SI power was -43.3 dBm and -8.9 dBm for a BER of 10^{-6} and -38 dBm and -7.2 dBm for a BER of 10^{-3} for each of the previous cases as shown in Fig. 3.28. This illustrates the advantage of the proposed CD TX SI rejection technique in increasing the dynamic range of the RX by more than 34 dB.

Table 3.1 compares the performance of the CD filters front-end with passive high-order N-path filters implementations. Table 3.2 summarizes the performance of the proposed RF CD signal processing RX along with other FD RX implementations.

3.4 Conclusion

This chapter presented the design of a CD RX in a 45-nm CMOS SOI process. The CD RX uses DSSS techniques implemented in the RF domain to reject the TX SI while receiving the desired RX signal occupying the same bandwidth. The CD RX uses a

Table 3.1: CD filters performance summary and comparison with passive high-order N-path filters

	RFIC15 [51]	RFIC16 [66]	JSSC19 [67]	This Work
Architecture	N-path	N-path	N-path	Code-domain N-path
Technology	65 nm	65 nm	65 nm	45 nm
Supply	1.2-V	2.5-V	1.1/2.5-V	1-V
Frequency	0.6-0.85 GHz	0.5-1.1 GHz	0.8-1.1 GHz	0.25-1 GHz
IL	4.7-6.2 dB	4.6-5.2 dB	3.8-4.6 dB	5-6.5 dB
NF	8.6 dB	3.8-5.8 dB	5-8.6 dB	5-7.9 dB
Power	75 mW	15-25 mW	80-97 mW	13-40 mW
IB IIP3	7 dBm	19.2 dBm	25 dBm	3 dBm**
OOB IIP3	17.5 dBm	26 dBm	24 dBm	13.6 dBm
Area	1.2 mm^2*	0.8 mm^2	1.9 mm^2	1.3 mm^2

*without board inductors, **Without PN codes

cascade of CNF and CPF at the same center frequency to increase the achieved rejection. The RX is tunable from 0.25 GHz to 1.25 GHz and has a gain of 39 dB at 1 GHz while consuming 90 mW of which 40 mW are consumed in the front-end filters. The CD front-end achieves a peak rejection of 52 dB enabling FD operation as verified through measurements and OTA wireless demonstrations.

Table 3.2: CD FD RX performance summary and comparison

	JSSC 2018 [23]	ISSCC 2018 [59]	JSSC 2019 [80]	JSSC 2018 [60]	CICC 2018 [46]	This Work
Architecture	Circulator + Digital Cancellation	EBD + RF Cancellation	Frequency Hopping Spread Spectrum	Code-Domain*	EBD + Code-Domain*	Code-Domain
Technology	65 nm	40 nm	65 nm	65 nm	45 nm	45 nm
Supply	1.2/2.4-V	–	1-V	–	–	1/1.8-V
Frequency	0.61 - 0.975 GHz	1.6 - 1.9 GHz	0.4 - 1 GHz	0.3 - 1.4 GHz	1.1 - 2.5 GHz	0.25 - 1.25 GHz
RX Gain	28 dB	42 dB	–	35 dB	15 dB	39 dB
RX NF	8 dB	9.7 dB	6 dB**	3.4 - 4.9 dB	3.5 - 4.2 dB**	9.35 dB
RX Power	108 mW	106 mW	24 mW***	36 mW	50 mW***	90 mW
BW	20 MHz	40 MHz	0.5 MHz	1 MHz	1 MHz	6.25 MHz
RX IB IIP3	-18.4 dBm	-17 dBm	–	-26 dBm	–	-22 dBm
RX OOB IIP3	15.4 dBm (Δf = 500 MHz)	–	–	–	–	9 dBm (Δf = 80 MHz)
Rejection (Technique)	40 dB (Circulator) + 40 dB (Digital)	39 dB (EBD) + 31 dB (RF Canc.)	33 dB (FHSS Rej.)	38.5 dB (Code Rej.)	41 dB (EBD) + 20 dB (Code Rej.)	52 dB (Code Rej.)
Area	0.94 mm^2	4 mm^2%	3.1 mm^2	0.31 mm^2	1.4 mm^2%	2.6 mm^2

* off-chip code generation / modulation, ** measured at LNA input , *** does not contain a complete RX chain, %including PA

Chapter 4

An FD Rake Receiver for Improved SNR in Multipath Environments

RF CD signal processing was proposed in the previous chapters to increase the achieved TX SI rejection in FD transceivers. RF CD processing operates by allocating orthogonal PN codes to the TX and RX of an FD transceiver such that both occupy the same spread BW but the desired RX signal is correlated and the TX SI is rejected in the RF domain through PN code multiplication. This chapter extends CD architectures to deal with multipath propagation effects by introducing a 3-finger RF rake receiver that uses PN codes to increase the RX signal-to-noise (SNR) ratio while rejecting TX SI in FD transceivers as shown in Fig. 4.1.

This chapter expands on previous chapters to include more details about the effects of multipath propagation on FD transceivers, and how they affect RX signal integrity and TX SI rejection. It presents a 3-finger FD rake RX which exploits the multipath propagation properties of wireless channels and PN code orthogonality to gather signal from different multipaths increasing the RX SNR while avoiding the fading effects of

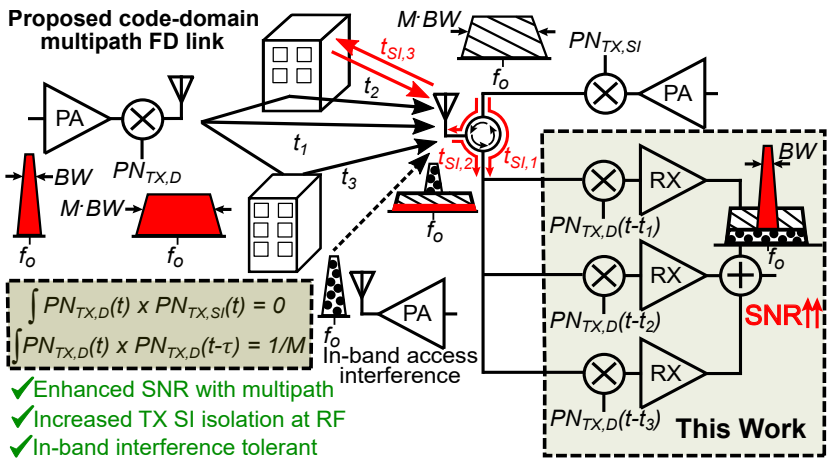
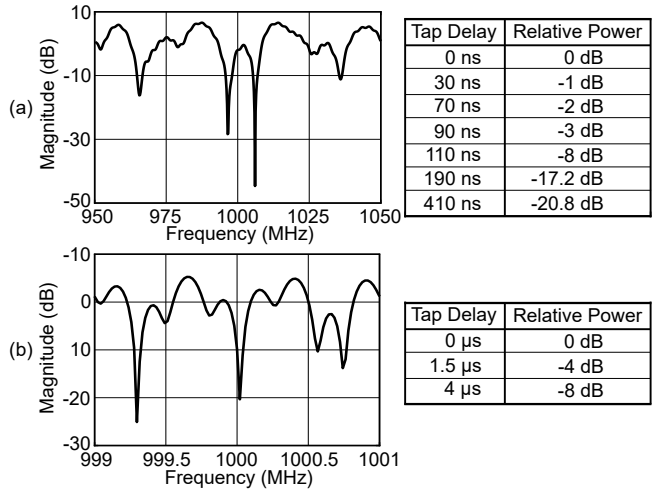


Figure 4.1: Proposed FD 3-finger rake RX in a multipath environment including RX and TX SI reflections.

multipath channels. The rake RX uses a shared LNA between the 3 rake fingers and a high-linearity BB section with 2^{nd} order filtering to improve the rejection with low power consumption.

The chapter discusses the various trade-offs encountered when designing a multi-finger RX architecture such as power consumption, rejection, and SNR improvement and how the proposed rake RX deals with these trade-offs for maximum SNR improvement at low power consumption. Section 4.1 analyzes the effects of multipath propagation including different indoor and outdoor channel models and how the proposed rake RX benefits from multipath effects. Implementation details of the proposed rake RX are given in Sections 4.2 and 4.3 including theoretical analysis of the 3-finger single LNA RF front-end, details about the high-linearity BB Rauch filter design along with design details of the clock generation, PN modulation, and synchronization circuitry. Section 4.4 presents the measurement results of the rake RX in a multipath channel model including TX SI rejection, SNR improvement, and various characteristics of the implemented chip prototype.



Tap Delay	Relative Power
0 ns	0 dB
30 ns	-1 dB
70 ns	-2 dB
90 ns	-3 dB
110 ns	-8 dB
190 ns	-17.2 dB
410 ns	-20.8 dB

Tap Delay	Relative Power
0 μs	0 dB
1.5 μs	-4 dB
4 μs	-8 dB

Figure 4.2: Frequency response of different multipath channels: a) EPA channel model, b) SUI-4 channel model.

4.1 Multipath Channel Impairments and Rake RX Concept

4.1.1 Multipath Channel Impairments

The wireless channel between the TX and RX is characterized by having multiple paths [31, 81] as shown in Fig. 4.1. The delay of these paths can be in the range of a few nanoseconds for indoor environments and a few microseconds for outdoor channels. Fig. 4.2 presents typical values for the relative path delays and gains in different multipath channels based on the extended pedestrian A model (EPA) [82] and the Stanford university interim model (SUI-4) [83]. The channel model can be expressed in terms of its impulse response:

$$h_{CH}(t) = \sum_{i=1}^{I} h_{CH,i} \times \delta(t - t_{CH,i}) \tag{4.1}$$

where $h_{CH,i}$ and $t_{CH,i}$ are the relative gain and delay of the i^{th} path given by Fig. 4.2.

The different multipaths could add destructively according to the phase difference among the paths resulting in deep notches in the frequency response of the channel

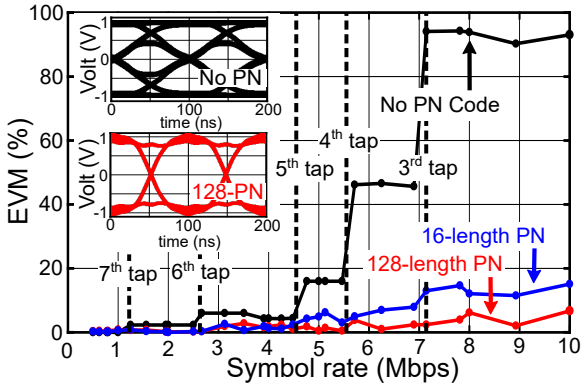


Figure 4.3: Simulated EVM versus symbol rate using the EPA channel model. Without PN codes, the EVM degrades as the symbol rate increases due to ISI as indicated by the closed eye diagram at 10 MSymbol/sec. PN codes help in recovering the EVM and eye opening. A 128-length PN code offers better performance compared to a 16-length PN code.

known as frequency selective fading as shown in Fig. 4.2. These notches limit the data rate to a few MHz when the path delays are in the ns range for the EPA channel and a few KHz for the SUI-4 channel with μs delays between the paths[1].

Also, the multiple propagation paths cause intersymbol interference (ISI) between the received symbols as the symbol period approaches the path delays degrading the SNR of the received signal. Fig. 4.3 shows the simulated EVM using the EPA channel model for increasing symbol rate. As the symbol rate increases, multiple symbols interfere with each other affecting the bit decision and degrading the EVM as indicated by the eye diagram at 10 Msymbol/sec which shows a closed eye in Fig. 4.3. The vertical lines in Fig. 4.3 indicate the symbol rate at which each path begins to affect the bit decision given by $1/(2 \times t_{CH,i})$. As multiple paths with higher relative power start to affect the bit decision, the EVM degrades more rapidly limiting the link data rate.

Another aspect of multipath detrimental effects that greatly impacts FD transceivers is the multiple paths between the TX SI and RX as shown in Fig. 4.1. Limited TX-

[1]Orthogonal frequency-division multiplexing (OFDM) can be used to avoid multipath propagation effects by using orthogonal subcarriers, but here we focus on single-carrier operation.

RX isolation at the antenna interface (circulator or EBD) causes some of the TX SI signal to leak to the RX after experiencing some delay. Also, mismatches at the antenna port cause some of the TX SI to be reflected to the RX with a different attenuation and delay compared to the first path. Meanwhile, the TX SI also reflects from nearby objects and re-appear at the RX with significant power. Cancelling the multiple TX SI versions with different delays and amplitudes with an RF canceller is a challenging design problem. The RF canceller could drastically overwhelm the power and area requirements of the FD transceiver to be able to cover such large delay spreads in the order of tens of nanoseconds.

4.1.2 Code-Modulated Rake RX

One of the unique properties of PN codes is that they only correlate signals that are tagged with the same PN code at the same delay. In other words, the correlation between different PN codes is ideally zero for any lag and the correlation between the same PN code is unity at only zero lag.

$$\frac{1}{M}\int_0^{M\cdot T_c} PN_i(t)\times PN_j(t-\tau)dt = \begin{cases} 0, & \forall\tau, i\neq j \\ 1, & \tau=0, i=j \end{cases} \tag{4.2}$$

This property is useful for an FD transceiver in two different aspects. First, it allows the transceiver to operate in multipath environments without being affected by multipath fading. Second, and more important for FD, it allows the rejection of the main TX SI as well as mismatch and environment generated TX SI reflections.

The received signal (RF_{in}) at the FD transceiver using (4.1) is expressed as:

$$\begin{aligned} RF_{in}(t) &= m_{RX}(t) * h_{CH}(t) + m_{SI}(t) * h_{SI}(t) \\ &= \sum_{i=1}^{I} h_{CH,i} \times m_{RX}(t - t_{CH,i}) + \sum_{j=1}^{J} h_{SI,j} \times m_{SI}(t - t_{SI,j}) \end{aligned} \tag{4.3}$$

where m_{RX} and m_{SI} are the RX and TX SI message signals; $h_{CH,i}$, $t_{CH,i}$ are the gain and delay of the different multipaths between the far TX and RX; $h_{SI,j}$, $t_{SI,j}$ are the gain and delay of the SI channel as illustrated in Fig. 4.1; and $*$ denotes the convolution operation. By spreading the desired RX signal and the TX SI using orthogonal PN codes PN_{RX} and $PN_{TX,SI}$ respectively, RF_{in} is given by:

$$\begin{aligned} RF_{in}(t) = &\sum_{i=1}^{I} h_{CH,i} \times RX(t - t_{CH,i}) \times PN_{RX}(t - t_{CH,i}) \\ &+ \sum_{j=1}^{J} h_{SI,j} \times TX_{SI}(t - t_{SI,j}) \times PN_{TX,SI}(t - t_{SI,j}) \end{aligned} \tag{4.4}$$

The input RF signal is multiplied by a synchronized version of PN_{RX} at the code-domain front-end. Thus, the output after code multiplication by the PN code of the main path $PN_{RX}(t - t_{CH,1})$ is given by:

$$RF_{out,1}(t) = PN_{RX}(t - t_{CH,1}) \times RF_{in}(t) \approx h_{CH,1} \times RX(t - t_{CH,1}) \tag{4.5}$$

Only the desired signal is correlated at the RX while rejecting multipath RX components reducing fading and ISI. Also, the TX SI and its delayed reflections are rejected by code orthogonality assuming ideal code properties as given by (4.2). However, when implemented, the rejection is limited by the used code properties and other circuit non-idealities resulting in residual multipath and TX SI components along with the correlated

signal as discussed in Section 4.3.

Fig. 4.3 shows the benefits of using RF code-domain signal processing where the EVM and eye diagram can still be recovered due to the multipath rejection of PN codes. It is worth mentioning that higher length codes offer better multipath tolerance and the system can possibly switch between different code length depending on the number of simultaneous users, wireless environment, and symbol rate requirements.

The CD front-end can also be configured in a rake RX architecture consisting of multiple fingers as shown in Fig. 4.1 where each finger correlates a specific multipath component [84]. By synchronizing the PN_{RX} code delay to the path delays, the output of each finger is given as:

$$RF_{out,i}(t) \approx h_{CH,i} \times RX(t - t_{CH,i}) \tag{4.6}$$

The SNR of the RX can be enhanced by combining the outputs of the different fingers after proper adjustments. The amount of SNR improvement depends on the wireless channel and number of rake fingers requiring a power-efficient RX architecture as discussed in Section 4.2.

4.2 Rake RX Architecture

4.2.1 Comparing Different Approaches

The rake RX requires combining the output of multiple fingers without much power consumption overhead. The problem is first analyzed in the frequency domain for better visualization where it is assumed that multiple frequency bands are to be combined as in carrier aggregation applications [53, 85]. Then, theoretical analysis is provided for CD operation.

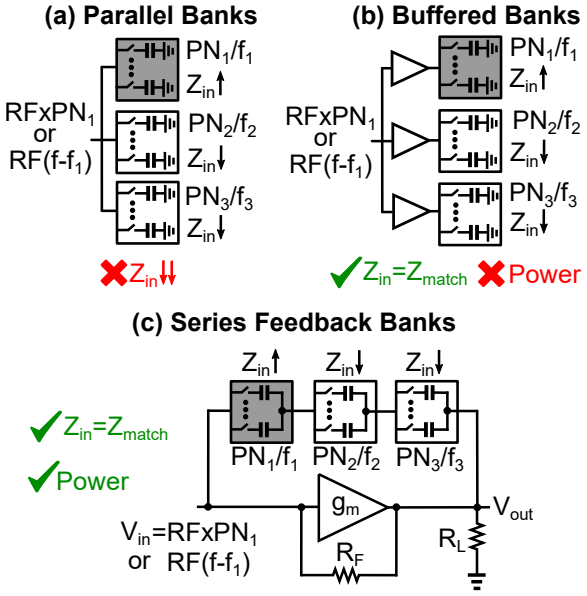


Figure 4.4: Rake RX architectures: a) Parallel banks suffer from the loading effect of non-matched inputs, b) Buffered banks solve the loading problem but with high power overhead, c) Series feedback banks solve the loading effect with low power consumption.

One way to combine different fingers is by using parallel N-path filters where each filter is configured to a specific frequency band (PN code in a code-modulated RX) as shown in Fig. 4.4. The input impedance (Z_{in}) of an N-path filter clocked at ω_o is given by [34]:

$$Z_{in}(\omega) = R_{sw} + R_{sh}//\frac{N}{\pi^2}sin^2(\frac{\pi}{N})Z_{BB}(\omega - \omega_o) \tag{4.7}$$

where R_{sw} is the switch resistance, N is the number of paths, Z_{BB} is the baseband capacitance impedance, and R_{sh} is the harmonic dependent shunt resistance accounting for N-path insertion loss as described in [56] and given by:

$$R_{sh} = (R_{sw} + R_s)\frac{N\gamma}{1 - N\gamma} \tag{4.8}$$

where γ is a factor depending on the number of paths of the N-path filter given by $\frac{N}{\pi^2}sin^2(\frac{\pi}{N})$ which equals $2/\pi^2$ for 4-path filters.

The input impedance is high around ω_o while it is nearly a short (R_{sw}) at frequencies far from ω_o indicating that for a multi-finger RX where each finger is matched to a certain frequency (PN code); other fingers short the input impedance in the parallel fingers architecture making it unsuitable for the rake RX. Adding a buffer at each filter solves this problem at the expense of higher power consumption.

Another approach is adding the multiple fingers in the feedback path of an LNA [60, 63]. Each filter provides a high impedance for inputs at its frequency band (matched PN code) and otherwise a short for out-of-band inputs (orthogonal PN code). The overall series feedback impedance is dominated by the high impedance such that the LNA still provides gain for desired inputs. Alternatively, the architecture can be viewed as an LNA with notch filters in the feedback path which notch specific frequencies (PN codes) such that the overall response with negative feedback is bandpass for inputs notched by the filters.

4.2.2 Rake RX with Series Feedback Fingers

The gain of the LNA with series feedback filters is analyzed using the admittance (Y) parameters of the configuration. The voltage gain (A_v) of a g_m stage with shunt-shunt feedback is given by:

$$A_v = \frac{-y_{21}}{y_{22} + y_L} \tag{4.9}$$

where y_{21}, y_{22} are the short circuit transfer admittance and short circuit output admittance of the circuit in Fig. 4.4c, and y_L is the load admittance given by $1/R_L$. The short circuit transfer admittance of the N-path feedback path ($y_{21,N_{FB}}$) in Fig. 4.4c is given by:

$$y_{21,N_{FB}} = \left.\frac{I_2}{V_1}\right|_{V_2=0} = \frac{-1}{\sum_{k=1}^{K} Z_{in,k}} \tag{4.10}$$

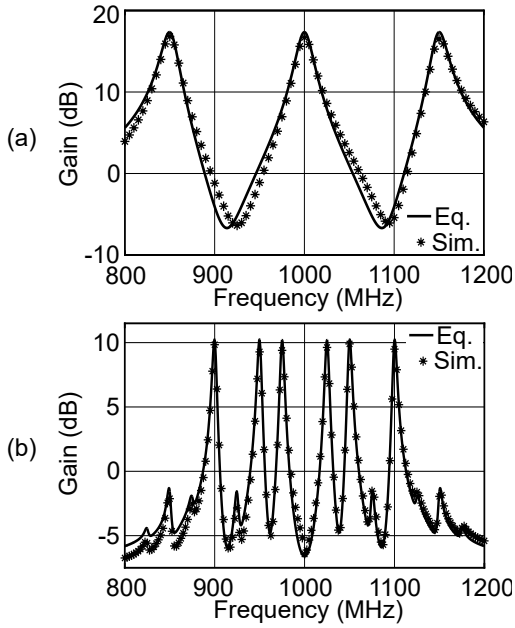


Figure 4.5: Gain of a g_m stage with 3-series feedback filters: a) Each finger has a different clock frequency, b) All fingers clocked with a 1 GHz clock modulated by a unique PN code for each finger. [$N = 4$, $g_m = 100$ mS, $R_{sw} = 5\ \Omega$, $R_L = 100\ \Omega$, $R_F = 1$ KΩ, $C = 40$ pF (top), and $C = 150$ pF (bottom)].

where Z_{in} is given by (4.7) and K is the number of fingers. similarly, $y_{22,N_{FB}} = -y_{21,N_{FB}}$.

The overall gain is thus given by:

$$A_v = \frac{-(y_{21,N_{FB}} + y_{21,R_F} + y_{21,g_m})}{(y_{22,N_{FB}} + y_{22,R_F} + y_{22,g_m}) + y_L} = \frac{-(\frac{-1}{\sum_{k=1}^{K} Z_{in,k}} - \frac{1}{R_F} + g_m)}{\frac{1}{\sum_{k=1}^{K} Z_{in,k}} + \frac{1}{R_F} + \frac{1}{R_L}} \tag{4.11}$$

For multiple filters in feedback where each filter is clocked at a different frequency, the gain becomes:

$$A_v = \frac{\frac{1}{\sum_{k=1}^{K} R_{sw} + R_{sh} // \frac{N}{\pi^2} sin^2(\frac{\pi}{N}) Z_{BB}(\omega - \omega_k)} + \frac{1}{R_F} - g_m}{\frac{1}{\sum_{k=1}^{K} R_{sw} + R_{sh} // \frac{N}{\pi^2} sin^2(\frac{\pi}{N}) Z_{BB}(\omega - \omega_k)} + \frac{1}{R_F} + \frac{1}{R_L}} \tag{4.12}$$

Fig. 4.5a compares the gain given by (4.12) with the simulated response for a g_m stage with three feedback filters centered at 0.85 GHz, 1 GHz, and 1.15 GHz. Gain only exists around the center frequencies of the feedback filters (ω_k).

Having analyzed the feedback fingers for multiple bands in the frequency domain, it is now easier to modify (4.12) for code-domain operation where all the feedback filters are clocked at the same clock frequency but with different PN code modulation on top of the N-path clock pulses.

Assuming an M-length PN code with a period $M \times T_{chip}$, the PN code is expressed in terms of its Fourier series expansion:

$$PN(t) = \sum_{m=-\infty}^{\infty} c_m e^{j\frac{2\pi m}{MT_{chip}}} = \sum_{m=-\infty}^{\infty} c_m e^{j\frac{m\omega_{chip}}{M}} \tag{4.13}$$

where c_m is the Fourier coefficient of the m^{th} harmonic of the PN code. The input impedance of an N-path filter modulated by PN codes is modified by the harmonic content of the PN code. The input impedance is shifted from being high around ω_o as indicated by (4.7) to be high at the harmonics of the PN code around ω_o [86].

$$Z_{in,PN}(\omega) = R_{sw} + \sum_{m=-\infty}^{\infty} R_{sh_m}//|c_m|^2 \frac{N}{\pi^2} sin^2(\frac{\pi}{N}) Z_{BB}(\omega - \omega_o - \frac{m\omega_{chip}}{M}) \tag{4.14}$$

where R_{sh_m} is modified by PN code modulation through changing γ in (4.8) to $\gamma_m = |c_m|^2\gamma$. Substituting the expression for the PN modulated input imedance $Z_{in,PN}$ in the gain expression in (4.11) gives the expression in (4.15); where K is the number of the feedback filters, $c_{k,m}$ is the Fourier coefficient of the m^{th} harmonic of the PN code modulating the k^{th} filter, and $R_{sh_{k,m}}$ is the corresponding shunt impedance.

$$A_{v_{PN}} = \frac{\frac{1}{\sum_{k=1}^{K}(R_{sw}+\sum_{m=-\infty}^{\infty} R_{sh_{k,m}}//|c_{k,m}|^2 \frac{N}{\pi^2} sin^2(\frac{\pi}{N}) Z_{BB}(\omega-\omega_o-\frac{m\omega_{chip}}{M}))} + \frac{1}{R_F} - g_m}{\frac{1}{\sum_{k=1}^{K}(R_{sw}+\sum_{m=-\infty}^{\infty} R_{sh_{k,m}}//|c_{k,m}|^2 \frac{N}{\pi^2} sin^2(\frac{\pi}{N}) Z_{BB}(\omega-\omega_o-\frac{m\omega_{chip}}{M}))} + \frac{1}{R_F} + \frac{1}{R_L}} \tag{4.15}$$

Fig. 4.5b compares the gain given by (4.15) with the simulated response for a g_m stage

with three feedback filters clocked at 1 GHz and each filter is modulated by a unique PN code on top of the 1 GHz clock pulses. Gain only exists around the harmonics of the PN code of the feedback filters. More details about how PN modulation was performed on top of the N-path switches are given in Section 4.3. It is worth mentioning that the PN modulated switches of the N-path filters de-spread the input signal matched to the modulating PN code and rejects orthogonal coded inputs (spread OOB) and the down-converted correlated signal is available at the capacitors of each feedback filter.

4.2.3 Effect of Number of Fingers

The choice of the number of rake RX fingers entails a tradeoff between SNR improvement and power consumption. Multipath components vary in signal power depending on the channel model affecting the overall SNR improvement. Fig. 4.6 shows the effect of the number of rake fingers on SNR using the EPA channel model (Fig. 4.2a). Fig. 4.6a indicates that for a 1-finger RX, the output SNR is greater than the input SNR by the processing gain of the PN code ($PG = 10 \times log_{10}M$) allowing the detection of signals below the environment noise floor due to orthogonality between noise and PN codes. The desired signal is correlated and de-spread while the noise remains spread across the spreading BW. Adding more fingers further improves the SNR beyond the PG by the multipath gain.

The amount of multipath gain depends on both the number of fingers and the input SNR level. Fig. 4.6b shows the effect of the number of fingers at various input SNR levels. At high input SNR, the output SNR improves by 5.5 dB, 8.6 dB, and 10.6 dB for 2, 3, and 4 fingers respectively. As the input SNR decreases, the amount of SNR improvement diminishes. For instance, the output SNR improves by only 2.3 dB, 3.8 dB, and 4.1 dB for 2, 3, and 4 fingers respectively at low input SNR (-10 dB) compared

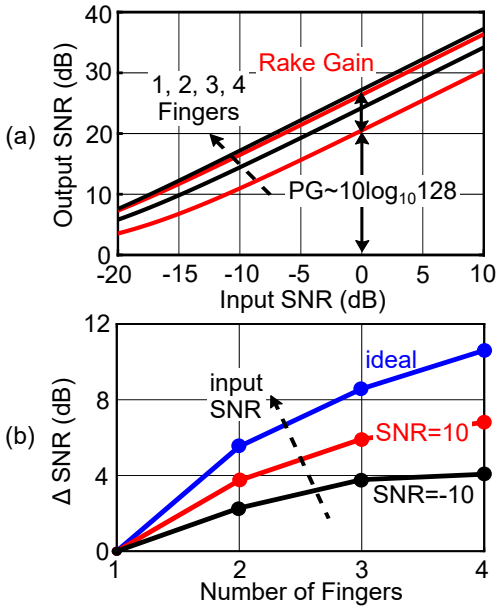


Figure 4.6: Effect of number of rake fingers on SNR: a) output SNR versus input SNR for increasing number of fingers, b) SNR improvement at varying input SNR for different number of fingers.

to 3.7 dB, 5.9 dB, and 6.8 dB at moderate input SNR (10 dB) for the same number of fingers.

The number of fingers also affects the OOB rejection of the N-path filters as the rejection of N-path filters is limited by the switch resistance (R_{sw}). Adding more fingers in series effectively increases R_{sw} linearly with the number of fingers. Fig. 4.7 demonstrates the effect of increasing the number of feedback fingers (K) on the rejection profile. The

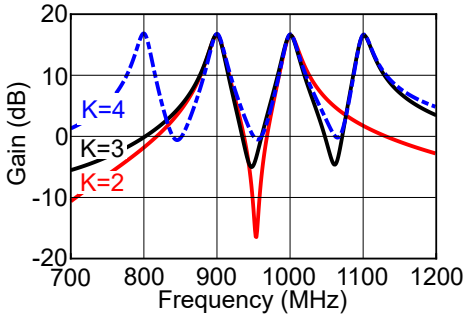


Figure 4.7: Effect of number of rake fingers on OOB rejection.

rejection is shown for multiple frequency bands for visualization and a similar profile can be anticipated for code-modulated fingers. Moreover, increasing the number of fingers adds to the power overhead of the RX due to additional clocking circuitry.

The SNR improvement, OOB rejection, and power consumption tradeoffs indicate that a 3-finger design is optimum as further increasing the RX number of fingers results in minimal SNR improvements at the expense of reduced OOB rejection and higher power consumption. An overall SNR improvement of nearly 29 dB is possible between the PG and multipath gain in a 3-finger rake RX design at reasonable input SNR levels allowing using wide switches for low switch resistance while keeping the power consumption below 50 mW per finger as discussed in Section 4.3 for implementation details.

4.2.4 PN codes and Synchronization

The performance of the proposed CD FD rake RX depends greatly on the choice of the used PN codes. Ideal PN codes should reject both TX SI and multipath as indicated by (4.2). An ideal PN code is characterized by having a unique auto-correlation peak (for multipath rejection) and zero cross-correlation (for TX SI rejection). Different code families were proposed for CD operation [31, 38] such as Walsh codes, m-sequence, and Barker codes[2]. Although these code families do not have the optimum properties of ideal code, they can approximate some of them.

For example, Walsh codes have ideal cross-correlation as shown in Fig. 4.8a providing 50 dB TX SI rejection [38, 87] while they have bad auto-correlation due to repetitive nature (Fig. 4.8b) making them unsuitable for multipath operation. On the other side; m-sequences, Gold codes, and Barker codes have near ideal auto-correlation (Fig. 4.8c) making them more suitable in multipath environments while their cross-correlation is limited reducing the achieved TX SI rejection.

[2]More details can be found in Section 3.1.6

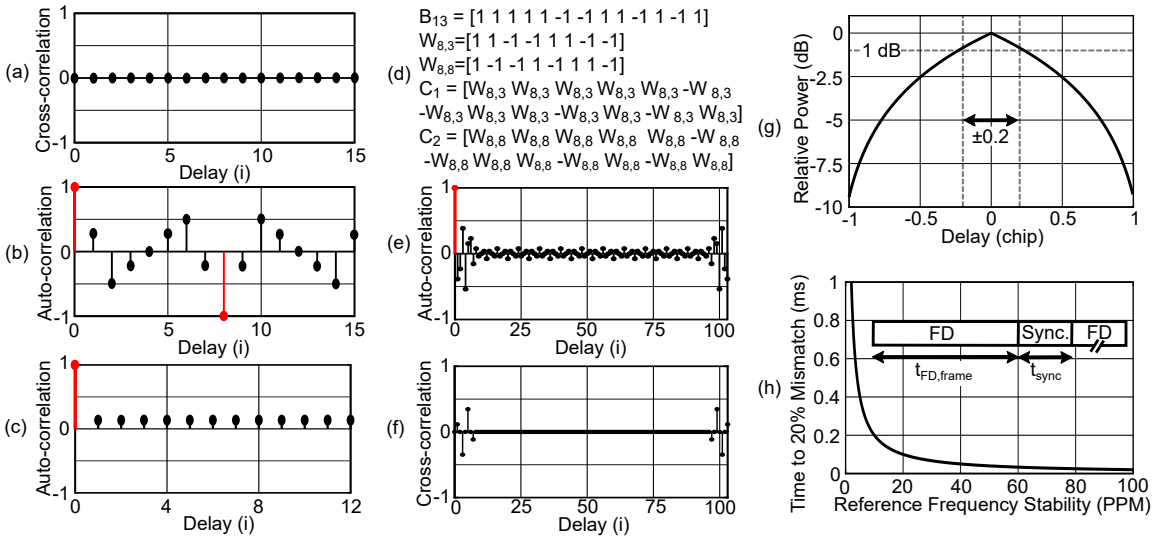


Figure 4.8: Properties of different PN codes: a) Zero cross-correlation of 16-length Walsh code (good for SI rejection), b) Auto-correlation of 16-length Walsh code having multiple peaks (bad for multipath), c) Auto-correlation of 13-length Barker code having single peak (good for multipath), d) Combining Barker and 8-length Walsh codes for better auto-correlation and cross-correlation, e) Auto-correlation of combined codes with a unique peak, f) Cross-correlation of combined codes with ideal rejection for most lags, g) Effect of synchronization mismatch on IL, h) Effect of reference frequency stability on synchronization.

Combining two codes from different families leverages the merits of both codes resulting in better TX SI and multipath rejection compared to the original code. One way to combine different code families is through the repetition of a code family based on the phase of another code family. For example, Walsh codes could be repeated based on the phase of Barker code resulting in a PN code with improved auto-correlation and cross-correlation characteristics as indicated in Fig. 4.8d-f [87]. This is useful in a rake RX rejecting both TX SI and multipath components.

Another important aspect of the code-domain RX is synchronization. The code-domain RX only correlates matched code inputs when they are synchronized. Any synchronization mismatch results in breaking the correlation and thus hinders the correct reception of the signal. Synchronization dictates that the PN code of the RF modulated signal and the locally generated finger PN code have the same delay. This can be achieved

by delaying the finger PN code and observing the in-band signal power for various delays and adjusting the delay for peak power. A shift-register can be used for synchronization as discussed in Section 4.3.

A critical point for synchronization is maintaining the synchronization state for a long duration. Frequency references such as micro-electromechanical system (MEMS), surface acoustic wave (SAW), and crystal oscillators suffer from variations in their oscillating frequency with environmental changes such as temperature and supply variations. The frequency stability is characterized by a part per million (PPM) accuracy indicating how much the frequency deviates from the desired frequency. This frequency deviation affects the synchronization of PN codes and could result in losing the acquired synchronization state. Simulations indicate that 20% synchronization mismatch increases the IL by <1 dB as shown in Fig. 4.8g for the combined Walsh-Barker code.

Fig. 4.8h plots the time it takes to reach the 20% synchronization mismatch for different 100 MHz reference frequency stability. For example, a 10 PPM reference would take 200 μs (200 symbols at 1 MSymbol/sec) to lose synchronization while a 2 PPM reference would take 1 ms (1000 symbols at 1 MSymbol/sec which is long enough) for the same mismatch. This means that the FD transceiver could transmit/receive an FD frame for a duration ($t_{FD,frame}$) determined by the available reference frequency stability then a synchronization cycle takes place with a duration (t_{sync}) where synchronization is restored before re-establishing FD operation. Maintaining FD BW efficiency requires that $t_{sync} << t_{FD,frame}$, and this can be achieved by using high stability references. It is worth mentioning that there are frequency sources with sub-PPM stability [88] and GPS references [89] with part per billion (PPB) accuracy could be used instead if tighter specifications are required depending on the FD system application.

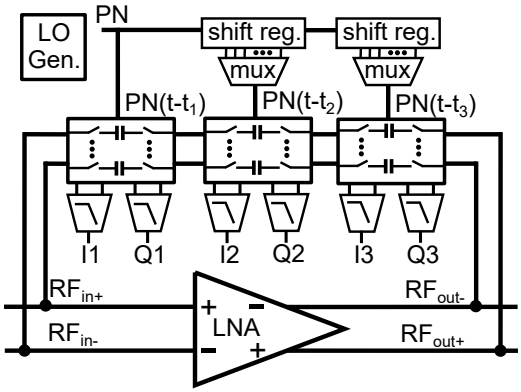


Figure 4.9: Top level schematic of the 3-finger rake RX.

4.3 Rake RX Implementation

The proposed rake RX is implemented in a 45-nm CMOS SOI process. The RX schematic is shown in Fig. 4.9 consisting of an LNA with three PN-modulated N-path filters in feedback. The chip also includes high-linearity BB filtering providing I and Q outputs for the three fingers along with digital logic for clock generation and PN synchronization. A detailed schematic for the building blocks of the rake RX is shown in Fig. 4.10 and this section describes the design details of the RX different blocks.

4.3.1 LNA and N-path Feedback filters

The RF front-end of the rake RX consists of an LNA with resistive feedback for matching and three PN modulated N-path filters to capture different multipath components. The LNA and filters schematics are shown in Fig. 4.10a and b. The filters employ a double switch configuration for improved rejection compared to using a single switch architecture [63]. The LNA uses thin oxide devices at 1-V supply while the switches of the N-path filters use thick oxide NMOS devices with $W/L = 75\mu/112nm$.

Thick oxide switches allow higher clock swings at the gate of the switches thereby reducing the switch resistance compared to thin oxide switches as the source/drain of

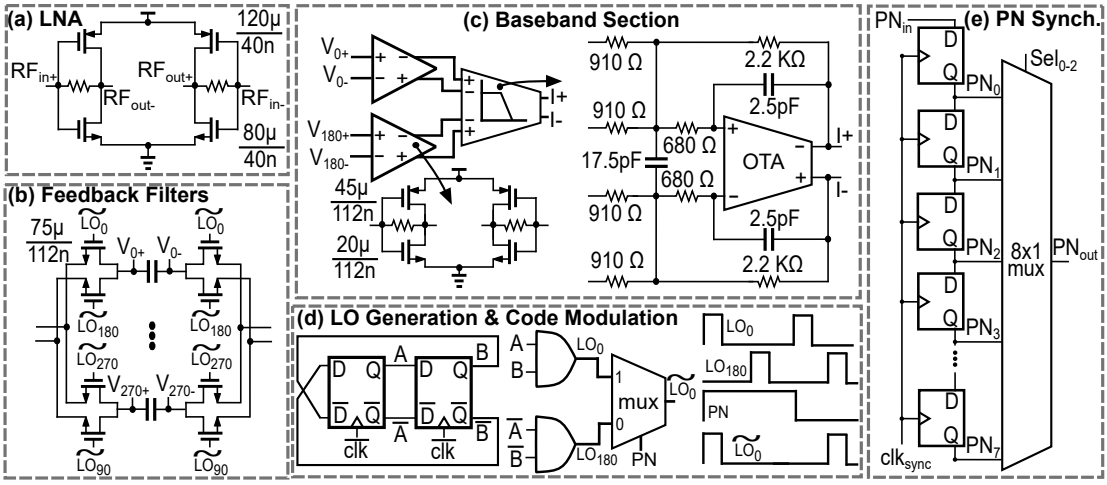


Figure 4.10: Detailed schematics for the rake RX building blocks: a) LNA with resistive feedback, b) 4-path feedback filters, c) High-linearity BB Rauch biquad filter, d) Non-overlapping clock pulses generation and PN modulation, e) Digital logic for PN synchronization.

the switches connected to the input/output of the LNA are biased at $V_{DD_{LNA}}/2$ (0.5-V), as well as increasing the RX linearity. The thick oxide switches are clocked at 1.7-V resulting in a gate-source voltage swing of 1.2-V compared to only 0.5-V if thin oxide switches were used. The filters non-overlapping clock pulses are modulated by delayed versions of the same PN code for code correlation as detailed in Section 4.3.3. The feedback filters are 4-path instead of 8-path for reduced clock power consumption at the expense of reduced OOB rejection. Each of the 4-path filters uses a capacitance of 35 pF which is implemented with a high-quality factor MIM capacitor with reduced back-plate parasitics.

4.3.2 High-Linearity BB Filtering

The BB section of the rake RX consists of a high-linearity Rauch filter as shown in Fig. 4.10c. The Rauch filter increases the RX roll-off to 60 dB/decade due to its 2^{nd} order transfer characteristics having 40 dB/decade roll-off in addition to the N-path 1^{st}

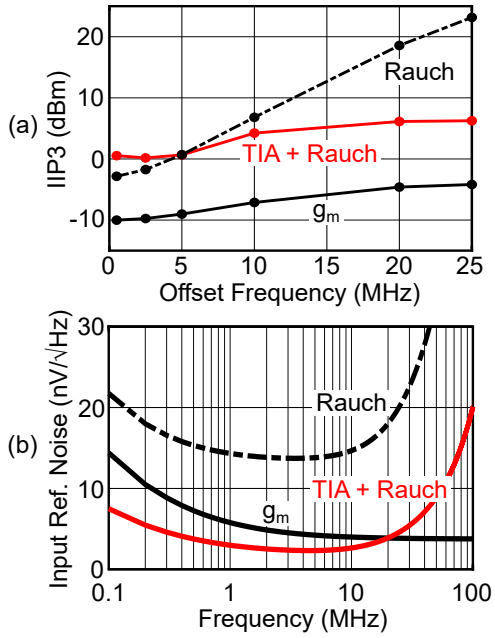


Figure 4.11: Different BB section implementation comparison: a) IIP3 versus offset frequency, b) Input referred noise.

order filtering of 20 dB/decade. In addition to enhancing the OOB IIP3 due to higher roll-off and OOB rejection, the Rauch filter also enhances the IB IIP3 of the RX. The IB IIP3 is enhanced due to the virtual ground at the operational transconductance amplifier (OTA) input due to negative feedback which enforces small signals at the OTA input across the gain-bandwidth product (GBW) of the OTA. The used OTA is a 2-stage OTA with common-mode feedback (CMFB) having a gain of 47.4 dB and a GBW of 440 MHz while consuming 1.3 mA at 1-V supply. The OTA uses 112 nm devices to reduce the effect of flicker noise. Fig. 4.11a demonstrates the IIP3 improvement of the Rauch filter when compared to open-loop g_m-cells having the same gain and BW.

However, the standalone Rauch filter has an input-referred noise of 13.2 nV/$\sqrt{Hz}$ which would increase the NF of the RX. To overcome the increase in the NF, trans-impedance amplifiers (TIAs) were added between the N-path capacitors and the Rauch filter inputs. After adding the TIA, the input-referred noise is reduced to 2.3 nV/$\sqrt{Hz}$

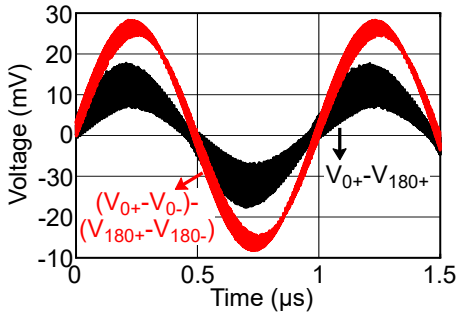


Figure 4.12: Differential sampling of BB capacitors (red) to reduce clock coupling compared to sampling single capacitor plate (black).

as shown in Fig. 4.11b at the expense of a slight decrease in OOB IIP3. IB IIP3 was also slightly improved due to less gain required from the Rauch filter enhancing its negative feedback. As demonstrated in Fig. 4.11, a TIA followed by the 2^{nd} order Rauch filter offers a good tradeoff between the noise and linearity requirements of the RX.

To further reduce common-mode noise and clock coupling, the capacitors of the N-path filters are sampled differentially by the TIAs and the Rauch filter was designed with dual differential inputs as shown in Fig. 4.10c. Fig. 4.12 shows the simulated transient waveform of the N-path capacitors and how differential sampling reduces common-mode noise compared to sampling one capacitor plate as done in previous literature.

4.3.3 Clock Generation, Code Modulation, and Synchronization

The non-overlapping clock pulse generation circuitry is shown in Fig. 4.10d generating 25% duty cycle clock pulses for the 4-path filters. The clock pulses are followed by PN code modulation logic. PN code modulation operates by selecting the clock pulse between 2 differential phases (i.e. select either clk_0 or clk_{180}, clk_{90} or clk_{270}, ...) using a multiplexer controlled by the PN code as illustrated by the waveforms in Fig. 4.10d.

The PN code was applied off-chip to facilitate measurements with different PN code

lengths and families but it can be easily integrated on-chip as done in Chapters 2 and 3. However, synchronization was implemented on-chip using the synchronization logic in Fig. 4.10e. The synchronization logic consists of an 8-bit shift register, implemented using D flip-flops, followed by an 8-to-1 multiplexer to select the desired delayed PN code. The shift register is clocked by a 100 MHz synchronization clock such that the 8-bit shift register is sufficient to cover the first 3 taps of the EPA channel. More bits can be added for a more general RX with minimal power overhead as the synchronization circuitry uses static logic with ultra-low power consumption. Also, fine-tuning can be added using the same synchronization architecture clocked at a higher clock frequency depending on the used chip rate and required synchronization accuracy.

4.3.4 Fingers Combining

Finally, after capturing the different multipath components at each finger, the outputs of the fingers should be combined for SNR improvement. The output of each finger was given in the time domain by (4.6) which can be expressed in the frequency domain as:

$$RF_{out,i}(\omega) \approx h_{CH,i} \times RX(\omega) e^{-j\omega t_{CH,i}}, \tag{4.16}$$

where $RF_{out,i}(\omega)$ is the finger output spectrum and $RX(\omega)$ is the spectrum of the received signal. The channel delay ($t_{CH,i}$) is a random variable leading to different IQ phase rotation for each finger output. This phase rotation should be accounted for before combining the outputs of the different fingers to avoid corrupting the received signal.

The IQ phase rotation correction can be done in the RF domain using phase interpolation [90] to delay the N-path I and Q clocks of each finger or in the digital domain using DSP techniques. Doing the phase correction in the digital domain would require 6 ADCs for the 3-finger RX. However, the overall power consumption would be lower compared

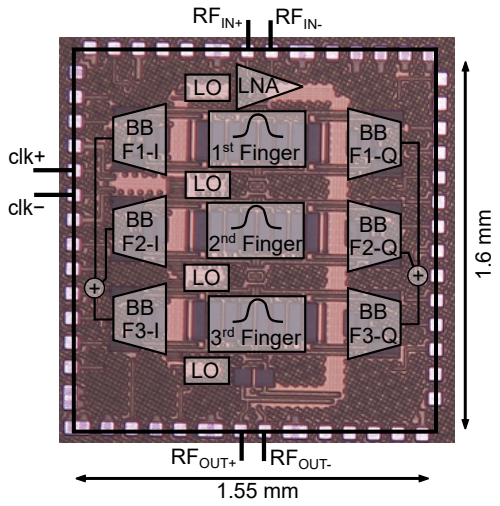


Figure 4.13: Chip micrograph in 45-nm SOI process.

to delaying the RF clocks as the ADCs only sample the signal BW of a few MHz. The implemented chip included a unity gain 3-input analog summer to sum the outputs of the three fingers in the BB domain for demonstration purposes and the channel delays were assumed integer multiples of the RF clock cycle to avoid any phase rotation issues[3].

4.4 Rake RX Measurements

The rake RX is implemented in a 45-nm CMOS SOI process and occupies an active area of 1.6 mm^2 as shown in Fig. 4.13. The RX measurements were performed on a chip-on-board assembly of the rake RX as shown in Fig. 4.14 where an arbitrary waveform generator (AWG) was programmed in Matlab to model the multipath channel propagation effects. The RX consumes 44 mA from 1 V supply (LNA and 3 BB fingers) and 55 mA from 1.7 V supply (clock, logic, and PN output test buffers) corresponding to 45.8 mW/finger at 1 GHz.

[3]The channel delays were 30 ns and 70 ns for a 1 GHz RF carrier such that the outputs can be added directly.

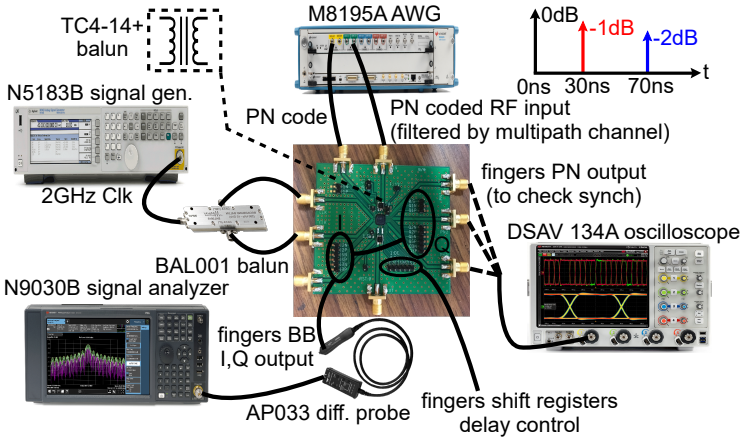


Figure 4.14: Measurement setup of the rake RX.

4.4.1 Conversion Gain and NF Measurements

The conversion gain of each finger was measured by applying an unmodulated CW to the RX (with PN codes off for the desired finger while the other fingers having their PN modulation on) and observing the finger's BB output. The RX is tunable from 0.4 to 1.4 GHz (limited by baluns BW) with a conversion gain of 30.5 dB at 1 GHz and a 3-dB BW of 10 MHz. The conversion gain is consistent between the 3 fingers with only ±0.25 dB of variation as shown in Fig. 4.15. The conversion gain profile is characterized by a 60 dB/decade roll-off due to the BB high-order Rauch filter enhancing the RX OOB linearity and rejection. The LNA provides 7 dB of the RX conversion gain and the rest is from the BB TIAs and Rauch filter.

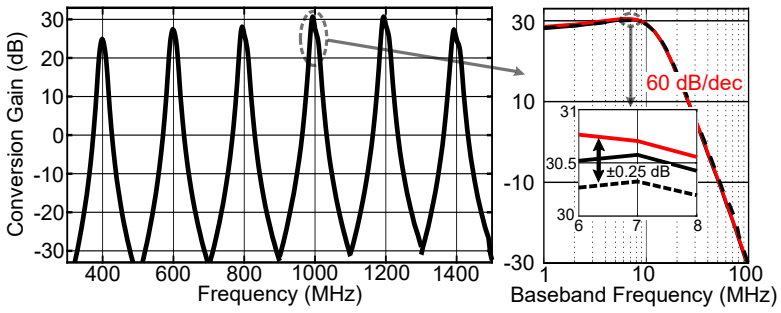


Figure 4.15: Measured conversion gain of the rake RX fingers with 60 dB/decade roll-off and negligible variations between the 3-fingers.

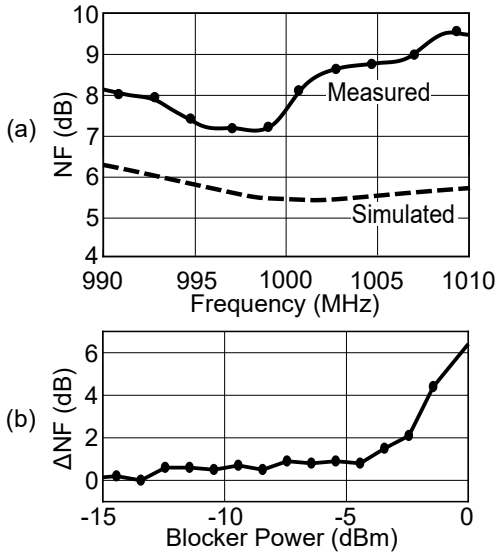


Figure 4.16: NF performance of the RX: a) Measured NF compared with simulations, b) Blocker NF for a CW blocker at 76 MHz offset.

The RX has an NF of 7.1 dB at 1 GHz. Fig. 4.16a illustrates the NF variation across the BW of the RX and Fig. 4.16b shows how the NF is affected by a blocker at 76 MHz offset frequency. The blocker NF increases by less than 1 dB until a -4 dBm blocker and further increases by 6.4 dB for a 0 dBm blocker. There is around 2 dB variation between simulated and measured NF that is attributed to the rise and fall times of the N-path clock pulses and the NF can be improved by enhancing the clock path routing and the clock generation power consumption.

4.4.2 Rejection Measurements

The rejection of the 3 fingers is measured using Walsh PN codes and is shown in Fig. 4.17 illustrating the BB spectrum of the three fingers for a QPSK input signal with a symbol rate of 6.25 MS/sec modulated by a 100 MChips/sec 16-length Walsh PN code matched to the 3^{rd} finger while orthogonal to the 1^{st} and 2^{nd} fingers. The matched finger output spectrum is correlated into the signal BW while the orthogonal finger output

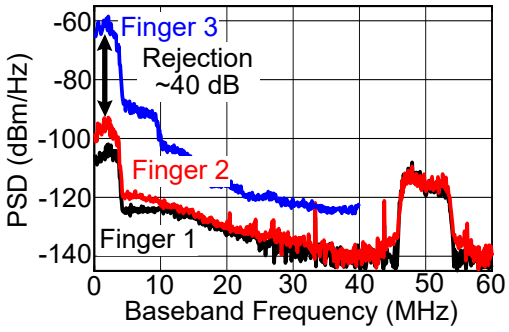


Figure 4.17: Measured rejection for a 6.25 MS/sec QPSK signal modulated by a 100 MChip/sec 16-length Walsh code matched to the 3^{rd} finger while orthogonal to the 1^{st} and 2^{nd} fingers.

spectrum is spread OOB and rejected by the high-order BB filtering. For optimum Walsh code pairs with the highest rejection, the OOB signal is located at $f_{chip}/2$ and significantly rejected by the BB filter as shown in Fig. 4.17.

The measured rejection varies between 41.2 dB and 33.9 dB depending on the order of fingers. The rejection of the 1^{st} finger is 38.8 dB and 41.2 dB to the 2^{nd} and 3^{rd} fingers respectively. While, the rejection of the 2^{nd} finger is 36.6 dB and 33.9 dB to the 1^{st} and 2^{nd} fingers. Also, the rejection of the 3^{rd} finger is 35 dB and 34.2 dB to the 1^{st} and 2^{nd} fingers. It is observed that non-adjacent fingers have better rejection due to reduced leakage between these fingers.

The achieved rejection of the RX can be enhanced by employing extra SI cancellation techniques such as using a circulator/EBD at the antenna interface, analog cancellation, or digital cancellation. Applying other techniques in other domains could possibly increase the RX rejection to around 100 dB making it suitable for FD communications at reasonable TX power levels as will be demonstrated in Chapter 5.

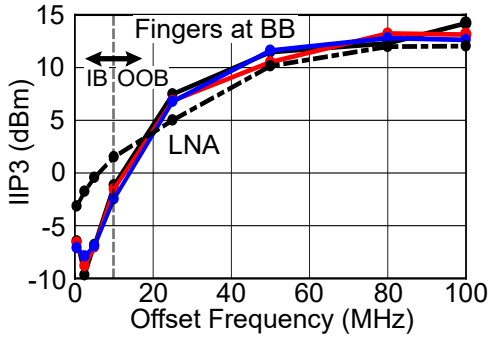


Figure 4.18: Measured IIP3 for IB and OOB frequencies at the LNA and fingers BB outputs.

4.4.3 Linearity and Compression Measurements

The linearity of the RX was characterized at both the LNA RF output and fingers BB outputs as shown in Fig. 4.18. The LNA IIP3 ranges from -3.2 dBm for IB frequencies and increases to 12 dBm for OOB frequencies. The BB IIP3 was measured for the three fingers. The IIP3 of the 1^{st} finger varies between -6.5 dBm for IB frequencies and increases to 14.2 dBm for OOB frequencies. While the IIP3 for the 2^{nd} and 3^{rd} fingers was -6.6 dBm/-7.1 dBm and 13.2 dBm/12.8 dBm for IB and OOB frequencies respectively. The IIP3 profile is consistent among the three fingers and presents one of the highest reported BB IB IIP3 values due to the highly-linear Rauch BB filters and thick oxide CMOS N-path switches.

Similarly, the 1-dB compression point (P1dB) and blocker 1-dB compression point (B1dB) were measured for the LNA and BB fingers. The LNA P1dB is -11.7 dBm while the B1dB ranges from -12.4 dBm to -1.8 dBm for a CW blocker at 10 MHz and 400 MHz offset frequency respectively. The BB fingers B1dB ranges from -22 dBm at 5 MHz offset to 0 dBm at 200 MHz offset. The blocker compression behavior for the LNA and BB output is summarized in Fig. 4.19. The compression behavior is consistent among the three fingers with less than 1 dB variation. The above measurements were performed at 1 GHz operating frequency and improved performance was observed at 0.6

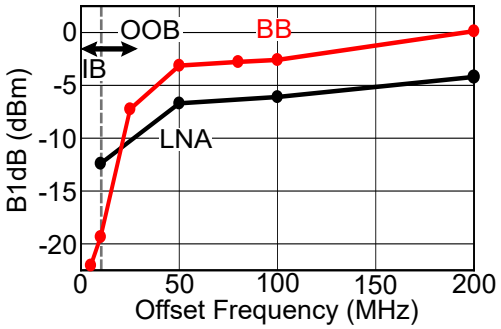


Figure 4.19: Measured compression behavior for blockers at different offset frequencies at the LNA and fingers BB outputs.

GHz where the LNA P1dB increased from -11.7 dBm to -4.9 dBm and the BB B1dB increased from 0 dBm to 4.4 dBm and this can be attributed to better rise/fall times for the non-overlapping N-path clock pulses at the lower frequency.

4.4.4 Performance in Multipath Channels

To demonstrate the operation of the proposed rake RX, it was measured in the EPA channel model with 3 multipath taps. A 0.78125 MS/sec QPSK signal modulated by a 100 MChip/sec 128-length PN code was filtered with the multipath channel model in Matlab and generated by the AWG. Each finger was synchronized to a specific multipath component by controlling the delays of the on-chip shift registers and the BB output spectrum was observed. The measured synchronization profile for the 1^{st} finger, shown

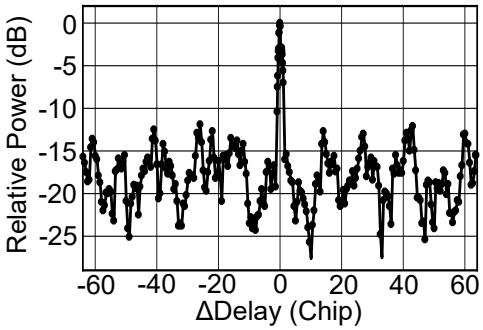


Figure 4.20: Measured synchronization profile of the 1^{st} finger demonstrating signal reception at the correct delay while rejecting delayed multipath versions.

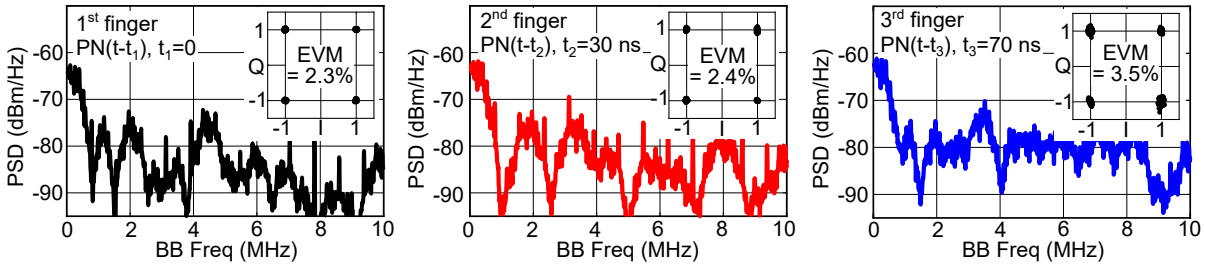


Figure 4.21: Measured BB spectrum and EVM of the three fingers in the EPA channel model.

in Fig. 4.20, has a single unique auto-correlation peak at the correct multipath lag indicating reception of the synchronized multipath tap while rejecting other taps.

The measured spectrum in Fig. 4.21 shows that signal can be gathered at each finger output and the measured EVM is 2.3%, 2.4%, and 3.5% for each of the 3 fingers. The EVM degrades slightly for the 3^{rd} finger due to reduced signal power for this tap. PN code synchronization between the 1^{st} and 2^{nd} fingers is shown in Fig. 4.22 with 30 ns time difference corresponding to the used EPA channel model delay.

The chip also includes a unity gain 3-input summer to sum the outputs of the 3 fingers and the sum signal has an average 9.04 dB increase in signal power compared to that of a single finger as shown in Fig. 4.23. There are some variations compared to the theoretical SNR improvement of 8.6 dB due to measurements non-idealities and mismatches in the fingers and summer gain. It is worth mentioning that the combining

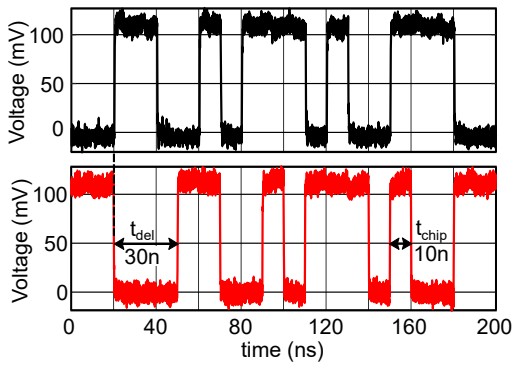


Figure 4.22: Measured PN code synchronization between the 1^{st} and 2^{nd} fingers.

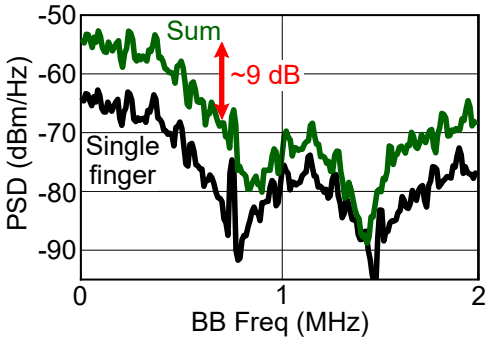


Figure 4.23: Measured signal improvement of the summer output spectrum compared to that of a single finger.

ratio of the three fingers can be configured in different ways such as equal-gain combining (as implemented here) or maximal-ratio combining to improve the SNR of the RX [91].

Table 4.1 summarizes the performance of the proposed code-domain RF rake RX with respect to previous FD receivers. The proposed work demonstrates the first multipath RF CD FD RX for improved SNR in fading environments and has one of the highest reported BB in-band IIP3s due to the highly-linear Rauch BB section.

4.5 Conclusion

This chapter presented a TX SI tolerant, multipath tolerant, multi-finger FD rake RX. The rake RX uses PN code orthogonality to reject both TX SI and multipath propagation non-idealities. The rake RX consists of 3 fingers each synchronized to a multipath component delay to capture multipath signals and enhance the RX SNR. Measurements indicate around 40 dB of TX SI rejection and 9 dB SNR improvement in multipath channels while consuming 45.8 mW per finger.

Table 4.1: Rake RX performance summary and comparison

	JSSC17 [22]	ISSCC18 [59]	JSSC18 [60]	JSSC19 [92]	JSSC19 [80]	JSSC20 [38]	TMTT20 [93]	RFIC20 [94]	This Work
Architecture	Circulator + BB Camcellation	EBD + RF Cancellation	Code-Domain RX	2x2 FD MIMO Circulator RX	Freq. Hopping	Code-Domain RX	BB Cancellation	RF + BB Cancellation	Code-Domain Rake RX
Technology	65 nm	40 nm	65 nm	65 nm	65 nm	45 nm	65 nm	65 nm	45 nm
Frequency	0.6 - 0.8 GHz	1.6 - 1.9 GHz	0.3 -1.4 GHz	2.2 GHz	0.4 - 1 GHz	0.25 - 1.25 GHz	0.5 - 3.5 GHz	0.1 - 1 GHz	0.4- 1.4 GHz
RX Gain	42 dB	42 dB	38 dB	30 dB	–	39 dB	30 - 50 dB	15 - 38 dB	30.5 dB
RX NF	10.9 dB	8.1 dB	3.4 - 4.9 dB	9.5 dB	6 dB	9.35 dB	5.3 dB	7.2 dB	7.1 dB
RX Power	159 mW	106 mW	36 mW	202 mW/element	24 mW	90 mW	20-58 mW	63 mW	45.8 mW/finger
BW	12 MHz	40 MHz	1 MHz	20 MHz	0.5 MHz	6.25 MHz	10 MHz	20 MHz	0.78 - 10 MHz
RX IB IIP3	-33 dBm	-17 dBm	-26 dBm	–	–	-22 dBm	6 dBm	-18.7 dBm	-6.5 dBm
RX OOB IIP3	19 dBm	–	–	–	–	9 dBm	27 dBm	–	14.2 dBm
Rejection (Technique)	42 dB (Circ. + BB)	39 dB (EBD) + 31 dB (RF)	38.5 dB (Code Rej.)	45 dB (RF+BB)	33 dB (FHSS)	52 dB (Code Rej.)	35 dB (BB)	30.2 dB (RF + BB)	33.9 - 41.2 dB (Code Rej.)
Area	1.4 mm^2	4 mm^2	0.31 mm^2	5.6 mm^2	3.1 mm^2	2.6 mm^2	1.5 mm^2	5.15 mm^2	1.6 mm^2

Chapter 5

A CD FD Transceiver with a CMOS Magnetic-Less Circulator for >100 dB SI Rejection

This chapter presents a CMOS-based CD FD transceiver operating in a link at 1 GHz. The CD FD link rejects in-band TX SI by more than 100 dB through a combination of PN code orthogonality, circulator, and digital cancellation algorithms. A non-magnetic CMOS circulator based on switched transmission lines is used as an antenna interface with >40 dB maximum rejection[1]. Then, TX and RX modulators spread the TX SI and correlate the desired RX signal in the RF domain. Orthogonality between PN codes allows an additional >40 dB maximum rejection relaxing the FD transceiver linearity requirements. Finally, digital SI cancellation (SIC) eliminates any residual TX SI in the digital domain using a least mean squares (LMS) estimation for the SI channel based

[1]The work presented in this chapter is a collaboration between UCSB and Columbia University. Special thanks to Aravind Nagulu and Prof. Harish Krishnaswamy from Columbia University for providing their CMOS circulator to demonstrate the complete FD transceiver.

on a non-linear truncated Volterra series model. The digital SIC can have almost 40 dB of rejection depending on the SI power level. An implemented FD node leverages these techniques to achieve an overall rejection that is around 104 dB bringing the TX signal from 20 dBm to the noise floor of the RX at -85 dBm.

CD receivers for TX SI rejection were presented in previous chapters of the thesis, which focused on the stand-alone implementation of the CD sub-system. This chapter expands on previous chapters to present a detailed discussion about a complete CD FD transceiver with circulators and digital SIC. This chapter highlights the challenges in implementing a full system and how system-level integration and the accompanied non-idealities affect the rejection of each sub-system when they co-exist. Measurements were used to quantify the effects of system-level integration and solutions were proposed to overcome some of these challenges.

Section 5.1 discusses the proposed FD transceiver implementation with details about the non-magnetic circulator, TX and RX modulators, and digital cancellation algorithm performance. Section 5.2 addresses the challenges in achieving the RF CD operation and proposes solutions to overcome these challenges. Section 5.3 outlines some of the unique advantages of RF CD signal processing such as linearity improvement, and blocker/multipath tolerance in practical wireless environments. Section 5.4 presents the measurement results of the proposed CD FD transceiver and a discussion about FD transceivers figure of merit (FOM) allowing a quick evaluation of different transceiver architectures is presented in Section 5.5.

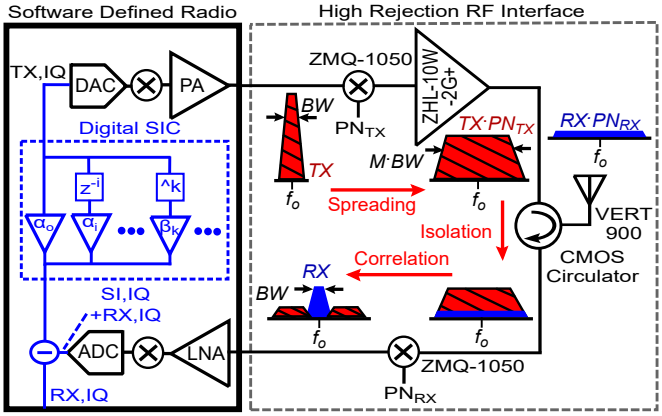


Figure 5.1: Proposed CD FD transceiver employing a non-magnetic CMOS circulator, TX/RX code modulators at RF, and digital SIC.

5.1 Proposed CD FD Transceiver with CMOS Circulator and Digital SIC

The proposed CD FD transceiver is shown in Fig. 5.1 and is built upon a software-defined radio (SDR) that allows reconfiguration of the radio parameters such as the carrier frequency, data rate, modulation characteristics, TX power, etc. A National Instruments universal software radio peripheral (NI USRP 2930) [74] is used as an SDR and controlled through Labview and Matlab. Using an SDR allows a fair evaluation of the proposed system given the limited resources of a real transceiver (such as ADC sampling rate and resolution, RX noise figure, ...) compared to using high-end, off-the-shelf measurement equipment such as oscilloscopes and spectrum analyzers. The USRP provides access to the TX and RX RF data along with the BB IQ data streams which are used for digital SIC.

The USRP is preceded by the proposed high-rejection RF interface consisting of the TX and RX code modulators and the CMOS circulator. More details about the modulators and circulator are presented in later subsections. Finally, a commercial-off-the-shelf (COTS) antenna is used to evaluate the effect of antenna voltage standing

wave ratio (VSWR) on the achieved rejection. A dual-band, omni-directional antenna (VERT900 antenna) covering 824-960 MHz and 1710-1990 MHz frequency range is used [75] as a demonstrative example.

5.1.1 FD Transceiver Requirements

Implementing an FD transceiver with high SI rejection requires a careful consideration of the specifications of the various sub-blocks of the transceiver. Also, targeting a TX power of >20 dBm increases the linearity, compression, and rejection requirements of the RF interface. An FD link analysis is presented for the proposed CD FD transceiver relating the specifications of various blocks and how they impact the performance of the proposed transceiver.

The antenna interface greatly impacts the performance of subsequent RX blocks. Circulators are the optimum choice for FD systems allowing compact FD systems with a single antenna while avoiding the fundamental 3-dB loss of the EBD. Magnetic circulators offer ∼15 dB of isolation [76] requiring the RX modulator to handle >5 dBm TX SI to target >20 dBm TX power level which is challenging and magnetic circulators are bulky increasing the FD transceiver form factor. This leaves non-magnetic CMOS circulators with >40 dB of isolation and watt-level power handling as the only currently viable option for the proposed CD FD transceiver [24, 26]. CMOS circulators greatly relax the RX modulators' power handling requirement to -20 dBm. However, this comes with an extra challenge for the circulator linearity requirements.

The circulator should be highly linear such that any third-order intermodulation (IM3) tones are below the minimum detectable signal (MDS) of the RX. The MDS of the RX is given by

$$MDS = -174 + 10 \times log_{10}(BW) + NF, \tag{5.1}$$

where NF is the noise figure of the RX. The NF of the implemented RX includes the noise from the USRP, circulator, and PN modulators. The USRP has an average NF of 6 dB [74], the circulator has 2.5 dB NF [26], the modulator NF is 5 dB consistent with its IL [78], and extra 2.5 dB are added to the NF to account for extra losses from used cables, baluns and connectors. This results in an overall NF of 16 dB for the RX and an MDS of -88 dBm for a sampling BW of 10 MHz[2].

The required circulator IIP3 is given by [25, 93]

$$IIP3_{circ} = \frac{3 \times P_{TX} - Rej_{circ} - Rej_{dig} - P_{RX,IM3}}{2}, \tag{5.2}$$

where $P_{RX,IM3}$ is the IM3 power level at the RX due to circulator nonlinearity and should be reduced to the MDS signal level. This results in a circulator TX-RX IIP3 requirement of 34 dBm to handle a 20 dBm TX signal assuming 40 dB of rejection is achieved from each of the circulator and non-linear digital cancellation[3]. A similar analysis shows that the modulator linearity requirement is not a limitation given that the RX modulator handles a TX SI of -20 dBm due to the available 40 dB of rejection from the circulator.

The above analysis also indicates that 108 dB of rejection is required for the FD transceiver to bring the 20 dBm TX signal to the noise floor of the RX at -88 dBm. This rejection is budgeted among the 3 used domains such that ∼40 dB of rejection is achieved from the circulator, another ∼40 dB from CD rejection, and the remaining rejection from digital SIC. The actual performance of the FD transceiver slightly deviates from the theoretically calculated values due to various system imperfections as discussed in Section 5.4.

[2]The sampling BW is the used chip rate to avoid aliasing. The NF can be reduced by ∼ 5dB for a fully integrated RX by reducing the modulators' and connectors' losses.

[3]Assuming that code rejection only affects the TX signal and does not reject the IM3 tones generated by the circulator. It will be verified through measurements later that spreading improves the circulator IIP3 by PN code processing gain as analyzed in Chapter 3.

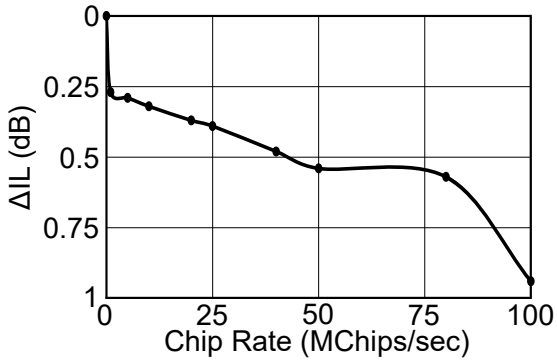


Figure 5.2: Measured IL of the TX/RX modulators as a function of chip rate.

5.1.2 TX and RX Modulators

The TX signal is spread by a PN code (PN_{TX}) while the RX signal is correlated by an orthogonal PN code (PN_{RX}). Both codes are clocked at a chip rate that is M times the symbol rate where M is the length of the PN code. The TX signal spreads across a bandwidth BW_{spread} that is M times the signal bandwidth, BW_{sig}. Spreading RF signals at high chip rates requires high-speed modulators.

Minicircuits ZMQ-1050 modulators were used to spread and correlate the TX and RX signals [78]. COTS modulators allow easier experimentation of the FD node and comparison of code parameters. CMOS CD FD implementations for the RX correlators were presented in previous chapters allowing low IL with high power handling and post PA TX modulators were presented in [68,69] with <1.5 dB IL and >30 dBm power handling capability. Consequently, there is no limitation in implementing a compact CMOS CD FD RF front-end including the TX and RX modulators along with the CMOS circulator.

The modulators operate between 0.8 GHz and 1.05 GHz with an IL of 4.9 dB and a 1-dB compression point of 4 dBm. The modulators support frequencies (chip rates) up to 100 MChip/sec and Fig. 5.2 plots how the IL changes with modulation frequency indicating <1 dB degradation in IL at very high modulation frequencies. The 4 dBm compression point allows the RX to support TX SI power levels up to 30 dBm given

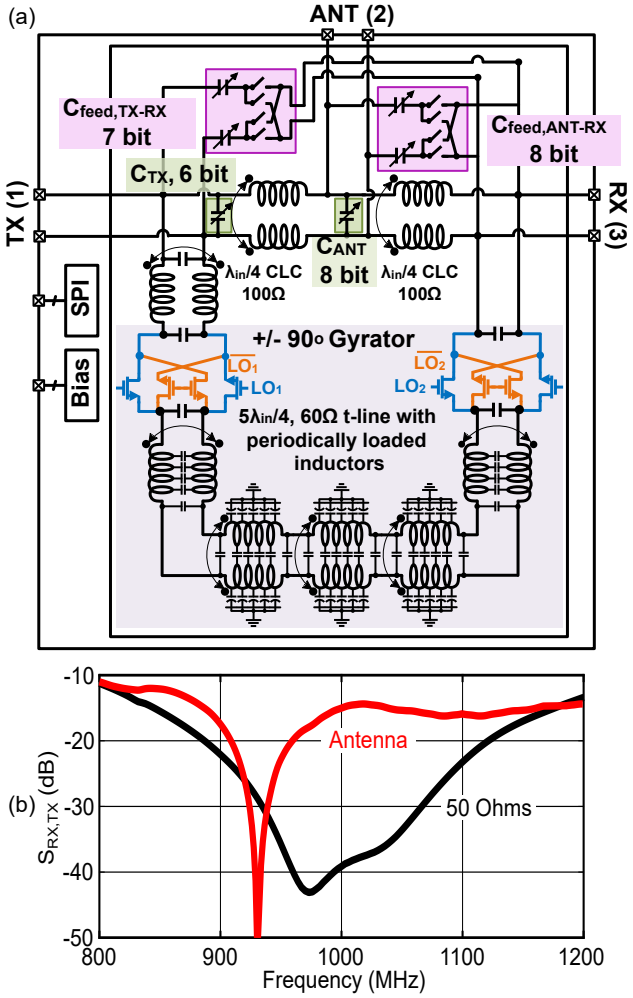


Figure 5.3: Multi-watt 1 GHz CMOS circulator employing the concept of switched transmission lines: a) Circuit schematics, b) Measured TX-RX rejection with 50 Ω and antenna termination.

that the circulator provides >30 dB rejection. However, the 4-dBm compression point limits the TX power levels. Thus, the TX modulator is followed by a wideband PA (ZHL-10W-2G+) to allow 30 dBm TX power levels [95].

5.1.3 Non-magnetic CMOS Circulator

The circuit implementation of the magnetic-less CMOS circulator is shown in Fig. 5.3a and is based on switched transmission lines. The circulator includes a built-in an-

tenna balancing scheme with tunable feed-capacitors at orthogonal feed points to cancel the TX-RX leakage generated due to ANT mismatches and other non-idealities. In addition, a novel clock boosting technique using level-shifted capacitors was used to increase the peak-to-peak voltage of the modulation signal to $3\times V_{dd}$ without compromising the long-term reliability of the transistors. The level-shifted capacitors allow the clock path to operate at its regular supply voltage V_{dd} yet providing a $3\times$ modulation signal swing. The circulator consumes $4\times$ lower power consumption than that of the circulator in [24], yet provides $2.5\times$ higher power handling at the TX port.

The 1-GHz, 180-nm SOI CMOS circulator exhibits 2.1/2.6 dB TX-ANT/ANT-RX IL with a 1dB BW of 172MHz. When terminated with a 50Ω termination, the measured TX-to-RX isolation is >40dB. The feed-capacitors can be tuned to achieve >40dB isolation across the entire 2.33:1 antenna VSWR and beyond. The circulator achieves TX-ANT and ANT-RX IIP3s of +50dBm and +36.3dBm respectively. The TX-ANT IIP3 is larger than the ANT-RX IIP3 due to the placement of the gyrator next to the RX port, consequently eliminating the TX swing on the gyrator switches [23]. The measured TX-ANT P_{1dB} is +34dBm, thanks to the used linearity enhancement techniques such as clock boosting and programmable capacitors with device stacking. This large signal performance represents a significant improvement compared to the prior CMOS circulators [23, 24]. More details about the circulator operation and performance can be found in [26]. The measured TX-RX rejection of the circulator is shown in Fig. 5.3b when a 50 Ω termination and a COTS antenna are connected at the antenna port. The implications of the antenna VSWR on the overall rejection and code orthogonality in terms of group delay are discussed in Section 5.4.

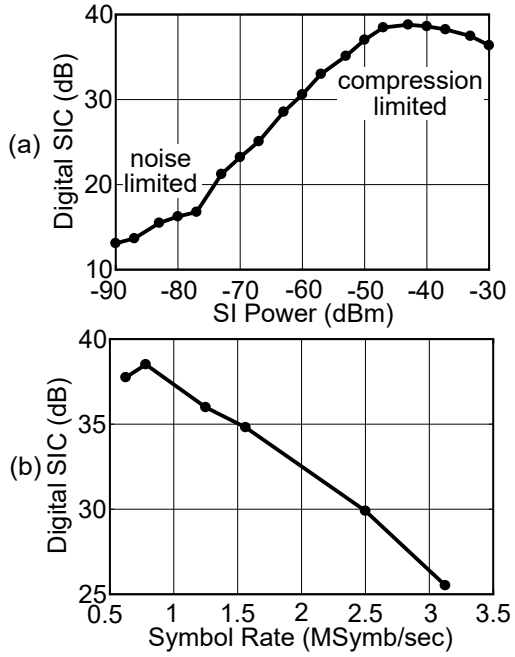


Figure 5.4: Digital SIC: a) Digital SIC versus SI power level, b) Digital SIC versus symbol rate at a fixed ADC sampling rate.

5.1.4 Digital SIC

Digital SIC was applied to the captured baseband IQ data from the USRP in Matlab. Digital SIC was implemented with a reduced-order non-linear Volterra series model for the SI channel with least mean squares (LMS) estimation to cancel residual in-band SI to the noise floor of the USRP [13]. The model of digital SIC is

$$SI[n] = \sum_{i=-5}^{7} \alpha_i \times TX[n-i] + \sum_{k=3,5,7} \beta_k \times TX^k[n], \tag{5.3}$$

where α and β are the coefficients of the linear and nonlinear taps solved by the LMS algorithm.

Fig. 5.4a shows the effect of applying digital SIC at different SI power levels for a 0.625 MSymbol/sec QPSK signal sampled at 12.5 MSample/sec. Digital SIC increases almost linearly with SI power for SI power levels between -75 dBm and -50 dBm indicating the

ability to reduce the SI to the noise level of the USRP. However, the digital SIC deviated from the linear behavior at high SI power levels by compression (SI greater than the ADC DR) and at extremely low SI power levels as the noise floor is approached. This suggests that the SI power should be reduced by the circulator and code rejection to the linear region of the digital SIC for optimal overall SI rejection.

Fig. 5.4b shows the achieved digital SIC at various symbol rates at a fixed ADC sampling rate of 12.5 MSample/sec. Digital SIC is reduced as the symbol rate increases due to reduced number of samples per symbol which degrades the quality of the SI channel estimation. Fig. 5.4b indicates that 8 samples per each TX symbol are required to have a rejection >35 dB. It is worth mentioning that this is a hardware limitation and higher symbol rates could be achieved using other high-end reconfigurable transceivers such as [11, 96] which could possibly allow data rates up to 15 MSymbol/sec. However, this requires a spreading BW in excess of 100 MHz which could be achieved in a 2-antenna transceiver configuration to avoid circulator BW limitations.

5.2 Challenges of CD FD Transceivers Implementation

Performing the CD signal processing in the RF domain entails addressing challenges of radio operation in a practical wireless environment. This section explores some of the challenges encountered in designing CD FD transceivers and proposes solutions to overcome these challenges. Meanwhile, numerous advantages are also gained by the RF CD processing that enhances the radio operation. These advantages are subsequently covered in the next section and verified by measurements.

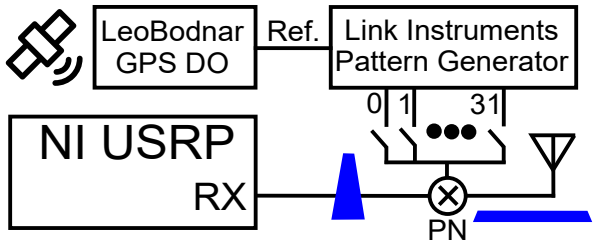


Figure 5.5: Synchronization setup using GPSDO.

5.2.1 Synchronization

CD operation demands the synchronization between at least two transceivers for proper operation. Doing the code correlation in the RF domain adds to the synchronization complexity compared to previous CDMA systems that relied on DSP for code correlation. In CDMA systems, the spread BW is captured by the ADC which allows utilizing digital resources for code synchronization and correlation. However; by doing the code correlation at the RF front-end, the RX BB processor will not be able to receive the desired signal unless exact code alignment is guaranteed at the RF correlators.

There are multiple challenges in CD FD transceivers synchronization. First, any two frequency references suffer from an inevitable frequency drift due to temperature, process, and supply variations. This drift complicates the synchronization process and demands using frequency sources with high-frequency stability. Advances in RFIC technologies make GPS available in most cellular devices with low power and area overheads. These GPS-synchronized receivers can be utilized to provide a stable frequency source [89]. While GPS synchronization is suitable for outdoor environments like base stations where a reliable GPS signal can be received, it might be unreliable for indoor situations. In that case, high stability frequency references such as temperature-compensated crystal oscillators (TCXO) with sub-part per million (ppm) accuracy can be used [88]. For example, a 1 ppm 10 MHz crystal would take 20 msec to have 20% synchronization mismatch which is extremely long compared to a symbol period of 1.6 μS at 0.625 MSymbol/sec.

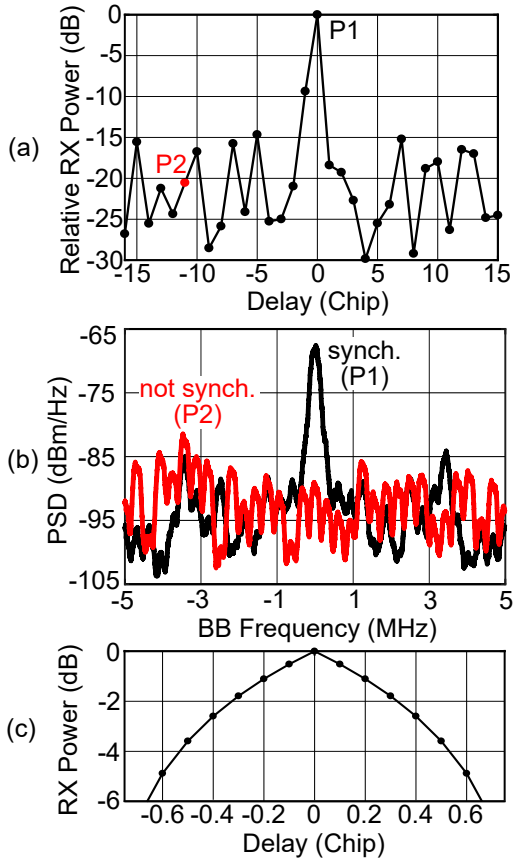


Figure 5.6: Measured synchronization profile: a) Relative RX power vs chip delay, b) Illustrative RX spectrum for synchronized and non-synchronized cases, c) Simulated synchronization profile near the peak.

The second challenge is code alignment. Any timing skew results in signal-to-noise ratio (SNR) reduction. However, the skew can be overcome by delaying the PN code with fixed digital delay steps and measuring the RX power for each step. Then, the correct delay is selected that maximizes the RX power. The code delay alignment can be updated regularly using digital logic gates with negligible power consumption.

Lastly, synchronization is more challenging for moving objects compared to stationary radios due to the accompanied Doppler shift. Multiple techniques were previously proposed in CDMA systems to overcome this issue [97, 98]. Synchronization would also require changes in the FD physical layer frame requiring a synchronization preamble be-

fore data transmission and this preamble should be much shorter compared to the data frame to maintain FD BW efficiency.

In the demonstration, synchronization was achieved using a GPS disciplined oscillator (LeoBodnar) to provide a 10 MHz reference to the PN pattern generator (Link-Instruments). The pattern generator has 32 output channels which were sufficient for synchronizing 32-length PN codes. The synchronization test setup is shown in Fig. 5.5 where one USRP was transmitting a QPSK signal spread by 32-length random PN code and the RX node was synchronized by observing the RX power. The measured synchronization profile is shown in Fig. 5.6 with a delay step of one chip period indicating a unique auto-correlation peak. Simulations indicate that the RX power is not affected by a slight synchronization mismatch and the RX IL increases by only 1.1 dB for $\pm 20\%$ synchronization offset as shown in Fig. 5.6c.

5.2.2 Out-of-Band Spectral Emissions

Another challenge in CD signal processing at RF is the spectral emission associated with the PN code spreading. RF transceivers should comply with a specific spectral mask as determined by the communication standard. Otherwise, OOB emissions could harm other receivers operating in nearby bands. One obvious approach to reducing the OOB spectral leakage uses a SAW filter after the TX. However, measurements with a commercial SAW filter [99] indicate insufficient adjacent channel leakage suppression as shown in Fig. 5.7a.

Another approach to reducing the OOB spectral leakage is by applying the pulse encoded transition (PET) technique described in [100]. The nearby OOB leakage can be greatly reduced through proper choice of the pulse width of the used PN code as indicated in Fig. 5.7c. Table 5.1 compares the effect of using a SAW filter and PET on the TX IL

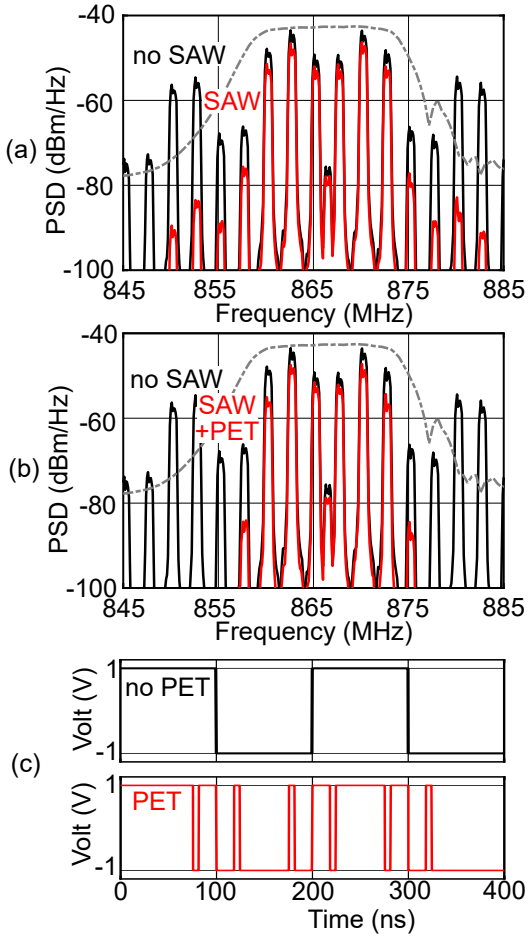


Figure 5.7: Measured ACLR improvement with PET: a) TX spectrum with limited ACLR rejection using a SAW filter, b) TX spectrum with enhanced ACLR rejection with PET and SAW filter, c) Added transitions on PN code for ACLR improvement.

and achieved adjacent channel leakage ratio (ACLR). The used PET technique reduces ACLR by >40 dB for an extra 1.2 dB of IL which is less than the SAW IL of 2.9 dB. Thus, presenting less degradation to the TX efficiency compared to SAW filters.

Table 5.1: Effect of PET on TX IL and ACLR

	TX IL (dB)	ACLR (dB)
No SAW	0	12.4
SAW	2.9	32.9
SAW + PET	4.1	40.1

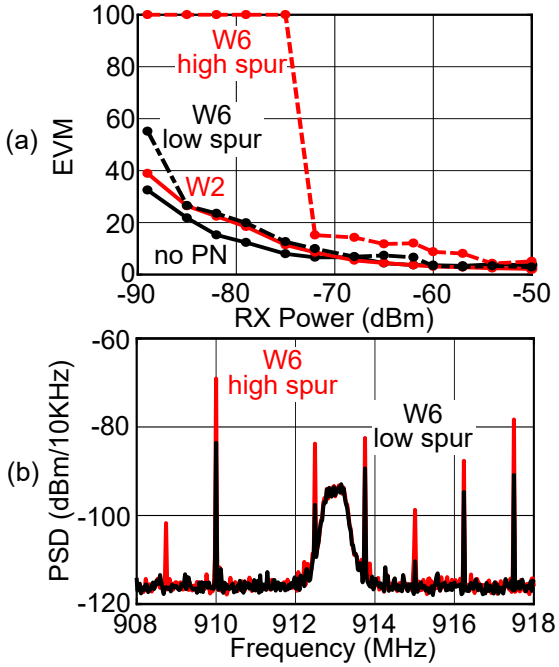


Figure 5.8: Effect of PN spurs: a) RX EVM vs RX power for different PN codes, b) Measured RX spectrum with high and low W6 spurs.

5.2.3 Minimum Detectable Signal and PN Spurs

Modulating the RF front-end with PN codes generates PN spurs in the RX spectrum. PN spurs are generated due to leakages and mismatches in the RF switches. PN spurs may pose a challenge in CD FD transceivers if not well taken care of when detecting signals near the sensitivity level of the RX.

Fig. 5.8a shows the measured EVM for varying RX power level without PN codes and with different 16-length Walsh codes using QPSK modulation. PN spurs degrade the RX EVM as the RX power approaches the noise floor of the RX. However at a reasonable RX SNR, around 15 dB, the EVM differences become negligible[4]. Also, it was noticed that PN codes with spurs at a higher frequency offset such as W2; which has the nearest spur at $f_{chip}/2$ from the RX center frequency (f_{RF}); has a better performance compared

[4]PN spurs require an extra 3-4 dB in SNR for a targeted bit error rate (BER) of 10^{-6} as QPSK requires an SNR of ~11dB.

to other Walsh codes where the spurs lie closer to f_{RF}.

To confirm that the EVM degradation is due to PN spurs, two measurements were performed using the same Walsh code but at different spur levels. The spur level was controlled by varying the PN code signal swing and the RX spectrum is shown for both cases in Fig. 5.8b. It is evident from Fig. 5.8a that reducing the PN spur level greatly enhances the RX EVM. Also, a longer PN code reduces the spur level and the PN spur offset frequency is deterministic depending on the used PN code and the performance can still be enhanced using digital spur cancellation techniques as in [101].

5.3 Advantages of CD Signal Processing for FD Communications

5.3.1 Linearity Improvement

FD links are designed to tolerate high TX power levels while receiving small desired RX signals. This places strict requirements on the rejection and linearity requirements of the TX-RX chain to handle the dynamic range difference between the TX and RX signals. Nonlinear distortion generated in the TX-RX chain should be reduced to the RX sensitivity level for proper signal reception and becomes of extreme importance when using CMOS circulators as analyzed in Section 5.1.

In contrast to the nonlinearity of the PA which can be cancelled through conventional RF cancellation techniques, the cancellation of distortions generated by the circulator is non-trivial as they are generated after the RF canceller tap. Based on (5.2), a circulator TX-RX IIP3 of 34 dBm is required to handle a 20 dBm TX signal.

Code-domain signal processing proves useful in relaxing the circulator IIP3 requirements in FD links. The IIP3 with PN code is enhanced by the processing gain (PG) of

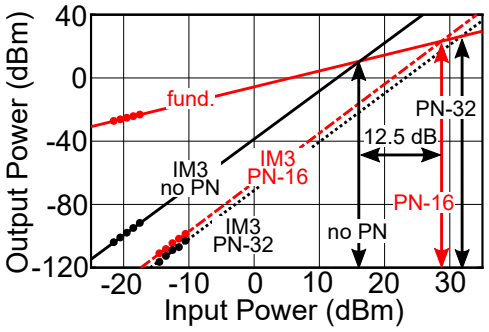


Figure 5.9: IIP3 improvement for the RX modulator with PN codes.

the used PN code as derived in Chapter 3, and is expressed as:

$$IIP3_{PN} = IIP3 + 10 \times log_{10}(M), \tag{5.4}$$

where M is the code length. The circulator IIP3 is increased by 12 dB for 16-length PN codes allowing >20 dBm TX power levels for the same RX sensitivity. Fig. 5.9 shows the effect of different PN codes on the RX modulator IIP3. The IIP3 increases from 16.25 dBm without PN codes to 28.75 dBm for a 16-length PN code and further increases to 31.75 dBm for a 32-length PN code confirming the theoretical prediction.

5.3.2 Blocker Tolerance

RF receivers operate in congested wireless channels demanding the RX to tolerate many blockers in addition to the TX SI. Radio regulation agencies like the Federal Communications Commission (FCC) regulate the spectrum by allocating different bands to different applications. So, RF filters are used at the RF front-end to remove blockers. These filters are usually implemented off-chip for better rejection raising the area and cost overhead. Moreover, RF radios could operate in hostile environments where jammers intend to obscure the RF communication link. RF CD signal processing relaxes the required filtering and blocker tolerance requirements due to the PG of the used PN code

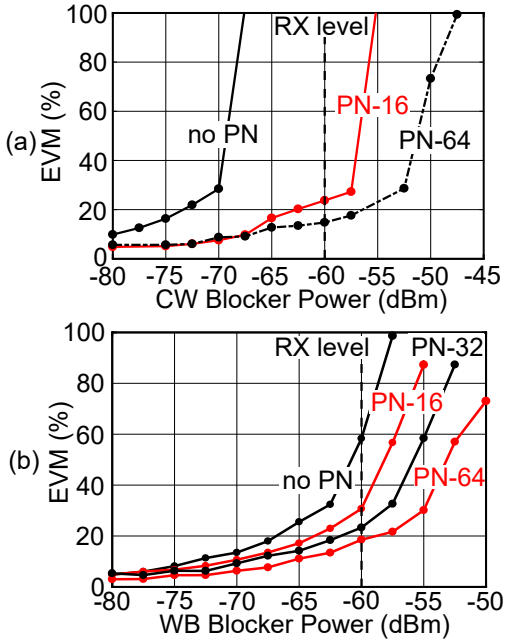


Figure 5.10: Blocker tolerance of RF CD signal processing: a) RX EVM versus IB CW blocker power without PN codes and with PN codes of different length, b) RX EVM versus IB WB blocker power without PN codes and with PN codes of different length.

which spreads the unwanted blockers across the spread BW.

Fig. 5.10a shows the measured RX EVM versus the power of a continuous wave (CW) IB blocker at 0.25 MHz offset. The desired RX signal is a QPSK signal at -60 dBm while the IB blocker power is increased. Measurements indicate that without PN codes, the RX is desensitized even at a blocker power 10 dB less than the desired signal. Using 16-length PN codes enhances the blocker tolerance by 12.5 dB while using 64-length codes enhances it by 17.5 dB for the same EVM level. These results are consistent with the PG of the used code.

The same experiment was repeated with an IB wideband (WB) blocker (a QPSK signal with 10 MSymbol/sec at the same center frequency). PN codes also proved to be tolerant to WB blockers as shown in Fig. 5.10b.

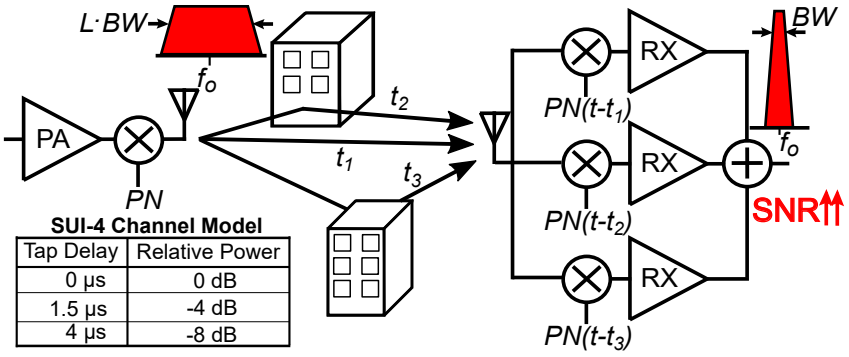


Figure 5.11: Multipath channel based on the SUI-4 model.

5.3.3 Multipath Tolerance

Another challenge in wireless environments is multipath propagation. As the TX signal propagates through different paths to the RX, the SNR can be harmed by fading and intersymbol interference (ISI) if the path delays are in the same order of magnitude as the symbol period.

Fig. 5.11 shows a typical wireless channel model based on the Stanford University Interim (SUI-4) channel model [83]. The wireless channel can be described as

$$h_C(t) = \sum_{i=1}^{I} h_{C,i}\delta(t - t_{C,i}), \tag{5.5}$$

where $h_{C,i}$, $t_{C,i}$ are the gain and delay of the additive wireless channel paths. Consequently the signal arriving at the RX antenna is

$$RX_{in}(t) = TX(t) * h_C(t) = \sum_{i=1}^{I} h_{C,i} \times TX(t - t_{C,i}), \tag{5.6}$$

indicating that the RX signal is deformed by the different multipath components.

RF CD signal processing proves to be resilient to multipath propagation. The PN coded TX signal $TX(t) = m(t) \times PN(t)$ reaches the RX after propagating through the

multipath channel as

$$RX_{in}(t) = \sum_{i=1}^{I} h_{C,i} \times m(t - t_{C,i}) \times PN(t - t_{C,i}). \tag{5.7}$$

Upon arriving at the antenna, the RX signal is multiplied by a PN code corresponding to a specific tap delay (with the largest path gain). This allows rejecting other multipath components due to orthogonality between different delayed versions of the same PN code.

$$\frac{1}{T}\int_{T} PN(t) \times PN(t - \tau)dt = 1/M \ \forall \tau \neq 0, \tag{5.8}$$

$$RX_{out}(t) = PN(t - t_{C,i}) \times RX_{in}(t) \approx h_{C,i} m_D(t - t_{C,i}) \tag{5.9}$$

The RX modulator output is then passed down the RX chain to the LNA without being affected by multipath effects.

The proposed RX was tested in a multipath environment to show the effects of the used PN code on multipath resilience. A QPSK signal with 0.625 MSymbol/sec was modulated by a PN code of varying length and filtered by the multipath channel (Fig.

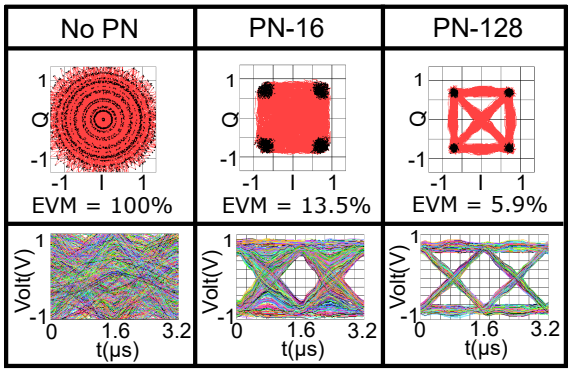


Figure 5.12: Measured EVM and eye diagram for different PN code length in a SUI-4 multipath channel showing the advantage of PN codes in restoring the RX eye diagram and EVM.

5.11) in Matlab and generated by an arbitrary waveform generator (M8195a) to the proposed RX. The RX EVM and eye diagram were measured using Labview Software for 16/32/64/128 length PN codes and without PN codes as shown in Fig. 5.12. Measurements indicate that PN codes help in restoring the eye-opening enabling correct reception despite multipath effects. Also, increasing the used PN code length results in a better RX EVM.

Another important advantage of using PN codes is that the RX can be configured to receive different multipath components by using different RX fingers each synchronized to a different tap known as a "Rake RX" [84]. A simple rake RX implementation is shown in Fig. 5.11 and a low power CMOS implementation was proposed Chapter 4 [39].

Fig. 5.13 shows the 3-fingers EVM and eye diagram for 128-length code and Table 5.2 summarizes the results of the proposed RX with the multipath channel model and

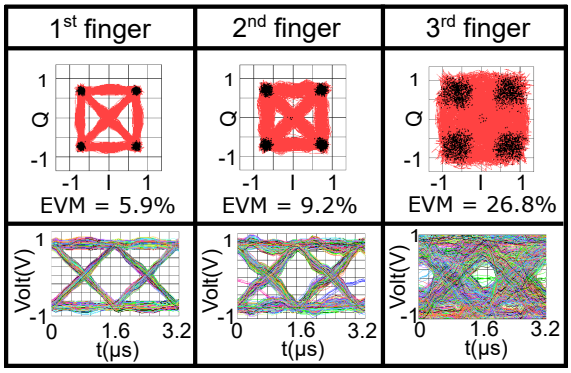


Figure 5.13: Measured EVM and eye diagram for the 3-fingers of the rake RX with 128-length PN code in a SUI-4 multipath channel indicating correct reception of multipath components improving the RX SNR.

Table 5.2: Measurements summary in a multipath environment based on the SUI-4 channel model

	no PN	PN-16	PN-32	PN-64	PN-128
1^{st} Finger EVM	NR	13.5%	12.8%	7.5%	5.9%
2^{nd} Finger EVM	NR	NR	NR	22.6%	9.2%
3^{rd} Finger EVM	NR	NR	14.5%	NR	26.8%

NR=Not Recognized

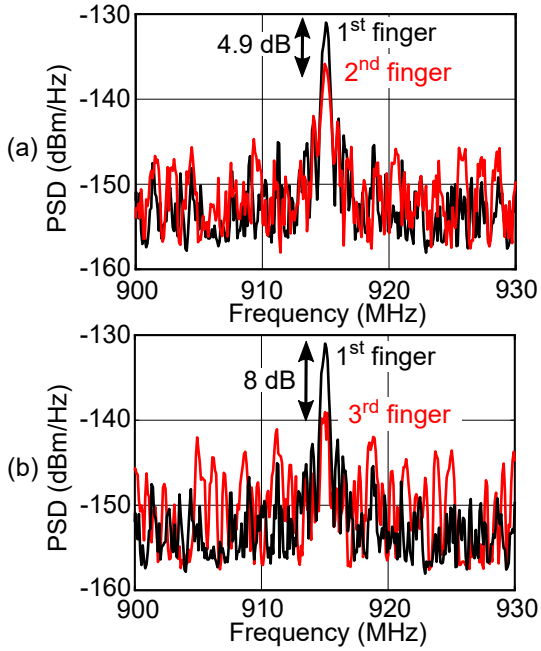


Figure 5.14: Measured spectrum in a SUI-4 channel with 128-length PN code: a) 1^{st} finger versus 2^{nd} finger, b) 1^{st} finger versus 3^{rd} finger.

shows the advantages of increasing the PN code length on the RX signal SNR. Fig. 5.14 shows the measured spectrum for the 3 fingers. The measured RX power levels were -73.5 dBm, -78.4 dBm, and -81.5 dBm for the 3 fingers in agreement with the multipath channel model relative gains.

5.4 CD FD Transceiver Link Measurements

The CD FD transceiver system was measured by generating a QPSK signal from the USRP TX port. The TX signal symbol rate was programmed between 0.625 to 3.125 MSymbol/sec limited by the used hardware. Then, the TX signal was modulated by a 16-length Walsh PN code with a chip rate between 10 MChip/sec and 50 MChip/sec depending on the used symbol rate. The Walsh code was generated by the Link Instruments pattern generator shown in Fig. 5.5. The modulated TX signal was amplified

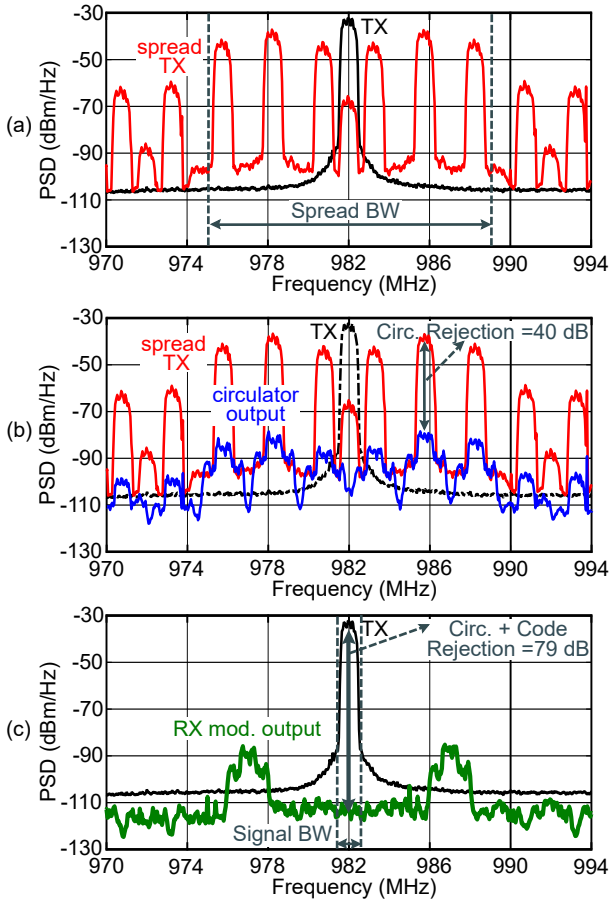


Figure 5.15: Measured spectrum at various nodes of the transceiver. a) TX spectrum at 26 dBm, b) cirulator RX output with 40 dB rejection, c) RX modulator output showing combined circulator and code rejection of 79 dB.

by a wideband PA (ZHL-10W-2G+) for an integrated power between 10 and 30 dBm. The PA output signal passes through the CMOS circulator to the RX modulator with an orthogonal PN code and the output of the RX modulator is connected to the USRP RX port for further signal processing.

An illustrative measured spectrum at various nodes of the transceiver is shown in Fig. 5.15 demonstrating the modulation of a 0.625 MSymbol/sec 26 dBm TX signal by a Walsh code at 10 MChip/sec and how the circulator rejection and RX code correlation increases the rejection of the TX signal.

For a complete characterization of the proposed CD FD transceiver, the rejection

was measured at varying symbol rates, chip rates, and TX power levels. Also, different combinations of Walsh codes were experimented with different antenna terminations to investigate the interaction between spreading and circulator rejection BW on the achieved rejection.

5.4.1 Performance with 50 Ω Termination

The rejection of the FD transceiver at the circulator RX port and after the RX modulator is shown in Fig. 5.16 when a broadband 50 Ω termination is used at the antenna port. The circulator rejection across the spread BW reaches 46.9 dB at 20 dBm TX power and 10 MChip/sec chip rate and the rejection decreases at higher chip rates and TX power levels as demonstrated in the left plot of Fig. 5.16.

The combined circulator and code rejection across the signal BW depends on the choice of PN codes as discussed in Chapter 3. For example, Walsh codes W1 and W2 offer better rejection relative to Walsh codes W5 and W6 due to the robustness of orthogonality to bandwidth limitations. Measurements demonstrate that a maximum rejection of 90.5

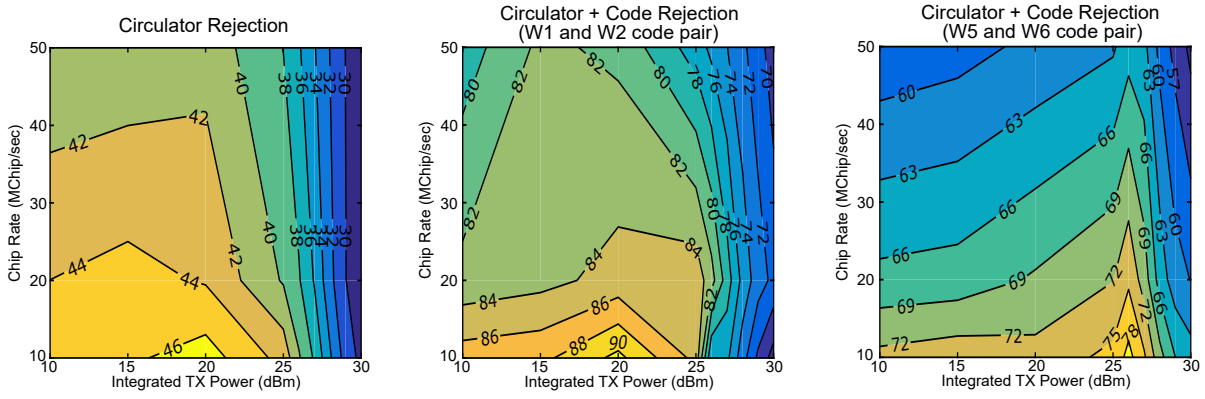


Figure 5.16: Measured Rejection of the FD system in a 50Ω environment at different power levels and chip rates. Left: circulator rejection, Middle: circulator and code rejection using optimum 16-length Walsh code pairs (W1 and W2), Right: circulator and code rejection using other Walsh code pairs (W5 and W6).

dB is possible with W1 and W2 Walsh code pairs (Fig. 5.16 middle). When using W5 and W6 code pairs, the rejection reduces to 79 dB (Fig. 5.16 right). It was also observed that the TX power peak rejection depends on the code spreading properties suggesting that the rejection can be optimized by re-tuning the circulator at different TX power levels for different PN codes.

5.4.2 Performance with Antenna Termination

The same experiment was repeated with the circulator connected to a COTS VERT900 antenna. The measured circulator TX-RX isolation with the antenna after tuning the feed-capacitors is shown in Fig. 5.3b compared to that with a 50 Ω termination. The rejection bandwidth of the circulator is reduced due to the antenna and the achieved circulator rejection depends on the effective signal bandwidth over which the TX signal is spread. Fig. 5.17 shows that the combined circulator and code rejection drops to 56 dB for W5 and W6 code pairs and to 70.9 dB for W1 and W2 code pairs representing represents around 20 dB degradation compared to 50 Ω termination.

This degradation can be attributed to the group delay (GD) variation between the TX and RX ports of the circulator when connected to the antenna. Fig. 5.18 illustrates the measured GD between the TX and RX ports with 50 Ω and antenna termination.

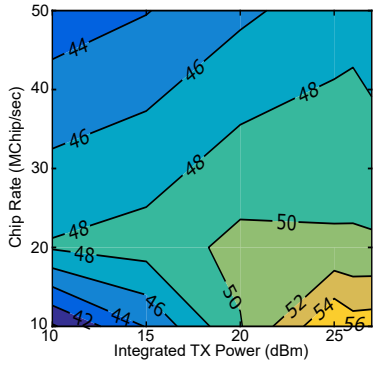


Figure 5.17: Measured circulator and code rejection with an antenna (W5 and W6).

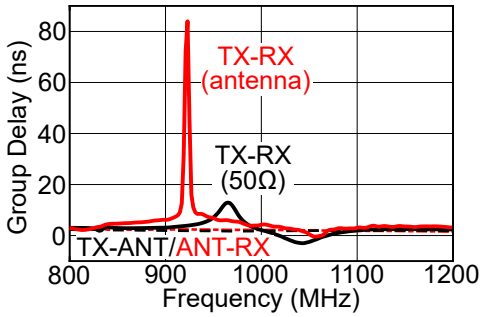


Figure 5.18: Measured group delay between different circulator ports with 50 Ω and antenna termination.

The TX-RX peak GD increases from 13 ns to 84 ns when adding the VERT900 antenna. This GD variation across the spread BW degrades Walsh codes orthogonality as the GD approaches the used chip period (100ns at 10 MChip/sec). The GD between the TX-ANT and ANT-RX ports was negligible compared to that between the TX-RX ports presenting no limitation on the signal transmission or reception. The rejection can be improved using a broadband antenna with lower VSWR variations across the spread BW given that high circulator rejection is maintained till 2.33 VSWR through the feed-capacitors tuning network.

5.4.3 Overall Rejection with Digital SIC

Finally, digital SIC was applied to the IQ BB data from the USRP as detailed in Section 5.1.4. Fig. 5.19a shows the results of applying digital SIC for the best case rejection where digital SIC was adding 13.6 dB rejection to the 90.5 dB achieved in the RF domain for a total of 104.1 dB. The overall rejection brings the 20 dBm TX power to the noise floor of the USRP around -85 dBm. It was noticed that the noise floor is degraded by ∼3 dB from the theoretically calculated value of -88 dBm due to TX induced NF from the circulator switches as the reported 2.5 dB NF of the circulator was measured without a TX signal and applying a TX signal increases the circulator NF.

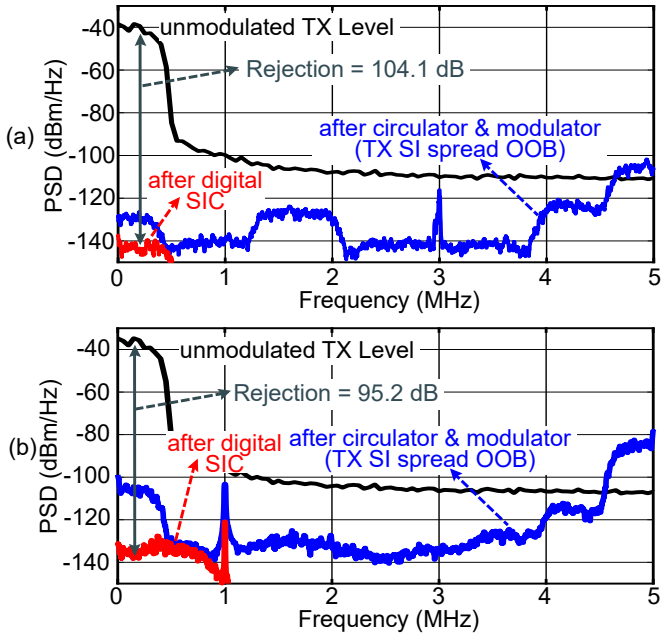


Figure 5.19: Measured overall rejection with digital SIC: a) 104.1 dB of rejection at 20 dBm TX power with 50 Ω termination, b) 95.2 dB of rejection at 23.5 dBm TX power with antenna termination.

Using the VERT900 antenna; digital SIC adds 26 dB to the 70.9 dB of RF rejection for a total of 96.9 dB at 15 dBm, and 27 dB to the 68.2 dB of RF rejection for a total of 95.2 dB at 23.5 dBm as shown in Fig. 5.19b. Digital SIC was more effective with antenna termination due to higher SI level confirming Fig. 5.4a and was limited by the noise floor in both cases of 50 Ω and antenna termination. An NF degradation of 2-3 dB was observed in the USRP noise floor after connecting the antenna due to the measurement environment and this slightly reduced the achieved rejection compared to the peak digital rejection in Fig. 5.4a. The total rejection and symbol rate can be improved by combining other RF/analog cancellation techniques with a better broadband antenna along with a lower noise RX with higher ADC sampling rates increasing the FD transceiver overall rejection.

5.5 FD Figure of Merit

Table 5.3 summarizes the performance of the proposed CD FD transceiver and how it compares with state-of-the-art literature. Fig. 5.20 compares the achieved figure of merit (FOM) of the proposed transceiver with that of other FD transceivers in literature. Table 5.3 and Fig. 5.20 focused on comparing the proposed work with full system FD implementations that span multiple SI rejection techniques for a fair comparison. The FOM is similar to that defined in [3] and is given by:

$$FOM = REJ \times P_{TX} \times BW \tag{5.10}$$

where REJ is the total system TX SI rejection in linear units, BW is the bandwidth in MHz, and P_{TX} is the TX output power in milliwatts. While there are other important factors to consider in FD systems (such as power consumption, NF, ...), these were not included in the FOM as most FD systems spanning multiple rejection domains relied on SDRs, FPGAs, or standard measurement equipment as their implementation platform and these factors were rarely mentioned in the respective papers.

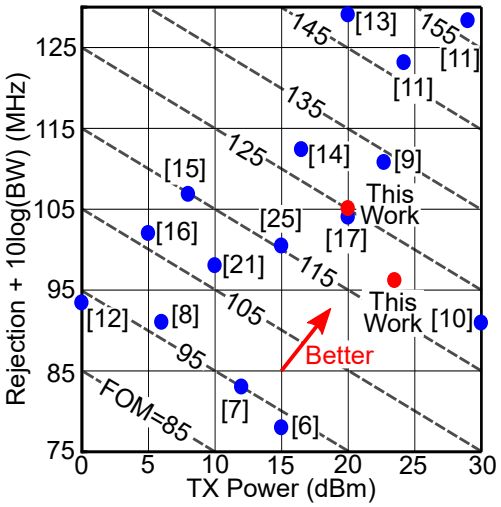


Figure 5.20: FD FOM comparison.

Table 5.3: CD FD transceiver performance summary and comparison with other FD systems

		Antenna Interface	Freq. (GHz)	Antenna Rej. (dB)	RF Rej. (dB)	Digital Rej. (dB)	Total Rej. (dB)	TX Power (dBm)	BW (MHz)	FOM (dBm.MHz)
Asilomar'10 [6]		2 Ant.	2.4	45	31	4	80	15	0.625	93
MobiCom'11 [7]		2 Ant.	2.45	45		28	73	12[1]	10	95
CoRR'11 [8]		2 Ant.	2.4	57	24	NA	81	6	10	97
Sigcomm'13 [13]		Magn. Circ.	2.45	72/62		38/48	110	25/20	20/80	148/149
GLOBECOM'15 [14]		Magn. Circ.	2.46	79/56		31.9/45.9	110.9/101.9	16.5/13.3	1.4/20	128.9/128.2
IMS'15 [9]		Ant. Array	2.45	81.8[1]	14.2	NA	96	22.7	30	133.5
VTC'15 [21]		EBD	0.89/1.89	44/45	41/38	NA	85/83	10	20	108/106
Comm. Mag.'16 [15]		Magn. Circ.	2.45	19.9/22.2	48.3/40.9	25.3/24.7	93.5/87.8	6.4/8	20/80	112.9/114.8
Wireless Comm.'16 [10]		Isol. Ant.	2.45	56/56.4	21.9/13.3	NA	77.9/69.7	30	20/120	120.9/120.5
GLOBECOM'17 [17]		Magn. Circ.[2]	0.9	21	36	34	91	20	20	124
INFOCOM'17 [16]		Magn. Circ.	0.9	50		45	95	5	5	107
Ant. & Prop. '17 [11]	Anechoic	Relay Ant.	2.56	75.5	16.9/7	22.9/24.6	115.3/107.2	29/28.5	20/80	157.3/154.7
	Indoors			64.1/63.5	NA	43/39.9	107.1/103.4	24.2/23.7	40/80	147.3/146.1
Wireless Comm.'18 [12]		Pol. Ant.	3.5	41.9	NA	30.6	72.5	0	123	93.4
ICC'19 [25]		CMOS Circ.	1	55		40	95	15	3.5[3]	115.4
This Work	50 Ohm	CMOS circ.	1	45.5	45[4]	13.6	104.1	20	1.25[5]	125.1
	Antenna			35.9/37.4	35/30.8[4]	26/27	96.9/95.2	15/23.5		112.9/119.7

[1]with spatial beamforming, [2]with passive antenna emulation, [3]estimated from plot, [4]RF code-domain rejection, [5]signal BW spread at 10Mchip/sec

The FOM only considers three metrics of the FD transceiver (REJ, P_{TX}, and BW) as they are the most important factors for FD systems and were reported in all FD systems papers. Rejection is clearly an important factor and the TX power level that can be handled is an extremely challenging problem given the linearity requirements of the RX. Also, the BW over which the rejection is achieved is an important factor to consider as achieving high rejection over a wide BW is a challenging problem for FD systems given the large variations in the frequency response of the SI channel.

The proposed CD FD transceiver achieves a FOM of 125.1 dBm.MHz and 119.7 dBm.MHz with 50 Ω and COTS antenna termination. The FOM was calculated using the signal BW of 1.25 MHz for a fair comparison with other works that do not apply signal spreading. However, the FOM would increase to 137.1 dBm.MHz if the spread BW was used and it can be justified by noting that the overall system BW efficiency is not affected by spreading as we can have multiple transceivers operating in the same spread BW such that each transceiver uses an orthogonal PN code given that the system uses PN codes with good cross-correlation properties to maintain rejection and system capacity along with network coordination to assign and synchronize codes for the simultaneous users.

Section 3.1.5 briefly discussed various PN code families for code-domain systems indicating the availability of various codes with good cross-correlation. It is also evident that increasing the used code length is advantageous for the proposed FD system (improved PG, multipath tolerance, ...) but this requires a trade-off between the used symbol rate and spread BW. Increasing the code length for a fixed symbol rate requires higher spread BW dictating higher circulator BW and ADC sampling rate. While increasing the code length for a fixed spread BW would severely limit the used symbol rate. Other tradeoffs for longer codes also exist like synchronization and increased system latency. However, this can be alleviated by using better synchronization algorithms. CD FD systems with

32-length codes at 64 MChip/sec chip rate and 2 MSymbol/sec symbol rate seem feasible and continued research in FD systems would certainly result in better systems[5].

5.6 Conclusion

This chapter presented a CD FD transceiver with around 100 dB TX SI rejection at >20 dBm TX power levels. The CD transceiver operates by spreading/de-spreading the TX/RX signals in the RF domain to achieve rejection due to the orthogonality of different TX/RX PN codes. The FD transceiver also uses a multi-watt, high-rejection CMOS circulator and digital SIC to improve the achieved rejection. Measurements indicate a CD FD technique that is tolerant to TX SI as well as IB CW and modulated blockers. Moreover, orthogonality between delayed PN codes proves useful in practical wireless environments providing tolerance to multipath propagation effects and reflections.

[5]CDMA started with 14.4 kbps in IS-95 and eventually reached 10 Mbps in WCDMA [32].

Chapter 6

Conclusions and Future Directions

This thesis presented an RF CD signal processing technique to improve the TX SI rejection in FD transceivers. RF CD signal processing operation was demonstrated with various chip implementations and a full system demonstration. RF CD signal processing allowed up to 50 dB of TX SI suppression which greatly increased the achieved rejection in FD transceivers along with relaxing the RX linearity requirements due to the PG of the used PN codes. Several advantages of the proposed RF CD signal processing technique were also investigated in the thesis such as tolerance to IB CW and modulated jammers, tolerance to multipath propagation effects in the wireless and SI channels, and enhanced SNR in multipath wireless environments.

Future directions possibly include a full system IC implementation of the RF CD signal processing front-end along with a circulator and an RF canceller, extending the CD operation to higher frequency bands such as millimeter-wave (mm-wave) frequencies, and investigating the application of the proposed RF CD signal processing in radars and multiple-input multiple-output (MIMO) systems.

6.1 Integrated FD Transceiver IC Implementation

Chapter 5 presented an FD transceiver demonstration that provided > 100 dB of TX SI rejection. The FD transceiver employed RF CD rejection along with a magnetic-less CMOS circulator and digital SIC to achieve good rejection. The FD transceiver can be enhanced through the application of RF and analog SI cancellation to increase the achieved rejection to more than 120 dB allowing higher TX power levels and a longer range for the FD link.

The FD transceiver implementation setup can also be improved through the application of a more powerful SDR with lower NF and increased ADC dynamic range and sampling rate. Moreover, the FD transceiver could be integrated in a single IC implementation including the CMOS circulator, RF CD correlators, and RF or analog cancellers. This would decrease the extra losses in the connectors, cables, and baluns allowing better RX sensitivity and NF. However, this requires careful design and simulations to avoid any substrate coupling and leakage in a single IC which could affect the RX performance.

Also, it was demonstrated that the used antenna greatly affects the achieved TX SI rejection and variations in the antenna VSWR across the spread BW degraded the circulator rejection and PN code orthogonality. A possible solution to mitigate these effects is the co-design of the circulator and antenna in a single printed circuit board (PCB) which would allow better control of the antenna tuning network, and consequently, achieving better TX SI rejection.

6.2 Millimeter Wave CD Signal Processing

This thesis focused on the application of CD signal processing to RF bands around 1 GHz. It was also shown that increasing the used PN code length results in better

performance due to increased PG, $PG = 10 \times log_{10}M$, where M is the used code length. The increased PG results in better rejection, easier synchronization as the difference between the synchronized power peak and unsynchronized spectrum increases, better blocker and multipath tolerance. However, increasing the code length at RF frequencies is challenging. Increasing the code length could be achieved at a fixed spread BW limiting the used symbol rate or at a fixed symbol rate requiring higher chip rates and increased spread BW.

Millimeter-Wave bands could allow longer PN codes at higher chip rates and symbol rates due to the availability of a much wider spectrum compared to RF bands. The RF CD signal processing techniques presented in this thesis could be extended to mm-wave bands either in the context of FD or FDD transceivers. Also, N-path and mixer-first RX architectures were recently extended to mm-wave bands where good performance was demonstrated at 28 GHz and even 70 to 100 GHz [102–108]. It might be worth investigating the application of the proposed CD modulation techniques to N-path and mixer-first receivers at mm-wave bands along with exploring their different applications such as CD radars and MIMO systems.

6.3 CD Signal Processing Applications in Radars and MIMO Systems

In addition to FD communications as presented in this thesis. RF and mm-wave CD signal processing could have potential applications in radars and MIMO systems. Automotive radars operate in environments surrounded by multiple barriers and objects in a congested wireless spectrum. This degrades the SNR of the radar decreasing the probability of target detection and possibly resulting in false detection of objects [109].

PN code orthogonality could enhance the performance of radars [110] and the various techniques implemented in this thesis could be extended to automotive radar applications as well.

Additionally, CD signal processing techniques could be useful in MIMO systems where multiple transceivers and beamforming are used to enhance the SNR of the communication link enabling higher data rates compared to conventional transceivers [111]. RF CD signal processing could be used in MIMO systems for interference and crosstalk mitigation due to code orthogonality, and power consumption reduction through sharing some of the transceiver resources by CD multiplexing [112–114].

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