

UC Riverside

UC Riverside Electronic Theses and Dissertations

Title

Advanced ESD Protection Using Graphene Technologies

Permalink

<https://escholarship.org/uc/item/0jv84981>

Author

Ma, Rui

Publication Date

2016

Peer reviewed|Thesis/dissertation

UNIVERSITY OF CALIFORNIA
RIVERSIDE

Advanced ESD Protection Using Graphene Technologies

A Dissertation submitted in partial satisfaction
of the requirements for the degree of

Doctor of Philosophy

in

Electrical Engineering

by

Rui Ma

June 2016

Dissertation Committee:

Dr. Albert Wang, Chairperson

Dr. Sheldon Tan

Dr. Ming Liu

Copyright by
Rui Ma
2016

The Dissertation of Rui Ma is approved:

Committee Chairperson

University of California, Riverside

Acknowledgements

Firstly, I would like to express my sincere gratitude to my advisor Prof. Albert Wang for the continuous support of my Ph.D study and related research, for his patience, motivation, and immense knowledge. His guidance helped me in all the time of research and writing of this thesis. I could not have imagined having a better advisor and mentor for my Ph.D study.

Besides my advisor, I would like to thank the rest of my thesis committee: Prof. Sheldon Tan, and Prof. Ming Liu, for their insightful comments and encouragement. I also want to thank all my labmates: Dr. Xin Wang, Dr. Qiang Fang, Dr. Hui Zhao, Dr. Jian Liu, Dr. Zitao Shi, Dr. Zongyu Dong, Dr. Chen Zhang, Dr. Li Wang, Mr. Fei Lu, Mr. Qi Chen, Mr. Chenkun Wang, Mr. Feilong Zhang and Mr. Chen Li. Thank you all for the advices and help over the years, for the times we were working together before deadlines, and for all the fun we have had in the last five years. I would like to thank Prof. Yahong Xie and Dr. Wei Zhang at University of California, Los Angeles, for their various forms of support during my graduate study. Also I thank Prof. Feng Liu for his precious support in the VCO research. I am very grateful for all your help.

My sincere thanks also go to Marvell Semiconductor and Broadcom Limited for the intern opportunity, especially to Dr. Wei Lu and Mr. Tom Liu.

Last but not the least; I would like to thank my family: my parents and my husband for supporting me spiritually throughout writing this thesis and my life in general.

To my family

ABSTRACT OF THE DISSERTATION

Advanced ESD Protection Using Graphene Technologies

by

Rui Ma

Doctor of Philosophy, Graduate Program in Electrical Engineering
University of California, Riverside, June 2016
Dr. Albert Wang, Chairperson

One of the most pervasive reliability problems of the IC (integrated circuits) industry is the ESD (electrostatic discharging) induced. It causes up to 35% of total IC field failures and billions of dollars are lost annually. Therefore, on-chip ESD protection structures are commonly used to protect IC parts from being damaged by ESD stresses. And ESD protection design becomes one of the most challenging IC design problems.

The popular ESD protection structures may or may not be suitable for ESD protection at sub-32nm. ESD-protected I/O dummy monitor circuits can be used to evaluate ESD protection capability and suitability for general ICs. Various simple diode ESD protection structures is studied by mixed-mode ESD simulation and conducted comprehensive TLP (transmission line pulse) characterization for both individual ESD diodes and ESD-protected monitor circuit blocks. Stand-

alone SCR and DTSCR are also studied to utilize the large current handling ability of SCR. TCAD simulation is discussed to provide design predictions. The goal is to provide practical design guidelines for robust ESD protection circuit design at 28nm node and beyond.

Compared to Si based ESD structures, 2D material graphene have unique electronic properties, it has been a rapidly rising star since it was found experimentally at 2004. Experimental results from transport measurements show that graphene has remarkably high electron mobility at room temperature. The structure of an electromechanical switch using graphene films is demonstrated. The graphene film is pulled into electrical contact with the bottom silicon by application of voltage bias between the layers. Contact is broken by mechanical restoring forces after bias is removed. The device switches several times without tearing. TLP testing confirmed that graphene is an attractive material for electromechanical switches which can be used as novel ESD protection structure.

Technology innovation is the key to IC design advances. However, conventional spiral inductors which have large size, poor Q-factor do not benefit from CMOS scaling. Novel IC inductors with vertical nano-particle magnetic cores could increase the L-density and thus reduce the area of the RF system-on-a-chip (SoC). A prototype LC-VCO using such a new magnetic-cored inductor is designed in an 180nm SOI CMOS.

Contents

| | |
|---|-----|
| List of Figures | xi |
| List of Tables | xiv |
| Chapter 1 General ESD Protection Design | 1 |
| 1.1 ESD Failure Problem | 1 |
| 1.2 ESD Protection Design Window | 2 |
| 1.3 ESD Protection Device Solutions | 3 |
| 1.3.1 Diode in ESD Protection Operation..... | 3 |
| 1.3.2 BJT in ESD Protection Operation..... | 5 |
| 1.3.3 MOSFET in ESD Protection Operation..... | 6 |
| 1.3.4 SCR in ESD Protection Operation | 7 |
| 1.4 Whole-Chip ESD Protection..... | 8 |
| Chapter 2 ESD-protected Monitor Circuits | 10 |
| 2.1 ESD Protection at Sub-32nm Node | 10 |
| 2.2 Diode ESD Design in 28nm CMOS | 10 |
| 2.3 ESD Design with Dummy Monitor | 12 |
| 2.3.1 ESD Behavior Modeling..... | 14 |
| 2.3.2 Dummy Monitor Circuit Measurements Analysis | 16 |
| 2.4 Conclusion | 20 |
| Chapter 3 SCR ESD Design..... | 21 |
| 3.1 SCR for ESD Protection Design | 21 |
| 3.2 SCR Design for CMOS 28nm Technology | 21 |
| 3.2.1 SCR TCAD Simulation Guidelines | 22 |
| 3.2.2 Core SCR Testing Results | 26 |
| 3.2.3 IO SCR Testing Results | 27 |
| 3.2.4 SCR Structure Horizontal Comparison..... | 28 |
| 3.3 Diode Triggered SCR Design for CMOS 28nm Technology | 32 |
| 3.3.1 DTSCR TCAD Simulation Guidelines..... | 34 |
| 3.3.2 DTSCR Design Splits | 41 |
| 3.3.3 Core STI DTSCR Testing Results | 42 |
| 3.3.4 IO STI DTSCR Testing Results..... | 43 |

| | | |
|---|---|----|
| 3.3.5 | IO Gated DTSCR Testing Results | 44 |
| 3.3.6 | DTSCR Structure Horizontal Comparison | 45 |
| 3.4 | Conclusion | 48 |
| Chapter 4 Introduction of Graphene | | 50 |
| 4.1 | History of Graphene..... | 50 |
| 4.2 | Band Structure of Graphene..... | 51 |
| 4.2.1 | Linear Dispersion..... | 51 |
| 4.2.2 | Effective Mass | 54 |
| 4.2.3 | Dirac Equation | 55 |
| 4.3 | Electrical Properties of Graphene | 57 |
| 4.3.1 | Ambipolar Electric Field Effect..... | 57 |
| 4.3.2 | Carrier Mobility | 58 |
| 4.3.3 | Minimum Conductivity..... | 59 |
| 4.3.4 | Quantum Hall Effect..... | 60 |
| 4.3.5 | Summary | 63 |
| Chapter 5 Graphene ESD Switch..... | | 64 |
| 5.1 | Graphene vs Conventional ESD Protection Structures..... | 64 |
| 5.2 | Graphene NEMS ESD Switch | 65 |
| 5.2.1 | A Novel ESD Concept | 65 |
| 5.2.2 | gNEMS ESD Switch Fabrication..... | 67 |
| 5.3 | Characterization and Discussions | 69 |
| 5.3.1 | DC Measurement Results | 70 |
| 5.3.2 | TLP Measurement Results..... | 70 |
| 5.3.3 | Reliability..... | 72 |
| 5.4 | Conclusion | 73 |
| Chapter 6 LC-VCO with Magnetic-Enhanced Inductor..... | | 74 |
| 6.1 | Introduction..... | 74 |
| 6.2 | Vertical Magnetic-Cored Inductors in CMOS..... | 74 |
| 6.3 | VCO Prototype Using Magnetic Inductor | 76 |
| 6.4 | Measurements And Discussions | 79 |
| 6.5 | Summary | 85 |
| Chapter 7 Conclusion..... | | 86 |

Bibliography..... 88

List of Figures

| | |
|---|----|
| Figure 1.1 Typical I-V curve shows ESD-critical parameters..... | 2 |
| Figure 1.2 An ESD protection design window | 3 |
| Figure 1.3 Typical diode I-V characteristics..... | 4 |
| Figure 1.4 Typical diode ESD protection schemes..... | 4 |
| Figure 1.5 Typical BJT ESD protection schemes..... | 5 |
| Figure 1.6 Typical GGMOS cross-section and equivalent circuit..... | 6 |
| Figure 1.7 Typical GGMOS ESD protection schemes..... | 7 |
| Figure 1.8 Typical SCR equivalent circuit and typical cross-section..... | 7 |
| Figure 1.9 Complete full-chip ESD protection scheme..... | 9 |
| Figure 2.1 Cross-section and ESD discharge path for an N+/P-well STI diode ESD device. ESD current crowding at STI reduces ESD protection capability... | 11 |
| Figure 2.2 Cross-section and ESD current discharging path for a poly-gated diode ESD protection structure..... | 12 |
| Figure 2.3 Schematics for ESD dummy gate monitor circuits: (a) gate ESD testing monitor only, and (b) gate ESD monitor and MOFET I-V testing circuit..... | 13 |
| Figure 2.4 ESD gate monitor circuit simulation schematic..... | 15 |
| Figure 2.5 Simulated ESD I-V curve for a gated diode 60um dummy ESD gate monitor circuit using behavior models..... | 15 |
| Figure 2.6 Measured ESD discharging curves by TLP testing for STI N diode designed in core process (W=60μm) with and without gate monitor..... | 17 |
| Figure 2.7 Measured ESD discharging curves by TLP testing for STI N diode designed in I/O process (W=60μm) with and without gate monitor..... | 17 |
| Figure 2.8 Measured ESD discharging curves by TLP testing for gated N diode designed in I/O process (W=60μm) with and without gate monitor..... | 18 |
| Figure 2.9 Measured ESD discharging I-V curves by TLP testing for STI P diode designed in core process with and without gate monitor with finger width 60um, 100um and 120um..... | 19 |
| Figure 2.10 Measured Id-Vds curves before and after TLP testing for STI N diode 120um designed in core process..... | 19 |
| Figure 3.1 SCR X-section..... | 23 |
| Figure 3.2 TCAD simulation results for SCR X-sections..... | 23 |
| Figure 3.3 TCAD simulation results for SCR temperature..... | 23 |
| Figure 3.4 TCAD simulation results for SCR current flow..... | 24 |
| Figure 3.5 TCAD SCR I-V characteristic..... | 25 |
| Figure 3.6 SCR core TLP testing I-V curve..... | 27 |
| Figure 3.7 SCR IO TLP testing I-V curve..... | 28 |
| Figure 3.8 SCR Vt1 comparison..... | 29 |
| Figure 3.9 SCR Vt2 comparison..... | 29 |
| Figure 3.10 SCR It2 comparison..... | 30 |
| Figure 3.11 SCR Vh comparison..... | 30 |
| Figure 3.12 SCR Ih comparison..... | 31 |
| Figure 3.13 SCR Ron comparison..... | 31 |

| | |
|---|----|
| Figure 3.14 DTSCR Schematic..... | 32 |
| Figure 3.15 STI DTSCR X-section..... | 33 |
| Figure 3.16 Gated DTSCR X-section..... | 33 |
| Figure 3.17 TCAD simulation results for STI DTSCR X-sections..... | 34 |
| Figure 3.18 TCAD simulation results for STI DTSCR temperature..... | 35 |
| Figure 3.19 TCAD simulation results for STI DTSCR current flow..... | 35 |
| Figure 3.20 TCAD STI DTSCR I-V characteristic..... | 36 |
| Figure 3.21 TCAD simulation results for Gated DTSCR X-sections..... | 37 |
| Figure 3.22 TCAD simulation results for Gated DTSCR temperature..... | 37 |
| Figure 3.23 TCAD simulation results for Gated DTSCR current flow..... | 38 |
| Figure 3.24 TCAD Gated DTSCR I-V characteristic..... | 38 |
| Figure 3.25 TCAD SCR I-V characteristic comparison..... | 39 |
| Figure 3.26 TCAD SCR key ESD parameter comparison..... | 40 |
| Figure 3.27 TCAD SCR ESDV..... | 40 |
| Figure 3.28 STI DTSCR core TLP testing I-V curve..... | 42 |
| Figure 3.29 STI DTSCR IO TLP testing I-V curve..... | 43 |
| Figure 3.30 Gated DTSCR IO TLP testing I-V curve..... | 44 |
| Figure 3.31 DTSCR V_{t1} comparison..... | 45 |
| Figure 3.32 DTSCR V_{t2} comparison..... | 46 |
| Figure 3.33 DTSCR I_{t1} comparison..... | 46 |
| Figure 3.34 DTSCR V_h comparison..... | 47 |
| Figure 3.35 DTSCR I_h comparison..... | 47 |
| Figure 3.36 DTSCR R_{on} comparison..... | 48 |
| Figure 4.1 Graphene with crumpling in the third dimension..... | 51 |
| Figure 4.2 Lattice structure and Brillouin zone..... | 51 |
| Figure 4.3 Electronic dispersion in graphene..... | 53 |
| Figure 4.4 Cyclotron mass of grapheme..... | 55 |
| Figure 4.5 Ambipolar electric field effect in grapheme..... | 58 |
| Figure 4.6 Minimum conductivity of graphene..... | 59 |
| Figure 4.7 Chiral quantum Hall effects..... | 61 |
| Figure 4.8 Landau levels..... | 62 |
| Figure 5.1 Cross-section and circuit scenario for the new gNEMS ESD switch.. | 66 |
| Figure 5.2 New CMOS-compatible gNEMS fabrication process flow..... | 67 |
| Figure 5.3 Raman spectroscopy of monolayer graphene grown by CVD..... | 68 |
| Figure 5.4 SEM images of a sample gNEMS switch..... | 69 |
| Figure 5.5 DC sweeping test for sample gNEMS devices shows static switching effect with VON affected by the graphene membrane length (7.0, 7.6, 15, 29.8V). | 70 |
| Figure 5.6 Measured I-V curve by TLP pulsing for a prototype gNEMS device shows transient ESD switching with a fast response time down to 200ps..... | 71 |
| Figure 5.7 Measured I-V curve by TLP for a prototype gNEMS device shows near symmetric I-V switching behaviors desired for ICs..... | 72 |
| Figure 6.1 A conceptual X-section of new vertical magnetic-cored inductors in CMOS back-end..... | 75 |

| | |
|---|----|
| Figure 6.2 Measurements show that the vertical magnetic-cored inductors outperform reported state-of-the-art in L-density and $Q_{max} \cdot f_{max}$ (f_{max} is the frequency at Q_{max})..... | 76 |
| Figure 6.3 Illustration of the new post-CMOS process flow developed to fabricate mL. (a) A spiral inductor in top metal. (b) Patterning and etching by O ₂ plasma. (c) Magnetic material filling. | 77 |
| Figure 6.4 Simplified schematic for the VCO and its equivalent circuit. C1 and C2 are 2.5V nMOS capacitor (tuning range from 2pF to 3.8pF). R _p is around 100Ω at 2.6GHz. | 78 |
| Figure 6.5 Die photo for the LC-VCO (a) and SEM images for the magnetic-cored inductor after removing the passivation layer (b) and nano-particle magnetic material filling (c). | 80 |
| Figure 6.6 Measured inductance of inductors with and without magnetic core shows substantial improvement in L-density across a wide frequency range for the new vertical magnetic inductor. | 81 |
| Figure 6.7 Measured waveform of LC-VCO confirms oscillation (a) with oscillating frequency of $\omega_0 \approx 2.57\text{GHz}$ at $V_{tune} = 2.25\text{V}$ (b)..... | 82 |
| Figure 6.8 Measurement shows a tuning range of 2.24 GHz to 3.01 GHz with V_{tune} changing from 1V to 3V for LC-VCO..... | 83 |
| Figure 6.9 Measured phase noises shows improvement of the VCO using mL over the VCO using regular L with $V_{tune} = 2.25\text{V}$ | 84 |

List of Tables

| | |
|--|----|
| Table 2.1 Designed ESD HBM Levels with Gate Monitor | 20 |
| Table 3.1 SCR dimensions for TCAD simulation | 22 |
| Table 3.2 SCR dimensions for TCAD simulation | 25 |
| Table 3.3 SCR design splits | 26 |
| Table 3.4 SCR core ESD parameters table | 27 |
| Table 3.5 SCR core ESD parameters table | 28 |
| Table 3.6 DTSCR design splits..... | 41 |
| Table 3.7 STI DTSCR core ESD parameters table..... | 42 |
| Table 3.8 STI DTSCR IO ESD parameters table | 43 |
| Table 3.9 Gated DTSCR IO ESD parameters table | 44 |
| Table 6.1 Measured key Specs for VCOs with regular L and mL..... | 83 |

Chapter 1 General ESD Protection Design

1.1 ESD Failure Problem

ESD (electrostatic discharge) is an extremely fast discharging phenomenon occurring when two charged objects are brought into proximity and electrostatic charges transfer in between [1]. The resulting high current (to 40Amps) and high voltage (to 20KV) may damage or degrade IC (integrated circuit) parts [1]. ESD damages consist of catastrophic and latent failures with the former causing immediate IC malfunction due to thermal breakdown or MOSFET gate dielectric rupture and the latter causing IC degradation and future failure. ESD-induced failures become one of most important reliability problems in the semiconductor IC field. According to industry statistics, ESD induced damages account for 35-50% of all IC field failures, resulting in billions of dollars of loss annually to the IC industry.

As IC technologies continue advance into sub-100nm domain, on-chip ESD protection circuit design rapidly emerges as a major design challenge, particularly for parasitic sensitive analog, mixed-signal (AMS) and multi-GHz RF ICs [2]. In principle, on-chip ESD protection works in the way that an ESD protection unit is connected between a pair of IC pins facing ESD stresses, e.g., I/O to ground (GND). The ESD protection structure remains off in normal IC operation. When an ESD transient appears at the I/O pin, it will trigger the ESD protection unit and form a low-impedance conducting path to shunt the large ESD current efficiently without generating too much heat and to clamp the I/O voltage to a sufficiently low level to avoid any dielectric rupture, hence provides ESD protection.

Figure 1.1 illustrates a typical snapback I-V characteristic for an ESD protection structure where ESD-critical parameters are defined for triggering threshold (V_{t1} , I_{t1} , t_1), holding point (V_h , I_h), discharging impedance (R_{on}) and thermal breakdown (V_{t2} , I_{t2}).

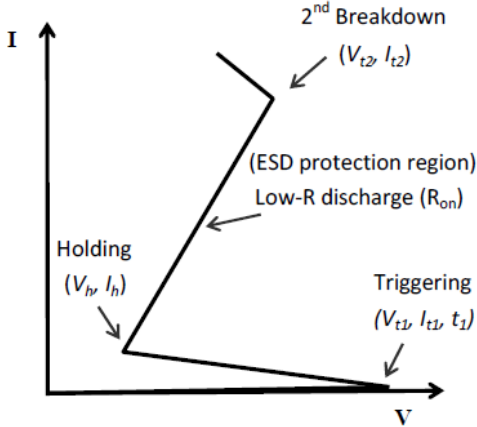


Figure 1.1 Typical I-V curve shows ESD-critical parameters.

1.2 ESD Protection Design Window

Proper ESD protection requires comprehensive design consideration in practices. Firstly, the V_{t1} of ESD protection structure must be lower than the breakdown voltage of the protection node (e.g., $BVDSS$ for drain and BVG for gate in CMOS) by a safety margin. Secondly, its V_h should be higher than the supply voltage (V_{DD}) by a safety margin to avoid possible latch-up of ESD protection structures. Thirdly, the I_h of ESD protection device should be higher than the total supply currents (I_{DD}) on a chip to further prevent possible latch-up effect. These critical design boundaries establish a design window for good ESD protection design as illustrated in Figure 1.2 [3].

The emerging challenge is that, as IC technologies continue to advance into sub-100nm domain, this ESD design window becomes narrower when using traditional ESD

protection structures. Therefore, it is imperative to explore novel non-traditional ESD protection structures and triggering-assisting circuitry to effectively keep a suitable ESD protection design window in practical designs, which makes today's ESD protection design fairly complicated.

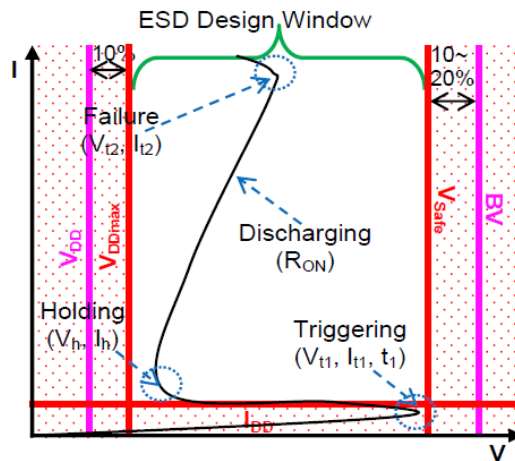


Figure 1.2 An ESD protection design window

1.3 ESD Protection Device Solutions

1.3.1 Diode in ESD Protection Operation

As an ESD protection device, a diode can be operated in both forward and reverse biasing regions. Figure 1.3 shows a typical diode I-V characteristic. In forward-biasing condition, a diode starts to conduct significant current after turn-on, typically at $V_{on} \sim 0.65V$ for silicon diode. In forward-biasing mode, the diode is operating in high-current mode, which is actually the case for all devices under ESD protection. Under high-current condition, both drift and diffusion current components must be considered. Further, the potential drop across the intrinsic PN junction becomes insignificant

compared to the ohmic drop over the diode series resistance, under high injection. Hence, the diode I-V characteristic in ESD events can be approximated.

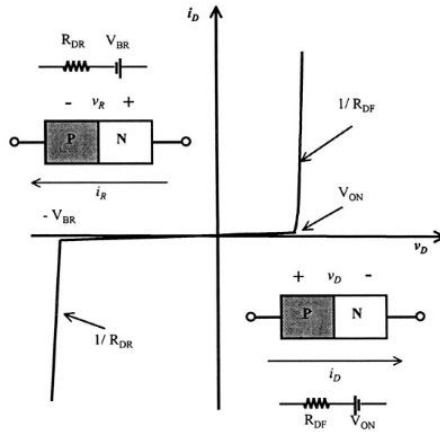


Figure 1.3 Typical diode I-V characteristics.

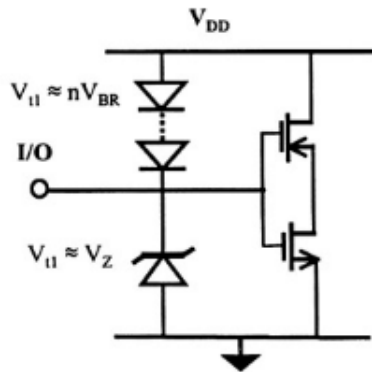


Figure 1.4 Typical diode ESD protection schemes.

Typical diode ESD protection scheme is illustrated in Figure 1.4 for both forward and reverse biasing modes. Because of its low forward turn-on voltage, single forward diode normally cannot be used as ESD protection device for power supply of $V_{dd} > 5V$. A diode string can be used instead with the number of diodes in the chain depending upon IC chips. In contrast to forward-biasing mode, a reverse connected diode is the

simplest ESD protection solution, where its triggering voltage V_{t1} , is determined by reverse breakdown voltage V_{br} .

1.3.2 BJT in ESD Protection Operation

A BJT normally works in a snapback mode as an ESD protection device. Typical BJT ESD protection schemes are illustrated in Figure 1.5, where the collector of a BJT is connected to an I/O pad. As a positive ESD pulse comes to the I/O pad with respect to the V_{ss} , collector junction of BJT Q_2 is reverse-biased to its breakdown. After avalanche multiplication takes off at collector, V_{be} increases and Q_2 is turned on. V_c starts to decrease and Q_2 moves into snapback region. If a negative ESD pulse appears at the I/O pad with reference to the V_{ss} , BE junction diode will be forward turned on to form a shunt path.

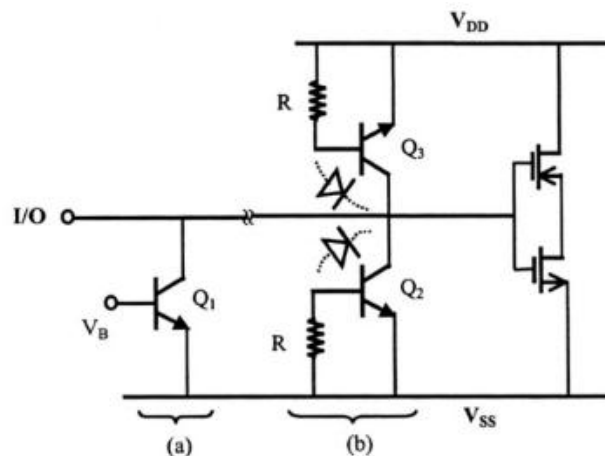


Figure 1.5 Typical BJT ESD protection schemes.

1.3.3 MOSFET in ESD Protection Operation

One of the simplest MOS ESD protection devices is the so-called grounded-gate NMOS (ggNMOS) structure, where the drain (D) goes to an I/O pad and the gate (G), source (S) and body (B) are shorted together to ground. Figure 1.6 illustrates its typical cross-section and equivalent circuit. The principle of a ggNMOSFET in ESD protection operation follows.

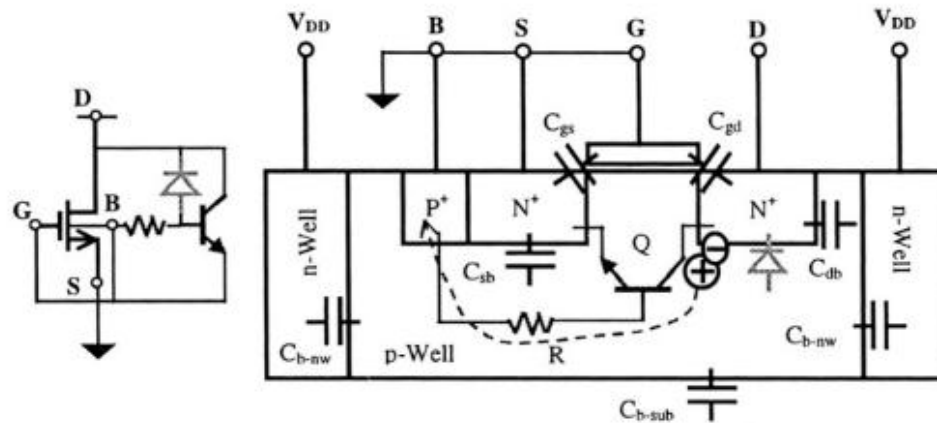


Figure 1.6 Typical GGMOS cross-section and equivalent circuit.

As a positive ESD transient appears at an I/O pad, the DB junction is reverse-biased all the way to its breakdown. After avalanche multiplication takes place, a potential V_r is built up and the BS junction turns on, eventually triggers the parasitic lateral NPN transistor Q. As a negative ESD pulse comes to the I/O pad, a forward-biased parasitic diode, BD, will take the role to shunt the transient.

Figure 1.7 illustrates a typical ESD protection scheme for an I/O pad, where the I/O-to-V_{DD} protection resorts to a ggPMOS device.

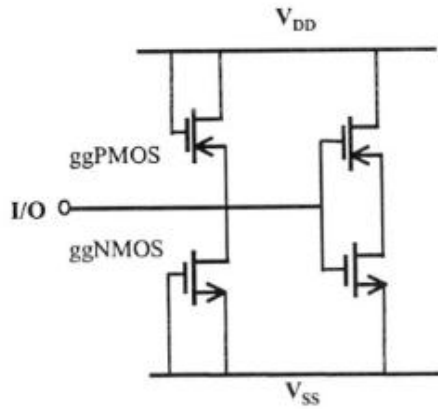


Figure 1.7 Typical GG MOS ESD protection schemes.

1.3.4 SCR in ESD Protection Operation

Silicon controlled rectifier (SCR) device may be one of the most efficient structure in terms of ESD protection because of its deep snapback I-V characteristics, which enables it to handle large current transients. A simple SCR-based ESD protection structure and its equivalent circuit, as shown in Figure 1.8, is discussed here.

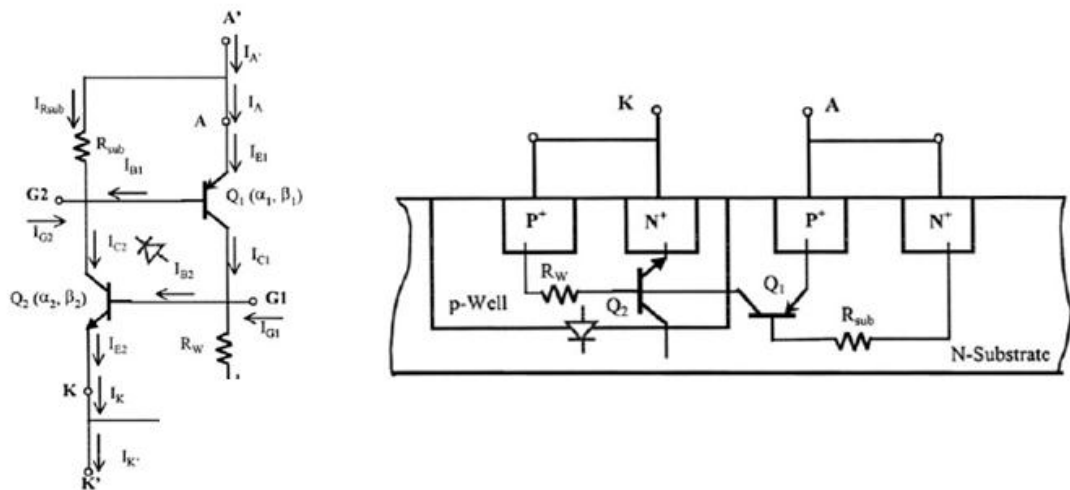


Figure 1.8 Typical SCR equivalent circuit and typical cross-section

The principle of a SCR in ESD protection operation follows. As a positive ESD transient appears at the I/O pad with respect to GND, the SCR is pushed into regeneration mode to form a low-impedance discharge channel to shunt the ESD current safely. A brief regeneration mechanism is that, collector current of Q1 supplies base current for Q2 and push it into active mode; in turn, Collector current of Q2 sources base current for Q1. As a negative ESD pulse comes to I/O pad with respect to GND, a large parasitic diode of p-well/n-sub will be forward turned on and takes the charge.

1.4 Whole-Chip ESD Protection

It is critical to point out that ESD protection design is application-specific and portability shall not be expected in practical designs, in other word, there is not any universal ESD protection solution. Importantly, ESD protection design is a whole-chip design task as opposed to designing stand-alone ESD protection devices.

Ideally, a good practical ESD protection solution must ensure complete ESD protection for the whole IC chip as illustrated in Figure 1.10 for a mixed-signal chip where ESD protection structures are used for all I/O pad to protect against all possible ESD pulse modes, i.e., positive (PD) and negative (ND) to VDD, and positive (PS) and negative (NS) to VSS, as well as a number of power clamping devices for all supply lines to defend against possible ESD surges from VDD to VSS (DS) or vice verse (SD). While practical IC products may adopt partial ESD protection only, full-chip complete ESD protection scheme shall be ideal and should be considered with allowed costs and parasitic effects.

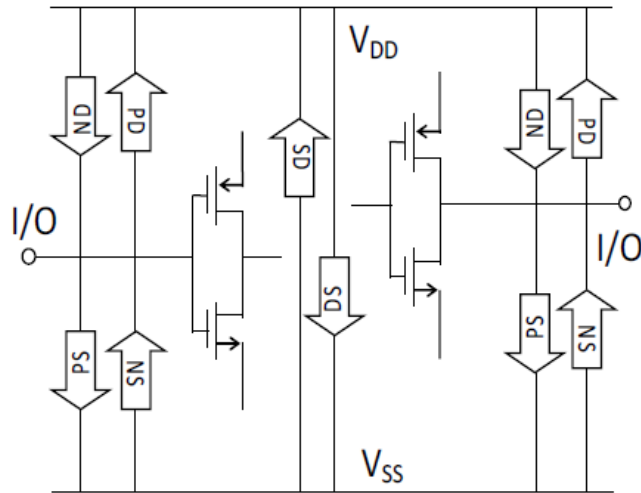


Figure 1.9 Complete full-chip ESD protection scheme.

As shown in Figure 1.9, if traditional one-directional ESD protection devices are used, multiple ESD protection units may be needed to ensure all-active low-impedance full-chip ESD protection, resulting in significant ESD-induced parasitic effects and large Si area used. Hence, novel multi-directional ESD protection structures are desired [2].

Chapter 2 ESD-protected Monitor Circuits

2.1 ESD Protection at Sub-32nm Node

ESD failure has become a major design barrier as semiconductor IC technologies advance into sub-32nm nodes. ESD protection capability, layout size and ESD-induced parasitic effects are important design factors to consider. The popular ESD protection structures, such as, FET, SCR and diode, and their derivatives, may or may not be suitable for ESD protection at sub-32nm [2]. The key ESD design tasks are: First, accurate ESD protection design and optimization must be ensured by ESD simulation in design phase. Second, systematic ESD characterization is required to evaluate various ESD protection devices. Third, suitable ESD-protected I/O dummy monitor circuits are used to evaluate ESD protection capability and suitability for general ICs. Various simple diode ESD protection structures are designed by mixed-mode ESD simulation and conducted comprehensive TLP ESD characterization for both individual ESD diodes and ESD-protected monitor circuit blocks. The goal is to provide practical design guidelines for robust ESD protection circuit design at 28nm node and beyond.

2.2 Diode ESD Design in 28nm CMOS

While research is on-going to explore novel non-traditional ESD protection solutions for sub-32nm technologies [8, 9, 10], diode based ESD remains attractive to IC designers due to its capability and simplicity [11]. Based on its process features, a group of various diode ESD protection structures were designed in the 28nm CMOS for comparison.

Fig 2.1 illustrates the cross-section of N+/P-well STI diode ESD structure designed, where the N+ diffusion (Cathode) and P+/P-well diffusion (Anode) are separated by STI. Since STI has very short dimension, STI diode ESD structures can be made very small, hence reduce ESD-induced parasitic effects and alleviate ESD layout burden. On the negative end, with a narrow and sharp STI plug, the large ESD discharge current has to make sharp turns in conduction, resulting in severe current crowding at the bottom of a STI plug that affects ESD protection capability. The foundry 28nm CMOS offers both core (0.85V) and I/O (1.8V) process modules. Accordingly, STI diode ESD devices in both core and I/O processes are designed with finger width 60um, 100um, 120um for comparison studies.

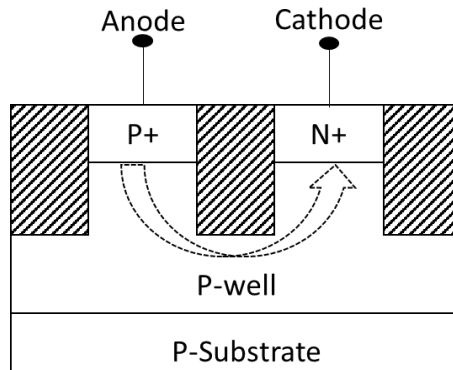


Figure 2.1 Cross-section and ESD discharge path for an N+/P-well STI diode ESD device. ESD current crowding at STI reduces ESD protection capability.

Fig 2.2 depicts the cross-section of a gated diode ESD structure where a poly gate is used to isolate the cathode (N+) and anode (P+) instead of using a conventional STI plug. There are two main advantages for the gated-diode ESD device. First, the large ESD current can conduct straightly through the channel between the N+ and P+ without any sharp turning and current crowding as seen in an STI diode ESD device. Second, the

ESD discharge is extremely short as defined by the 28nm CMOS channel. Hence, the ESD protection capability for a gated-diode ESD device shall be stronger than that of a STI diode ESD structure, which is confirmed in testing. In ESD design, the gate must be properly biased for a gated-diode ESD device in order to avoid unexpected channel turn-on in normal IC operation. Nevertheless, relatively higher leakage current may be expected for such gated-diode ESD protection devices. Gated diode with finger width 60um, 100um, 120um is designed for comparison.

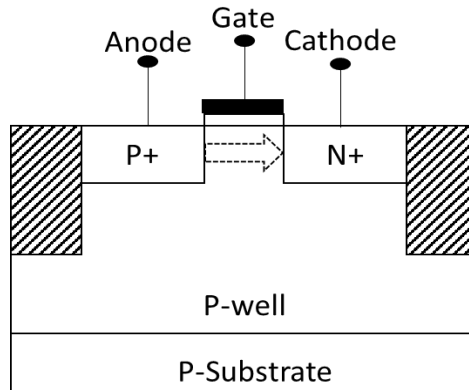


Figure 2.2 Cross-section and ESD current discharging path for a poly-gated diode ESD protection structure.

2.3 ESD Design with Dummy Monitor

Practically, it is common that an ESD structure designed and tested as an individual ESD device works well, however, fails on chip. ESD-circuit co-design is critical for success of chip level ESD protection circuit design because complex ESD to circuit interactions exist [2]. Co-design becomes essential to 28nm ESD design due to more unexpected interaction effects.

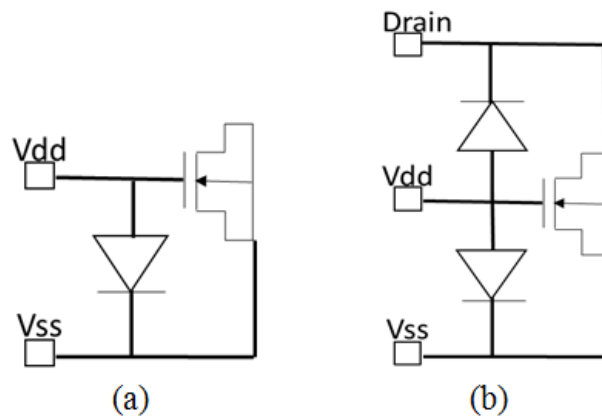


Figure 2.3 Schematics for ESD dummy gate monitor circuits: (a) gate ESD testing monitor only, and (b) gate ESD monitor and MOSFET I-V testing circuit.

To ensure successful on-chip ESD protection for general circuit protection, a couple of ESD monitor dummy circuit blocks in 28nm CMOS is designed to evaluate ESD performance at chip level [4]. While such dummy monitor circuits are not for any specific circuit, it considers critical CMOS gate breakdown risks for general circuits. Fig 2.3 illustrates the schematics for the two dummy ESD gate monitor circuit blocks. Fig 2.3a is designed to evaluate ESD protection to the gate by ESD stressing test. The dummy monitor circuit in Fig 2.3b allows both ESD protection testing and general MOSFET I-V characterization before and after ESD stressing, so that any potential ESD damage to the MOSFET may be evaluated in terms of its I-V behaviors. This circuit level ESD design helps to determine if a given ESD diode device would provide required ESD protection at chip level. This is a critical ESD design aspect, which may often be ignored by IC designers in real world circuit designs.

Core NFET with area $0.5\mu\text{m}^2$ and IO NFET with area $30\mu\text{m}^2$ is used as gate monitor for core/IO ESD devices respectively. Gate leakage current for core and IO gate monitor is tested to be 596.17pA and 1.16pA using Agilent 4156C parameter analyzer.

2.3.1 ESD Behavior Modeling

Whole-chip ESD protection circuit simulation is essential to chip-level ESD protection design synthesis, optimization, verification and prediction. Today, trial-and-error approaches still dominate in practical ESD circuit designs due to lack of accurate ESD device modeling technique, which is very challenging due to the extremely complex ESD discharging behaviors. A new ESD behavior modeling technique is developed to overcome the difficulties to extract complicated parameters based on high current and thermal physics [5,6,7]. The new ESD behavior modeling technique utilizes Verilog-A to describe complicated ESD discharging behavior by ESD-critical parameters extracted from ESD I-V curves by TLP testing. After extracting ESD-critical parameters from TLP testing results and analysis, a scalability model per device dimensions can be set up. Then the TLP curves are divided into several section-wise segments according to ESD functions. Each segment of the TLP testing curve can be modeled by a formula to describe the corresponding ESD function in Verilog-A and the fitting parameters can be extracted from the TLP curve directly correlated with device dimensions. An accurate scalable ESD behavior model is then obtained.

Such modeling technique is used here to extract gated diode model using single gated diode TLP testing results. Then SPICE simulation of HBM zapping is conducted

for the dummy ESD gate monitor circuit blocks in Fig 2.4 using the extracted gated diode models. Fig 2.5 shows simulated ESD discharging I-V characteristics for one sample dummy ESD gate monitor circuit shown in Fig 2.3a, which confirms the designed ESD protection behaviors. This circuit level ESD simulation helps to determine if a given ESD diode device, though already being confirmed in ESD simulation for an individual ESD device, would provide required ESD protection at chip level. This is a critical ESD design aspect, which may often be ignored by IC designers in real world circuit designs.

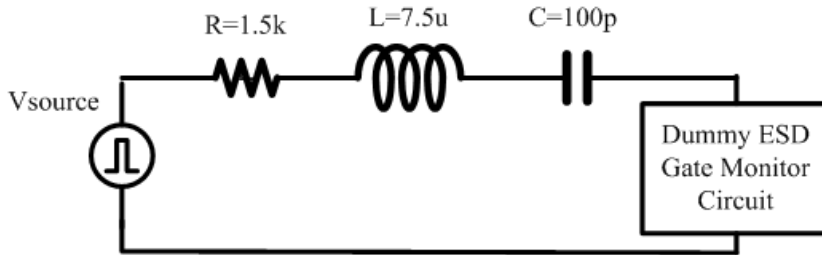


Figure 2.4 ESD gate monitor circuit simulation schematic.

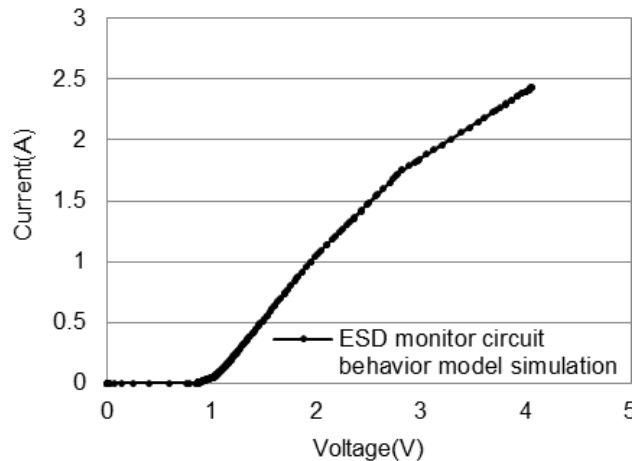


Figure 2.5 Simulated ESD I-V curve for a gated diode 60um dummy ESD gate monitor circuit using behavior models.

2.3.2 Dummy Monitor Circuit Measurements Analysis

A large set of diode ESD protection structures of various layout dimensions and connections, including STI diodes in core and I/O processes, as well as poly gated diodes, were designed and fabricated in a foundry 28nm high-performance CMOS technology. Comprehensive ESD characterization was conducted for all fabricated ESD structures using TLP tester (Barth Model 4002+) for transient ESD discharging evaluation, which provides all ESD-critical parameters and ESD-induced leakage current.

As discussed before, to ensure whole-chip ESD protection, circuit level ESD characterization is required in addition to evaluating individual ESD protection devices. TLP testing for ESD devices with (Fig 2.3a) and without dummy gate monitor are conducted to get I_{t2} values for comparison. If I_{t2} with gate monitor is almost the same as single ESD device, the designed ESD device has the full ability to protect the gate monitor. The ESD device breakdown happens before the gate monitor. Otherwise, gate monitor is already damaged and ESD device cannot fulfill its discharging ability.

Fig 2.6, 2.7, 2.8 depicts the measured ESD I-V behaviors for sample stand-alone N+/P-well STI core, I/O diode and gated diode ESD device of 60 μ m and its corresponding dummy ESD gate monitor circuit as shown in Fig 2.3a. It is clearly observed that I_{t2} level for all three cases with and without gate monitor is similar, which shows good protecting ability of designed diodes. I_{t2} level is also the same for finger width 100 μ m and 120 μ m. Due to extra core gate leakage associated to the dummy MOSFET, relatively higher leakage current was observed for the ESD core gate monitor circuit, which was expected.

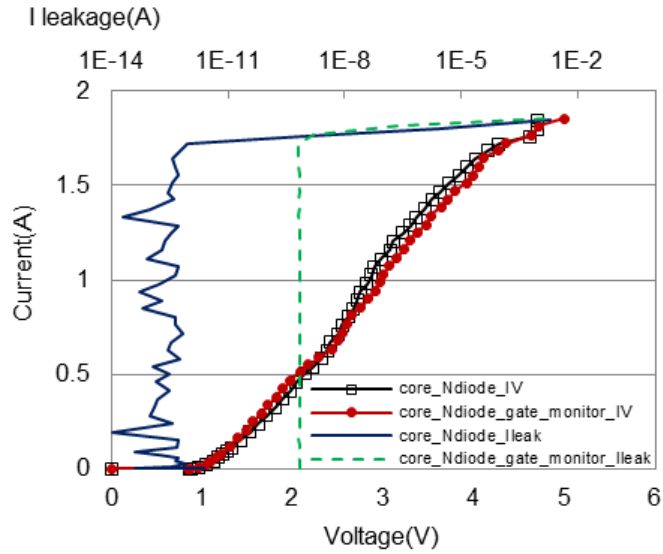


Figure 2.6 Measured ESD discharging curves by TLP testing for STI N diode designed in core process (W=60μm) with and without gate monitor.

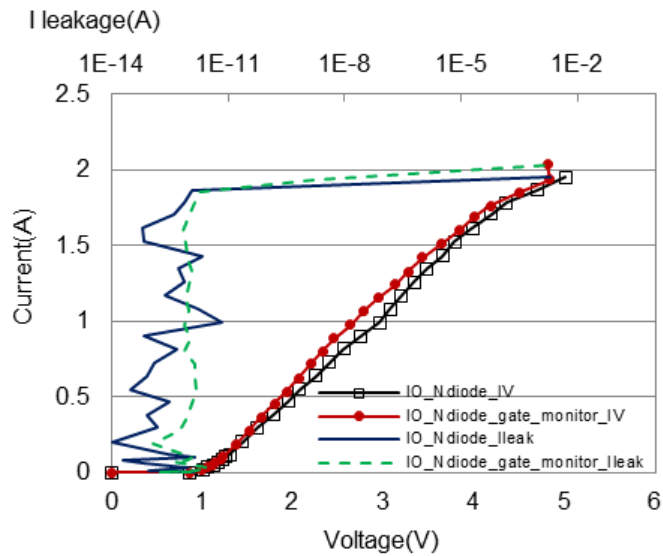


Figure 2.7 Measured ESD discharging curves by TLP testing for STI N diode designed in I/O process (W=60μm) with and without gate monitor.

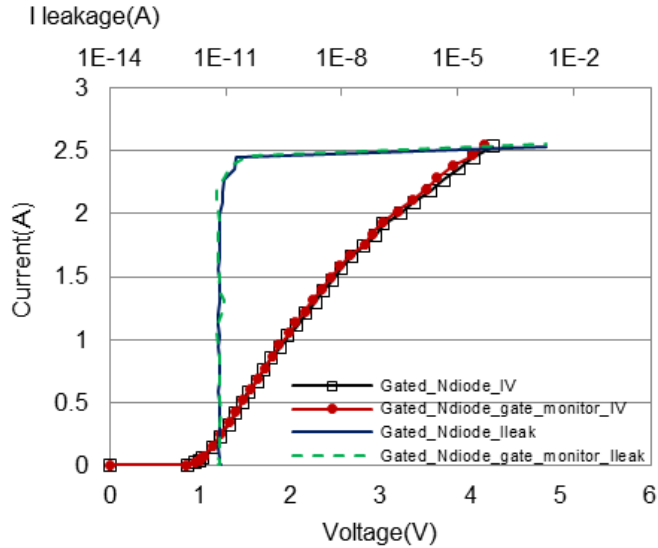


Figure 2.8 Measured ESD discharging curves by TLP testing for gated N diode designed in I/O process ($W=60\mu\text{m}$) with and without gate monitor.

P+/N-well STI core, I/O diode and gated diode ESD structures with and without gate monitor are also tested by TLP. ESD I-V behaviors for core P diode with finger width 60um, 100um and 120 um are shown in Fig 2.9. More testing results show that I_{t2} level for different finger width and technology have good consistency with and without dummy gate ESD testing monitor.

Testing results with gate ESD testing monitor only has demonstrated that core/IO STI and gated N+/P-well & P+/N-well diode with different width 60um, 100um and 120um have full ability to protect the gate oxide. Dummy monitor circuit with 3 pads (Fig 2.3b) could further proven the ESD protection abilities by conducting MOSFET IV testing. Setting gate voltage equal to 0.5V, I_d - V_{ds} is measured before and after TLP testing by Agilent 4156C. Comparisons between two IV curves show whether gate monitor still have good function after TLP testing.

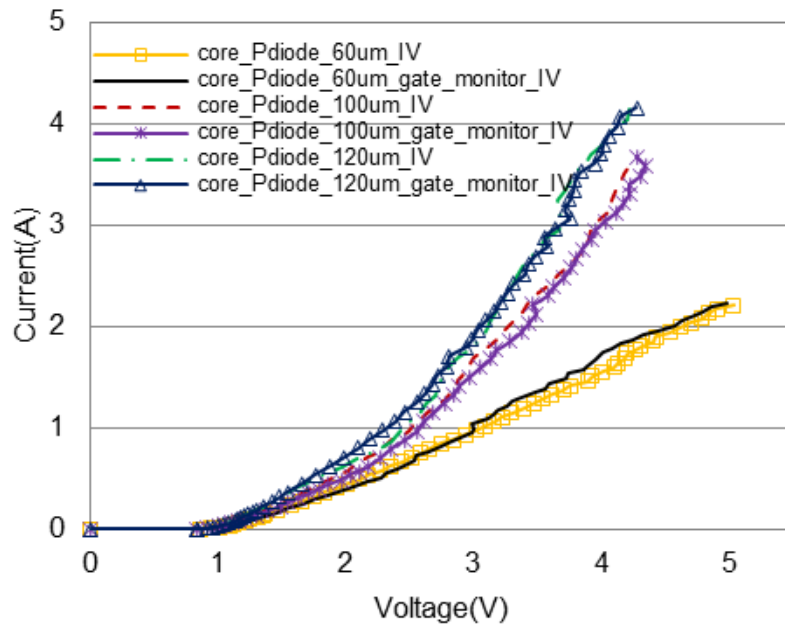


Figure 2.9 Measured ESD discharging I-V curves by TLP testing for STI P diode designed in core process with and without gate monitor with finger width 60um, 100um and 120um.

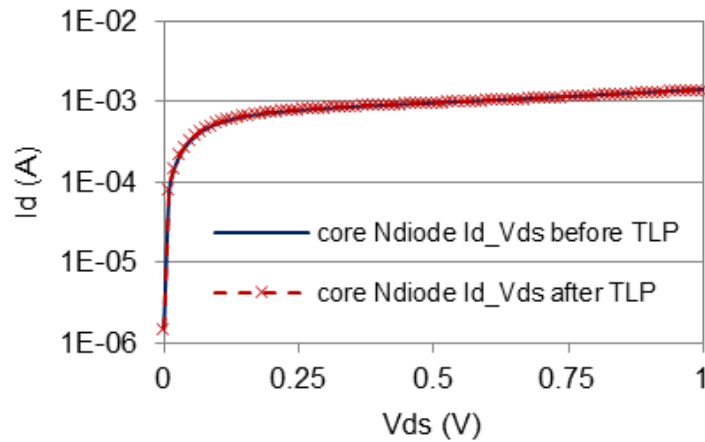


Figure 2.10 Measured I_d - V_{ds} curves before and after TLP testing for STI N diode 120um designed in core process.

I_d - V_{ds} testing results for core/IO STI and gated N+/P-well & P+/N-well diode with finger width 120um have shown no significant changes before and after the TLP testing. As an example, Fig 2.10 is the core N diode 120um IV comparison. Testing

results further proven that gate monitor function is not influenced by TLP testing. The designed ESD HBM levels are shown in Table 2.1 with full ability to protect the core circuit.

| ESD Device Type | | Finger Width (um) | HBM ESDV with Gate Monitor |
|-----------------|----------------|-------------------|----------------------------|
| STI Diode | Core N+/P-Well | 120 | 5KV |
| | Core P+/N-Well | 120 | 6KV |
| | IO N+/P-Well | 120 | 5.5KV |
| | IO P+/N-Well | 120 | 6KV |
| Gated Diode | N+/P-Well | 120 | 7KV |
| | P+/N-Well | 120 | 7KV |

Table 2.1 Designed ESD HBM Levels with Gate Monitor

2.4 Conclusion

A comprehensive design and analysis of STI and gated diode ESD protection structures with dummy circuit monitor in 28nm CMOS is studied. Mixed-mode ESD simulation can predict chip level ESD protection performance using behavior models. The dummy ESD gate monitor circuit blocks were characterized by TLP testing. HBM protection capability of 5KV, 5.5KV, 7KV are obtained for STI core, I/O and gated I/O N+/P-well diodes, 6KV, 6KV, 7KV for STI core, I/O and gated I/O P+/N-well diodes, respectively. The ESD protection design technique and results shall be useful to IC designs at 28nm node and beyond.

Chapter 3 SCR ESD Design

3.1 SCR for ESD Protection Design

SCR is commonly used as ESD protection devices for its several advantages. First, SCR have very high current handling and excellent voltage clamping capabilities. When SCR is on, two intrinsic parasitic BJT all turned on so it has deep snapback I-V characteristic. Second, SCR have low dynamic on resistance and thus high failure current, which makes it perfect candidate for high ESD protection level applications. Last is the area efficiency. SCR only consumes small die area due to its large current handling ability. There are also some drawbacks for SCR, such as very high trigger voltage, causing SCR itself could only be used in HV designs. Also possible latch up may also be an issue caused by low holding current and voltage. Attention need to be paid here in order to avoid latch up. Overshoot may happen under fast ESD pulse like CDM due to SCR relatively low trigger speed. Overall, SCR have certain advantages other than all other MOS and diode based devices, so careful design is needed here to fulfil it and also avoid the latch up and overshoot issues.

3.2 SCR Design for CMOS 28nm Technology

A wild range stand-alone SCR ESD structures which cover different levels of ESD protection is designed at 28nm CMOS technology. TCAD simulation and layout has been implemented for all of these SCR ESD structures. Full characterization of TLP testing has been conducted according to the test plan. Testing results have been analyzed thoroughly for different ESD structures which satisfy different protection level. Critical

ESD parameters, including trigger voltage, holding voltage, Ron, breakdown current, leakage, have been characterized for the 28nm process. So ESD protection ability relationship with different SCR size has been established. Also ESD protection ability relationship with different SCR type ESD device for the same size has been established.

3.2.1 SCR TCAD Simulation Guidelines

TCAD simulation could provide insights as guidelines for ESD designer. From TCAD simulation results, device doping cross section, current density, current flow, temperature information are obtained. By adding ESD pulse current waveforms, IV curve results could be used to analyze key ESD parameters such as trigger and holding points. Minimum width for certain ESD level gives designer some prediction and guidelines.

TCAD simulation is done for several SCR splits. By changing the width and length of different ESD device region, ESD critical parameters will also be different to provide the insights. One example of SCR TCAD simulation guidelines is shown here. SCR cross section is shown at Fig 3.1. N2 length as a varying parameter with range from 200nm to 2um, all other parameters remain constant at Table 3.1. TCAD simulation results for N2 length 200nm and 2um under 2KV HBM pulse at 12ns is demonstrated to provide design guidelines. X-section, temperature, current flow are shown in Fig 3.2, Fig 3.3 and Fig 3.4. 200nm case is at right side while 2um case is at left.

| N1 | P1 | P2 | STI1 | STI2 | STI3 | Width |
|-----|-----|-----|-------|------|------|-------|
| 1um | 1um | 1um | 100nm | 1um | 1um | 100um |

Table 3.1 SCR dimensions for TCAD simulation

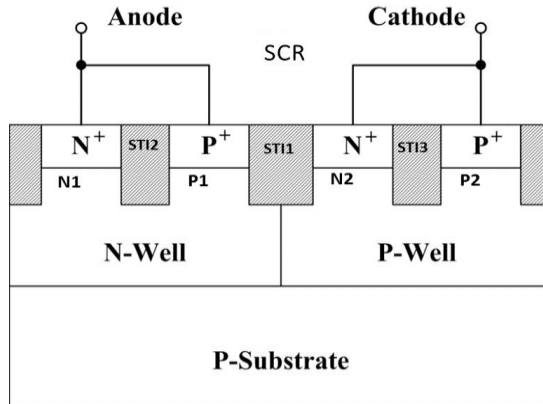


Figure 3.1 SCR X-section

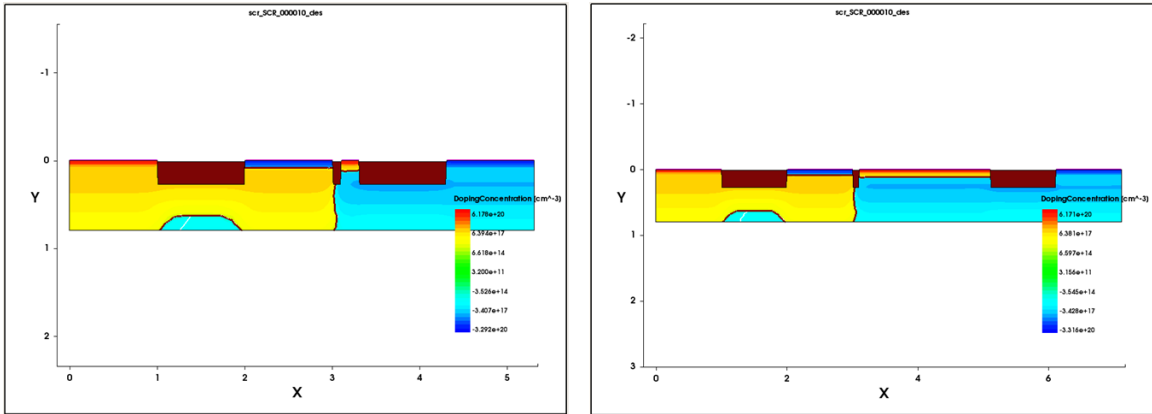


Figure 3.2 TCAD simulation results for SCR X-sections

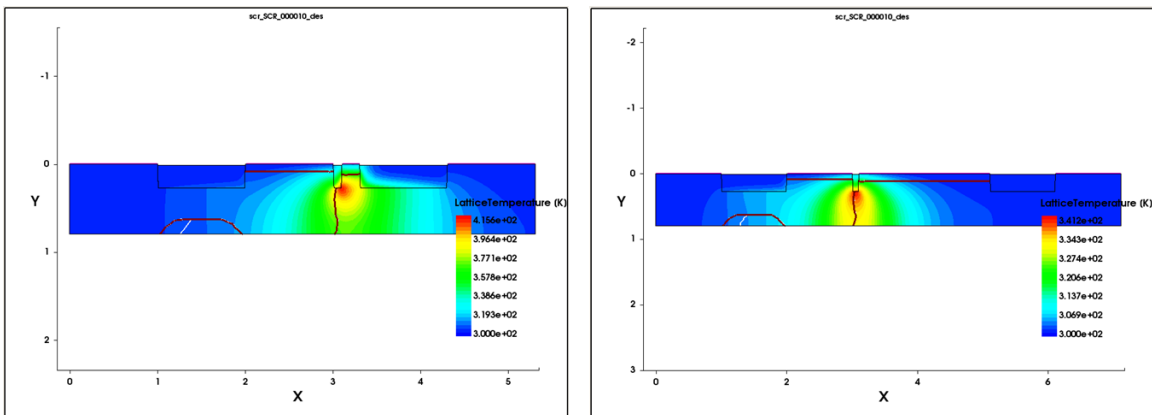


Figure 3.3 TCAD simulation results for SCR temperature

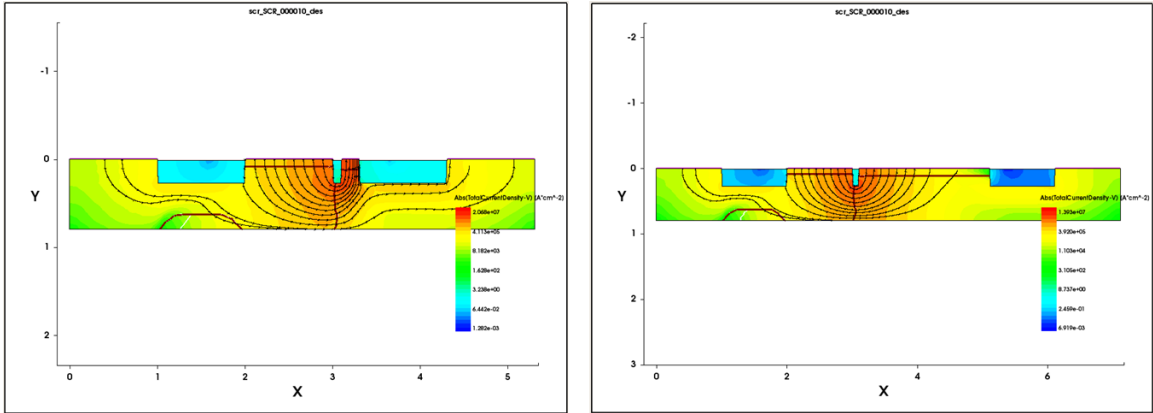


Figure 3.4 TCAD simulation results for SCR current flow

From X-section it clearly shows the P+, NW, N+, PW regions in SCR, which confirms that the correct device simulation results are completed. HBM current waveform is then applied to the simulated SCR device. Temperature comparison proves that when there is not enough N2 length, hot spot will formed at one side of the STI, makes it very vulnerable to high ESD pulsed. For the 2nm N2 length case, the hot spot is well distributed underneath the STI in the middle, which could dissipate the heat evenly through the silicon substrate. And heat and power is the main cause for HBM failure. Designer should make sure that N2 length is enough to get sufficient ESD protection levels. Current flow curves also confirmed this observation. 200nm case the current is too crowded at the N+ side. Another finding is that 2nm will be overdesign for the SCR N2 length, since the current flows mainly at the left side of N+. Too much N2 length will be a waste of die area.

Four N2 cases 200nm, 500nm, 1um, 2um are simulated under HBM 2KV waveforms. TCAD simulation results of HBM 2KV I-V characteristic is displayed in Fig 3.5. Key ESD parameters are extracted in Table 3.2.

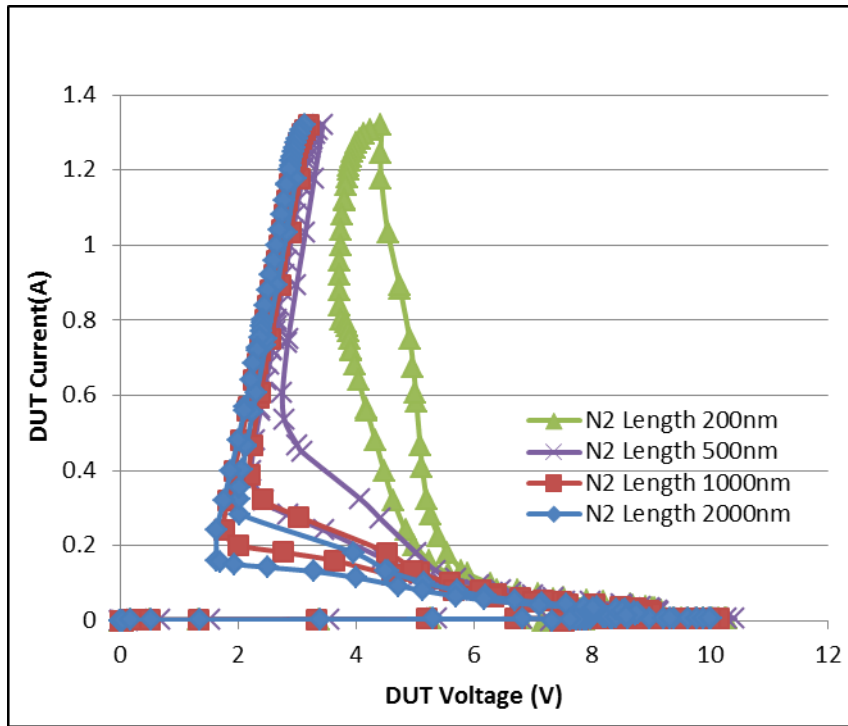


Figure 3.5 TCAD SCR I-V characteristic

| SCR IO | Width (um) | Vt1 (V) | Vt2 (V) | Vh (V) | Ron (ohm) |
|------------------|------------|---------|---------|--------|-----------|
| N2 Length 200nm | 100 | 10.3 | 4.41 | - | - |
| N2 Length 500nm | 100 | 10.4 | 3.43 | 2.75 | 0.992457 |
| N2 Length 1000nm | 100 | 10.1 | 3.19 | 2.2 | 1.112471 |
| N2 Length 2000nm | 100 | 10 | 3.12 | 2.01 | 1.158346 |

Table 3.2 SCR dimensions for TCAD simulation

From the IV curve, as N2 length increases, holding voltage decreases. This demonstrated that SCR need enough N2 length in order to trigger, if N2 length is too small, then two parasitic BJT cannot be triggered and SCR high current handling ability cannot be used. Minimum width for 4 cases at HBM 2KV are simulated. The results

show ESD protection level increases as N2 length increases, which is in line with the temperature simulation results.

To use TCAD simulation as guild lines, 1um is chosen as the final layout size for SCR. Since from the IV curve, 1um and 2um case does not show significant differences. The good impact of longer N2 is saturated at around 1um. If use 2um for design, it will consume too much area also could induce large ESD parasitic capacitance which is not desirable for core IC designs.

3.2.2 Core SCR Testing Results

SCR is designed in both core and IO technology using 28nm process. Different SCR width is used for various ESD protection levels. SCR design splits are shown in Table 3.3.

| ID# | Name | STI 2/3 (um) | STI 1 (um) | P1/2 (um) | N1/2 (um) | Width (um) |
|-----|----------|--------------|------------|-----------|-----------|------------|
| 1 | SCR_core | 1 | 0.5 | 1 | 1 | 25 |
| 2 | | 1 | 0.5 | 1 | 1 | 50 |
| 3 | | 1 | 0.5 | 1 | 1 | 75 |
| 4 | SCR_IO | 1 | 0.5 | 1 | 1 | 25 |
| 5 | | 1 | 0.5 | 1 | 1 | 50 |
| 6 | | 1 | 0.5 | 1 | 1 | 75 |

Table 3.3 SCR design splits

Figure 3.6 shows the I-V curve of TLP testing [12] and Table 3.4 shows the critical parameters which representing the ESD performance of SCR core in 1/2/3 KV. All ESD level protection has been realized from the results. Trigger voltage for SCR in 28nm core process is around 12.5V. Holding voltage around 3.5V proved deep snapback and SCR is turned on. Meanwhile, with wider width of high ESD protection level, Ron is decreased from 2.96V to 1.33V.

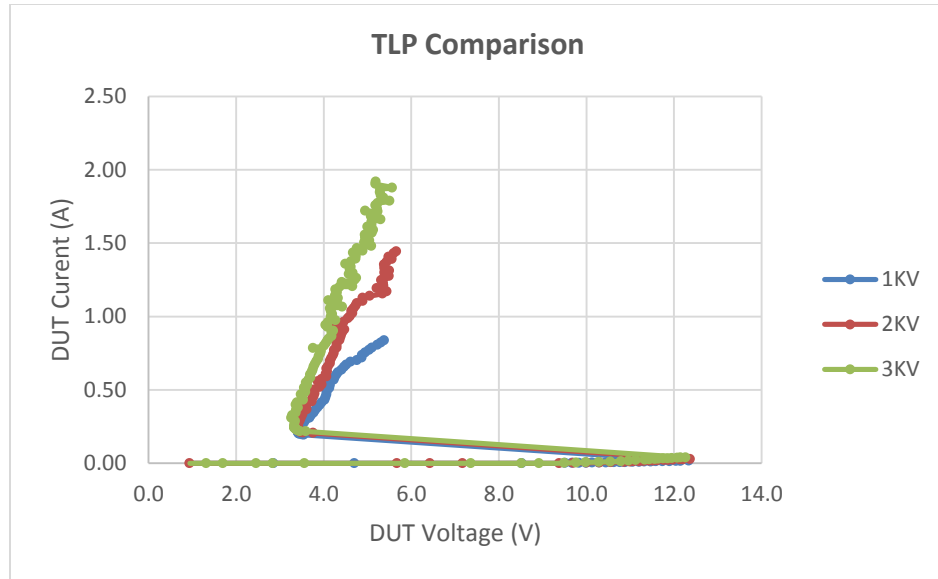


Figure 3.6 SCR core TLP testing I-V curve

| Name | Vt1 (V) | Vt2 (V) | It2 (A) | Vh (V) | Ih (A) | Ron (Ohm) | Area* (um ²) |
|--------------|---------|---------|---------|--------|--------|-----------|--------------------------|
| SCR core 1KV | 12.33 | 5.38 | 0.84 | 3.41 | 0.21 | 2.96 | 6.63*25.36 |
| SCR core 2KV | 12.36 | 5.65 | 1.44 | 3.41 | 0.22 | 1.92 | 6.63*50.36 |
| SCR core 3KV | 12.26 | 5.19 | 1.92 | 3.32 | 0.24 | 1.33 | 6.63*75.36 |

Table 3.4 SCR core ESD parameters table

3.2.3 IO SCR Testing Results

Figure 3.7 shows the I-V curve of TLP testing and Table 3.5 shows the critical parameters which representing the ESD performance of SCR IO in 1/2/3 KV. All ESD level protection has been realized from the results. Trigger voltage for SCR in 28nm core process is around 12.5V. Holding voltage around 3.5V proved deep snapback and SCR is turned on. Meanwhile, with wider width of high ESD protection level, Ron is decreased from 2.93V to 0.86V.

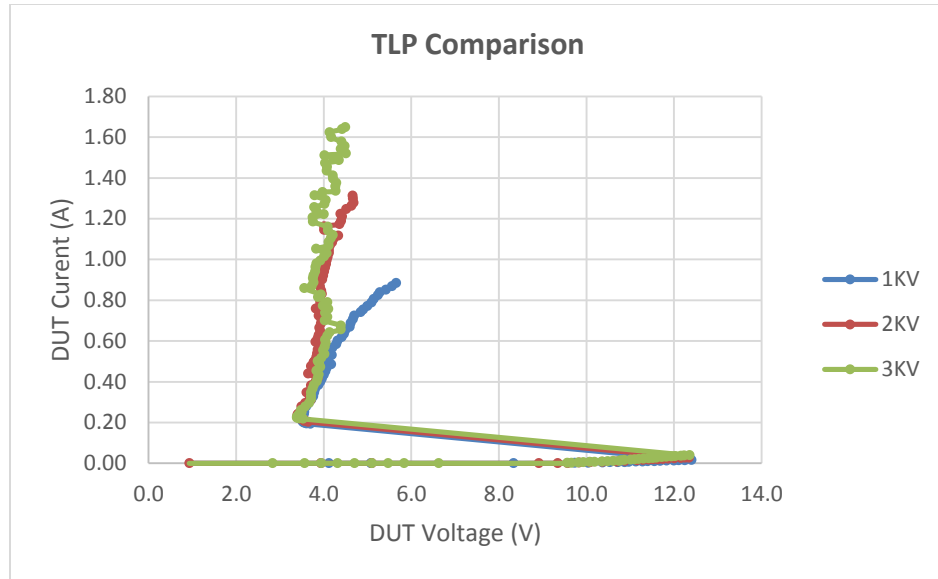


Figure 3.7 SCR IO TLP testing I-V curve

| Name | Vt1 (V) | Vt2 (V) | It2 (A) | Vh (V) | Ih (A) | Ron (Ohm) | Area* (um ²) |
|------------|---------|---------|---------|--------|--------|-----------|--------------------------|
| SCR IO 1KV | 12.40 | 5.66 | 0.88 | 3.50 | 0.22 | 2.93 | 6.63*25.36 |
| SCR IO 2KV | 12.34 | 4.66 | 1.31 | 3.42 | 0.23 | 1.01 | 6.63*50.36 |
| SCR IO 3KV | 12.36 | 4.49 | 1.65 | 3.39 | 0.22 | 0.86 | 6.63*75.36 |

Table 3.5 SCR core ESD parameters table

3.2.4 SCR Structure Horizontal Comparison

Figure 3.8, Figure 3.9 Figure 3.10 Figure 3.11 Figure 3.12 Figure 3.13 shows the comparison of Vt1, Vt2, It2, Vh, Ih, Ron of SCR core/IO structure with three ESD level from 1KV to 3KV. Since there is no gate in SCR structure, core or IO technology with thin or thick gate thickness does not have much differences. In general, Vt1 of SCR structure is too big to be used in 28nm circuit design. Typical gate oxide breakdown

voltage under DC for core and IO process are 2.8V and 5.2V, under TLP are 6.2 and 9.3V. Single SCR device is not suitable to protect the core circuit.

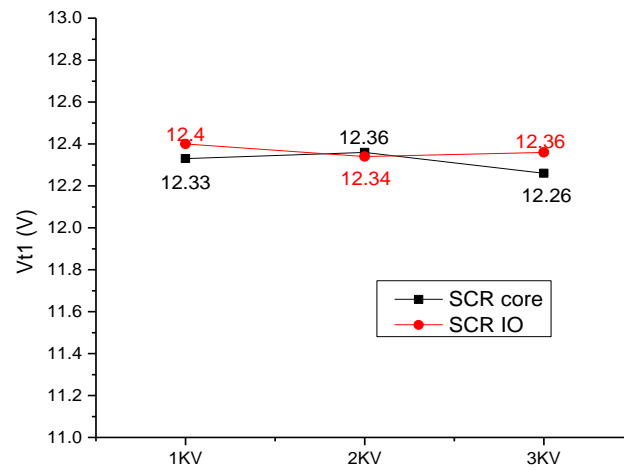


Figure 3.8 SCR Vt1 comparison

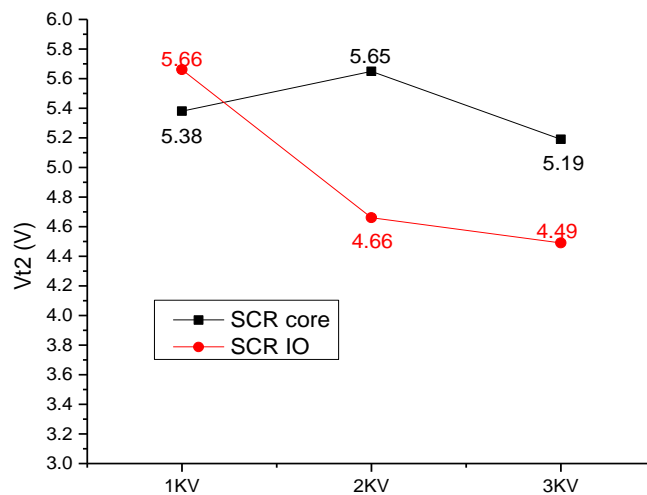


Figure 3.9 SCR Vt2 comparison

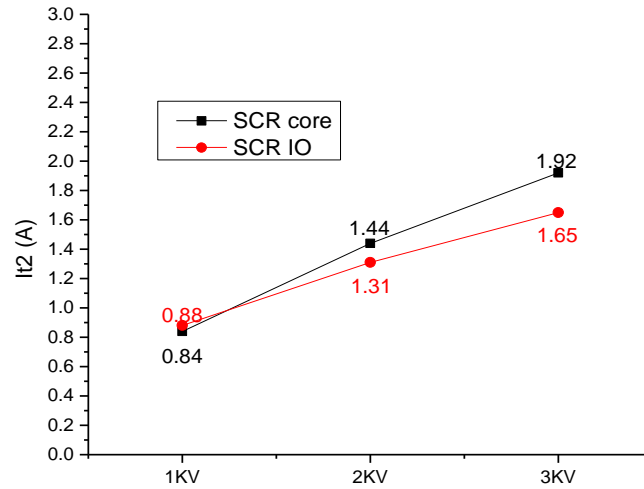


Figure 3.10 SCR It2 comparison

It2 is an expression of ESD failure highest current tolerance. From those it is easily find out that It2 increases with ESD level increase which all pass its ESD protection standard.

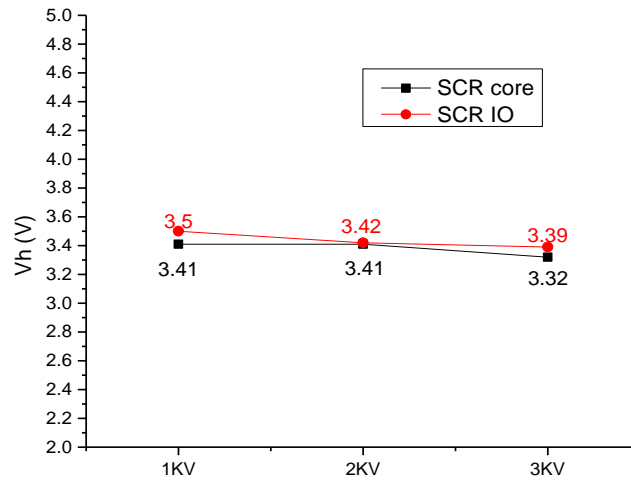


Figure 3.11 SCR Vh comparison

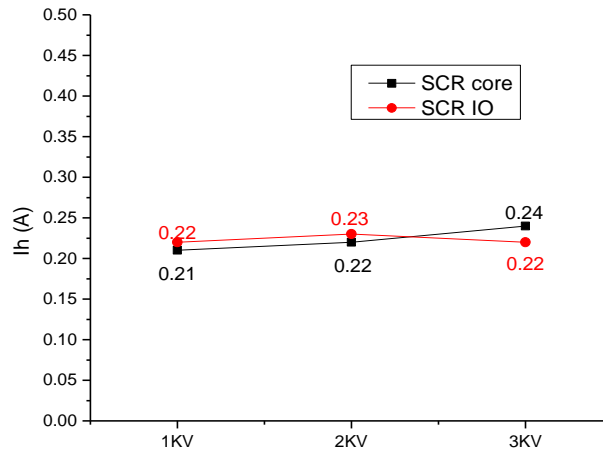


Figure 3.12 SCR Ih comparison

It is noticed that there is nearly no difference of V_h and I_h , exhibits that the width of SCR will not affect the holding point of I-V curve.

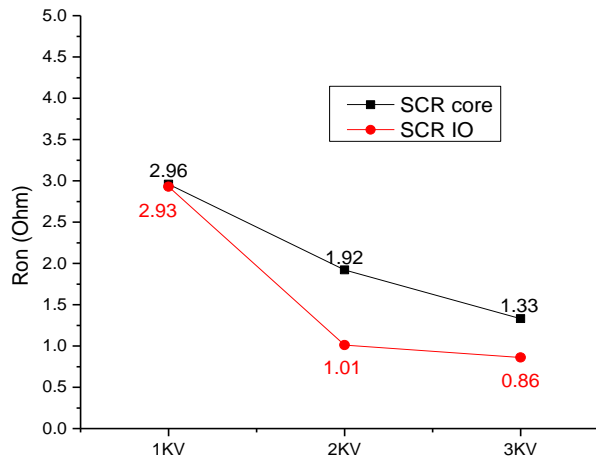


Figure 3.13 SCR Ron comparison

R_{on} shows the performance of SCR ESD protection when it is turned on. Lower R_{on} means current will go more quickly through ESD path. From the figure, R_{on}

decrease obviously when ESD level increase. It is easy to understand since wider the SCR, smaller the resistance. IO structure which has thicker gate has a lower R_{on} .

3.3 Diode Triggered SCR Design for CMOS 28nm Technology

As discussed before, standalone SCR usually cannot be used as 28nm node ESD protection devices due to its large trigger voltage. Trigger assistant circuits will help to lower the trigger voltage of SCR and make it suitable for the design window. Commonly used trigger assistant circuits including diodes, GCMOS and RC components. Among all, diode triggered SCR is very efficient and also could help to well control the trigger voltage because of its structure. Schematics of diode triggered SCR (DTSCR) commonly used in industry are shown in Fig 3.14 [13]. By adding diode strings at G_2 node, one could control trigger voltage easily simply by choosing the series diode string numbers. Trigger voltage will be one SCR intrinsic diode trigger voltage plus series diode string trigger voltage.

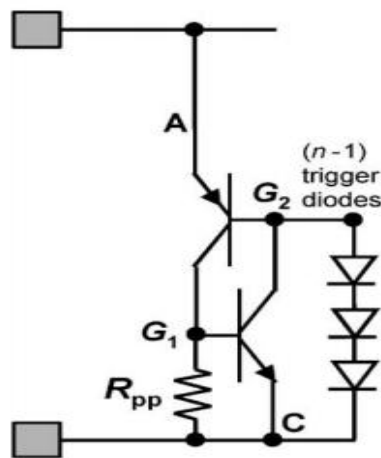


Figure 3.14 DTSCR Schematic

For diode string designs, since they only act as a trigger assistant element, after the current is large enough through the substrate to trigger the SCR, current will mostly go through SCR because SCR's large current handling capability. Diode string size no need to be large, it only need to handle the current at the very beginning, this is good for the area considerations. Also, since there are two diode types as STI diode and Gated diode, DTSCR also could be designed as STI DTSCR and Gated DTSCR [14]. Cross sections of STI DTSCR and Gated DTSCR are demonstrated in Fig 3.15 and Fig 3.16. External diode strings are connected through G2 nodes comes from intrinsic SCR. Isolations of PW is shown between each diodes and are connected to cathode.

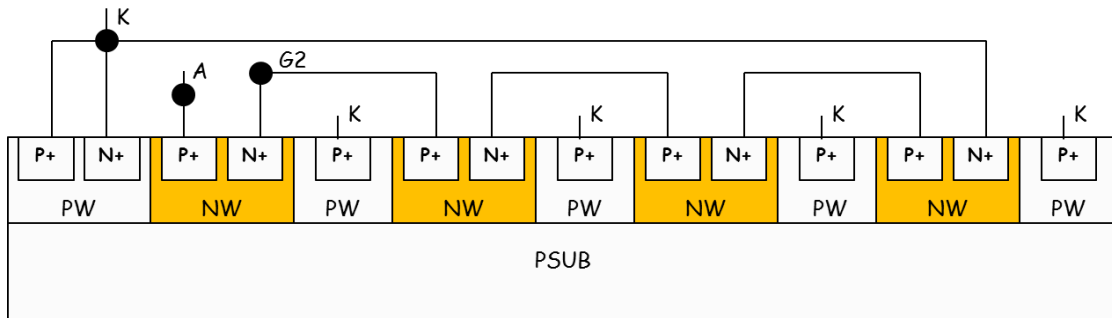


Figure 3.15 STI DTSCR X-section

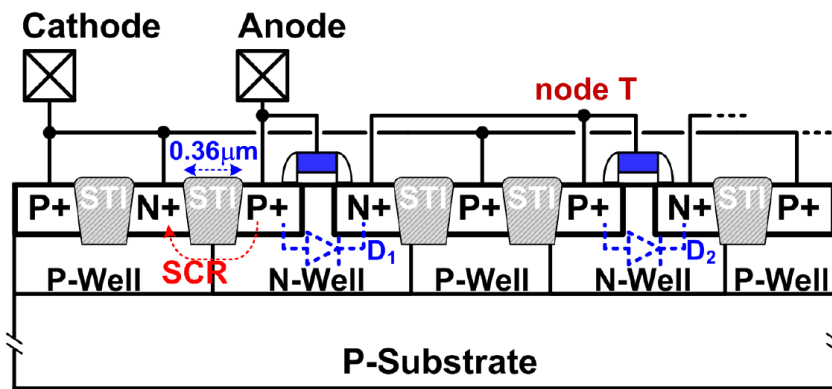


Figure 3.16 Gated DTSCR X-section

For Gated DTSCR, intrinsic diode of SCR are also using gate on top to prevent STI formation. Compared with STI diode, gated diode will have smaller Ron and higher Vt2 since the current path is shorter. Trigger time will be faster and thus ideal for fast ESD pulses like CDM pulse. However the leakage current will also increase since no STI between N plus and P plus. Gated DTSCR capacitance will also be higher compared with STI DTSCR. Designers could choose the DTSCR types according to their priorities among all specs.

3.3.1 DTSCR TCAD Simulation Guidelines

DTSCR TCAD simulation is done to provide design guideline. X-section, temperature and current flow for STI DTSCR are shown in Fig 3.17, Fig 3.18 and Fig 3.19. It is taken under 2KV HBM pulse at 12ns.

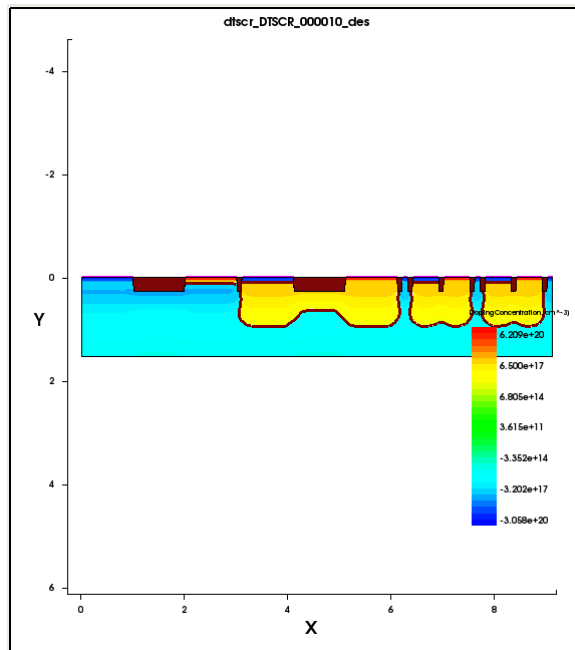


Figure 3.17 TCAD simulation results for STI DTSCR X-sections

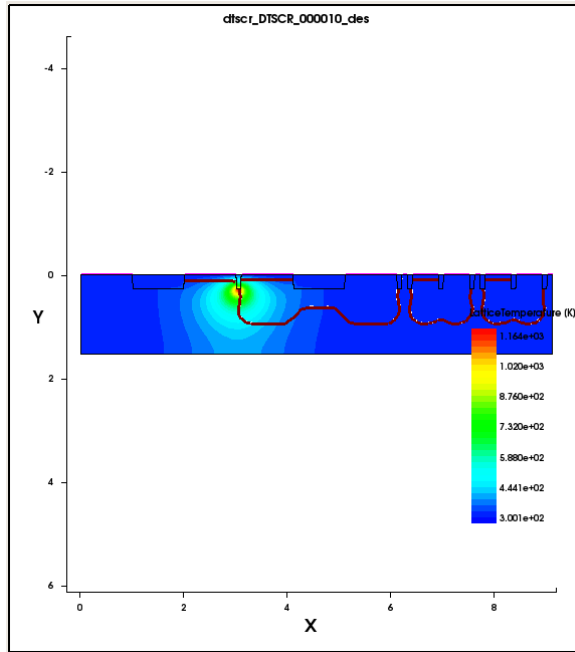


Figure 3.18 TCAD simulation results for STI DTSCR temperature

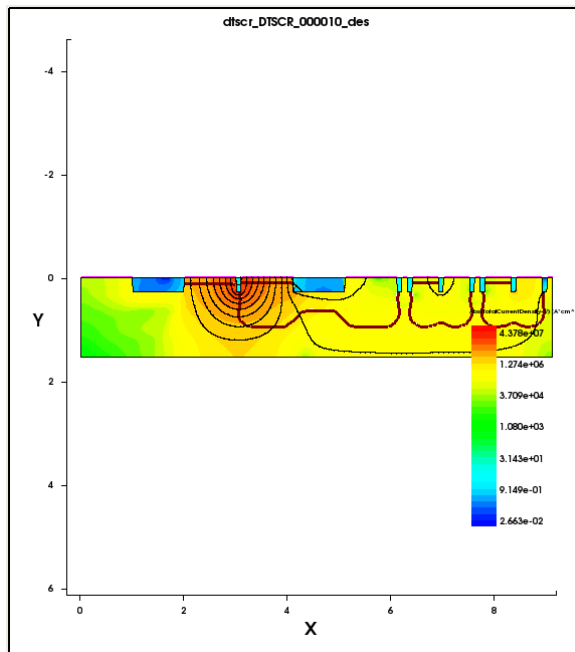


Figure 3.19 TCAD simulation results for STI DTSCR current flow

From temperature and current flow results, it is confirmed that most of current go through SCR when it is ON. IV characteristics in Fig 3.20 showing trigger voltage around 3V for DTSCR with two external diodes. The trigger voltage could be well controlled by changing diode numbers for different design requirements. After the diode string is on, current start to increase, when the current is large enough at the substrate, SCR is turned on and holding voltage is around 2V, this deep snapback proves the SCR is on. SCR takes large amount of the current since then. Advantages of SCR are fully used in the DTSCR design.

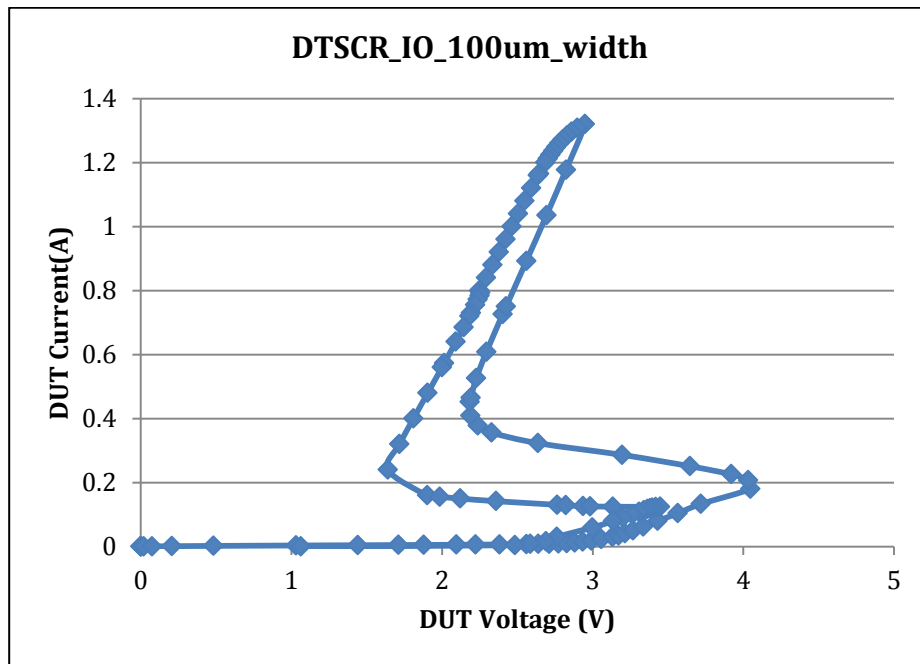


Figure 3.20 TCAD STI DTSCR I-V characteristic

Gated DTSCR TCAD simulation is done to provide design guideline. X-section, temperature and current flow for Gated DTSCR are shown in Fig 3.21, Fig 3.22 and Fig 3.23. It is taken under 2KV HBM pulse at 12ns. Compared with STI DTSCR, there is no STI between Nplus and Pplus.

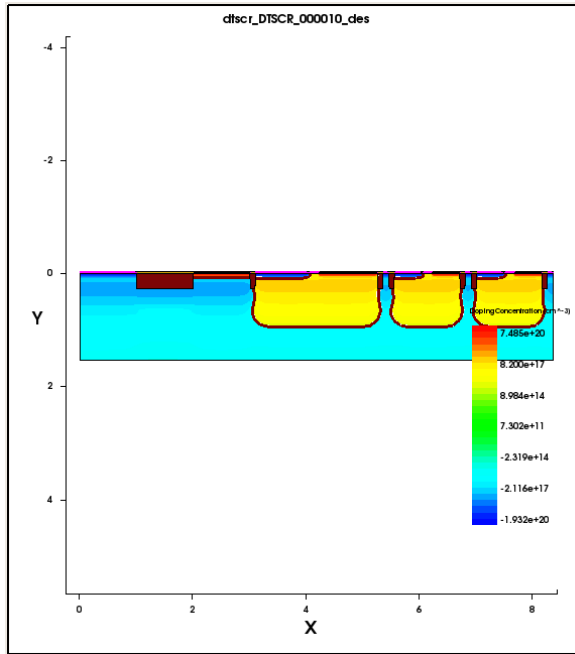


Figure 3.21 TCAD simulation results for Gated DTSCR X-sections

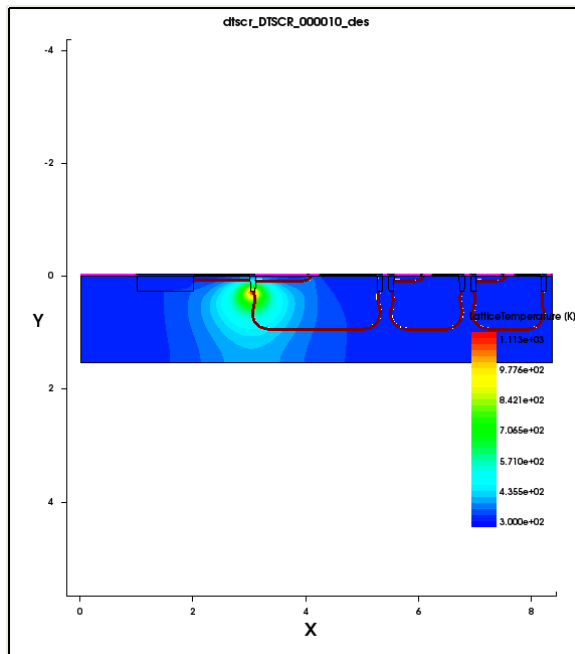


Figure 3.22 TCAD simulation results for Gated DTSCR temperature

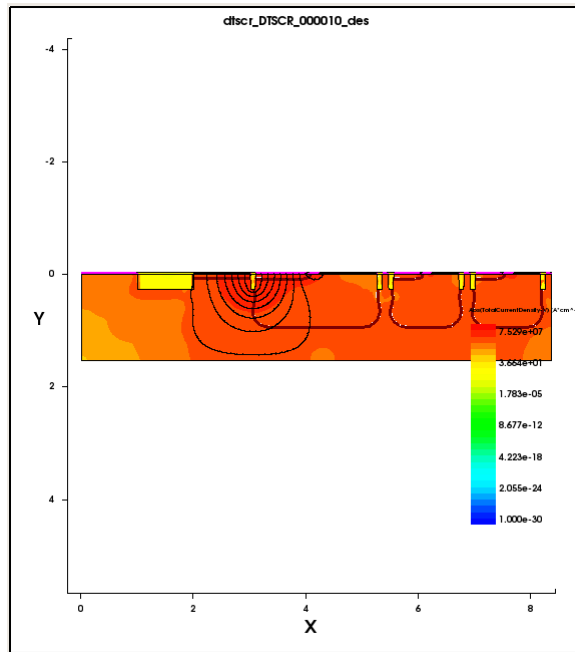


Figure 3.23 TCAD simulation results for Gated DTSCR current flow

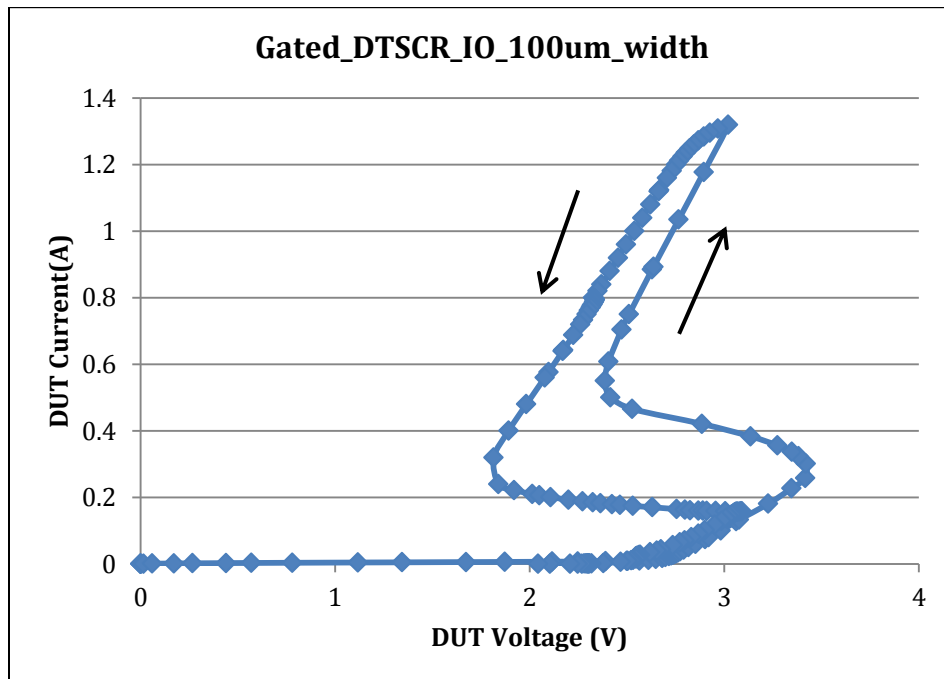


Figure 3.24 TCAD Gated DTSCR I-V characteristic

Compared with STI DTSCR, it is obvious that the higher temperature are lower for the same HBM level, this means that protection level is higher for Gated DTSCR case. Also current is more evenly distributed and no large crowding. Heat is dissipated more efficiently to the substrate.

IV characteristic of Gated DTSCR is in Fig 3.24. Fig 3.25 compared 3 cases with the same SCR dimension, 2 DTSCR cases and 1 SCR only case. It is obvious that DTSCR case could significantly reduce the trigger voltage of standalone SCR. After the trigger of SCR, three curves have the same IV performance confirms that SCR is taking most of the current flows. Gated DTSCR, compared with STI DTSCR, will have smaller Ron, thus need more substrate current and voltage to help trigger SCR, so holding current is higher. This gives us the difference of 3 cases key ESD parameters.

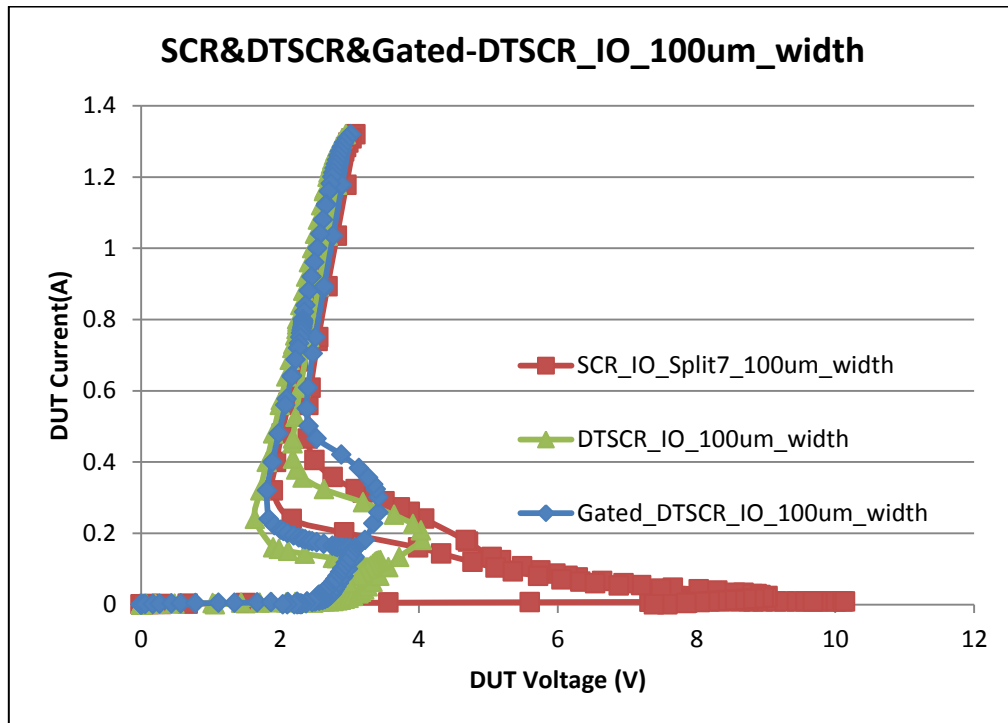


Figure 3.25 TCAD SCR I-V characteristic comparison

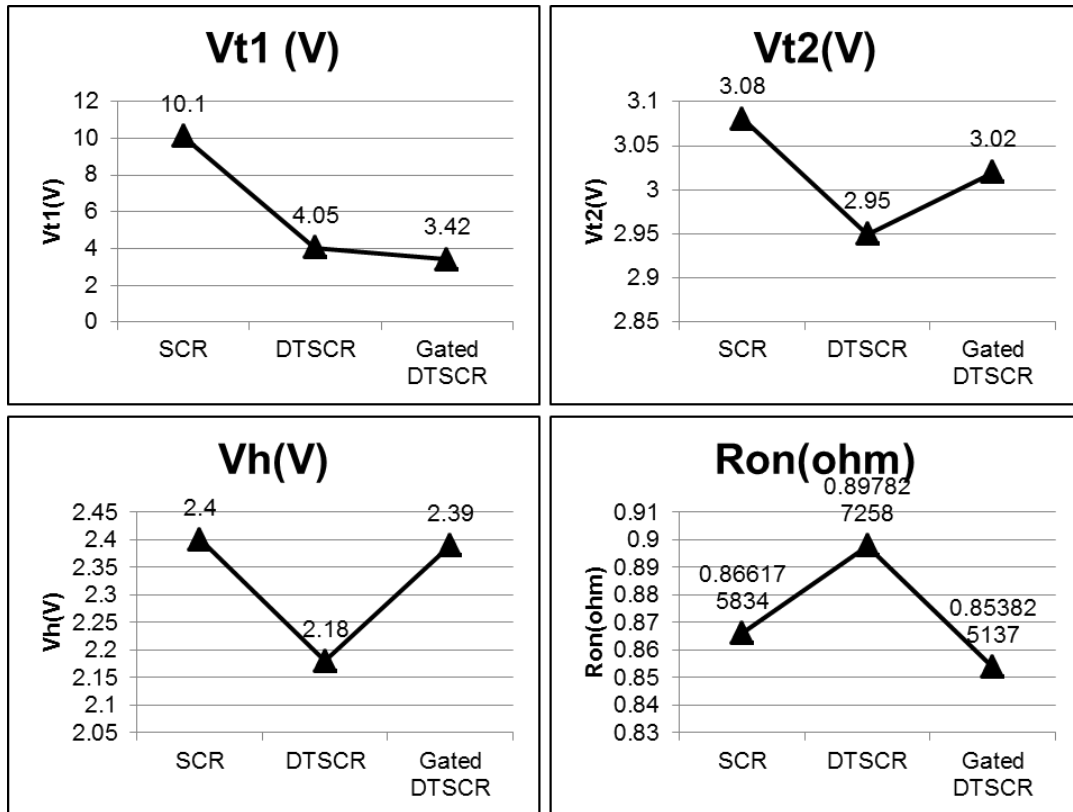


Figure 3.26 TCAD SCR key ESD parameter comparison

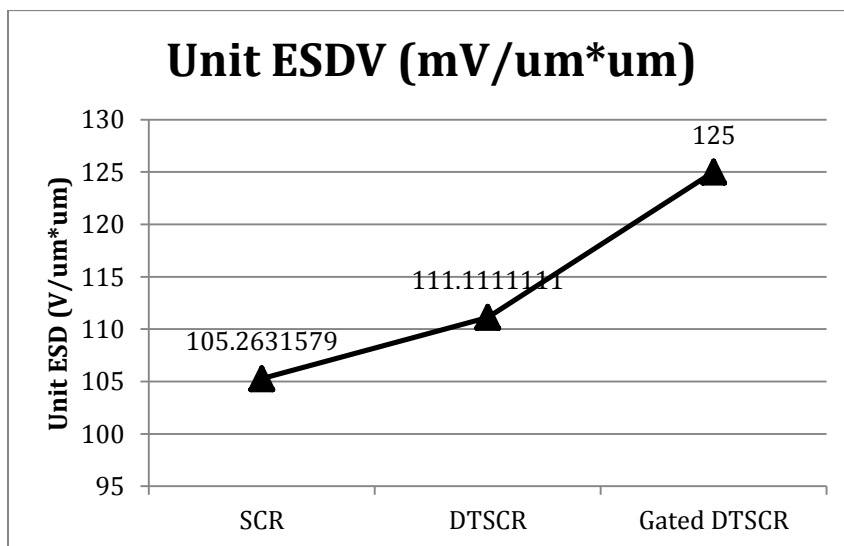


Figure 3.27 TCAD SCR ESDV

Key ESD parameter summary and ESDV are shown in Fig 3.26 and Fig 3.27. Diode triggered SCR trigger voltage is the lowest among all SCR splits. Gated DTSCR Vt1 is lower than DTSCR because of gated diode structure. Diode string trigger voltage is around 3V which comes from one intrinsic diode in SCR and two external diodes. Diode triggered SCR has higher ESDV than regular ones. Gated DTSCR have highest ESDV because there are no STI in between. However leakage current also higher for gated diodes.

3.3.2 DTSCR Design Splits

STI DTSCR is designed in both core and IO technology using 28nm process. Gated DTSCR is designed in only IO technology. Gated splits in core technology will have large leakage current. Different DTSCR diode string number is used for various ESD trigger voltage applications. DTSCR design splits are shown in Table 3.6.

| ID # | Name | Diode No. | Diode Plus (um) | Diode Iso. (um) | SCR Plus (um) | STI/Gate (um) | Width (um) |
|------|-------------|-----------|-----------------|-----------------|---------------|---------------|------------|
| 1 | DTSCR core | 1 | 0.5 | 0.14 | 1 | 0.15 | 50 |
| 2 | | 2 | 0.5 | 0.14 | 1 | 0.15 | 50 |
| 3 | | 3 | 0.5 | 0.14 | 1 | 0.15 | 50 |
| 4 | DTSCR IO | 1 | 0.5 | 0.14 | 1 | 0.15 | 50 |
| 5 | | 2 | 0.5 | 0.14 | 1 | 0.15 | 50 |
| 6 | | 3 | 0.5 | 0.14 | 1 | 0.15 | 50 |
| 7 | DTSCR gated | 1 | 0.5 | 0.14 | 1 | 0.15 | 50 |
| 8 | | 2 | 0.5 | 0.14 | 1 | 0.15 | 50 |
| 9 | | 3 | 0.5 | 0.14 | 1 | 0.15 | 50 |

Table 3.6 DTSCR design splits

3.3.3 Core STI DTSCR Testing Results

Figure 3.28 shows the I-V curve of TLP testing and Table 3.7 shows the critical parameters which representing the ESD performance of DTSCR core with external diode number 1, 2, 3. From those we can find out that more than 3KV ESD level protection has been realized and trigger voltage can be well controlled by diode number. Meanwhile, Ron doesn't change a lot as diode number increase.

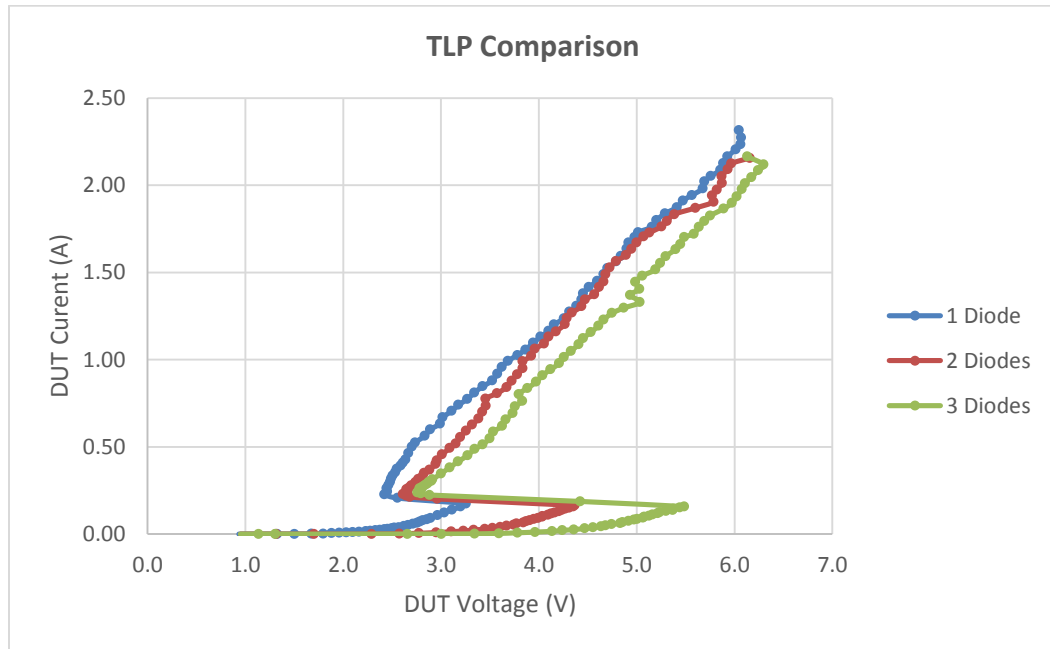


Figure 3.28 STI DTSCR core TLP testing I-V curve

| Name | Vt1 (V) | Vt2 (V) | It2 (A) | Vh (V) | Ih (A) | Ron (Ohm) | Area* (um ²) |
|---------------|---------|---------|---------|--------|--------|-----------|--------------------------|
| DTSCR core 1D | 3.26 | 6.05 | 2.31 | 2.42 | 0.23 | 1.88 | 9.04*50.89 |
| DTSCR core 2D | 4.37 | 6.16 | 2.16 | 2.61 | 0.23 | 1.77 | 11.45*50.89 |
| DTSCR core 3D | 5.49 | 6.13 | 2.16 | 2.76 | 0.24 | 1.86 | 13.86*50.89 |

Table 3.7 STI DTSCR core ESD parameters table

3.3.4 IO STI DTSCR Testing Results

Figure 3.29 shows the I-V curve of TLP testing and Table 3.8 shows the critical parameters which representing the ESD performance of DTSCR IO with external diode number 1, 2, 3. From those we can find out that more than 3KV ESD level protection has been realized and trigger voltage can be well controlled by diode number. Meanwhile, Ron doesn't change a lot as diode number increase.

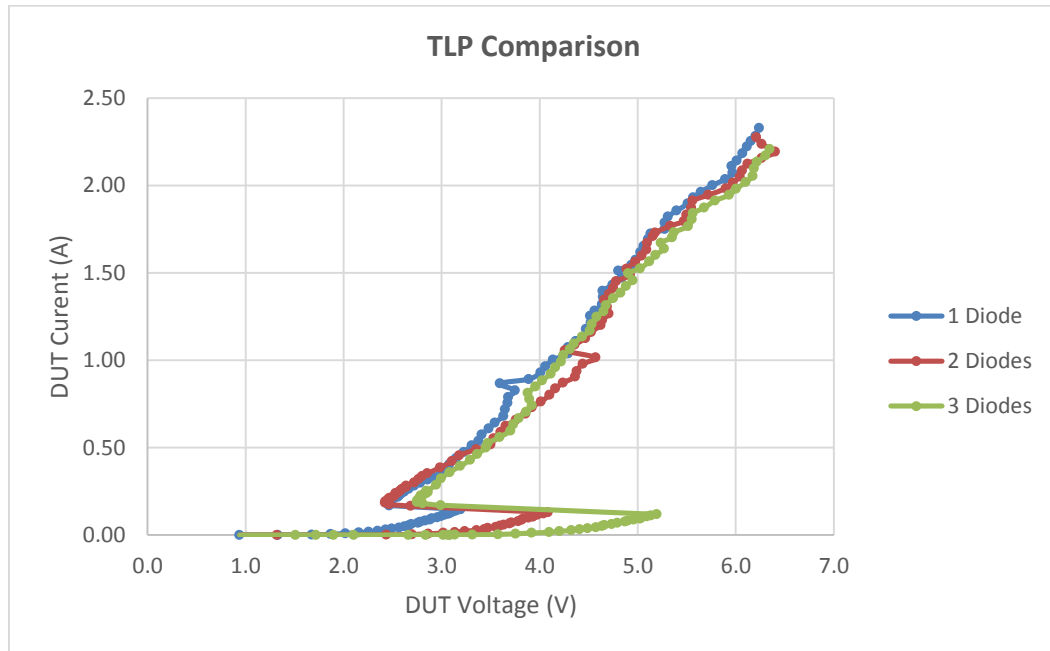


Figure 3.29 STI DTSCR IO TLP testing I-V curve

| Name | Vt1 (V) | Vt2 (V) | It2 (A) | Vh (V) | Ih (A) | Ron (Ohm) | Area* (um2) |
|-------------|---------|---------|---------|--------|--------|-----------|-------------|
| DTSCR IO 1D | 3.19 | 6.24 | 2.33 | 2.45 | 0.18 | 1.74 | 9.04*50.89 |
| DTSCR IO 2D | 4.08 | 6.21 | 2.27 | 2.42 | 0.18 | 1.85 | 11.45*50.89 |
| DTSCR IO 3D | 5.19 | 6.35 | 2.21 | 2.75 | 0.19 | 1.74 | 13.86*50.89 |

Table 3.8 STI DTSCR IO ESD parameters table

3.3.5 IO Gated DTSCR Testing Results

Figure 3.30 shows the I-V curve of TLP testing and Table 3.9 shows the critical parameters which representing the ESD performance of Gated DTSCR IO with external diode number 1, 2, and 3. From those we can find out that more than 3KV ESD level protection has been realized and trigger voltage can be well controlled by diode number. Meanwhile, Ron doesn't change a lot as diode number increase.

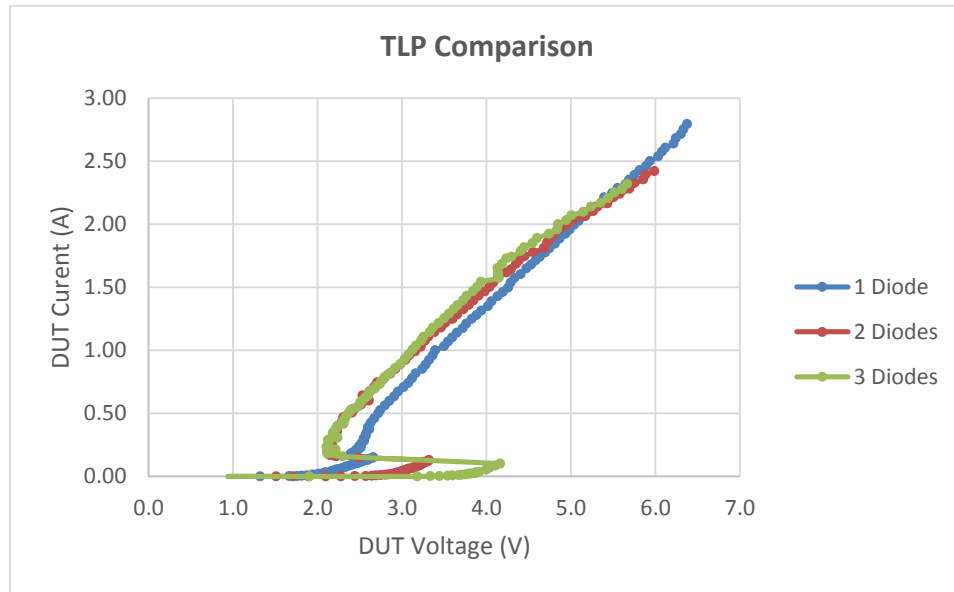


Figure 3.30 Gated DTSCR IO TLP testing I-V curve

| Name | Vt1 (V) | Vt2 (V) | It2 (A) | Vh (V) | Ih (A) | Ron (Ohm) | Area* (um2) |
|----------------|---------|---------|---------|--------|--------|-----------|-------------|
| DTSCR Gated 1D | 2.66 | 6.38 | 2.79 | 2.39 | 0.17 | 1.55 | 9.04*50.89 |
| DTSCR Gated 2D | 3.32 | 5.99 | 2.42 | 2.12 | 0.19 | 1.75 | 11.45*50.89 |
| DTSCR Gated 3D | 4.16 | 5.67 | 2.32 | 2.11 | 0.23 | 1.68 | 13.86*50.89 |

Table 3.9 Gated DTSCR IO ESD parameters table

3.3.6 DTSCR Structure Horizontal Comparison

Figure 3.31, Figure 3.32 Figure 3.33 Figure 3.34 Figure 3.35 Figure 3.36 shows the comparison of V_{t1} , V_{t2} , I_{t2} , V_h , I_h , R_{on} of STI DTSCR core/IO structure and Gated DTSCR IO structure with external diode string number of 1, 2 and 3.

Trigger voltage drops obviously when diode number decreases. Also we can notice that gated diode trigger SCR has the lowest V_{t1} and thicker gate decreases it a little bit.

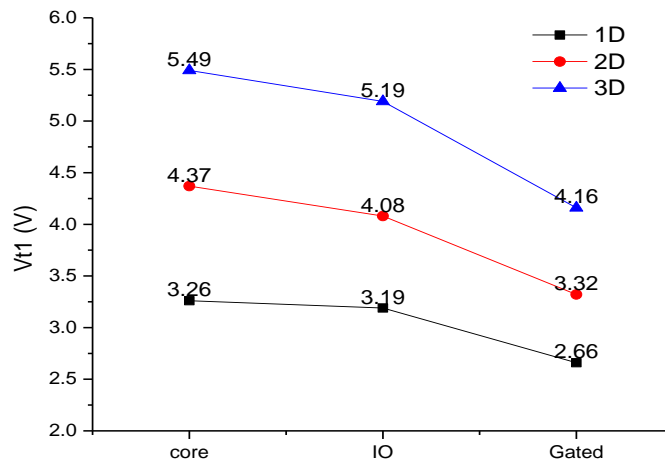


Figure 3.31 DTSCR V_{t1} comparison

From V_{t2} and I_{t2} results, Gated DTSCR has the highest protection level. So if the ESD protection level is determined, Gated DTSCR will have the smallest area. Thanks to the direct path between Nplus and Pplus, the current are more evenly distributed. There is no current crowding or hotspot underneath the STI as the STI DTSCR case.

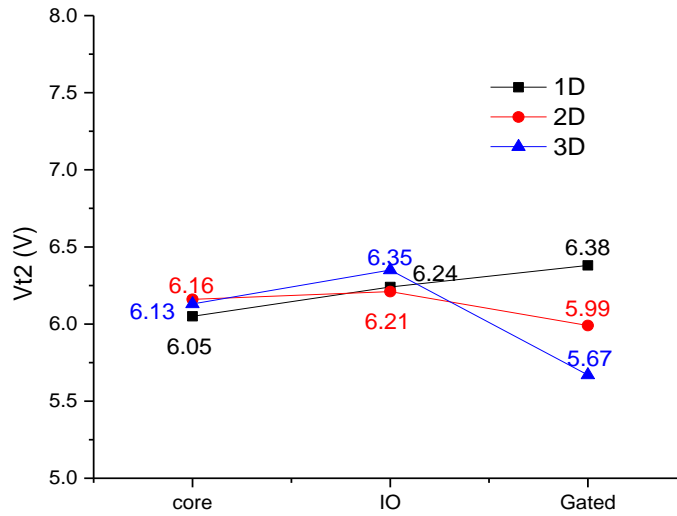


Figure 3.32 DTSCR Vt2 comparison

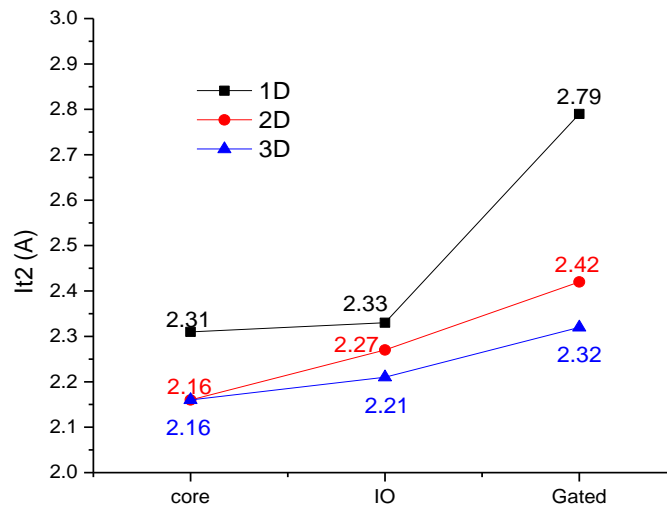


Figure 3.33 DTSCR It1 comparison

Holding voltage of Gated DTSCR is lower than STI DTSCR. This is due to the different core SCR structure. Gated case have shorter gate in between P+ and N+ of NW.

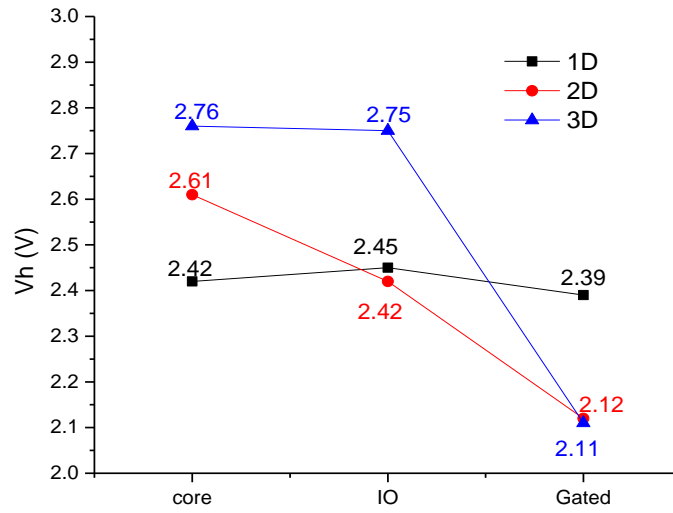


Figure 3.34 DTSCR Vh comparison

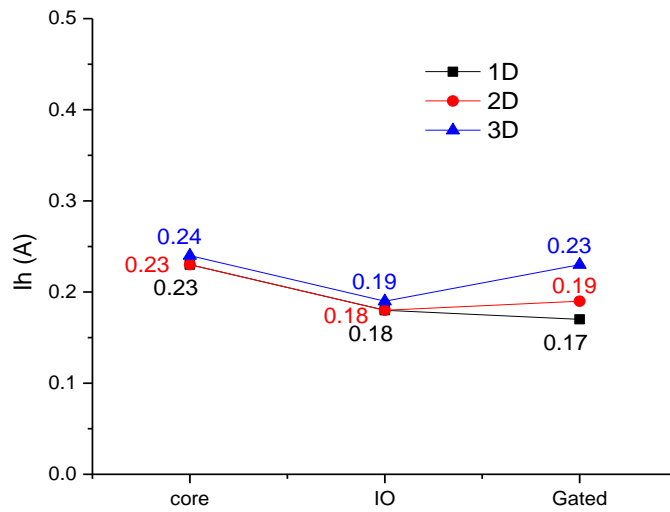


Figure 3.35 DTSCR Ih comparison

Ron of Gated DTSCR is smallest as predicted. It's value is around 1 to 2V thanks to SCR properties.

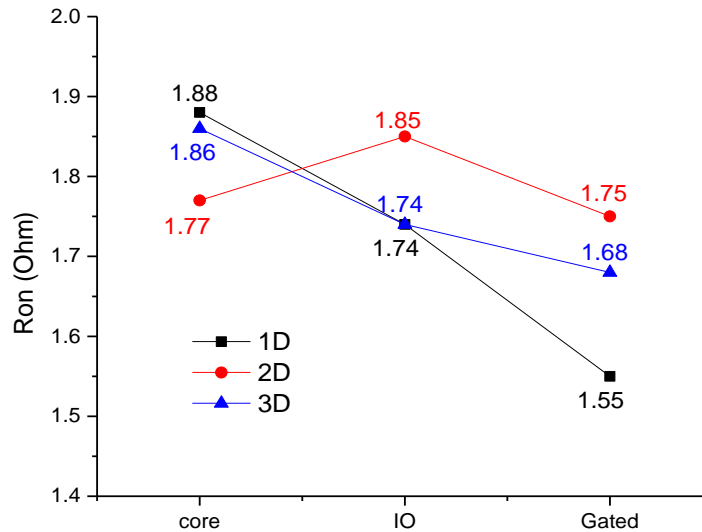


Figure 3.36 DTSCR Ron comparison

3.4 Conclusion

Stand-alone SCR ESD structures, including SCR, STI DTSCR and Gated DTSCR, cover different levels of ESD protection. TCAD simulation gives a great instruction before design and analysis before tape-out. Full characterization of TLP testing has been conducted according to the test plan. Testing results have been analyzed thoroughly for different ESD SCR structures which satisfy different protection level. Critical ESD parameters, including trigger voltage (V_{t1}), R_{on} , I_{t2} , V_h and I_h , have been characterized for SCR in 28nm process. A SCR ESD design flow is established for sub-32nm node.

For SCR, an obvious snapback can be seen and the turned-on resistance is really small which is good for ESD protection. But the trigger voltage of SCR is much bigger

than normal IC supply voltage. Meanwhile, 1/2/3KV protections have been realized. Compared the results of core and IO structure, there is no big difference as poly-gate hasn't been used.

For DTSCR, it has the best performance with controllable trigger voltage by changing diode number. It's after turned-on performance is like SCR with good holding voltage and R_{on} . Also, DTSCR realizes 3KV ESD protection with 50um width. By comparing different diode structure, core/IO/gated, it's easy to find out that gated diode trigger SCR can realize higher ESD protection level which means higher I_{t2} .

Chapter 4 Introduction of Graphene

4.1 History of Graphene

Since 2004, two great scientists Andre Geim and Konstantin Novoselov from University of Manchester has found graphene experimentally, graphene has been a rapidly rising star on the horizon of condensed matter physics and electrical. Experimental results from transport measurements show that graphene has remarkably high electron mobility at room temperature, with reported values in excess of $15,000 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$. The unique electronic properties of this magic 2D structure have led to a number of exotic effects that can be used to improve the performance of electronic devices.

More than 70 years ago, Landau and Peierls argued that strictly two-dimensional crystals were thermodynamically unstable and could not exist. The argument was supported by both theory and experimental observations until the experimental discovery of graphene and other 2D atomic crystals.

Importantly, the 2D crystals were found not only to be continuous but to exhibit high crystal quality. Charge carriers in graphene can travel thousands interatomic distances without scattering. Some explanation of the existence of 2D structure is that the extracted 2D crystals become intrinsically stable by gentle crumpling in the third dimension on a lateral scale of about 10nm, which leads to a gain in elastic energy that suppresses thermal vibrations [15].

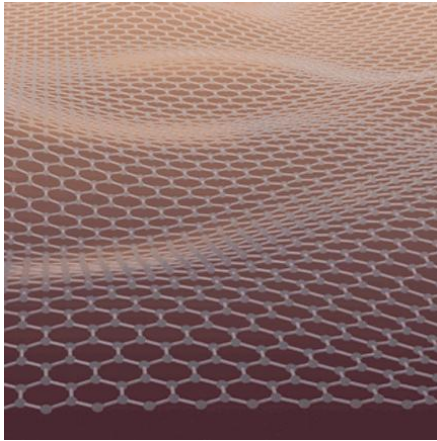


Figure 4.1 Graphene with crumpling in the third dimension

4.2 Band Structure of Graphene

4.2.1 Linear Dispersion

Graphene is a flat monolayer of carbon atoms tightly packed into a two-dimensional (2D) honeycomb lattice.

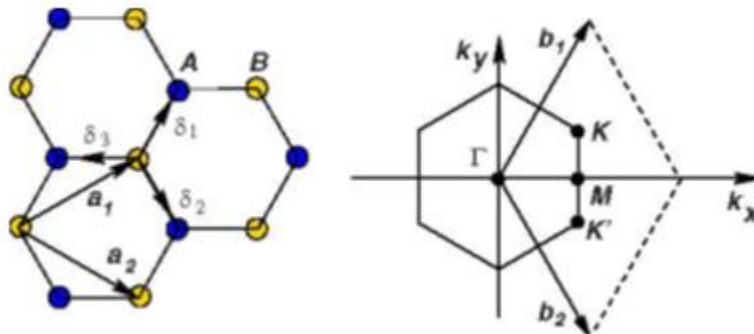


Figure 4.2 Lattice structure and Brillouin zone

The structure can be seen as a triangular lattice with a basis of two atoms per unit cell. Carbon-carbon distance is $a=1.42\text{\AA}$. Lattice vectors:

$$\vec{a}_1 = \frac{a}{2}(3, \sqrt{3}), \quad \vec{a}_2 = \frac{a}{2}(3, -\sqrt{3}) \quad (1)$$

Reciprocal vectors:

$$\vec{b}_1 = \frac{2\pi}{3a}(1, \sqrt{3}), \quad \vec{b}_2 = \frac{2\pi}{3a}(1, -\sqrt{3}) \quad (2)$$

Two points K and K' at the boundary of first BZ is called Dirac points:

$$\vec{K} = \left(\frac{2\pi}{3a}, \frac{2\pi}{3\sqrt{3}a} \right), \quad \vec{K}' = \left(\frac{2\pi}{3a}, -\frac{2\pi}{3\sqrt{3}a} \right) \quad (3)$$

In solid-state physics, the tight binding model is an approach to the calculation of electronic band structure using an approximate set of wave functions based upon superposition of wave functions for isolated atoms located at each atomic site. The tight binding Hamiltonian for electrons in graphene considering that electrons can hop to both nearest- and next-nearest-neighbor atoms can be written as:

$$H = -t \sum_{\langle i,j \rangle, \sigma} (a_{\sigma,i}^\dagger b_{\sigma,j} + h.c.) + t' \sum_{\langle\langle i,j \rangle\rangle, \sigma} (a_{\sigma,i}^\dagger a_{\sigma,j} + b_{\sigma,i}^\dagger b_{\sigma,j} + h.c.) \quad (4)$$

$a_{\sigma,i}$ annihilates an electron with spin σ on site R_i on sublattice A. $a_{i,\sigma}$ creates an electron. $b_{\sigma,i}$ is the same definition for sublattice B. t is the nearest neighbor hopping energy which is 2.8eV (hoping between different sublattices). t' is the next nearest neighbor hopping energy (hoping in the same sublattice). Thus we can calculate the energy [16]:

$$E_{\pm}(\vec{k}) = \pm t \sqrt{3 + f(\vec{k})} - t' f(\vec{k}) \quad (5)$$

$$f(\vec{k}) = 2 \cos(\sqrt{3}k_y a) + 4 \cos\left(\frac{\sqrt{3}}{2}k_y a\right) \cos\left(\frac{3}{2}k_x a\right) \quad (6)$$

From the band structure, graphene is semimetal and has zero energy gaps. Plus sign means the upper side of the band structure and minus sign means the lower side.

From the energy equation, the energy bands are only symmetric around zero when t' is 0.

The electron-hole symmetry is broken with finite values of t' .

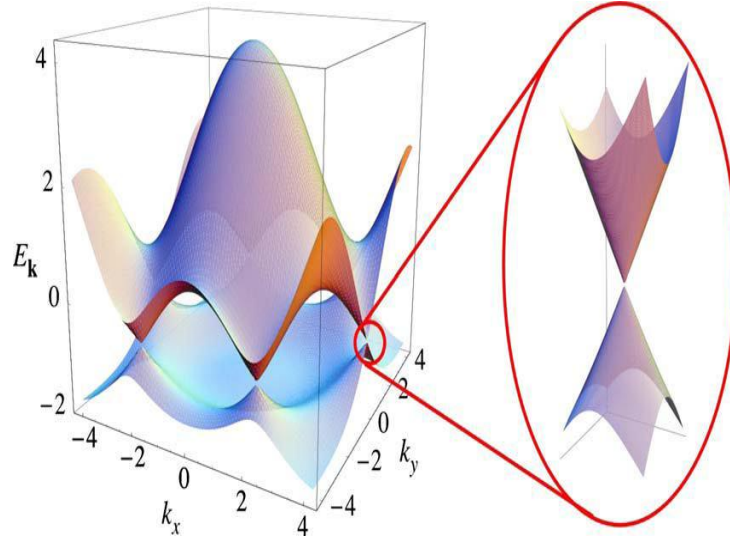


Figure 4.3 Electronic dispersion in graphene

Right side of Fig 4.3 is the band structure zoom in of the Dirac points. When wave factor k is close to Dirac points K , it can be written as:

$$\vec{k} = \vec{K} + \vec{q} \quad (7)$$

With $|q| \ll |K|$, the dispersion relation near Dirac points is:

$$E_{\pm}(\vec{q}) = \pm v_F |\vec{q}| + O\left[\left(\frac{q}{K}\right)^2\right] \quad (8)$$

$$v_F = 3ta / 2 \approx 1 \times 10^6 \text{ m/s} \quad (9)$$

As a consequence, quasiparticles in graphene, like massless relativistic particles, have the linear dispersion law, where the Fermi velocity $v_F \approx c/300$ plays the role of the speed of light. In view of the linearity of the spectrum, we can expect the behavior of quasiparticles in graphene to be principally different from the behavior of quasiparticles

in ordinary metals and semiconductors, where they have parabolic dispersion and behave like free electrons.

In usual massive case, the velocity changes substantially with energy or momentum. However in graphene case, the velocity is independent of energy or momentum.

4.2.2 Effective Mass

An immediate consequence of this massless Dirac-like dispersion is a cyclotron mass that depends on the electronic density as its square root. The cyclotron mass is defined, within the semi-classical approximation, as

$$m^* = \frac{1}{2\pi} \left[\frac{\partial A(E)}{\partial E} \right]_{E=E_F} \quad (10)$$

A(E) is the area in k space enclosed by the orbit:

$$A(E) = \pi q(E)^2 = \pi \frac{E^2}{v_F^2} \quad (11)$$

The electronic density n is related to the Fermi momentum:

$$k_F^2 / \pi = n \quad (12)$$

Finally get the cyclotron mass which depends on the electronic density as its square root:

$$m^* = \frac{\sqrt{\pi}}{v_F} \sqrt{n} \quad (13)$$

Fig 4.4 gives us cyclotron mass of charge carriers in graphene as a function of their concentration n. Positive and negative n correspond to electrons and holes,

respectively. Symbols are the experimental data extracted from the temperature dependence of the SdH oscillations. Solid curves are the best fit by Eq.(13).

The usual parabolic dispersion implies a constant cyclotron mass. Thus the experimental observation of the $n^{1/2}$ dependence on the cyclotron mass is an indication of a linear dispersion law and provides evidence for the existence of massless Dirac quasiparticles in graphene.

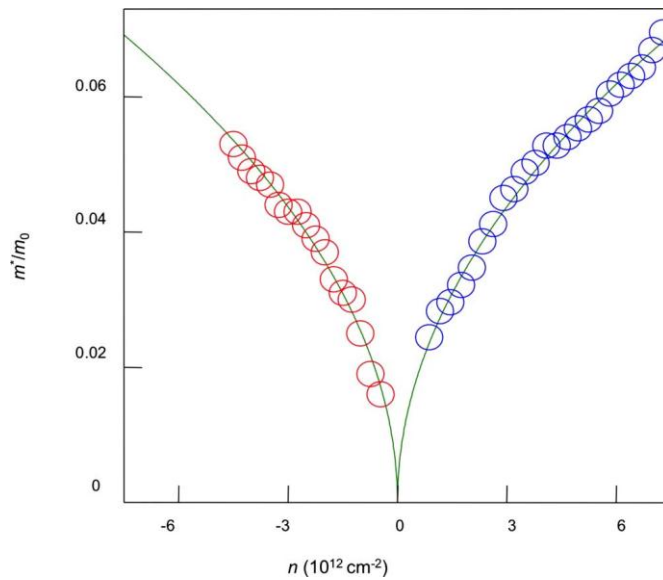


Figure 4.4 Cyclotron mass of graphene

4.2.3 Dirac Equation

In condensed matter physics, the Schrödinger equation rules the world, usually being quite sufficient to describe electronic properties of materials. Graphene is an exception: under tight binding approximation, we solve the Schrödinger equation and get the linear dispersion relation close to Dirac points. However, this linear dispersion law makes graphene easier and more natural to be described with Dirac equation. Although

there is nothing particularly relativistic about electrons moving around carbon atoms, their interaction with a periodic potential of graphene's honeycomb lattice gives rise to new quasiparticles that at low energies E are accurately described by the (2+1)-dimensional Dirac equation with an effective speed of light $v_F \approx 10^6 \text{m/s}$. These quasiparticles, called massless Dirac fermions, can be seen as electrons that lost their rest mass m_0 or as neutrinos that acquired the electron charge e .

Dirac-like Hamiltonian:

$$\vec{H} = \hbar v_F \vec{\sigma} \cdot \vec{k} = \hbar v_F \begin{pmatrix} 0 & k_x - ik_y \\ k_x + ik_y & 0 \end{pmatrix} \quad (14)$$

σ is the 2D Pauli matrix.

The Dirac equation is a direct consequence of graphene's crystal symmetry. Its honeycomb lattice is made up of two equivalent carbon sublattices A and B, and cosine-like energy bands associated with the sublattices intersect at zero E near the edges of the Brillouin zone:

$$\hbar v_F \begin{pmatrix} 0 & k_x - ik_y \\ k_x + ik_y & 0 \end{pmatrix} \begin{pmatrix} \phi_A \\ \phi_B \end{pmatrix} = E \begin{pmatrix} \phi_A \\ \phi_B \end{pmatrix} \quad (15)$$

$$\begin{aligned} -(\hbar v_F)^2 \nabla^2 \phi_A &= E^2 \phi_A \\ -(\hbar v_F)^2 \nabla^2 \phi_B &= E^2 \phi_B \end{aligned} \quad (16)$$

By quantum electrodynamics analysis, we get the same result of linear dispersion:

$$E(\vec{k}) = \hbar v_F k \quad (17)$$

Electronic states near zero E (where the bands intersect) are composed of states belonging to the different sublattices, which need index A and B to indicate. This is similar to the spin index (up and down) in QED and, therefore, is referred to as

pseudospin. Accordingly, in the formal description of graphene's quasiparticles by the Dirac-like Hamiltonian above, σ refers to pseudospin rather than the real spin of electrons. Importantly, QED-specific phenomena are often inversely proportional to the speed of light c and, therefore, enhanced in graphene by a factor $c/v_F \approx 300$.

By analogy with QED, one can also introduce a quantity called chirality that is formally a projection of σ on the direction of motion k and is positive (negative) for electrons (holes). In essence, chirality in graphene signifies the fact that k electron and $-k$ hole states are intricately connected by originating from the same carbon sublattices. The concepts of chirality and pseudospin are important because many electronic processes in graphene can be understood as due to conservation of these quantities.

4.3 Electrical Properties of Graphene

4.3.1 Ambipolar Electric Field Effect

Fig 4.5 shows the ambipolar electric field effect in single-layer graphene. The insets show its conical low-energy spectrum $E(k)$, indicating changes in the position of the Fermi energy E_F with changing gate voltage V_g .

Positive (negative) V_g induce electrons (holes) in concentrations $n=\alpha V_g$ where the coefficient $\alpha \approx 7.2e^{10} \text{cm}^{-2}/\text{V}$ for field-effect devices with a 300 nm SiO_2 layer used as a dielectric. The rapid decrease in resistivity ρ with adding charge carriers indicates their high mobility [17,18,19].

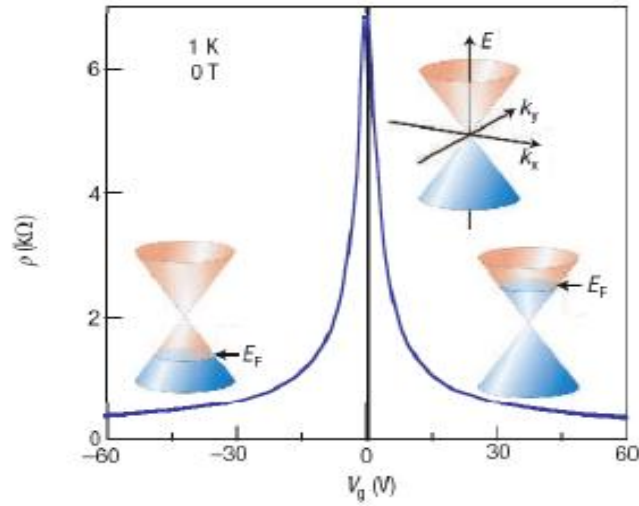


Figure 4.5 Ambipolar electric field effect in graphene

4.3.2 Carrier Mobility

Graphene's quality clearly reveals itself in a pronounced ambipolar electric field effect (Fig 4.5) such that charge carriers can be tuned continuously between electrons and holes. Charge carrier concentrations up to 10^{13}cm^{-2} can be achieved in electric fields at which electric breakdown of the insulator sets in.

Carrier mobilities μ can exceed $15,000 \text{ cm}^2/\text{Vs}$ even under ambient conditions. Moreover, the observed mobilities weakly depend on temperature T , which means that μ at 300K is still limited by impurity scattering or the nanorippling of crystals. Therefore, it potentially can be improved significantly, perhaps, even up to $\approx 100,000 \text{ cm}^2/\text{Vs}$.

Although some semiconductors exhibit room-temperature μ as high as $\approx 77,000 \text{ cm}^2/\text{Vs}$, those values are quoted for undoped bulk semiconductors. In graphene, μ remains high even at high n ($>10^{12} \text{cm}^{-2}$) in both electrically and chemically doped

devices, which translates into ballistic transport on submicron scale (up to $\approx 0.3 \mu\text{m}$ at 300K).

Ballistic transport is the transport of electrons in a medium with negligible electrical resistivity due to scattering. Without scattering, electrons simply obey Newton's second law of motion at non-relativistic speeds [20].

4.3.3 Minimum Conductivity

Another important observation is that graphene's zero-field conductivity σ_{min} does not disappear in the limit of vanishing n but instead exhibits values close to the conductivity quantum $4e^2/h$ per carrier type.

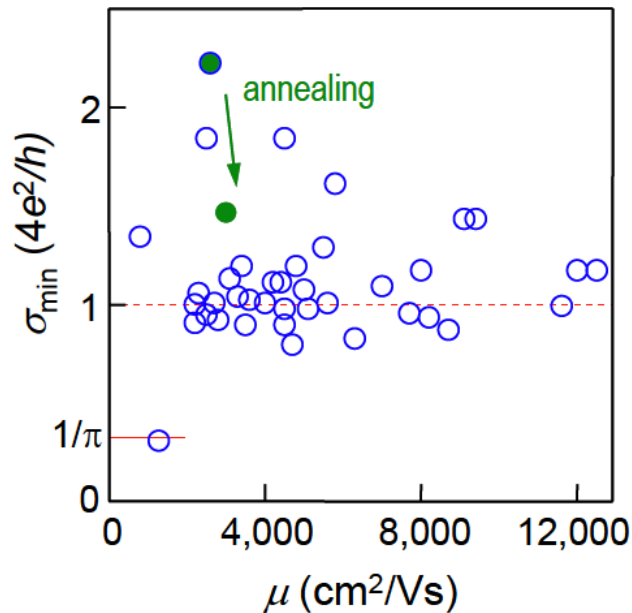


Figure 4.6 Minimum conductivity of graphene

Fig 4.6 shows the lowest conductivity measured near the neutrality point for nearly 50 single-layer devices. Independent of their carrier mobility μ , different

graphene devices exhibited approximately the same conductivity at the neutrality point (open circles) with most data clustering around $\approx 4e^2/h$ indicated for clarity by the dashed line. The green arrow and symbols show one of the devices initially exhibited an anomalously large value of σ_{\min} but after thermal annealing at 400K its σ_{\min} moved closer to the rest of the statistical ensemble.

For all other known materials, such a low conductivity unavoidably leads to a metal-insulator transition at low T but no sign of the transition has been observed in graphene down to liquid helium T.

The minimum of quantum conductivity for Dirac fermions was predicted in theoretical papers. In some of them, the key moment is the density of states tending to zero in the vicinity of the Dirac point on the linear two-dimensional spectrum. However, comparison between the experimental behavior of massless and massive Dirac fermions in graphene and its bilayer allows one to distinguish between chirality and masslessness related effects. To this end, bilayer graphene also exhibits a minimum conductivity of the order of $4e^2/h$ per carrier type, which indicates that it is chirality, rather than the linear spectrum, that is more important.

4.3.4 Quantum Hall Effect

The main experimental effort following the discovery of graphene was aimed at studying the electric properties of graphene that would confirm that the quasiparticles in it are indeed described by QED. Quantum Hall effect was one of the most spectacular manifestations.

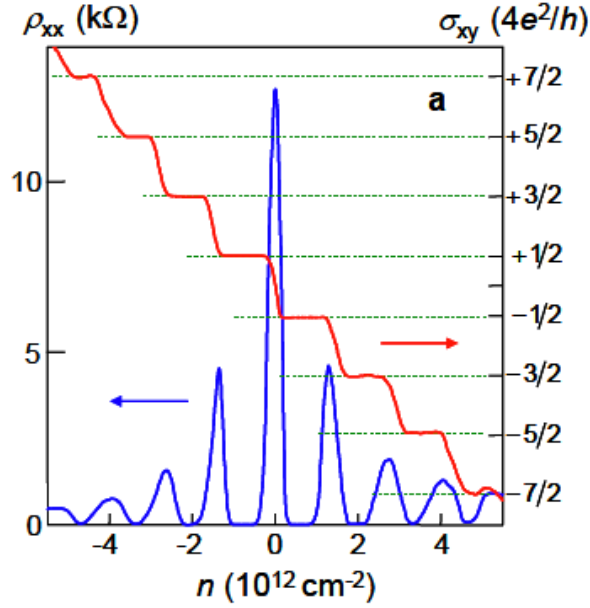


Figure 4.7 Chiral quantum Hall effects

The QHE in monolayer graphene is observed as a series of equidistant steps of the Hall conductivity, which passes through zero at the Dirac point, where the hole conductivity changes to the electron type. The sequence of plateaus has the expected step height but is shifted by 1/2 compared with the standard curve, such that the Hall conductivity takes the form:

$$\sigma_{xy} = 4(N + 1/2)e^2 / h \quad (18)$$

N is the Landau level index and factor 4 appears due to double valley and double spin degeneracy. This QHE has been dubbed “half-integer” to reflect both the shift and the fact that, although it is not a new fractional QHE, it is not the standard integer QHE either.

This unusual behavior is well understood now: it occurs because of the specifics of quantization of Dirac fermions in graphene with linear dispersion in the magnetic field B , and is described by the expression:

$$E_N = \pm v_F \sqrt{2e\hbar BN} \quad (19)$$

$+$ and $-$ respectively refer to electrons and holes. The essential observation is that there is the zeroth Landau level at $E=0$, which simultaneously belongs to electrons and holes. This explains the unusual quantization of the Hall conductivity. Fig 4.8 (a) shows the Landau levels for massless Dirac electrons in monolayer graphene and (b) for Schrodinger electrons with two parabolic zones tangent at the point of zero energy [21,22,23,24].

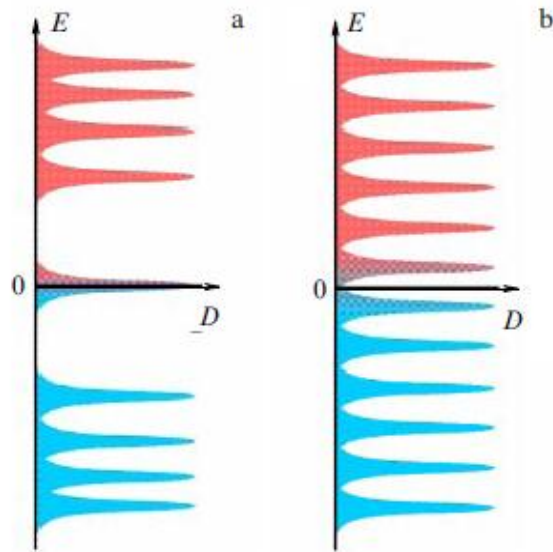


Figure 4.8 Landau levels

An alternative interpretation of the reasons for the half-integer QHE starts with the fact that the superposition of pseudospin and orbital motion results in giving electrons an additional Berry phase of π ; it is accumulated along the cyclotron trajectory. The

additional phase results in a half-period phase shift of quantum oscillations and a shift of Hall plateaus by $1/2$ after the transition to the quantum Hall effect mode [25, 26].

4.3.5 Summary

Graphene became the first and is so far the most vivid representative of a new class of materials two-dimensional crystals. What makes the electron properties of graphene unique is the fact that charge carriers in it resemble massless relativistic fermions and are described by the relativistic Dirac equation, not the Schrodinger equation.

This part reviews several significant electronic properties of graphene, such as ambipolar electric field effect, high carrier mobility, minimum conductivity and quantum hall effect. Graphene immediately emerged as a realistic candidate for the role of one of the main materials for microelectronics in the post-silicon era [27,28].

Chapter 5 Graphene ESD Switch

5.1 Graphene vs Conventional ESD Protection Structures

ESD protection design is a major reliability challenge as IC technologies rapidly migrate to nano nodes. For decades, conventional ESD protection structures relied on PN-junction-based device structures inside silicon to provide active paths to discharge fast ESD transients safely. In principle, an ESD protection structure is a switch that may be turned on by an ESD transient to shunt ESD surges [2]. ESD protection structures are characterized by ESD-critical parameters including triggering voltage, current and time (V_{t1} , I_{t1} , t_1), holding voltage and current (V_h , I_h), discharging resistance (R_{ON}), and failure voltage and current (V_{t2} , I_{t2}) [29]. However, in-Si PN-type ESD protection structures have inherent disadvantages such as parasitic junction leakage (I_{leak}), easily being a few tens of nA for typical ESD structures and becoming intolerable to ICs at nano nodes [29,30,31]. It hence calls for novel ESD protection mechanisms and structures for future ICs. A revolutionary ESD protection concept may be an ideal zero-leakage mechanical switch built above Si that is triggered by ESD transients.

Graphene were widely investigated to make electron devices due to its high electron mobility ($\sim 5000 \text{ cm}^2/\text{V-s}$) [15,16], however, with little practical success due to its zero bandgap nature. On the other hand, its excellent mechanical properties, e.g., Young's modulus of $\sim 1 \text{ T Pa}$ [32] and light mass density, make it possible to build graphene-based mechanical devices. For example, low-current DC graphene mechanical switching phenomena was reported recently [33,34,35]. Targeting for low static power dissipation for ICs, the reported DC graphene switches have major problems: it has slow

switching time (~40ns) and can only survive a few switching times before failure [33,34]. The first dual-polarity transient graphene NEMS (gNEMS) switch ESD protection mechanism and structures are demonstrated [36,37].

5.2 Graphene NEMS ESD Switch

5.2.1 A Novel ESD Concept

Figure 5.1 illustrates a conceptual graphene NEMS switch ESD protection structure and its application scenario. The gNEMS ESD switch is a two-terminal device with a vacuum gap between a conducting substrate (Si or metal serving as the anode, A) at the bottom and a suspended graphene membrane on top serving as the cathode (K). In a typical on-chip ESD protection design, A is connected to an I/O pad and K is connected to the supply or ground buses (VDD, GND). Unlike traditional in-Si PN-type ESD structures, the new gNEMS switch is a mechanical switch built in the BEOL module of ICs above the Si substrates. In normal IC operations, the gNEMS ESD switch stays OFF with minimum parasitic CESD and zero I_{leak} , ideally. As an ESD pulse appears at the I/O, the transient electrostatic force will pull down the graphene membrane to in contact with the anode, hence forming a discharge (ON) path to shunt the ESD surge. After the ESD pulse is over, the elastic force of the graphene will pull the graphene membrane back to its original position, i.e., return to OFF.

The new gNEMS switch have several superior features highly desired for an ESD structure: The high carrier mobility of graphene film ensures low RON. The high graphene thermal conductivity ($\kappa=4.84\sim 5.30\times 10^3\text{W/m}\cdot\text{K}$) [15] prevents over heating

during ESD stressing. The gap-based gNEMS structure minimized ESD-induced parasitic effects including C_{ESD} , noises and I_{leak} . The light mass and relatively high Young's modulus [32,35] allows fast switching, critical to fast ESD protection requirements. The super mechanical strength of graphene also ensure high ESD robustness.

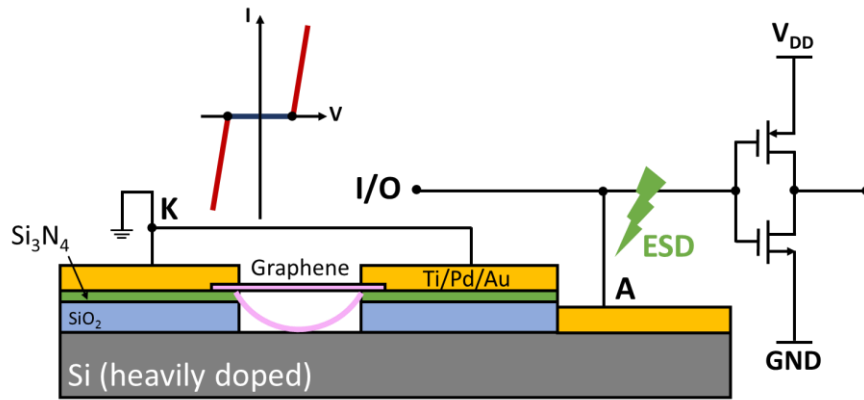


Figure 5.1 Cross-section and circuit scenario for the new gNEMS ESD switch.

Ideally, a gNEMS switch is a dual-polarity device that can significantly reduce the total ESD device head counts in ICs [2]. A big advantage of gNEMS ESD switch is that, because it is an above-IC device, the new gNEMS ESD structures can be placed above Si ICs through 3D heterogeneous integration. Since ESD structures are often very large, the new above-IC gNEMS ESD switch can not only alleviate IC layout headaches, but also save the precious Si assets. This means that normal IC designers will not have to include ESD protection structures during their core circuit designs, which may be handled in the back-end flow of IC designs and fabrication, thus, a paradigm change in on-chip ESD protection designs.

5.2.2 gNEMS ESD Switch Fabrication

A fully CMOS-compatible device fabrication process flow is critical to achieving 3D heterogeneous integration of the proposed gNEMS switches with ICs, hence realize the novel above-IC ESD protection concept.

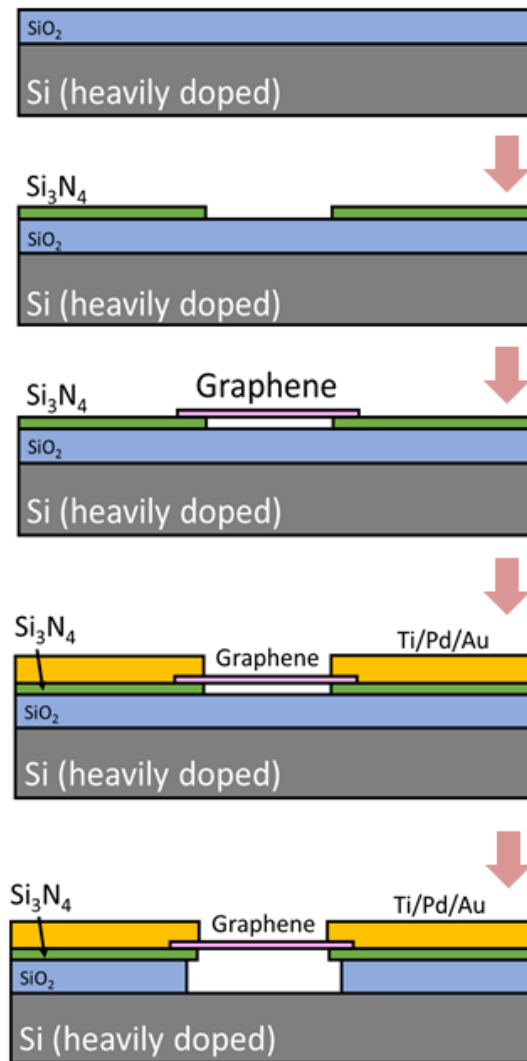


Figure 5.2 New CMOS-compatible gNEMS fabrication process flow.

Figure 5.2 illustrates the device fabrication process flow developed in this work. First, a thin Si₃N₄ layer of 100nm is grown on a SiO₂(300nm)/Si (heavily doped p-type)

substrate by low pressure chemical vapor deposition (LPCVD). The Si₃N₄ was then patterned by etching to define the gNEMS trench. Next, single (or many) layer graphene film was produced by CVD method, suitable for making large area graphene film, followed by Raman evaluation (Figure 5.3). The graphene film was then transferred onto the trenched substrate where graphene is completely attached to the surface to avoid graphene breakage during subsequent steps. Next, the graphene was patterned by oxygen plasma to form graphene beams. The top electrodes were made of Ti/Pd/Au (5/30/50nm) by deposition and etching. Last, the graphene membrane was released by HF vapor etch of SiO₂ using Si₃N₄ as hard mask to form an air chamber, resulting in a gNEMS switch device. Si₃N₄ layer was used to prevent graphene lift-off from electrode pads, because etching into Si₃N₄/graphene interface by HF vapor is negligible compared to SiO₂/graphene interface. The graphene membrane was released using HF steaming to avoid liquid environment to improve device yield and possibly use the hydrophilic property of monolayer graphene [33]. The undercut into the SiO₂ trench by HF vapor is negligible because the SiO₂ layer is very thin.

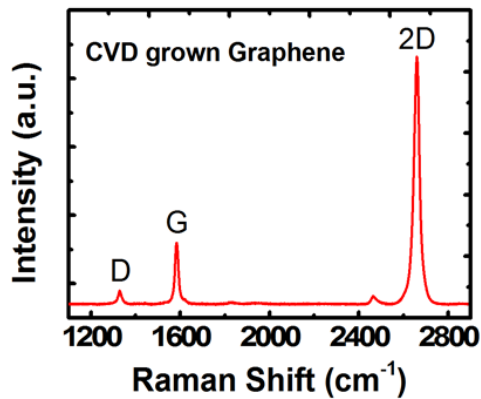


Figure 5.3 Raman spectroscopy of monolayer graphene grown by CVD

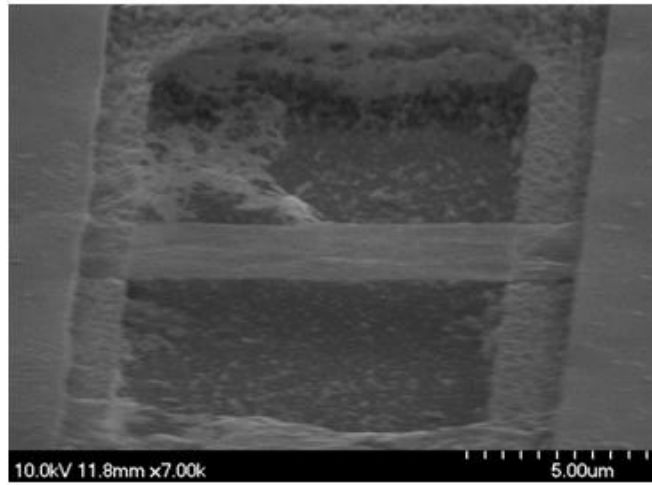


Figure 5.4 SEM images of a sample gNEMS switch.

Figure 5.4 is SEM image of a gNEMS ESD switch fabricated where the suspended graphene membrane is observed.

5.3 Characterization and Discussions

A large number of prototype gNEMS ESD switch structures were designed and fabricated for both static and transient switching characterization. The ESD-critical parameters of the gNEMS switch structures are affected by many factors such as shapes, sizes and dimensions of the chamber and graphene membranes, as well as the fabrication processes and quality of the gNEMS devices. Various device parameters (i.e., design splits) were used for the gNEMS prototypes, including chamber depth ($d=350\text{nm}$), graphene membrane film length ($L= 7/10/15/20\mu\text{m}$) and width ($W=5/7/10\mu\text{m}$).

5.3.1 DC Measurement Results

Static switching effect was first characterized by applying a DC bias between the top and bottom contacts. As the bias increases, the suspended graphene film is pulled-in towards the bottom by electrostatic forces, resulting in DC switching, as shown in Figure 5.5 where DC turn-on voltage (V_{ON}) is related to L of the sample gNEMS devices, likely due to changes in the pull-in forces associated with a varying L .

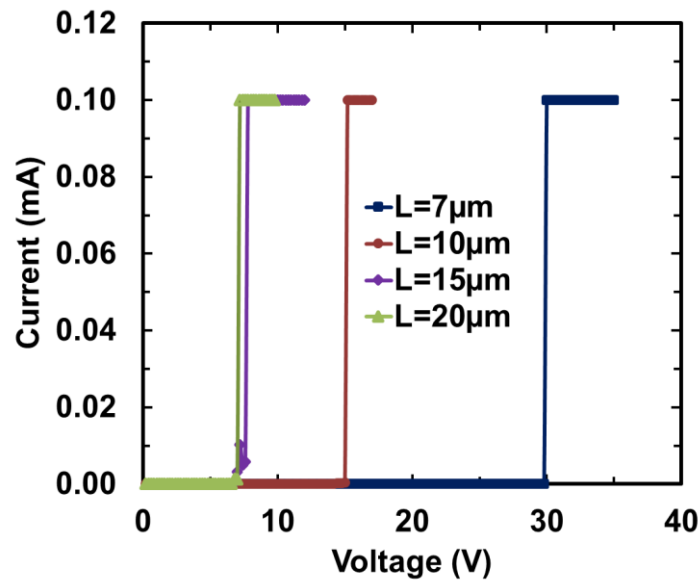


Figure 5.5 DC sweeping test for sample gNEMS devices shows static switching effect with V_{ON} affected by the graphene membrane length (7.0, 7.6, 15, 29.8V).

5.3.2 TLP Measurement Results

For ESD protection operations, transient ESD switching is critical, which were performed using TLP test for human body model (HBM) ESD characterization. Figure 5.6 depicts a transient I-V curve for a sample gNEMS switch ($L=7\mu\text{m}$, $W=5\mu\text{m}$) under TLP stress (ESD pulse rising time $t_r=200\text{ps}$ and duration $t_d=100\text{ns}$), which clearly shows

ultra-fast switching behavior with $V_{t1} \sim 12V$. The transient switching effect induced by fast ESD pulse is different from static switching caused by a DC bias in that transient switching may be greatly affected by extra pulling force associated with the large and sudden change in electrostatic force density induced by an ESD pulse. Hence, a lower V_{t1} threshold and much faster switching time are expected that were confirmed in TLP test.

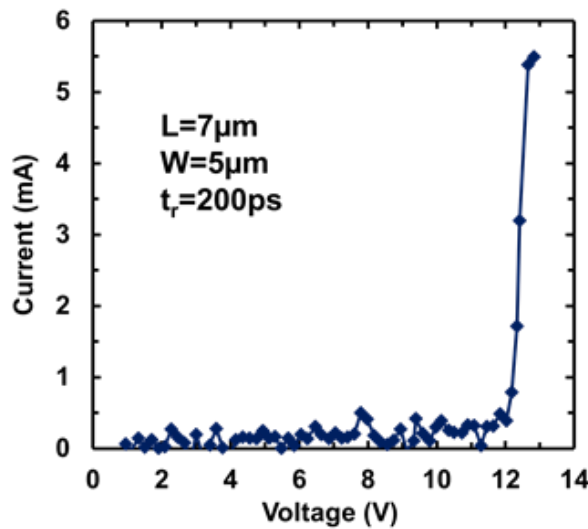


Figure 5.6 Measured I-V curve by TLP pulsing for a prototype gNEMS device shows transient ESD switching with a fast response time down to 200ps.

Uniquely, an ESD switch must be able to respond to extremely fast ESD transients, which is made possible due to the light mass and relatively high Young's modulus of a graphene film. The critical ESD triggering voltage (V_{t1}) values may be accurately controlled by careful designs of L , W and d of a gNEMS switch, which showed a wide range of V_{t1} (7~17.5V) measured. The accurate relationship between V_{t1} and gNEMS switch dimensions requires more research to improve the fabrication processes and device quality.

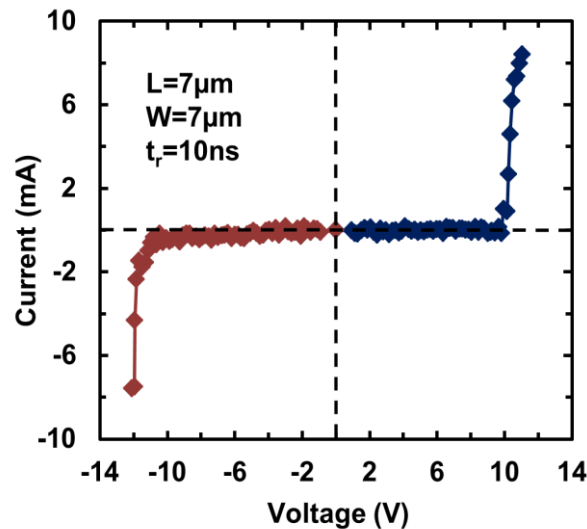


Figure 5.7 Measured I-V curve by TLP for a prototype gNEMS device shows near symmetric I-V switching behaviors desired for ICs.

Figure 5.7 depicts a near symmetric switching I-V behavior, which is highly desirable for full-chip ESD protection to reduce ESD device head counts [2], hence ESD area size and parasitic effects. The slight asymmetry is attributed to the asymmetric prototype device structure used. Measurement shows ultra-low leakage of $I_{leak} \sim 3\text{-}13\text{pA}$ at DC bias of 0.5-3V expected for normal IC operations. TLP testing reveals exceptionally high current handling capability of $I_{max} \sim 108\text{A/cm}^2$ ($>1.5\text{kV}/\mu\text{m}^2$), much higher than existing in-Si PN-type ESD structures (e.g., $\sim 7.5\text{V}/\mu\text{m}^2$ for an SCR ESD device).

5.3.3 Reliability

Reliability of the new gNEMS switch structures were characterized by repeating ESD switching tests by TLP stresses. It was observed that the prototype gNEMS devices

maintained good switching property after more than 30 switching times by TLP tests. Considering that the measured samples were initial prototype devices only, it is expected that both switching performance and reliability of the gNEMS switches can be much improved to enable practical applications. Our on-going optimization research include graphene growth, switch structures and fabrication processes. For example, graphene quality must be controlled for better switch reliability and dielectric leakage has to be avoided.

5.4 Conclusion

The first transient graphene gNEMS ESD switch structures is developed. TLP testing shows symmetric transient switching with ultra-fast ESD response time down to 200ps, adjustable ESD V_{t1} by design splits and low leakage of a few pA. The gNEMS devices remain functional after 30 times of TLP zapping. A CMOS-compatible process flow was developed to allow 3D heterogeneous integration with ICs. The novel 3D above-IC gNEMS ESD switch structure offers a revolutionary on-chip ESD protection solution for future ICs.

Chapter 6 LC-VCO with Magnetic-Enhanced Inductor

6.1 Introduction

Technology innovation is the key to IC design advances. Specifically, the continuous CMOS scaling down has not only significantly improved IC performance and integration, but also made RF CMOS a reality. However, conventional spiral inductors do not benefit from CMOS scaling. The main disadvantages of popular spiral IC inductors include large size, poor Q-factor and inductor density (L-density) due to significant electrical and magnetic losses of the spiral structures, which make design of high-performance low-cost compact RF SoC still unrealistic today. Significant research efforts have been devoted to improve IC inductor performance, including using MEMS structures and integrating magnetic media to reduce energy losses and enhance inductor performance. Novel IC inductor is designed with vertical nano-particle magnetic cores to reduce magnetic losses, hence substantially improved operation frequency, Q-factor and L-density [39,40,41,42]. A prototype LC-VCO using such a new magnetic-cored inductor in an 180nm SOI CMOS is demonstrated [38].

6.2 Vertical Magnetic-Cored Inductors in CMOS

MEMS inductors are not suitable for CMOS integration. Reported magnetic-enhanced inductors typically use lateral magnetic film structures that are unsuitable to CMOS [43-57]. We invented and demonstrated stacked-via vertical magnetic-cored inductors equivalent to inserting an ideal discrete solenoid inductor into the back-end of

CMOS where vertical magnetic core bars can be formed inside conventional spiral IC inductors by replacing the stacked vias within an inductor. A close-loop magnetic circuit serves to minimize magnetic losses associated with spiral inductors. Novel nano particle magnetic materials help to improve operation frequency, Q-factor and L-density.

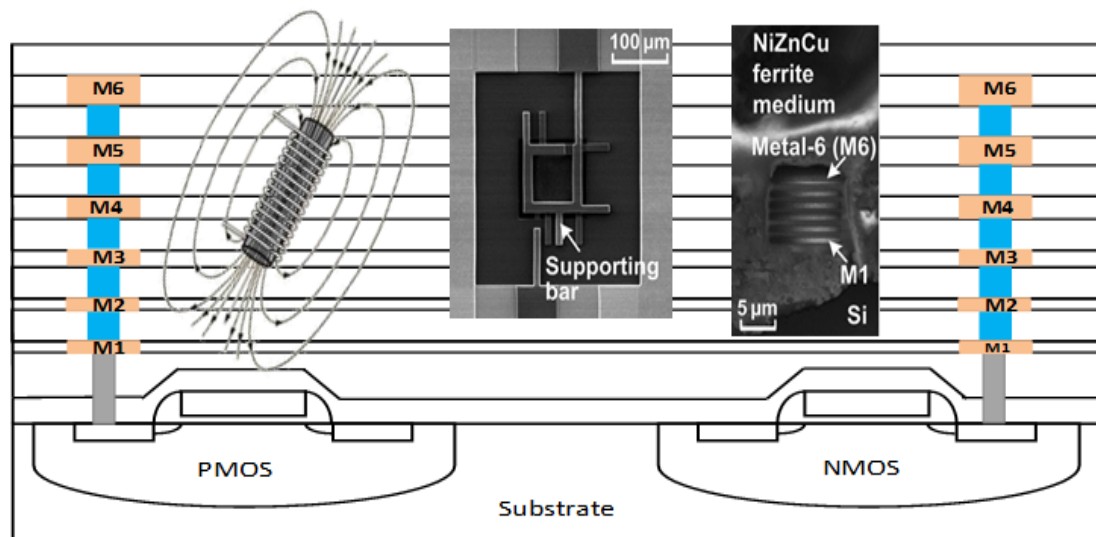


Figure 6.1 A conceptual X-section of new vertical magnetic-cored inductors in CMOS back-end.

Fig 6.1 illustrates the conceptual structure of the new stacked-via vertical magnetic-cored inductors in CMOS. The insets show an ideal discrete solenoid inductor and SEM photos for a 6-metal-layer new inductor filled with vertical nano magnetic core in this work.

Fig 6.2 shows that the vertical magnetic-cored inductors outperformed the reported lateral magnetic-enhanced inductors [43-57].

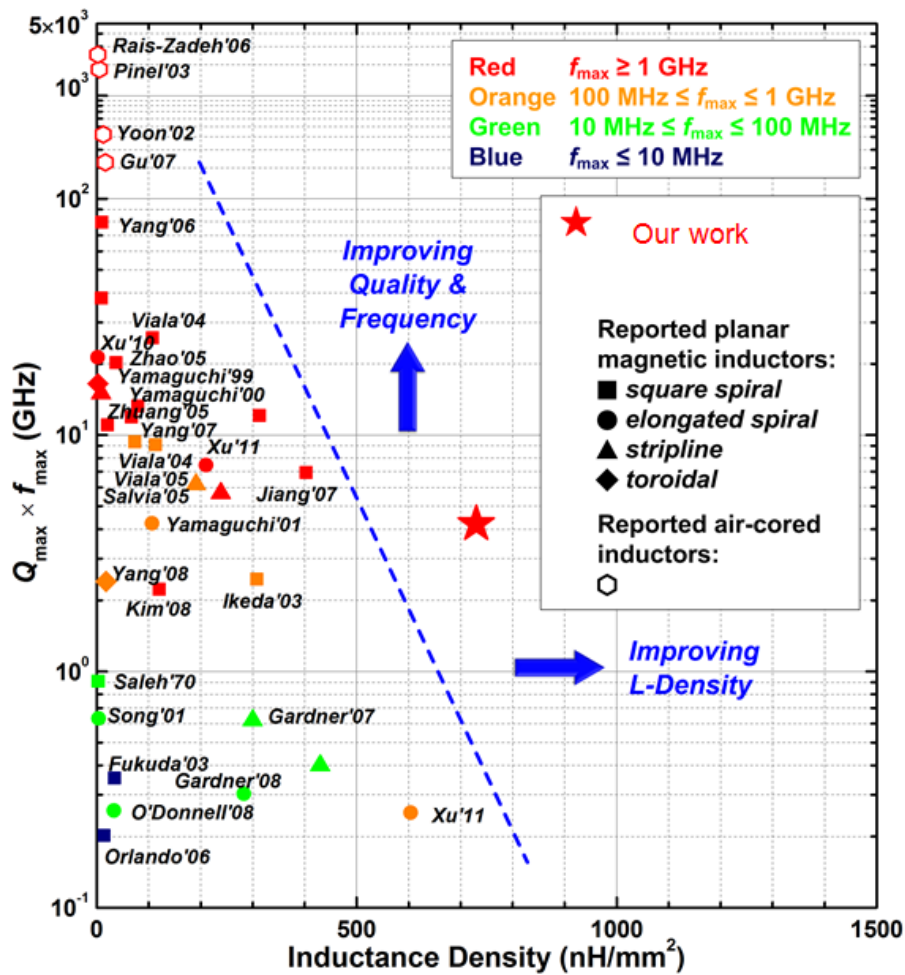


Figure 6.2 Measurements show that the vertical magnetic-cored inductors outperform reported state-of-the-art in L-density and Q_{max}·f_{max} (f_{max} is the frequency at Q_{max}).

6.3 VCO Prototype Using Magnetic Inductor

With substantial progresses in making vertical magnetic-cored inductors, it is important to demonstrate it in a real RF IC. As the first step, a single-layer spiral inductor with magnetic core was used to design an LC-VCO circuit in a foundry 180nm SOI CMOS to show real-world feasibility.

The nano particle magnetic media used is the $Ba_3Co_2Fe_{24}O_{41}$ family materials. The prototype LC-VCO circuit was fabricated in foundry SOI CMOS first. The required magnetic-cored inductor was then fabricated in the IC back-end using a new CMOS-compatible post-process flow developed as illustrated in Fig 6.3. First, the etching windows were formed using photoresist that followed by dry etch (using O_2 plasma) to remove the passivation layer on top of the spiral inductor made in the top metal. The nano particle magnetic materials were then filled into the spiral to cover the whole inductor. A magnetic-cored inductor (mL) was then formed for the LC-VCO. To characterize the mL, inductor without magnetic filling was also made.

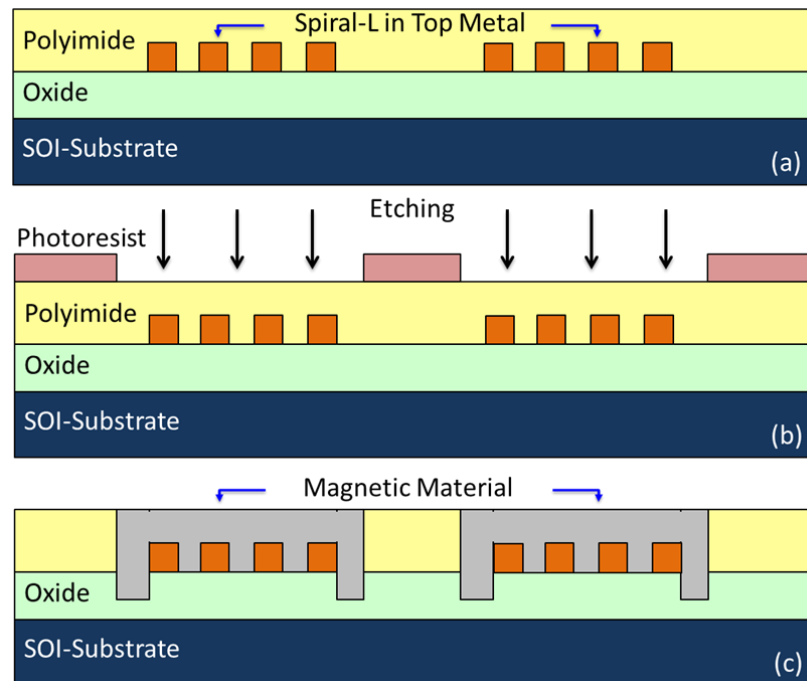


Figure 6.3 Illustration of the new post-CMOS process flow developed to fabricate mL. (a) A spiral inductor in top metal. (b) Patterning and etching by O_2 plasma. (c) Magnetic material filling.

A simple LC-VCO is used to demonstrate real-world RF IC using the new magnetic-integrated inductor without chasing for the best VCO specs. A simple single-layer mL is used in this work to ensure first Si design success. Fig 6.4 depicts the simplified schematic for the VCO based on the popular negative-resistance LC-VCO topology. A PDK spiral inductor was used with a moderate L of around 1.95nH, which has a symmetrical structure in the LC tank for smaller size and better Q-factor. The active circuit is properly designed to form negative resistance in shunt with LC tank resistance R_p in order to oscillate.

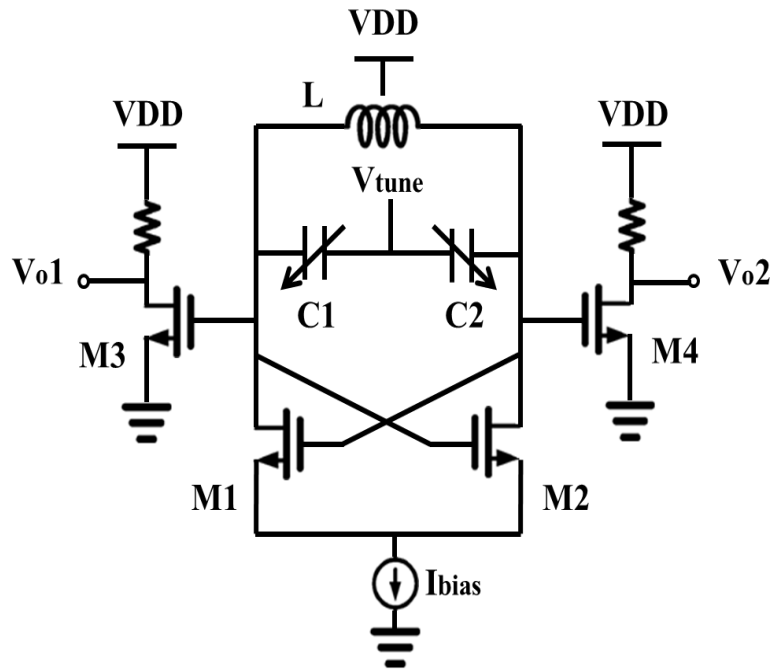


Figure 6.4 Simplified schematic for the VCO and its equivalent circuit. C1 and C2 are 2.5V nMOS capacitor (tuning range from 2pF to 3.8pF). R_p is around 100Ω at 2.6GHz.

Based on the Rael model, the phase noise (PN) of an LC-VCO circuit can be given as

$$\mathcal{L}\{\Delta\omega\} = 10\lg \left[\frac{FkT}{(4I/\pi)} \cdot \frac{1}{L \cdot Q_{\text{tank}}^3} \cdot \frac{\omega_0}{\Delta\omega^2} \right] \quad (20)$$

where F is a complicated experimental parameter, k is the Boltzmann constant, T is temperature, P_{sig} is power of the oscillating signal, ω_0 is the oscillating frequency and $\Delta\omega$ is the offset frequency. It is obvious that, given everything else being the same for the LC-VCO circuits and assuming noises in the LC tank dominate, the new magnetic inductor with higher L and Q factor shall improve the phase noise of a VCO circuit. On the other hand, the oscillation start up condition for an LC-VCO is given as

$$g_m \geq \frac{1}{R_p} = \frac{1}{\omega_0 \cdot L \cdot Q_{tank}} \quad (21)$$

where g_m is transconductance for the driving transistors. It is hence ready to understand that the new vertical magnetic-cored inductor will allow smaller transistor size and current required to start up an LC-VCO circuit, which translates into a smaller die area and lower power consumption given that everything else being the same for the VCO circuit. More importantly, the higher L -density of the new vertical magnetic-cored inductors leads to a much smaller inductor size, which has been a major design challenge for RF ICs using inductors.

6.4 Measurements And Discussions

Fig 6.5 shows die images of the LC-VCO and the magnetic-cored inductor. The die area is $405\mu\text{m} \times 530\mu\text{m}$ including GSG pads.

The split of inductors with and without magnetic material filling were characterized by the de-embedding technique using Agilent 8722ES Network Analyzer.

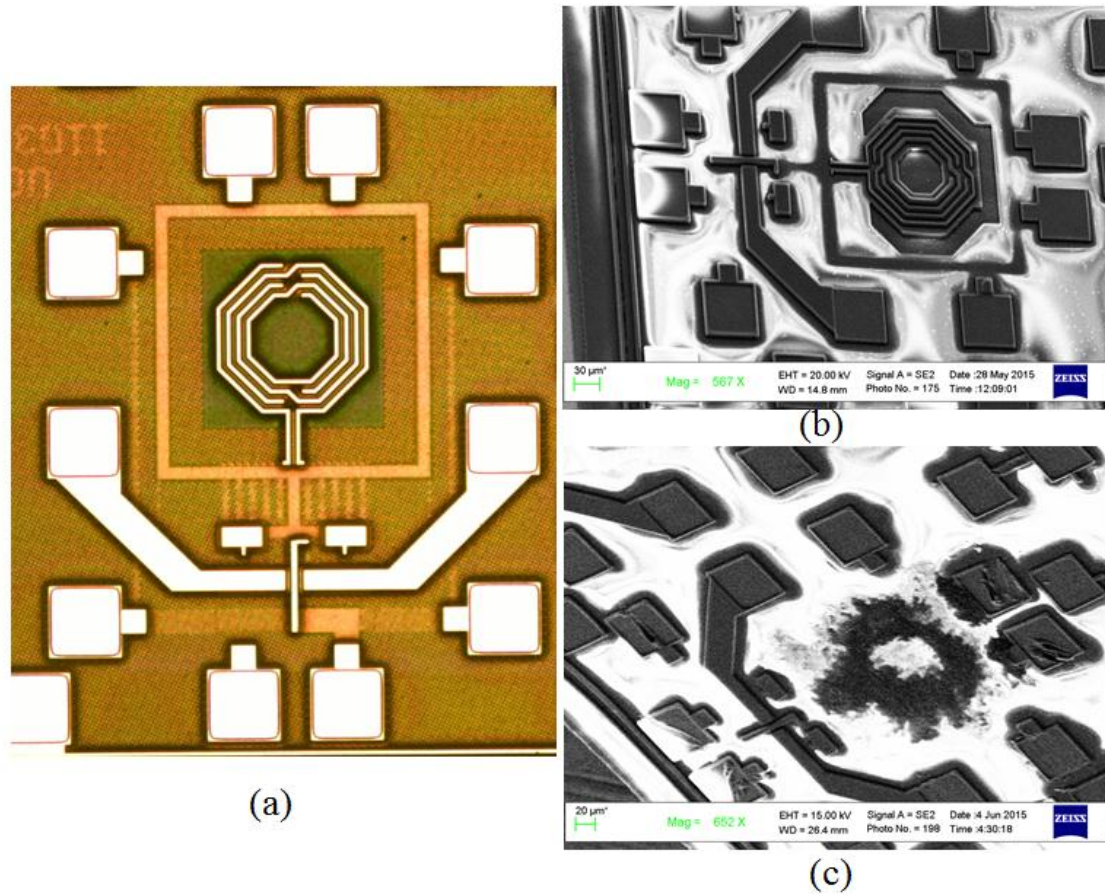


Figure 6.5 Die photo for the LC-VCO (a) and SEM images for the magnetic-cored inductor after removing the passivation layer (b) and nano-particle magnetic material filling (c).

Fig 6.6 compares the measured inductance for the inductors with and without magnetic cores. It is readily observed that the magnetic-cored inductor, though in a not-yet-optimized single-layer prototype format, increases the inductance by up to 16.9% across a wide frequency. The higher L-density obtained is mainly due to reduced magnetic losses associated with the close-loop magnetic circuit of the magnetic-cored inductor structure using nano particle magnetic media. The improvement in L-density continues to f_{max} around 21GHz corresponding to near Q_{max} . The increased L-density

will improve phase noise performance of the LC-VCO, as well as reducing the VCO power dissipation and the die size.

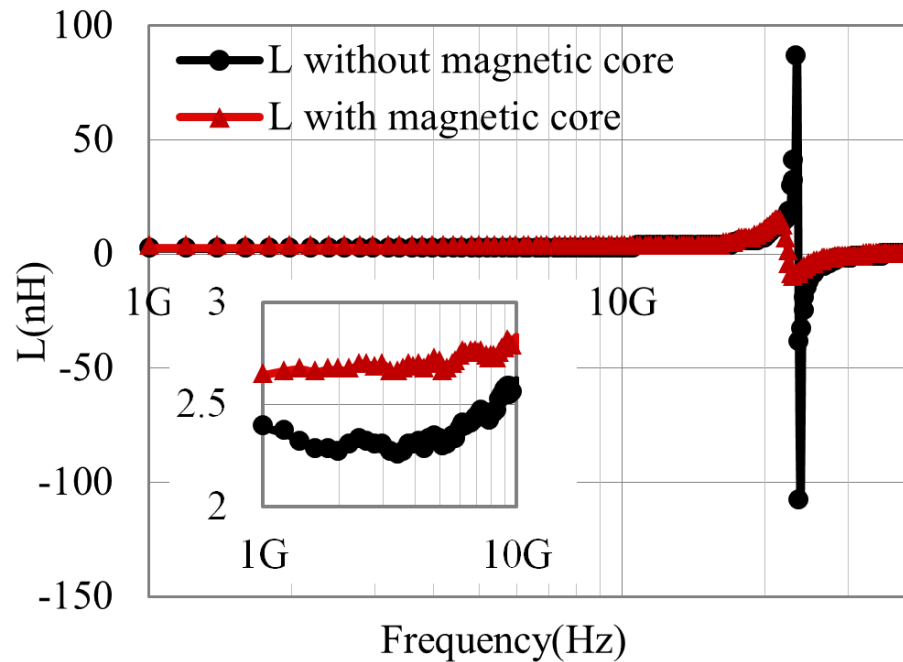
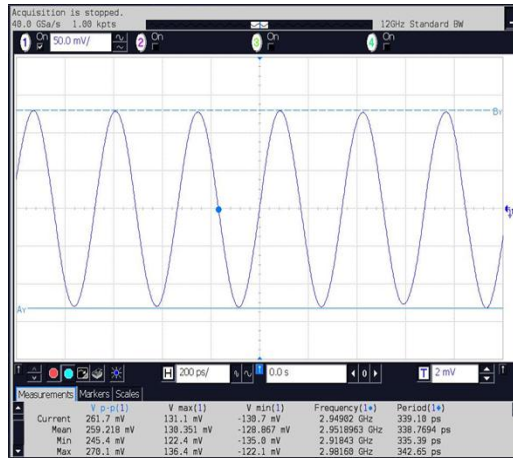


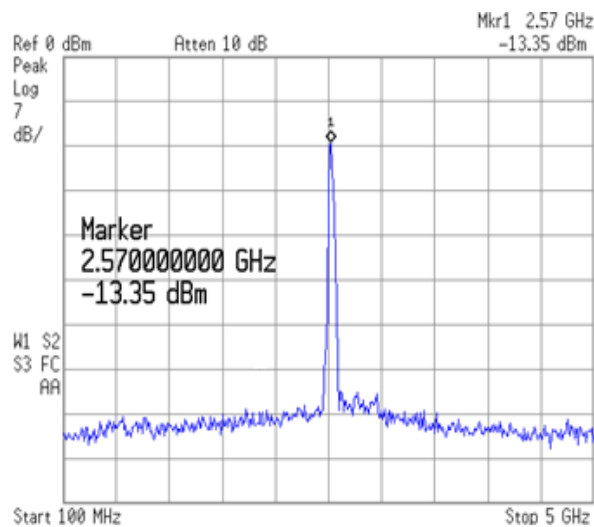
Figure 6.6 Measured inductance of inductors with and without magnetic core shows substantial improvement in L-density across a wide frequency range for the new vertical magnetic inductor.

The VCO splits using inductors with and without magnetic core were designed to operate in the 2.6GHz frequency band. The output power and phase noise of the VCOs are measured using an Agilent E5052B Signal Source Analyser. A common source buffer is used between the VCO and the tester for 50Ω matching.

Fig 6.7 shows the measured waveform and oscillating frequency of 2.57GHz with a tuning voltage of 2.25V.



(a)



(b)

Figure 6.7 Measured waveform of LC-VCO confirms oscillation (a) with oscillating frequency of $\omega_0 \approx 2.57 \text{ GHz}$ at $V_{\text{tune}} = 2.25 \text{ V}$ (b).

By adjusting tuning voltage from 1V to 3V, VCO achieves FTR (frequency tuning range) of 2.24–3.01GHz as shown in Fig 6.8.

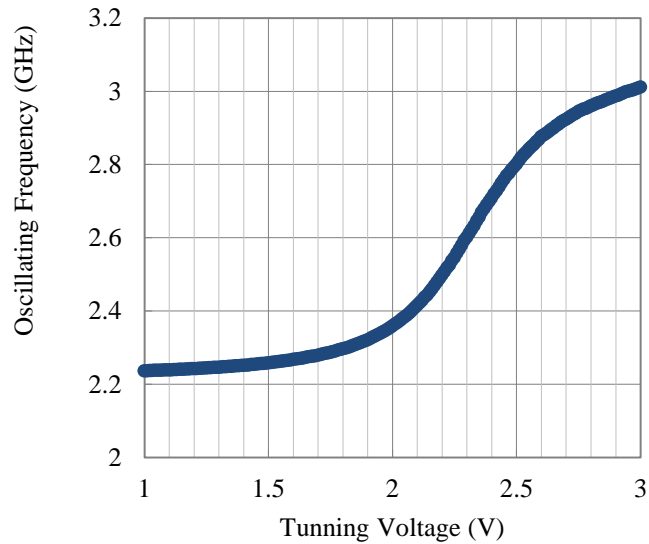


Figure 6.8 Measurement shows a tuning range of 2.24 GHz to 3.01 GHz with V_{tune} changing from 1V to 3V for LC-VCO.

| VCOs | V_{tune} (V) | f (GHz) | PN@1MHz (dBc/Hz) | PN@10MHz (dBc/Hz) |
|--------------|-------------------|--------------|---------------------|----------------------|
| Regular L | 1 | 2.23 | -82.48 | -88.62 |
| | 2 | 2.31 | -81.04 | -105.96 |
| | 3 | 2.98 | -80.28 | -106.97 |
| New mL | 1 | 2.22 | -108.99 | -130.43 |
| | 2 | 2.28 | -89.33 | -115.75 |
| | 3 | 2.92 | -85.27 | -113.49 |

Table 6.1 Measured key Specs for VCOs with regular L and mL

Table 6.1 compares key specs for VCO splits using regular L and new mL. Fig 6.9 shows measured phase noise comparison for the VCO splits at $V_{tune}=2.25V$ and $\omega_0 \approx 2.6GHz$. It is readily observed that the measured phase noises for the VCO using the new

magnetic-cored inductor was reduced significantly for above-1MHz frequency offset. Considering that the two VCOs are exact the same except for using different inductors, the observed reduction in phase noises was apparently attributed to the new magnetic-cored inductor where the close-loop magnetic circuit using nano particle magnetic materials serves to reduce magnetic losses by enhancing the magnetic flux and to improve inductor performance, for smaller inductor sizes.

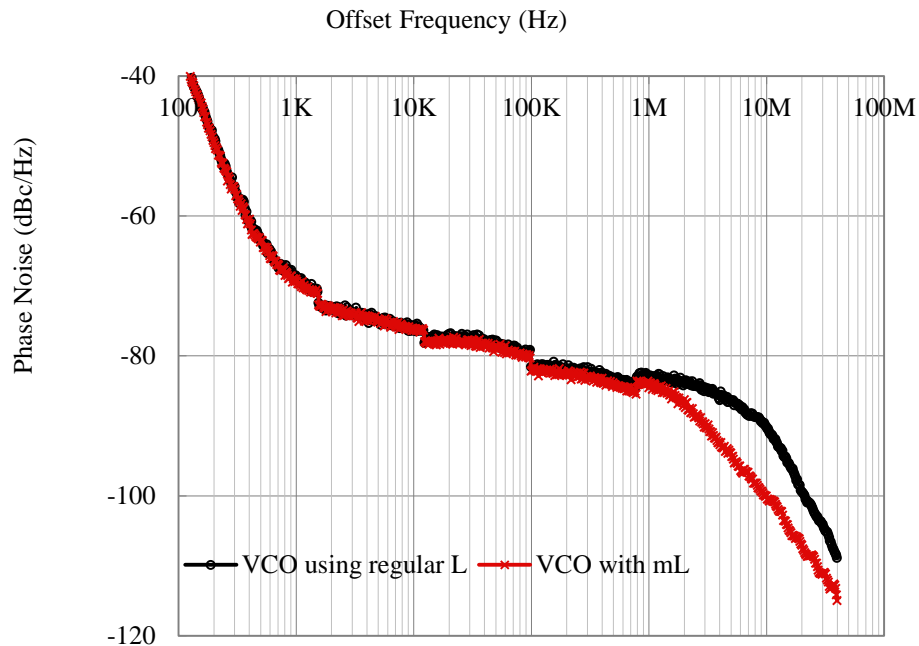


Figure 6.9 Measured phase noises shows improvement of the VCO using mL over the VCO using regular L with $V_{tune} = 2.25V$.

Comparison of the two VCO circuits also shows a shift in oscillating frequency for the VCO using mL, i.e., decreasing from 2.98GHz to 2.92GHz as measured at V_{tune} of 3V, which is attributed to increase in inductance of the magnetic-cored inductor. The tuning range for the VCO using mL changes from 2.23–2.98GHz to 2.22–2.92GHz, which means that if one wants to keep the simulated tuning range for a VCO, a much

smaller inductor is enough if using the new magnetic-cored inductor, hence, a smaller total die size for an VCO. While improvement in both inductors and VCO circuits were observed in this work, it is worth noting that the goal of this design is to show the feasibility by using simple and not-yet-optimized mL and a simple VCO circuit. More improvement is expected with on-going design and process optimization.

6.5 Summary

The first LC-VCO using an integrated vertical magnetic-cored inductor implemented in an 180nm SOI CMOS is designed. The magnetic-cored inductor with nano-particle magnetic media results in a higher L-density of 16.9% as measured, hence smaller size for inductors and VCO circuits. A COMS-compatible process flow was developed to integrate the magnetic inductors into RF ICs. Using a classic LC-VCO topology and a simple single-layer spiral inductor, we demonstrated that the novel vertical magnetic-cored inductor structure proved feasibility of real-world RF ICs using the novel magnetic-core inductors. While research is on-going for improvement, including using multi-layer inductors and more RF IC circuits with optimized process optimization, this work successfully demonstrates the potential of low-cost, high-performance RF SoC using the novel vertical magnetic inductors.

Chapter 7 Conclusion

ESD occurs when objects of different potential are brought together and electrostatic charges transfer in between, resulting in huge current (to ~500A) and voltage (to ~50kV) surges, which can easily damage integrated circuits (IC) and systems. Today, ESD failure is the most devastating reliability problem to ICs, causing the industry billions of dollars annually. On-chip ESD protection is required for all ICs, which is typically placed at I/O and power lines to protect ICs against any ESD damages. In principle, ESD protection works in two basic ways: to provide active low-impedance (low- R_{ON}) discharging paths to shunt the huge ESD currents without over-heating and to clamp the pad-voltage to a safe level to avoid dielectric breakdown.

First part of the dissertation established ESD design flow at 28nm CMOS process. Successful ESD protection requires accurate design of all ESD-critical parameters, i.e., triggering voltage, current and response time (V_{t1} , I_{t1} & t_1); holding voltage and current (V_h & I_h); discharging resistance (R_{ON}); thermal breakdown voltage and current (V_{t2} & I_{t2}); etc.; in order to optimize and predict ESD protection designs on chip. Various design splits are done using TCAD simulation as a design prediction and guideline. Dummy circuits are included to prove the gate is still functional under ESD pulses. Both diode and SCR cases are studied and certain ESD protection levels are obtained from TLP testing results as predicted.

Second part of the dissertation is the novel graphene based ESD protection structures. Unfortunately, traditional ESD protection has inherent disadvantages at nano nodes. These emerging nano ESD challenges will be attacked using novel Graphene-

based ESD protection. A new breed of graphene ESD protection mechanisms and structures feature orders of magnitude lower leakage and parasitic, excellent current surge handling capability and sufficiently fast response time.

A graphene nano electromechanical system (gNEMS) ESD switch device is demonstrated. The high carrier mobility is ideal to achieve extremely low ESD discharging RON and to eliminating the devastating ESD overheating problem. The thin layer results in the smallest mass per unit area of any membrane achievable and thus the fastest response time of an NEMS switch. Another key advantage for graphene NEMS ESD switch is that it will eliminate the significant leakage current inherent to any existing ESD structures, which is a major technical challenge to design of ultra-low power high-reliable ICs for mobile electronics. The proposed novel graphene NEMS ESD switch lead to a paradigm change in ESD protection designs, hence offers a revolutionary solution to the most challenging ESD design problem today. More statistic studies of gNEMS are still on going.

Third part of the dissertation is the VCO design using magnetic cores. Single layer inductor could get inductance increase of 16.9% in SOI technology, showing large potentials of very compact RF SoCs. Future works including multi layers inductors and mature magnetic material filling process, will prove larger amount of area saving for m-L. Also, for VCO designs, NMOS and PMOS coupled pairs could be used to achieve better phase noise performance [58,59]. Shunt capacitance and series inductor also could be an efficient way to lower the thermal noise induced by tail current source [60]. All of above will be considered in the future.

Bibliography

- [1] A. Wang, On-Chip ESD Protection for Integrated Circuits: an IC Design Perspective, Kluwer Academic Publishers, ISBN: 0-7923-7647-1, 2002.
- [2] A. Wang, H. Feng, R. Zhan, H. Xie, G. Chen, Q. Wu, X. Guan, Z. Wang and C. Zhang, "A Review on RF ESD Protection Design", IEEE Trans. Electron Devices, V52, N7, pp. 1304-1311, July 2005.
- [3] L.Lin, X.Wang, H.Tang, Q.Fang, H.Zhao, A.Wang, R.Zhan, H.Xie, G.Chai, B.Zhao, Y.Zhou, G.Zhang, X.Wang, "Whole-Chip ESD Protection Design Verification by CAD", IEEE Trans. Electron Devices, EOS/ESD Symposium, Aug 2009.
- [4] Stadler, Wolfgang, et al. "Test circuits for fast and reliable assessment of CDM robustness of I/O stages." *Microelectronics Reliability* 45.2 (2005): 269-277.
- [5] L. Wang, Rui Ma, et al, "Behavior Modeling for Whole-Chip HV ESD Protection Circuits", Proc. IEEE ISPSD, pp. 182 – 184, 2014.
- [6] L. Wang, Rui Ma, et al, "Scalable Behavior Modeling for SCR Based ESD Protection Structures for Circuit Simulation", Proc. IEEE ISCAS, pp. 2333, 2014.
- [7] L. Wang, X. Wang, Z. T. Shi, Rui Ma, et al, "Scalable Behavior Modeling for 3D Field-Programmable ESD Protection Structures", Proc. IEEE CICC, 2013
- [8] X. Wang, et al, "Post-Si programmable ESD protection circuit design: mechanisms and analysis", to appear, IEEE JSSC, May 2013.
- [9] Rui Ma, et al, "Design and Analysis of New Silicided Nano Crystal Dots Field Programmable ESD Protection Structures in BiCMOS", Proc. IEEE BCTM, pp. 5-8, 2012.
- [10] L. Wang, et al, "Dual-directional nano crossbar array ESD protection structures", IEEE EDL, pp. 111, January 2013.
- [11] M. Ker, et al, "Interference of ESD protection diodes on RF performance in Giga-Hz RF circuits", Proc. IEEE ICSS, p297, 2003.
- [12] Rui Ma, et al, "TLP and HBM ESD Test Correlation for Power ICs", Proc. IEEE EDSSC, 2013.
- [13] Mergens, Markus PJ, et al. "Diode-triggered SCR (DTSCR) for RF-ESD protection of BiCMOS SiGe HBTs and CMOS ultra-thin gate oxides." *Electron Devices Meeting, 2003. IEDM'03 Technical Digest. IEEE International. IEEE, 2003.*
- [14] Chen, Wen-Yi, Elyse Rosenbaum, and Ming-Dou Ker. "Diode-triggered silicon-controlled rectifier with reduced voltage overshoot for CDM ESD protection." *Device and Materials Reliability, IEEE Transactions on* 12.1 (2012): 10-14.

- [15] Geim, A.K., Novoselov, K.S., The rise of graphene, *Nature Materials*, 2007, 6:183-191
- [16] A H. Castro Neto, F. Guinea, K.S. Novoselov and A.K. Geim, The electronic properties of graphene, *Reviews of modern physics*, 2009, 81
- [17] Novoselov, K. S. et al, Electric field effect in atomically thin carbon films, *Science*, 2004, 306:666-669
- [18] Novoselov, K. S. et al, Two-dimensional atomic crystals, *Proc. Natl Acad. Sci. USA*, 2005, 102:10451-10453
- [19] Novoselov, K. S. et al, Two-dimensional gas of massless Dirac fermions in graphene, *Nature*, 2005, 438:197-200
- [20] Schedin, F. et al, Detection of individual gas molecules by graphene sensors, *cond-mat*, 0610809.
- [21] Zheng, Y. & Ando, T, Hall conductivity of a two-dimensional graphite system, *Phys. Rev*, 2002, B65:245420
- [22] Gusynin, V.P. & Sharapov, S.G., Unconventional integer quantum Hall effect in graphene, *Phys. Rev. Lett.*, 2005, 95:146801
- [23] Peres, N.M.R., Guinea, F. & Castro Neto, A.H., Electronic properties of disordered two-dimensional carbon, *Phys. Rev.*, 2006, B73:125411
- [24] MacDonald, A.H., Quantized Hall conductance in a relativistic two-dimensional electron gas, *Phys. Rev*, 1983, B28:2235-2236
- [25] Mikitik, G. P. & Sharlai, Yu.V, Manifestation of Berry's phase in metal physics, *Phys. Rev. Lett.*, 1999, 82:2147-2150
- [26] Zhang, Y., Tan, J.W., Stormer, H.L., Kim, P, Experimental observation of the quantum Hall effect and Berry's phase in graphene, *Nature*, 2005, 438:201-204
- [27] S. Das Sarma et al, Electronic transport in two-dimensional graphene, *Reviews of modern physics*, 2011, 83:4-6
- [28] S V Morozov, K S Novoselov, A K Geim, Electron transport in graphene, *Phys.-Usp*, 2008, 51-744
- [29] Z. Shi, X. Wang, J. Liu, L. Lin, H. Zhao, Q. Fang, L. Wang, C. Zhang, S. Fan, H. Tang and B. Li, "Programmable on-chip ESD protection using nanocrystal dots mechanism and structures", *IEEE Trans. Nanotechnology*, 11(5), pp.884-889, September 2012
- [30] X. S. Wang, X. Wang, F. Lu, C. Zhang, Z. Dong, L. Wang, R. Ma, Z. Shi, A. Wang, A., M. C. Chang and D. Wang, "Concurrent design analysis of high-linearity SP10T switch with 8.5 kV ESD protection", *IEEE J. Solid-State Circuits*, 49(9), pp.1927-1941, September 2014

- [31] C. Zhang, Z. Dong, F. Lu, R. Ma, L. Wang, H. Zhao, X. Wang, S. X. Wang, H. Tang and A. Wang, "Fuse-based field-dispensable ESD protection for ultra-high-speed ICs", *IEEE Electron Device Letters*, 35(3), pp.381-383, March 2014
- [32] J. S. Bunch, A. M. van Der Zande, S. S. Verbridge, I. W. Frank, D. M. Tanenbaum, J. M. Parpia, H. G. Craighead and P. L. McEuen, "Electromechanical resonators from graphene sheets", *Science*, 315(5811), pp.490-493, January 2007
- [33] K. M. Milaninia, M. A. Baldo, A. Reina and J. Kong, "All graphene electromechanical switch fabricated by chemical vapor deposition", *Applied Physics Letters*, 95(18), p.183105, November 2009
- [34] S. M. Kim, E. B. Song, S. Lee, S. Seo, D. H. Seo, Y. Hwang, R. Candler and K. L. Wang, "Suspended few-layer graphene beam electromechanical switch with abrupt on-off characteristics and minimal leakage current", *Applied Physics Letters*, 99(2), p.023103, July 2011
- [35] B. Hajgató, S. Güryel, Y. Dauphin, J.-M. Blairon, H. E. Miltner, G. Van Lier, F. De Proft and P. Geerlings, "Out-of-plane shear and out-of plane Young's modulus of double-layer graphene", *Chemical Physics Letters*, 564 (2013): 37-40. February 2013
- [36] Ma, Rui, et al. "A Dual-Polarity Graphene NEMS Switch ESD Protection Structure." (2016).
- [37] Zhang, Wei. "The Electromechanical Responses of Suspended Graphene Ribbons for Electrostatic Discharge Applications." (2015).
- [38] Rui Ma, et al, "A 2.22–2.92GHz LC-VCO Demonstrated with An Integrated Magnetic-Enhanced Inductor in 180nm SOI CMOS", *IEEE RFIC*, 2016.
- [39] Z. Ni, et al, "Design and Analysis of Vertical Nanoparticles- Magnetic-Cored Inductors for RF ICs", *IEEE TED*, Vol. 60, pp. 1427-1435, April 2013.
- [40] C. Yang, et al, "Investigation of on-Chip Soft-Ferrite-Integrated Inductors for RF ICs — Part I: Design and Simulation", *IEEE TED*, Vol. 56, pp. 3133-3140, Dec. 2009.
- [41] C. Yang, et al, "Investigation of on-Chip Soft-Ferrite-Integrated Inductors for RF ICs — Part II: Experiments", *IEEE TED*, Vol. 56, pp. 3141-3148, Dec. 2009.
- [42] J. Zhan, et al, "Stacked-Spiral RF Inductors with Fully-Filled Vertical Nano-Particle Magnetic Core", *Proc. IEEE RFIC*, pp367-370, 2012.
- [43] M. Yamaguchi, et al, "Improved RF integrated magnetic thin-film inductors by means of micro slits and surface planarization technique", *IEEE Trans. Magn.*, pp.3495, 2000.
- [44] M. Yamaguchi, et al, "Sandwich-type ferromagnetic RF integrated inductor", *IEEE TMTT*, vol. 49, pp. 2331, 2001.

- [45] M. Yamaguchi, et al, "Ferromagnetic RF integrated inductor with closed magnetic circuit structure", Proc. IEEE IMS, pp. 351–354, 2005.
- [46] Y. Zhuang, et al, "Ferromagnetic RF inductors and transformers for standard CMOS/BiCMOS", Proc. IEEE IEDM, pp.475–478, 2002.
- [47] D. S. Gardner, et al, "Integrated on-chip inductors with magnetic films", IEEE Trans. Magn., pp. 2615, 2007.
- [48] B. Viala, et al, "RF planar ferromagnetic inductors on silicon", IEEE Trans. Magn., pp. 1999–2001, 2004.
- [49] B. Viala, et al, "Bidirectional ferromagnetic spiral inductors using single deposition", IEEE Trans. Magn., pp. 3544, 2005.
- [50] Y. Zhuang, et al, "Magnetic properties of electroplated nano/microgranular NiFe thin films for RF application", J. Appl. Phys., vol. 97, 10N305, 2005.
- [51] W. Xu, et al. "Improved freq. response of on-chip inductors with patterned magnetic dots", IEEE EDL, pp. 207, 2010.
- [52] Y. Zhuang, et al, "Integrated solenoid inductors with patterned, sputter-deposited Cr/Fe₁₀Co₉₀/Cr ferromagnetic cores", IEEE EDL, vol. 24, pp. 224–226, 2003.
- [53] R. F. Jiang, et al, "Exchange-coupled IrMn/CoFe multilayers for RF-integrated inductors", IEEE Trans. Magn., vol. 43, pp. 3930–3932, 2007.
- [54] K. Ikeda, et al, "Thin-film inductor for gigahertz band with CoFeSiO–SiO₂ multilayer granular films and its application for power amplifier module", IEEE Trans. Magn., pp. 3057, 2003.
- [55] J. Zhao, et al, "RF planar integrated inductor with permalloy granular films", IEEE Trans. Magn., pp. 2334, 2005.
- [56] J. Salvia, et al, "Tunable on-chip inductors up to 5GHz using patterned permalloy laminates", Proc. IEEE IEDM, pp. 943, 2005.
- [57] D. S. Gardner, et al, "Review of on-chip inductor structures with magnetic films", IEEE Trans. Magn., pp. 4760, 2009.
- [58] Hajimiri, Ali, and Thomas H. Lee. "A general theory of phase noise in electrical oscillators." *Solid-State Circuits, IEEE Journal of* 33.2 (1998): 179-194.
- [59] Lee, Thomas H., and Ali Hajimiri. "Oscillator phase noise: a tutorial." *Solid-State Circuits, IEEE Journal of* 35.3 (2000): 326-336.
- [60] Rael, J. J., and Asad A. Abidi. "Physical processes of phase noise in differential LC oscillators." *Custom Integrated Circuits Conference, 2000. CICC. Proceedings of the IEEE 2000.* IEEE, 2000.