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Near Zero Sub-threshold Swing Nano-Electro-Mechanical Field Effect Transistor with Suspended Ge/Si Core/Shell Nanowire Chanel

A dissertation submitted in partial satisfaction of the
requirements of the degree
Doctor of Philosophy

in

Electrical Engineering (Nanoscale Devices and Systems)

by

Ji Hun Kim

Committee in charge:

Professor Jie Xiang, Chair
Professor Peter M. Asbeck
Professor Prabhakar R. Bandaru
Professor Renkun Chen
Professor Deli Wang

2013

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Chair

University of California, San Diego

2013

DEDICATION

I dedicate this thesis to my loving family.

- *To my wife Mi Kyoung, without your love and devotion, I couldn't have accomplished my degree, I love you so much.*
- *To my daughter Minjeong, your smile always give me strength to carry on.*
- *To my loving parents, you are always on my side when I'm down and out.*

TABLE OF CONTENTS

Signature Page iii

Dedication iv

Table of Contents v

List of Figures vii

List of Tables xiii

Acknowledgement xiv

Vita xvii

Abstract of the Dissertation xix

Chapter 1 Introduction 1
1.1 Static Power Consumption and Sub-threshold Swing 2
1.2 Breakthrough of Sub-threshold Swing Limitation 4
1.3 Nano-Electro-Mechanical System [NEMS] 7
1.3.1 NEM switch with various structures 7
1.3.2 Scaling Challenges 12
1.3.3 Reliability Issue 16
1.4 Summary 17

Chapter 2 Device Fundamentals and Simulation 19
2.1 Device Principle of NEMFET 19
2.2 Device Simulation 22
2.3 Conclusion 27
2.4 Acknowledgement 27

Chapter 3 NEM switch with suspended Nanowire Channel 28
3.1 Introduction 28
3.2 Device Fabrication 28
3.3 Electrical Property 31
3.4 Gate Width Effect 33
3.5 Conclusion 34

Chapter 4 Back Gate NEMFET with Suspended Nanowire Channel 36
4.1 Introduction 36
4.2 Device Design and Fabrication 36
4.2.1 Back Gate NEMFET Scheme 36

4.2.2 Back Gate NEMFET Scheme ······ 39
4.3 Electrical Property of Back Gate NEMFET ······ 43
4.3.1 DC Property ······ 43
4.3.2 AC Property ······ 47
4.4 Conclusion ······ 50
4.5 Acknowledgement ······ 50

Chapter 5 Local Metal Gate NEMFET with Suspended Nanowire Channel ······ 51
5.1 Introduction ······ 51
5.2 Device Design ······ 52
5.2.1 Atomic Layer Deposition for High-*k* Gate Oxide ······ 52
5.2.2 Passivation Effect ······ 58
5.2.3 Selectable Electrode Scheme ······ 58
5.3 Device Fabrication ······ 62
5.4 Electrical Property ······ 65
5.4.1 DC Property ······ 65
5.4.2 AC Property ······ 71
5.5 Conclusion ······ 73
5.6 Acknowledgement ······ 74

Chapter 6 Gate Modulated Thermoelectric Power Factor of Hole Gas in Ge-Si Core Shell Nanowires ······ 75
6.1 Introduction ······ 75
6.2 Device Fabrication ······ 76
6.3 Device Property ······ 77
6.4 Conclusion ······ 87
6.5 Acknowledgement ······ 87

Chapter 7 Conclusion ······ 89

Bibliography ······ 91

LIST OF FIGURES

Fig 1.2:	Schematic V_g-I_g curve of *n-MOSFET*. The I_{off} with same Ion can be decreased with two ways. Line(1) Decrease of *SS*, line(2) Increase of V_{th}. ···	3
Fig 1.2:	Comparison of schematic V_g-I_g curve between ideal switch and MOSFET. ···	4
Fig 1.3:	Tunneling Field Effect Transistor[8], (a) Schematic structure and band diagram of *TFET*, (b) Transfer curve of the fabricated *TFET*. The SS value is 52.*8mV/dec* at room temperature . ···	5
Fig 1.4:	*I-MOS* by W. Y. Choi et. al.[12], (a) Basic structure and band diagram in the *On/Off* states of the n-channel I-MOS, (b) Transfer curve of the fabricated device with 7.*5m*V*/dec* sub-threshold swing.	6
Fig 1.5:	3-terminal NEM relay using suspended CNT cantilever[16], (a) Basic structure, (b) Transfer curve of the fabricated device. ···	8
Fig 1.6:	3-terminal NEM switch using suspended CNT channel[18], (a) 45° tilted SEM image of fabricated NEM switch with triode structure, (b) Transfer curve of the fabricated device with V_d=0.5V. ···	9
Fig 1.7:	2-terminal NEM switch using suspended TiN Cantilever[21], (a) 45° tilted SEM image of fabricated NEM switch, (b) Transfer hysteresis curve of the fabricated device with compliance of 10*n*A. ···	9
Fig 1.8:	2 or 3 terminal NEM switch using vertical CNT[22], (a) 45° tilted SEM image of fabricated NEM switch, (b) Transfer curve of the fabricated device with 3-termianal, (c) Transfer curve of 2-terminal, Inset of (b),(c) is the SEM image in ON state of each device. ···	10
Fig 1.9:	4-terminal relay device with suspended metal gate[23], (a) Schematic of device, (b) Pull-in occurs at Vg=6.1V with SS=1mV, (c) Pull-out occurs at Vg=5. ···	11
Fig 1.10:	Low voltage 2-terminal NEM switch suspended metalized SiC nanowire[24], (a) Low magnification SEM image of device, (b) High magnification SEM image of device, (c), (d), NEMS	

switching events from two 20μm long devices, with $V_{on} \approx$ 3.1 V and 7.0 V, respectively. (e) Measured switching event from a 15 μm long device, with $V_{on} \approx$ 7.8 V. ········ 12

Fig 1.11: Pipe-clip shape NEM switch using top-down process. (a) Schematic process flow, (b) Cross section TEM image of the device[25]. ········ 13

Fig 1.12: Large-scale graphene sheet resonator. (a) Angled scanning electron microscopy (SEM) image of Type A suspended graphene membranes over trenches in silicon oxide. (b) Angled SEM of an array of graphene membranes[26]. ········ 14

Fig 1.13: Direct assembly pattern of SWNT with AFM (a),(b) parallel pattern, (c)Random line structure[28]. ········ 14

Fig 1.14: Nanostructure ensemble using a fabric of SWNT, (a)Schematic of process flow, (b)SEM image of fabricated device[29]. ········ 15

Fig 2.1: Suspended gate FET[37], (a) Schematic structure of SGFET and the gate position change with applied gate voltage(V_g), (b)Analytically and numerically calculated SGFET transfer characteristics (MOSFET characteristic is shown for comparison). ········ 20

Fig 2.2: Normalized restoring and electrostatic forces vs. normalized electrode separation[39]. ········ 21

Fig 2.3: NEMFET structure for the device simulation. The important parameters are summarized in the right side. ········ 23

Fig 2.4: Simulation results of NEMFET, (a)normalized gap thickness vs. Vg, (b)Vg-Id characteristic of NEMFET. ········ 24

Fig 2.5: Comparison of simulated V_g-I_d curve between NEMFET and MOSFET having same dimension for the same I_{on}/I_{off} ratio. ········ 25

Fig 2.6: Comparison of simulated V_g-I_d curve of NEMFET with different doping. ········ 25

Fig 2.7: NEMFET scaling map in various diameter and length of suspended nanowire channel. ········ 26

Fig 3.1: Schematic cartoon of process procedure for NEM switch with suspended nanowire channel. ········ 29

Fig 3.2: SEM image of NEM switch with suspended nanowire channel, (a) plan view, (b) tilt view. ········ 30

Fig 3.3: V_g-I_g measurement scheme of NEM switch with suspended NW channel. ········ 31

Fig 3.4: Measured V_g-I_g curve of NEM switch with suspended NW channel. Inset is the SEM image before measurement(scale bar=500*nm*). ····· 32

Fig 3.5: Analytically calculated V_{pi} vs. L_{ch} plot in t_{gap}=40*nm* with various NW diameter(20/30/40*nm*). ········ 33

Fig 3.6: Analytically calculated V_{pi} vs. Gate coverage of NEM switch with L_{ch}=1300*nm*, NW dia.=20*nm*, and t_{gap}=40*nm.* ········ 34

Fig 4.1: Schematic structure of the device, (a)the back gate NEMFET, (b)the local metal gate NEMFET. ········ 37

Fig 4.2: Schematic cartoon of process procedure for the back gate NEMFET with suspended i-Ge/Si core/shell nanowire channel. ········ 39

Fig 4.3: HRTEM image of the Ge/Si core/shell nanowire. ········ 40

Fig 4.4: Plan-view SEM image of back gate NEMFET, (a) low magnification (scale bar=50*um*), (b) high magnification (scale bar=10*um*). ········ 41

Fig 4.5: SEM image of fabricated back gate NEMFET with suspended i-Ge/Si core/shell nanowire channel, (a) low magnification (scale bar=200*um*), (b) high magnification (scale bar=1*um*). ········ 42

Fig 4.6: Schematics of measurement system, (a) V_d-I_d, (b) V_g-I_d. ········ 44

Fig 4.7: Transfer characteristics of NEMFET, (a) V_d-I_d *curve* (SEM image of measured device, scale bar=1*um*), (b) V_g-I_d *curve.* ········ 44

Fig 4.8: Comparison of Vpi, Vpo value between 3D COMSOL simulation and measurement results of NEMFET. ········ 46

Fig 4.9: Pull-in and pull-out switching of other device, Inset is V_d-I_d curve. ·· 46

Fig 4.10: Schematics of measurement system for one-source method.·········· 48
Fig 4.11: Measurement results of resonant frequency. (a)Frequency vs. I_{mix} plot in different AC drive amplitude. The data was taken at V_g^{dc}=1V. The each line is the fitted value with the analytical equation of I_{mix}. (b) The dependency of resonant frequency. ····························· 49
Fig 5.1: Schematic structure of ALD system with TDMAH and H_2O source.·· 53
Fig 5.2: Plan-view SEM of HfO2 film deposited on Si substrate with ALD system. The deposition cycle number is varied with (a)100cycle, (b)150cycle, (c)300cycle, (d)500cycle(The scale bar is 500nm). ····· 54
Fig 5.3: ALD cycle number vs. measured thickness plot of HfO2 film. The thickness is measured with ellipsometer . ······························· 55
Fig 5.4: MIS capacitor characterization, (a) Schematic structure of device, (b) Measured dielectric constant with ALD cycle number. ············ 56
Fig 5.5: Oxide leakage current property with different cycle number. ········· 56
Fig 5.6: i-CSNW planar FET with back gate.(a) Schematic structure of the device. The measurement is done with or without passivaition, (b) Plan-view SEM of the device(Scale bar is 1*um*). ······················ 58
Fig 5.7: Comparison of V_g-I_d characteristic between passivation and no-passivation planar FET with i-CSNW channel. ························ 59
Fig 5.8: Parasitic conduction path of NEMFET, (a)Tilt-SEM after nanowire transfer. The position of nanowire is random(Scale bar=2*um*), (b)V_g-I_d curve at V_d=1V of parasitic channel without anchor electrode. ···· 60
Fig 5.9: Schematic design of selectable electrode scheme. ······················ 61
Fig 5.10: Schematic process flow of NEMFET with suspended i-CSNW channel. ·· 63
Fig 5.11: SEM images of fabricated NEMFET device with different magnification. (a) low magnification(scale bar=100*um*), (b)mid magnification(scale bar=10*um*), (c) mid magnification(scale bar=5*um*), (d)high magnification(500*nm*). ····························· 64

Fig 5.12: V_g-I_g curve of NEMFET with abrupt "pull-in", "pull-out" behavior. 66
Fig 5.13: Simulated V_g-I_g curve of NEMFET with different doping level. The condition is summarized in chapter. 2. ································ 67
Fig 5.14: V_g-I_g curve of NEMFET with multiple switching behavior. ·········· 68
Fig 5.15: V_g-I_g curve of NEMFET with 130times switching behavior. ·········· 68
Fig 5.16: Increase of *Vpi* in first a few switching in various devices. ·········· 69
Fig 5.17: Switching number vs. V_{pi} and V_{pi}-V_{po} plot of 130times switching NEMFET device. ·· 53 69
Fig 5.18: The plot of I_{mix} vs. drive frequency with various V_{ac}^{d} amplitude. The symbols are the measurement data, and the line is I_{mix} fitting. ········ 71
Fig 5.19: The plot of V_{ac}^{d} amplitude vs. I_{peak}. ····································· 72
Fig 5.20: The plot of V_g vs. f_o and V_{ac}^{d} vs. f_o of NEMFET device. ················ 73
Fig 6.1: Core shell NW samples and devices. (a) Shematic structure and band diagram of CSNW, (b)HRTEM of CSNW, (c) SEM image of the device used for the gated electrical conductivity and thermopower measurements. ·· 72 77
Fig 6.2: Gate modulated electrical and thermopower measurements of the NWs. (a) V_d-I_d plot, (b) Seebeck voltage V_S vs. temperature difference between electrodes 2 & 3 under various gate voltages. ··· 79
Fig 6.3: Source drain current and (b) electrical conductivity of the NWs as a function of gate voltage. ·· 80
Fig 6.4: Gate modulated hole concentration and mobility of the NWs. (a) Hole concentration as a function of gate voltage, (b) Mobility vs. hole concentration of the NWs along with p-type Ge (from Ref. [67]). ··· 82
Fig 6.5: Temperature dependent mobility of the NWs and bulk p-Ge. The bulk Ge data are adapted from Ref. [67] with the following dopant (Gallium)concentrations: (a)1.1×10^{18}cm^{-3}, (b)4.9×10^{18}cm^{-3}, (c)1.2×10^{19}cm^{-3}, (d) 5.8×10^{19}cm^{-3}, (e)1×10^{20}cm^{-3}. ··················· 84

Fig 6.6: Gate modulated thermopower of Ge-Si core shell NWs. (a)Seebeck coefficient of the NWs under various gate voltages. (b)Seebeck coefficient as a function of hole concentration of the NWs and bulk p-Ge. ········ 85

Fig 6.7: Power factor ($S^2\sigma$) vs. carrier concentration of the NWs and bulk p-Ge. ········ 86

LIST OF TABLES

Table 3.1: Important parameters of NEM switch with suspended NW channel. 32

Table 4.1: Comparison of the characteristics between the back gate NEMFET and the local metal gate NEMFET. ······································ 37

Table 4.2: Important parameters of back gate NEMFET switch with suspended CSNW channel. ·· 43

Table 5.1: The Important problems of back gate NEMFET and the solution. ··· 51

Table 5.2: Process condition of HfO_2 film with ALD system. ····················· 53

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I still remember the day clearly when I arrived in San Diego Airport. Clear sky, hot sun light with cool breeze from the sea, people who dressed up lightly with smiling, these were the first things I met in San Diego. I was nervous a little bit, but I felt so good. “I’m in California!.”

Five years have passed. There were many happenings around me, and sometimes I was very disappointed with myself - passive manner, unfluent English, misjudgments, indolence, and so on. But, now I’ve come to understand this was the way to learn how to live the life wisely, and I must keep learning through my whole life. I’m sure the experience and study within this five-year will be the important nourishment for rest of my life.

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    *These authors contributed same.
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- **Ji-Hun Kim***, Zack C. Y. Chen*, Soonshin Kwon, and Jie Xiang, “Steep Subthreshold Slope Nanoelectromechanical Field-Effect Transistors with Nanowire Channel and Back Gate Geometry”, to appear in *Device Research Conference (DRC),* 2013.

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- Soonshin Kwon, Zack C. Y. Chen, **Ji-Hun Kim**, and Jie Xiang, "Misfit-Guided Self-Organization of Anticorrelated Ge Quantum Dot Arrays on Si Nanowires," *Nano Letters,* vol. 12, pp. 4757-4762, 2012/09/12 2012.

- Jaeyun Moon*, **Ji-Hun Kim***, Zack C. Y. Chen, Jie Xiang, and Renkun Chen, “Gate-Modulated Thermoelectric Power Factor of Hole Gas in Ge-Si Core-Shell Nnowires”, *Nano letters,* vol.13, pp.1196-1202, 2012.

  *These authors contributed same.

- Mattew C. Wingert, Zack C. Y. Chen, Edward Dechaumphai, Jaeyun Moon, **Ji-Hun Kim**, Jie Xiang and Renkun Chen, “Thermal Conductivity of Ge and Ge–Si Core–Shell Nanowires in the Phonon Confinement Regime,” *Nano Letters.* vol 12, pp.5507-5513, 2012.
- **Ji-Hun Kim**, Zack C. Y. Chen, Soonshin Kwon, and Jie Xiang, “Three-Terminal Nanoelectromechanical Field Effect Transistor with Abrupt Subthreshold Slope”, Submitted, *Nature*, 2013 .

ABSTRACT OF THE DISSERTATION

Near Zero Sub-threshold Swing Nano-Electro-Mechanical Field Effect Transistor with Suspended Ge/Si Core/Shell Nanowire Chanel

by

Ji Hun Kim

Doctor of Philosophy in Electrical Engineering (Nanoscale Devices and Systems)

University of California, San Diego, 2013

Professor Jie Xiang, Chair

The static power consumption became one of the key limiting factors on the shrinkage of feature size of VLSI circuit using CMOS technology. One major reason of high static power consumption is the off-state sub-threshold leakage current of the transistor. At room temperature, the possible steepest sub-threshold swing (SS) for turning off the transistor, is limited to 60 mV/decade due to a constant fundamental thermal dynamical limit (k_BT/q) that is not scalable with reduced dimension. This limitation is inherent to CMOS because its off-state is governed by thermally activated

diffusive current over a potential gate-controlled potential barrier. Completely different switching mechanism such as using the mechanical degree of freedom is necessary to break the SS limit. Previous studies using nano-electro-mechanical-system (NEMS) have shown suspended-gate MOSFET (SG-MOSFET) as logical switch, while we have previously proposed a suspended nanowire (NW) channel FET (NEMFET) with low pull-in voltage(V_{pi}) and high I_{on}/I_{off} ratio due to the flexibility of nanowires. Here we report the first demonstration of a NEMFET device using suspended Ge/Si core/shell nanowire channel. The NEMFET channel is suspended over a local metal gate with the air gap thickness defined by the thickness of the supporting source/drain electrodes. DC transfer characteristics on multiple switching NEMFET demonstrates close-to-zero SS (<6mV) at room temperature with the slope only limited by measurement equipment resolution. Furthermore, we employed electrostatic actuation to study the AC mechanical response of the nanowire channel. Using the NEMFET as a signal mixer we characterized the resonant frequency and the speed of NEMFET device to be 125.9 MHz.

Chapter 1

Introduction

In VLSI technology, the aggressive shrinkage of device dimension is still going on for better device performance and productivity. With this motivation, the physical gate length has already scaled down to 20~25*nm* with sub-1V V_{dd} in CMOS technology[1]. In application, with the skyrocketing of the mobile electronics market, the power consumption has become the one of most important factor of VLSI technology. The power consumption can be divided to the dynamic power consumption and the static power consumption. The dynamic power, which arises from the repeated capacitance charge and discharge on the output of the billions of gates in today's IC, can be scaled down with gate length shrinkage successfully with the principle of constant-field scaling[2], but the static power consumption has a limitation as I_{off} can't be scale down due to it's thermodynamic nature[3, 4].

I_{off} is simply controlled by sub-threshold swing(*SS*) value of the device, and CMOS has a minimum limitation in *SS* as 60*m*V*/dec*. A few different types of device was introduced to overcome this thermodynamic limit of CMOS using band to band tunneling, impact ionization, and nano-electro-mechanical system(NEMS).

In this thesis, I will demonstrate the nano-electro-mechanical field effect transistor(NEMFET) using suspended intrinsic Ge/Si core/shell nanowire channel, which combines the mechanical motion of elements to electrical property. This can be one possible gain mechanism to overcome the 60*m*V *SS* limitation.

1.1 Static Power Consumption and Sub-threshold Swing

The static power consumption became one of the key limiting factors on the shrinkage of feature size of VLSI circuit using CMOS technology[5]. An equation that T. Mudge presented defines overall power consumption as the sum of dynamic and static power[6],

$$P = ACV^2f + VI_{leak} \tag{1.1}$$

where the first term is the dynamic power lost from charging and discharging the processor's capacitive loads, and the second term is the static power lost due to leakage current, I_{leak}. V is the supply voltage, f means the operation frequency, and I_{leak} is the leakage current in off state. In Equation (1.1), its V^2 factor suggests deducing supply voltage as the most effective way to decrease power consumption, and V_{dd} has been scaled down successfully less than 1V with the continuous efforts to shrink the device dimension and circuit perspectives. But, this shrinkage of device geometries exacerbate leakage current, so static power begins to dominate the power consumption equation in IC design. I_{leak} can be expressed as

$$I_{leak} = I_{sub} + I_{ox} \tag{1.2}$$

where I_{sub} is subthreshold leakage current and I_{ox} is the gate oxide leakage current. I_{ox} is very important parameters in CMOS technology, but as it's not a main topic of this thesis, let's concentrate on I_{sub} term. Fig 1.1 shows the representative V_g-I_g curve of *n-MOSFET* in semi-log scale. In the figure, I_{off} is the I_{sub} at V_g=0. In given V_g-I_g curve, there are two simple way to decrease I_{off} current with maintaining same I_{on}. The first is increasing V_{th}, marked as (1) line, and the second is decreasing the sub-threshold swing(*SS*), marked as

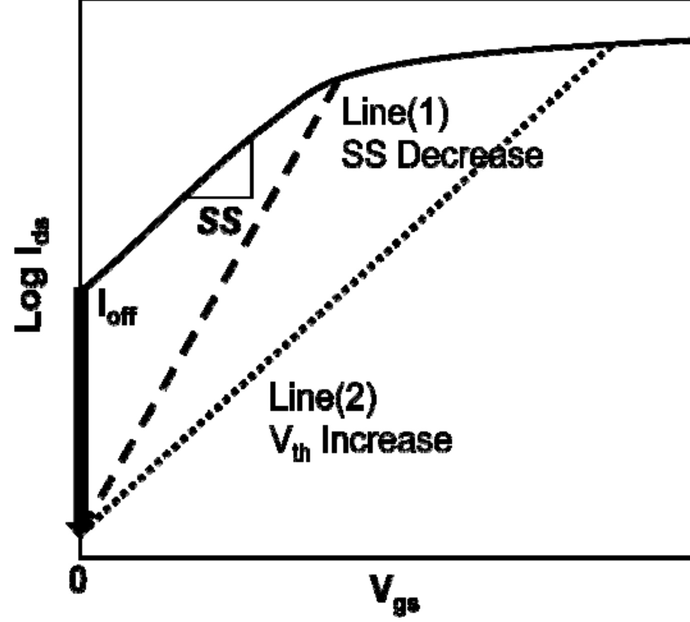

Fig 1.1: Schematic V_g-I_g curve of *n*-MOSFET. The I_{off} with same Ion can be decreased with two ways. Line(1) Decrease of *SS*, line(2) Increase of V_{th}.

(2) line. But increasing V_{th}, the device speed is decreased in return. The Equation (1.3) shows the relation between operating frequency *f* and V_{th} of the device[6],

$$f \propto \frac{(V - V_{\mathrm{th}})^{\alpha}}{V} \tag{1.3}$$

where *V* is the supply voltage, and exponent α is an experimentally derived constant. If we consider the supply voltage *V* is continuously scaled down, and V_{th} term is inside of exponential term, increasing V_{th} can't be a solution for the I_{off} decrease.

Sub-threshold swing indicates how fast the channel can be off with the gate signal. SS can be expressed with the equation below

$$SS = \left(\frac{d(log_{10} I_{ds})}{dV_g}\right)^{-1} = 2.3\frac{mkT}{q} = 2.3\frac{kT}{q}\left(1 + \frac{C_{dm}}{C_{ox}}\right) \tag{1.4}$$

, and typically 70-100*m*V/decade as *m*=1.1~1.5 practically. Even in ideal switch, *m* =1, *SS* can't be decreased under 60*m*V in room temperature. This minimum limitation of *SS*

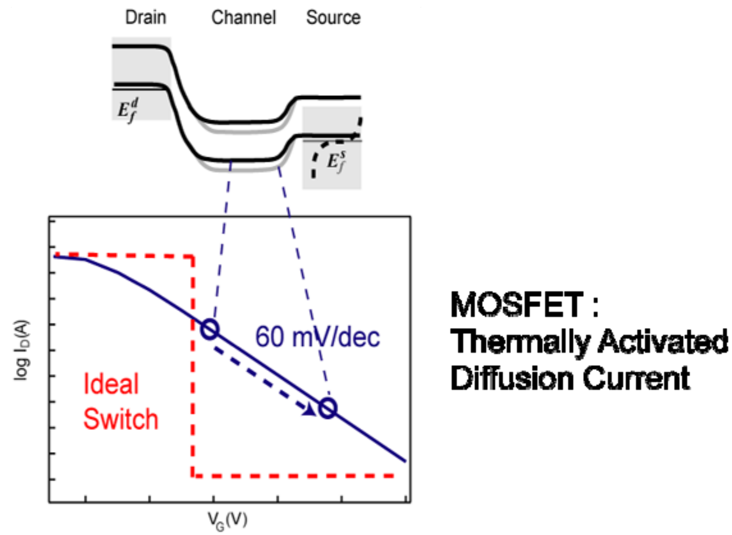

Fig 1.2: Comparison of schematic V_g-I_g curve between ideal switch and MOSFET.

value comes from the thermally activated diffusion current terms over the channel energy barrier. Fig 1.2 shows the different switching behavior of ideal switch and real transistor. This thermodynamic limit of *SS* prohibits the further decrease of I_{off} in CMOS technology. Going back to Fig 1.1, the I_{off} is varied with *SS* exponentially.

$$I_{off} = I_{th} \times 10^{\frac{-V_{th}}{SS}} \tag{1.5}$$

And,

$$P_{static} = VI_{leak} \propto exp\,(-\frac{V_{th}}{SS}) \tag{1.6}$$

In conclusion, the static power consumption varied exponentially with *SS* of the device.

1.2 Breakthrough of Sub-threshold Swing Limitation

As reviewed in chapter 1.1, the decrease of SS is the most efficient way to suppress the static power consumption without any drawbacks. But, at room temperature, the sub-threshold swing (*SS*), the steepest transition rate for turning off the transistor, is

limited to 60*m*V/*decade* due to a constant fundamental thermal dynamical limit (k_BT/q) that is not scalable with reduced dimensions. This limitation is inherent to CMOS because its off-state is governed by thermally activated diffusive current over a gate-controlled potential barrier. There have been some demonstrations of novel switches and FETs to overcome the thermodynamic limits of MOSFETs using band-to-band tunneling[7-10], impact ionization[11-14], or nano-electro-mechanical–system(NEMS) [15-18] .

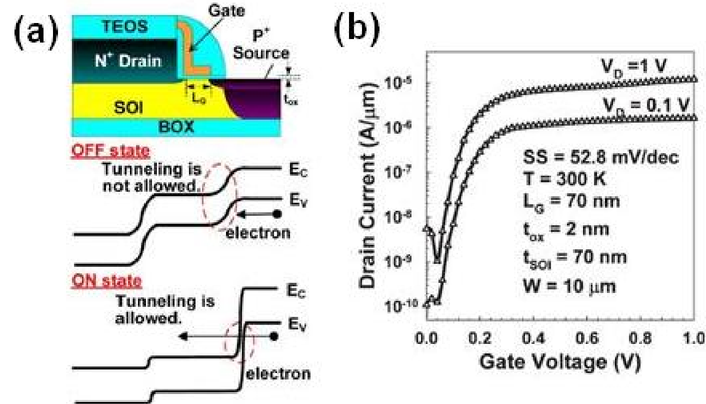

Fig 1.3: Tunneling Field Effect Transistor with *L*-shape gate[8], (a) Schematic structure and band diagram of *TFET*, (b) Transfer curve of the fabricated *TFET*. The SS value is 52.*8mV/dec* at room temperature.

Tunneling FET(TFET) is a gated p-i-n diode operating under reverse bias, as shown in Fig 1.3[8]. Different from MOSFET using thermal carrier injection, TFET use band-to-band tunneling phenomenon as a source carrier injection mechanism. In *OFF* state, the gap between conduction band(E_c) and valance band(E_v) is so wide that tunneling current is limited with only very small leakage current. With the increase of gate voltage, E_c and E_v come to close enough to allow a huge tunneling current. As the

carrier injection mechanism is different from MOSFET, TFET can achieve the steep *SS* value lower than 60*m*V. However, *SS* increases rapidly with gate voltage and thus steep *SS* only occurs within limited current, or gate voltage range and the average *SS* is still relatively high[9]. In addition, low I_{on} is another issue due to the poor tunneling probability of silicon[19].

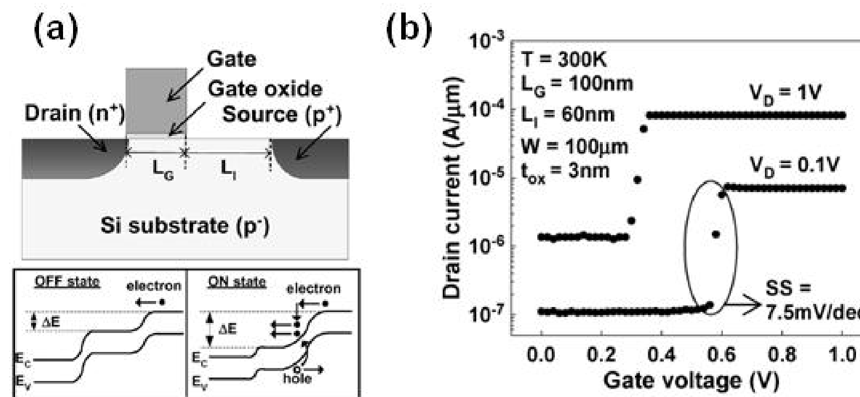

Fig 1.4: *I-MOS* by W. Y. Choi et. al.[12], (a) Basic structure and band diagram in the *On/Off* states of the n-channel I-MOS, (b) Transfer curve of the fabricated device with 7.5*m*V/*dec* sub-threshold swing.

Impact-Ionization MOS(IMOS) uses modulation of the breakdown voltage of a gated p-i-n structure in order to switch from *OFF* to *ON* state and vice versa. Since impact-ionization is an abrupt function of the electric field, the device has a subthreshold slope much lower than *kT/q*[11]. Fig 1.4 shows the basic structure and operating principle of the n-channel I-MOS[12]. *I-MOS* has two big difference compared with MOSFET, opposite doping in the source/drain and the *i*-region which is not completely overlapped by the gate. In the *OFF* state, when the gate is biased below the threshold voltage, in the source cannot acquire enough energy for impact ionization. Thus, the leakage current is

dominated by the reverse current of the *p-i-n* diode. However, with the gate voltage above the threshold, the ON state utilizes the electrons which acquire the enough energy for the impact ionization that gives rise to avalanche breakdown. As the *p-n* junction barrier lowering is not the mechanism of current flow control, I-MOS can realize the subthreshold swing less than 60*m*V/*dec* in room temperature. But, it needs high supply voltage to induce avalanched breakdown and process difficulty in self-aligned fabrication.

1.3 Nano-Electro-Mechanical System[NEMS]

NEMS is the device exploiting the mechanical degree of freedom with movable component like gate or channel. NEMS architectures are being explored as components in various application like switch, actuator, resonator, and senor. As the NEM switch has related to this thesis directly, I'll discuss about the NEM switch in detail here.

1.3.1 NEM switch with various structure

The NEM switch is the old and common idea in MEMS using pull-in/pull-out movement of suspended components. NEMS technologies are being investigated because they offer reduced leakage currents which leads to reduced power consumption and improved I_{on}/I_{off} ratio. NEM switch also relatively insensitive to radiation, temperature and external electric field[20]. So, NEM switches are studied as components in various transistor, memory, logic and sensing applications.

The previous studies have shown the abrupt on/off switching, and minimized *SS* with movable gate or channel with various materials like metal, carbon nanotube(CNT),

silicon carbide(SiC), nanowire(NW), and various structure like crossbar, cantilever, suspended channel, or vertical pillar. The basic switch structure is 2-terminal(one for bias, one for ground), but use 3-terminal or 4-terminal to limit the current path between source and drain only without intervention of gate signal and gate leakage. The suspended moving part has a various shape, too, like thin film, tube, wire, beam, u-shape, pipe clips, etc.

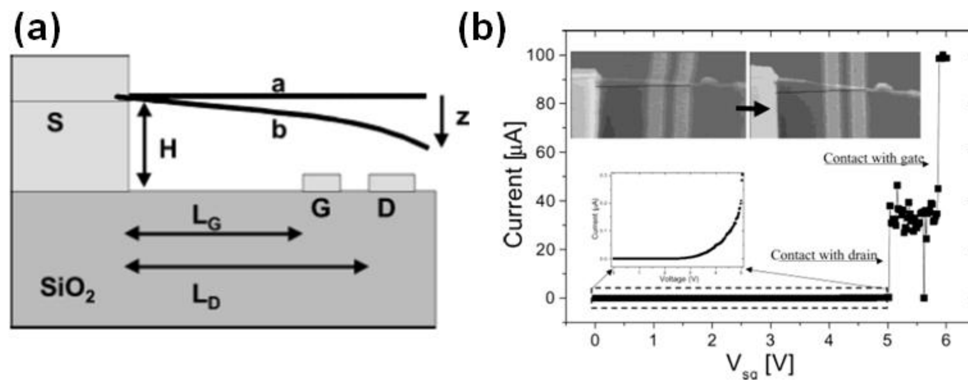

Fig 1.5: 3-terminal NEM relay using suspended CNT cantilever[16], (a) Basic structure, (b) Transfer curve of the fabricated device.

Fig 1.5 is 3-terminal CNT nano relay presented by S. Lee. et al[16]. The CNT channel is suspended(ground) over drain and gate electrode. Drain electrode is maintained to V_{dd}, and gate is swept to pull-in and pull-out the suspended cantilever channel. With the gate voltage, the cantilever can touch with drain electrode only, or make a contact with the gate, too. The V_{sg} vs. $I_s(=I_{ds}+I_{gs})$ graph(Fig 1.5(b)) shows this behavior clearly.

Fig 1.6 illustrates 3-terminal NEM-switch with suspended CNT channel[18]. The CNT channel supported by drain electrode in both end is suspended in the air, and two symmetrical side electrodes (source and gate) are self-aligned over the suspended CNT

channel. The CNT acts as a self-align mask during the source/gate electrode formation process. The drain set to 0.5V and source is grounded. In V_{gs}-I_{ds} characteristic(Fig 1.5 (b)), the abrupt switching arises at V_g=3.6V with I_{on}/I_{off}=10^4. This device can be used as 2-terminal NEM-switch, too.

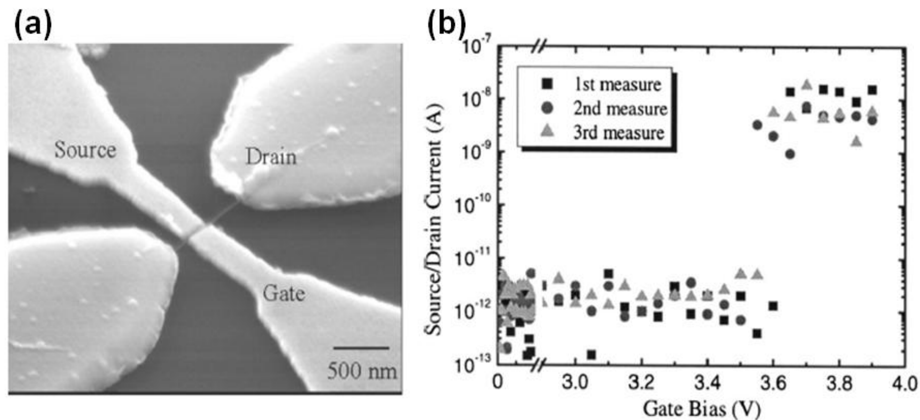

Fig 1.6: 3-terminal NEM switch using suspended CNT channel[18], (a) 45° tilted SEM image of fabricated NEM switch with triode structure, (b) Transfer curve of the fabricated device with V_d=0.5V.

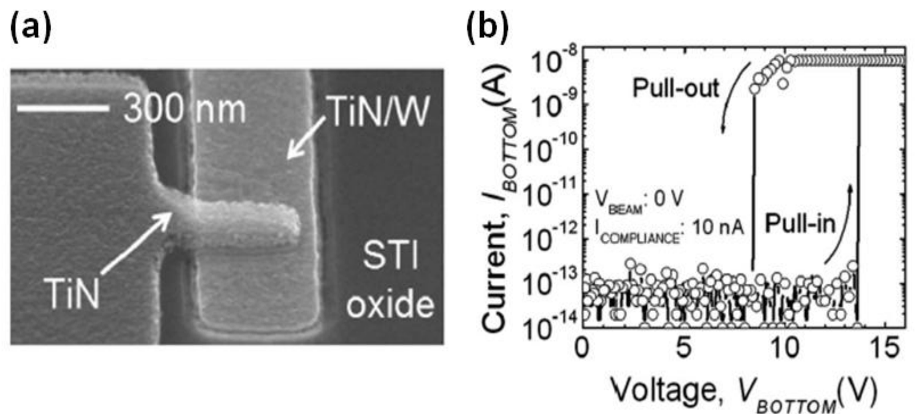

Fig 1.7: 2-terminal NEM switch using suspended TiN Cantilever[21], (a) 45° tilted SEM image of fabricated NEM switch, (b) Transfer hysteresis curve of the fabricated device with compliance of 10*n*A.

W. Jang. et al. presented 2-terminal NEM-switch with suspended TiN thin film

cantilever structure[21]. In Fig 1.7, the thin TiN cantilever is suspended over TiN bottom electrode with 15*nm* air gap. The switch shows ideal on/off characteristic with $I_{on}/I_{off}=10^5$. The switch demonstrates the multiple switching behavior over hundreds of ac and dc bias condition in air ambient. Another advantage of this device is that they use the CMOS process.

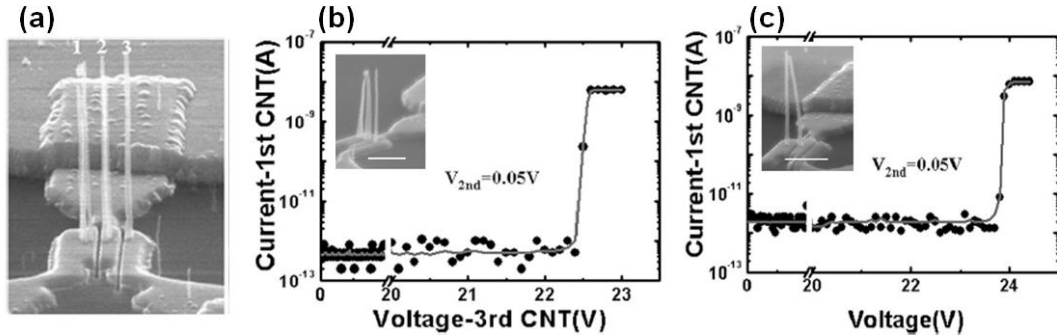

Fig 1.8: 2 or 3 terminal NEM switch using vertical CNT[22], (a) 45° tilted SEM image of fabricated NEM switch, (b) Transfer curve of the fabricated device with 3-termianal, (c) Transfer curve of 2-terminal, Inset of (b),(c) is the SEM image in ON state of each device.

Different from the planar structure NEM-switches, J. Jang. et al. suggested NEM-switch architecture with vertically aligned CNT[22]. Fig 1.8(a) is the schematic of the device. The device uses a pair(2-terminal) or 3(3-terminal) of vertically aligned CNT pillar as electrode. In case of 2-terminal, one is grounded(source), and other is biased(gate). With this condition, the top of two electrode comes to contact due to the electrostatic force. At 3 terminal device, the adjacent electrodes are biased as same polarity, and the rest electrode is grounded. Because of the repulsive force between two electrode biased same polarity, the electrode in the middle comes to contact to the grounded electrode. Fig 1.8(b) is the switching property of 2-terminal device, and Fig 1.8(c) is that of 3-terminal device. Both graph shows the abrupt switching property of

device clearly.

Fig 1.9(a) illustrates 4-terminal relay technology for complementary logic circuit

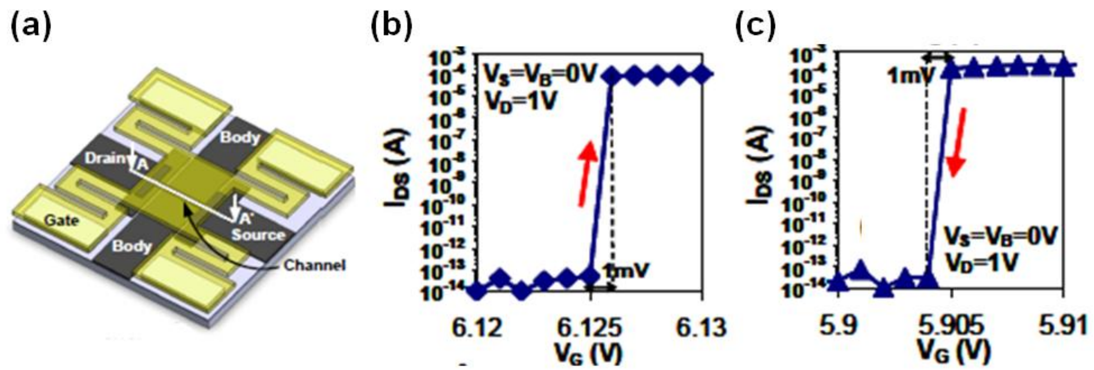

Fig 1.9: 4-terminal relay device with suspended metal gate[23], (a) Schematic of device, (b) Pull-in occurs at Vg=6.1V with SS=1mV, (c) Pull-out occurs at Vg=5.

presented by R. Nathanael. et al.[23]. NEMS relay technology has been proposed for ultra-low-power digital integrated circuit application. This is because the relay is an ideal switch with abrupt on/off switching and zero off current, so that the operating voltage can be zero in principle. However, there are two critical problems to solve for conventional 3-terminal NEMS relay: reliability problem comes from surface wear and stiction-induced failure and low switching voltage. They used a highly reliable mechanical contact technology employing tungsten electrodes with TiO_2 coating and 4-terminal design adopting body electrode.

Fig 1.10 shows 2-terminal switch using suspended SiC nanowire channel[24]. The suspended SiC nanowire and side gate is fabricated top-down process with E-beam lithography and etching process. The nano-beam size is controlled to 55*nm* width, 50*nm* height, 20*um* length including 30*nm* Al top metallization layer to gain high I_{on} current. The final gap was 30*nm* with various side-gate width like tip(tens of *nm*) and planar(8*um*,

15*um*). They demonstrate the sharp pull-in behavior with high I_{on}/I_{off} rate successfully. Furthermore, they showed the possibility of multiple pull-in stage with the various width of side gate in single device.

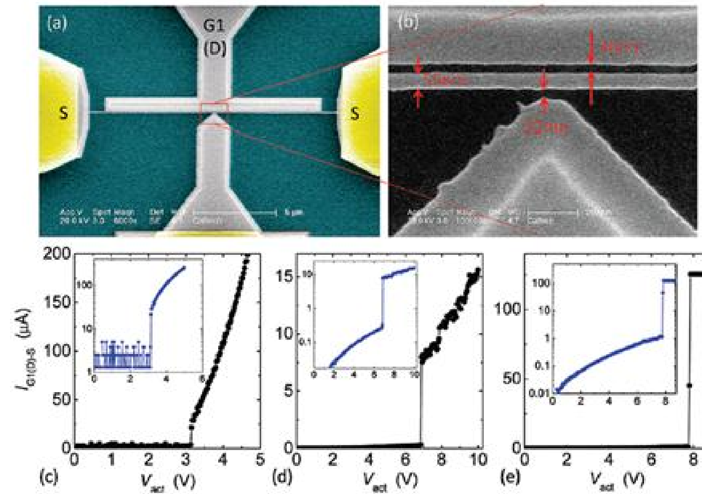

Fig 1.10: Low voltage 2-terminal NEM switch suspended metalized SiC nanowire[24], (a)Low magnification SEM image of device, (b) High magnification SEM image of device, (c), (d), NEMS switching events from two 20μm long devices, with $V_{on} \approx 3.1$V and 7.0 V, respectively. (e) Measured switching event from a 15 μm long device, with $V_{on} \approx 7.8$ V.

1.3.2 Scaling Challenges

In many types of NEM switches reviewed previous, NEM switch has a limitation in large-scale production due to its bottom-up process scheme or use of special process like manipulator to place nano-structures in proper position. And the use of E-beam lithography technique which is used to form contacts to randomly distributed nanostructures prohibits the NEM switch device from wafer-scale fabrication process. To enhance NEM switch's application, we need special technique to overcome this issues.

The simplest way is to make large-scale array of NEM switch using top-down process which consist of “deposition-patterning-etch” steps. At first, making the pattern of moving part over the fixed bias part covered with sacrificial layer with photolithography and dry etch process. After finishing the top layer, vapor Hf etching process can be used to release the moving part of NEM switch. The conventional deposition, photo lithography, and dry etching process are needed. Fig 1.11 is the pipe-clip shape sub-1V NEM switch using top-down process by J.O.Lee, et al[25].

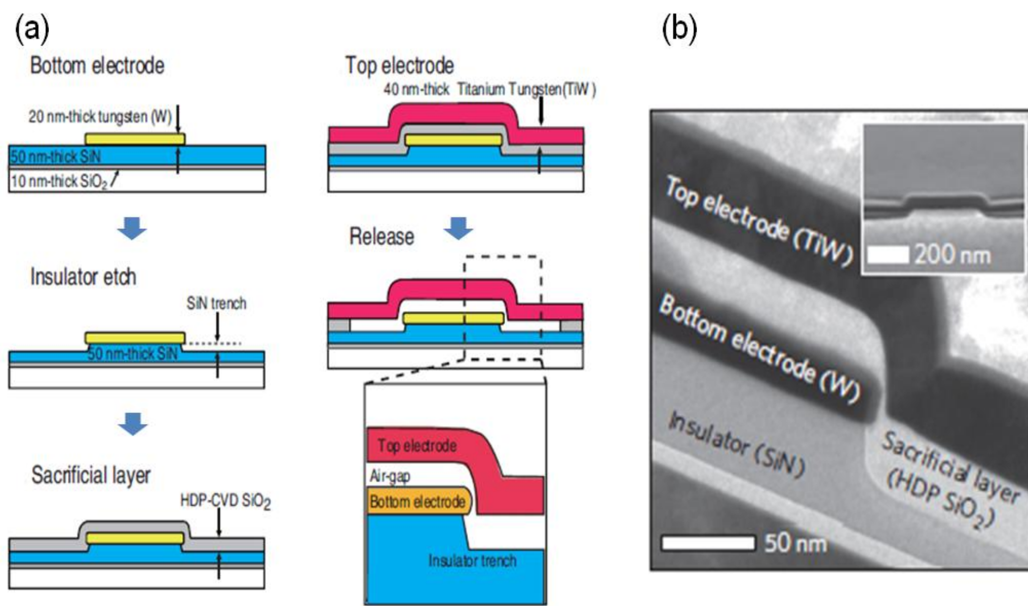

Fig 1.11: Pipe-clip shape NEM switch using top-down process. (a) Schematic process flow, (b) Cross section TEM image of the device[25].

In case of Si or metal layer as moving part, the top-down process can be used for NEM switch fabrication, but other nanostructures like carbon nanotube, graphene, or nanowire with various materials are hard to be used with top-down process. The other process like pattern-and-transfer, direct self assemble, or nanostructure ensemble can be a alternative solution for the large-scale array fabrication of NEM switch.

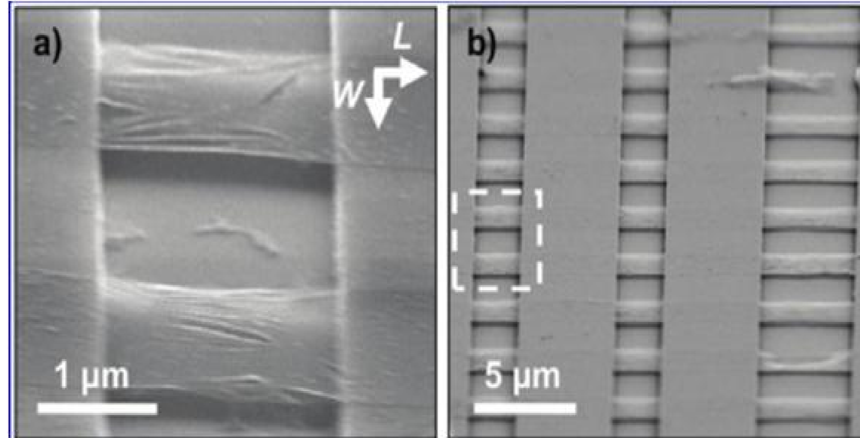

Fig 1.12: Large-scale graphene sheet resonator. (a) Angled scanning electron microscopy (SEM) image of Type A suspended graphene membranes over trenches in silicon oxide. (b) Angled SEM of an array of graphene membranes[26].

A. M. Zande, et al reported large-scale arrays of graphene resonator in 2010[26]. They realized fabrication of wafer-scale NEMS arrays using array growth and transfer process[27]. Fig 1.11 shows the SEM images of large-scale graphene sheet resonators. The graphene sheet was deposited on Cu foil using CVD method. Then graphene sheet was transferred to PMMA layer and released on the patterned silicon oxide wafer with appropriate alignment.

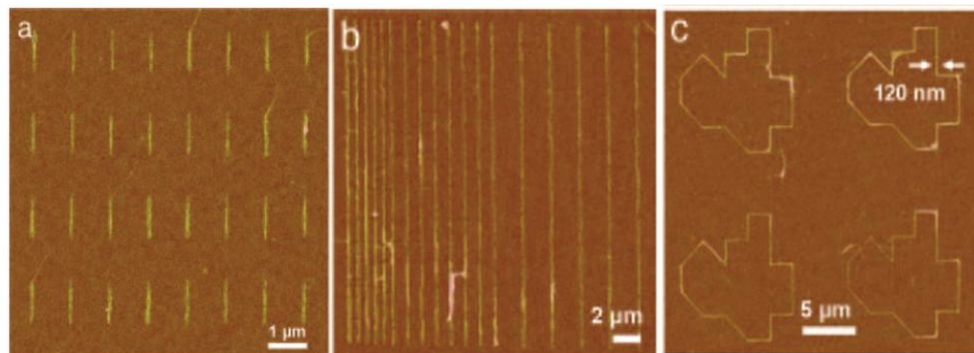

Fig 1.13: Direct assembly pattern of SWNT with AFM (a),(b) parallel pattern, (c)Random line structure[28].

Direct assembly of nanostructure can be another candidate for the large-scale array fabrication. Y. Wang, et. al. shows the patterned single wall nanotube array using direct assembly[28]. Direct assembly use the attraction force between the nanostructure and specially terminated substrate surface. They used nanopatterned affinity templates, in this case COOH-terminated self-assembly monolayer(COOH-SAM) and CH_3-terminated self-assembly monolayer(CH_2-SAM). The SWNT have attraction to COOH-SAM only, and this property make it possible to place SWNTS in accurate pre-patterned position.

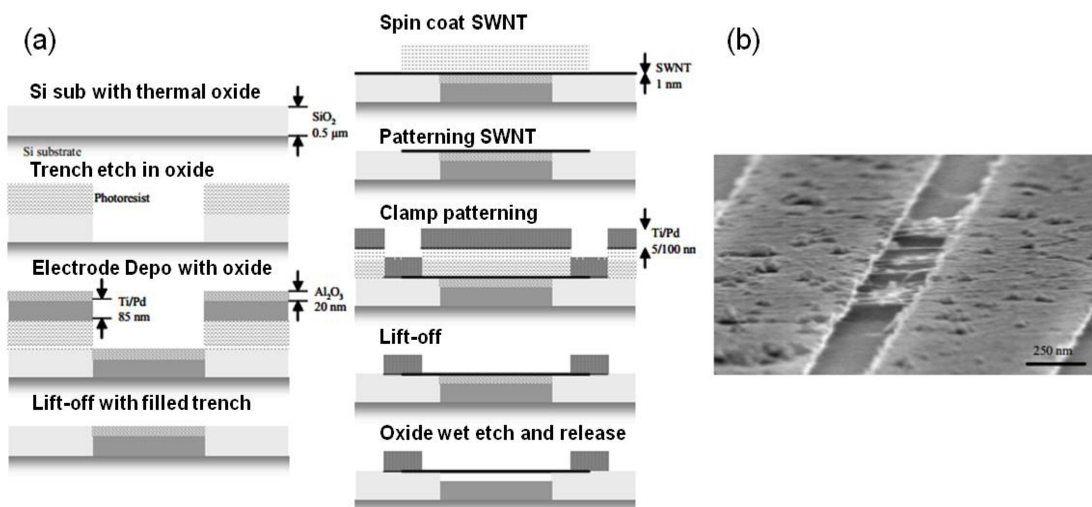

Fig 1.14: Nanostructure ensemble using a fabric of SWNT, (a)Schematic of process flow, (b)SEM image of fabricated device[29].

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J. W. Ward, et. al. demonstrated NEM switch using nanostructure ensemble. The monolayer of SWNT was spin coated over the pre-patterned electrode layer with sacrificial lay. With the photolithography and lift-off process was used to pattern and form a clamping electrode with alignment process. Fig 1.14 is the schematic of process flown and SEM image of fabricated device.

Many possible ways are being developed for the large-scale fabrication of NEM switch including traditional top-down process, the encapsulation can be the serious obstacle in NEM switch technology. Many of results of NEM switch so far were operated in vacuum[20]. When one considers sticking, oxidation, capillary force from the humidity of air, particles, or contamination, NEM switch in the air is still a big challenge. The encapsulation increases the device size and the complexity of the process at the same time.

1.3.3 Reliability Issue

Reliability is the one of the most critical issue of NEM switch as we must consider the mechanical and electrical reliability at the same time. Furthermore, the mechanical motion of moving elements and the repeated contact-detach motion at the same contact position can make various failure mode: stiction, burn-out from electrical discharge, wear(exacerbated easily with electrical discharge), fatigue, fracture, or all together.

Among them, stiction and burn-out are the most common fail mechanism in NEM switch. Stiction is the moving channel which comes to attach to the bias electrode, and doesn’t be detached after removal of bias. In nano-scale device, the relative magnitudes of van der waals and elastic forces, and in significance of surface roughness relative to the dimensions of the active elements are should be considered more seriously[20]. Coating the surface of electrode with thin films which can reduce adhesion[30], or changing of electrode material having less affinity with suspended channel can improve

the resistance against stiction problem[31].

Burn-out is the localized melting of contact point in NEM switch. The charges stored during the off state come to flow through the electrode in “pull-in” moment with higher magnitude in orders compare to steady-state on current. This huge current in short time can be enough to melt the contact point locally. The best way to prevent burn-out is to decrease the pull-in voltage. The decrease of t_{gap} or increase of stiffness of moving elements is the easiest way to accomplish it, but these solutions can make “stiction” problem worse. The other solution is to increase contact resistance with thin oxide coating[32]. But, this method has drawbacks of increasing power dissipation, delay, and decreasing noise margin of device.

1.4 Summary

Within these previous researches review, *NEM* switches suffer from the fundamental design limitation that when turned on, the current relies solely on the contact resistance between the two contact surface and the typically large threshold voltage used to pull in the device. Therefore two terminal switches have no control over it’s on or off current and their performances depend heavily on the nature of the mechanical contacts which is still not well understood[33]. On the other hand, three terminal suspended gate NEMS field effect transistors are configured as a traditional transistor with the gate voltage used to independently tune the current from source to drain. However the large micrometer sized metal suspended gate electrode in previously reported devices[17, 34] have limited operational speed in several MHz due to their heavy moving mass. Our

concept, in contrast, is based on the ultra-small mass and volume of a suspended semiconductor nanowires which has shown to be able to scale to ultra-high-frequency (UHF) and beyond in mechanical resonance[35]. Nanowires have also previously demonstrated extreme high performance as field effect transistors with near-ballistic transport[36]. Therefore, by employing the thin nanowire as the nano-electro-mechanically suspended channel, we will demonstrate near zero SS and high operational speed with combination of mechanical motion and electrical property of core/shell nanowires.

Chapter 2

Device Fundamentals and Simulation

In chapter 1, I reviewed the importance of the sub-threshold swing in terms of I_{off}, which vary the static power consumption exponentially. I mentioned a few solutions to overcome kT/q limitation like tunnel FET, impact ionization MOS, and NEMS. In this chapter, I'll explain the principle of NEMFET device and show the simulation results of NEMFET with suspended nanowire channel.

2.1 Device Principle of NEMFET

NEMFET is the device which has steep sub-threshold swing less than 60mV/dec in room temperature using mechanical movement of device elements like gate or channel. As the basic principle is exactly same both suspended gate and suspended channel, I'll explain the device basic with suspended gate case[37].

Fig 2.1(a) shows the schematic of suspended gate NEMFET. The device has same structure with conventional MOSFET except that the gate is suspended over gate oxide with certain initial air gap thickness, x_o. Compared to previous NEMS-switch, the NEMFET remains a three-terminal device with the current via the source to the drain electrodes being modulated by a gate electrode. It draws no current from the gate and requires no electrical contact between the gate and channel. With the increase of V_g, the suspended gate come to get two kind of force, the downward electrostatic force from V_g, and the upward elastic restoring force from mechanical property of suspended gate. In certain value of V_g, so-call "*pull-in*" voltage(V_{pi}), the elastic force overcome the restoring

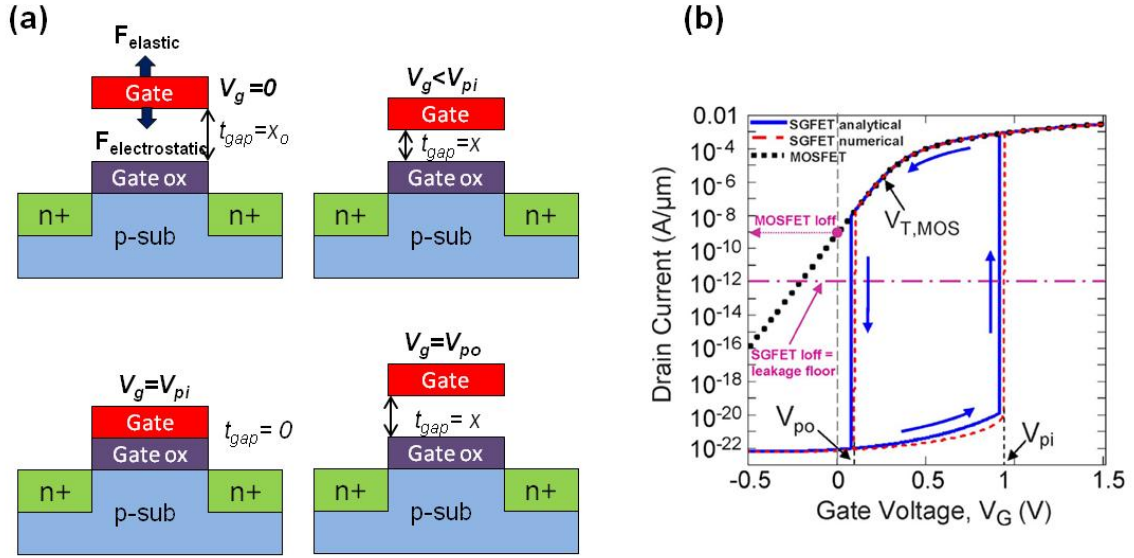

Fig 2.1: Suspended gate FET[37], (a) Schematic structure of SGFET and the gate position change with applied gate voltage(V_g), (b)Analytically and numerically calculated SGFET transfer characteristics(MOSFET characteristic is shown for comparison).

force, then the suspended gate get stuck to gate oxide. On the contrary, with the decrease of V_g, the gate come to be detached from gate oxide surface as the upward restoring force becomes greater than the downward electrostatic force. This motion is called "*pull-out*", and the voltage is V_{po}. This abrupt mechanical motion of suspended gate with given V_g can be converted to V_g- I_g curve with abrupt on/off behavior at V_{pi} and V_{po} like Fig 2.1(b).

The force-balance equation related to the suspended gate without external force is[15]

$$\frac{WL\varepsilon_{gap}V_{gap}^2}{2x^2} = k(x_o - x). \quad (2.1)$$

The left-hand side designates the electrostatic attraction force applied to the suspended gate, whereas the right-hand side designates the counteracting elastic restoring force(W=suspended gate width, L= suspended gate length, ε_{gap}= gap permittivity, V_{gap} =

the voltage drop across the gap, k = spring constant of suspended gate, x_o=initial air gap thickness, and x =varying air gap thickness).

For a uniformly distributed electrostatic force along the beam and neglecting the residual stress, the spring constant k is given in terms of the structural parameters by[38]

$$k = \frac{32ELh^3}{W^3}, \tag{2.2}$$

where E=Young's modulus, and h=thickness of suspended gate.

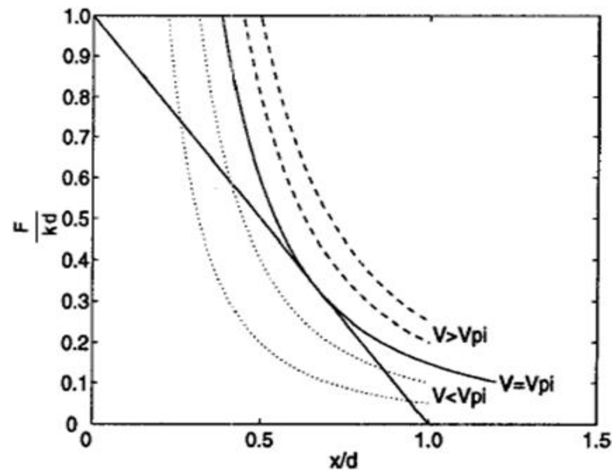

Fig 2.2: Normalized restoring and electrostatic forces vs. normalized electrode separation[39].

Fig 2.2 is the dimensionless plot a linear restoring force(solid line), and electrostatic force(dash line) due to V_g[39]. Intersection of the restoring and electrostatic forces indicate equilibrium positions, assuming zero external force. On the electrostatic force curve corresponding to the critical "pull-in" voltage, V_{pi}, there is exactly one equilibrium point. Below this voltage, the device has two equilibria; above this voltage, the electrostatic force dominates the restoring force, and hence, there are no equilibria.

This holds true for nonlinear restoring forces provided that they remain finite at x=0.

In a simple MEMS switch, consisting of two parallel metallic plates separated by an air gap, the stability analysis yields $x_{pi}=2x_o/3$, and V_{pi} can be expressed

$$V_{pi} = \sqrt{\frac{8kx_o^3}{27\varepsilon_{gap}WL}} \ . \tag{2.3}$$

2.2 Device Simulation

As reviewed above, NMFET structure has a strong point as three terminal device compare to NEMS switch. The suspended gate NEMFET demonstrate the abrupt on/off switching with near zero sub-threshold swing, but has the limitation in operational speed due to large mass and size penalty of the moving gate element. In this chapter, I will show the strong point of suspended nanowire channel due to the excellent electrical and mechanical property with numerical simulation.

Device simulation was performed by 3D modeling of suspended p-doped silicon nanowire NEMFET in Sentaurus device simulator combining with COMSOL multiphysics simulation software. The nanowire channel is suspended over the gate electrode with certain initial air gap thickness x_o, and connected to source/drain electrode mechanically and electrically. Due to the hole gas accumulation in Ge-core/Si-shell interface[40], the channel is normally on. With the increasing gate voltage, the NW is pulled down by the electrostatic force from the gate. At the point which the electrostatic force overcomes the upward mechanical force of NW channel, the NW channel comes to be stuck to gate electrode with abrupt mechanical motion. This motion is the ‘pull-in’,

and the voltage of gate at this point is pull-in voltage (V_{pi}). And opposite, in case of decrease the gate voltage, the restoring mechanical force will be bigger than the electrostatic force from the gate. Then, the stuck channel will be detached from the gate surface, and go back to its original position. This motion is the 'pull-out', and the gate voltage at this moment is pull-out voltage (V_{po}).

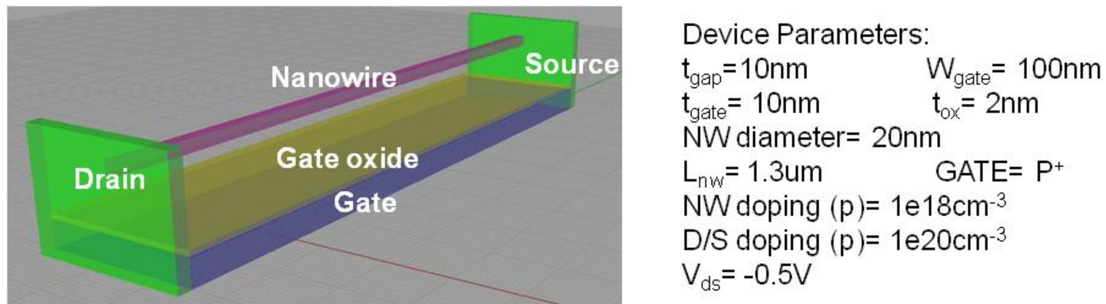

Fig 2.3: NEMFET structure for the device simulation. The important parameters are summarized in the right side.

Fig 2.3 shows the structure and the important parameters of the device. Static pull-down displacement x vs. V_g was solved self-consistently using a moving mesh condition solving the Arbitrary Lagrangian Eulerian (ALE) where the boundaries to the NW beam are constantly iterated. The x vs. V_g data was then imported into Sentaurus for the device's I_d-V_g transfer characteristics. A key feature of the NW-NEMFET is the abrupt pull-in or snap-in of the NW towards the bottom gate stack at V_{pi} due to imbalance of the mechanical restoring force and the electrostatic attraction force across the air gap, which functions as an infinitely high gain mechanical amplification of the V_g-surface potential control. In particular, as the diameter of the NW is on the same order of the air gap x_0, electric field lines terminating on the sides of the NW contributed to an enhanced 3D

electrostatic coupling and up to 20% reduction in V_{pi} compared to capacitive couplings in 2D interactions of previous MOS-NEMFETs.

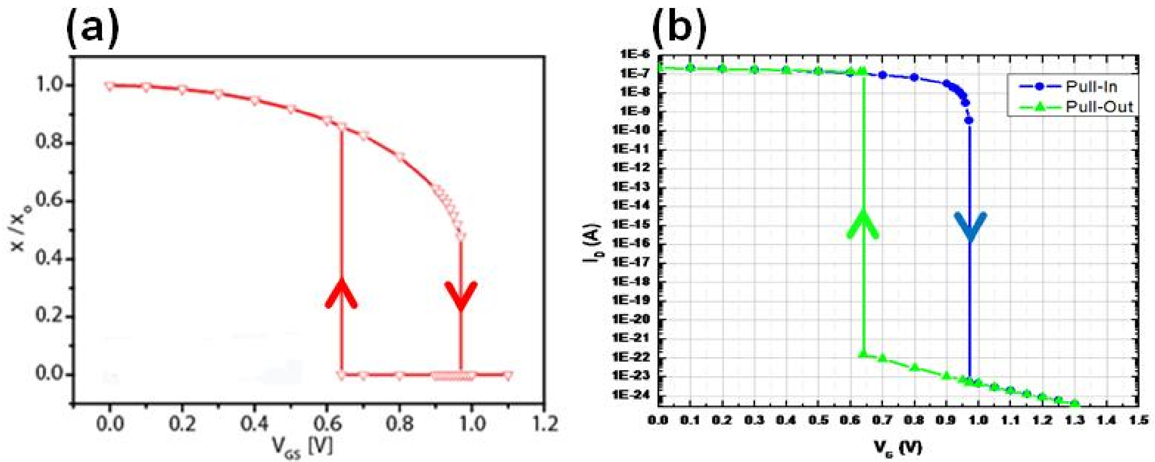

Fig 2.4: Simulation results of NEMFET, (a)normalized gap thickness vs. Vg, (b)Vg-Id characteristic of NEMFET.

Fig 2.4(a) is the simulation results of V_g vs. normalized air gap thickness(x/x_o). The abrupt "pull-in" occurs at V_{pi}=0.97V, and "pull-out" takes place at V_{po}=0.63V. This mechanical movement of suspended channel can be converted to V_g-I_g curve like Fig 2.4(b). The I_{on}/I_{off} ratio can be as great as 10^{15} with almost zero subthreshold swing. Moreover, the operational voltage window(V_{pi}-V_{po}) is less than 0.5V, which is very important parameter for the NEMFET device. To clarify the importance of the sub-threshold swing value of NEMFET, we compare the V_g-I_g curve between NEMFET and planar PMOS with same dimension.

In Fig 2.5, the line with open circle is for planar FET, and the line with open triangle is for NEMFET. To get same I_{on}/I_{off} ratio, planar FET need 4-time-bigger operational voltage window even with 60*m*V/*dec SS* value. As expected in motivation

part, the abrupt mechanical motion of NEMFET channel can realize "near-zero" sub-threshold swing value, and it results in very high I_{on}/I_{off} ratio with very small operational

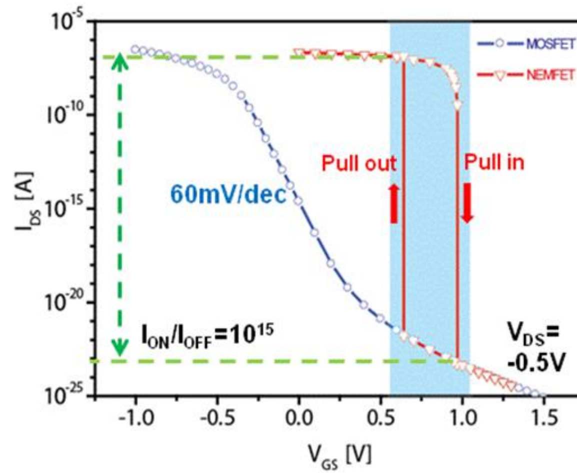

Fig 2.5: Comparison of simulated V_g-I_d curve between NEMFET and MOSFET having same dimension for the same I_{on}/I_{off} ratio.

voltage window compare to planar COMS with V_{dd}=0.5V.

To check the effect of doping in suspended channel, we did device simulation with different doping condition. Fig 2.6 is V_g–I_d curve with $1x10^{18}/cm^3$(red line) and $3x10^{18}/cm^3$(blue line). Other important parameters were same. With increasing doping

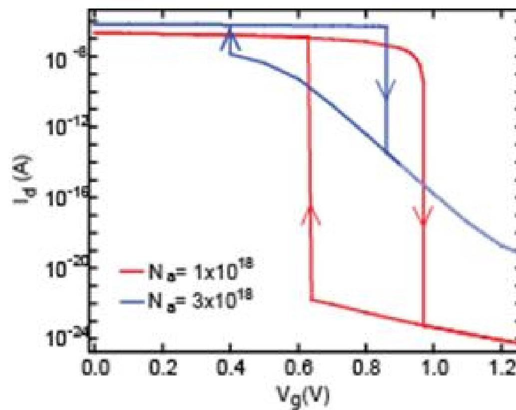

Fig 2.6: Comparison of simulated V_g-I_d curve of NEMFET with different doping.

density, the SS was increased, too, and the on-off ratio was degraded about a half. The decrease of V_{pi} and V_{po} can be explained with the increase of electrostatic coupling with the increase of doping.

One of the important parameter of FET is the operational speed of the device. The speed at which NEMFET can operate is essentially limited by the suspended beam's mechanical resonant frequency. For the fundamental flexural mode of a suspended beam, the resonant frequency f_o can be estimated as[41],

$$f_o = 1.03\frac{W}{L^2}\sqrt{\frac{E}{\rho}} \propto \left(\frac{W}{L}\right)\left(\frac{1}{L}\right)$$

where W=width of beam, L=length of beam, E=Young's modulus, and ρ=mass density. As shown in equation, the short channel length is needed to achieve high resonant frequency with constant aspect ratio.

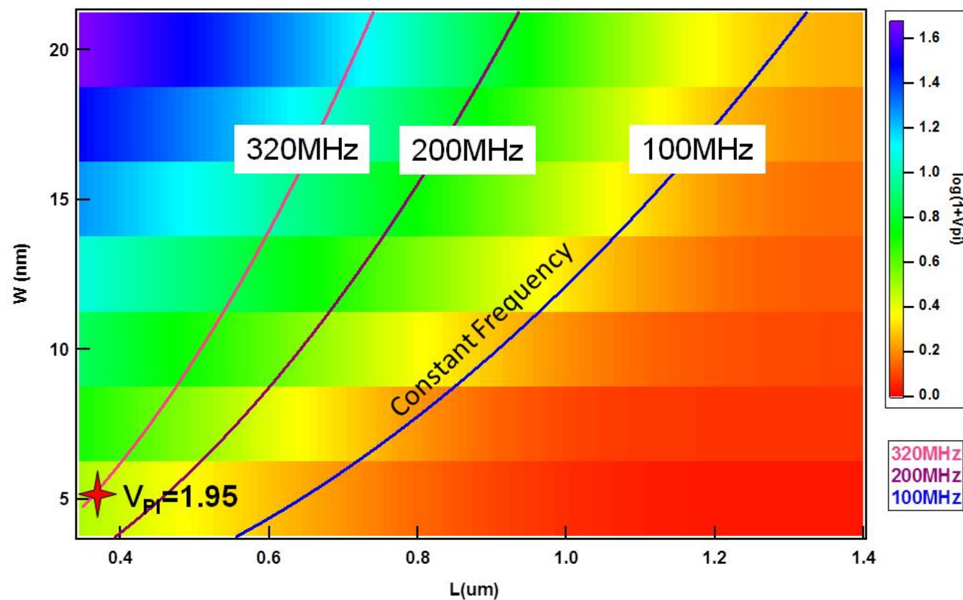

Fig 2.7: NEMFET scaling map in various diameter and length of suspended nanowire channel.

A common dilemma in NEMS switches is higher frequency and more rigid structures usually require much increased pull-in voltage. To explore the design space of NW-NEMFET, we plot the constant V_{pi} map for a range of different diameter/length NWs simulated given the same x_0 and t_{ox}. In Fig 2.7, The dotted and solid lines represent constant V_{pi} and constant frequency scaling for the device dimensions and it is clear from the interceptions that >300 MHz device with V_{pi}<5 V can be achieved using SiNWs with 11.7 *nm* diameter or Ge/Si CSNW with 12 *nm*. Furthermore, the scaling map suggests sub 1 V operation will demand nanowires with diameter smaller than 5 *nm*.

2.3 Conclusion

In this chapter, I reviewed the basic principles of NEMFET and showed the simulation results of NEMFET with suspended nanowire channel. With simulation, NW channel can achieve UHF operation speed with V_{pi}<5V, and NW channel is the only possible way to accomplish the results of that level. From the chapter 2, I'll demonstrate how I make a real NEMFET device step by step.

2.4 Acknowledgement

Chapter 2 is in part a reprint of "Steep Subthreshold Slope Nano-electro-mechanical Field Effect Transistors with Nanowire Channel and Back Gate Geometry", to appear in *Device Research Conference,* (2013) and "Three-Terminal Nano-electro-mechanical Field Effect Transistor with Abrupt Subthreshold Slope", Submitted, *Nature*, 2013.

Chapter 3

NEM Switch with Suspended Nanowire Channel

3.1 Introduction

In this chapter, I will demonstrate the feasibility of NEM switch with suspended nanowire channel. The scheme of device is same to NEMFET except the channel is suspended over the gate without gate oxide. So, the current flow is from the gate to source/drain which are all grounded when the channel is pull-in stage. With this simple switching device, we can confirm the feasibility and the abrupt mechanical motion of suspended channel with applied gate bias, which is essential mechanism of NEMFET.

3.2 Device Fabrication

To realize the NEMS switch with suspended nanowire channel, we used the n+ Si nanowire as suspended channel, and fabricate metal electrode array as gate and source/drain electrode to support the suspension of nanowire channel. Fig 2.x shows the schematic structure of NEMS switch. The *n+* Si nanowire were grown on Si(100) substrate using silane(SiH4, 2%) diluted in hydrogen as precursor gas sources in an LPCVD system(ET2000, Firstnano). Gold colloids(Ted Pella) with diameters ranging from 15~30*nm* were dispersed on the Si substrate as catalyst seeds. The Si nanowire was grown at 460°C for 39*min* with total pressure of 300*Torr*, and 20sccm of PH_3 was injected as n-type dopant.

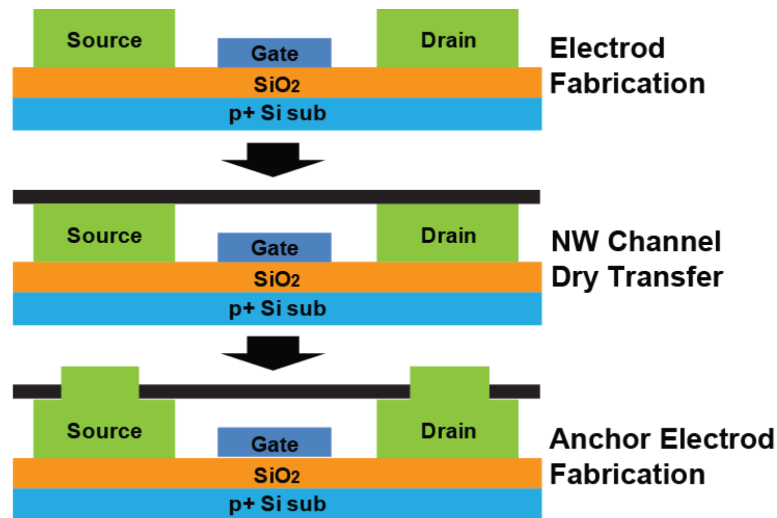

Fig 3.1: Schematic cartoon of process procedure for NEM switch with suspended nanowire channel.

Fig 3.1 is the process flow of the NEM switch. The p^+ Si substrate covered by 300 nm thermal SiO_2 is cut and cleaned in appropriate sizes. I designed the straight and parallel electrode arrays and used E-beam lithography process (JEOL6400 SEM combined with NPGS software) with MMA EL9 and 950 PMMA C2 double layer photo resist as pattern mask. The pattern-written substrate was developed with 1:3 MIBK:IPA solution for 1*min*, and cleaned with IPA for 1*min* again. At first, the gate electrode was patterned and Cr 5*nm* + Au 35*nm* metal film was deposited with E-beam evaporator with in-situ thickness monitor sensor and lift-off the photo resist mask within Acetone for overnight in room temperature. The Cr layer was used as an adhesion layer as the adhesion between SiO_2 and Au film is very poor. As 2nd step, the source/drain electrode as supporting suspended nanowire channel was patterned with E-beam lithography process aligned to gate electrode, and Cr 5*nm* + Au film was deposited and lift-off in same way. The thickness of Au film was important as the air gap thickness, t_{gap}, was

simply set by the difference of Au deposition thickness in gate and source/drain process. The space between source and drain set the channel length, L_{ch}, of the device, we chose the numbers carefully. After finishing the bottom electrode array fabrication, the nanowire channel is transferred perpendicularly on the electrode array with dry transfer method. As the suspension rate of nanowire channels was varied with nanowire channel diameter, source/drain channel length, and air gap thickness, we did Scanning Electron Microscope(SEM) observation with plan-view and tilt-view both to find the best suspended nanowire channel.

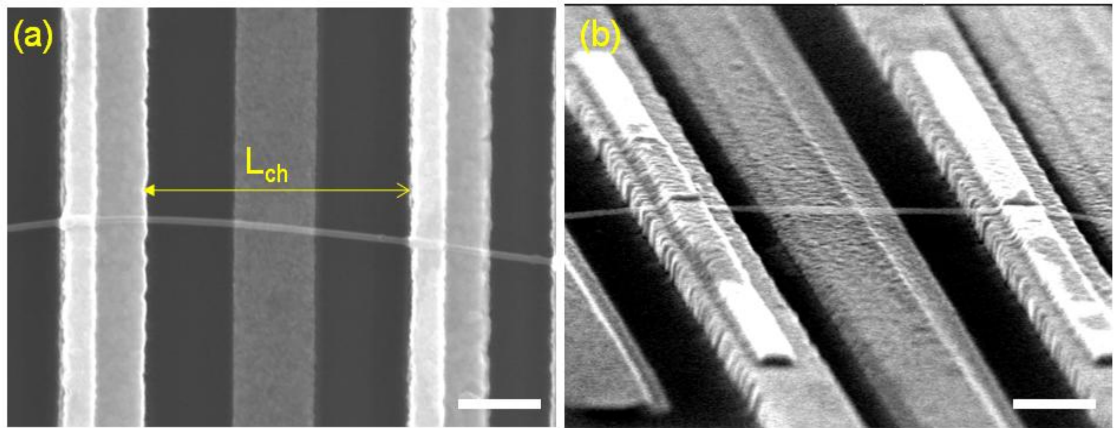

Fig 3.2: SEM image of NEM switch with suspended nanowire channel, (a) plan view, (b) tilt view.

After transfer the nanowire channel, anchor electrode process was followed. The anchor electrode connects the nanowire channel to supporting source/drain electrode electrically and mechanically. The anchor electrode was patterned in the form of small rectangle with hundreds nanometer width and a few micrometer length over the contact point of selected suspended nanowire channel with SEM observation, and local wiring which connects the selected source/drain electrode to probing pad outside at the same

time. The MMA and PMMA double layer photo resist was spin-coated over whole substrate range, and the nanowire position didn't change during the photo resist coating process. Ti 10*nm* + Au 50*nm* are deposited as anchor electrode and local wiring. Different from the previous metal layers(Cr+Au), Ti used as adhesion layer and electrical ohmic contact layer for the Si nanowire. After lift-off process acetone, we used the Critical Point Dryer(CPD) process to maximize the channel suspension rate during the drying process. At the end of process, the devices was inspected once again with plan-view and titl-view SEM to confirm the suspension of nanowire channel and alignment of anchor electrode. Fig 3.2 shows the SEM image of NEMS switch after whole process. The electrodes aligned well with E-beam litho process, and the air gap thickness controlled successfully with different thickness control of gate and source/drain. We can notice that the channel suspension can be monitored with tilt-SEM image successfully.

3.3 Electrical Property

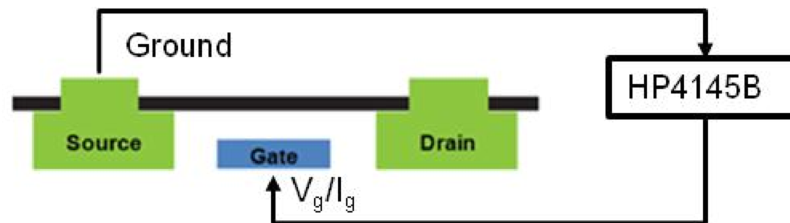

Fig 3.3: V_g-I_g measurement scheme of NEM switch with suspended NW channel.

To confirm the switch behavior of NEMS device, simple V_g-I_g DC measurement was flowed for selected devices. Fig 3.3 shows the schematic of measurement. At this time, we didn't have the measurement equipment for hysteresis, only sweep-up direction

measurement was done with HP4145B semiconductor parameter analyzer. The important parameters of NEMS switch are summarized in table 3.1.

Table 3.1: Important parameters of NEM switch with suspended NW channel.

S/D height	90*nm*(Cr+Au)	Anchor Electrode	60*nm*(Ti+Au)
Gate height	50*nm*(Cr+Au)	NW channel	*n*+
t_{gap}	40*nm*	NW diameter	40*nm*
L_{ch}	1.37*um*		

The V_g bias was applied to gate electrode from 0V to certain voltage, and source or drain electrode was grounded. We recorded the I_g current which flow through the gate electrode, which will change abruptly if the suspended channel was pulled in to gate electrode.

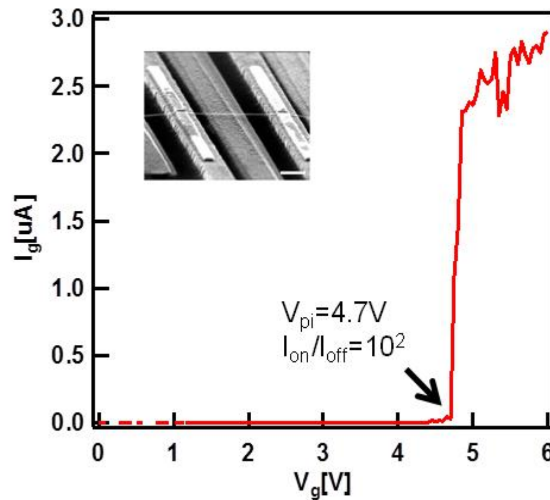

Fig 3.4: Measured V_g-I_g curve of NEM switch with suspended NW channel. Inset is the SEM image before measurement(scale bar=500*nm*).

Fig 3.4 is the V_g-I_g plot of NEMS switch device with the SEM image before

measurement as inset. The abrupt increase of I_g occurred at V_g=4.7V(V_{pi}) with $I_{on}/I_{off}=10^2$. The only possible current path from gate to source/drain is the pull-in of suspended channel. Even we failed to get a multiple switching behavior of NEMS switch, we can confirm the feasibility of NEMFET with suspended nanowire channel with simple NEMS switch structure. Fig 3.5 is the comparison of V_{pi} between analytical solution of NEMS switch and experiment data. The analytical V_{pi} was calculated with the Equation 2.3, and as shown in the graph, the measurement results fits very well with analytical calculation value.

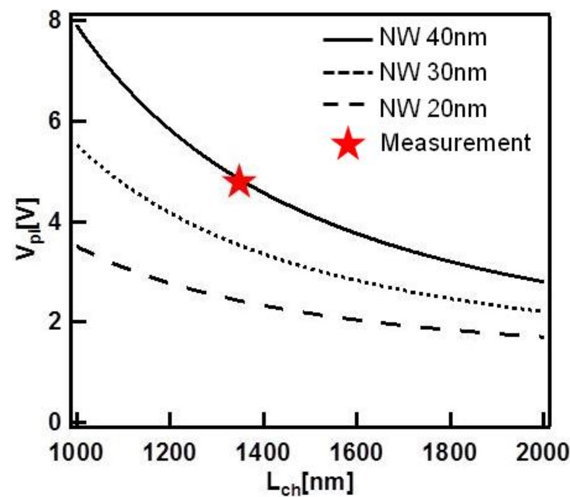

Fig 3.5: Analytically calculated V_{pi} vs. L_{ch} plot in t_{gap}=40*nm* with various NW diameter(20/30/40*nm*).

3.4 Gate Width Effect

Even we succeeded to fabricate NEMS switch, we continue the scaling down the device dimension to the check the low limit of channel suspension. I fabricated NEMS switch with L_{ch} 600*nm*, nanowire diameter 25*nm*, and t_{gap} 30*nm*. The expected V_{pi} was ~7V, but we couldn't get any abrupt pull-in behavior with this device. The problem was

the width of gate electrode. Due to the narrow channel length and alignment margin during the E-beam lithography, the width of gate electrode was limited to 250nm in this device. Fig 3.7 shows the simulation results of V_{pi} vs. gate width in NEMFET simulation. The V_{pi} is maintained same level, but skyrocketed from gate width coverage ~55%. The device in Fig 3.6 has the 40% of gate width coverage. With this results, we design and fabricate the gate width coverage more than 50% with special care of alignment step in E-beam litho process

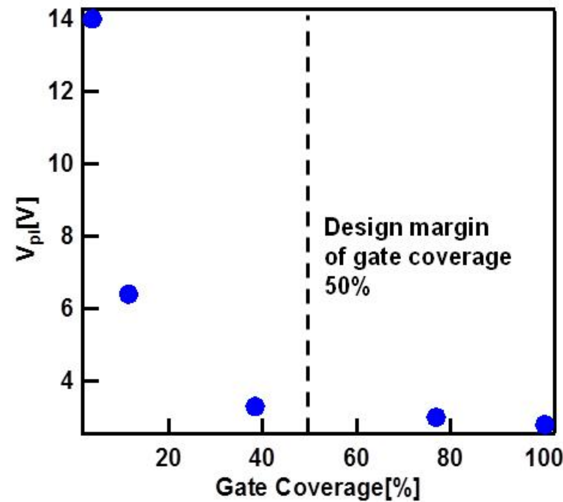

Fig 3.6: Analytically calculated V_{pi} vs. Gate coverage of NEM switch with L_{ch}=1300*nm*, NW dia.=20*nm*, and t_{gap}=40*nm.*

3.5 Conclusion

In this chapter, to confirm the feasibility of NEMFET with suspended nanowire channel, we designed and fabricated NEMS switch as proto-type of NEMFET. The switch shows abrupt increase of Ig at V_{pi}=4.7V, which fits very well with analytically calculated value. We've made it certain that suspended channel scheme works, and the measurement results fits well with calculation data. Even we didn't get the multiple

switching of device, we can verify the process scheme and the controllability of important parameters of NEMFET device.

Chapter 4

Back Gate NEMFET with Suspended Nanowire Channel

4.1 Introduction

We confirmed the feasibility and abrupt pull-in and pull-out behavior of suspended nanowire channel with applied gate voltage with NEMS switch. And, we can set the start point of various important parameters like nanowire diameter, air gap thickness, channel length, electrode array dimension, and drying process, etc. In this chapter, we will demonstrate real NEMFET with suspended Ge/Si nanowire channel in back gate scheme. We chose the back gate scheme as it has much more simple process scheme compare to local metal gate. Furthermore, thin gate oxide deposition on metal surface is much more complex and harder process than on Si surface.

4.2 Device design and fabrication

4.2.1 Back Gate NEMFET Scheme

Fig 4.1 is the schematic comparison between back gate NEMFET and local metal gate NEMFET, and Table 4.1 summarize the differences of the back gate NEMFET process comparing to local metal gate one. First, the critical gate oxide deposition process over suspended nanowire channel or metal gate is not needed. Instead of it, we can use

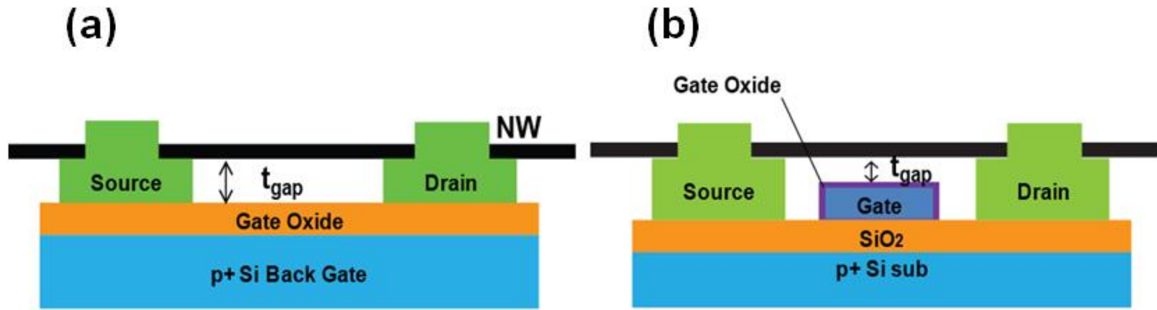

Fig 4.1: Schematic structure of the device, (a)the back gate NEMFET, (b)the local metal gate NEMFET.

Table 4.1: Comparison of the characteristics between the back gate NEMFET and the local metal gate NEMFET.

Gate structure	Back gate	Local gate
Gate metarial	*p*+ Si	Metal(Au)
Gate signal	Golbal	Individual
E-beam litho step/ Metal deposition step	2/2	3/3
Gate oxide	On Si	On metal or on NW
Gate leakage path	Large probing pad and wiring	NW contact area with gate

the highly doped silicon substrate covered with gate oxide. The thermal silicon oxide or high-k oxide on planar silicon substrate with atomic layer deposition process is well defined, so don't need to worry about the quality of the gate oxide. Second, we can skip the one step of E-beam lithography, metal deposition, and lift-off process, so the process step is much more simple then local metal gate process. Third, the gate is global back gate, the source/drain electrode don't be needed to align to gate electrode. As mentioned in chapter 2.5, the gate width should be 50% at least. It means the misalignment margin

of the source/drain electrode process aligned over gate electrode should be less than 200nm. Furthermore, if considering the electrode width variation comes from E-beam lithography and lift-off process(±10%) for both the gate and the source/drain electrode, the mis-alignment margin should be less than 150nm. As the maximum magnification of lithography process is x750, 150nm mis-alignment is not that enough number in terms of process stability. At last, the gate leakage can be minimized between the gate and the source/drain with nanowire channel which is place in unwanted position, as the NW is always isolated with global gate oxide in any position.

The back gate NEMFET process has the advantages, but some critical disadvantages can be pointed out. First, as it is the global gate scheme, it can’t control the each device individually. Even though, the isolation process such as isolation trench oxide or ion implantation process can be combined with the back gate scheme to insulating electrically each NEMFET device, but the process complexity will be increased a lot, too. So the back gate NEMFET can be used for the confirmation of NEMFET device scheme only. Second, in practical, the area of the probing pad for the source/drain electrode is extremely larger(60um x 60um) compare to the contact area between suspended nanowire channel and bottom gate(a few nm x a few nm). It means, there is a risk of huge gate leakage from metal – insulator - silicon substrate structure(source/drain probing pad – gate oxide – silicon back gate) specially with high gate voltage which is higher than breakdown voltage of gate oxide. At last, it’s very hard to decrease the air gap thickness even with critical point dryer process. This acts as an important obstacle for decreasing the pull-in voltage of the device. In the local metal gate scheme, the final air gap thickness can be reduced further with accurate control of gate

oxide deposition process precisely. This will be discussed in detail in chapter 5.

4.2.2 Device Fabrication of Back Gate NEMFET

Fig 4.3 summarizes the process flow of the back gate NEMFET. The basic process was same to NEMS switch device fabrication in chapter 3.3, I'll explain the fabrication process of the back gate NEMFET in short. To realize the back gate NEMFET with suspended nanowire channel, we used intrinsic Ge/Si core/shell nanowire as suspended channel, and fabricate metal electrode array as source/drain electrode to support the suspension of nanowire channel over the *p+* silicon substrate as back gate covered with 40*nm* ALD ZrO_2 as gate oxide.

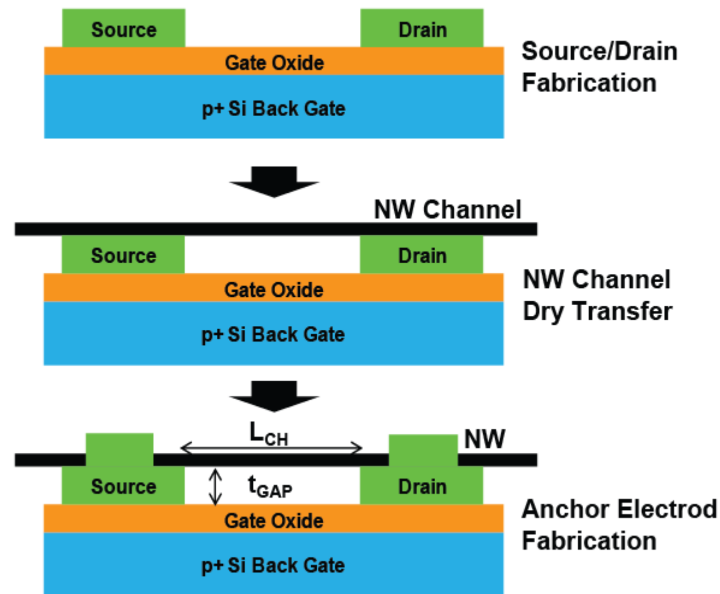

Fig 4.2: Schematic cartoon of process procedure for the back gate NEMFET with suspended i-Ge/Si core/shell nanowire channel.
Intrinsic Ge/Si core/shell nanowires were grown by vapor-liquid-solid process using previously described two-step growth process[42, 43].

For the intrinsic Ge/Si core shell nanowire, the intrinsic Ge core was grown first using gold colloids(Ted Pella) with diameters ranging from 10~15*nm* as catalyst seeds. The Ge nanowire was grown at 287°C for 60min using GeH_4 gas with total pressure of 300Torr, then the chamber heated up to 460°C which is the Si shell growth temperature within H_2 ambient. The silicon shell of thickness 2~3*nm* was grown at 460°C for 17*min* using SiH_4 with total pressure of 100Torr. No dopant was added during the whole process. After finishing the growth, the chamber was cooled down to room temperature with no gas flow. The target diameter was set to 25~30*nm* with 5*nm* silicon shell thickness.

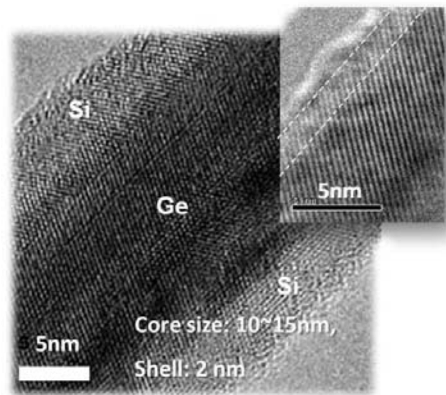

Fig 4.3: HRTEM image of the Ge/Si core/shell nanowire.

Fig 4.3 shows a representative high-resolution TEM (HRTEM) image of the Ge/Si core/shell nanowire. As shown in the figures and based on extensive TEM observations, the Ge cores have diameters of 10~25*nm* while the Si shells are typically 2~3*nm* thick, and the Si-Ge interface is epitaxial with no dislocations. The cross section of the wires are circular. The NWs typically exhibit a layer of ~1*nm* thick amorphous native SiO_2.

The *p*+ Si substrate covered with gate oxide(40*nm* ALD ZrO_2) is cut and cleaned in appropriate sizes. The high-*k* oxide is always favorable in terms of low V_{th} and small

sub-threshold swing with better gate coupling, but usually suffer from low breakdown voltage. We designed the straight and parallel source/drain electrode arrays without gate electrode.

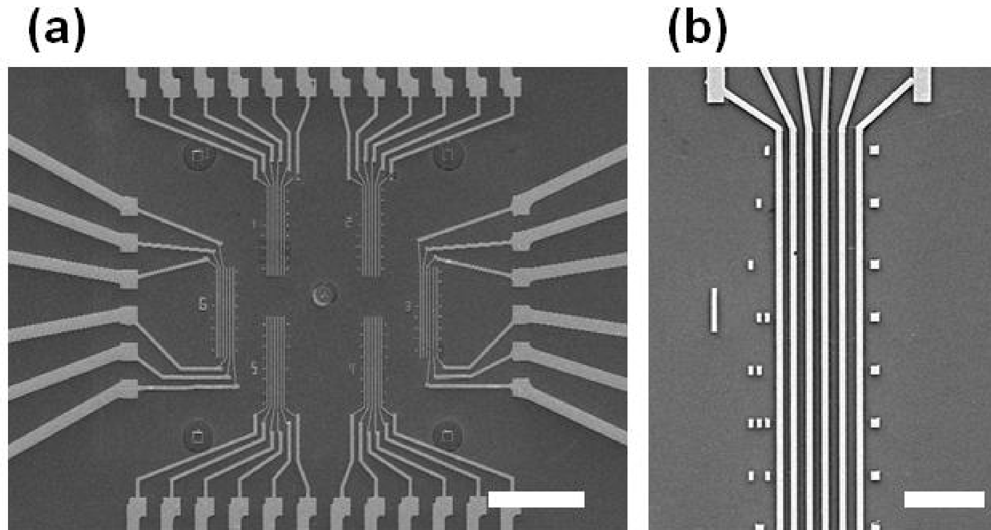

Fig 4.4: Plan-view SEM image of back gate NEMFET, (a) low magnification (scale bar=50*um*), (b) high magnification (scale bar=10*um*).

Fig 4.4 shows the design of the back gate NEMFET device. Another different point with NEMS switch design excepting gate-electrode-less is the wiring which connects the selected source/drain electrode to external probing pad was formed at the stage of patterning the source/drain electrode. This is for minimizing the parasitic conduction of unwanted nanowire channel among source and drain. If the wiring was formed after the nanowire channel transfer, the parasitic channel makes firm connection electrically and mechanically with the wiring metal. Furthermore, as I mentioned, the transfer process is random in density and position, there are a lot of nanowire on the substrate outside the electrode area. So, the parasitic conduction can screen out the electrical current of selected device severely. Different from this, the pre-formation of the

wiring line in the step of the source/drain electrode fabrication, the unwanted transferred nanowire channel was just place on the wiring line without electrical and mechanical contact.

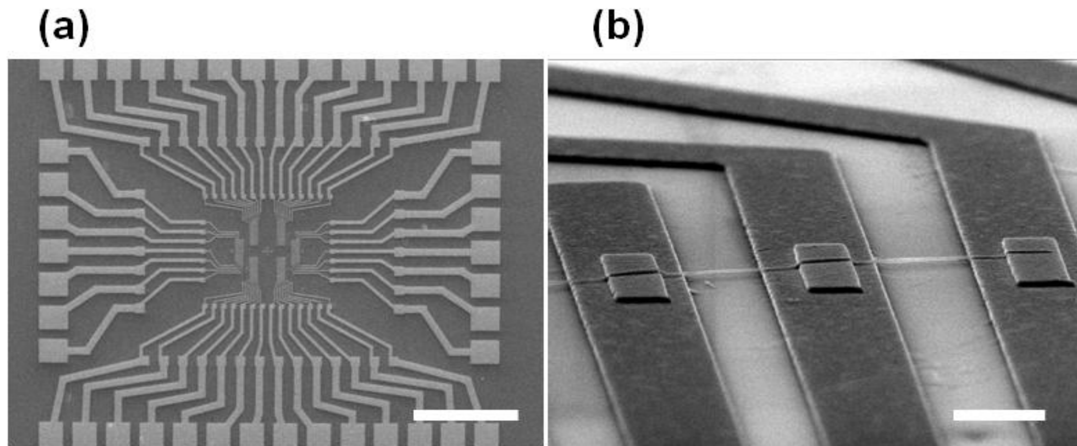

Fig 4.5: SEM image of fabricated back gate NEMFET with suspended i-Ge/Si core/shell nanowire channel, (a) low magnification (scale bar=200*um*), (b) high magnification (scale bar=1*um*).

As the gate electrode is not needed in the back gate NEMFET, the source/drain electrode as supporting suspended nanowire channel was patterned with E-beam lithography process without aligned to gate electrode, and Cr 5nm + Au film was deposited and lift-off in same way. The thickness of Au film is important as the air gap thickness, t_{gap}, is simply controlled by the Au deposition thickness. The L_{ch} was chose with the results of NEMS switch. After finishing the source/drain electrode array fabrication, the nanowire channel is transferred perpendicularly on the electrode array with dry transfer method. As the suspension rate of nanowire channels was varied, just same as NEM switch, we picked up the best suspended nanowire channel with plan-view and tilt-view SEM observation. After transferring the nanowire channel, anchor

electrodes process was followed. Different from the NEM switch, Ni 10*nm* was used as anchor electrode only for the ohmic contact to Ge/Si core/shell nanowire, and the wiring was formed with the source/drain already, so the adhesion with oxide is not a concern anymore. The NEMFET was selected after critical point dryer process with SEM observation.

Fig 4.5 shows the SEM image of the back gate NEMFET after whole process. The source/drain and anchor electrodes were patterned well with E-beam lithography, and the nanowire channel was suspended successfully after whole process.

4.3 Electrical Property of back gate NEMFET

4.3.1 DC Property

Table 4.2: Important parameters of back gate NEMFET switch with suspended CSNW channel.

S/D height	120*nm*(Cr+Au)	Anchor Electrode	60*nm*(Ti+Au)
Gate height	40*nm*(Cr+Au)	NW channel	i-CSNW
t_{gap}	80*nm*	NW diameter	28*nm*
L_{ch}	1.62*um*	Gate Oxide	40*nm* ZrO_2

To measure the electrical property of NEMFET, we used the Lakeshore vacuum probe station with HP4145B for V_d-I_d measurement, and DEQ of National instrument with Stanford SR570 current amplifier for V_g-I_d measurement at room temperature with the ~10^{-5}torr vacuum level. Fig 4.6 is the schematic of measurement system.

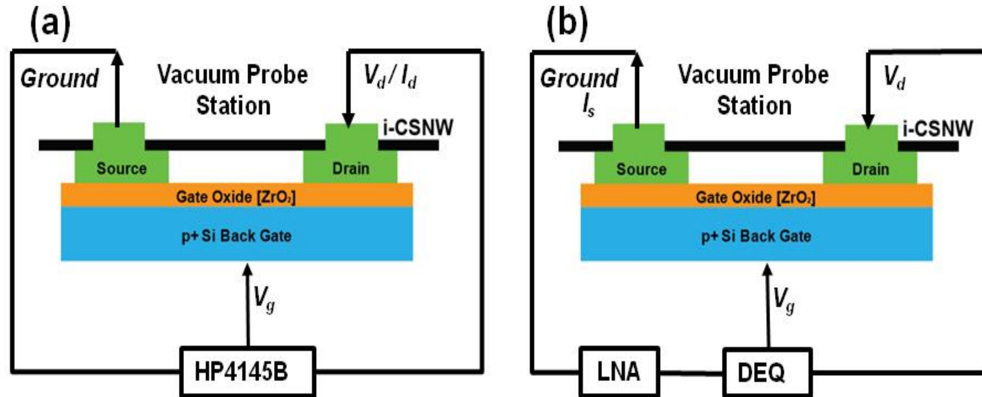

Fig 4.6: Schematics of measurement system, (a) V_d-I_d, (b) V_g-I_d.

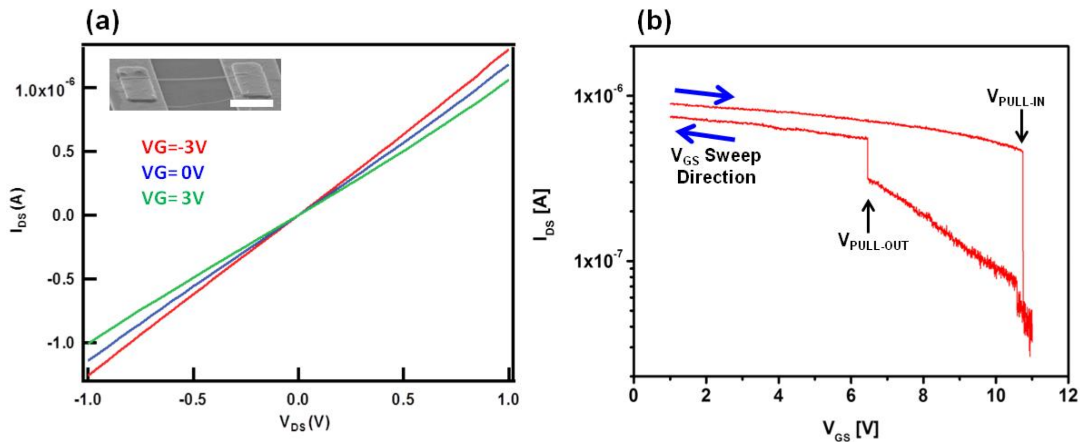

Fig 4.7: Transfer characteristics of NEMFET, (a) V_d-I_d *curve* (SEM image of measured device, scale bar=1*um*), (b) V_g-I_d *curve.*

Fig 4.7(a) is the V_d-I_d plot of NEMFET device with different V_g. The important parameters of device are summarized in Table 4.2. The top-left inlet of Fig 4.7(a) shows the tilt SEM image of device. The good ohmic contact and hole gas formation are achieved, and the small gate dependency of I_d can be an electrical evidence that the CSNW channel is suspended. As the CSNW channel is suspended over 80*nm* vacuum(same to 312*nm* SiO_2), the coupling with gate is very small, so the channel is still

remain on-state till large V_g(10V). With V_g sweep over the pull-in voltage, the V_g-I_d plot(Fig 4.7(b)) shows the abrupt transition from on-state to off-state at the pull-in voltage. The suspended CSNW channel abruptly touches the gate oxide due to electrostatic force from gate, then the CSNW is depleted with large coupling with positive gate voltage effectively. The pull-in occurs at V_{pi}=10.8V, and the on/off ratio ~10.7 with SS=15mV/dec. As the abrupt I_{on}/I_{off} transition of device comes from the mechanical motion, the SS is determined by the V_g sweep step only, and we can point out the SS can be almost zero if the V_g sweep step is small enough as

$$SS = \frac{Gae\ Sweep\ Step}{Log(\frac{I_{on}}{I_{off}})}. \quad (4.1)$$

The I_{on}/I_{off} at V_{pi} is smaller then simulation results, but it comes from large SS of stuck CSNW-FET(8V/dec). In back gate FET structure, the surface/interface state can increase SS of device with considering, because SS is 60mV x (C_{total}/C_g) at room temperature and C_{total} is the sum of all capacitances to the channel including parasitic contributions from intrinsic quantum capacitance of the semiconductor, charge traps, and source and drain electrodes. The on/off ratio can be increased significantly with local gate device with passivation process which will discuss in chapter 5 in detail. The back gate NWFET shows the V_{th}~5V, and the expected SS is 1.5V/dec in local gate device, which is extracted from back gate planar NW-FET using same nanowire with passivation, then the possible on/off ratio with local back gate NEMFET is 10^4 with I_{off} =40pA. We sweep down the V_g right after pull-in to confirm the pull-out behavior of device, and the pull-out occurs at V_{po}=6.5V. The V_{po} is smaller than V_{pi} as expected. The COMSOL 3D simulation(Fig. 4.8) shows the V_{pi} matches well with measured data, but V_{po} shows 16.4%

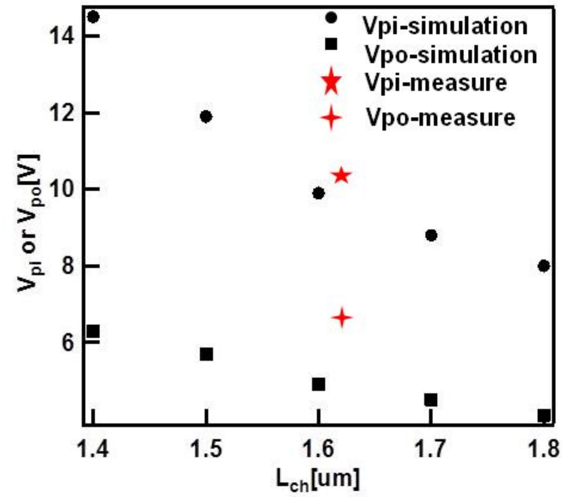

Fig 4.8: Comparison of Vpi, Vpo value between 3D COMSOL simulation and measurement results of NEMFET.

smaller value than simulation(5.4V). This can be explained with the residual tensile surface stress might comes from the lattice mismatch and the clamping method of the

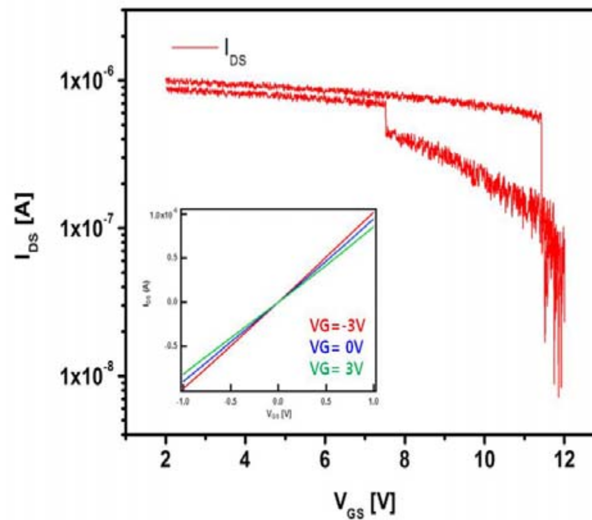

Fig 4.9: Pull-in and pull-out switching of other device, Inset is V_d-I_d curve.

device. The surface stress is added up to restoring force, so the V_{pi} can have a greater

value then the simulation. The similar NEMFET operation is demonstrated repeatedly with other device, and Fig 4.9 shows the results of it.

In back gate NEMFET measurement, we failed to get a multiple switching with this NEMFET, and there's misfit of I_d between sweep-up and sweep-down. This can be explained with the mechanical hardening effect of suspended channel with change of slack. This will be discuss in chapter 5 in detail, too. In addition, the noise under 100nA range is due to the reading range of DEQ is limited within 2 order. This noise issue was clear with using HP4155B parameter analyzer for the local metal gate NEMFET which will be discussed in chapter 5.

4.3.2 AC Property

One of the important factor on NEMFET is the operational speed of device. The speed at which NEMFET can operate is essentially limited by the suspended beam's mechanical resonant frequency. For a suspended beam, the resonant frequency f_o can be expressed as[41]

$$f_o = 1.03\frac{d}{L^2}\sqrt{\frac{E}{\rho}}, \tag{4.2}$$

where E is Young's modulus, ρ is the mass density, d is the thickness of the beam(in this case, the diameter of CSNW) in the direction of motion, and L is the length of the suspended beam. As the suspended channel is core/shell structure of Ge/Si, it's not easy to calculate the exact resonant frequency, but it should be a value between Ge-only f_o 34MHz and Si-only f_o 70MHz in same device dimension. So, we use the so-called single source method which measured I_{MIX} current using a NEMFET as a signal mixer.

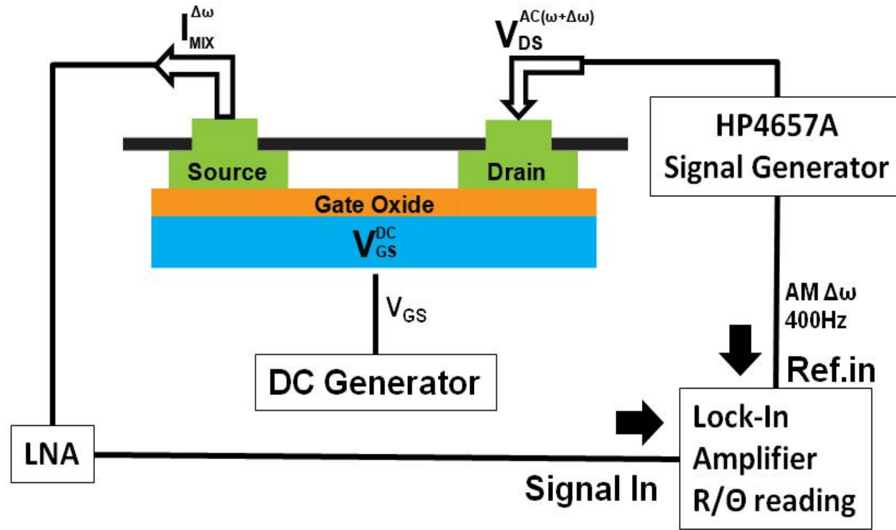

Fig 4.10: Schematics of measurement system for one-source method.

Fig 4.10 illustrate the concept of measurement[44]. The signal V_d^{ac} with frequency ω and amplitude modulated at $\Delta\omega$ is applied to drain electrode, while the gate electrode is held at a constant DC voltage V_g^{dc}. The intermediate band width mixing signal(AM 400Hz) by NEMFET is detected by low frequency lock-in amplifier. The mechanical motion of suspended NW channel cause a modulation of the capacitance between NW and the gate, making a modulation of output current at the drive frequency ω, and it shows the maximum value at the resonant frequency f_o. The shape of peak can be a various shape depending on the phase difference between reference signal and I_{MIX} signal. The I_{mix} follows the below[45]

$$I_{mix}(\omega) = A + B\omega + \frac{H\cos\left(\arctan\left(\frac{f_0^2-\omega^2}{\frac{f_o\omega}{Q}}\right)+\Delta\emptyset\right)}{\sqrt{\left(1-\left(\frac{\omega^2}{f_0^2}\right)^2\right)^2+\frac{\omega}{f_oQ}^2}}, \tag{4.3}$$

where, A,B,H, f_o, Q and $\Delta\emptyset$ are the independent fitting parameters. ω is the drive frequency, f_o is resonant frequency, and Q is quality factor. Fig 4.11(a) is the plot of I_{mix}

vs. drive frequency in different drive amplitude at V_g^{dc} is held to 1V. The I_{mix} peak shows f_o is 57MHz with drive amplitude 20mV, and the f_o increase non-linearly with increase of drive amplitude (Fig 4.11(b)).

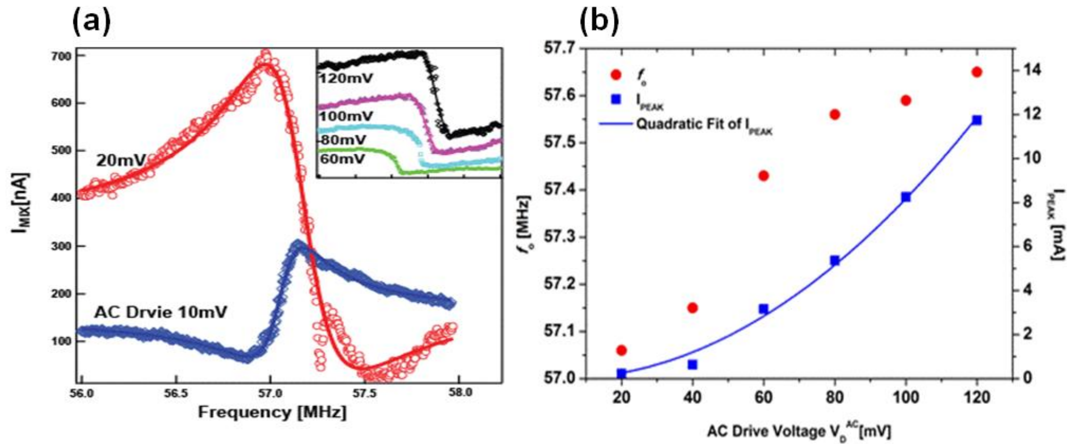

Fig 4.11: Measurement results of resonant frequency. (a)Frequency vs. I_{mix} plot in different AC drive amplitude. The data was taken at V_g^{dc}=1V. The each line is the fitted value with the analytical equation of I_{mix}. (b) The dependency of resonant frequency f_o and I_{peak} vs. AC drive amplitude.

The measured point fits well with Equation 4.3. The shape of peak can be varied with phase difference *Δø*). The measured resonant frequency 57*MHz* is fit very well with Ge/Si CSNW COMSOL simulation with bulk value of Young's modulus and density. In general, NW resonator shows smaller Young's modulus due to compress stress in the surface with small diameter NW less then 100nm[46, 47], but Si shell has smaller lattice constant than core Ge. This lattice mismatch makes tensile stress in the surface of CSNW resonator, which is not released due to very thin shell thickness(2.5nm), so the simulation results with continuum elastic theory equations fit very well with experimental results. The quality factor *Q*, which is defined as the ratio of the energy stored to the energy lost per cycle, of device is 201 with drive amplitude 20*m*V. The resonant frequency is

inversely proportional to the scale of the structure, but *Q* factor decreases with increasing of resonant frequency. The *Q* factor of our device is comparable to the previous study using 30*nm* diameter and 1.8*um* length double-clamped SiNW resonator with resonant frequency 75MHz and Q factor 700[35], considering the smaller diameter and core Ge with lower Young's modulus of our device. Fig 4.12 shows the typical non-linear increase of I_{peak} with increase of drive amplitude. This behavior arises because the V_d^{dc} driving term contributes to an AC force term that is proportional to $(V_d^{dc2} + V_d^{ac2})/2$ [35].The non-linear shift of f_o with drive amplitude tells the resonator operates in the elastic hardening types of frequency tuning for vibration in plane of the gate[41].

4.4 Conclusion

In this chapter, we demonstrate the back gate NEMFET with suspended i-Ge/Si core/shell wire channel with V_{pi}=10.8V, V_{po}=6.5V with *SS*=15mV/dec successfully. The back gate structure has the limitation due to large gate leakage current path, the difficulty in decreasing final air gap thickness, and I_{on} mismatch before and after pull-in, etc. These problems can be solved with the local metal gate NEMFET, and will be discussed in next chapter.

4.5 Acknowledgement

Chapter 4 is in part a reprint of "Steep Subthreshold Slope Nano-electro-mechanical Field Effect Transistors with Nanowire Channel and Back Gate Geometry", to appear in *Device Research Conference,* (2013).

Chapter 5

Local Metal Gate NEMFET with Suspended Nanowire Channel

5.1 Introduction

Table 5.1: The Important problems of back gate NEMFET and the solution.

	Reason	Solution
Ion Hysteresis	Large t_{gap}	Accurate t_{gap} control with Passivation process
On/Off ratio	*SS* of NWFET	Coupling improvement, D_{it} decrease with passivation
High-k dielectric on metal	Morphology from Au	G_{ox} on NW channel
Gate leakage current	MIS structure of probing pad	Local metal gate Selectable electrode scheme
Parasitic current	Random position of NW channel	Selectable electrode scheme

To realize near-zero sub-threshold slope NEMFET, we demonstrate NEMS switch and back gate NEMFET with suspended Ge/Si core/shell NW channel successfully. But, back gate device still have a few problems to be solved. Table 5.1 summarize the problems of back gate NEMFET and solutions. In this chapter, we will demonstrate the local metal gate NEMFET with suspended NW channel showing multiple switching with various solutions to overcome the disadvantage of back gate structure.

5.2 Device Design

To solve the critical problems of back gate NEMFET, we adopted passivation process of suspended nanowire channel and selectable electrode scheme. In this chapter, we will explain about these schemes in detail.

5.2.1Atomic Layer Deposition for High-k Gate Oxide

To realize NEMFET, the high-k gate oxide process is essential. Furthermore, the gate oxide should be deposited on the 3-D structure with good step coverage, and the low process temperature must be to compress the abnormal oxidation of suspended nanowire channel as the gate oxide will be deposited on the suspended nanowire channel, too. The atomic layer deposition is the best process which meets the standard above. In material part, HfO_2 was selected, as HfO_2 is widely use as the high-k gate oxide due to its reasonably high dielectric constant(>20), themodynamic compatibility with Si, gate poly Si compatibility, and a relatively large band gap(~5.68eV)[48]. Beneq TFS2000 ALD system was used for the deposit HfO_2 film for NEMFET.

Fig 5.1 is the schematic of ALD valve system. The growth rate and the quality of film was controlled with valve timing and deposition temperature mainly. The system can control the valve open time with millisecond level, and utilize the solid and liquid source both. The detail process condition was summarized in Table 5.2. Except the process condition in Table 5.2, the valve timing is very important factor for controlling the quality of oxide film, but it’s not a main issue of the thesis, so I skip in detail.

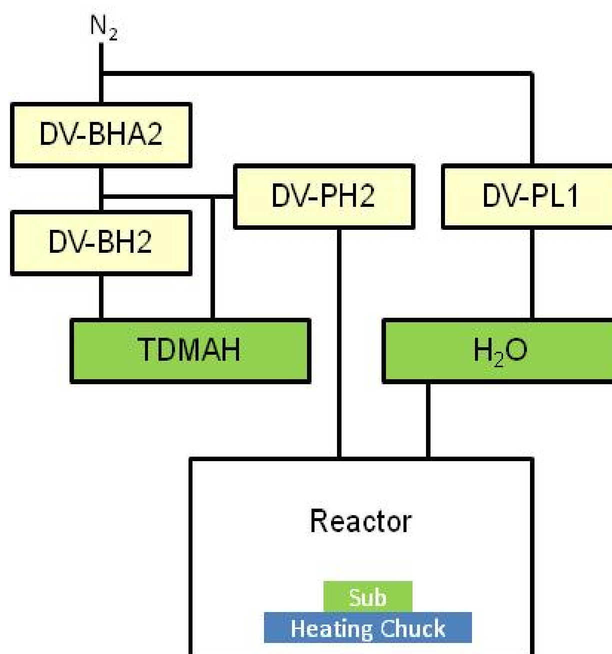

Fig 5.1: Schematic structure of ALD system with TDMAH and H_2O source.

Table 5.2: Process condition of HfO_2 film with ALD system.

System	Beneq TFS200
Hf source	TDMAH(solid)
Oxygen source	H2O(liquid)
Purge gas	Nitrogen
Deposition temp.	200^oC
Pre-treatment	Acetone+IPA
Top electrode	Cr+Au E-beam litho+Lift-off
Imaging	Plan SEM
Thickness measurement	Ellipsometry
CV/IV	Agilent BC1500

TDMAH(solid phase) was used as Hf source, and H_2O(liquid phase) was used for oxygen source. The TDMAH was maintained in 55°C, and H_2O temperature was in room temperature. The chuck temperature was set to 200°C during the deposition. We varied the important parameters like the deposition temperature, the source valve timing, and the thickness of the oxide film, and the condition in Table 5.2 showed the best results. The metal-insulator-Si(MIS) and metal-insulator-metal(MIM) capacitor structure was fabricated on the *p*+ Si and Au substrate. Au substrate was prepared exactly same to the

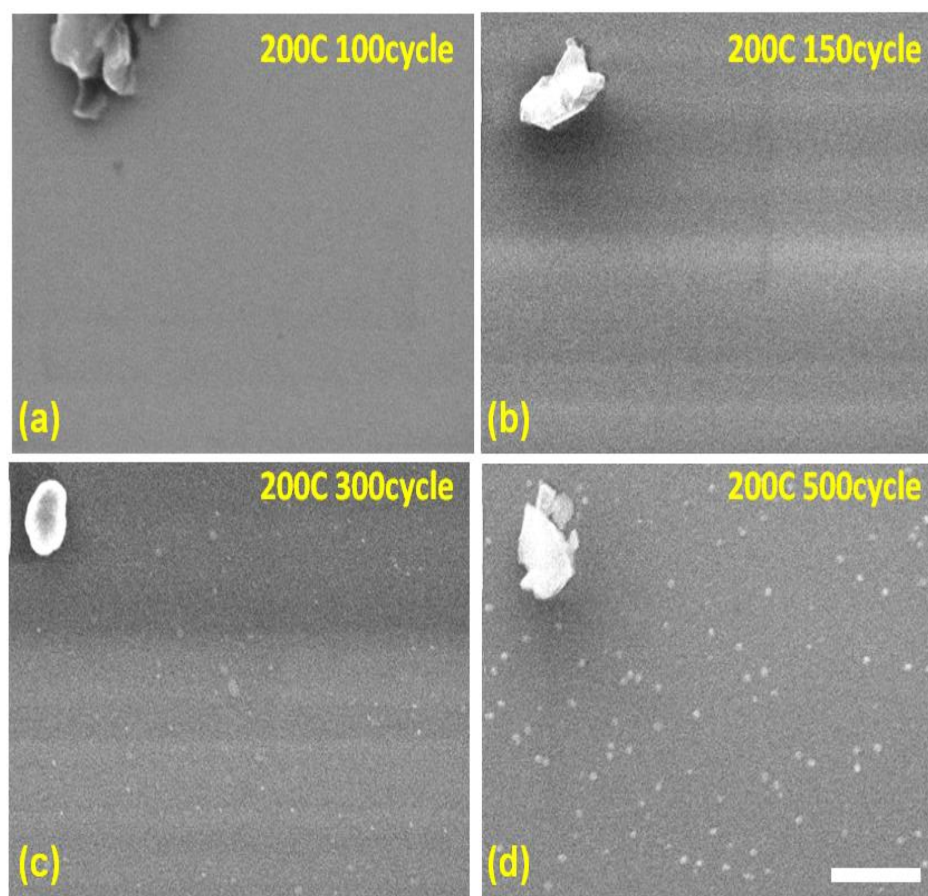

Fig 5.2: Plan-view SEM of HfO2 film deposited on Si substrate with ALD system. The deposition cycle number is varied with (a)100cycle, (b)150cycle, (c)300cycle, (d)500cycle(The scale bar is 500nm).

local metal gate of NEMFET to reproduce real device condition. Cr+Au top metal electrode was patterned using E-beam lithography process followed by metal evaporation process, and the electrical property of MIS/MIM capacitor like CV/IV was measured with Agilent BC1500. We measured the deposition thickness of oxide with ellipsometer /vertical SEM, and the morphology of film was confirmed with planar SEM observation.

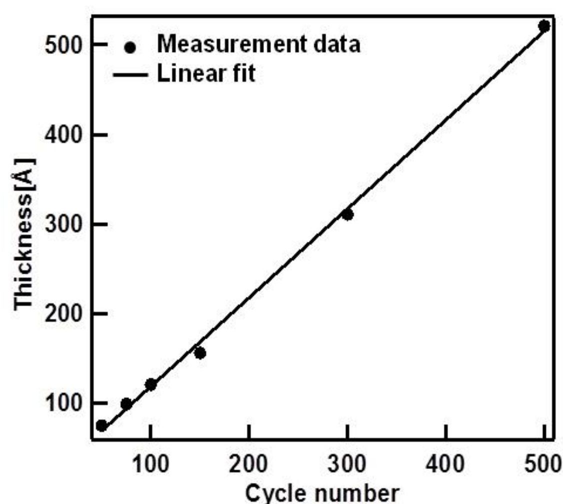

Fig 5.3: ALD cycle number vs. measured thickness plot of HfO2 film. The thickness is measured with ellipsometer .

Fig 5.2 shows the plan-view SEM image of HfO_2 film on Si substrate with different cycle number. Till 150cycle, the oxide film shows the smooth surface, but abnormal particle generation observed from 300cycle films. The target thickness of film is less than 15*nm*, and the growth rate is ~0.1*nm*/cycle(Fig 5.3), the particle generation was not a critical consideration in process set-up.

Fig 5.4(a) is the schematic MIS structure to characterize the electrical property of HfO_2 oxide film, and Fig 5.4(b) shows the dielectric constant vs. the oxide thickness

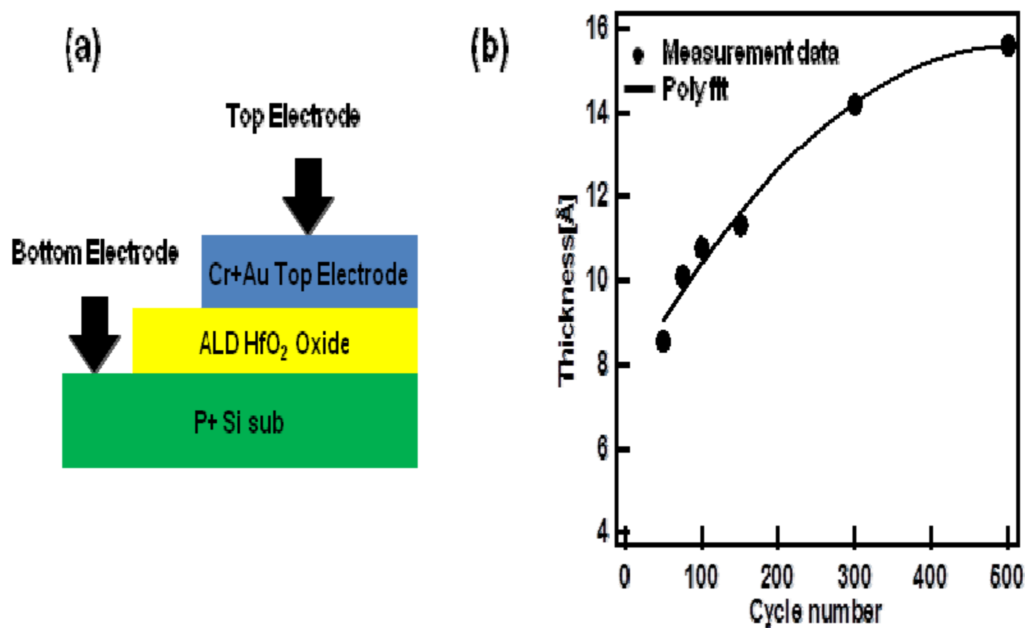

Fig 5.4: MIS capacitor characterization, (a) Schematic structure of device, (b) Measured dielectric constant with ALD cycle number.

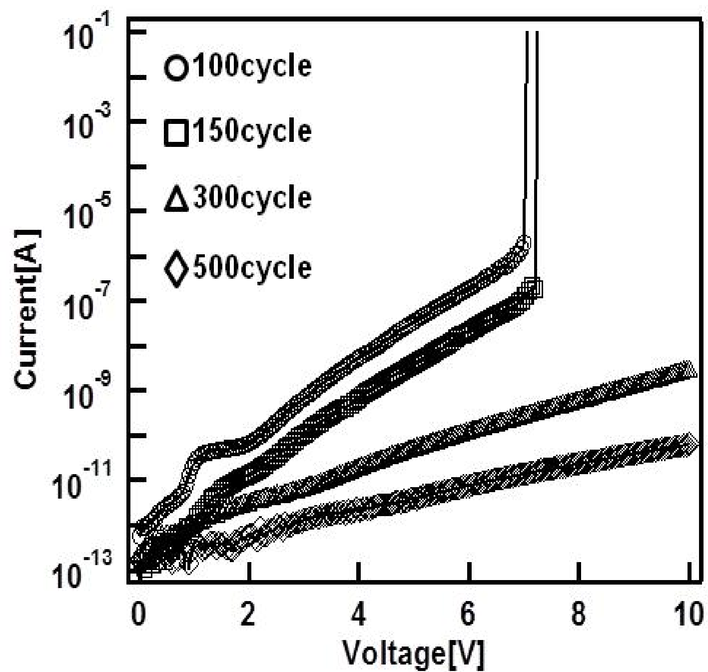

Fig 5.5: Oxide leakage current property with different cycle number.

relation. There's obvious drop of dielectric constant with the decrease of oxide thickness less than 20*nm*. This region is the important oxide thickness range, as we will use 15*nm* or less. This behavior was reported previously, and explained with the existence of thin interfacial layer even with Hf treatment before ADL process[49]. In addition, we didn't add any pre-treatment like Hf or BOE etch of Si substrate before ALD to reproduce a same condition of NEMFET as suspended nanowire channel can't be treated, neither.

Fig 5.5 is the oxide leakage current property with different thickness. The base level of leakage current is important, but the breakdown voltage is more important. The area of MIS pattern is 100*um* x 100*um*, and the contact area at the NEMFET between the NW channel and the bottom metal gate in pull-in condition is less than 100*nm* x 30*nm*. So, the leakage current level can be negligible except breakdown condition. The breakdown voltage of 100cyle is 7V, and 150cycle is 7.2V, not enough for the high V_g for pull-in. This can be another reason to adopt the nanowire channel passivation process, which will discuss in later.

Different from MIS property, we failed to have reasonable quality oxide film on MIM structure. In every condition and thickness, the capacitor showed very high leakage current even with less than 1V of V_g. I couldn't measure CV, of course, due to the huge loss. Furthermore, the thickness measurement with ellipsometer was very unstable due to large diffused reflection from the Au surface. We can find the reason of this phenomena from the roughness of Au surface itself. Although, we didn't deposit decent gate oxide on metal substrate, it might not be a serious problem with considering the area difference between the test pattern and real NEMFET device. This will be discussed in the electrical property part.

As summary, we set up the gate oxide process with ALD. The dielectric constant is ~10, and the breakdown voltage is ~7V with good morphology.

5.2.2 Passivaition Effect

In NEMFET device with suspended NW channel, the I_{on}/I_{off} ratio is the one of the most important factor of the device. To obtain high I_{on}/I_{off} ratio, inverse sub-threshold slope (SS) of the pull-in stage should be minimized, as

$$\frac{I_{on}}{I_{off}} \approx 10^{\left(\frac{V_{pi}-V_{th}}{SS}\right)}. \quad (5.1)$$

To confirm the passivation effect of CSNW channel, we fabricated back gate NW channel transistor (Fig 5.6). *p*+ Si substrate covered with 30*nm* SiO_2 layer is used as back

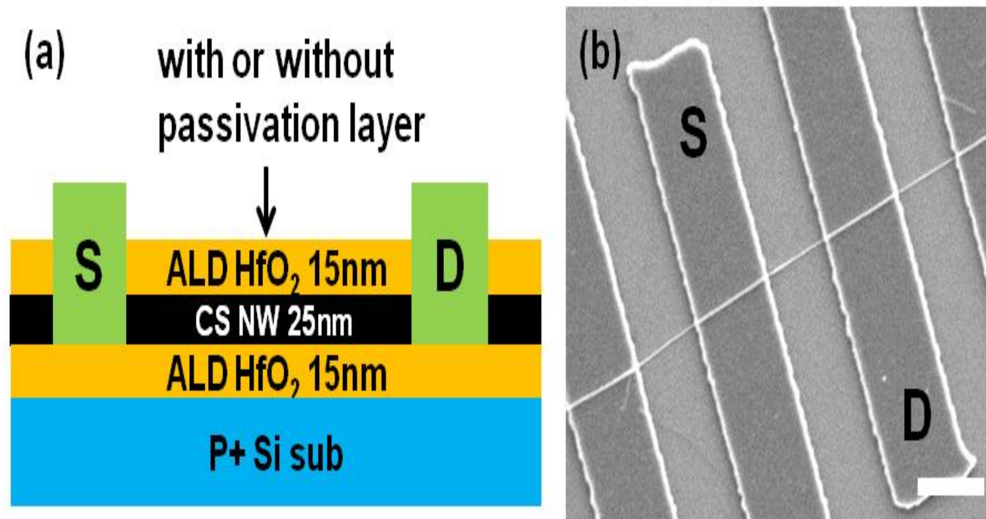

Fig 5.6: i-CSNW planar FET with back gate.(a) Schematic structure of the device. The measurement is done with or without passivaition, (b) Plan-view SEM of the device(Scale bar is 1*um*).

gate substrate. The same CSNW used for NEMFET device is transferred on the back gate substrate with dry transfer method. The Ni layer is patterned as source/drain contact and probing pad using E-beam lithography and E-beam evaporation method followed by lift-off with Acetone. Fig 5.6(b) is the plan-view SEM image of a representative device. The defined channel length is 880*nm*, and the diameter of NW channel is 26*nm*. After fabrication, we measured electrical property of back gate NWFET within vacuum probe station (base pressure < 1×10^{-4} torr). After the measurement, we passivated the entire device with 150 nm thick ALD HfO_2 layer. After passivation, we measured the electrical property of same NWFET again to compare the effect of passivation. The blue line in Fig 5.7 is V_g-I_d curve of NWFET without passivation. *SS* is 3.3V with V_{th}=2.6V and maximum I_{on}/I_{off}= 60. With passivation, the transfer characteristics (red curve in Fig 5.7)

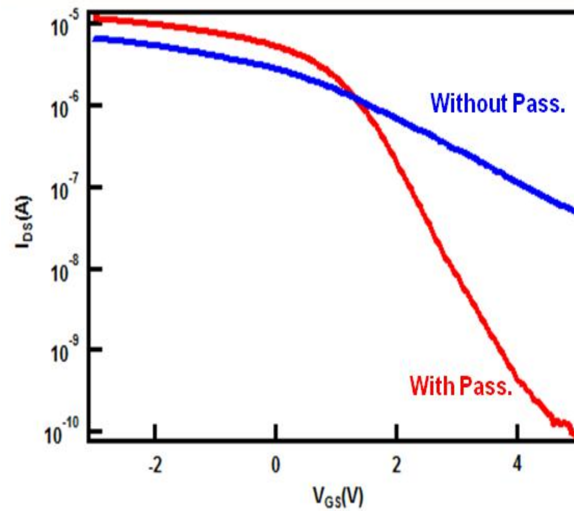

Fig 5.7: Comparison of V_g-I_d characteristic between passivation and no-passivation planar FET with i-CSNW channel.

are improved dramatically with SS=0.7V, V_{th}=1.7V, and I_{on}/I_{off}=10^5. In the sub-threshold region, SS is determined by the factor $C_{it}/C_{ox}(SS=60mV\ x\ (1+C_{it}/C_{ox}))$, and $C_{ox_pass}/C_{ox_no\text{-}pass}$ = 2.1 with COMSOL simulation. With the passivation, the gate capacitance increases almost twice, furthermore, C_{it} can be reduced 37.6 % as HfO_2 layer passivate the surface states of Si shell successfully.

5.2.3 Selectable Electrode Scheme

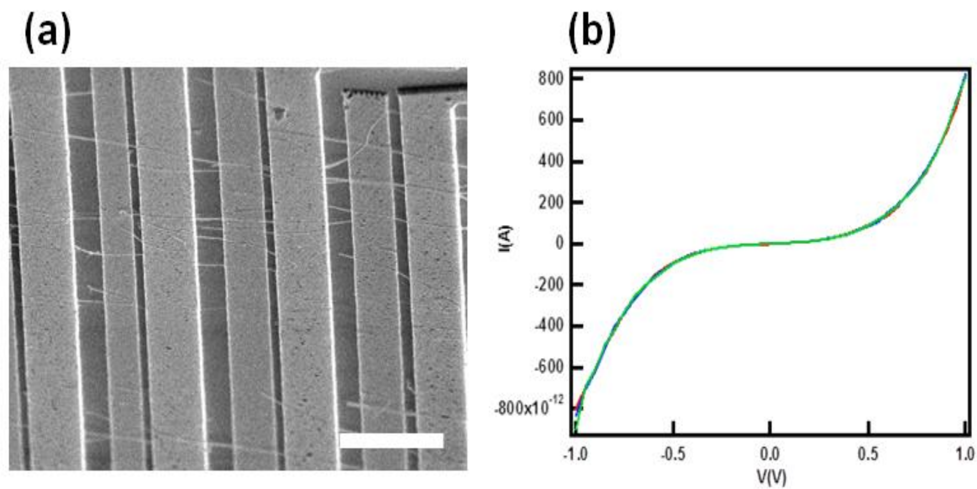

Fig 5.8: Parasitic conduction path of NEMFET, (a)Tilt-SEM after nanowire transfer. The position of nanowire is random(Scale bar=2*um*), (b)V_g-I_d curve at V_d=1V of parasitic channel without anchor electrode.

As the dry transfer was random process in density and position, the parasitic nanowire channel between source and drain, or source/drain and gate can be formed in unwanted position. As you see in Fig 5.8(a), the nanowire channel can be placed anywhere over source/drain electrode because the dry transfer process is totally random except the directionality. In case of the local metal gate process, the unwanted channel

formed between the gate and the source/drain can be critical gate leakage current path before the pull-in is occurred. Usually V_{pi} can be a range of a few V to more than 10V, this severe gate leakage current can block meaningful device current partially or fully even the leakage path is not connected to source/drain electrode with anchor electrode process. Fig 5.8(b) is the representative V_g-I_d curve of the device without anchor electrode process.

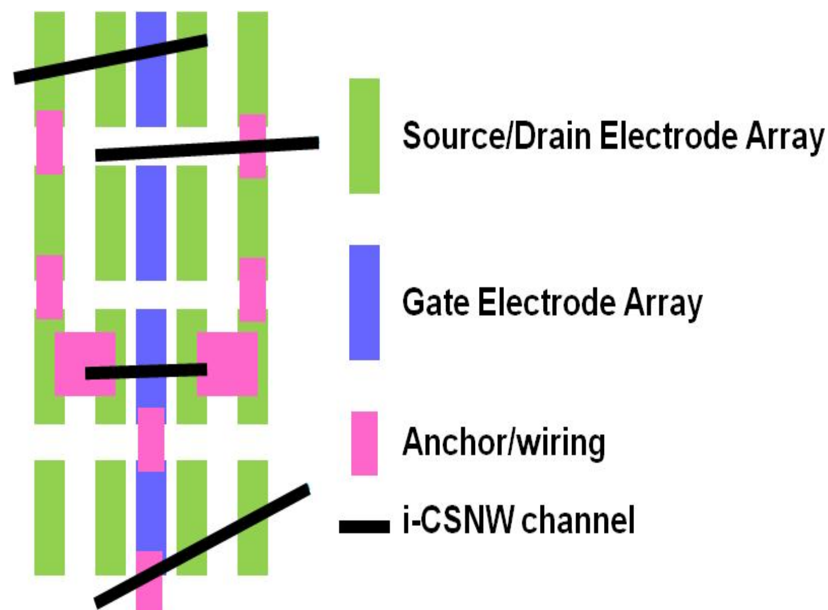

Fig 5.9: Schematic design of selectable electrode scheme.

The current level can reach hundreds of nA as the multiple nanowire leakage path can be formed in parallel. The parasitic current will block every meaningful NEMFET signal, so termination of parasitic current is so essential to increase the yield of NEMFET device. As a solution, we designed the selectable electrode array scheme with patterned isolated electrode arrays. Only selected electrodes after SEM imaging observation are connected

in subsequent steps to the probing pad during the anchor electrode deposition step. Fig 5.9 is the plan-view layout of selectable electrode scheme.

5.3 Device Fabrication

Fig 5.10 shows the schematic of the fabrication process. The *p*+ Si substrate covered by 300 nm thermal SiO_2 is cut and cleaned in appropriate sizes followed by patterning of the source/drain electrodes with E-beam lithography process (JEOL6400 SEM combined with NPGS software) and electron beam metal evaporation with 5 nm Cr and 90 nm thick Au and a conventional Acetone lift-off process. The gate electrode is patterned with same procedure aligned with the source/drain electrodes but with a smaller thickness at 5 nm Cr and 35 nm Au. To avoid parasitic conduction from unwanted parallel NW channel formation, a selectable electrode array scheme was used. As the dry transfer was random process in density and position, the parasitic nanowire channel between source and drain, or source/drain and gate can be formed in unwanted position. The parasitic current will block every meaningful NEMFET signal, so termination of parasitic current is so essential to increase the yield of NEMFET device. As a solution, we designed the selectable electrode array scheme with patterned isolated electrode arrays. Only selected electrodes after SEM imaging observation are connected in subsequent steps to the probing pad during the anchor electrode deposition step. The initial air gap thickness of device is controlled by the differential thickness of metal films with in-situ thickness monitoring sensor during the evaporation process and confirmed afterward with AFM and tilt-SEM observation.

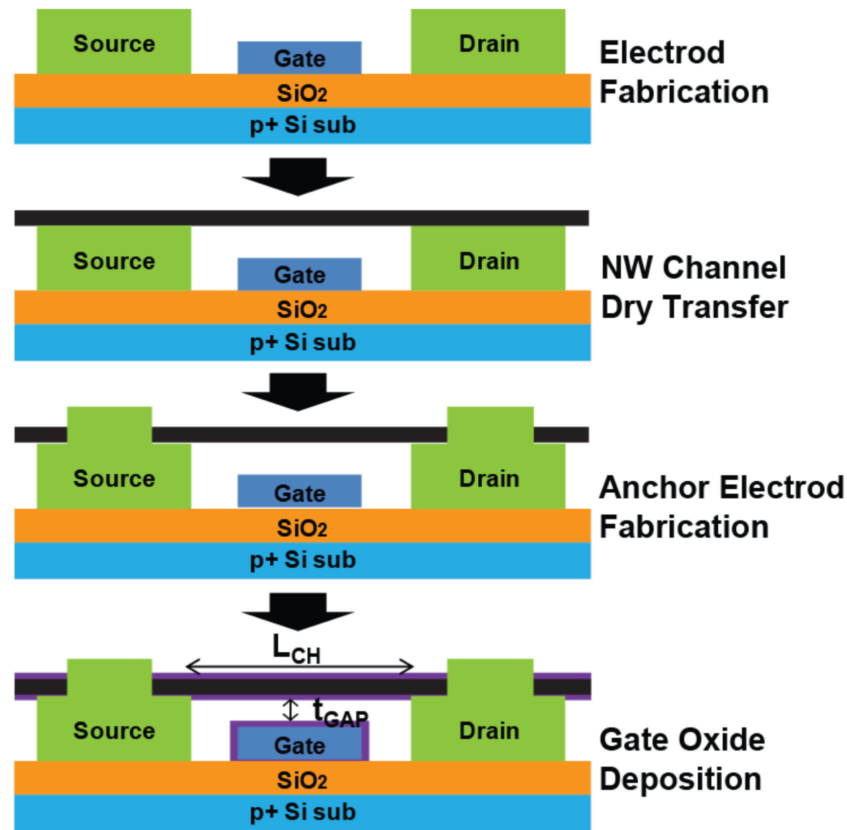

Fig 5.10: Schematic process flow of NEMFET with suspended i-CSNW channel.

The expected $t_{gap_initial}$ is 55*nm*(95*nm*-40*nm*). The channel length is designed as 1.3um. After finishing preparation of electrodes, the Ge/Si core/shell NWs, grown with VLS method in LPCVD with Au nano-particle, were transferred to the electrode perpendicularly with the dry transfer method in which the growth wafer containing nanowires was rubbed manually across the electrodes in a chosen direction, leaving aligned parallel nanowires on the electrodes. The successful suspension of CSNWs was verified at this stage from the plan-view/tilt-view SEM observation. E-beam resist (MMA+PMMA double layer) is spin coated covering the entire wafer and over the suspended nanowire, followed by one more e-beam lithography, metal deposition, and

liff-off to fabricate Ni anchors (130*nm* thick) as well as electrode wiring in the selected source/drain/gate electrode positions towards bonding pads predefined at the edge of the chip. We used the critical point drying at the final drying process after anchor electrode lift-off to increase the suspension yield and minimize a slack of CSNW channel.

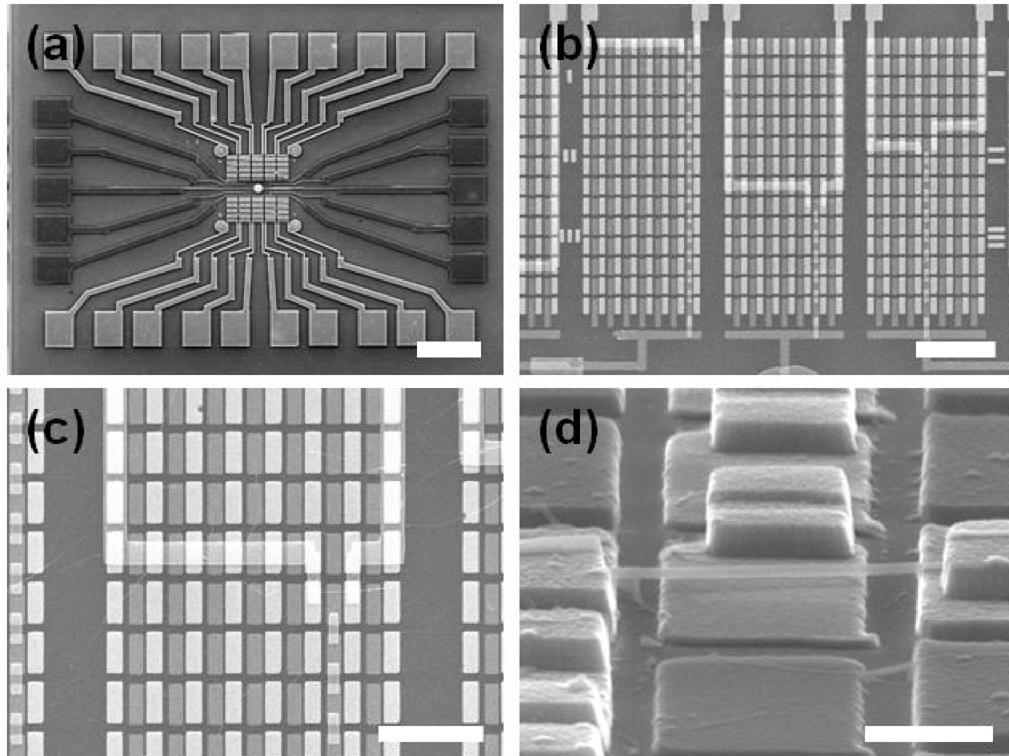

Fig 5.11: SEM images of fabricated NEMFET device with different magnification. (a) low magnification(scale bar=100*um*), (b)mid magnification(scale bar=10*um*), (c) mid magnification(scale bar=5*um*), (d)high magnification(500*nm*).

Finally, to define the gate oxide and to passivate of NW surface, we deposited a HfO_2 thin layer with atomic layer deposition system using TDMAH solid source for Hf and H_2O for oxygen. The TDMAH temperature is set to 55°C, and deposition temperature is 200°C. As the gate oxide is deposited uniformly over the suspended NW channel and

bottom gate electrode, we expect the final air gap thickness to be further reduced by twice the oxide thickness. The thickness of gate oxide is carefully selected to balance the reduction of the final air gap thickness, increase in the final diameter of suspended NW channel, and the breakdown voltage of the deposited gate oxide.

Fig 5.11 is the SEM images of NEMFET device with various magnifications. In Fig 5.11(a), the device area(source/drain/gate electrodes) is located in center of the device, and connected to probing pad with local wiring. The difference of color in probing pad comes from the difference metal thickness between source/drain and gate. Fig 5.11(b), (c) are mid magnification SEM image which show the selectable electrode scheme well. The anchor electrode and the local wiring connection are fabricated together using Ni. The difference in contrast of Ni layer is clear in SEM image. In high magnification tilt-view SEM(Fig 5.11(d)), we can confirm the NW channel is suspended successfully after whole process. The shadow beneath suspended channel can be another evidence of the suspension. Furthermore, we can check that the NW channel over the source/drain electrode is slightly varied in thin HfO_2 layer. And, the thin bright layer of the circumference of suspended NW channel is visible in the image, too. Some residues are observed in high magnification image, and this residues can be the one reason of the limted Ion/Ioff ratio in NEMFET device. I tried to keep the whole process as clean as possible, but some inevitable step is in bottom up process.

5.4 Electrical Property

5.4.1 DC property

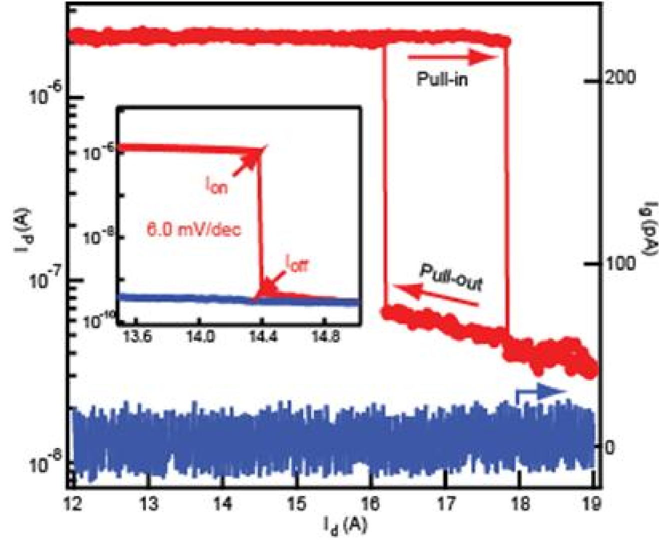

Fig 5.12: V_g-I_g curve of NEMFET with abrupt "pull-in", "pull-out" behavior. The inset is another V_g-I_g curve showing SS=6mV/dec.

Fig 5.12 is V_g-I_d and V_g-I_g data that demonstrate SS=11.7mV/dec. The I_d drops abruptly at V_{pi}=17.8 V and go back to on-stage at V_{po}=16.2V. SS of NEMFET can be minimized further with the maximization of I_{on}/I_{off} at V_{pi} point, as SS=(Gate voltage Sweep Step) / $log(I_{on}/I_{off})$. The reason of small on-off ratio in Fig 5.12 can be explained with the big SS value of pull-in state. The basic operation principle of NEMFET is the minimization of SS using the different electrical state between suspended and stuck-channel over the bottom gate. So, I_{off} is governed by the SS of stuck-channel state, as $I_{off} \approx I_{on} / Exp\ [\ (\ V_{pi}-V_{th_stuck})\ /\ SS_{_stuck}\ ]$.

Fig 5.13 shows the simulation results of CSNW NEMFET with different doping, which the higher doping make SS value increased. We grow intrinsic CSNW and use clean-room environment for fabrication, there is always risk of unwanted doping or contamination from CVD chamber, chemicals of wet process, photo resist residue and inevitable exposure to normal air for SEM observation before HfO_2 passivation process.

These uncertain factors can cause the degraded electrical property of NEMFET.

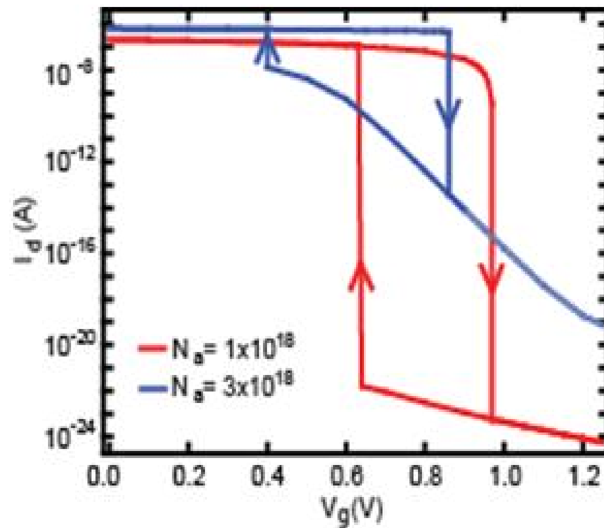

Fig 5.13: Simulated V_g-I_g curve of NEMFET with different doping level. The condition is summarized in chapter. 2.

Small pull-in voltage has always been the promise of nanoscale NEMS switches[20]. Though the V_{pi} values here are more than 10 V, it is important to note that the V_{pi}-V_{po} window is only 1.6 V in Fig 5.12. Traditionally, transistor threshold voltages can be shifted by engineering the gate stack work function. In the case of mechanical switches, it has also been proposed that by using trapped charges in the oxide layer, the absolute values of V_{pi} and V_{po} can be shifted closer to zero[50] and only a voltage slightly higher than the 1.6 V window may be needed for our NEMFET. Combined with further reduction of our x_{gap} from 35 nm, it is possible to achieve sub-1 V operation NEMFETs (Fig 2.7). The I_g remains sub-100pA level during the entire measurement range, it means the switching comes from the real mechanical motion of suspended NW channel. The inset graph is the pull-in behavior of the device with a smallest *SS*. The on-off ratio is

2173 which the current change before and after the abrupt pull-in, and *SS* is .6.0*m*V. We can say the *SS* value is near-zero as it is simply dominated by the V_g sweep step (20*m*V/*dec* in this case) with the given on/off ratio.

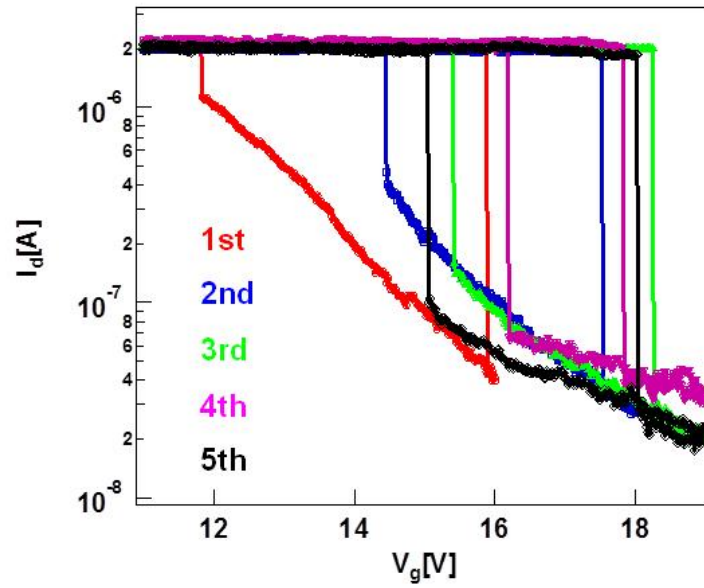

Fig 5.14: V_g-I_g curve of NEMFET with multiple switching behavior.

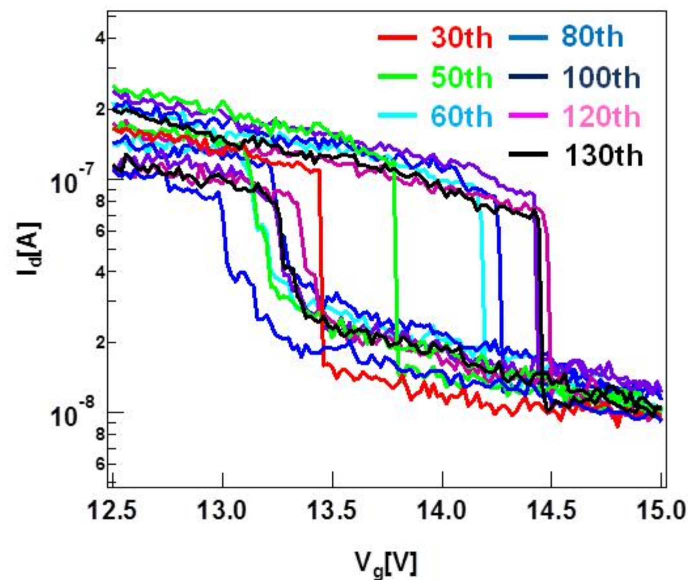

Fig 5.15: V_g-I_g curve of NEMFET with 130times switching behavior.

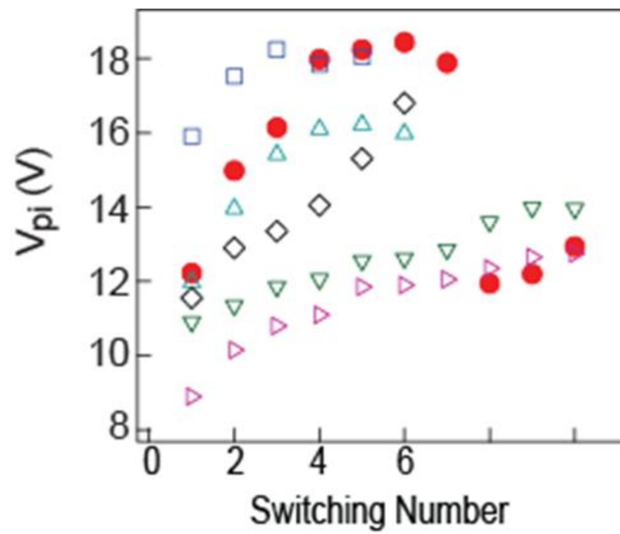

Fig 5.16: Increase of *Vpi* in first a few switching in various devices.

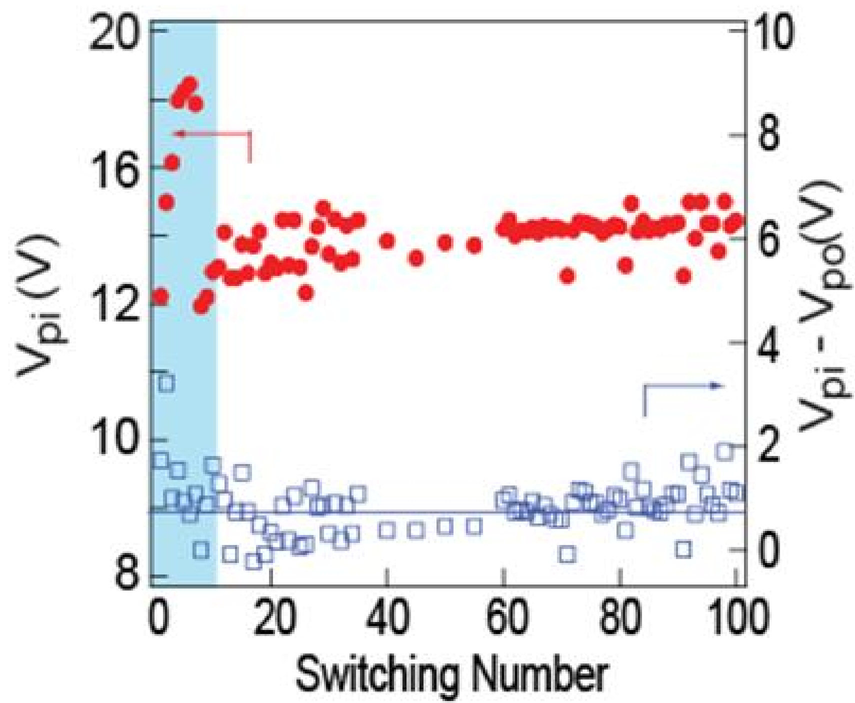

Fig 5.17: Switching number vs. V_{pi} and V_{pi}-V_{po} plot of 130times switching NEMFET device.

Fig 5.14 is V_g-I_g curve at $V_d = 1$V of the device showing sharp pull-in and pull-out behavior of 5 times. SS is all 12.0/11.5/11.6/11.6/11.2*m*V/*dec* with switching cycle number. Pull-in voltage starts from 15.9V, and increases up to 18.2V, which showing gradual increasing.

Fig 5.15 shows I_d-V_g data from another device showing multiple switching up to 130 times after which the device failed due to stiction. Compared to recent NEMS switches where only one or a few switching cycles can be observed[20,24,50], our results demonstrate the benefit of a 3-terminal device design where the gate electrode does not need to electrically contact the NEMS beam thus greatly minimizing device wear. To visualize device stability over time, we plot the trend of V_{pi} and V_{pi}-V_{po} window size in Fig 5.16, 5.17 vs switching numbers. In all 6 different devices in Fig5.16, V_{pi} increases within the first few cycles (also see blue shaded region in Fig 5.17), which we believe may be attributed to hardening effect of a doubly-clamped NW beam with repeated mechanical movement. Beyond the first few cycles however, Fig 5.17 shows that V_{pi} remains stabilized at ~15 V for up to 100 times, suggesting that the device has settled. Interestingly, despite the V_{pi} variation, the V_{pi}-V_{po} window remains stable at 0.83$\pm$0.52 V (Fig 5.17) throughout the 100 cycles. Notice that a drop in V_{pi} in this device occurs at the 7th cycle from 18 V to 12 V with no corresponding change in the V_{pi}-V_{po} window, suggesting that both V_{pi} and V_{po} are affected and shifted in the same direction. This is reminiscent of the rearrangement of positive surface charges as observed previously in microscale suspended gate FETs[17] and further suggests that both V_{pi} and V_{po} in our NEMFET could be reduced using fixed charges while the average V_{pi}-V_{po} operating window of 0.83 V is already compatible with modern transistors of traditional design.

5.4.2 AC property

As mentioned in chapter 4, the resonant frequency is the important parameter which set the operational speed of device. For a suspended beam, the resonant frequency f_o can be expressed as $f_o = 1.03\ d\sqrt{E}\ /\ L^2\sqrt{\rho}$, by the Euler-Berlulli theory, where E is Young's modulus, ρ is the mass density, d is the thickness of the beam(in this case, the total diameter of suspended channel including gate oxide) in the direction of motion, and L is the length of the suspended beam. The single source method for detecting fo is explained in chapter 4 previously, I'll show the measurement result directly.

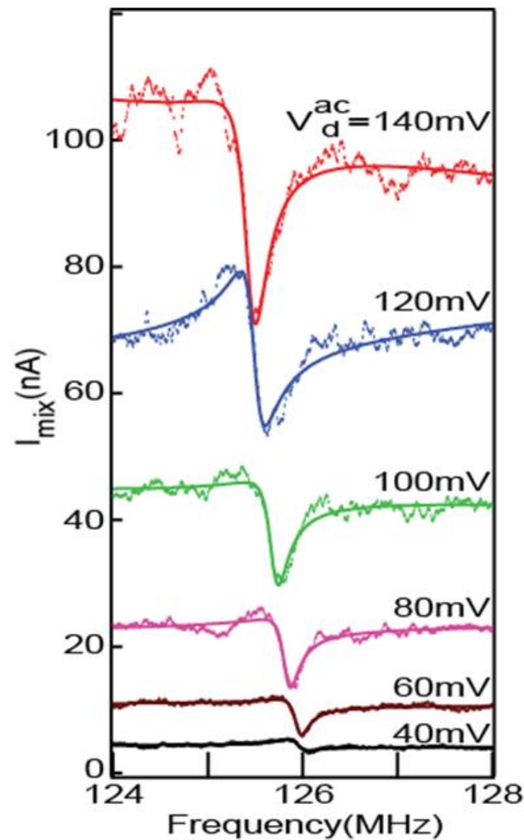

Fig 5.18: The plot of I_{mix} vs. drive frequency with various V_{ac}^{d} amplitude. The symbols are the measurement data, and the line is I_{mix} fitting.

Fig 5.18 is the plot of I_{mix} vs. drive frequency in different drive amplitude at V_g is held to 5V. The I_{mix} peak shows f_o is 125.9 MHz with drive amplitude 40*m*V, and the f_o decrease non-linearly with increase of drive amplitude (Fig 5.19). The measured point fits well with I_{mix} equation. The quality factor Q, which is defined as the ratio of the energy stored to the energy lost per cycle, of device is 632 with drive amplitude 40*m*V. Fig 5.x shows the typical non-linear increase of I_{peak} with increase of drive amplitude, and that means the resonance comes from true mechanical motion. Fig 5.20 is the shift of f_o with different V_d^{ac} and V_g. The increase of f_o with V_g is well-known elastic hardening effect of resonator which comes from the increased tension of suspended beam due to increase of

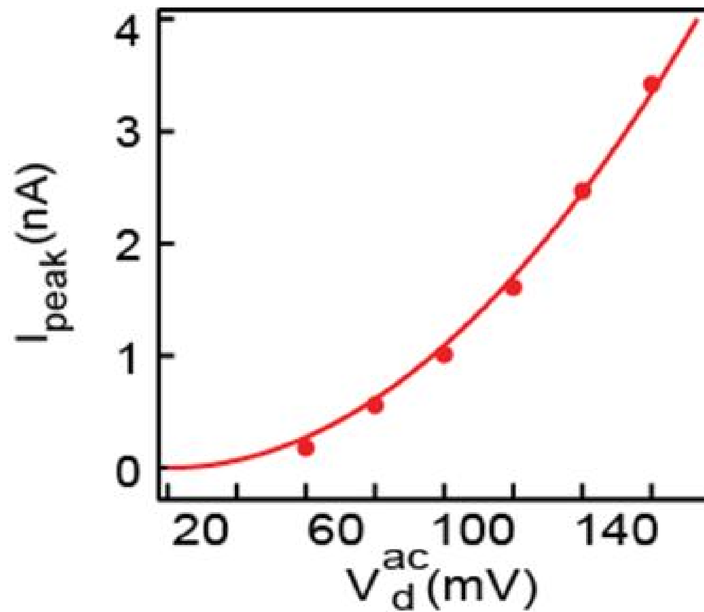

Fig 5.19: The plot of $V_{ac}{}^{d}$ amplitude vs. I_{peak}.

gate voltage[41, 44, 52, 53]. Different from f_o vs. V_g dependency, f_o is decreased with increase of V_d^{ac}. This behavior can be explained with the capacitive softening. C. C. Wu

et. al. demonstrated the capacitive softening effect on SWNT resonator with back gate and side gate scheme[52]. In case of side gate, the electrostatic force impedes in-plane vibration mode. In our NEMFET device, the AC drive from drain side is increased with constant V_g^{dc}, so the increase of V_d^{ac} acts like side gate. R. He et. al. showed another example of the softening effect with fixed V_g^{dc} condition[35].

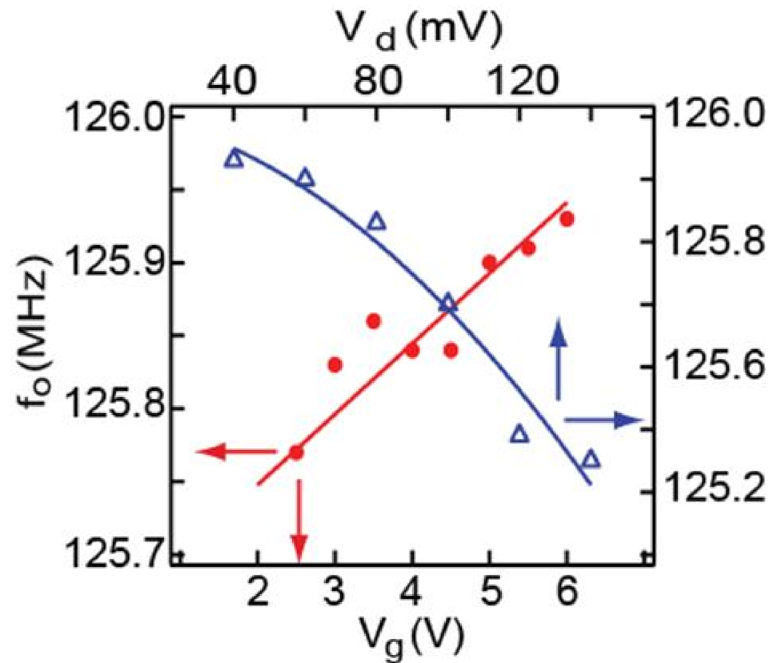

Fig 5.20: The plot of V_g vs. f_o and V_{ac}^d $vs.f_o$ of NEMFET device.

5.5 Conclusion

By combining semiconductor nanowire FET and high frequency nanowire NEMS resonators, the NEMFET is an exciting new device design that transcends previous NEMS switches and traditional FETs with finite subthreshold slope. The 3-terminal NEMFET eliminates the need for the gate electrode to contact the moving channel,

meaning both can be covered with protective oxide layers, greatly increasing the reliability and stability of NEMS devices. We already demonstrated less than 2 V V_{pi}-V_{po} operational voltage window with the potential to use fixed surface charges or work function differences to shift the V_{pi} values further towards zero. Looking forward, by leveraging the wealth of materials research in nanowire materials and more importantly, high strength, light weight carbon nanotubes and graphene-based materials, with further reduction of device dimensions to under 10 nm diameter and under 10 nm air gap, the NEMFET concept will open up a new avenue towards future reliable ultra-high-frequency, low-power computational systems with zero subthreshold slope and less than 1 V voltage that can operate in a wide range of ambient temperatures.

5.6 Acknowledgement

Chapter 5 is in part a reprint of “Three-Terminal Nano-electro-mechanical Field Effect Transistor with Abrupt Subthreshold Slope”, Submitted, *Nature*, 2013.

Chapter 6

Gate Modulated Thermoelectric Power Factor of Hole Gas in Ge-Si Core Shell Nanowires

6.1 Introduction

Thermoelectric power generation has attracted significant interest recently due to its promise in waste heat recovery and power generation[54]. There is a resurging effort to improve the energy conversion efficiency of thermoelectric devices, which is determined by its figure of merit ZT, defined as $S^2\sigma T/\kappa$, where S, σ, κ and T are thermopower(or Seebeck coefficient), electrical conductivity, thermal conductivity and absolute temperature, respectively[55]. The most common approach to improve the ZT is to suppress lattice component of the thermal conductivity (κ_L) by using complex and/or nano- structures[56] for enhanced phonon scattering. The numerator of the ZT formula, namely the power factor ($S^2\sigma$), has been more challenging to engineer, because S and σ are highly interdependent. As the carrier concentration is increased for higher σ, most commonly by chemical doping, S generally decreases. Moreover, chemical doping inevitably suppresses carrier mobility (μ) due to the increased ionized impurity scattering in the degenerate doping regime[57]. Even though it has been theoretically predicted that the power factor could be enhanced in low dimensional systems by carrier confinement effect in quantum wells[58] and quantum wires[59, 60], experimental observation of such enhancement has been very challenging. One of the difficulties in using nanostructures

for enhanced power factor lies in the surface charge states in small dimension nanostructures, which tend to suppress μ and σ via surface scattering.

6.2 Device Fabrication

To systematically investigate the power factor, it is necessary to study its dependence on carrier concentration. Field effect modulation provides a convenient means to facilitate such measurements on individual nanostructures to identify the optimized power factor, as has been shown previously on PbSe NWs[61] and Si nanoribbons[62] . Here, we report the first such experimental study on gate modulated electrical conductivity and thermopower of individual Ge-Si core shell NWs and the relationship between thermoelectric power factor and carrier concentration in core shell NWs. Unlike previously measured nanostructures, core shell NWs provide a unique situation in which the core contains high concentration of free holes by surface Fermi level pinning even without dopants[63, 64]. In addition, the surface charge scattering can also be significantly suppressed by the passivation of epitaxial shell. Therefore, it is expected that core shell NWs could serve as an excellent platform for investigating the thermoelectric-carrier concentration relationship of nanoscale interface electron/hole gas without the complication of ionized impurity, surface charge scatterings, as well as dopant segregation and non-uniformity that are usually encountered in highly doped NWs. In this study, we use rationally synthesized Ge-core Si-shell NWs as the material system to perform the gate modulation experiments. Single crystalline Ge-Si core shell NWs studied here were synthesized by a chemical vapor deposition (CVD) method within the framework of vapor liquid solid (VLS) growth, as described in detail in earlier works.

Briefly, colloidal Au nanoparticles of ~2-5*nm* diameter were deposited onto Si substrates as the growth catalysts and placed in a tube furnace. Intrinsic Ge NWs were grown first by flowing 10% GeH_4 in H_2 (30 standard cm^3 per min (sccm) at 300 torr and 280 ^oC for ~15*min*. Subsequently, the intrinsic Si shell was deposited within the same reactor immediately after the Ge core growth at 450°C for 5*min* by using SiH_4 (5 sccm) at 5 torr.

6.3 Device Property

Fig 6.1(a) shows the schematic illustration of the core-shell structure, while Fig 6.1(b) shows a representative high-resolution TEM (HRTEM) image of the Ge-Si core-shell NWs. As shown in the figures and based on extensive TEM observations, the Ge

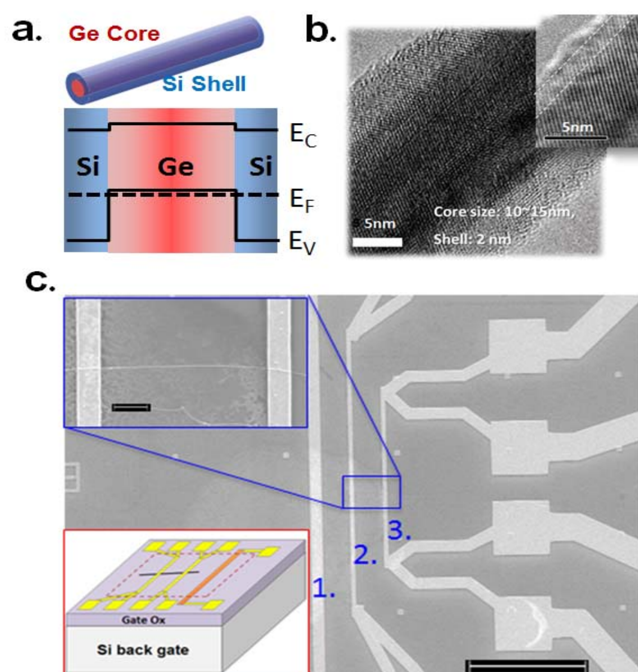

Fig 6.1: Core shell NW samples and devices. (a) Shematic structure and band diagram of CSNW, (b)HRTEM of CSNW, (c) SEM image of the device used for the gated electrical conductivity and thermopower measurements.

cores have diameters of 10-30*nm* while the Si shells are typically 1-3*nm* thick, and the Si-Ge interface is epitaxial with no dislocations[64]. The cross section of the wires are circular[65] . The NWs typically exhibit a layer of ~1 *nm* thick amorphous native SiO_2.

Fig 6.1(c) shows a SEM image of the device for the gated electrical conductivity and thermopower measurements. Electrode 1 is used as the heating element to create a temperature gradient along the NWs for the thermopower measurements. Electrodes 2 and 3 are used for 2-point I-V characterization as well as the voltage and temperature measurements. Doped Si substrates were used as the global gate electrode(bottom inset in Fig 6.1(c)). To fabricate the devices, Ge-Si core shell NWs were casted onto a Si substrate deposited with a thermal SiO_2 insulation layer(30 or 300 *nm* thick). NW devices in a back-gated configuration were fabricated using standard lithography techniques. 5/55/30 *nm* Ti/Ni/Au were patterned onto a NW by e-beam lithography, lift-off and thermal evaporation (top inset in Fig 6.1(c)). A brief(~1-5 seconds) buffered hydrofluride(BHF) dip was performed immediately prior to the metal evaporation to remove the native oxides on NWs. The devices were annealed at 350°C in a reforming gas (5% H_2 in N_2) for 30 seconds to improve the electrical contacts between the metal electrodes and the NWs. Table 1 lists the NW samples measured in this study. The overall diameters of each NW were measured by an atomic force microscope (AFM) in a taping mode. The Ge core diameters were estimated by subtracting the overall diameters with twice of the Si shell thickness (~ 4*nm*). The channel length, namely the distance between the two electrodes, is approximately 2*um* to ensure diffusive transport of the carriers. The gate oxide thickness is 30*nm* for NW1 and 300*nm* for NW 2&3. As shown in Fig 6.2(a), the I-V curves of the NW under various gate voltages are linear, suggesting

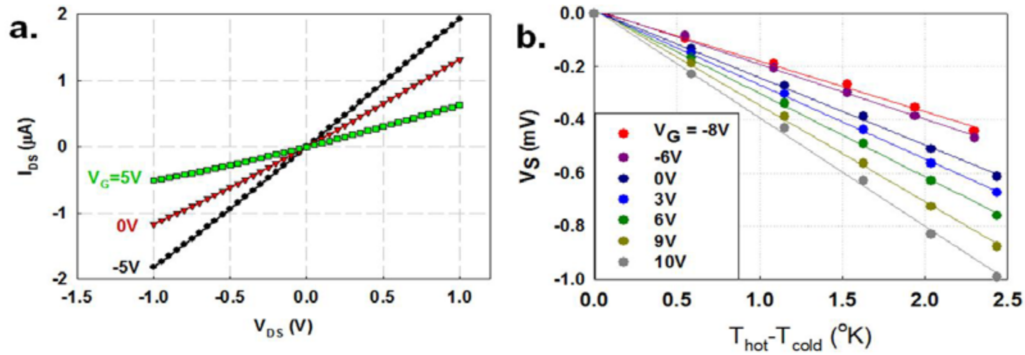

Fig 6.2: Gate modulated electrical and thermopower measurements of the NWs. (a) V_d-I_d plot, (b) Seebeck voltage V_S vs. temperature difference between electrodes 2 & 3 under various gate voltages.

Ohmic contacts formed between the semiconductor NWs and the metal electrodes due to the highly conducting nature of the NWs. It also shows that the conductance of the NWs decreases at the gate voltage increases, indicating a p-type behavior as expected for such Ge-Si core shell NWs [64].

For thermopower measurement, electrode 1 is used as the heating element to create a temperature difference ΔT and a Seebeck voltage ΔV at the two ends of a NW, both are measured by the electrodes 2 and 3 to obtain the Seebeck coefficient,

$$S = -\frac{\mathrm{dV_s}}{\mathrm{d}\Delta T} \ . \qquad (6.1)$$

The temperature difference from electrode 2 to 3 was obtained by measuring the four-point resistance changes of the electrodes . The temperature coefficient of resistance (TCR) of each resistive thermometer probe is calibrated during the. In the experiments, the heater power is gradually increased from 0 to approximately 0.2 Watt such that the temperature difference increases from 0 to ~2°K, as shown in Fig 6.2(b). It is worth

noting that the high thermal conductivity of the metal electrodes 2 & 3 ensures a uniform temperature distribution underneath them, as demonstrated by the finite element thermal modeling. Therefore, the temperature measured by each of the electrodes represents the appropriate temperature entered into Equation 6.1 to determine the Seebeck coefficient. Fig 6.2(b) shows the measured V_s vs. ΔT under various gate voltages. It shows that the slope of V_s vs. ΔT, hence the S, increases as the gate voltage increases, as a result of p-type behavior.

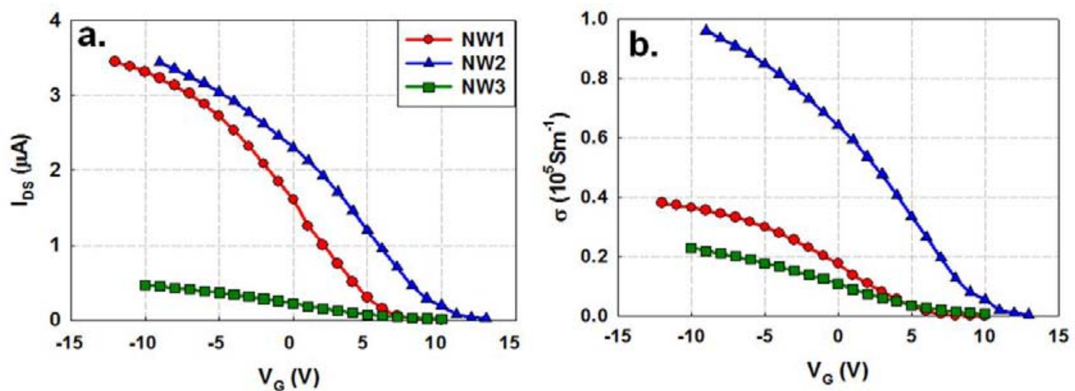

Fig 6.3: (a) Source drain current and (b) electrical conductivity of the NWs as a f unction of gate voltage.

We first discuss the gate modulated electrical transport in the core shell NWs. Fig 6.3(a) shows V_g-I_d curve for the three NW samples. The data were collected with source-drain voltage V_{ds} = 1 V. As expected, all the NWs show increased I_{ds} as V_g decreases, as a result of the p-type behavior and hole transport. The threshold voltages (V_{th}) for NW 1-3 are 7, 11 and 10 V, respectively. At V_g=0, there is still a large current, indicating that free holes are accumulated in the dopant-free Ge cores. The large hole concentration is induced by the surface Fermi level pinning, as observed previously in similar Ge-Si core

shell NWs[63, 64]. As shown in the energy diagram of the core-shell heterostructures (Fig 6.1(a)), due to the offset between the valence band edges (E_v) of Si and Ge (~0.3-0.4eV), the Fermi level (E_f) lies somewhere close to E_v of Ge, inducing a highly concentration 'hole gas' in the Ge cores[64]. This resembles the two-dimensional electron gas (2DEG) in planar heterostructures[66]. As the V_G shifts to higher voltage (+10-15 V), the E_f is shifted up, positioning above the E_v in the Ge core and turning off the NWs (Fig 6.3(a)) when $V_g>V_{th}$. On the other hand, as the gate voltage decreases to negative values, the E_F continues shifting down, injecting more carriers into the Ge core and creating higher current (Fig 6.3(a)). Fig 6.3(b) shows the electrical conductivity of the NWs, calculated from $\sigma = \frac{LI_{DS}}{AV_{DS}}$ where A is the cross-sectional area of the Ge cores. The observed σ's are in the range of 10^4-10^5 S.m^{-1} depending on the NW diameter and gate voltage, which are very high for NWs with such small diameters.

To investigate the origin of the high conductivity in the NWs, we estimated the hole mobility and concentration. From the I_{DS}-V_G data shown in Fig. 3a, we can calculate the transconductance of the NWs as,

$$g_m = \frac{dI_{DS}}{dV_G} \tag{6.2}$$

and the hole mobility as,

$$\mu = \frac{g_m L^2}{V_{DS} C} \tag{6.3}$$

where L is the NW length and C the capacitance of the gate oxide, calculated from,

$$C = \frac{2\pi\varepsilon_0\varepsilon_r}{\cosh^{-1}((R+h)/R)} \tag{6.4}$$

where h is the gate oxide thickness, R is the NW radius, ε_0 is the permittivity of the vacuum, and ε_r is the relative dielectric constant of the gate oxide. A value of 2.2 for ε_r has been shown to fit very well with the Finite element analysis of the gate oxide capacitance. From the calculated mobility, one can also estimate the carrier concentration in the NWs from

$$n = \sigma/\mu e \tag{6.5}$$

where e is the charge per electron.

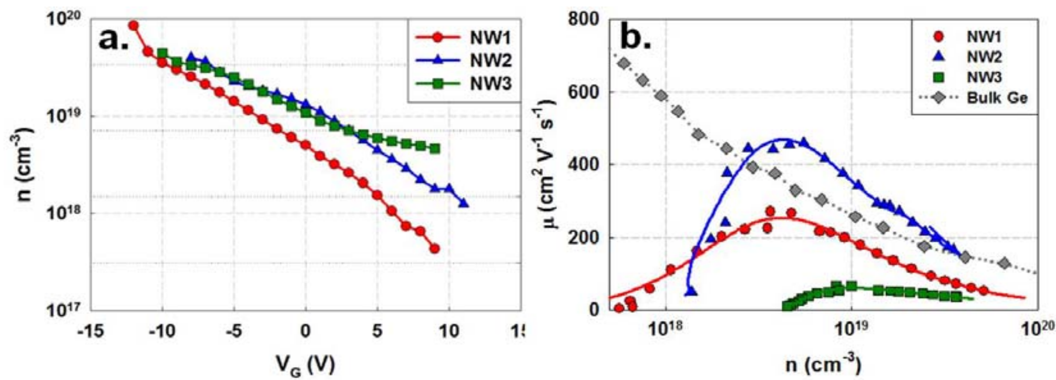

Fig 6.4: Gate modulated hole concentration and mobility of the NWs. (a) Hole con centration as a function of gate voltage, (b) Mobility vs. hole concentration of the NWs along with p-type Ge (from Ref. [67]).

Figure 6.4(a) shows the hole concentration n in Ge core as the gate voltage varies. The calculated n falls in the range of ~10^{18} to 5×10^{19} cm^{-3} for NW 2 & 3, and within 5×10^{17} to 10^{20} cm^{-3} for NW1 because of the thinner gate oxide thickness. This shows that surface Fermi level pinning and the gate modulation can be utilized to achieve a very high doping concentration into the degenerate regime in a nominally 'dopant –free' NW.

This can only be achieved in the small diameter core shell NWs such as the ones studied here (≤ 25 nm), because of the comparable screening depth of the field effect (in the range of 10-20 nm).

Fig 6.4(b) plots the mobility as a function of hole concentration for the NWs. For NW 1 and 2, μ varies with *n* and peaks at (4-5)×10^{18} cm^{-3} and for NW 3 at (4-5)×10^{18} cm^{-3}. At higher *n*, μ decreases with increasing *n*, suggesting that the acoustic phonon scattering is significant. In the acoustic phonon scattering regime, μ can be written as $\mu \propto E^{-\frac{1}{2}}$ where E is the carrier energy and is larger for higher hole concentration [57]. The mobility is lower in the thinnest nanowire (NW 3) compared to the thicker ones (NW 1 & 2), suggesting that the surface scattering becomes significant when the diameter is small. One the other hand, the decrease in mobility from NW 2 to NW1 is presumably due to the variation in defect concentration in the NWs, which could have been unintentionally induced during the NW growth. Nevertheless, if we compare the mobility of the NWs with bulk Ge (Fig 6.4(b)), we find that the mobility of NW2 is considerably higher than that of bulk Ge. The high mobility is a result of the two important attributes of the core shell NWs as we discussed previously: first, the NWs are nominally dopant-free such that the impurity scattering is suppressed; second, the passivation of the Ge core by the Si shell significantly decreases the surface charge density and hence weakens the surface scattering. The lower mobility in NW 1 and 3 suggests that further optimization of the NW quality and surface passivation will be needed in order to more consistently achieve higher mobility in the core shell NWs.

To further illustrate the relative roles of phonon scattering and impurity scattering, we measured the temperature dependent mobility of the NWs and compare it with p-type

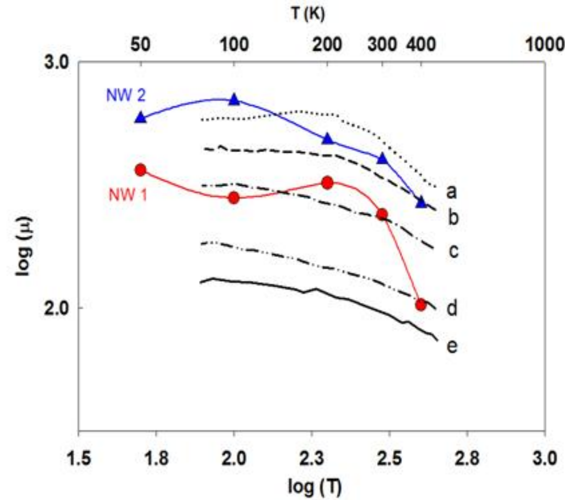

Fig 6.5: Temperature dependent mobility of the NWs and bulk p-Ge. The bulk Ge data are adapted from Ref. [67] with the following dopant (Gallium)concentrations: (a)1.1×10^{18}cm^{-3}, (b)4.9×10^{18}cm^{-3}, (c)1.2×10^{19}cm^{-3}, (d) 5.8×10^{19}cm^{-3}, (e)1×10^{20}cm^{-3}.

bulk Ge [67, 68], as shown in Fig 6.5 (data for NW 3 is not shown because its low temperature data was not available). The NW mobility is obtained from the linear I_{DS}-V_G regime at each temperature. For bulk Ge, the mobility increases as the dopant concentration decreases and it generally decreases with temperature because of the acoustic phonon scattering. For the NWs studied here, the absolute values as well as the temperature dependence of μ are similar to that of bulk Ge with dopant impurity concentrations ranging from 1.1 to 4.9×10^{18} cm^{-3} for NW2 and from 5.8×10^{19} to 1×10^{20} cm^{-3} for NW1, clearly showing that the *effective* impurity that contributes to carrier scattering is lower (higher) than the free-hole concentration in NW2 (1), consistent with our hypothesis discussed above.

Now we turn our discussion to the gate modulated thermopower in the core shell NWs. As shown in Fig 6.2(b), thermoelectric voltage is linearly related to the measured

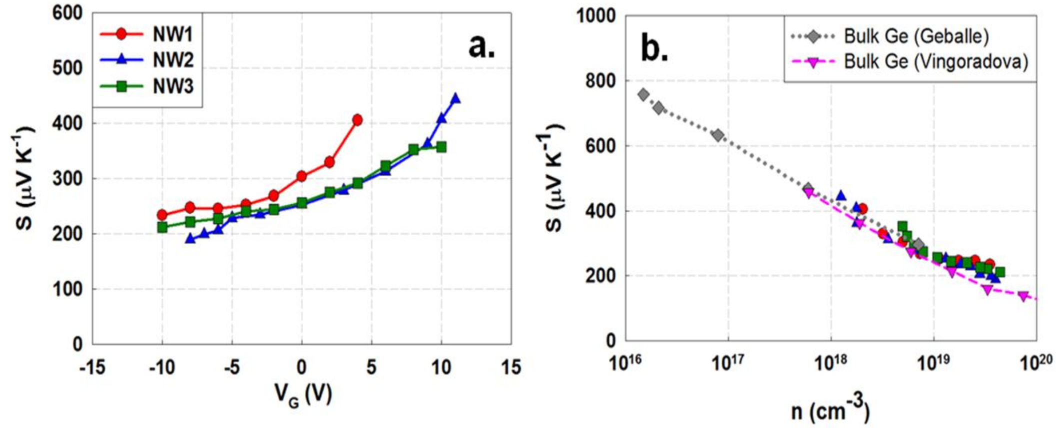

Fig 6.6: Gate modulated thermopower of Ge-Si core shell NWs. (a)Seebeck coefficient of the NWs under various gate voltages. (b)Seebeck coefficient as a function of hole concentration of the NWs and bulk p-Ge(bulk data adapted from Geballe et al. [69] and Vinogradova et al. [70])

temperature difference between the two electrodes (2 and 3) under various gate voltages. We have also checked the leakage current between the gate electrode (Si substrate) and the NWs, and found that it is negligible. The measured *S* under various gate voltages is shown in Fig 6.6(a). The measured positive values of the *S* show that holes are the majority carriers (Note: *S* is defined as $-\frac{dV_S}{d\Delta T}$), consistent with the I_{DS}-V_G measurements Besides, *S* increases as V_G is raised to more positive values, also consistent with the *p*-type characteristics of the NWs. For the NWs studied here, the *S* can be modulated within a range of 200 to ~ 450V/K by changing the gate voltage.

The gate modulation provides an effective means to investigate the relationship between *S* and carrier concentration within a range of ~10^{18} to ~5×10^{19} cm^{-3}. As shown in Fig. 6(b), *S* decreases monotonically as *n* increases, as expected. More interestingly, *S* vs. *n* plots of the NWs fall into the same curve as that of p-type bulk Ge [69, 70], suggesting that *S* in the NWs, even with diameters down to ~11 nm, does not differ

significantly from that in a bulk system, even though the mobility in the NWs behaves quite differently.

The similarity of the thermopower between the Ge NWs and bulk Ge suggests that the electronic structures in the NWs are still bulk-like and the quantum confinement effect is not significant. As studied in detailed by Liang *et al.* [71], the sub-band energy separation is only a few meV for a 15 nm Ge NW, much smaller than $k_B T$ (~ 26 meV) at 300 K. The diameter of Ge NWs has to be smaller than 5 nm in order to see pronounced quantum confinement effect [71]. Therefore, we don't expect quantum confinement effect plays a big role in the observed Seebeck coefficient.

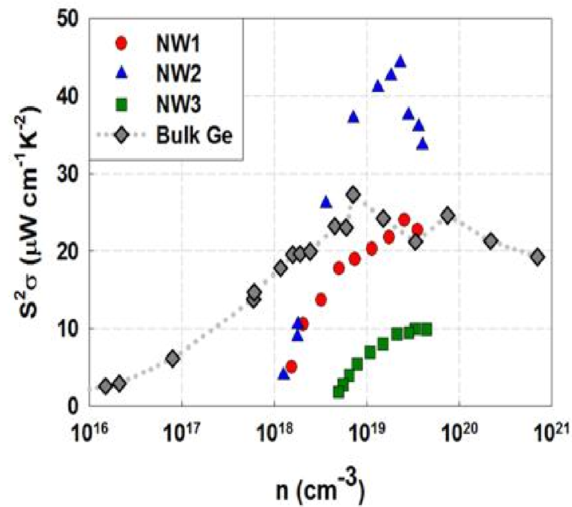

Fig 6.7: Power factor ($S^2\sigma$) vs. carrier concentration of the NWs and bulk p-Ge.

Finally, we present the power factor ($S^2\sigma$) vs. carrier concentration in the Ge/Si core shell NWs and compare them with bulk Ge, as shown in Fig 6.7. Similar to bulk Ge, there exists an optimal carrier concentration for the peak power factor, for NWs. The optimal concentration lies within (2-4) $\times 10^{19}$ cm^{-3} . The peak value(s) of the power

factor is the highest for NW 2 ($44W.cm^{-1}.K^{-2}$), and are similar between NW 1($24W.cm^{-1}.K^{-2}$) and bulk Ge ($27W.cm^{-1}.K^{-2}$), and finally is the lowest in NW 1 ($10W.cm^{-1}.K^{-2}$). It can also be seen that the power factor correlates clearly with the mobility (Fig. 6.4(b)). This can be readily understood from the formula for S and σ, as the former depends on the n (and slightly on scattering mechanism [57]) and the latter depends on both n and . At the same n, higher leads to higher power factor. In particular, for NW 2, the peak power factor is increased by more than 60% over that of p-type bulk Ge, suggesting the great promise of exploiting the high carrier mobility of interface hole gas in core-shell heterostructure NWs to enhance the power factor. Previously, similar approach has been explored by using modulation-doped nano-composites of Si-Ge alloys, which showed improved power factor via increased carrier mobility[72, 73]. Our present study, however, represents the 'extreme' of what the modulation doping can achieve, namely, strongly degenerate hole gas in nominally 'dopant-free' Ge NWs. As a result, the relative enhancement ratio as well as the absolute value of the power factor for NW2 is considerably higher in our case.

6.4 Conclusion

In conclusion, we presented the first gated thermoelectric power factor measurement on single Ge/Si core shell NWs with Ge core diameters ranging from 11-25 nm. It was found that surface Fermi level pinning introduces high concentration interface hole gas in the dopant-free Ge core and the field effect further increases the concentration into the strong degenerate regime. As a result, the gate modulated core shell NWs offer an excellent and convenient platform to probe the relationship between the thermoelectric

power factor and carrier concentration. Absolute values as well as the temperature dependence of carrier mobility of the NWs were compared with bulk Ge, and it was revealed that the suppressed ionized impurity and surface charge scattering could lead to higher mobility. The dependence of the Seebeck coefficient on the carrier concentration of the NW samples studied here still follows the bulk Ge behavior, indicating that the electronic structures are still bulk-like and the quantum confinement effect is not significant in the diameter range studied here. The results also suggest that core shell heterostructures coupled with field effect could be an effective way to enhance the thermoelectric power factor, a new mechanism to improve the thermoelectric figure of merit in NWs in addition to the existing phonon boundary scattering approach. Further optimization of the NW quality and better control of surface passivation will likely lead to higher mobility and power factor.

6.4 Acknowledgement

Chapter 6 is a reprint of "Gate-Modulated Thermoelectric Power Factor of Hole Gas In Ge-Si Core-Shell Nanowires", *Nano letters,* vol.13, pp.1196-1202, 2012.

Chapter 7

Conclusion

Power consumption comes to the one of the most important concern in COMS technology nowadays. With shrinkage of device dimension, the dynamic power was scaled down effectively. But, the static power can't be scaled down due to I_{off} can't be decreased with dimension with its thermodynamic limitation (kT/q). To breakthrough this, we design NEMFET with suspended i-Ge/Si core/shell nanowire channel, which combine the abrupt switching property of NEMS with excellent electrical property of i-CSNW.

Before starting to make a real device, I showed the simulation results using Sentaurus combined with COMSOL. The results shows NEMFET using suspended NW channel can operate at >300MHz with V_{pi}<5V.

In chapter 3, I demonstrated NEM switch with suspended NW channel. The switch shows abrupt increase of I_g at V_{pi}=4.7V, which fits very well with analytically calculated value. We've made it certain that suspended channel scheme works, and the measurement results fits well with calculation data.

In chapter 4, we demonstrate the back gate NEMFET with suspended i-Ge/Si core/shell wire channel with V_{pi}=10.8V, V_{po}=6.5V with SS=15mV/dec successfully. The back gate structure is simple and short process time, but has the limitation due to large gate leakage current path, the difficulty in decreasing final air gap thickness, and I_{on} mismatch before and after pull-in, etc. To solve this problem, we designed and fabricated the local metal gate NEMFET combined with passivation and selectable electrode

scheme. These solutions can improve *SS* value itself and terminate parasitic current and gate leakage current successfully.

Finally, we can realize multiple switching NEMFET demonstrates close-to-zero SS (<6mV) at room. Furthermore, we employed electrostatic actuation to study the AC mechanical response of the nanowire channel. Although a high voltage of 10~16V is needed for the device to pull in, significantly the window between V_{pi} and V_{po} is shown to be less than 2V. Our current NEMFET devices can operate at 125.9 MHz and with further reduction in nanowire dimensions and optimization of process and materials, we expect our NEMFET design window to extend well beyond very-high-frequency (VHF) operation with less than 1V pull-in voltage and NEMFET will be a promising candidates for future low-power computational systems.

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