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# Low-Temperature UV-Assisted Fabrication of Metal Oxide Thin Film Transistor

A thesis submitted in partial satisfaction

of the requirements for the degree Master of Science

in Materials Science and Engineering

by

Shuanglin Zhu

2017

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2017

ABSTRACT OF THE THESIS

Low-Temperature UV-Assisted Fabrication of Metal Oxide Thin Film Transistor

by

Shuanglin Zhu

Master of Science in Materials Science and Engineering

University of California, Los Angeles, 2017

Professor Yang Yang, Chair

Solution processed metal oxide semiconductors have attracted intensive attention in the last several decades and have emerged as a promising candidate for the application of thin film transistor (TFT) due to their nature of transparency, flexibility, high mobility, simple processing technique and potential low manufacturing cost. However, metal oxide thin film fabricated by solution process usually requires a high temperature (over 300 °C), which is above the glass transition temperature of some conventional polymer substrates. In order to fabricate the flexible electronic device on polymer substrates, it is necessary to find a facile approach to lower the fabrication temperature and minimize defects in metal oxide thin film. In this thesis, the electrical properties dependency on temperature is discussed and an UV-assisted annealing method incorporating Deep ultraviolet (DUV)-decomposable additives is demonstrated, which can effectively improve electrical properties solution processed metal oxide semiconductors

processed at temperature as low as 220 °C. By studying a widely used indium oxide ($In_2O_3$) TFT as a model system, it is worth noted that compared with the sample without UV treatment, the linear mobility and saturation mobility of UV-annealing sample are improved by 56% and 40% respectively. Meanwhile, the subthreshold swing is decreased by 32%, indicating UV-treated device could turn on and off more efficiently. In addition to pure $In_2O_3$ film, the similar phenomena have also been observed in indium oxide based Indium-Gallium-Zinc Oxide (IGZO) system. These finding presented in this thesis suggest that the UV assisted annealing process open a new route to fabricate high performance metal oxide semiconductors under low temperatures.

The thesis of Shuanglin Zhu is approved.

Ximin He

Jenn-Ming Yang

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University of California, Los Angeles

2017

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# List of Abbreviations

| | |
|---|---|
| **2-ME** | 2-methoxyethanol |
| **AcAc** | Acetylacetone |
| **AFM** | Atomic Force Microscope |
| **ALD** | Atomic Layer Deposition |
| **AMLCD** | Active Matrix Liquid Crystal Display |
| **AMOLED** | Active Matrix Organic Light Emitting Diodes |
| **AOS** | Amorphous Oxide Semiconductor |
| **a-Si** | Amorphous Si |
| **CBM** | Conduction Band Minimum |
| **CBT** | Conduction Band Tail |
| **DFT** | Density Function Theory |
| **DOS** | Density of States |
| **DUV** | Deep Ultraviolet |
| **EA** | Electron Affinity |
| **GIWAXS** | Grazing Incident Wide-Angle X-ray Scattering |
| $I_{ds}$ | Drain-Source Current |
| **IGO** | Indium-Gallium Oxide |
| **IGZO** | Indium-Gallium-Zinc Oxide |
| **IPA** | Isopropanol |

| | |
|---|---|
| **IZO** | Indium-Zinc Oxide |
| **LCD** | Liquid Crystal Display |
| **LTPS** | Low-Temperature Poly-Silicon |
| **MOSFET** | Metal Oxide Field-Effect Transistors |
| **PBS** | Positive Bias Stress |
| **PPC** | Persistent Photoconductivity |
| **S.S** | Sub-threshold Voltage Swing |
| **SPM** | Scanning Probe Microscope |
| **SSE** | Solid-State Energy |
| **TFT** | Thin Film Transistor |
| **VBM** | Valence Band Maximum |
| **VBT** | Valence Band Tail |
| $V_{ds}$ | Drain-Source Voltage |
| $V_{gs}$ | Gate-Source Voltage |
| $V_{o}$ | Oxygen Vacancy |
| $V_{on}$ | Turn on Voltage |
| **ZGO** | Zinc-Gallium Oxide |
| **ZTO** | Zinc-Tin Oxide |

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# 1. Introduction

## 1.1 Motivation

In the last decade, there has been considerable development in the area of oxide semiconductors, owing to their superior electrical properties as compared to hydrogenated amorphous silicon (a-Si:H), lower cost and better uniformity over large areas as compared to polymer crystalline silicon (poly-Si). Amorphous metal oxide semiconductors (AOSs) have shown good electrical properties due to their unique electron configuration. Electron transport in AOSs is insensitive to structure distortion and thus can be a promising candidate for flexible electronic devices. Compared to vacuum-processed thin film transistor (TFT) devices, solution-processed TFTs can potentially enable low-cost mass production but also require higher processing temperature (up to 350°C) because there are more defects and trapped charges introduced in solution based film deposition step. The high temperature is fatal for some conventional flexible polymer substrates with a low glass transition temperature. Also, it is difficult to control the carrier concentration in the bulk of film when the annealing temperature is high. High carrier concentration and high conductivity results in a negative turn on voltage ($V_{on}$) and high off current for n type TFT devices. The low temperature process of metal oxide semiconductor is necessary for the flexible electronic device. However, low-temperature processed TFTs exhibit low electron mobility and high hysteresis as well as sub-threshold voltage swing since there is insufficient thermal energy to overcome the energy barrier for lattice rearrangement. An UV-activation annealing approach has been developed to ensure a low-temperature process and achieve mobility as high as 7 $cm^2/V \cdot s$.[37] However, this method did not include a temperature control and monitoring component, resulting in less reproducibility. Meanwhile, this method is only compatible with $Al_2O_3$ gate dielectric layer deposited by atomic layer deposition (ALD), which is rather

expensive and has low throughput. Thus it is worthwhile to developing a low-temperature approach that is compatible to low-cost gate dielectric material while maintaining high electron mobility and good transfer characteristics.

## 1.2 Objective

The aim of this work is to understand the effect of annealing temperature on device performance and based on this knowledge to lower the processing temperature of metal oxide thin film semiconductors while maintaining high mobility, small hysteresis and sub-threshold voltage swing. A novel UV-assisted annealing method was developed for this purpose. The proper mechanisms are proposed and the function of additives was discussed.

# 2. Background

## 2.1 Thin-Film Transistor Principles

The first TFT was a microcrystalline cadmium sulfide (CdS) n-type TFT, with silicon monoxide gate dielectric, and Au electrodes on a glass substrate, developed by Weimer at RCA Labs in 1962 using vacuum based evaporation and shadow masking.[1] Two years later the first oxide TFT, a tin oxide ($SnO_2$) TFT was fabricated using photolithographic techniques. Oxide TFTs would garner attention again in 1996 as potential ferroelectric memory TFTs. Prins et al. demonstrated the first transparent oxide TFT in an antimony-doped tin oxide ($SnO_2$:Sb), deposited via pulsed layer deposition.[2] Sager et al. demonstrated the first indium oxide ($In_2O_3$).[3] In 2003, oxide TFT gained interest again, mostly in zinc oxide (ZnO) TFTs, which would yield electron mobilities greater than 1 $cm^2$ $V^{-1}$ $s^{-1}$; a potential replacement for the a-Si employed in TFT display backplanes. Hoffman, Norris, and Wager produced a transparent ZnO TFT with 2.5 $cm^2$ $V^{-1}$ $s^{-1}$ mobility and an on/off ratio of $10^7$. [4]A breakthrough occurred in 2003 when Nomura et al. developed an indium gallium zinc oxide (IGZO) mono-crystalline active layer, a TFT that presented an electron mobility of 80 $cm^2$ $V^{-1}$ $s^{-1}$ and on/off ratio of $10^6$. [5] This high-performance TFT validated the use of metal oxide semiconductors and demonstrated their potentials.

The TFT relies on modulation of a current that flows between source and drain through the gate electrode; the gate electrode affects or modulates, current flow through capacitive injection of carriers close to the dielectric/semiconductor interface to produce the field effect.

The device structure of amorphous oxide semiconductor TFTs is as follows: a semiconducting channel layer lies between the source and drain electrodes while a dielectric is deposited in

between the semiconductor and gate layer, either from the top or bottom, depending on if the device is a top-gated or bottom-gated device. In addition, the device can either be top or bottom contact, depending on electrode placement. At the bottom of the device is the substrate on which everything is laid. A diagram of a typical TFT structure and its working principle can be seen in Fig. 2.1a. For an n-type enhancement mode TFT, by grounding the source terminal ($V_S = 0$ V) and applying a positive voltage to the gate ($V_G > 0$ V), charge carriers will start accumulating at the semiconductor/dielectric interface. A positive drain bias ($V_D > 0$ V) will make the carrier flow from source to drain. There are four typical configurations for a TFT as shown in Fig. 2.1b, each with different advantages and disadvantages.[6] For a-Si:H TFT's, the staggered bottom-gate configuration was widely used in order to counter light sensitivity that the semiconductor layer would experience from a liquid crystal display (LCD) backlight. In contrast, poly-Si TFTs utilized a coplanar top gate structure due to its need for a high processing temperature and flat continuous film.[7] Bottom-gate devices fail to protect the semiconductor surface from the air but they can be used to easily modify the semiconductor surface's properties[8] For oxide TFT, different architectures are adapted for different applications and no one has overwhelming advantage so far.

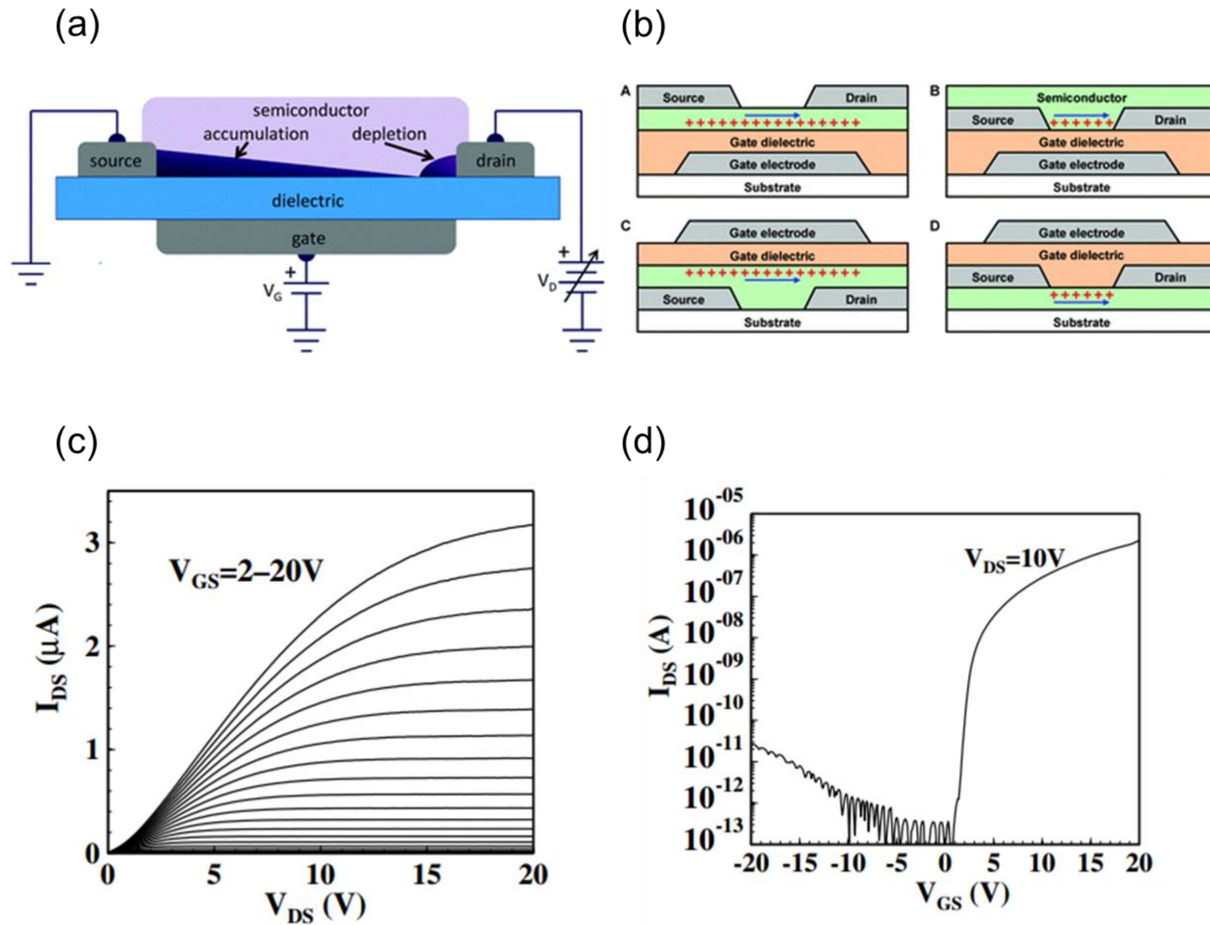


**Figure 2.1: (a) Schematic of a thin-film transistor.[9] (b) Schematic cross-sections of the four principle thin-film transistor structures. The carrier channel is schematically shown in red. A: Bottom-gate (inverted) staggered TFT; B: Bottom gate (inverted) coplanar TFT; C: Top-gate staggered TFT; D: Top-gate coplanar TFT.[10] (c) Output and (d) transfer curves for a-Si TFT with channel width and length of 28 and 6 µm, respectively.[11]**

Different types of materials can also be used for the semiconductor layer. The two types of materials examined here are silicon and metal oxide. Silicon can be further classified as amorphous silicon or polysilicon, distinguished by the grain size. Amorphous silicon consists of a network of covalently bonded silicon atoms, with each silicon having four neighboring atoms with various bond lengths and angles. Amorphous silicon is non-periodic and does not exhibit long-range order or crystallinity. This gives rise to good uniformity but a low electron mobility. The typical grain sizes for amorphous silicon are on the order of 1 nm.[7] Polysilicon can be

obtained from amorphous silicon using techniques such as laser crystallization. Polysilicon has grain sizes on the order of 1 micrometer. The increased grain size gives rise to a higher carrier mobility, ranging from 50 to 100 cm$^2$ V$^{-1}$ s$^{-1}$ [7]. However, due to the grain boundaries inherent in polysilicon, uniformity is much lower than that of amorphous silicon. Amorphous oxide semiconductor (AOS), on the other hand, combines both the advantages of amorphous and polysilicon, achieving a high mobility and good uniformity. A comparison of each material for the semiconductor layer is shown in Table 2.1.

$$I_D = \frac{1}{2}(\mu_n C_i)\left(\frac{W}{L}\right)\left[2(V_G - V_T)V_D - V_D{}^2\right], 0 \leq V_D \leq V_G - V_T \quad (2.1)$$

$$I_D = \frac{1}{2}(\mu_n C_i)\left(\frac{W}{L}\right)(V_G - V_T)^2, V_D > V_G - V_T \quad (2.3)$$

**Table 2.1: Comparison of various characteristics for different channel materials in thin film transistors.**

| **Material** | **Amorphous Si** | **Low-Temperature Poly-Si** | **Metal Oxide Semiconductor** |
|---|---|---|---|
| Carrier Mobility | <1 cm$^2$/Vs | 50-100 cm$^2$/Vs | 10-100 cm$^2$/Vs |
| Sub-threshold Swing | 0.4-0.5 V/dec | 0.2-0.3 V/dec | 0.09-0.6 V/dec |
| Leakage Current | ~10$^{-12}$ A | ~10$^{-12}$ A | ~10$^{-13}$ A |
| Uniformity | Good | Poor | Good |
| Number of Masks | 4-5 | 5-9 | 4-5 |
| Manufacturing Cost | Low | High | Low |
| Process Temperature | ~250 °C | ~250 °C | RT to ~350 °C |

Like conventional metal-oxide-semiconductor field-effect transistor (MOSFET), the I-V characteristics of a thin film transistor can be described by the above equations where μ is the field effect mobility ($cm^2$ $V^{-1}$ $s^{-1}$), C is the capacitance per unit area of the insulator layer (F $cm^{-2}$), threshold voltage ($V_T$) is the threshold voltage, $V_G$ is the gate voltage, $V_D$ is the drain voltage, and channel width (*W*) and length (*L*) are the channel width and length respectively.[7]With sufficiently large $V_G$, the channel becomes conductive and the current in the channel increases with increasing $V_D$. The current increases linearly with $V_D$ until the channel cannot support more current as described by (2.1). At this point, the channel is said to be saturated and a corresponding saturation region where the current levels off can be observed and described by (2.2). The saturation current can be increased by increasing $V_G$, which allow for more carriers to be accumulated at the semiconductor-insulator interface.[7] This type of $I_D$-$V_D$ plot shown in Fig. 2.1c is typically known as an output curve. Fig. 2.1d is a plot of $I_D$ versus $V_G$, typically called the transfer curve. As can be seen, the drain current remains quite low until the gate voltage reaches a certain value upon which the drain current increases rapidly and eventually levels off. This critical value of the gate voltage is known as the threshold voltage, $V_T$.

Major electrical characteristics of TFT devices are field effect mobility, threshold voltage, and subthreshold swing. These parameters vary depending on factors such as device structure, fabrication process, amorphous oxide semiconductor material, and the interface between semiconductor and gate dielectric. Ideal electrical characteristics for TFT's are high mobility, near zero threshold voltage and small subthreshold swing. Each of these characteristics is further examined in detail below.

Carrier mobility is a parameter that describes the efficiency of charge carrier transport in a material, affecting the maximum drain current of a device. Commonly, the intrinsic mobility of a

bulk material is obtained by extracting the Hall-effect mobility. However, TFT mobility is different from the intrinsic bulk mobility of its semiconductor, due to the narrow thin film channel through which charge transfer can occur. In addition, scattering from dielectric charges, interface states, and surface roughness affects the mobility.[12] Several mobilities can be extracted from TFTs: effective mobility, field effect mobility, and saturation mobility. The most commonly used mobility is the field-effect mobility.

Threshold voltage corresponds to the gate voltage at which a conductive channel is formed at the dielectric/semiconductor interface.[13] The most common method for determining the threshold voltage is done by linear extrapolation of the $I_D$-$V_G$ linear regime plot. The threshold voltage plays a significant role in device operation as the desired value of threshold voltage will be close to the voltage at which the device can operate. For n-type TFTs, if the threshold voltage is positive, the device is in enhancement mode and if it is negative, the device is in depletion mode. The opposite applies for p-type TFTs. Enhancement mode is desirable as no voltage is required to turn off the transistor, making circuit design easier and minimizing power dissipation. The concept of the threshold voltage is to determine the gate voltage necessary to fully turn-off the transistor.[14]

The on/off ratio is calculated by dividing the maximum drain current by the minimum drain current.[13] The minimum drain current is generally given by the noise level of the measurement equipment or the gate leakage current, while the maximum drain current depends on the semiconductor material and the effectiveness of capacitive injection by the field-effect.[15] For TFTs large values are required for successful usage as electronic switches, generally with values higher than $10^6$.

Subthreshold swing measures how efficiently a TFT turns on and off, directly related to the interface of the dielectric/semiconductor and its quality.[13] It is defined as the inverse of the max slope of the $I_D$-$V_G$ plot, indicating the gate voltage needed to increase drain current by one decade. Low subthreshold swing is characterized as less than 100 mV $dec^{-1}$ and is ideal for reducing device power consumption and operating voltage.[16]

Another property of transistor worth paying attention to is hysteresis. Hysteresis appears as a difference in $I_D$ values observed between forward and backward scan of $V_G$. It may affect device stability, which represents the reproducibility of current-voltage behavior.[17] Extracted TFT parameters could be contaminated by hysteresis effects thus it should always be avoided in transistor devices.

## 2.2 Metal Oxide Semiconductors

AOS TFTs are highly sought after for their switching elements for large areas, ultra-high definition, and fast frame rate. They are valuable especially in display technology, where TFTs act as switches to turn pixels on and off. They can replace a-Si technology in active matrix liquid crystal displays (AMLCD) as well as replacing low-temperature poly-silicon (LTPS) used in active matrix organic light emitting diodes (AMOLED) displays. Previous thin film transistor technology centered on amorphous Si (a-Si). Although a-Si semiconductors exhibited lower carrier mobilities than TFT's based on polycrystalline silicon, they were sufficient for serving as switching elements in LCD technology while providing better uniformity and reproducibility across large areas at a lower cost. However, due to their low mobility, a-Si was limited in its application to AMOLED. Amorphous oxide semiconductors do not have grain boundaries and are not limited in the same way as polycrystalline semiconductors. In addition, AOS can be easily processed at low temperatures and use environmentally friendly and less expensive

facilities.[18] As a result, extensive research has been conducted on oxide TFTs for their superior electrical properties, including high mobility, high optical transparency, good durability, and low cost in manufacturing while maintaining amorphous microstructure.[15]

### 2.2.1 Materials Physics

Hosono et al. compares silicon and IGZO in the amorphous and crystalline phase and explains the observed differences in mobility from an atomic bonding perspective (Fig. 2.2). In the crystalline phase, silicon achieves high carrier mobility due to effective overlapping of $sp^3$ orbitals.[5] However, in the amorphous phase, the $sp^3$ orbitals lack directionality and cannot achieve efficient overlap, resulting in very poor carrier mobility. In the case of IGZO, the metal s orbitals are large and isotropic, allowing for good overlap even in the amorphous structure. This is the reason metal oxide semiconductors are able to achieve decent mobility even in the amorphous phase. Hosono et al. also proposed the cation candidates in designing oxide semiconductor in TFTs in 1996[19] based on electron configuration and the selected cations from periodic table is shown in Fig. 2.3a. Zn, Ga, In and Sn are the most commonly used elements because of their low cost and non-toxicity.[20] Although it is difficult to compare the merit of specific elements and compositions since the fabrication process also affects device performance significantly, we can still summarize the overall materials behaviors.

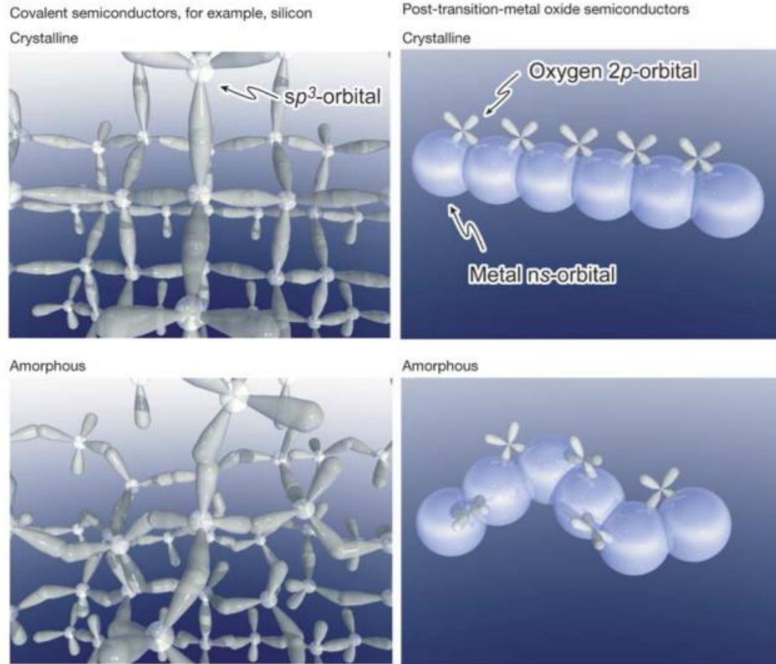


**Figure 2.2: Comparison of mobilities for silicon and IGZO in the crystalline and amorphous phase from an atomic bonding perspective.[5]**

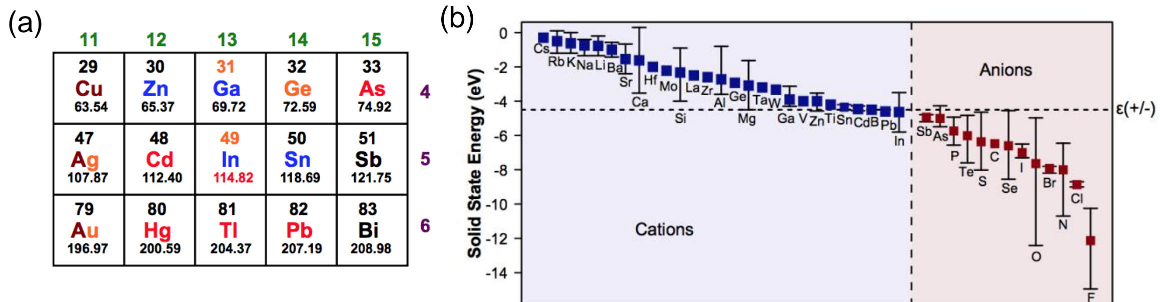


**Figure 2.3: (a) Candidates elements for heavy metal cations with (n - 1)$d^{10}ns^0$ electronic configuration.[20] b) Solid-state energy (SSE) values for 40 elements arranged in descending energy order.[21]**

Binary, ternary and quaternary compounds of these elements listed above have been reported as oxide semiconductor acting as an active layer in TFT. $SnO_2$, ZnO, $In_2O_3$, and $Ga_2O_3$ are the first reported binary compounds. However, due to the simplicity of component, binary compounds suffer from poor device performance such as high electrical resistivity, low stability, and low on-off ratio.[15] Meanwhile, binary compounds tend to crystallize, resulting in grain boundaries,

which greatly scatter the free carriers and affect device reliability. Multicomponent amorphous compounds, which refer to AOS, allow better performance than binary compounds because amorphous structure could avoid grain boundaries, which are associated with a high potential barrier. As a representative example, here we considered the case of amorphous IGZO. It has been noted that ZnO and $In_2O_3$ are easy to have polycrystalline phase while other multi-component oxides, such as IGZO, indium zinc oxide (IZO), and zinc gallium oxide (ZGO), are likely to be amorphous.[22] The reason is that adding different ionic charges and sizes in the phase disturbs crystallization and enhances the formation of amorphous phase (Fig. 2.4).[23] Thus, utilizing binary oxide helps to form an amorphous phase of the metal oxide semiconductor.

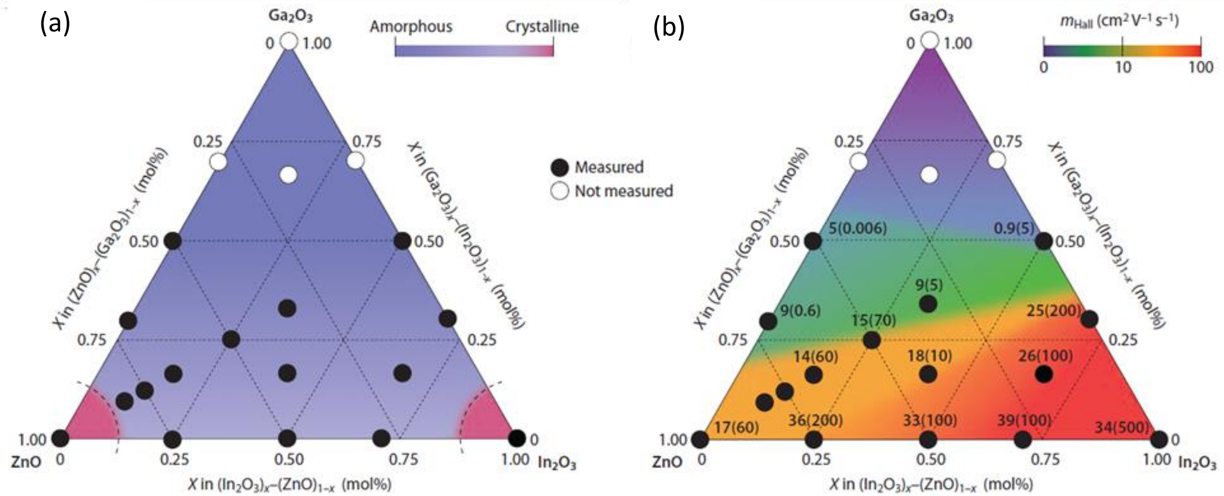


**Figure 2.4: Crystallinity of representative metal oxide semiconductor and each hall mobility.** [22]

Furthermore, different ions contribute differently to carrier concentration. Fig. 2.3b[21] shows the solid-state energy (SSE) values that denote the electron affinity (EA) for cations or ionization potential for anions of 40 different elements. The dashed line that distinguishes cations and anions at -4.5 eV equals to the ionization energy ε(+/-) of hydrogen donor/acceptor. For those elements with an SSE close to -4.5 eV (In, Sn, and Zn), which is a favorable energy for electron doping, the carrier concentration is enhanced. Noted that for TFT channel layer, the electron

concentration needs to be reduced to as low as possible. Therefore, elements with SSE above ε(+/-) should be employed for suppressing carriers. In this case, Ga with an SSE value of -3.1 eV is the most common electron-suppressing cation. The main breakthrough is the invention of IGZO in 2003.[24] As a representative AOS, IGZO has high mobility (10-30 $cm^2 V^{-1} s^{-1}$), high stability, low process complexity and has ready been commercialized in the display industry.

AOS TFTs have better electrical performance than a-Si:H TFTs because of their different chemical bonding,[25] resulting in the different origin of mobility. In the case of a-Si:H TFTs, the origin of mobility is hopping conduction rather than band conduction, so the drift mobilities of a-Si:H TFTs are lower than 1 $cm^2 V^{-1} s^{-1}$.[26] The conduction band minimum (CBM) and valence band maximum (VBM) of a-Si:H are formed by $sp^3$ hybridized orbitals which have strong spatial directivity. Therefore, deep and high-density localized states are formed below CBM and above VBM due to distortion of $sp^3$ hybridized orbitals caused by the disordered amorphous structure. As a result, the electrons and holes migrate mostly by hopping and result in low drift mobilities. By contrast, the electrical properties of AOSs do not degrade significantly in the crystalline phases. The CBMs of metal oxides are mainly formed by spherically spread large s orbitals of metal cations, and the overlaps between neighboring s orbitals are not altered significantly by structural disorder, thus enabling band conduction. Even in the amorphous phase, the mobility of AOSs could still exceed 10 $cm^2 V^{-1} s^{-1}$.

The chemical bonding theory is consistent with the density function theory (DFT). Pseudo-band structures of amorphous In-Ga-Zn-O (a-IGZO) and a-Si are shown in Fig. 2.5a and b. Fig. 2.5a shows conduction band dispersion with a bandwidth around 1 eV of a-IGZO.[27] The effective masses of electron do not deviate appreciably from that of c-IGZO.[23] By contrast, the pseudo-band structure shown in Fig. 2.5b indicates that all the bandwidth of a-Si is small (less than 0.5

eV), suppressing the band conduction. Meanwhile, because of its wider band gap, a-IGZO is expected to have lower off-state leakage current than a-Si:H for non-oscillated devices like biosensors.

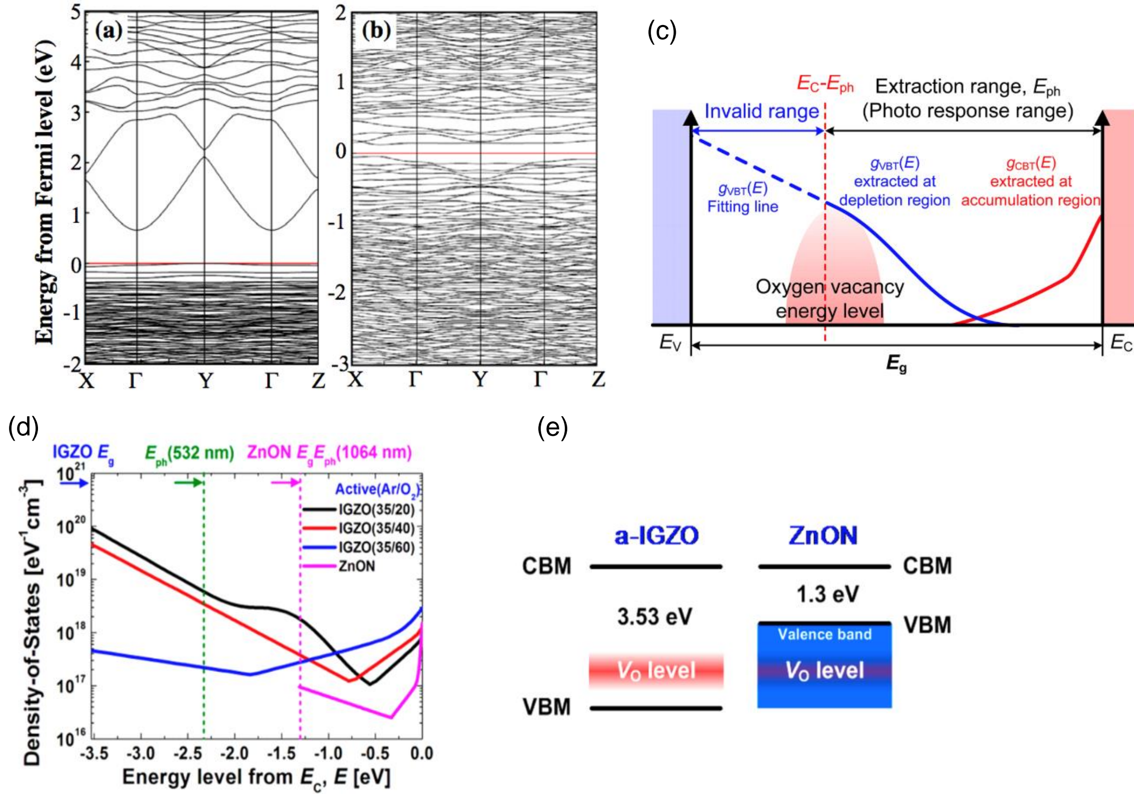


**Figure 2.5: (a) Pseudo-band structure of a-IGZO. b) Pseudo-band structure of a-Si. [27] c) Schematic diagram of the sub-bandgap states, which may be distinguished as valence band tail (VBT) states and conduction band tail (CBT) states. d) Modeled distributions of subgap states using exponential and Gaussian distributions. e) Schematic illustrating the Vo-related defects in a-IGZO and their negligible effects in ZnON semiconductors.[28]**

Here, we offer some guidance on choosing cations for future design of oxide semiconductor materials for TFTs. For better electrical properties, multicomponent compound mixing different cations with different SSE is more favorable than a binary compound. At the same time, stable amorphous structures could be achieved as well when mixing cations with different sizes. The incorporation of cations such as $In^{3+}$ and $Sn^{2+}$ is needed for forming broad-spreading CBMs even

in the amorphous phase, and the incorporation of cations with an SSE value much above -4.5 eV such as Ga is needed to better control the electron concentration.

Similarly, bond dissociation energy or formation energy is also sometimes used as a reference in choosing cations of TFT oxide semiconductor. In other words, AOS can be doped with elements that can form a strong bond with oxygen such as Y, S, Si, B and Al, which could be used as oxygen stabilizer. The first two elements Y and Sc are categorized as rare earth elements along with the lanthanides. Y and Sc have EA (-3.6 and -3.4, respectively) much above ε(+/-) and the high formation energy of their oxides can act as oxygen stabilizers. By alloying Y and Sc, the oxygen vacancy-related defects could be reduced.[29] Shin et al. have fabricated YIZO thin film transistors with comparable electrical properties to IGZO TFTs.[30] Using the latter three elements (Si, B and Al), covalent-ironic hybrid AOS materials with high mobility, high stability, and low hysteresis can be achieved.[31]

On the other hand, anion selection could also be a consideration in designing materials that are more stable to light. The oxygen vacancies ($V_o$) located within the band gap is the main reason for a persistent photoconductivity (PPC) effect,[32] which strongly affect the stability of the device. A new material that has been attractive to researchers recently is oxynitride. By substituting some of the oxygen of ZnO into nitrogen, the VBM of ZnON is elevated above the oxygen vacancies defect level. ZnON has much higher mobilities and a lower sub-threshold voltage swing (S.S) value than a-IGZO, as well as a smaller band gap. The reasons are discussed by Jang et al and illustrated in Fig. 2.5c-e.[28] The different electrical properties of a-IGZO and ZnON TFTs are determined by the distribution of subgap density of states (DOS). A schematic diagram of subgap states is shown is Fig. 2.5c, which could be distinguished by conduction band tail (CBT) states and valence band tail (VBT) states. The former determines the electrical

performance of TFT device, whereas the latter influences the stability with respect to electrical stress. The calculated subgap density of states is shown in Fig. 2.5d. The subgap DOS of IGZO varies with oxygen concentration, indicating that the $V_o$ with an energy level at 1.0-1.5 eV above VBM affects the VBT and CBT. However, as shown in Fig. 2.5e, the $V_o$ level is below the VBM of ZnON, resulting in a smaller VBT near VBM than that of a-IGZO. Thus in the case of ZnON TFTs, carriers undergo direct band-to-band generation and recombination because of their smaller band gap. It is also suggested that besides nitrogen, other cations having a larger size than oxygen such as $S^{2-}$ and $Se^{2-}$ with higher p orbital energy could also elevate the VBM above $V_o$ and deactivate oxygen vacancies.[33]

### 2.2.2 Sol-Gel Method Deposition of Metal Oxide Thin Film

Many kinds of metal oxides have been prepared based on sol-gel processing, such as $In_2O_3$, ZnO, IZO, IGZO, zinc tin oxide (ZTO), and indium gallium oxide (IGO). Sol-gel chemistry is a process to synthesize materials through a phase transformation from liquid precursors to a sol, which is known as a colloidal suspension and eventually to a gel, which is a network structure. In more detail, the main step for sol-gel chemistry starts with the synthesis of the sol from hydrolysis and condensation alkoxides after preparing the precursor. Next, it forms the gel by polycondensation to produce metal-oxo-metal or metal-hydroxy-metal bonds. Aging step is followed with shrinking the gel network and expulsion of solvent. The last step is a drying the gel to create a dense xerogel or aerogel. The gel can be generally classified into five different types, colloidal, metal-oxane polymer, metal complex, polymerizable complex and crosslinking polymers. In the case of metal oxide materials, metal salts are dissolved in a solvent first to prepare precursor solutions and they go through hydrolysis forming hydroxides. It transforms to colloidal solutions, so-called sol, and finally converted to metal oxide networks consisting of

liquid and solid phases together, so-called gel.[34] There are several advantages of sol-gel chemistry. It ensures desired stoichiometry of reagents, which eventually produces complex materials. In addition, it has good control over particle size and morphology. Cost effectiveness is regarded as one of the most attractive points in the sol-gel process. Several different deposition methods using sol-gel chemistry have been introduced. Usually, they are different in terms of how sol-gel solution is deposited, such as spin coating, spray coating, and printing.[35]

## 2.3 Low Temperature Process and UV Treatment

Current trend is that the rigid glass or silicon substrates are being replaced by polymer substrates because of their bendability and low cost in the application of flexible electronic devices. The main issue in the usage of flexible polymer substrate is their low glass transition temperatures. Glass transition temperature of various kind of polymer substrate is shown in Fig. 2.6.

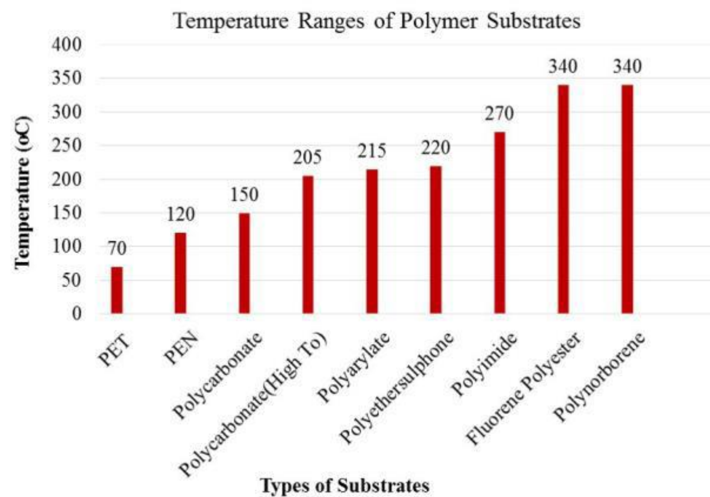


**Figure 2.6: Glass transition temperature of commonly used polymer substrates in flexible electronic devices.[36]**

Solution-process is an effective way to form high-quality metal oxide films on flexible polymer substrates, but a high-temperature (up to 350 °C) annealing step is typically required, which could cause phase transition and crystallization to some conventional polymer substrates, such as

PEN, which has a glass transition temperature of 220 °C. Thus, it is meaningful to understand the chemistry of metal oxide thin film formation and to develop low temperature fabrication process that is compatible with polymer substrate that have low glass transition temperature base on this knowledge.

Yong-Hoon Kim and his coworkers published a novel photochemical method incorporating deep-ultraviolet (DUV) light into annealing process which is conducted in nitrogen under room temperature.[37] Various metal oxide systems were fabricated on both glass and polymer substrates with $Al_2O_3$ as gate insulator grown by atomic layer deposition (ALD). During the DUV treatment, sol-gel condensation and film densification occurs and high performance TFT with a mobility as high as 7 $cm^2/V{\cdot}s$ is obtained, while the flexibility and transparency of polymer substrates are negligibly affected. Fig. 2.7 illustrates the two stages of photo annealing process: first rapid chemical condensation followed by slow structure rearrangement and densification. The thermal energy of this process is offered by the heating effect of DUV. However, this method doesn't work as well when using thermally grown $SiO_2$ as a gate dielectric.

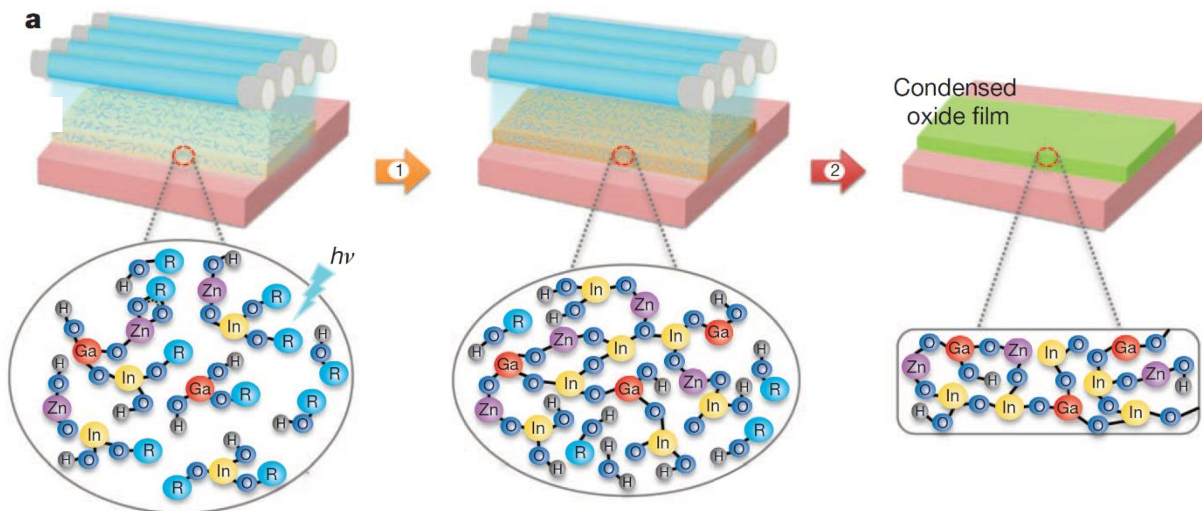


**Figure 2.7: Condensation mechanism of metal oxide precursors by DUV irradiation.[37]**

# 3. Experimental Methods

One issue of solution-processed TFT is that it shows poor electrical properties under low annealing temperature. The main goal of this thesis is to develop a low-temperature process which is compatible to low-cost gate dielectric material while maintaining high electron mobility and good transfer characteristics. Based on this starting point, TFT devices annealled at different temperatures were fabricated in order to study the effect of thermal energy. Devices fabricated with or without UV treatment were studied in $In_2O_3$ and IGZO systems. The absorbance of films with or without additives were compared to analyze the effect and mechanism of additives.

## 3.1 Substrate Cleaning

The 4 inch boron-doped ($p^{++}$) silicon wafers with 1000 Å $SiO_2$ (purchased from WaferPro company) were cut into several 1.5 cm × 1.5 cm square substrates. The substrates were cleaned by organic solvents and the cleaning process contained two steps. First, the substrates were immersed by acetone in a cylindrical container and subjected to ultrasonic treatment for 15 minutes in order to remove dust, oil, etc.. Then, the substrates were ultra-sonicated with isopropanol (IPA) following the same method of first step. The cleaned substrates were immersed and stored in IPA.

## 3.2 Precursor Solution Preparation

The active layer fabricated in this work was composed by either indium oxide ($In_2O_3$) or indium gallium zinc oxide (IGZO). The concentration of all solutions was 0.1 M and their compositions were shown in Table 3.1. The 0.1 M $In_2O_3$ precursor solutions were prepared by dissolving 300.8 mg of indium nitrate hydrate ($In(NO_3)_3 \cdot xH_2O$, Aldrich, 99.999%) in 10 mL of 2-methoxyethanol (2-ME, Aldrich, 99%). The 0.1 M IGZO precursor solution was prepared by dissolving 270.8

mg of Indium nitrate hydrate, 12.8 mg of gallium nitrate hydrate ($Ga(NO_3)_3 \cdot xH_2O$, Aldrich, 99.999%), and 9.5 mg of zinc nitrate hydrate ($Zn(NO_3)_2 \cdot xH_2O$, Aldrich, 99.999%) in 10 mL of 2-ME. Both $In_2O_3$ and IGZO precursor solutions were stirred for 10 minutes at 40°C. The total molar ratio of IGZO solution was 9:0.5:0.5 of In, Ga and Zn. Then 200 μL of acetylacetone (AcAc, Aldrich, 99%) and 70 μL of ammonium hydroxide (aq) ($NH_4OH$, 28% $NH_3$ in water, Aldrich, 99.99%) were added to precursor solutions and stirred for 12 hours. Solutions were filtered through 0.2 μm PTFE syring filter (GE, Trevose, PA, USA) and stored under room temperature. Pristine $In_2O_3$ precursor solution without any additive was also prepared for comparison.

**Table 3.1: Composition of precursor solution**

| Solution | Precursor | Additive |
|---|---|---|
| **$In_2O_3$** | $In(NO_3)_3$ | AcAc, ammonium |
| **$In_2O_3$ (pristine)** | $In(NO_3)_3$ | none |
| **IGZO (9:0.5:0.5)** | $In(NO_3)_3$, $Ga(NO_3)_3$, $Zn(NO_3)_2$ | AcAc, ammonium |

## 3.3 Fabrication of Devices

The substrates were blow dried with nitrogen after every step of fabrication process. Before spin coating, the substrates were treated in UV-Ozone cleaner for 20 minutes to remove organic contaminants on surface and to improve the wettability of substrates. Both $In_2O_3$ and IGZO precursor solutions were spin-coated on UV-Ozone pre-cleaned substrates at 3000 rpm for 30 seconds. Approximately 20 μL of precursor solution was dispensed onto the substrate before spinning. After spin-coating, the substrates were immediately prebaked at 100°C for 10 minutes to remove the excess solvent, preventing the formation of pin holes. The substrates were then

either annealed at different temperatures, varying from 200 °C to 350 °C, on a hotplate in fume hood for 4 hours or annealed under DUV exposure with a combined wavelength of 184.9 nm (10%) and 253.7 nm (90%) on a self-made hotplate at 220 °C for 4 hours. The temperature of the self-made hotplate was monitored by a thermal couple. After annealing, all samples were slowly cooled to room temperature to prevent cracks caused by quenching induced stress. The Al source and drain electrodes (thickness = 100 nm) were deposited by thermal evaporation (power controlled by Sorensen Power Supplies DCR 7-300B) through a shadow mask under vacuum pressure of $5 \times 10^{-6}$ Torr. The deposition rate was controlled at 1.5 Å/s. The channel region was defined by 1000 μm of width (*W*) and 200 μm of length (*L*). Fig. 3.1 demonstrated a detailed flowchart of device fabrication. The devices were scathed in order to expose the silicon gate before conducting various electrical characterizations.

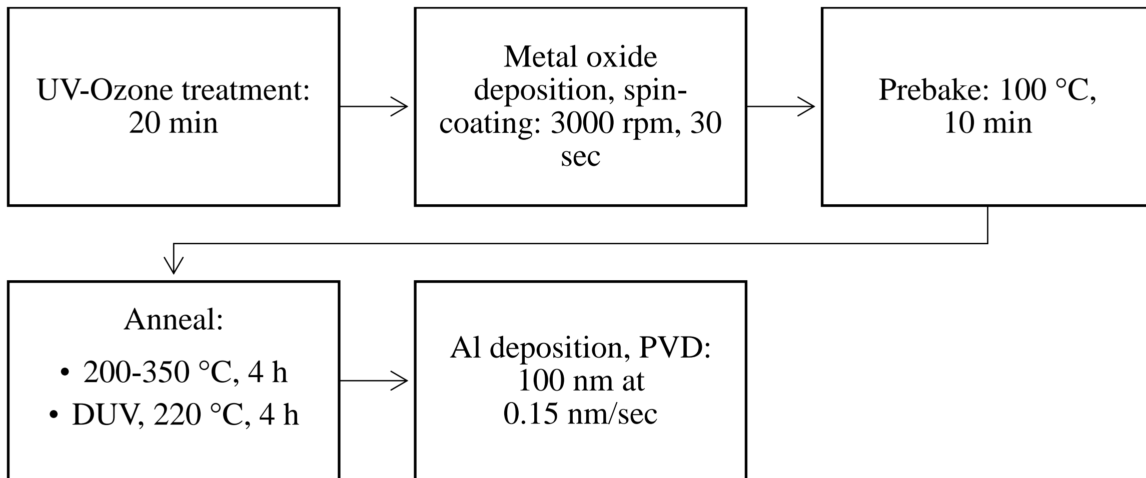


**Figure 3.1: Schematic illustration of fabrication process**

## 3.4 Film and Device Characterization

The electrical characteristics of devices were measured in ambient air by Agilent 4155C semiconductor parameter analyzer controlled by a PC. The transfer characteristics were obtained by fixing drain-source voltage ($V_{ds}$) at 20 V and double sweeping gate-source voltage ($V_{gs}$) form

-30V to 40V by a step size of 100 mV and measuring drain-source current ($I_{ds}$). Linear mobility and saturation mobility were calculated by equation 2.1 and 2.2, respectively.

For stress test scenario, multiple transfer I-V measurements (single sweep) were performed by inserting the positive bias stress (PBS) at certain pre-defined times. During the measurement, constant positive-bias stress is applied over consecutive periods of 20 s, 40 s, 80 s, 160 s, 320 s and 640 s by holding $V_{ds}$ =10 V and $V_{gs}$ = 20 V.

The microstructures and morphologies of films were investigated by atomic force microscope (AFM) (Bruker Dimension FastScan Scanning Probe Microscope (SPM)). The optical absorption spectra of metal oxide films were determined by Hitachi U-4100 UV-Visible spectroscopy. The indium oxide films prepared for UV-Vis measurement were deposited on the quartz substrates.

Grazing incident wide angle X-ray scattering measurement was carried out at Advanced Light Source on 7.3.3. beamline. All the samples were prepared on the silicon wafer. Samples were irradiated by 10 keV at a fixed X-ray incident angle of 0.2 °. The incident angle was above the critical angle of the indium oxide film. The X-ray exposure time was 5 seconds.

# 4. Results and Discussion

## 4.1 Device Structure

A bottom gate staggered structure is employed in this study. The schematic structure of as-fabricated metal oxide TFT device is shown in Fig. 4.1, using aluminum as source and drain terminal, metal oxide ($In_2O_3$ or IGZO) as active layer, $SiO_2$ as gate insulator and boron doped silicon as gate terminal.

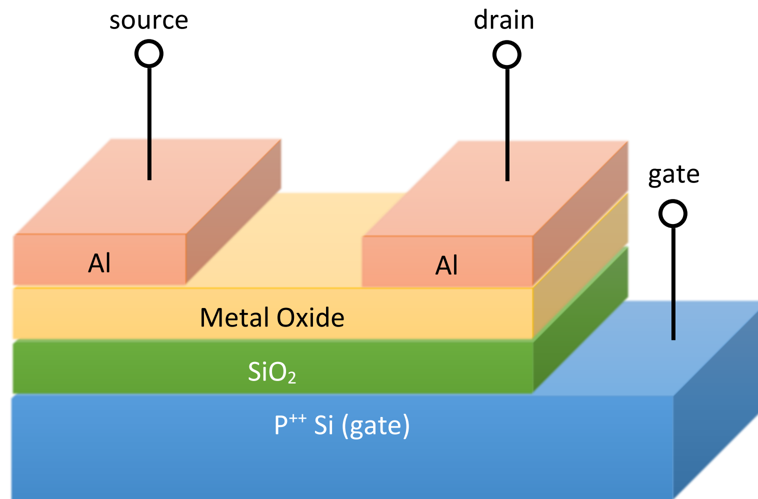


**Figure 4.1: The schematic structure of TFT.**

## 4.2 Annealing Temperature Dependency of $In_2O_3$ TFT Device Performance

Solution processed metal oxide thin film usually requires a high temperature thermal annealing process (up to 350°C). The electrical properties of TFT device are strongly dependent on the annealing temperature. Fig. 4.2 illustrates the transfer characteristics of devices processed under different annealing temperature. Table 4.1 summaries the average electrical properties of devices fabricated under various annealing temperatures. When annealing temperature was as low as 200 °C, the transfer curve is rather irregular. Device exhibits poor electrical properties with a linear mobility of 1.1 $cm^2/V \cdot s$ and a saturated mobility of 0.75 $cm^2/V \cdot s$. The main reason to

explain the poor mobility is that there was not sufficient thermal energy for lattice to rearrange, resulting in severe defects and trap states. With the elevation of annealing temperature, device mobility exhibits a rapid increase. Both linear mobility and saturated mobility increase to 25.45 $cm^2/V \cdot s$ and 13.68 $cm^2/V \cdot s$ respectively in the device processed by 350 °C thermal-annealing.

Although the significant improvement has been observed in mobility as a function of annealing temperature, it is worth noting that other electrical properties such as subthreshold swing and on/off ratio become worse. When temperature was higher than 300 °C, The devices show large subthreshold swing, indicating inefficacy in turning device on and off. The on/ off ratio also becomes smaller when temperature was above 300 °C. Though the on-current increases by a few times compared with that of devices fabricated at low temperature, the off current raises by several magnitudes as well, indicating that gate leakage current and power consumption are much higher. Besides, it is difficult to control the carrier concentration in the bulk of film at high temperature, resulting in negative turn on voltage. Choosing the annealing temperature is a compromise between achieving the desired performance while also maintaining other properties. In this case, to obtain high mobility and decent transfer characteristics, preferred annealing temperature should be around 250 °C.

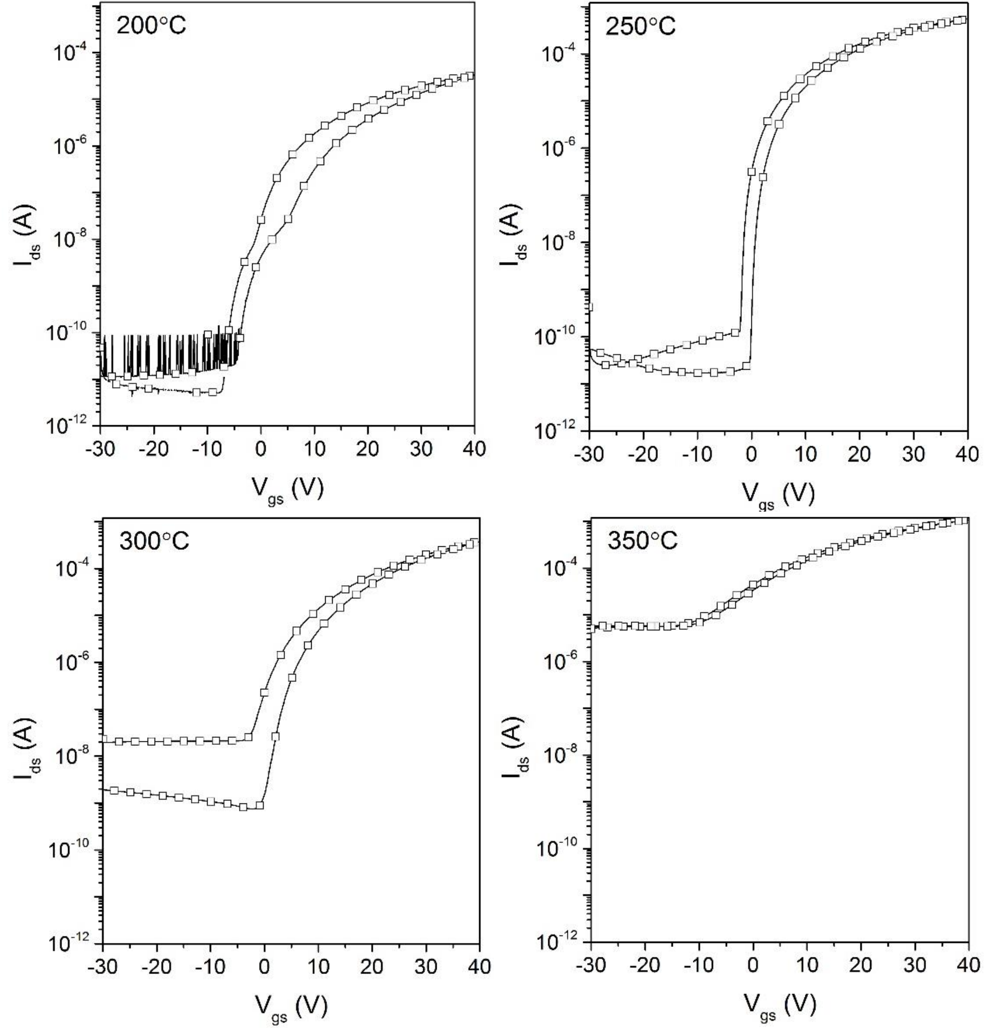


**Figure 4.2: Transfer characteristics of thermal-annealed devices with different annealing temperatures.**

**Table 4.1: Average electrical properties of thermal-annealed $In_2O_3$ TFT under different annealing temperatures.**

| Temperature (°C) | $\mu_{lin}$ ($cm^2/V\cdot s$) | $\mu_{sat}$ ($cm^2/V\cdot s$) | Subthreshold Swing | On/off |
|---|---|---|---|---|
| **200** | 1.10 | 0.75 | 0.89 | $10^6$ |
| **250** | 6.36 | 5.74 | 0.40 | $10^7$ |
| **300** | 12.71 | 7.96 | 2.1 | $10^4$ |
| **350** | 25.45 | 13.68 | 12.1 | $10^2$ |

## 4.3 UV-Annealing Treatment

In order to achieve higher mobility at the low temperature processed $In_2O_3$ film, a UV-annealing treatment was employed. Table 4.2 compares the average electrical properties of both UV-annealing and thermal-annealing devices processed at low temperature (220°C). Under the same annealing temperature, UV-annealing devices show better overall performance than thermal-annealing devices. UV treatment improved the average linear mobility by 56% and saturation mobility by 40%, indicating that the charge carriers could transport in channel materials much more efficiently. The subthreshold swing was decreased by 32%, indicating that devices could turn on and off more efficiently due to UV treatment, enabling lower operating voltage and less power consumption for future devices.

**Table 4.2: The average electrical properties of UV-annealing and thermal-annealing $In_2O_3$ devices.**

| Device | Temperature (°C) | $\mu_{lin}$ (cm²/V·s) | $\mu_{sat}$ (cm²/V·s) | Subthreshold Swing | On/off |
|---|---|---|---|---|---|
| **Thermal-annealing** | 220 | 2.39±0.08 | 2.10±0.09 | 0.40±0.04 | $10^7$ |
| **UV-thermal** | 220 | 3.75±0.23 | 2.95±0.32 | 0.27±0.04 | $10^7$ |

The typical transfer characteristics of unpassivated UV-annealing and thermal-annealing devices are shown in Fig. 4.3. In order to examine the UV-annealing is a universe method to improve the electrical properties of low temperature processed metal oxide TFT, in addition to $In_2O_3$, IGZO was also studied. Apparently, under the same sweeping rate, thermal-annealing devices of both systems exhibit a wider hysteresis, while narrower hysteresis is preferred during the operation of TFT, since it may affect device stability. For $In_2O_3$ system, the UV-annealing devices have an average hysteresis width less than 1 V and thermal-annealing devices have an average hysteresis width more than 5 V. UV-annealing method shows an obvious improvement of hysteresis for

both systems. For IGZO system, the thermal-annealing devices turn on around 10 V while the UV-annealing devices turn on at 0 V, indicating that less energy is required to turn on the devices after UV-annealing.

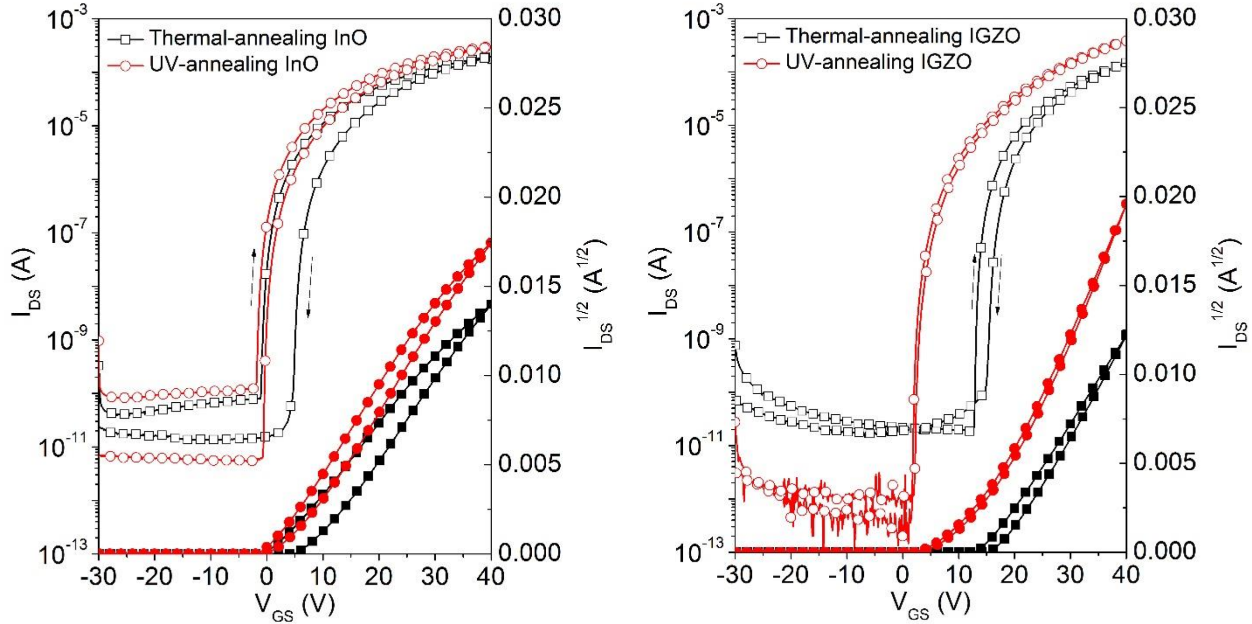


**Figure 4.3: Typical transfer characteristic of thermal-annealing and UV-annealing devices of $In_2O_3$ (left) and IGZO (right).**

Since voltage shift and hysteresis have similar physical origin[38], it is predictable that UV-annealing devices may have much better stability. The results of positive bias stress (PBS) test of thermal-annealing and UV-annealing $In_2O_3$ devices fabricated by same precursor solution are shown in Fig. 4.4 ($V_{ds}$ =10 V and $V_{gs}$ =20 V). The voltage shift after 640s of thermal-annealing and UV-annealing devices are 12 V and 4 V, respectively, indicating that device stability was improved by three times after UV-annealing.

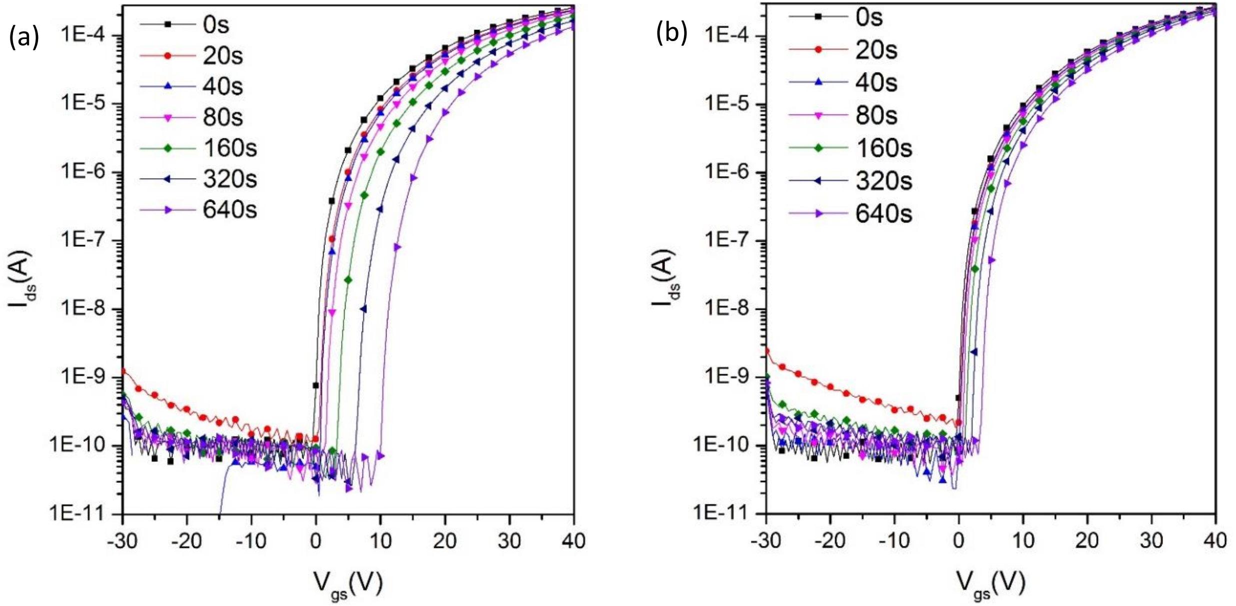


**Figure 4.4: Positive bias stress test of (a) thermal-annealing $In_2O_3$ device and (b) UV-annealing $In_2O_3$ devices.**

Although the UV-annealing method cannot completely remove the hysteresis and instability effect, there is still room for the further improvement. The channel layers of TFT device presented in this work had not been patterned and all devices were unpassivated. Patterning and surface passivation could reduce hysteresis and instability.

In order to the understand the UV effect on the morphology and microstructure of solution processed $In_2O_3$ film, AFM surface topography of $In_2O_3$ films with different treatments was measured, shown in Fig. 4.5. It is obvious that both thermal-annealing and UV-annealing film show good uniformity in AFM image without any large feature. The thermal-annealing device has a roughness $R_{max}$ of 1.66nm and the UV-annealing film shows slightly improved roughness $R_{max}$ of 1.46 nm.

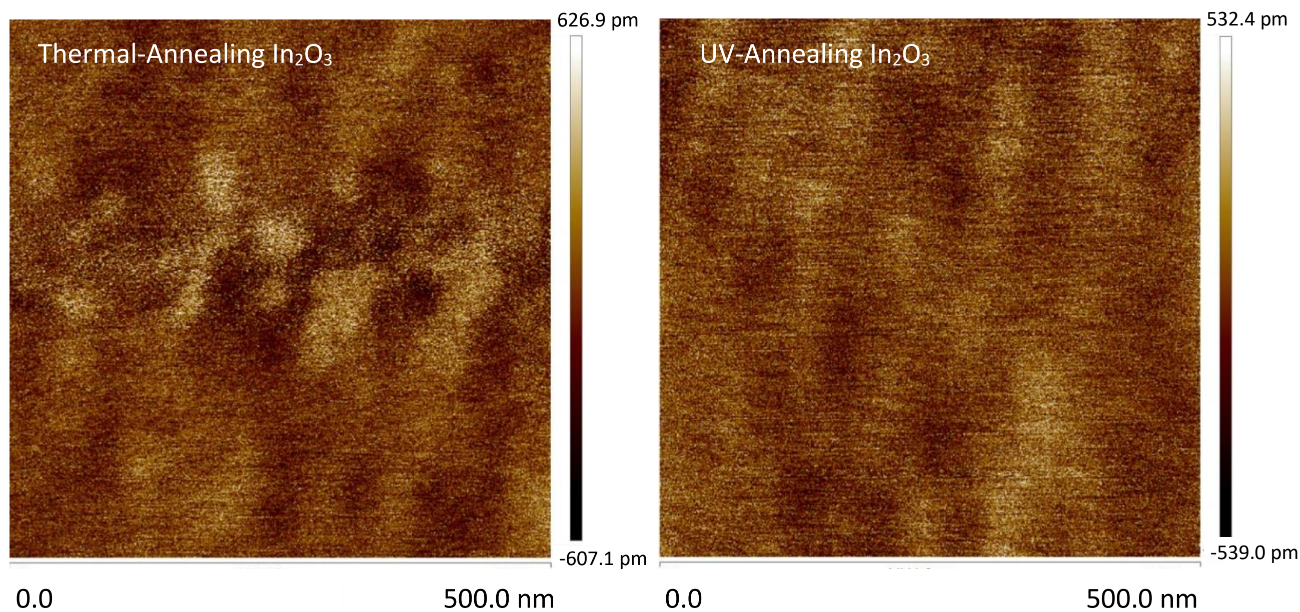


**Figure 4.5: AFM image of thermal-annealing (left) and UV-annealing (right)**

The X-ray scattering technique is also used to further probe the crystallization behavior of $In_2O_3$ film with different treatment. Due to their thin thickness (~30nm), the lab-based X-ray diffraction cannot provide enough scattering signal. The grazing incident wide-angle X-ray scattering technique (GIWAXS) is used to probe the crystallization behavior of indium oxide film processed with different methods. The scattering patterns of indium oxide processed with and without UV-annealing illumination are shown in Fig. 4.6. In both scattering images, a very weak scattering pattern is observed at q=2.1Å, which is corresponding to the indium oxide (222) peak. Compare to the indium oxide film processed without UV-annealing illumination, the DUV treated film exhibits the slightly stronger scattering intensity, indicating that the UV-annealing is able to slightly improve the crystallization of indium oxide film. However, the weak scattering signal demonstrates that the crystallinity of both film is still very low and most of region are amorphous phase.

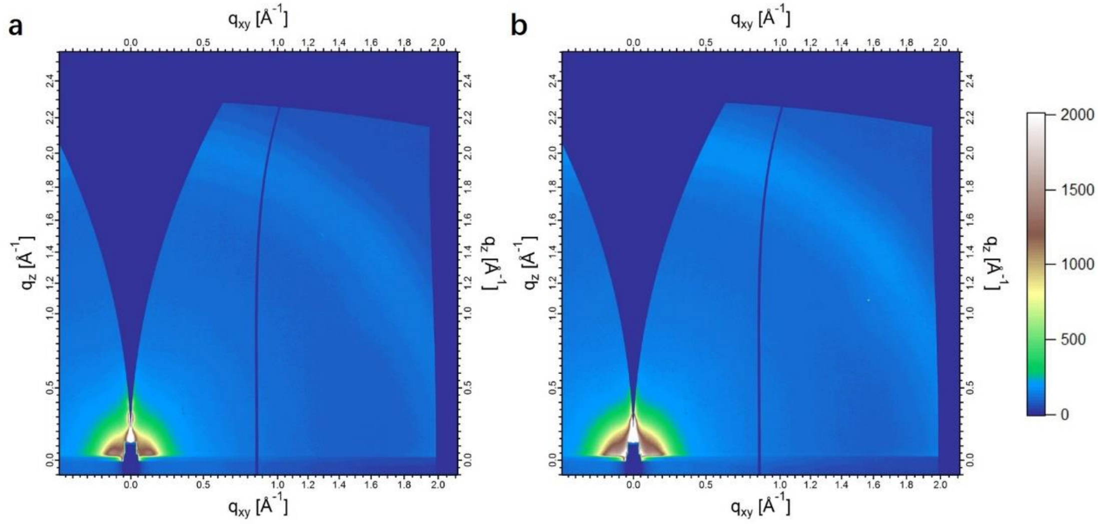


**Figure 4.6: 2D GIWAXS scattering patterns of (a) indium oxide film processed without UV-assisted method and (b) indium oxide film processed with UV-assisted method.**

## 4.4 Proposed Mechanism

In this case, both of DUV treatment and additives contribute to the enhancement of electrical properties in low temperature processed metal oxide semiconductors. Chemical condensation and lattice rearrangement occur during the annealing process, which requires certain energy to overcome energy barrier. When temperature is not high enough, defects generated during spin coating process will remain and degrade the performance of TFT. When DUV light is shined on the film, it may provide extra energy to the film and facilitate the rearrangement of atoms, thus lowering the required annealing temperature, which is confirmed by X-ray scattering. The relative higher crystallinity of $In_2O_3$ film was observed in the UV-annealing device. Trapped charges, both electrons and holes, in bulk of oxide are one of the general types of charges.[12] It can be introduced during device fabrication or can occurs during operation and its occurrence leads to hysteresis in inorganic field effect transistor devices. The improvemenst of hysteresis and stability indicated that UV-annealing could remove the trapped charges.

The additives enhanced the absorption of DUV due to π→π* transition of AcAc. Fig. 4.7 compares the absorbance of thin film formed by pristine $In(NO_3)_3$ solution and solution with additives at wavelength ranges from 200 nm to 800 nm. The precursor solution with additives shows better absorbance at wavelength below 300nm while the wavelength of DUV lamp (184.9 nm (10%) and 253.7 nm (90%)) lies in this regime. Meanwhile, since the additives are DUV decomposable, the absorbance of visible light was not affected significantly, suggesting that the transparency of film changed negligibly.

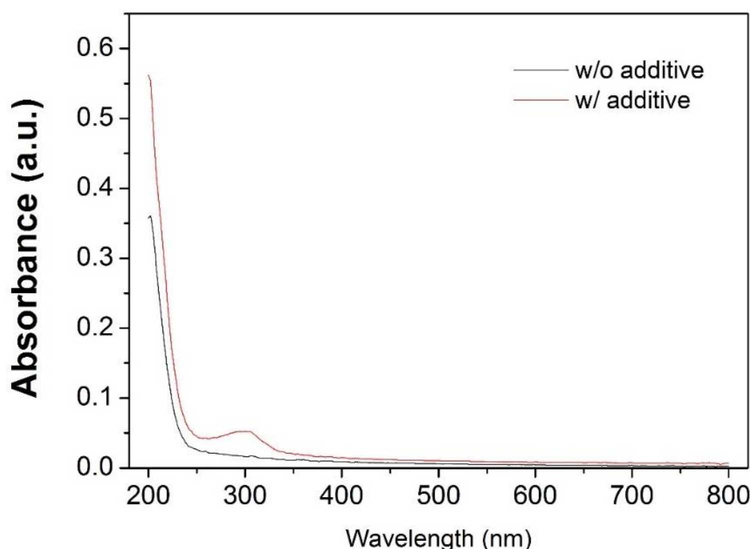


**Figure 4.7: Absorbance of film formed by $In_2O_3$ precursor solution w/ and w/o additive.**

The incorporation of a small amount of additives in precursor solutions also contributes to film condensation. Previous study has shown that DUV could be used to directly pattern various metal oxide thin film based on photo chemical reaction, assisted by AcAc and ammonium[39]. The proper mechanism of this technique is described by a combustion reaction between additives and precursor shown below (Fig. 4.8).

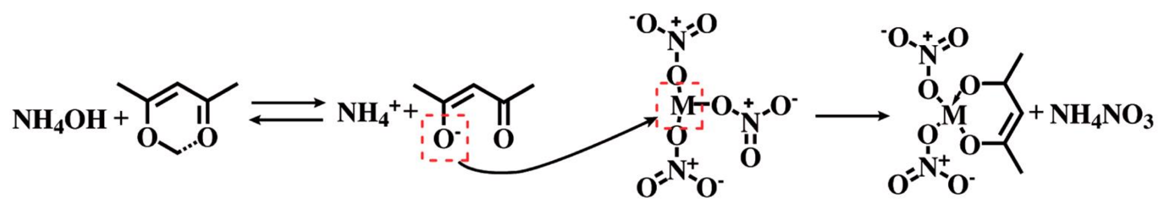


**Figure 4.8: Chemical reaction of additives assisted metal oxide formation.[39]**

This AcAc chelates metal nitrates to form a metal complex assisting by $NH_4OH$. The two additives promote oxide lattice formation at low temperature, thus improve the performance of TFT. The byproduct will decompose by heat and leave the system as vapor phase.

# 5. Conclusions

It has been known that the fabrication of solution-processed metal oxide TFT includes a high temperature annealing step, which is incompatible with some conventional flexible polymer substrates. In this work, the electrical properties dependency on temperature was studied. Based on this knowledge, a DUV-assisted annealing method incorporating DUV-decomposable additives was demonstrated. The TFT devices were processed at temperature as low as 220 °C. By this mean, the electrical properties had been successfully improved for both $In_2O_3$ and IGZO systems compared with thermal-annealing devices. The linear mobility and saturation mobility of UV-annealing samples were improved by 56% and 40% respectively; the subthreshold swing was decreased by 32%; the stability was increased by three times and more narrower hysteresis had been achieved.

These results are in line with expectation, indicating that UV-assisted annealing method serves as an effective approach to lower the fabrication temperature because it offers extra energy for lattice rearrangement and the combustion reaction between additives and metal oxide precursor also contributes to the film condensation. Thus, this approach opens a new route for low temperature fabrication of high performance solution-processed metal oxide TFT on flexible polymer substrates and also offers new solution to low temperature metal oxide synthesis.

# 6. Scope of Future Work

The starting point of this study is to lower the processing temperature of metal oxide thin film semiconductors while maintaining decent device performance by using a novel UV assisted annealing method. Whether the ozone generates in the UV chamber contributes to this process is inconclusive. More research should be done under same condition in nitrogen atmosphere instead of in ambient atmosphere to investigate the effects of ozone.

The active layer of TFT devices presented in this work had not been patterned and all devices were unpassivated. In future work, direct light patterning or photolithography could be employed after metal oxide thin film deposition to reduce the leakage current while surface passivation could be conducted as the final processing step to reduce hysteresis and instability.

There is an absorbance peak around 300 nm in UV-Vis spectroscopy and the reason for this phenomenon remains unclear. Due to experimental condition, the wavelength and power of UV lamp cannot be altered. More work could be done by comparing the performance of devices annealed at different UV wavelength, especially wavelength around 300 nm. Besides, better electrical properties could be achieved by optimizing DUV energy density.

# 7. References


[1] P. K. Weimer, *Proceedings of the IRE* **1962**, *50*, 1462.

[2] M. Prins, K. O. Grosse-Holz, G. Müller, J. Cillessen, J. Giesbers, R. Weening, R. Wolf, *Applied physics letters* **1996**, *68*, 3650.

[3] C. Seager, D. McIntyre, W. Warren, B. Tuttle, *Applied physics letters* **1996**, *68*, 2660.

[4] R. L. Hoffman, B. J. Norris, J. F. Wager, *Appl. Phys. Lett.* **2003**, *82*, 733.

[5]K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, H. Hosono, *Nature* **2004**, *432*, 488.

[6] M. J. Powell, *IEEE Trans. Electron Devices* **1989**, *36*, 2753.

[7] J.-H. Lee, D. N. Liu, S.-T. Wu, *Introduction to flat panel displays*, Vol. 20, John Wiley & Sons, 2008.

[8] A. C. Tickle, *Thin-film transistors: a new approach to microelectronics*, John Wiley & Sons, 1969.

[9] S. R. Thomas, P. Pattanasattayavong, T. D. Anthopoulos, *Chem. Soc. Rev.* **2013**, *42*, 6910.

[10] H. Klauk, *Chem. Soc. Rev.* **2010**, *39*, 2643.

[11] T. Kamiya, K. Nomura, H. Hosono, *Science and Technology of Advanced Materials* **2016**.

[12] D. K. Schroder, *Semiconductor material and device characterization*, John Wiley & Sons, 2006.

[13] S. M. Sze, K. K. Ng, *Physics of semiconductor devices*, John wiley & sons, 2006.

[14] R. Hoffman, *J. Appl. Phys.* **2004**, *95*, 5813.

[15] E. Fortunato, P. Barquinha, R. Martins, *Adv. Mater.* **2012**, *24*, 2945.

[16] D. Geng, D. H. Kang, M. J. Seok, M. Mativenga, J. Jang, *IEEE Electron Device Lett.* **2012**, *33*, 1012.

[17] M. Egginger, S. Bauer, R. Schwödiauer, H. Neugebauer, N. S. Sariciftci, *Monatshefte für Chemie-Chemical Monthly* **2009**, *140*, 735.

[18] E. M. Fortunato, L. M. Pereira, P. M. Barquinha, A. M. Botelho do Rego, G. Gonçalves, A. Vilà, J. R. Morante, R. F. Martins, *Appl. Phys. Lett.* **2008**, *92*, 222103.

[19] H. Hosono, M. Yasukawa, H. Kawazoe, *J. Non-Cryst. Solids* **1996**, *203*, 334..

[20] J. F. Wager, B. Yeh, R. L. Hoffman, D. A. Keszler, *Curr. Opin. Solid State Mater. Sci.* **2014**, *18*, 53.

[21] B. D. Pelatt, R. Ravichandran, J. F. Wager, D. A. Keszler, *J. Am. Chem. Soc.* **2011**, *133*, 16852.

[22] K. Nomura, A. Takagi, T. Kamiya, H. Ohta, M. Hirano, H. Hosono, *Jpn. J. Appl. Phys.* **2006**, *45*, 4303.

[23] T. Kamiya, H. Hosono, *NPG Asia Mater.* **2010**, *2*, 15.

[24] K. Nomura, H. Ohta, K. Ueda, T. Kamiya, M. Hirano, H. Hosono, *Science* **2003**, *300*, 1269.

[25] T. Kamiya, K. Nomura, H. Hosono, *Phys. Status Solidi A* **2010**, *207*, 1698.

[26] H. Fritzsche, K.-J. Chen, *Physical Review B* **1983**, *28*, 4900.

[27] T. Kamiya, K. Nomura, H. Hosono, *Science and Technology of Advanced Materials* **2016**.

[28] J. T. Jang, J. Park, B. D. Ahn, D. M. Kim, S.-J. Choi, H.-S. Kim, D. H. Kim, *ACS Appl. Mater. Interfaces* **2015**, *7*, 15570.

[29] W. Hu, Yttrium and Scandium in Solution-processed Oxide Electronic Materials, University of Michigan,  2016.

[30] H. S. Shin, G. H. Kim, W. H. Jeong, B. Du Ahn, H. J. Kim, *Japanese Journal of Applied Physics* **2010**, *49*, 03CB01.

[31] T. Xiao, G. Yu, C. L. Shieh, J. W. Park, F. Foong, K. Lee, J. Musolf, G. Wang, K. Ottoson, K. Yang, "26-1: Invited Paper: Metal Oxide TFT Turnkey Manufacturing Solution for a-Si TFT Lines", presented at *SID Symposium Digest of Technical Papers*, 2016.

[32] S. Lany, A. Zunger, *Physical Review B* **2005**, *72*, 035215.

[33] H.-S. Kim, S. H. Jeon, J. S. Park, T. S. Kim, K. S. Son, J.-B. Seon, S.-J. Seo, S.-J. Kim, E. Lee, J. G. Chung, *Sci. Rep.* **2013**, *3*, 1459.

[34] A. Danks, S. Hall, Z. Schnepp, *Mater. Horiz.* **2016**, *3*, 91.

[35] J. S. Heo, J. W. Jo, J. Kang, C. Y. Jeong, H. Y. Jeong, S. K. Kim, K. Kim, H. I. Kwon, J. Kim, Y. H. Kim, M. G. Kim, S. K. Park, *ACS Appl. Mater. Interfaces* **2016**, *8*, 10403.

[36] S. Khan, L. Lorenzelli, R. S. Dahiya, *IEEE Sensors Journal* **2015**, *15*, 3164.

[37] Y. H. Kim, J. S. Heo, T. H. Kim, S. Park, M. H. Yoon, J. Kim, M. S. Oh, G. R. Yi, Y. Y. Noh, S. K. Park, " *Nature* **2012**, *489*, 128.

[38] M. G. Kane, *Organic Field-Effect Transistors* **2007**, 551.

[39] Y. S. Rim, H. Chen, S. H. Bae, H. J. Kim, Y. Yang, *ACS nano* **2014**, *8*, 9680.