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***Abstract*—The power consumption of next-generation high-performance processors is expected to reach and eventually exceed 1000 W, with core logic voltages below 1 V and peak current demand beyond 1000 A. To deliver ultra-high currents at low voltages with minimal power distribution network losses, this paper presents a compact 48-V-to-sub-1-V switching bus converter (SBC), a single-stage hybrid switched-capacitor (SC) voltage regulator for processor vertical power delivery (VPD). The SBC comprises a 2-to-1 SC front-end and two 10-branch series-capacitor buck modules, which are merged through two switching buses. A hardware prototype was designed and built with two-phase coupled inductors for performance validation. The coupled inductors were customized for VPD, with their windings both functioning as part of the coupled inductors and serving as the connection between the SBC and the processor motherboard. The hardware prototype met a stringent maximum height limit of 5 mm and achieved a current density of 0.614 A/mm^2 at a full-load current of 600 A. Additionally, it demonstrated excellent performance compared to the state-of-the-art academic works for 48 V to point-of-load conversion.**

I. Introduction

Driven by the rapid development of generative artificial intelligence (AI), data centers have become the fastest-growing electricity consumers in the grid. By 2030, they are expected to consume 8% of U.S. power, up from 3% in 2022 [1]. According to a recent projection [2], the combined power demand of NVIDIA AI servers alone could reach 9.75–15.3 GW by 2027, resulting in an annual electricity consumption of 85.4–134.0 TWh, which could surpass the annual electricity consumption of some countries [3]. Behind this rapid growth is the dramatic increase in the electric power consumption of high-performance processors (e.g., graphics processing units [GPUs], central processing units [CPUs], application-specific integrated circuits [ASICs], etc.). In recent years, processor power consumption has increased dramatically due to the fast-growing demand for greater computational power and is expected to reach and eventually exceed 1000 W, with core logic voltages below 1 V and peak current demand beyond 1000 A.

With operating currents exceeding 1000 A, the high power distribution network (PDN) resistance in existing two-stage lateral power delivery (LPD) solutions (e.g., the power delivery solution for the NVIDIA H100 tensor core GPU [4]) can cause significant voltage drops and unacceptable PDN conduction losses. These issues severely limit processor performance, reduce system energy efficiency, and impede data center decarbonization efforts. Furthermore, the low efficiency resulting from these losses requires larger thermal management systems, which currently pose a bottleneck to system densification.

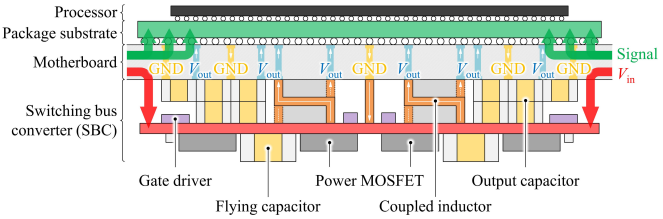


Fig. 1: Single-stage VPD with the presented SBC.

As power levels increase, modern data centers are gradually replacing the legacy 12-V dc bus with the 48-V bus for greatly reduced power distribution losses (i^2R losses). This significantly complicates the design of voltage regulation modules (VRMs) responsible for 48 V to point-of-load (PoL) power conversion with a quadrupled voltage conversion burden. Beyond the large conversion ratio of 48-to-1 or higher, VRMs for next-generation ultra-high-power processors must deliver ultra-high current (hundreds of amperes or even beyond 1000 A) at low voltages ($\leqslant$ 1.0 V) while achieving high efficiency, high power density, and fast dynamic response simultaneously.

To address these challenges, multiple academic works have been proposed for 48-V-to-PoL conversion in data center applications, including transformer-based solutions [5]–[10] and hybrid switched-capacitor (SC) solutions [11]–[25]. As a single-stage hybrid SC voltage regulator for 48-V-to-PoL conversion, the switching bus converter (SBC) [23], [24] demonstrates outstanding theoretical potential and hardware performance, enabled by improved intermediate bus architecture, increased SC stage conversion ratio, optimized gate drive circuitry, and customized coupled magnetics.

This work focuses on the high-density and low-profile implementation of the SBC topology to address the above-mentioned challenges in 48-V-to-PoL data center power conversion with a single-stage vertical power delivery (VPD) solution, as illustrated in Fig. 1. In this single-stage VPD solution, the presented SBC is placed on the bottom side of the motherboard directly underneath the processor, allowing it to deliver high current vertically to the processor on the top

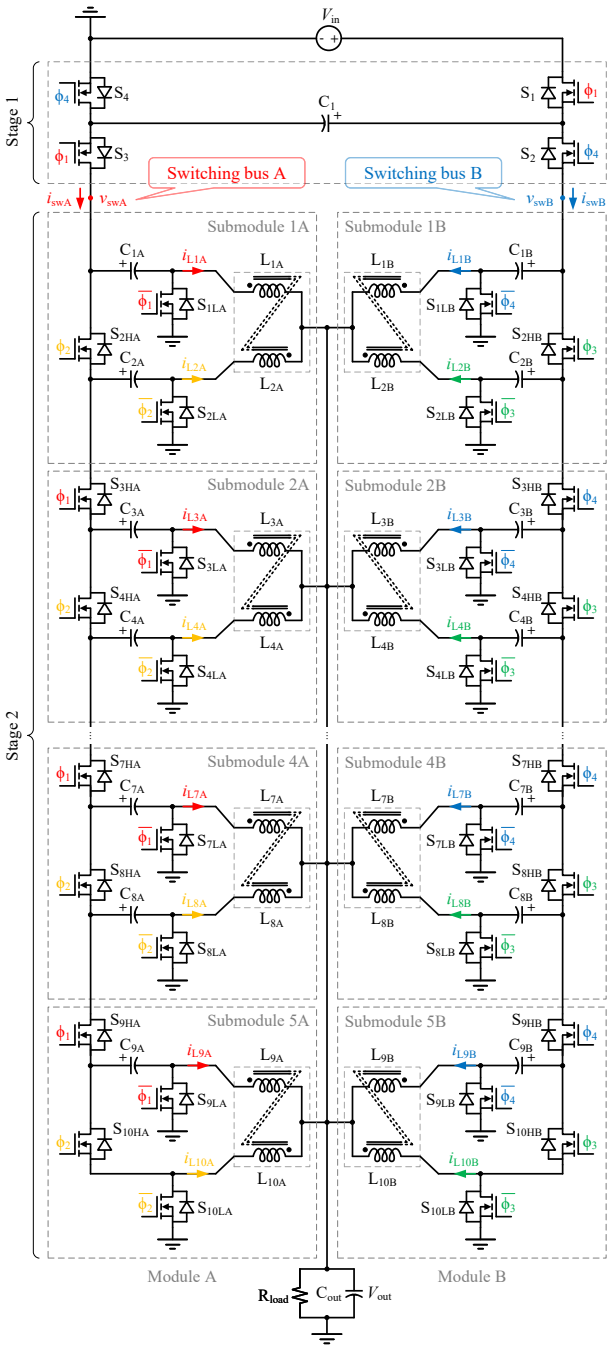


Fig. 2: Schematic of the switching bus converter.

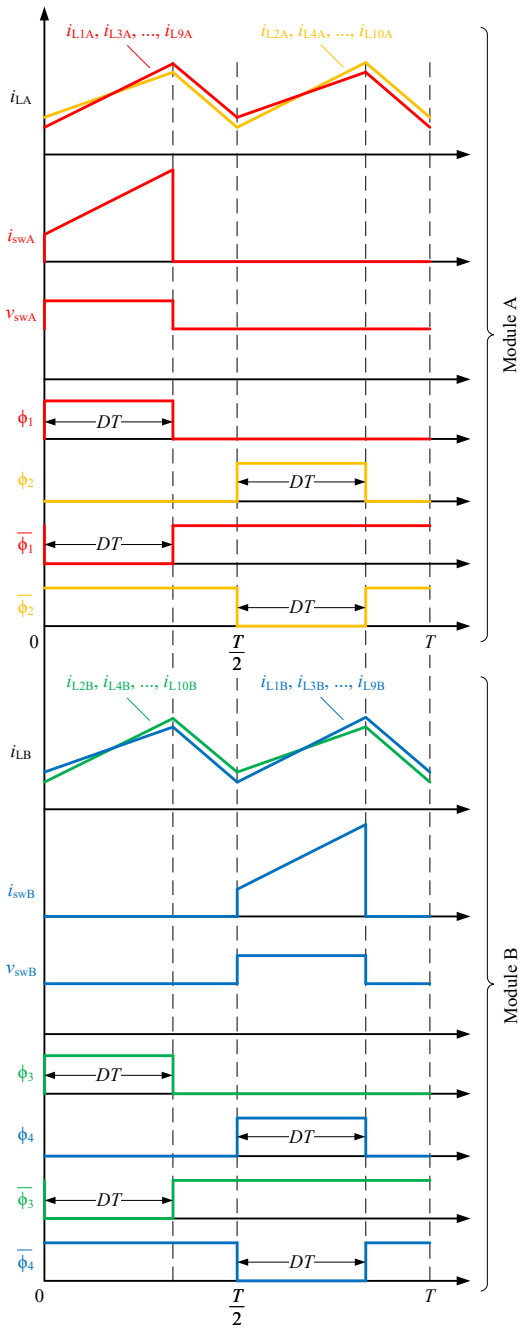


Fig. 3: Control signals of the switching bus converter.

side through vias. Compared to the existing two-stage LPD solutions, the presented single-stage VPD solution greatly reduces the PDN size and losses, and saves the valuable topside area on the motherboard for high-speed communication and high bandwidth memory (HBM). In addition to an overall small converter size, stringent height limitations (e.g., < 5 mm) are required for the solution in this application due to connector heights. Moreover, merging two conversion stages into one single stage reduces total power conversion losses and eliminates the need for dc bus capacitors, which effectively improves overall system efficiency and power density.

II. Circuit Topology and Operating Principles

Fig. 2 shows the schematic drawing of the SBC, which is composed of a 2-to-1 SC front-end (i.e., Stage 1) and two 10-to-1 series-capacitor-buck (SCB) modules (i.e., Modules A and B in Stage 2) merged through two switching buses (i.e., Switching buses A and B). As illustrated in Fig 3, each SCB module consists of five submodules and operates in a two-phase fashion with a phase shift of $180°$ between neighboring branches, and therefore, the adjacent two inductors in each submodule are implemented as a two-phase coupled inductor.

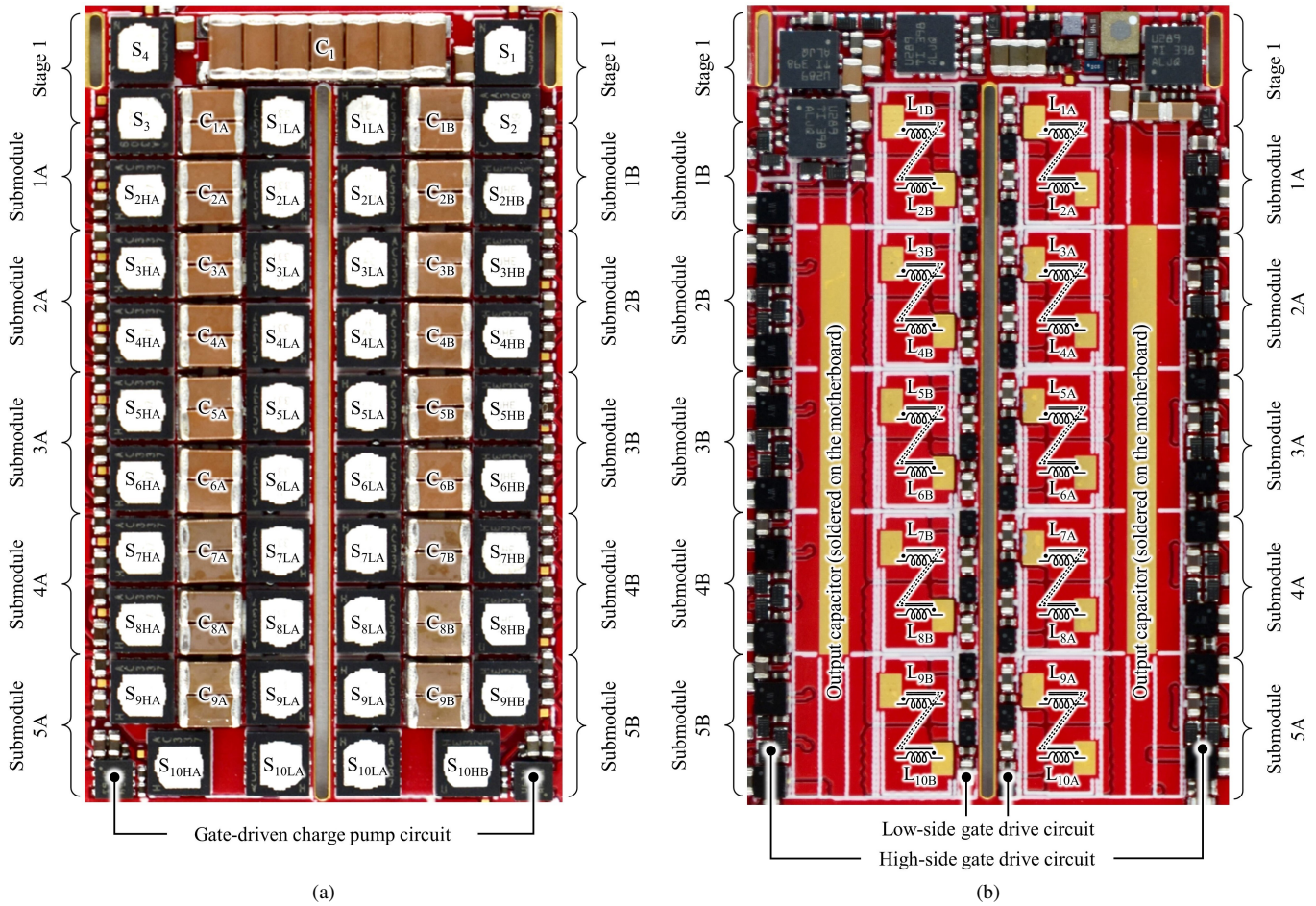


Fig. 4: Photographs of the hardware prototype. Dimensions: $1.60 \times 0.945 \times 0.185$ in^3 ($40.7 \times 24.0 \times 4.7$ mm^3). (a) Top view. (b) Bottom view.

The operating principles and main advantages of the SBC have been explained in detail in [23], [24]. The intermediate buses are referred to as *switching buses* since the bus voltages v_{swA} and v_{swB} always switch between two voltage levels rather than being dc. As explained in [23], [24], compared to the existing dc-bus-based architecture, the switching-bus-based architecture does not require decoupling capacitors to maintain a stiff dc bus voltage, reduces the number of switches with redundant switches removed, and ensures complete soft-charging operation of all flying capacitors. In addition, the two-phase operation of the SCB modules greatly increases the effective conversion ratio of the SC stage compared to the conventional multi-phase control scheme, which enables higher efficiency and higher power density. Moreover, all inductor currents and capacitor voltages are naturally balanced because of the negative feedback mechanism of the SCB converter, as explained in [26] and [23].

III. Hardware Implementation

A 48-V-to-sub-1-V hardware prototype was designed and constructed to adhere to a stringent height constraint of less than 5 mm, while achieving a current density exceeding 0.5 A/mm^2. Fig. 4 shows annotated photographs of the prototype, with the main circuit components listed in Table I. Power MOSFETs and flying capacitors are placed on the top side of the printed circuit board (PCB), while the coupled inductor and the gate drive circuitry are placed on the bottom side.

As explained in Section II, the two inductors in each SCB submodule are implemented as a two-phase coupled inductor. Fig. 5 illustrates the structure of the coupled inductor customized for this prototype, with its key parameters and operating conditions listed in Table II. The two copper windings are negatively coupled through two pieces of magnetic cores. The top core has a similar shape to an I core with two slots open for the windings. Similarly, the bottom core is modified from an E core with two winding slots. The magnetic cores were fabricated with DMEGC DMR53 Mn-Zn ferrite material [27]. As illustrated in Figs. 5(b) and (c), the current in each winding flows vertically from the switch node (i.e., the node connecting the high-side and low-side switches in each SCB branch) on the bottom side of the PCB to the output node.

Fig. 6 provides an overview of the prototype mounted on a white motherboard. As shown in Fig. 6(b), the coupled inductors are packaged between the red converter board and

TABLE I: Component list of the hardware prototype

Component	Part number	Parameters
MOSFET S_{1-4}	Infineon IQE013N04LM6SC/IQE013N04LM6CGSC	40 V, 1.35 mΩ, dual-side cooling
MOSFET $S_{2HA/B-10HA/B}$	Infineon IQE004NE1LM7SC/IQE004NE1LM7CGSC	15 V, 0.45 mΩ, dual-side cooling
MOSFET $S_{1LA/B-10LA/B}$	Infineon IQE004NE1LM7CGSC	15 V, 0.45 mΩ, dual-side cooling
Flying capacitor C_1	TDK C3216X7R1H106K160AC	X7R, 50 V, 10 µF*×7 (in parallel)
Flying capacitor $C_{1A/B-6A/B}$	TDK C3216X6S1E226M160AC	X6S, 25 V, 22 µF*×2 (in parallel)
Flying capacitor $C_{7A/B-9A/B}$	TDK C3216X5R1A107M160AC	X5R, 10 V, 100 µF*×2 (in parallel)
Input capacitor C_{in}	TDK C2012X5R2A475K125AC	X5R, 100 V, 4.7 µF*×15 (in parallel)
Output capacitor C_{out}	Murata GRM21BC80G107ME15L	X6S, 4 V, 100 µF*×242 (in parallel)
Gate driver in Stage 1	Texas Instruments UCC27289	3-A peak source current, 3-A peak sink current
Low-side gate driver in Stage 2	Texas Instruments LMG1020	7-A peak source current, 5-A peak sink current
High-side gate driver in Stage 2	EPC uP1966E	0.4-Ω pull-down resistance, 0.7-Ω pull-up resistance

* The capacitance listed in this table is the nominal value before dc derating.

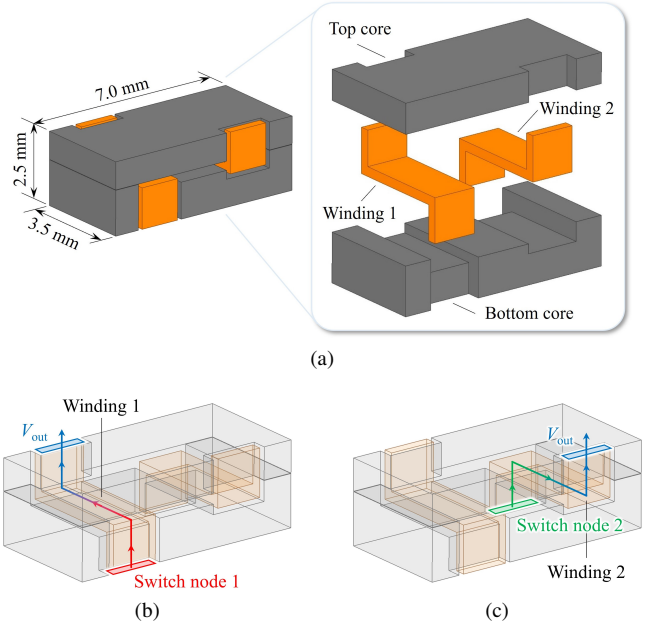


Fig. 5: Custom two-phase coupled inductor. (a) Structure of the coupled inductor. Dimensions: $7.0 \times 3.5 \times 2.5$ mm^3. (b) Current path in winding 1. (c) Current path in winding 2.

TABLE II: Key parameters and operating conditions of the two-phase coupled inductor

Parameter	Value
Coupling coefficient	-0.87
Per-phase steady-state inductance	58.8 nH
Per-phase transient inductance	19.9 nH
Per-phase dc resistance	0.227 mΩ
Nominal output voltage	0.65 V
Switching frequency	600 kHz
Nominal duty ratio	0.27
Per-phase peak-to-peak current ripple	13.4 A
Per-phase average current at full load	30 A
Per-phase saturation current	42 A
Height	2.5 mm

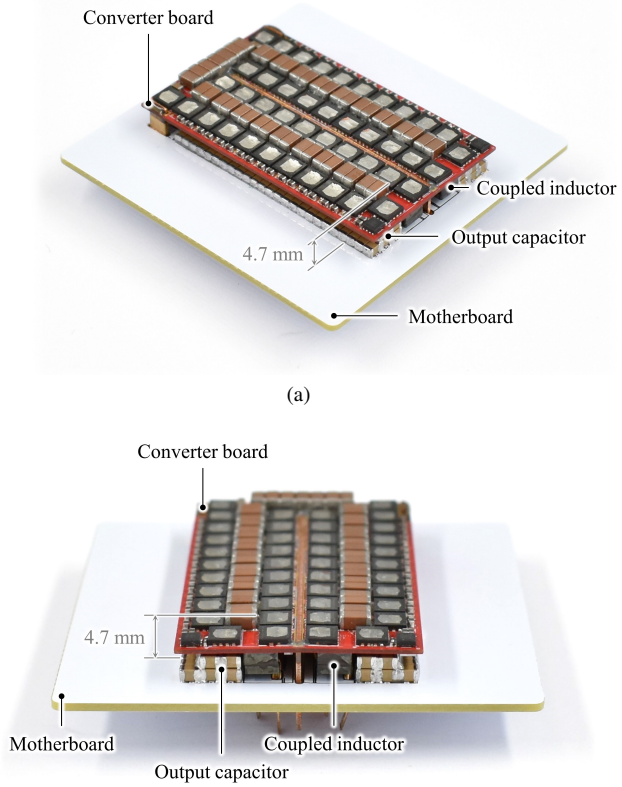


Fig. 6: (a) Overview of the hardware prototype mounted on a white motherboard. The height of the prototype is 4.7 mm. (b) Coupled inductors and output capacitors are packaged between the red converter board and the white motherboard.

the white motherboard. It is worth noting that the copper windings not only function as part of the coupled inductors but also serve as the connection between the SBC and the motherboard, eliminating the need for additional output connectors and reducing the resistance on the output current path. The assembly of the SBC and the processor motherboard is demonstrated in Fig. 7, where the coupled inductors deliver the output current to the motherboard, and a 0.4-mm thick copper sheet in the middle of the red converter board provides the return path for the ground node at the output. This compact, vertically stacked structure reduces the area of the hardware prototype and increases its current density.

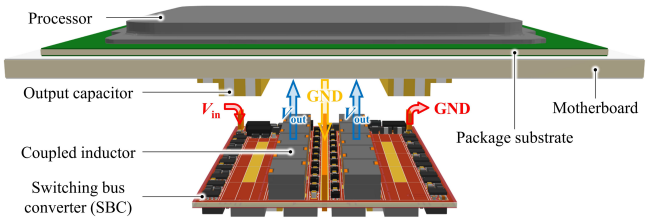


Fig. 7: 3D rendering of the assembly of the SBC and the processor motherboard.

TABLE III: Key parameters and test conditions of the hardware prototype

Parameter	Value
Nominal input voltage	48 V
Nominal output voltage	0.65 V
Switching frequency	600 kHz
Gate drive voltage of Stage 1	8.0 V
High-side gate drive voltage of Stage 2	6.6 V
Low-side gate drive voltage of Stage 2	5.3 V
Height	4.7 mm
Width	24.0 mm
10-branch configuration	
Length	40.7 mm
Full-load output current	600 A (30 A/phase)
Current density	0.614 A/mm^2
8-branch configuration	
Length	33.3 mm
Full-load output current	400 A (25 A/phase)
Current density	0.501 A/mm^2

IV. Experimental Results and Performance Comparison

The hardware prototype presented in Section III was tested with an output current of up to 600 A for performance validation. Table III lists the key parameters and test conditions of the hardware prototype, with the experimental setup for automated efficiency measurement shown in Fig. 8. A 1000-A Chroma 63206A-60-1000 dc electronic load was used to sink and measure the output current of the converter. The input voltage, input current, and output voltage were measured with a high-precision Yokogawa WT3000E power analyzer. A FLIR thermal camera was used to monitor the surface temperature of the prototype.

A. Experimental Results

The hardware prototype was tested in two configurations: a 10-branch configuration and an 8-branch configuration. Figs. 2 and 4 show the 10-branch configuration, where each SCB module consists of ten inductor branches. In addition, the hardware prototype was also reconfigured into the 8-branch configuration with eight inductor branches in each SCB module. This reconfiguration was achieved by removing all switches and flying capacitors in Submodules 5A and 5B in Fig. 2 and short-circuiting flying capacitors C_{8A} and C_{8B} in Submodules 4A and 4B. As will be mentioned in Section IV-B, most state-of-the-art academic works on 48-V-to-PoL conversion were designed for an output voltage of 1 V. To compare the hardware performance of this work with that of the state-of-the-art, the prototype was reconfigured in the 8-branch configuration to maintain an output voltage of 1 V across the entire load range. The 10-branch configuration was unable to supply the 1-V output voltage at full load due to its duty ratio limit. The maximum duty ratio of the SBC, regardless of its configuration, is 0.5. Although the prototype was evaluated in the 8-branch configuration for performance comparison at an output voltage of 1 V, it is worth noting that it was originally designed and optimized for the 10-branch configuration with an output voltage of 0.65 V.

Fig. 9 presents the measured power stage efficiency (excluding the gate drive loss) and system efficiency (including the gate drive loss) of the hardware prototype at 48-V input voltage and sub-1-V output voltages, with the key performance

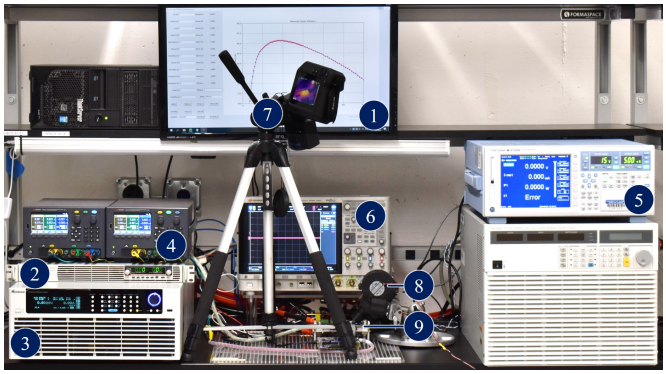
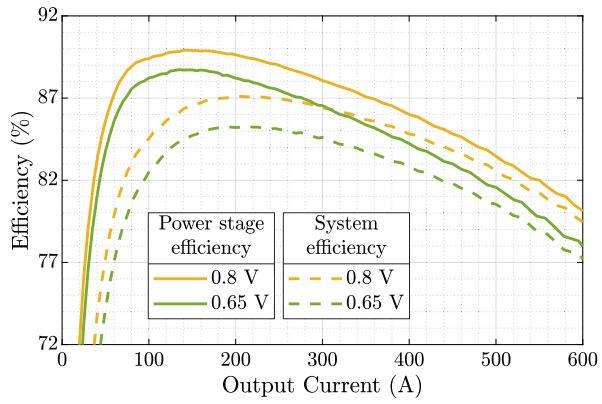


Fig. 8: Experimental setup for automated efficiency measurement with remote control of equipment. List of equipment: ① Monitor for displaying measurement results. ② GW Instek PSU 60-25 programmable dc power supply (60 V, 25 A). ③ Chroma 63206A-60-1000 dc electronic load (60 V, 1000 A). ④ Keysight E36312A triple output programmable dc power supply used to power the control and gate drive circuitry. ⑤ Yokogawa WT3000E precision power analyzer used to measure the input voltage, input current, and output voltage. ⑥ Keysight oscilloscope. ⑦ FLIR thermal camera. ⑧ CUI Devices CBM-979533B-154 dc blower. ⑨ Hardware prototype under test.

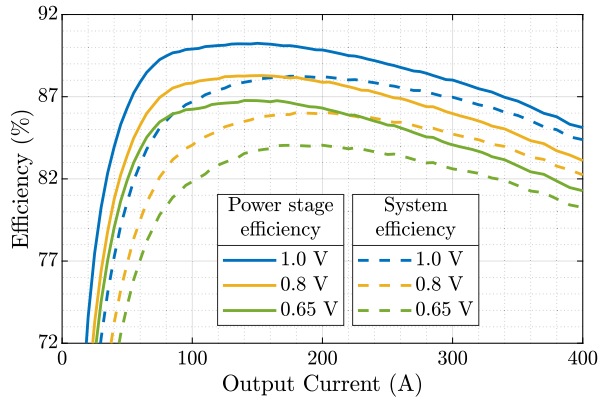
TABLE IV: Measured performance of the hardware prototype in the 10-branch and 8-branch configurations with various output voltages

Output Voltage	Power Stage Efficiency	System Efficiency†	Power Density‡
10-branch configuration			
0.8 V	Peak efficiency: 89.9% Full-load efficiency: 80.1%	87.1% 79.5%	1713 W/in^3
0.65 V	Peak efficiency: 88.7% Full-load efficiency: 78.0%	85.3% 77.2%	1392 W/in^3
8-branch configuration			
1.0 V	Peak efficiency: 90.2% Full-load efficiency: 85.1%	88.2% 84.4%	1745 W/in^3
0.8 V	Peak efficiency: 88.3% Full-load efficiency: 83.1%	86.0% 82.2%	1396 W/in^3
0.65 V	Peak efficiency: 86.8% Full-load efficiency: 81.3%	84.1% 80.3%	1134 W/in^3

† Gate drive loss is included in the calculation of system efficiency.
‡ Power densities are calculated with the box volume of each converter, which is measured as the smallest rectangular box that can contain the hardware prototype, including the gate drive circuitry.



(a)



(b)

Fig. 9: Measured power stage efficiency (excluding the gate drive loss) and system efficiency (including the gate drive loss) of the hardware prototype at 48-V input voltage and sub-1-V output voltages. (a) 10-branch configuration. (b) 8-branch configuration.

figures summarized in Table IV. In the 10-branch configuration with an output voltage of 0.65 V, it was tested up to an output current of 600 A and achieved 88.7% peak power stage efficiency at a 140-A output current and 78.0% full-load power stage efficiency at a 600-A output current. With the gate drive loss included, it achieved 85.3% peak system efficiency at a 215-A output current and 77.2% full-load system efficiency. Additionally, the prototype achieved a power density of 1392 W/in^3 by box volume (the volume of the best-fit cuboid encompassing the entire solution, including the gate drive circuitry) and a current density of 0.614 A/mm^2 at the 600-A full-load current current. Fig. 10 shows the steady-state thermal image of the prototype in the 10-branch configuration, cooled by a 44.2-CFM blower and running continuously at 300-A output current. It should be noted that the current hardware prototype does not incorporate any heat sinks, heat spreaders, or other types of thermal management systems. Given the flatness of the prototype, a custom cold plate can be designed and attached to the top side of the converter to provide liquid cooling for the power MOSFETs and leverage the great heat dissipation capability of their dual-side cooling package.

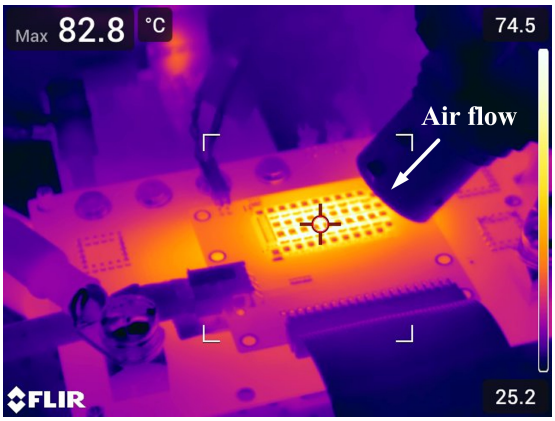


Fig. 10: Steady-state thermal image of the prototype in the 10-branch configuration cooled by a 44.2-CFM blower. (V_{in} = 48 V, V_{out} = 0.65 V, I_{out} = 300 A).

In the 8-branch configuration with an output voltage of 1.0 V, the hardware prototype was tested up to an output current of 400 A, achieving a power density of 1745 W/in^3 and a current density of 0.501 A/mm^2. It achieved 90.2% peak power stage efficiency at a 135-A output current and 85.1% full-load power stage efficiency. Additionally, it achieved 88.2% peak system efficiency at a 180-A output current and 84.4% full-load system efficiency, with the gate drive loss included.

B. Performance Comparison With the State of the Art

Table V compares the performance of this work in the 10-branch configuration with that of the state-of-the-art academic works for 48-V-to-0.8-V conversion presented in previous literature. It can be seen that this work achieves excellent efficiency and power density while adhering to the 5-mm height limit and the 0.5-A/mm^2 current density requirement simultaneously. In addition, as explained in Section IV-A, the hardware prototype was also reconfigured into the 8-branch configuration for performance comparison with prior works at an output voltage of 1 V. It should be noted that the prototype was originally designed and optimized for the 10-branch configuration with an output voltage of 0.65 V. Therefore, its measured performance in the 8-branch configuration does not represent the full potential of the SBC topology. For a nominal output voltage of 1 V and the 8-branch configuration, the coupled inductors should be redesigned to achieve improved performance due to the changes in their voltage stress and nominal duty ratio. Nevertheless, as shown in Table VI, even in the sub-optimal 8-branch configuration and an increased output voltage of 1 V, this work still achieves outstanding performance, which demonstrates its great potential for processor VPD applications.

V. Conclusion

This paper presents a compact SBC for single-stage VPD, with a height of 4.7 mm and a current density of 0.614 A/mm^2. The SBC consists of a 2-to-1 SC front-end and two 10-branch SCB modules that are merged through two switching buses. Compared to the existing dc-bus-based architecture, the

TABLE V: Performance comparison between this work in the 10-branch configuration and the state-of-the-art academic works for 48-V-to-0.8-V conversion

Year	Reference	Full-Load Output Current	Operating Frequency	Height	Current Density	Power Density†	Power Stage Efficiency	System Efficiency‡
2024	This work (SBC-VPD, 10-branch configuration)	600 A (30 A/phase)	600 kHz	4.7 mm	0.614 A/mm^2 (0.410 A/mm^2 at 400 A)	1713 W/in^3 (1142 W/in^3 at 400 A)	Peak efficiency: 89.9% Efficiency at 400 A: 86.0% Full-load efficiency: 80.1%	87.1% 84.8% 79.5%
2024	Mini-LEGO [22]	210 A (17.5 A/phase)	1.5 MHz	8.4 mm	0.625 A/mm^2	975 W/in^3	Peak efficiency: 86.0% Full-load efficiency: 84.1%	82.2% 81.8%
2022	VIB [18]	425 A (26.6 A/phase)	417 kHz	11.0 mm	0.147 A/mm^2	175 W/in^3	Peak efficiency: 94.5% Full-load efficiency: 88.6%	N/A N/A
2022	LEGO [16]	450 A (37.5 A/phase)	1 MHz	16.65 mm	0.298 A/mm^2	235 W/in^3	Peak efficiency: 89.8% Full-load efficiency: 84.7%	86.8% 83.5%

† Power densities are calculated with the box volume of each converter, which is measured as the smallest rectangular box that can contain the hardware prototype, including the gate drive circuitry.
‡ Gate drive loss is included in the calculation of system efficiency.

TABLE VI: Performance comparison between this work in the 8-branch configuration and the state-of-the-art academic works for 48-V-to-1-V conversion

Year	Reference	Full-Load Output Current	Operating Frequency	Height	Current Density	Power Density†	Power Stage Efficiency	System Efficiency‡
2024	This work (SBC-VPD, 8-branch configuration)	400 A (25 A/phase)	600 kHz	4.7 mm	0.501 A/mm^2 (0.375 A/mm^2 at 300 A)	1745 W/in^3 (1309 W/in^3 at 300 A)	Peak efficiency: 90.2% Efficiency at 300 A: 88.0% Full-load efficiency: 85.1%	88.2% 87.0% 84.4%
2024	Dual-inductor SBC* [25]	50 A (25 A/phase)	1 MHz	2.6 mm	0.321 A/mm^2	2020 W/in^3	Peak efficiency: 91.9% Full-load efficiency: 88.0%	90.1% 87.3%
2024	20-to-1 SBC [24]	1500 A (37.5 A/phase)	220 kHz	6.2 mm	0.287 A/mm^2	759 W/in^3	Peak efficiency: 94.1% Full-load efficiency: 86.0%	92.7% 85.7%
2024	16-to-1 SBC [23]	500 A (31.3 A/phase)	150 kHz	7.3 mm	0.207 A/mm^2	464 W/in^3	Peak efficiency: 94.7% Full-load efficiency: 86.4%	93.4% 86.1%
2024	Mini-LEGO [22]	240 A (20 A/phase)	1.5 MHz	8.4 mm	0.714 A/mm^2	1390 W/in^3	Peak efficiency: 87.1% Full-load efficiency: 84.1%	84.1% 82.3%
2024	SDIH [21]	116 A (58 A/phase)	750 kHz	3.6 mm	0.145 A/mm^2	663 W/in^3	Peak efficiency: 83.5% Full-load efficiency: 73.8%	81.4% 73.2%
2023	MSC [20]	220 A (27.5 A/phase)	400 kHz	7.0 mm	0.265 A/mm^2	607 W/in^3	Peak efficiency: 92.9% Full-load efficiency: 86.3%	91.1% 85.8%
2022	Dickson^2 [19]	270 A (30 A/phase)	280 kHz	6.45 mm	0.142 A/mm^2	360 W/in^3	Peak efficiency: 93.8% Full-load efficiency: 88.4%	91.6% 87.7%
2022	VIB [18]	450 A (28.1 A/phase)	417 kHz	11.0 mm	0.156 A/mm^2	232 W/in^3	Peak efficiency: 95.2% Full-load efficiency: 89.1%	93.3% 88.1%
2022	MLB [17]	60 A (30 A/phase)	250 kHz	7.8 mm	0.125 A/mm^2	263 W/in^3	Peak efficiency: 92.7% Full-load efficiency: 88.6%	91.5% 88.4%
2022	LEGO [16]	450 A (37.5 A/phase)	1 MHz	16.65 mm	0.298 A/mm^2	294 W/in^3	Peak efficiency: 91.1% Full-load efficiency: 85.7%	88.4% 84.8%
2020	Crossed-coupled QSD buck [12]	40 A (20 A/phase)	125 kHz	N/A	N/A	100 W/in^3§	Peak efficiency: 94.5% Full-load efficiency: 91.1%	N/A N/A
2020	Sigma [9]	80 A	1 MHz	4.0 mm	0.127 A/mm^2	420 W/in^3	Peak efficiency: 94.0% Full-load efficiency: 92.5%	N/A N/A

† Unless otherwise specified, power densities are calculated with the box volume of each converter, which is measured as the smallest rectangular box that can contain the hardware prototype, including the gate drive circuitry.
‡ Gate drive loss is included in the calculation of system efficiency.
* The dual-inductor SBC requires dual-side cooling.
§ The power density of the cross-coupled QSD buck converter is calculated with the power component volume.

SBC's switching-bus-based architecture does not require dc bus capacitors, reduces the number of switches, and ensures complete soft-charging operation. To validate the performance of the proposed converter, a 48-V-to-sub-1-V hardware prototype was designed and built with two-phase coupled inductors. The coupled inductors were customized for VPD, with their windings not only functioning as part of the coupled inductors but also serving as the connection between the SBC and the processor motherboard. The hardware prototype was tested up to a 600-A output current and achieved excellent performance

compared to the state-of-the-art academic works for 48-V-to-PoL conversion, demonstrating its great potential for processor VPD.

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