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Design Techniques for High Frequency PAs and VCOs

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Design Techniques for High Frequency PAs and VCOs

A dissertation submitted in partial satisfaction of the
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In Electrical Engineering

by

Farid Shirinfar

2016

ABSTRACT OF THE DISSERTATION

Design Techniques for High Frequency PAs and VCOs

by

Farid Shirinfar

Doctor of Philosophy in Electrical Engineering

University of California, Los Angeles, 2016

Professor Sudhakar Pamarti, Chair

TODAY's content-centric mobile world demands Gigabit-per-second ($Gbps$) wireless communication systems. With sub-10GHz radio frequencies cluttered with existing wireless infrastructures such as 2.4GHz and 5GHz Wi-Fi and a multitude of LTE bands in the 1-2GHz range, focus has shifted to microwaves and mm-waves. The inverse relation between frequency and wavelength (and thus antenna size) differentiates mm-wave solutions in terms of size. For example, a 16-element antenna array only takes about 1.5cm^2 at 60GHz. The pitfall, however, is the degraded active device performance at these high frequencies. Innovations at circuit-level and architecture-level are thus necessary. The dominant non-idealities that limit the performance of such radios in CMOS are the phase noise of the voltage controlled oscillator (VCO), the maximum output power of power amplifier (PA) limited by device breakdown voltage, and the non-linear behavior of the PA. Circuit and architecture level innovations presented in this research improve state-of-the-art performance in those areas.

To address the phase noise limitation, a mm-wave VCO architecture with low phase noise and large tuning range is presented. MM-wave systems rely on large channel bandwidths (e.g. 1.7GHz per channel, 7GHz total) to achieve high data rates. Channel selection using varactors and/or switched-capacitors suffers from poor phase noise performance due to the low quality factor of those elements at mm-waves. In the proposed architecture, the required frequency tuning range is divided amongst four narrow-band clusters of VCOs. Each cluster of VCOs can achieve lower phase noise due to the reduced frequency tuning range requirement. Phase noise of each cluster is further improved by using multiple cores of VCOs connected in parallel with differential transmission lines. The VCO achieves a phase noise of -101.8 dBc/Hz at 1 MHz offset with an FOM of -182dB/Hz and over 12.6% frequency tuning range (50.7 GHz to 57.5 GHz).

Another focus of this research is to improve the power amplifier (PA) performance (output power, linearity, and efficiency). Innovations in power combining techniques enable us to achieve the highest reported saturated power level of 22.6dBm in CMOS at 60GHz. Stacking transistors as a second remedy to improve the output power of the PA is considered and trade-offs in gain, reliability, and output power are treated analytically and an optimal stacking strategy for mm-wave PAs is presented. A simulation-based comparison shows the superiority of the proposed optimal stacking approach compared with the conventional stacking approach for a 60GHz SiGe PA.

A wideband self-contained PA linearization technique is presented to address mm-wave PA linearity challenges. The proposed Adaptive Gain and Phase Adjustment (AGPA) linearization technique compensates for both AM-AM and AM-PM distortion of the PA for large channel bandwidths of hundreds of megahertz at mm-waves. The gain and phase linearization

loop consists of an envelope detector, an Analog Mapping Core (AMC), and a variable RC feedback network. The detection and adjustment loop has a low group delay and thus enables one of the largest linearization bandwidths published. AGPA improves the OP1dB of a stacked mm-wave PA by 2.8dB (from 9.5dBm to 12.3dBm) and reduces the IM3 products by 3dB at 8dBm output power with a tone spacing of 200MHz. Power Added Efficiency (PAE) at OP1dB is improved from 6.5% to 10.5% by enabling AGPA at 57GHz.

The dissertation of Farid Shirinfar is approved.

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b. Professional Experience

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2009 (June-September) Sony Research & Development, Tokyo, Japan

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Shirinfar, F.; Nariman, M.; Sowlati, T.; Rofougaran, M.; Rofougaran, R.; Pamarti, S., "A fully integrated 22.6dBm mm-Wave PA in 40nm CMOS," Radio Frequency Integrated Circuits Symposium (RFIC), 2013 IEEE , vol., no., pp.279,282, 2-4 June 2013

Shirinfar, F.; Nariman, M.; Sowlati, T.; Rofougaran, M.; Rofougaran, R.; Pamarti, S., "A multichannel, multicore mm-Wave clustered VCO with phase noise, tuning range, and lifetime reliability enhancements," Radio Frequency Integrated Circuits Symposium (RFIC), 2013 IEEE , vol., no., pp.235,238, 2-4 June 2013

Nariman, M.; Shirinfar, F.; Pamarti, S.; Rofougaran, M.; Rofougaran, R.; De Flaviis, F., "A compact millimeter-wave energy transmission system for wireless applications," Radio Frequency Integrated Circuits Symposium (RFIC), 2013 IEEE , vol., no., pp.407,410, 2-4 June 2013

d. Patents

“Low phase noise voltage controlled oscillator,” U.S. Patent #8,933,757

“Low inductance transformer,” U.S Patent #9,048,018

“Systems and methods for maintaining power amplifier performance, ” U.S. Patent #9,065,387

“Reflective beamforming for performing chip-to-chip and other communications,” U.S Patent #8,977,208

“On-chip distributed power amplifier and on-chip or in-package antenna for performing chip-to-chip and other communications,” U.S. Patent #8,918,064

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Chapter 1

Introduction

ADVANCES in device physics and semiconductor fabrication have dramatically improved the maximum operating frequency of transistors over the years. Today's commercially available semiconductor processes have a unity current gain frequency (f_T) of over 200GHz and a unity power gain frequency (f_{max}) of over 300GHz [5]. Those leaps in operation frequency are realized at the expense of lower voltage swing tolerances, and thus power handling, in each subsequent generation of silicon. This f_{max}/breakdown-voltage trade-off is a recurring challenge in the design of RF front-end circuitry at high frequencies especially for mm-wave PAs and VCOs. As explained in Chapter 2, the achievable phase noise of an oscillator is inversely proportional to the voltage swing. Consequently, a low supply voltage limits the phase noise performance. Similarly, PAs maximum reliable output power is a quadratic function of its maximum allowable voltage swing.

Maximum reliable output power of a PA is limited by the breakdown voltage of its transistors and the value of R_{Load} (1.1).

$$P_{MAX\_SAFE} = \frac{V_{AC_{MAX}}^2}{2 * R_{Load}} \quad (1.1)$$

P_{MAX_SAFE} denotes the maximum reliable power the PA can handle over a specified continuous stress time (T_{Stress}) without significant degradation of performance (e.g. drop in gain, OP1dB, or efficiency). The length of stress time (T_{Stress}) depends on the use case of the product and the duty cycle that the product is ON. For example, a reasonable continuous stress time for consumer electronic products is about six months to one year assuming a five-year lifetime with 20% operational duty cycle.

V_{AC_MAX} is the maximum AC voltage the transistor can handle without significant degradation in performance over T_{Stress}. There is an inverse relation between f_{max} and V_{AC_MAX} (or VDD) (Fig. 1.1). To get reasonable gain from a device, the transistors f_{max} should be at least three to four times the operation frequency. This limits active device selection for high frequency operation to those with a VDD of 0.8V-1.8V (Fig. 1.1). With this voltage swing limitation, P_{MAX_SAFE} is limited to about 10dBm for a single device PA. Increasing this limit has been an area of active research for the past 5-10 years. The two techniques that have shown the most promise are power combing and stacking.

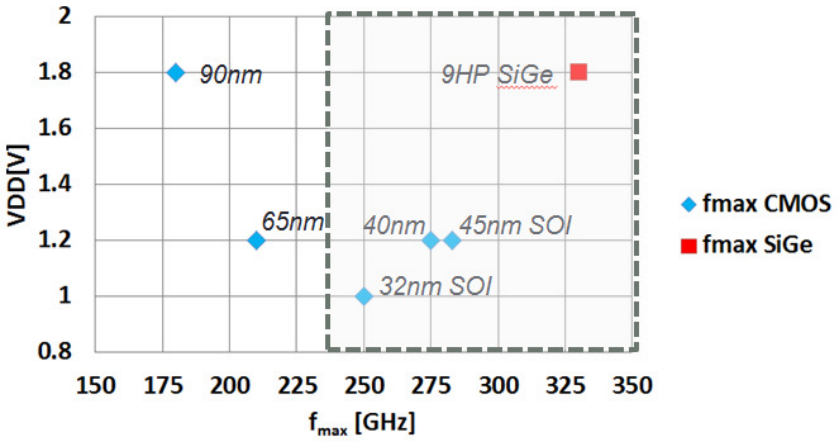


Figure 1.1 f_{max} and VDD of processes suitable for microwave and mm-wave design

Power combining relies on the summation of power from multiple PAs using passive devices. Low loss, compact passive combiners are the essence of this technique. Distributed Active Transformers (DAT), two half-loop transformers, compact Wilkinson combiners, and on-chip T-junction combiners are examples of power combiners that are shown in recent publications [1-4, 6-9]. Figure 1.2 graphically illustrates these approaches. These combiners typically have a loss of 0.7-1dB per combining stage. Figure 1.3 shows the achieved P_{SAT} for recently published work. Most papers report a P_{SAT} of 10-20dBm. Our proposed power combiner presented in chapter 3 of this work achieves the highest reported P_{SAT} of 22.6dBm in standard CMOS.

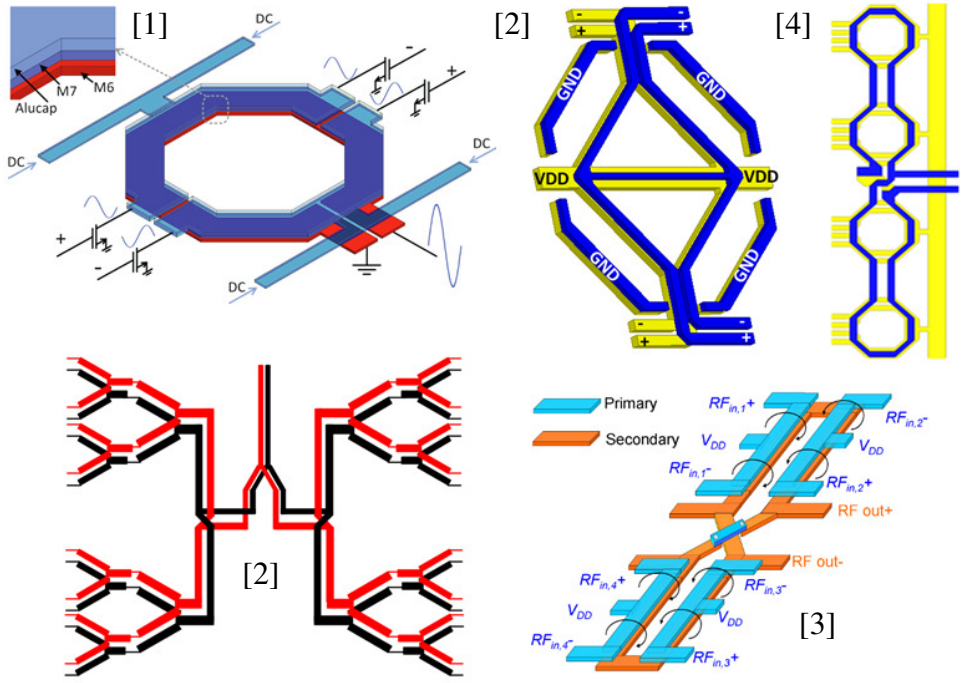


Figure 1.2 Summary of state-of-the-art passive combiners for mm-waves

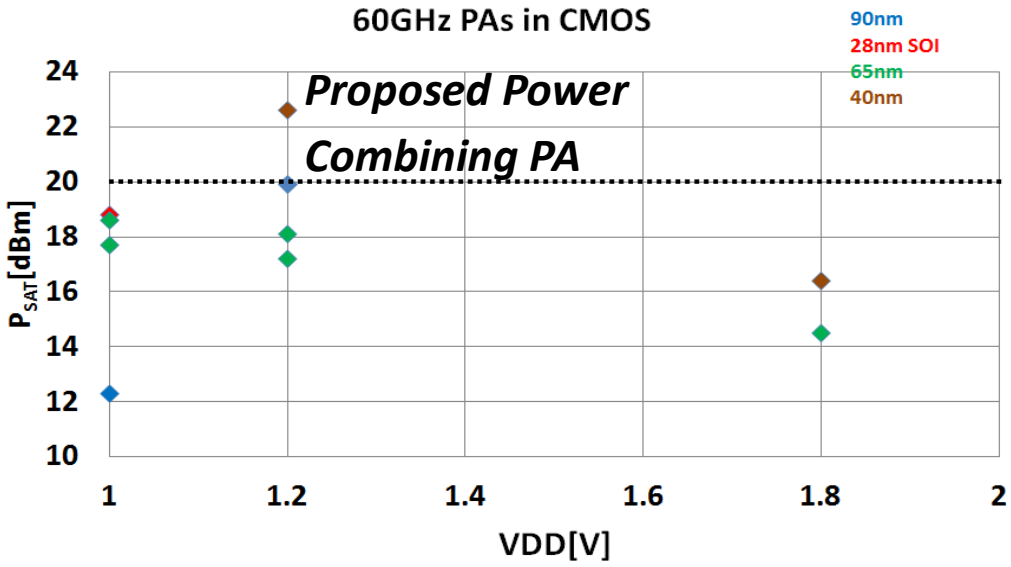


Figure 1.3 Summary of state-of-the-art passive combiners for mm-waves

Stacking is another approach to improve the output power of PAs. It involves stacking transistors with small breakdown voltage to increase the voltage swing handling of the composite

structure. The composite device uses a higher supply voltage due to the division of the swings on multiple devices. Recent publications have shown greater power handling capability compared with single transistor amplifiers at tens of gigahertz in CMOS and SiGe [10-18]. A detailed explanation of stacking approaches is presented in Chapter 4 of this work.

1.1 Organization of Thesis

This work presents new approaches to power combining and stacking for PAs and VCO and a wideband linearization technique for PAs. Chapter 2 presents a clustered VCO architecture suitable for achieving wideband tuning range and low phase noise through the division of bandwidth to multiple VCOs and combining multiple VCO cores to achieve state-of-the-art phase noise performance and figure of merit.

Chapters 3-5 focus on PA design for microwaves and mm-waves. Chapter 3 presents innovations in power combining techniques and structures that leads to the highest reported P_{SAT} in 60GHz CMOS. Chapters 4 introduces stacking and explores the trade-offs in gain/reliability/efficiency in the context of different stacking approaches. An example stacked PA designed with the findings of the analysis shows superior performance compared with the same PA designed with the conventional stacking approaches.

Chapter 5 introduces a novel, large bandwidth linearization technique for PAs with large bandwidths. The linearization technique corrects AM-AM and AM-PM distortion. A stacked 60GHz PA is designed and fabricated with the proposed linearization technique. The linearization technique improves OP1dB of the PA by 2.8dB. Efficiency at OP1dB is increased from 6.5% to 10.5% with the linearization loop turned ON. The proposed approached is suitable

for future massive microwave and mm-wave phased arrays currently under research and development.

Chapter 2

Multicore, Clustered VCO Design

TODAY's content-centric mobile world demands Gigabit-per-second ($Gbps$) wireless communication systems. With sub-10GHz radio frequencies cluttered with existing wireless infrastructures such as 2.4GHz and 5GHz Wi-Fi and a multitude of LTE bands in the 1-2GHz range, focus has shifted to microwaves and mm-waves. In this arena, two sets of systems are now actively pursued: indoor $Gbps$ mm-wave wireless links aimed at residential and office building environments (e.g. IEEE 802.11ad) and outdoor point-to-point links. Indoor links, mainly pursued by consumer electronic providers, will eventually augment the Wi-Fi infrastructure by providing a more efficient (e.g. lower $^{pJ}/_{bit}$) data link. Point-to-point and massive MIMO microwave and mm-wave links are actively pursued for both last-mile backhaul applications where running fiber optical cables are very expensive due to congestion and to provide internet connectivity to remote locations. For such applications, high modulation schemes (64-1024 QAM) and large channel bandwidths are strongly desired to provide a more

bandwidth efficient link. The local oscillator's performance, namely its phase noise and frequency tuning range, is one of the dominant determining factors in the overall radio performance. Achieving both large tuning range and a low phase in CMOS is challenging due to the reasons explained in details in Section 2.1.

Conventional LC-oscillators with an analog varactor used as the primary frequency-tuning element cannot provide the phase noise and tuning range (10%-15%) requirements of such systems due to reasons explained in details in Section 2.1 of this chapter. The main recurring issue is the trade-off between phase noise and tuning range due to low quality factor of varactors and switched capacitors at high frequencies. Capacitance of a varactor and/or switched-capacitor has to be a large portion of the total capacitance of the resonant tank in order to cover wide bandwidths. Low quality factor (Q) of varactors and capacitor banks reduces the overall Q of the tank to less than 10 at mm-waves and thus degrades phase noise. Furthermore, the conventional approach of using a bigger cross-coupled differential pair with a higher current consumption to improve phase noise suffers from a quick diminishing return at mm-waves due to the parasitic capacitance of the device and drop of the associated resonant tank quality factor. Voltage swing across the active device terminals is also limited by the reliability limits. This constrains the maximum current for a given load and introduces another challenge in mm-wave VCO design.

To combat these issues a number of new approaches have been proposed in the literature recently. One approach to combat the varactor's contribution to phase noise is to use a variable inductor [19, 20]. The variable inductor is realized by changing the effective inductance seen looking into the primary of a transformer by placing a variable resistor (an NMOS in triode typically) across the terminals of the secondary loop. This approach, typically called inductive-

tuning, provides a secondary mechanism for frequency tuning and thus reduces the size of the varactor. Coarse-tuning can be done with changing the variable resistor across the inductor and fine-tuning can be done with a smaller varactor. Since the PLL can use the fine-tuning control voltage of the varactor to lock the oscillator to an external crystal, the effective KVCO of the oscillator is also reduced which improves the oscillator's sensitivity to noise on frequency control lines. The limitation of this approach is the effective quality factor of the variable inductor due to the loss of the variable switch.

Isolating the cross-coupled pair parasitic capacitance from the varactor by placing a differential inductor in series with the varactor is another technique [21]. This approach further improves phase noise by separating the voltage swing across the varactor from the voltage swing across the device.

Dividing the total bandwidth to multiple oscillators and multiplexing them is another approach for addressing the tradeoff between phase noise and tuning range [22-25]. Because each individual oscillator covers a smaller bandwidth, it can be designed to have a better phase noise. More oscillators would occupy extra area. In essence, this approach trades off area for performance, which can be acceptable for high performance systems.

The oscillator architecture proposed in this paper utilizes both bandwidth division amongst multiple VCOs (clusters of VCOs) and addresses the scaling issues introduced by enlarging of the cross-coupled pair by using multiple cores of VCOs instead of enlarging a single device. Additionally, using transformers with a 2:1 turn ratio in each core eliminates the need for a mm-wave multiplexer by desensitizing the ON clusters from the loading of the OFF clusters. A 2:1 turn ratio was chosen because higher turn ratios result in a transformer with a low self-resonance that is not suitable for the 60GHz band. Finally, parallel connection of clusters

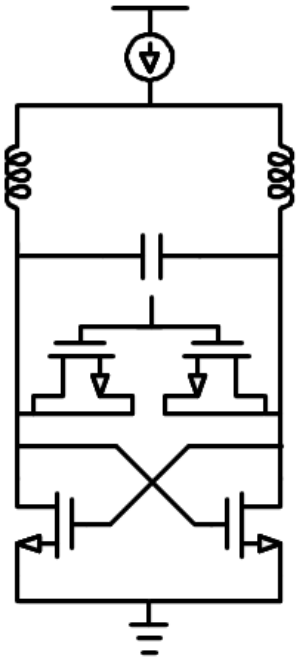
with a symmetric H-shaped transmission-line provides a unified single output for all of the clusters. The basic idea of this architecture was presented in [22]. This paper builds on that idea by explaining the practical challenges of mm-wave oscillators categorically with an example oscillator core and covers in more details the design approach, the OFF cluster desentization and more explanation of cluster coupling, as well as more simulation and measurement data.

2.1 Challenges of MM-Wave Oscillators

Optimal oscillator design at mm-waves needs to address new and unique challenges compared with lower frequency designs. This section summarizes these challenges. In particular, the drop in effective g_m over frequency and the degradation of quality factor of small passives are two unique issues present at mm-waves compared with lower radio frequencies. RC-extracted simulation results of a cross-coupled NMOS oscillator in 40nm CMOS with a lumped inductor with variable Q is used to better illustrate these challenges (Fig. 2.1). The example oscillator is tuned to 50GHz-60GHz with the assumption of a 7GHz IF frequency to alleviate VCO pulling and to cover the 57-67GHz ISM band.

2.1.1 Effective g_m Reduction with Increasing Frequency

In LC oscillators, loss of the LC tank is compensated with an effective negative resistance realized by a transistor (Colpitt oscillator) or a pair of cross-coupled transistors. The equivalent negative resistance is a function of the transconductance of the cross-coupled pair at the frequency of oscillation. At high frequencies, the parasitic capacitance of the device (c_{gd}, c_{gs}, c_{dd}) and the ohmic loss of gate routing (r_g) reduces the effective transconductance of the cross-coupled pair.



Variable Parameters:
I_{DC} (mA)
Inductance (pH)
Q of inductor
Number of fingers for the varactor
Varactor control voltage

Device Size:
Unit-Cell W/L of NMOS: 1µm/40nm
No. of NMOS fingers: 24
Unit-Cell W/L of varactor: 1µm/40nm

Cross-Coupled Pair Parameters (50GHz)
$C_{Cross\text{-}coupled}$=37fF
$R_{Cross\text{-}Coupled}$ = -130Ω

Figure 2.1 Example 40nm NMOS oscillator used to explore unique mm-wave oscillator design challenges

As shown in (2.1), the effective small-signal negative resistance of the cross-coupled pair (R_{in}) is a function of device's small-signal DC transconductance (g_m) and a frequency-dependent degradation term (g_m'). g_m' becomes larger with increasing frequency and thus worsens the effective negative R_{in} of the cross-coupled pair. (2.2) indicates the importance of minimizing r_g for improving R_{in} over frequency. Gate routing of the cross-coupled pair should be done with wide and stacked metals to minimize this parasitic gate resistance. Figure 2.3 shows RC-extracted simulation result of the effective negative resistance (R_{in}) seen by looking into an NMOS cross-coupled pair across frequency normalized to its DC value. The effective negative resistance realized by the device degrades by about 10%-15% at 50-60GHz compared with its value at DC. It should be noted that the drop in R_{in} is quadratic vs. frequency as it can be seen from both (2.2) and Fig. 2.3.

There are two remedies to compensate for the drop in AC transconductance. First, device

can be biased at a higher current density. However, this cannot be done arbitrarily because there is an optimal current density (mA/μm) for the device that achieves optimal RF performance (peak f_T). The second approach to compensate for this drop in transconductance is to increase the device size. A larger device, however, suffers from larger parasitic capacitance, which degrades both tuning range and phase noise as explained later. Consequently, there is a limit to how large a single oscillator can be. As demonstrated later, alternative approaches such as multi-coring and clustering may be superior to the conventional approach of just decreasing the size of the inductor in a single core oscillator.

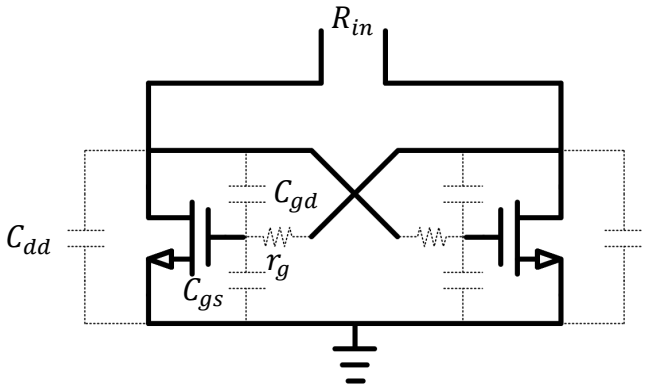


Figure 2.2 Cross-coupled NMOS pair with device parasitic elements

$$R_{in} = \frac{2}{-g_m + g'_m} \tag{2.1}$$

$$g'_m = r_g * \left(\frac{f}{f_t}\right)^2 \left(\frac{r_g}{r_o}\, {g_m}^2 + \left(2\, c_{gd} + c_{gs}\right)^2 (2\pi f_t)^2 + c_{gd}\, r_g\, g_m^2\, 2\pi f_t\right) \tag{2.2}$$

$$f_t = \frac{g_m}{2\pi\left(c_{gd} + c_{gs}\right)} \tag{2.3}$$

$$Normalized\ R_{in} = \frac{R_{in\ AC}}{R_{in\ DC}} \tag{2.4}$$

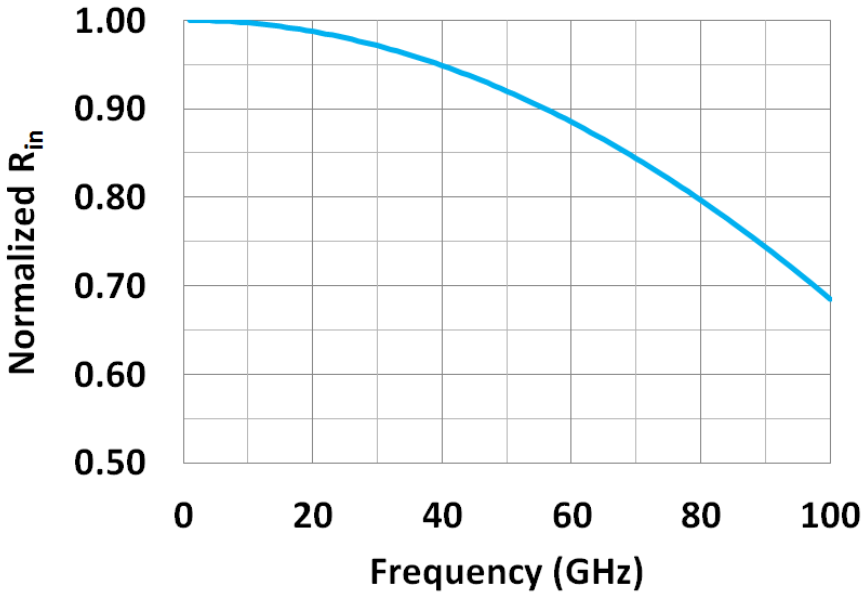


Figure 2.3 Simulated frequency dependence of effective negative resistance (R_{in}) of a cross-coupled pair normalized to its DC value in 40nm CMOS

2.1.2 Small Inductor Quality Factor Degradation

Tank quality factor (Q_T) has an inverse quadratic relation with the oscillator's phase noise as shown in the well-known Leeson's expression (2.5). For optimal phase noise, it is desired to maximize the tank's quality factor.

$$(f_m) = \frac{2kTFR_P}{A^2/2}\left(\frac{f_0}{2Q_T f_m}\right)^2 \tag{2.5}$$

$$Q_T = \left(1/Q_{Ind} + 1/Q_{Varactor}\right)^{-1} \tag{2.6}$$

Mid to large inductors ($L > 50pH$) can be realized on chip with good quality factors ($Q > 20$) at mm-waves (Fig. 2.5). As the size of the inductor reduces, however, the quality factor of the inductor reduces. As the loop radius of the inductor becomes smaller, the parasitic routing becomes comparable to the loop size and thus contributes significantly to the total Ohmic losses of the passive (Fig. 2.4). Furthermore, as the radius of the inductor becomes smaller, the

unwanted mutual coupling between the half turns increases that contributes to larger eddy current losses and reduced skin depth. This further increases the Ohmic loss of the inductor.

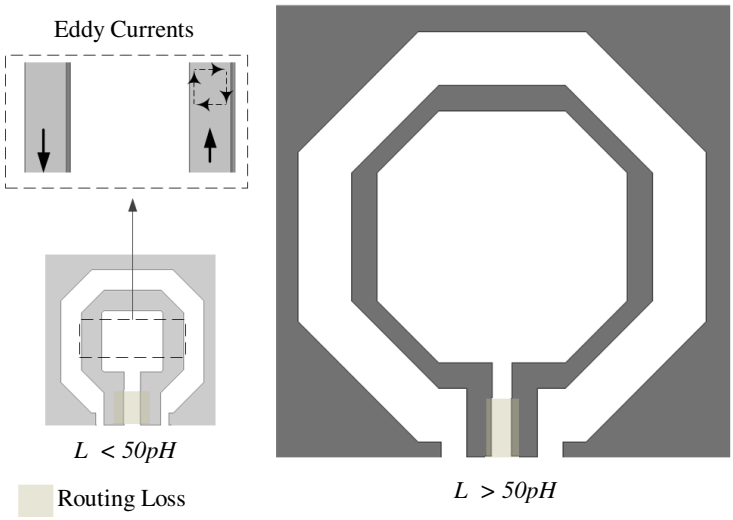


Figure 2.4 Q degradtion of small inductors due to unproportional routing loss and loop induced eddy currents

The drop in Q_{Ind} of small inductors results in diminishing return obtained from increasing the size of the cross-coupled differential pair. A larger device would have a larger parasitic capacitor and thus needs a smaller inductor. A smaller inductor would have a lower Q_{Ind} that defeats the purpose of making the device larger in terms of phase noise. Breaking the large oscillator cross-coupled pair into multi-cores of smaller oscillators addresses this issue as explained in more details later.

A large cross-coupled differential pair with large parasitic capacitance deteriorates the achievable tuning range too. As the fixed effective capacitance of the tank increases with the device, a larger varactor is needed to tune the oscillation frequency (7.7). At mm-waves, the varactor quality factor is limited to about 15 and dominates the quality factor of the tank. Thus, the conventional approach of increasing the device size to improve the phase noise faces diminishing return in terms of phase noise and reduces tuning range at mm-waves. A multi-core

oscillator with small devices would alleviate both problems as discussed later.

$$Tuning\ Range\ (\%) = 2 * \frac{\sqrt{C_{High}} - \sqrt{C_{Low}}}{\sqrt{C_{High}} + \sqrt{C_{Low}}} \tag{2.7}$$

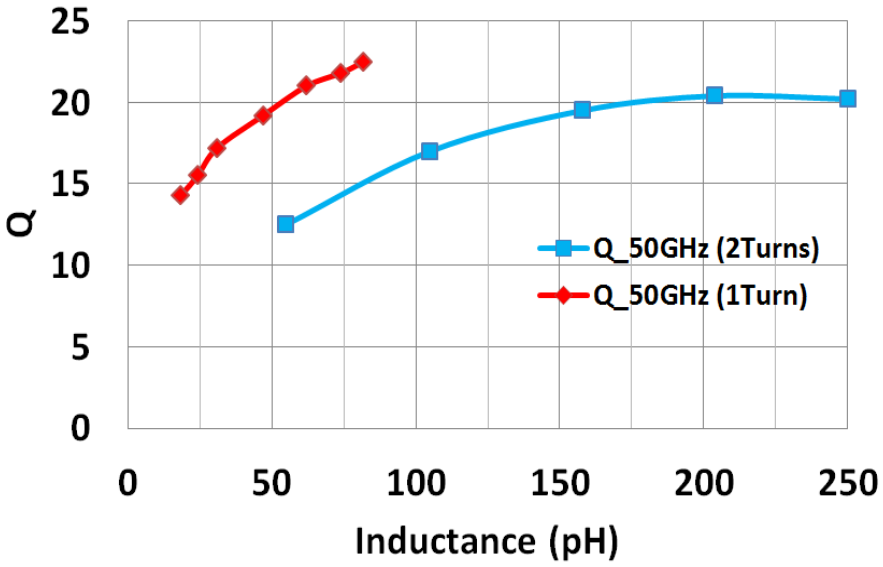


Figure 2.5 Q degradation with inductor size

2.1.3 Tuning Range and Phase Noise Trade-off

One of the advantages of mm-waves is the large available channel bandwidth for transmission of data. Table 2.1 shows the channel bandwidth for the 802.11ad standard. The oscillator needs to cover the center frequencies of each channel with some margin to ensure locking over PVT. The immediate solution to address this tuning range requirement is to use varactors to cover the bandwidth. Since the varactor loss is significant at mm-waves due to large Ohmic losses (Fig. 2.6), a large varactor would reduce the tank's quality factor and thus the phase noise.

Figure 2.7 demonstrates the degradation of phase noise as the tuning range of a cross-coupled CMOS oscillator is increased. For a tuning range of up to 1-1.5GHz, there is not a

significant drop in phase noise. However, as the varactor size is increased phase noise drops significantly.

Another disadvantage of this varactor-based frequency tuning is the resultant large KVCO of the oscillator. CMOS processes suitable for mm-wave systems have a VDD of 0.9-1.2V (Fig. 2.8). Covering 7GHz of frequency tuning with only about 1V of analog control voltage results in a KVCO of 7GHz/V. Consequently, any amplitude noise on the varactor control signal would turn into phase noise.

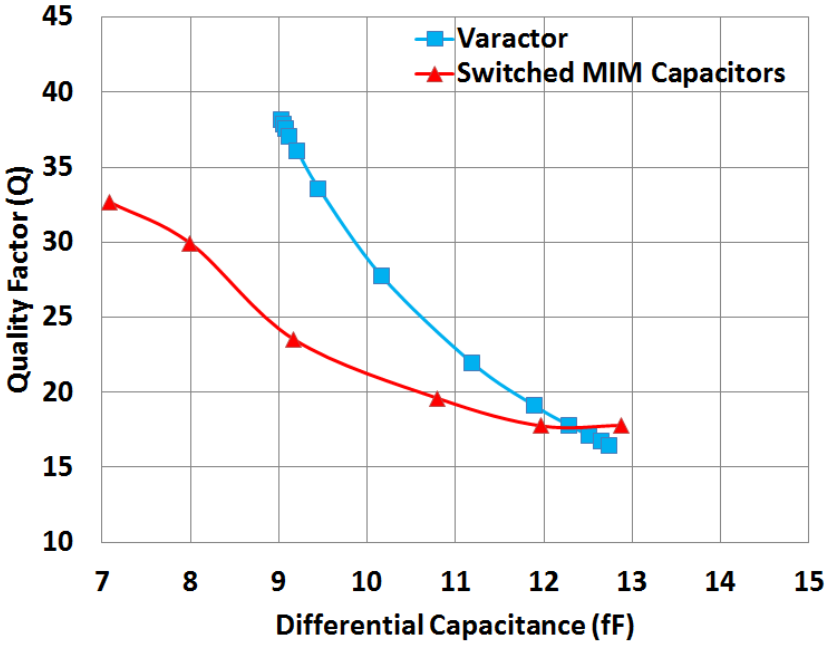


Figure 2.6 Varactor and switched-MIM capacitor quality factor at 50GHz

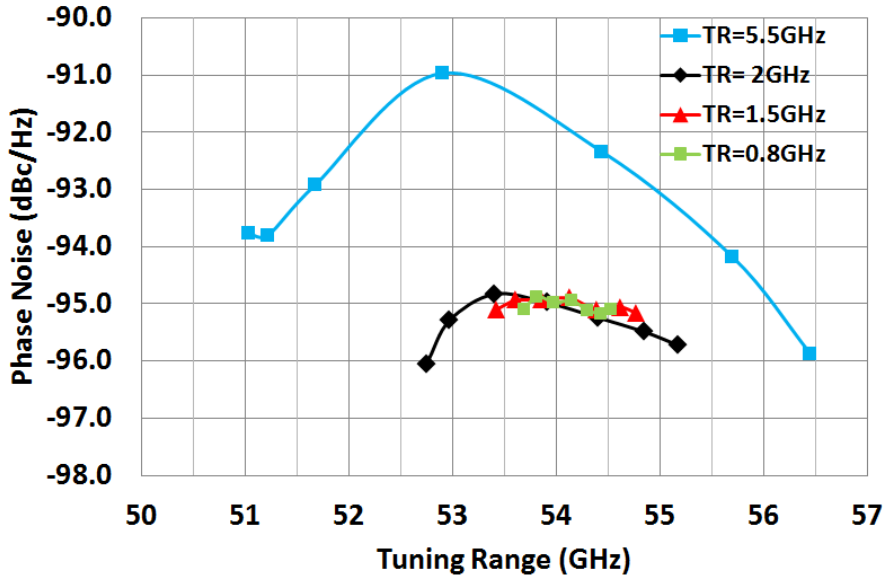


Figure 2.7 Phase noise (at 1MHz offset) and tuning range trade-off

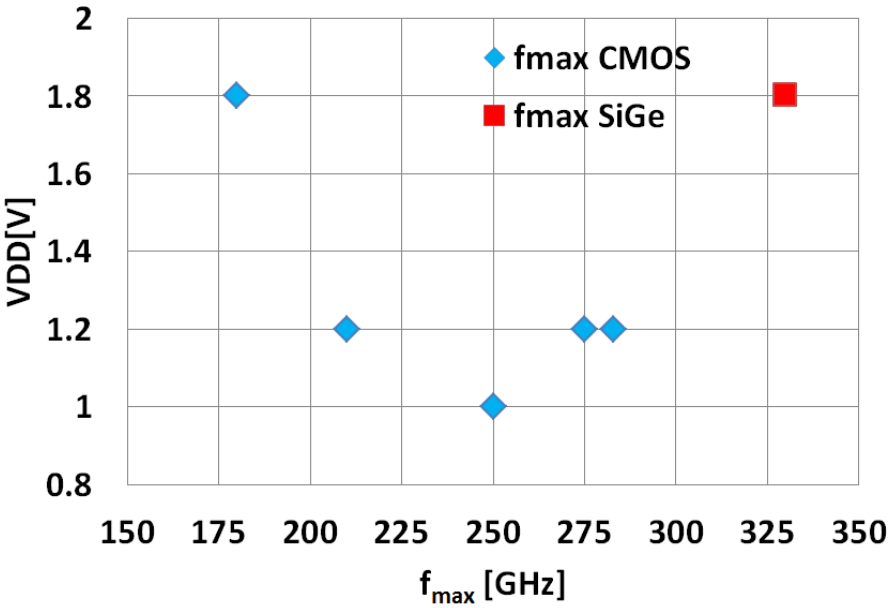


Figure 2.8 f_{max} and VDD of CMOS and SiGe processes

An alternative approach is to use digitally controlled switch MIM-capacitors (Fig. 2.9) for channel selection and MOS varactors for PLL locking. Although using digitally controlled MIM-capacitors addresses the large KVCO issue, it still suffers from limited Q and results in a

similar hit on phase noise. RC-extracted simulations show that digitally controlled switched MIM-capacitors with a capacitor ratio of 2 have a low quality factor of about 15 (Fig. 2.6). Clustering of VCOs such that each cluster covers one channel is intended to address the wide tuning range requirements of 60GHz band without a significant degradation on phase noise. This approach is explained in details in sections III and IV.

Table 2-1 IEEE 802.11ad channels.

Channel	Lower Edge (GHz)	Center (GHz)	Upper Edge (GHz)
1	57.42	58.32	59.22
2	59.58	60.48	61.38
3	61.74	62.64	63.54
4	63.90	64.80	65.70

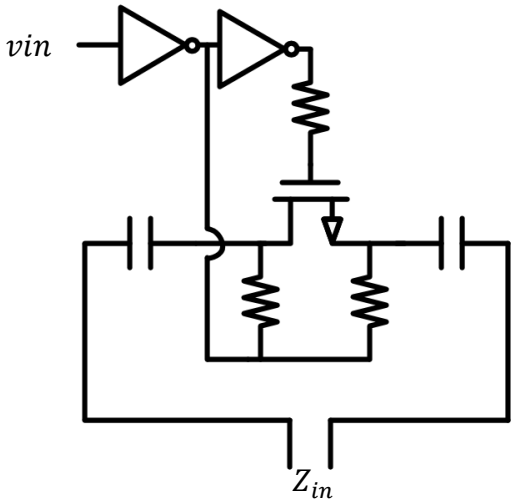


Figure 2.9 Digitally controlled switched-MIM capacitors

2.1.4 Aging and Frequency Shift

Phase noise improves as the voltage swing amplitude increases ((2.5) & Fig. 2.10). Large AC voltage swings on nanometer CMOS, however, changes the device characteristics such as threshold voltage, I_{DSAT} and thus device effective capacitance. These changes are undesired and

can result in failure of the system. For example, significant voltage stress can change the oscillation frequency to an extent that the PLL loop would not be able to lock to the center of the channel. Thus, the AC voltage swing must be constrained. Figure 2.11 shows simulated oscillation frequency shift in a 40nm NMOS cross-coupled pair when the oscillator is stressed for 6 months. The NMOS cross-coupled pair can sustain up to 1.8V of AC voltage on its drain terminals without a significant change in the frequency of oscillation. This corresponds to about 1.5x of the DC VDD rating of this process (1.2V) and can be used as a guideline for maximum AC voltage swing tolerance for consumer electronic devices with a life cycle of about 5 years.

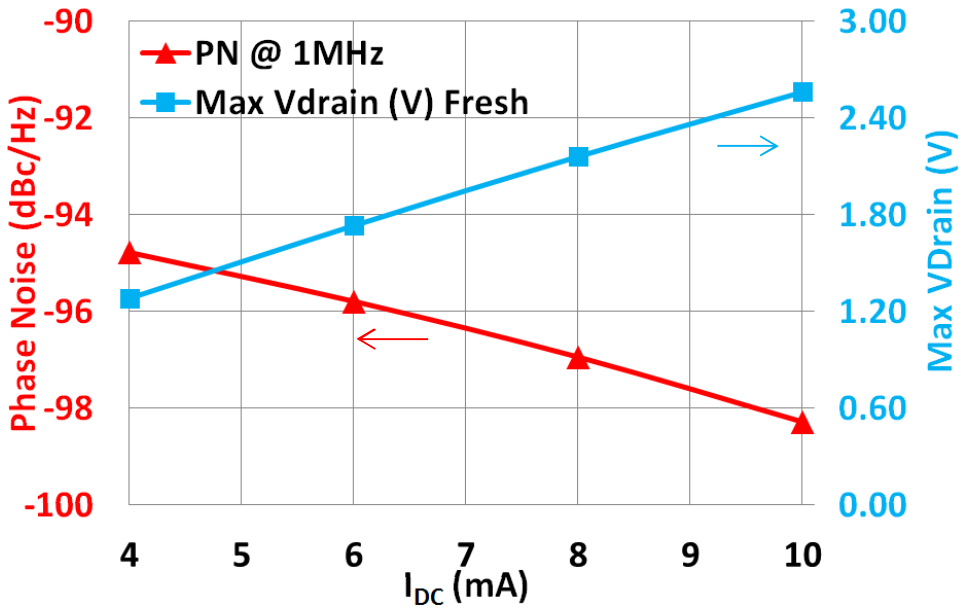


Figure 2.10 Effect of DC current on phase noise and voltage swing for a fixed device size

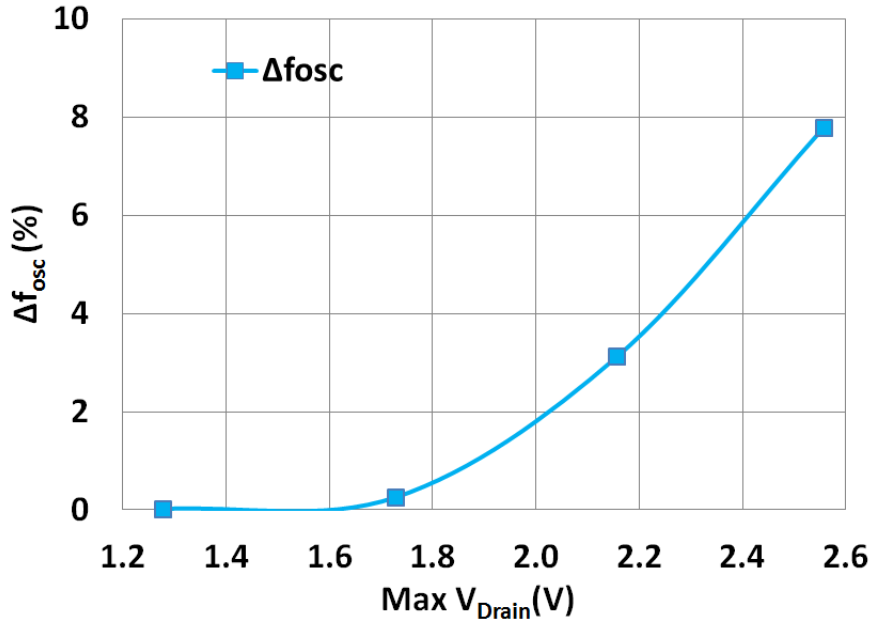


Figure 2.11 Effect of voltage swing on oscillation frequency after 6 months of continuous stress

A large AC voltage swing degrades g_m of the device overtime and thus can cause oscillation startup issues or weak and insufficient oscillator voltage swing amplitude. Figure 2.12 shows this issue in simulation. Under significant stress, the oscillation voltage swing drops significantly over a 6-month stress time from 2.6V to about 1.3V due to the drop in g_m.

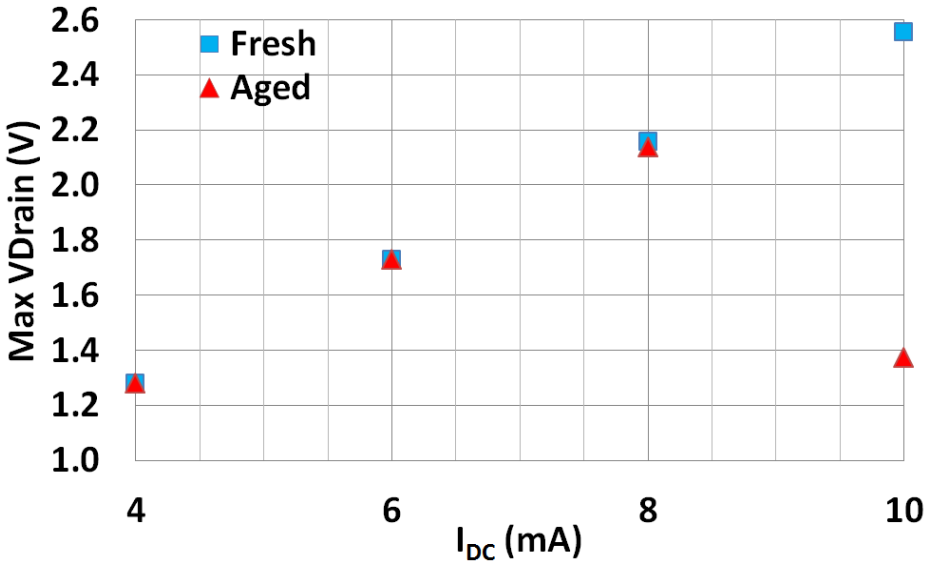


Figure 2.12 Long term voltage swing deviation due to 6 months of stress

2.2 Architecture

In the quad-cluster topology, each cluster covers one target channel. The desired cluster is activated by coarse digital control switches while other clusters are turned OFF. Splitting the VCO into clusters limits the tuning range requirement for each cluster to a few hundred megahertz for mm-waves thus eliminating the need for large varactors or capacitor arrays.

Fine-tuning for each cluster is achieved using NMOS varactors which provide more than 550MHz of continuous analog tuning for each channel. This range is sufficient for calibration and frequency locking in a PLL system.

The four clusters are connected in parallel using an H-shaped 100Ω differential coplanar transmission line (TL). The H-shaped figure makes the design more symmetrical and facilitates floor-planning (Fig. 2.13). The center point of the H-figure is connected to a GSSG pad via a TL.

Each cluster contains four identical VCO cores connected by the aforementioned H-shaped differential coplanar TLs. Each VCO core consists of an NMOS cross-coupled pair, a 2:1 transformer, and a PMOS current source placed on the transformer's center tap. This design keeps the layout symmetric. With the VCOs placed close together, the interconnect between the cores of a single cluster can be treated as a lumped connection. The proposed combination boosts the load impedance seen by each cross-coupled pair in two ways.

First, coupling M VCOs improves the impedance due to the replica-loading Q-Effective-enhancement effect as shown in Fig. 2.13. Second, the transformer provides further impedance transformation. As depicted in Fig. 2.13, the effective $R_{Parallel}$ seen by each VCO is $N^2 * M$, where N is the turn ratio of the transformer and M is the number of coupled VCOs (assuming ideal transformers). Consequently, Q-degradation of the LC tanks due to the external load is minimal. Furthermore, having multiple cores in parallel improves the phase noise due to

uncorrelated nature of device noise.

This approach also addresses the voltage swing reliability issues by combining the current of multiple VCO cores in parallel. This allows for the scaling of power without violating voltage swing constraints. The design achieves –101.8dBc/Hz at 1MHz offset with over 12% of tuning range.

Note that the cores in a multicore VCO will lock in phase if there is a finite external load across the differential output nodes. Consider the two-core case. Establishing a voltage swing across the load (and oscillation in the VCO) requires a current to pass through $R_{Load}(i_R \neq 0)$. In the absence of mismatches, two identical VCO cores connected in parallel experience the same voltage swing and must have the same current magnitudes (Fig. 2.13). This implies that the current through the load can only be applied as the summation of two in-phase currents induced by the VCOs. (If the currents were out-of-phase, there would be no current through the load and zero voltage swing; however, we assume that the VCOs are designed with enough negative-gm to compensate for the loss of the load.) In practice, to ensure functionality in the presence of mismatch between the VCO cores, R_{Load} should be chosen such that a small delta in the currents of the VCO going through the load does not produce a large enough swing that is comparable to the VCO swing.

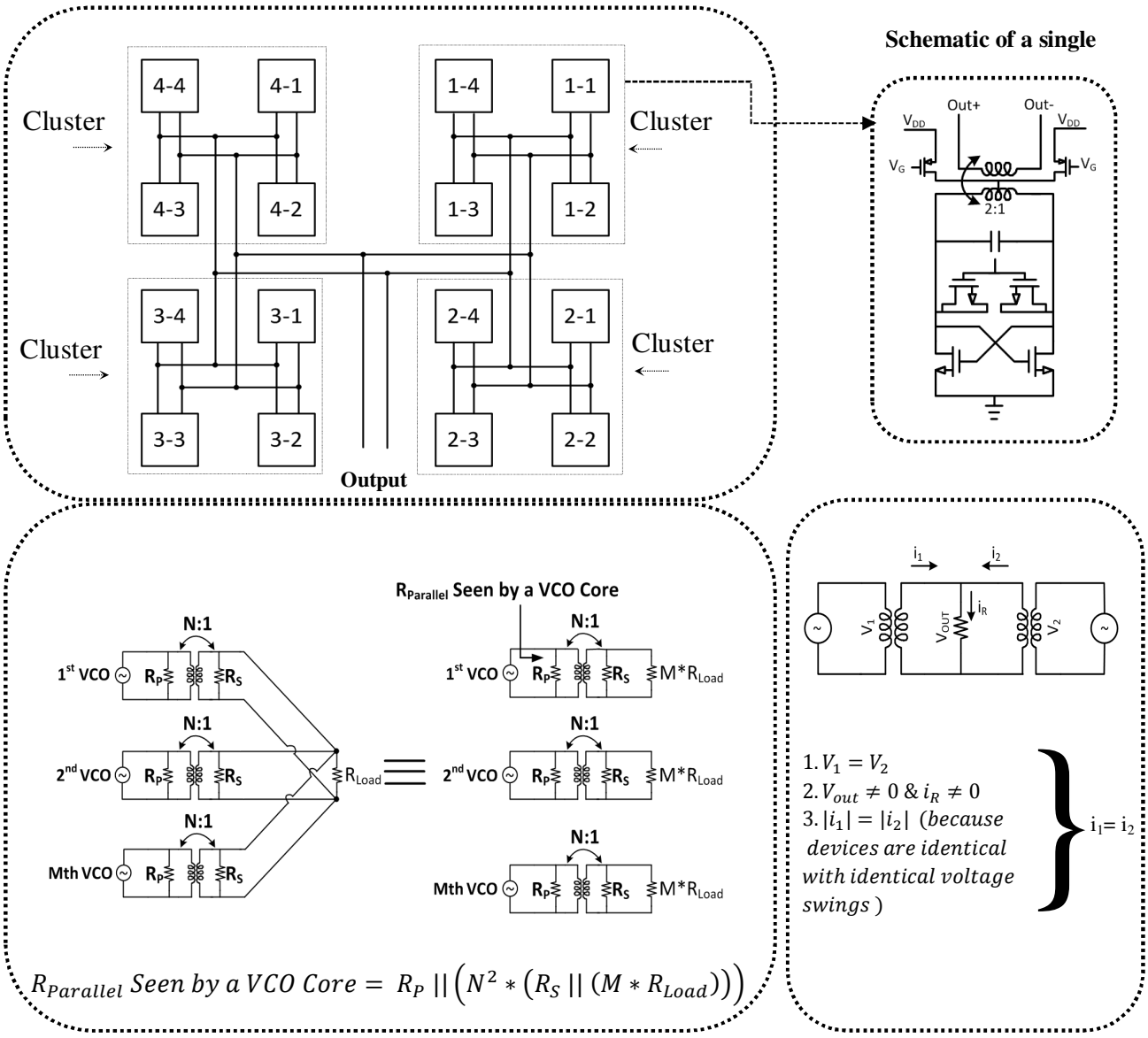


Figure 2.13 Schematic view of the clustered VCO

In the case of more than two identical VCOs with the same transient voltage form, the load seen by each of them has to be equal. This requires all cores to be locked in-phase (as a pair locked out-of-phase will see a different load than the rest of the cores; this would mean that it has a different current from the other cores and would violate the equal-in-amplitude current assumption).

2.3 Simulation and Measurement Results

Figure 2.18 shows the measurement setup. Testing was done cluster-wise by turning each cluster ON/OFF independently using DC needles. Furthermore, each core of cluster one could be turned ON/OFF, resulting in 15 different configurations for channel 1. Phase noise of each configuration is measured by an Agilent E5502B Signal Source Analyzer connected to an Agilent E5053A down-converter and two external mixers which down-convert the mm-wave frequency to the operating range of the signal source analyzer. Figure 2.15 shows the phase noise graphs obtained from different configurations of channel 1. With only a single VCO of cluster 1 turned ON, the phase noise is –86dBc/Hz at 1MHz offset. By turning two cores ON, the phase noise is improved significantly. This is primarily due to two reasons.

With two cores ON, the effective $R_{Parallel}$ of the tank improves, which results in a quadratic improvement in the phase noise due to replica-loading Q-enhancement. Additionally, the correlated oscillation generated by enabling multiple VCOs in the cluster reduces the impact of uncorrelated noise signals. As more cores turn ON, the oscillation frequency shifts down due to the change in capacitance of the cross-coupled pairs. The best phase noise is achieved when all four VCOs are ON as expected. This configuration achieves a PN value of –101.8dBc/Hz at 1MHz offset with an oscillation frequency of 50.72GHz and an FOM of -182.1dB/Hz. The phase noise and oscillation frequency for different configurations are listed in Table 2.2.

Table 2.3 shows $R_{Parallel}$ seen by the differential cross-coupled pair of each ON oscillator as the cores of cluster 1 are turned ON with clusters 2, 3, and 4 turned OFF. In single core operation, the ON core is loaded with the pad impedance (100Ω) as well the impedance of the OFF cores. Although the 2:1 transformer boosts this impedance to some degree, the extra loading of the pad and the OFF cores is large enough to degrade the phase noise significantly.

When the second core is turned ON, the impedance seen by the differential pair of each ON core is boosted from 220Ω to 422Ω because the dual core operation doubles the loading impedance (Fig. 2.13). Thus, the phase noise improvement purely due to this effective Q-enhancement is 5.6dB. Since the total current consumption is doubled as well, the phase noise improves by an extra 3dB. Finally, oscillation frequency is pushed down from 54.7GHz to 52GHz which would correspond to another 0.4dB in phase noise improvement purely to lower frequency. Adding these theoretically calculated improvements suggests a 9.1dB improvement in phase noise from single to dual core operation, which is very close to 9.7dB seen in simulation.

Turning the third core ON, $R_{Parallel}$ is increased to 550Ω with an associated 2.3dB of phase noise improvement purely due to this higher impedance compared with dual mode operation. Furthermore, since the total current increases by 1.5x, the phase noise should improve by 1.7dB due to the larger current consumption. An additional 0.1dB improvement is due to frequency downshift from dual-core to triple-core operation. The net theoretical phase noise improvement is 4.1dB, which is close to the simulated number of 4.4dB.

Turning the fourth core ON, $R_{Parallel}$ is increased to 650Ω with an associated 1.4dB of phase noise improvement purely due to this higher impedance compared with triple mode operation. Furthermore, since the total current increases by 1.3x, the phase noise should improve by 1.2dB due to the larger current consumption. An additional 0.1dB improvement is accounted for the frequency downshift from triple-core to quad-core operation. The net theoretical phase noise improvement is 2.8dB, assuming the oscillator is not voltage-limited. In simulation, only 0.6dB improvement is seen. This is because the oscillator is voltage limited at this stage and further increase of current does not increase the voltage swing nor phase noise.

Table 2.3 compares the proposed VCO's performance with the state-of-the-art mm-wave

VCOs. The clustered VCO achieves the lowest phase noise and best FOM without sacrificing frequency tuning range.

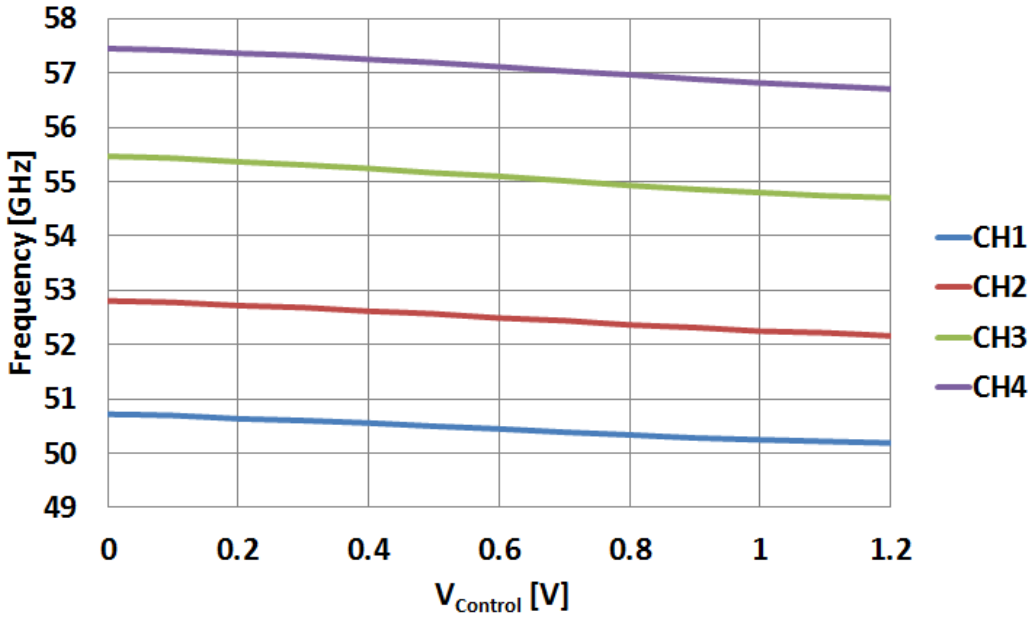


Figure 2.14 Measured VCO frequency tuning range in quad-core operation mode

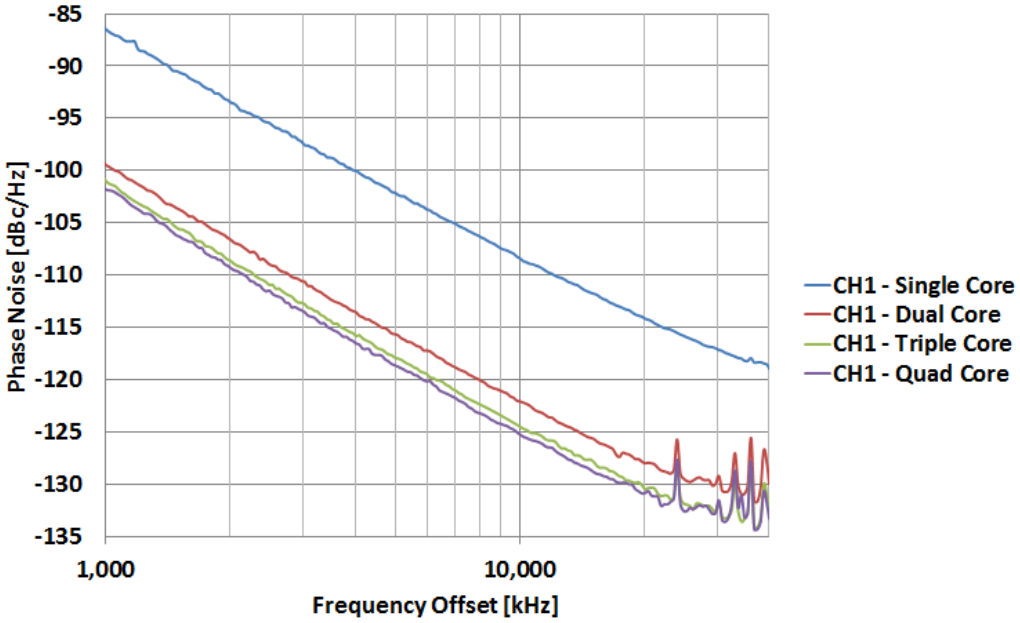


Figure 2.15 Measured phase noise comparison for CH1 configurations

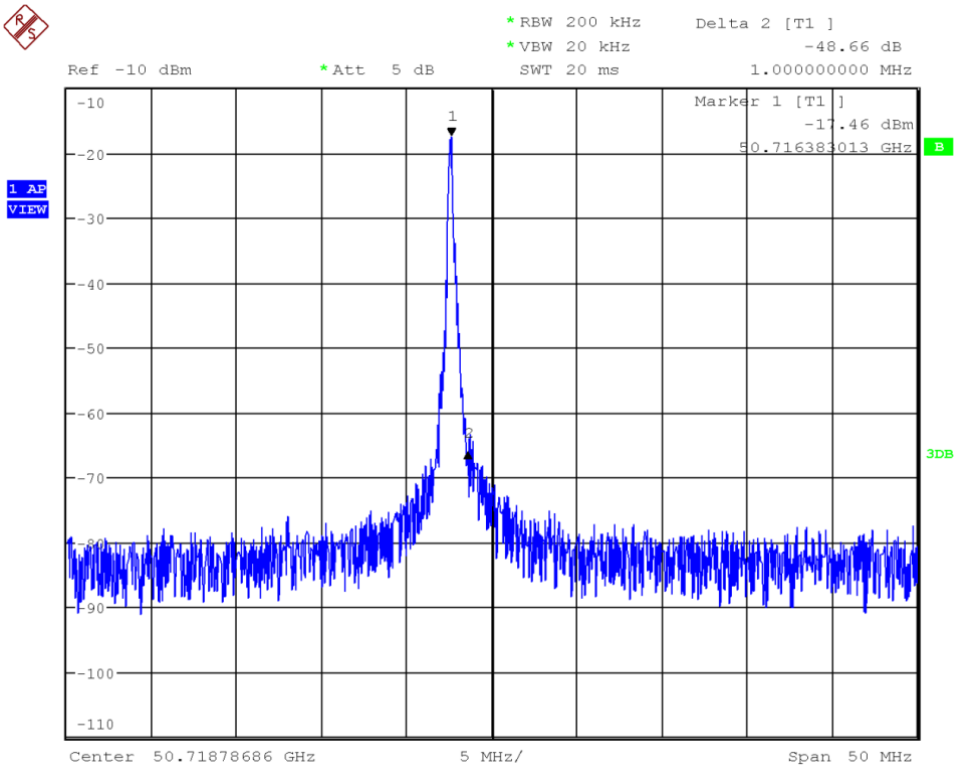


Figure 2.16 Spectrum of CH1 with four cores ON

Table 2-2 Performance comparison of clustered VCO for different configurations

Config.		Measurement Results				Simulation Results		
CH	# of Cores ON	Freq (GHz)	PN @ 1 MHz (dB/Hz)	PN @ 30 MHz (dB/Hz)	FOM (dB/Hz)	Freq (GHz)	PN @ 1MHz (dB/Hz)	PN @ 30MHz (dB/Hz)
1	4	50.72	-101.8	-132.1	-182.1	50.55	-102.2	-132.2
1	3	51.15	-101	-132.2	-182.6	51.14	-101.6	-130.2
1	2	52.01	-99.5	-129.6	-183.0	52.00	-97.2	-127
1	1	54.98	-86.5	-117.1	-173.5	54.75	-87.5	-117
2	4	52.80	-99.7	-131.9	-180.4	52.48	-100.3	-130.5
3	4	55.46	-98.2	-131.1	-179.3	54.52	-99.6	-130.3
4	4	57.45	-97.3	-130	-178.1	57.51	-98.9	-128.8

Table 2-3 Calculated phase noise improvement due to multicore operation of channel 1

	Freq. (GHz)	R_{Par} (Ω)	**PN+$_R$** (dB)	**PN+$_I$** (dB)	**PN+$_f$** (dB)	**Calculated PN+** (dB)	**Simulated PN+** (dB)
1	54.75	220	-	-	-	-	-
2	52.00	422	5.7	3	0.4	9.1	9.7
3	51.14	550	2.3	1.8	0.1	4.2	4.4
4	50.55	650	1.5	1.2	0.1	2.8	0.6

R_{Par}: $R_{Parallel}$ seen by each ON cross-coupled diff. pair

PN+$_I$: Phase noise improvement due to larger DC Current

PN+$_R$: Phase noise improvement due to higher R_{Par}

PN+$_f$: Phase noise improvement due to frequency downshift

Table 2-4 Overview of state-of-the-art mm-wave CMOS VCOs

	This Work	**[26]**	**[8]**	**[27]**	**[28]**
Technology	40nm CMOS	90nm CMOS	65nm CMOS	90nm CMOS	65nm CMOS
Frequency (GHz)	50.7 to > 57.5	53.2 to 58.4	56 to 60.5	48.2 to 51.7	34 to 40
Tuning Range	>12.6%	9.3%	7.7%	7%	15.1%
PN @ 1 MHz (dBc/Hz)	-101.8	-91	-97	-87	-98.1
P_{DC} (mW)	24	8.1	22	22.7	14.4
FOM* (dB/Hz)	-182.1	-176.7	-179	-167.4	-178.5
Area (mm^2)	0.33	0.077	0.075	-	0.15

$$^{*}FOM = L(\Delta f) - 20 * log\left(\frac{f_{osc}}{\Delta f}\right) + 10 * \log\left(\frac{P_{DC}}{1mW}\right)$$

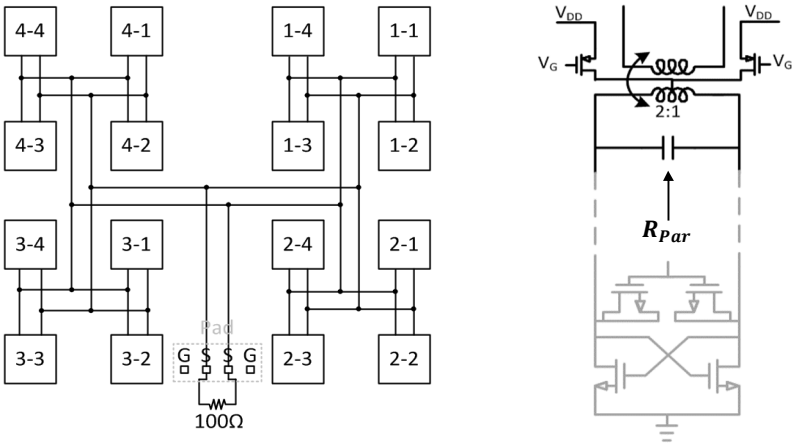


Figure 2.17 $R_{Parallel}$ seen by each ON oscillator core

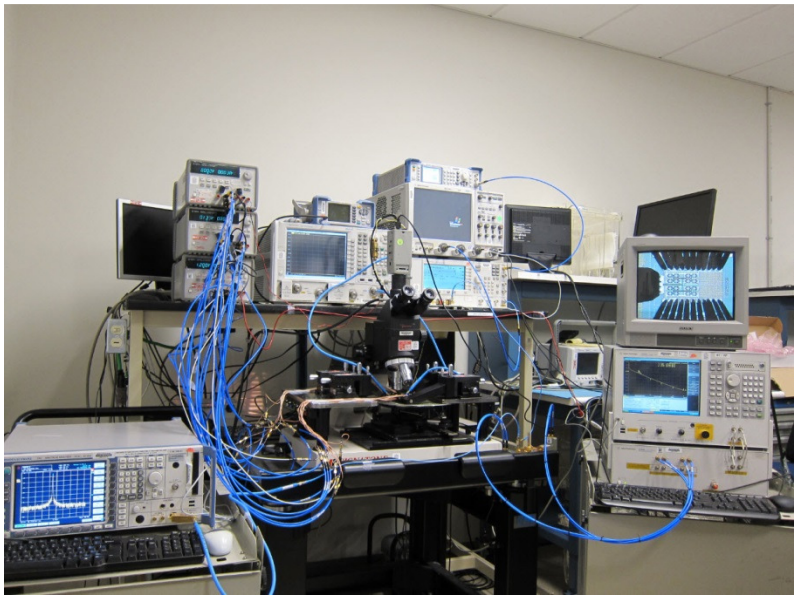


Figure 2.18 Measurement Setup

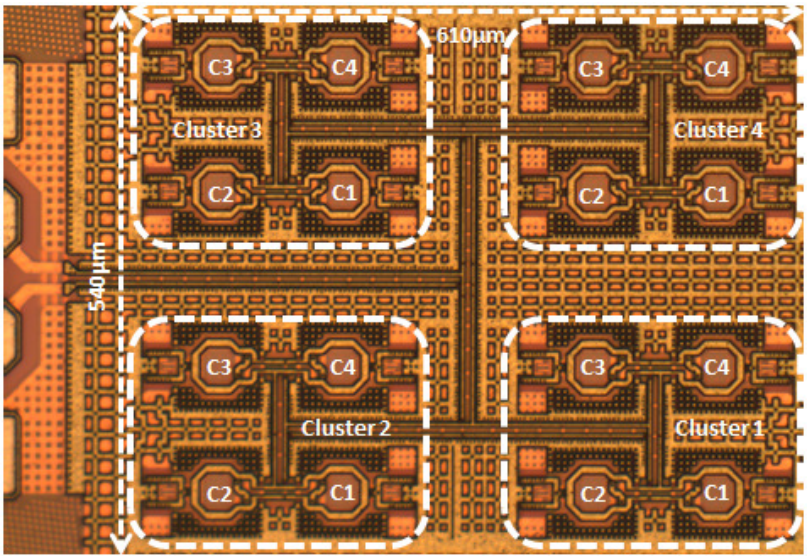


Figure 2.19 Die photo

2.4 Conclusion

The multi-cluster, multi-core mm-wave oscillator architecture decouples phase noise and tuning range trade-off of conventional oscillator architectures to a great extent. Using four clusters that each covers one channel of the WiGig standard, the tuning range requirement for

each cluster is reduced to only hundreds of megahertz for PVT variation and PLL locking instead of the 7GHz total bandwidth of the IEEE standard. As a result, each cluster can be designed with significantly better phase noise. Further enhancement of phase noise is obtained through using multicores of oscillators. Using 2:1 transformers desensitizes the ON cores from the loading of OFF cores and eliminates the need for a mm-wave multiplexer. Core activation control also enables different phase noise and power consumption states optimized for different modulation and coding schemes (MCS). All cores can be turned ON for high index MCS's with more stringent phase noise requirements while some cores can be turned OFF for lower MCS's with more relaxed phase noise requirements to save DC power consumption.

Chapter 3

Power Combining for Power Amplifiers

The achievable output power in sub-micron CMOS PAs is limited by reliability concerns. To avoid device breakdown and hot carrier injection, supply voltage has to be kept low resulting in low P_{SAT}. Worse yet, even if operating within the device breakdown limits, the high voltage stress on the transistors of the last stages in a PA chain can result in a gradual drop in gain and/or P_{SAT}. To mitigate metal electromigration concerns, thick top metals and wide VDD and ground traces (sometimes both in the same layer) are employed but the resulting geometries make achievable performance strongly dependent on the floor plan.

Power combining techniques have achieved P_{SAT} levels of 17 to 20dBm at mm-waves in standard CMOS processes [1, 3, 7] . However, conventional power combining approaches (e.g., solely combining with Wilkinson combiners) suffer from both the loss in combiners (0.6 to 1.5dB per stage) and significant interconnect loss (0.7 to 1dB per mm) between the output nodes. In-air power combining using antenna arrays can avoid combiner in some cases [29]. However,

this method may not be applicable in emerging applications that employ a single-feed high-gain radiator such as a reflector antenna (e.g., PtP wireless backhaul).

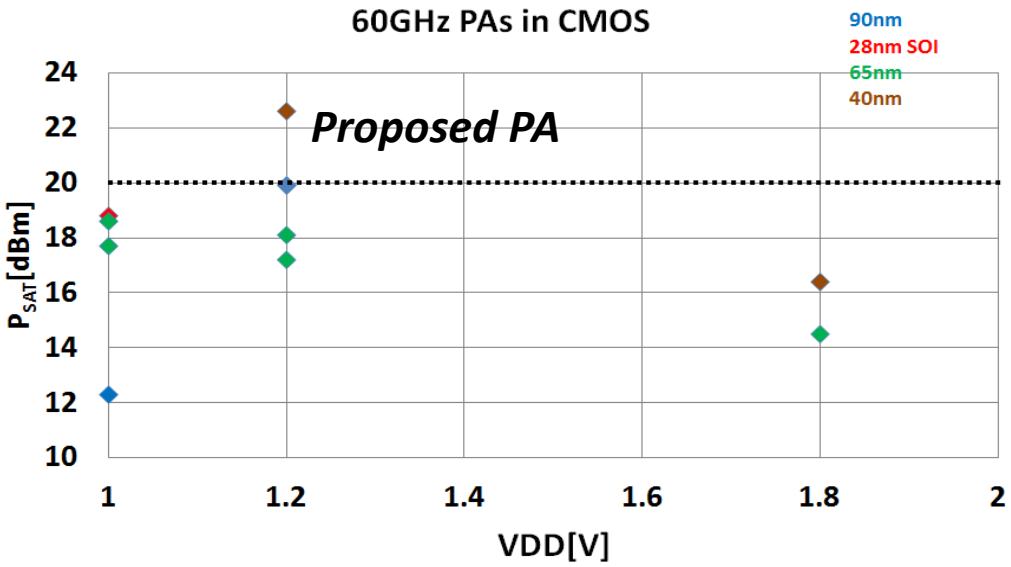


Figure 3.1 Survey of state-of-the-art 60GHz CMOS PA's

The fully integrated CMOS PA presented here achieves the highest reported P_{SAT} by combining the outputs of eight PA chains through a combination of transmission lines (TL), Wilkinson combiners, and multi-port argyle transformer (Fig. 3.2). The PA is designed in 40nm CMOS with six metal layers (UTM6) and an ultra-thick RDL layer.

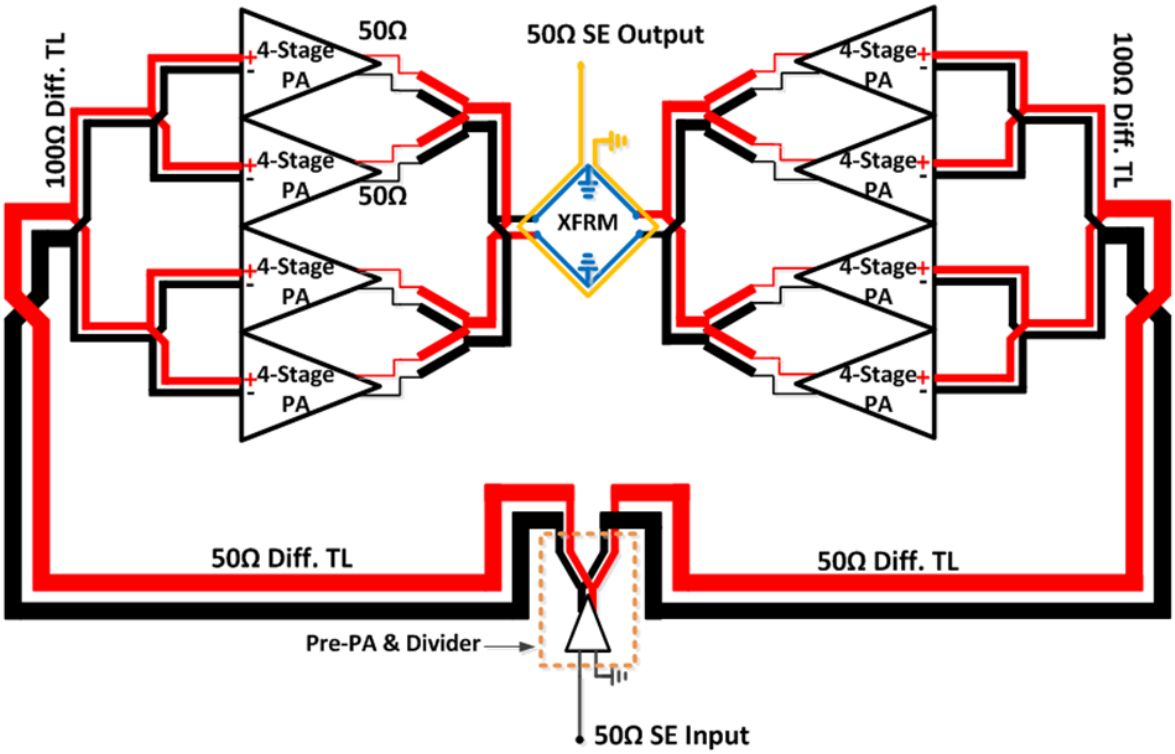


Figure 3.2 Block diagram of the fully integrated 60GHz PA

3.1 Architecture

A schematic of the individual PA chains is shown in Fig. 3.3 (see Fig. 3.4, Cell B2 also). Four PA stages, each employing common source differential pairs with neutralizers, are cascaded via transformers. A parallel RC structure stabilizes the PA. Stage 2 and 3 employ transformers with two pairs of input and two pairs of output differential nodes (Fig. 3.3.) This divides the total voltage swing between 4 sets of transistors instead of two sets if conventional transformer coupling were employed. Consequently, the swing on the drains and gates of each transistor is reduced thereby enhancing lifetime reliability. Each of the fourth stage transformers converts a 50Ω differential output to two pairs of 25Ω differential nodes at the drains of the last stage PAs.

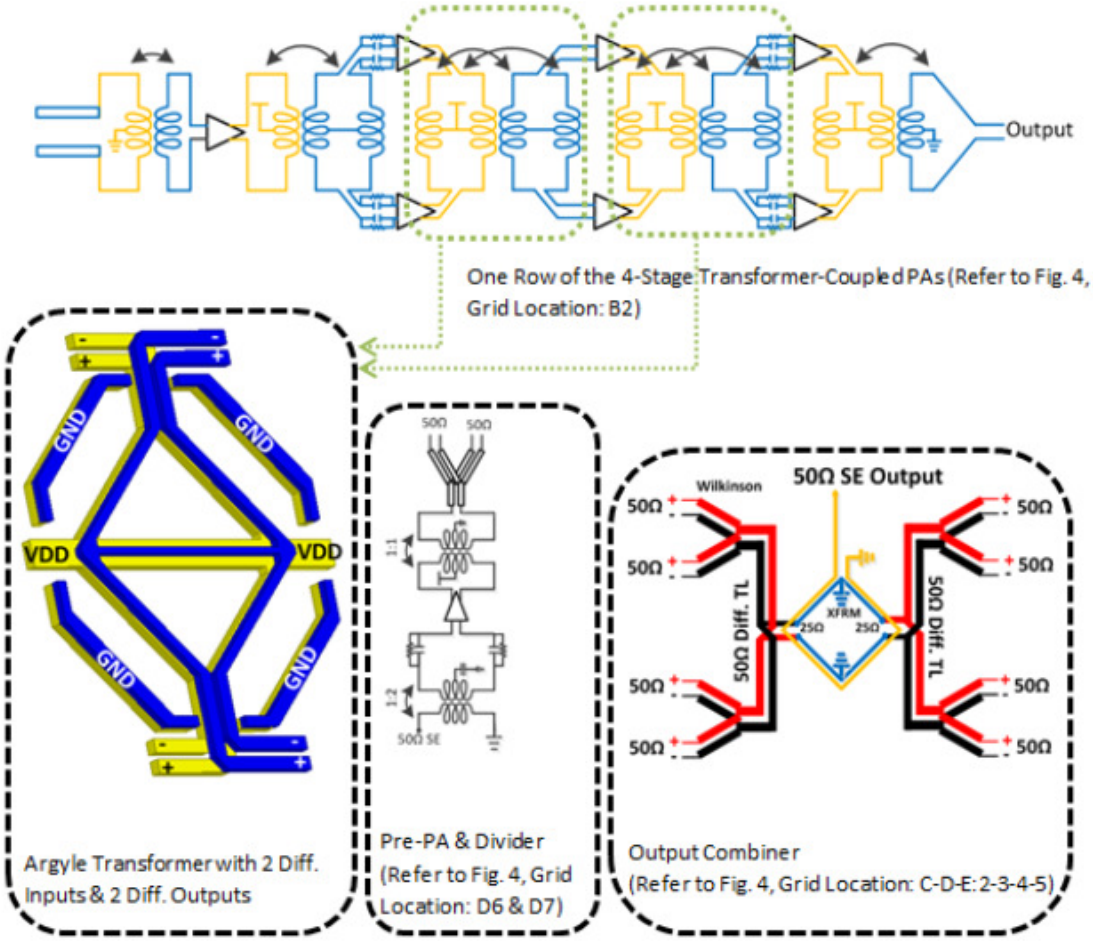


Figure 3.3 Sub-blocks of the PA

The low impedance seen by each differential pair (25Ω differential) alleviates the voltage stress on the drain of each device. These argyle-shaped transformers also reduce the routing length (and thus the parasitic inductance) between the transformers and the drains of the differential pairs. They also enable a tile-based placement of bypass capacitors between VDD and ground on each side of the transformer, resulting in an efficient allocation of space between transformers, transistors, bypass capacitors and VDD and ground routing. A schematic of the 8-way output combiner is shown in Fig. 3.3 (see also Fig. 3.4, Cells C-D-E: 2-5). It combines the outputs of eight pairs of differential nodes and delivers power to a 50Ω-SE output with just 3dB

loss. The outputs of each pair of PA chains are combined through a compact implementation of a Wilkinson combiner with two 50Ωinputs and a 50Ωoutput. A pair of 50Ωdifferential coplanar TLs follows the combiners and is connected in parallel at the inputs of the final transformer (Fig. 3.4, Cell D3 & D4). The coplanar TLs combine the output power of the Wilkinson combiners with low loss (<0.6dB) and provide a 50Ωto 25Ω impedance transformation. The argyle transformer that follows the TLs performs three tasks with 1.5dB loss. It combines two pairs of differential nodes, implements a 25Ωto 50Ω impedance transformation, and transforms differential input signals to a single-ended output. Grounding the mid-points of the input loops enhances differential behavior of the transformer.

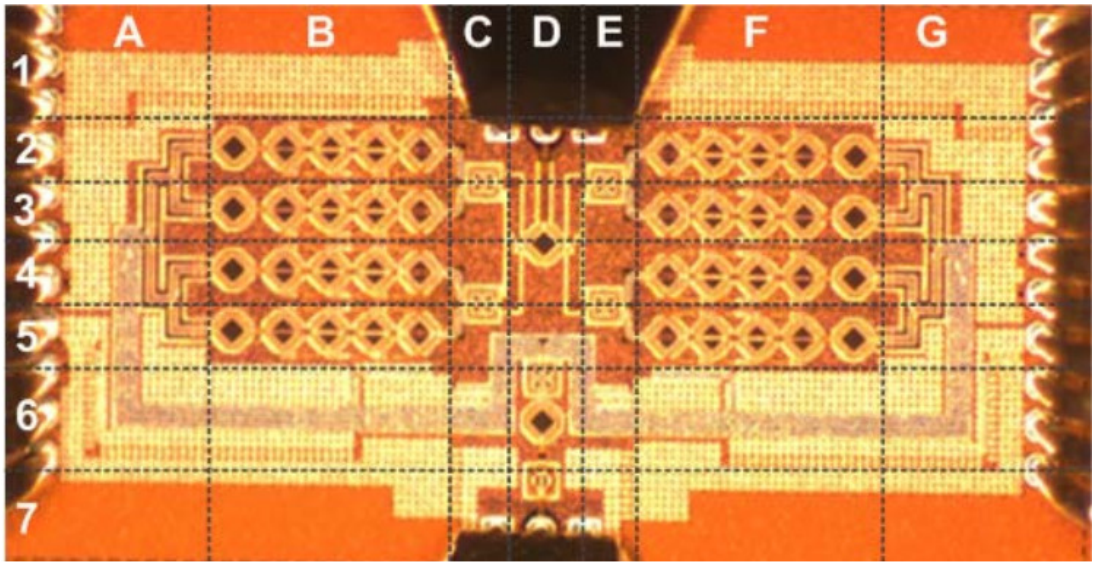


Figure 3.4 Die photo

The 8-way combiner needs to maintain the same impedance level (50Ω) at the inputs (for proper loading of each pairs of PA chains) and the output (for impedance matching to the antenna) with low loss. This is challenging since each parallel combination divides the impedance by two and each series combination multiples it by two. Conventional combining

approaches would have required additional stage(s) of transformation and suffer from extra loss. In the process used for this design, M6 is the only layer that can handle a reasonable current density (~34mA/μm at 110ºC compared with 12.6mA/μm of UTRDL). Due to this, both VDD and ground routings are implemented in M6. An M6 VDD line goes through each stack of PAs. It is wider in the final stages (10μm) and narrower at the initial stages (8μm), and is capable of handling 340mA at 110°C without significant degradation over 10-year/100% operation.

The input power is delivered to the PA stacks through two branches of 50Ω differential coplanar lines on each side of the input pad. Each branch is divided into two 100Ω TLs connected in parallel as shown in Fig. 3.2 (see also Fig. 3.4, Cells A3 and A4). Each 100Ω line is further divided into two differential TLs.

Although realizing a 200Ω-TL is impractical in silicon, the length of the last-stage TL is small and thus does not result in significant impedance mismatch. To compensate for the insertion loss of the TL divider network (~3.7dB), a pre-PA is added between the Wilkinson divider and the input GSG pad (Fig. 3.2 and 3.3). A 1:2 transformer is used to match the input of the first amplifying stage to a 50Ω-SE probe. As shown in Fig. 5, return loss at the input (S_{11}) is better than -10dB across the 60GHz band. S_{22} is well matched from 50GHz to beyond 67GHz.

3.2 Measurement Results

Figure 3.6 shows P_{OUT} vs. P_{IN} of the PA at 60GHz with a VDD of 1.2V. The graph is obtained by driving the PA with a mm-wave signal generator and measuring the output power by a mm-wave power meter. The loss of the cables and GSG probes are de-embedded by measuring an on-wafer thru GSG structure. The PA has a gain of about 30dB with an estimated measurement accuracy of 1dB. OP1dB is 17dBm at 60GHz.

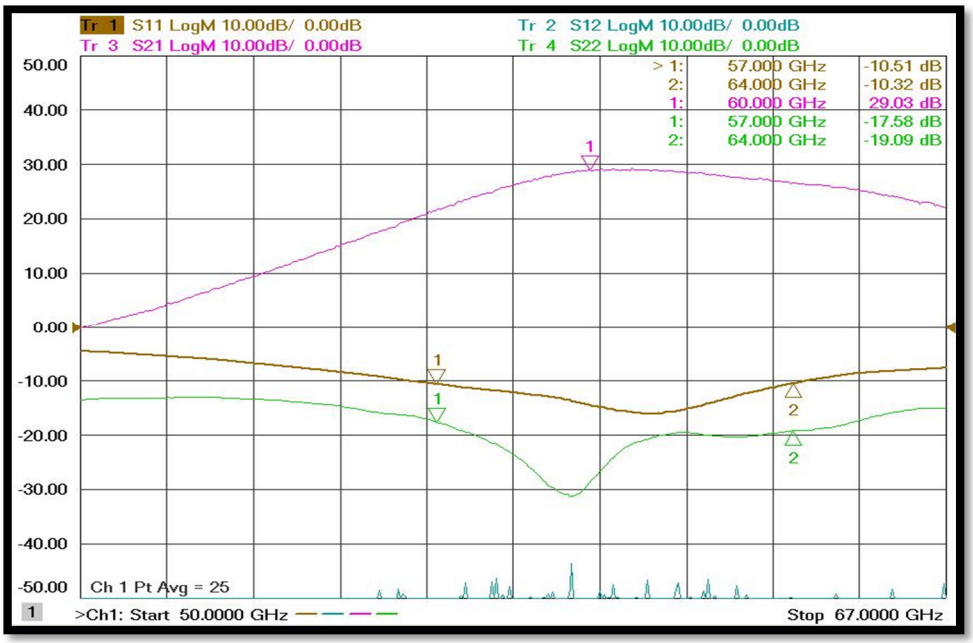


Figure 3.5 Measured S-parameters of the entire PA

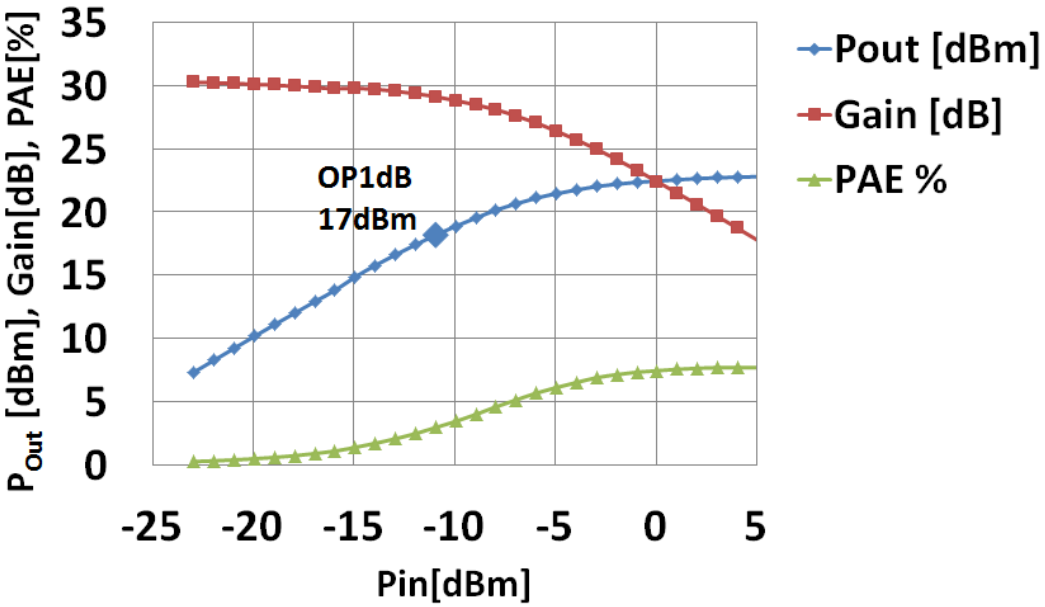


Figure 3.6 Measured PA P_{OUT}, Gain and PAE vs. P_{IN} at 60GHz (VDD=1.2V)

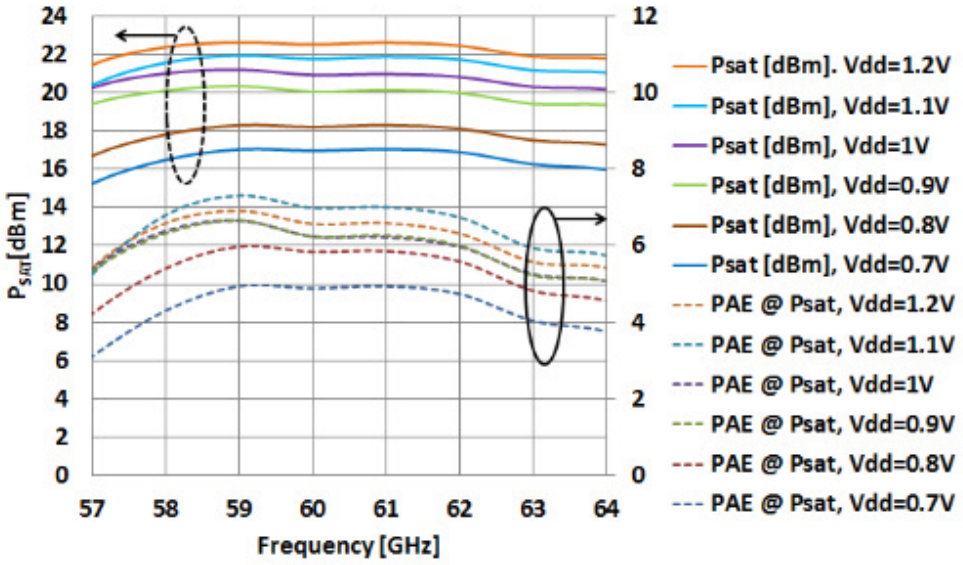


Figure 3.7 Shows P_{SAT} and maximum PAE versus both frequency and VDD

Biasing of the differential pairs is adjusted for each supply level to achieve the highest P_{SAT} for the given VDD. The IR drop of the DC probes is de-embedded by monitoring the voltage difference between a VDD and a GND pin. With a VDD of 1.2V, the PA achieves a P_{SAT} of 22.6dBm at 60GHz with less than 1dB variation across the band; PAE peaks at 7% at 59GHz. Efficiency can improve by 1% to 2% with wider VDD and GND routings between DC probes and the center of the chip (Fig. 3.5, cells A7 & B7) where VDD is fed to the PA chains. In an actual product, a large number of DC bumps that distribute the supply current more evenly would reduce the IR drop. When operating with a reduced 0.7V supply, this design achieves a P_{SAT} of 17dBm. This high level of mm-wave P_{SAT} on even a low VDD indicates that the proposed architecture can also be utilized in more refined CMOS processes such as 28nm CMOS that use a lower supply voltage.

Table 3-1 Comparison of state-of-the-art mm-wave CMOS power amplifiers

	This Work	**[7] [ISSCC'10]**	**[1] [ISSCC'11]**	**[3] [ISSCC'10]**	**[6] [ISSCC'15]**
Technology	40nm CMOS	90nm CMOS	65nm CMOS	65nm CMOS	28nm UTBB FS-SOI
Supply V/P_{DC}	1.2V/2.44W	1.2	1	1	0.8
S21 @ 60GHz (dB)	29	20.6	20.3	19.2	15.4
OP1dB @ 60GHz (dBm)	17	18.2	15	15.1	16.2
P_{SAT} (dBm)	22.6	19.9	18.6	17.7	16.9
PAE @ P_{SAT} (%)	7	14.2	15.1	11.1	21
FOM*	95.6	87.6	82.3	82.9	82.9
Area (mm^2)	2.16 [1x2.16mm]	1.76 [1.85x0.95]	0.28	0.83	0.162

$$^{*}FOM = \left(P_{SAT} + 10 * log(PAE) + Gain + 20 * log(f)\right)$$

Chapter 4

Stacked Power Amplifiers

Stacking of transistors with high f_{max} but low breakdown voltage is another technique to obtain high output power at microwaves and mm-waves. A number of recent publications have shown that by stacking transistors and designing feedback networks around them, reliable output power delivery of PAs can increase [10-18, 30, 31]. This chapter presents the design trade-offs between gain and reliable output power and proposes an optimal stacking solution.

4.1 Stacking Approaches

The common approach in this arena so far has been to design the PA such that the voltage swing is equally divided across the drain-source (or collector-emitter) of the different transistors. This approach would maximize the output power the PA can handle reliably over long term operation. It, however, would sacrifice G_{MAX} of the composite stacked transistor because the power generated by the g_m transistor is divided between the r_o of the g_m-device and the source

of the top device (Fig. 4.1). Since the effective r_o of CMOS devices suitable for an output power of larger than 15dBm is in the order of 50Ω -200Ω at mm-waves, there would be a significant current division between the g_m device and the source of the top. This current division reduces the G_{MAX} of the composite device (Fig. 4.1)

$$Z_{in\_em2} \sim \left(1 + \frac{c_\pi}{c_2}\right) * \left(\frac{1}{g_{m2}}\right) \quad (4.1)$$

$$A_V = \frac{v_{out}}{v_{in}} \sim g_{m1} \frac{r_{o1}}{r_{o1} + Z_{in_{em2}}} R_L \quad (4.2)$$

$$Swing\ Ratio = \frac{v_{ce2}}{v_{ce1}} \sim \frac{R_L}{Z_{in\_em2}} - 1 \quad (4.3)$$

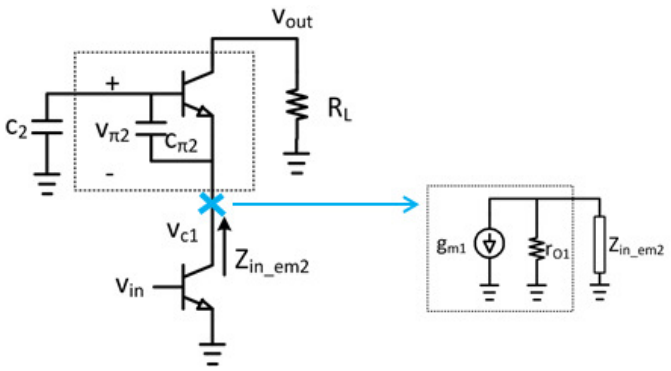


Figure 4.1 Equivalent circuit of stacked PA

To address this issue, a stacking approach with unequal voltage swing is proposed. In this approach, instead of using a single cassocde PA, a double cascade PA is used but with unequal voltage swing division across the three devices. The g_m- device would sustain a lower voltage swing, while the cascode devices sustain larger swings. This way, the impedance looking into the source of the cascode device can be reduced which results in increased gain (Fig. 4.1). Furthermore, because of the addition of the top cascode device, the maximum safe output power the PA can handle (P_{MAX_SAFE}) is not reduced. Figure 4.2 summarizes the pros and cons of different stacking approaches.

Conventional	Equal Swing	Proposed
☺ High Gain ☹ Low P_{MAX_Safe} ☹ Output Matching ☹ large voltage swing on a non-linear cascode device 😐 2 Nonlinear devices	☺ High P_{MAX_Safe} ☹ Low Gain 😐 2 Nonlinear devices 😐 medium voltage swing on a non-linear gm/cascode device	☺ High P_{MAX_Safe} ☺ Good Gain ☺ smaller voltage swings on each non-linear device ☹ 3 Nonlinear devices

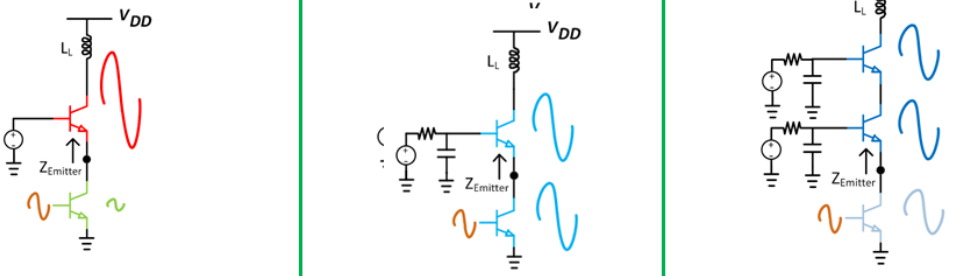


Figure 4.2 Comparison of Stacking Approaches

Figure 4.4 shows normalized P_{MAX_SAFE} vs. ratio of the voltage swing across the cascode devices to the voltage swing across the g_m device (namely α_1 and α_2). As it can be seen from the plot, V_{MAX_SAFE} is maximized when α_1 and α_2 are equal to 1 (when all devices have equal voltage swing). However, this condition has sub-optimal gain, a significant issue at mm-waves. A high P_{MAX_SAFE} with a high gain can be achieved by choosing α_1 and α_2 slightly larger than 1 (around 1.5 each).

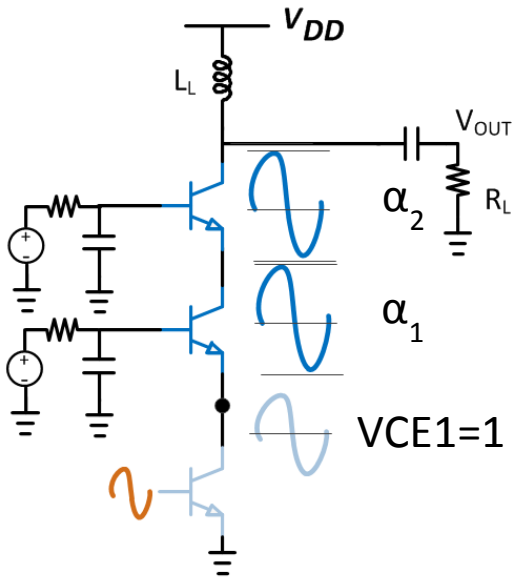


Figure 4.3 Stacked PA voltage swing designation

$$Largest\ V_{DS} < V_{Breakdown} \tag{4.4}$$

$$\frac{max(1,\ \alpha_1, \alpha_2)}{(1 + \alpha_1 + \alpha_2)} * V_{OUT} < V_{Breakdown} \tag{4.5}$$

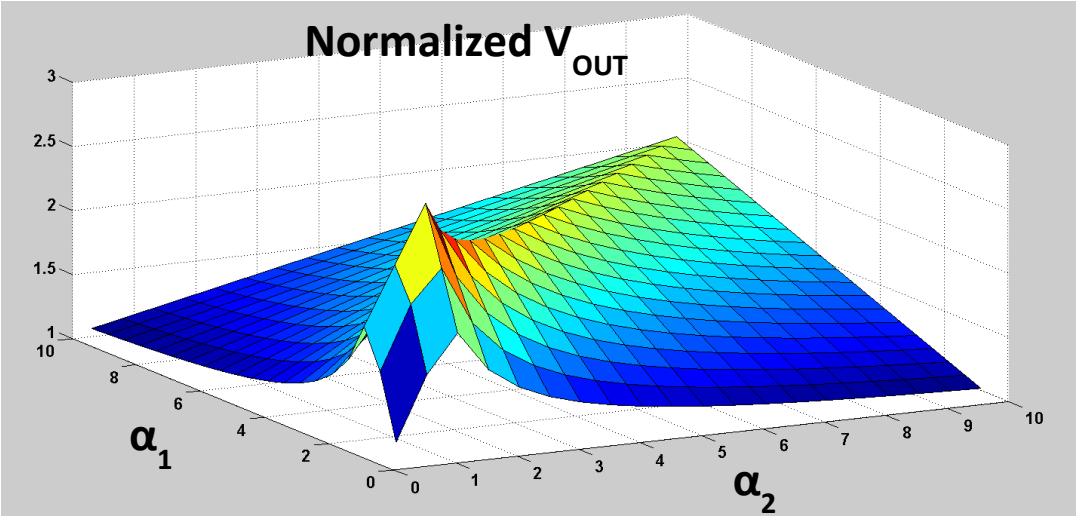


Figure 4.4 Normalized V_{MAX_SAFE} vs. voltage swing ratios of cascode devices to the g_m device

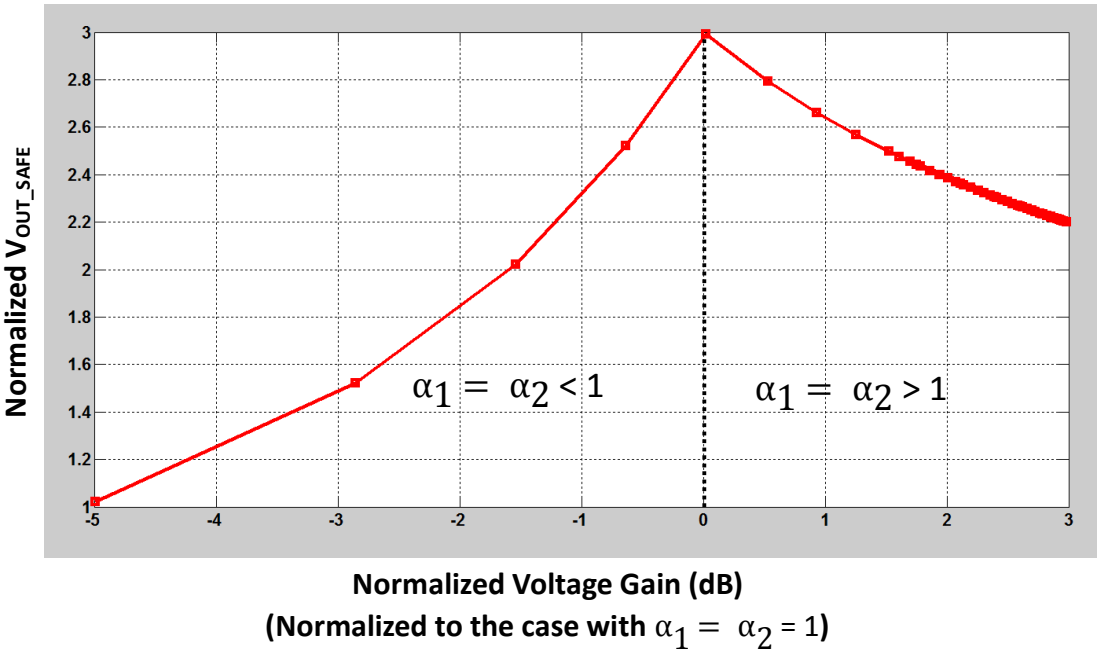


Figure 4.5 Voltage swing-gain trade-off

Using simple device models, it can be shown that the proposed approach of three-stacked PA with unequal voltage swing has about 3dB more gain that the more conventional single stacked-equal swing PA (Fig. 4.6).

$$\Delta PowerGain = 20 * \log\left(\frac{Z_{in1} + ro_1}{Z_{in1new} + ro_1}\right) = 3.1\text{dB}$$

* *Assumption* $RL = ro_1 * 2$

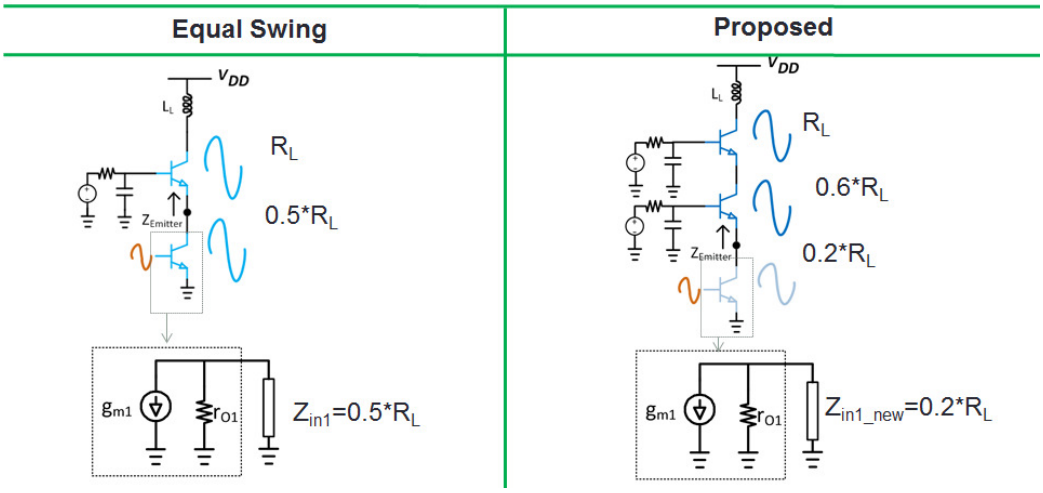


Figure 4.6 Theoretical gain comparison of 2-stack-equal-swing PA vs. proposed 3-stack-unequal-swing PA

4.2 Optimal Stacking for a 60GHz PA

To validate this idea, a PA case study is carried out. The goal is to design a 60GHz PA with a minimum of 10dB gain and a P_{MAX_SAFE} of 20dBm in SiGe. Three architectures are compared: common emitter, single cascode PA with equal voltage swings, and double cascode PA with unequal voltage swings. For each PA topology, a unit cell is first designed; then the number of combiners to reach 20dBm is calculated based on the assumption that each combiner has a loss of 0.7dB. An additional 0.1dB of loss per combiner (attributed to longer trace routings) is considered for cases where there are more than two stages of combining. Table 4.1 summarizes the PA unit cell performance for each of the topologies. Table 4.2 summaries the estimated overall performance of the three PAs using the three different topologies. Double cascode with unequal voltage swing has the best overall performance.

Table 4-1 Performance comparison of three unit cell PA topologies

Unit Cell	Gain	OP1dB	P_{SAT}	$P_{SAT-OP1dB}$	P_{Max_Safe}	Peak PAE	DC Vol		RF Swing
Common Emitter	7.8dB	11.1dBm	13.2dBm	2.1dB	10.9dBm	17.5%	VDD	1.4V	1
FDST Single Cascode	11.3dB	10.3dBm	13.7dBm	3.4dB	14.3dBm	13.4%	VDD	2.9V	1.04
							VCE2	1.5V	
							VCE1	1.4V	1
FDST Double Cascode	13.3dB	11.5dBm	15.6dBm	4.1dB	14.5dBm	12%	VDD	3.6V	2.2
							VCE3	1.5V	
							VCE2	1V	1.8
							VCE1	1.1V	1

Table 4-2 Performance comparison of a 20dBm PA based on three unit cell designs

PA	**Gain**	**OP1dB**	**P_{SAT}**	**$P_{Out\_Reliable}$**	**Peak PAE**	**# Comb.**	**# of Passives**
Common Emitter	3.6dB	20.7dBm	22.8dBm	20.5dBm	7.1%	3	41
Single Cascode	8.5dB	16.9dBm	20.3dBm	20.9dBm	9.7%	2	16
Double Cascode	11.8dB	16.8dBm	20.9dBm	19.8dBm	10%	1	10

The common emitter unit cell PA has the best efficiency of the three as expected. This is due to the fact common emitter has only one passive in the high power path whereas single cascode and double cascode PAs have two and three lossy passives as well as more internodes with device parasitic capacitors that add extra loss and thus reducing the overall efficiency. In terms of gain, double cascode has about 2dB more gain than the single cascode PA. Common emitter has the lowest gain of the all three designs. In terms of linearity measured by OP1dB, common emitter unit cell is the most linear design because it only has one non-linear device (the g_m transistor) contributing to non-linear behavior. Single cascode and double cascode PAs each have multiple devices that contribute to non-linear behavior of the overall PA and thus are less linear. A good measure of linearity is the difference between P_{SAT} and OP1dB of each topology. Table 4.2 shows that this difference is only 2.1dB for the common emitter PA compared with 3.4 and 4.1dB for single cascode and double cascode PA. This is a challenge that exists in many of today's stacked microwave and mm-wave PAs and will be addressed in the next chapter.

Once optimal unit cell PAs are obtained, the performance of a 20dBm PA is estimated using the three topologies. To reach 20dBm $P_{MAX\_SAFE,}$ common emitter unit cell needs to be combined three times (eight PAs). This results in large power loss at the output and degrades the gain and efficiency of the PA. Furthermore, such a structure would need about forty-one passives that would make it very large. Single cascode PA would need to be combined twice (four PAs) to reach 20dBm of P_{SAT_SAFE}. It would not have sufficient gain (only about 8.5dB) and thus would delegate the challenges of a high output PA to the previous stage. The double cascode PA would only need to be combined once (two PAs) and would only require 10 passives. Of the three topologies, the double cascode with unequal swing has the best overall performance in terms of gain, efficiency, and area.

Chapter 5

High Frequency PA Linearization

DEMAND for high data rate wireless links is driving concurrent development of multiple microwave and mm-wave wireless systems targeting Giga-bit-per-second (*Gbps*) links for novel applications. Some of these applications include indoor 60GHz wireless links (IEEE 802.11ad) targeting consumer electronics, outdoor last-mile wireless links using the unlicensed 60GHz as well as the licensed Ka- and Q-band, and more recently satellite links with massive phased arrays for distributing internet connectivity throughout the world. CMOS and SiGe are the two main processes used for these radios due to their f_t/f_{max} production readiness, and cost.

One of the recurring challenges of these radios is the limitations imposed by the maximum reliable output power, linearity, and efficiency of the PA. Figure 5.1 shows VDD of processes suitable for microwave and mm-wave circuit design. With a low supply voltage of less than 2V, a simple PA topology cannot deliver the output power (typically more than 10dBm) needed for most of those application. The two main approaches to address this problem are power combining and stacking. A number of recent works have explored this arena with

P_{SAT}/efficiency/area trade-offs.

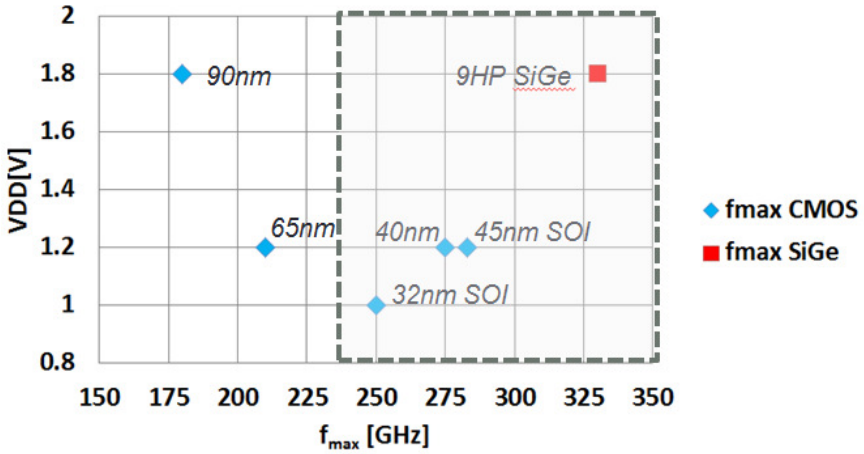


Figure 5.1 f_{max} and VDD of processes suitable for microwave and mm-wave design

Innovations in power combining such as distributed active transformers (DAT), argyle-type transformers, and compact Wilkinson combiners have helped to achieve output powers beyond 20dBm in standard CMOS [1-4, 6, 7] . Challenges that limit this approach are loss of the passive combiners and the large footprint of such devices.

Stacking transistors with the addition of feedback networks to split the swing between the transistors is another approach that is shown useful in designing power amplifiers at high frequencies [10-16, 18, 30, 31]. The benefit of stacking is typically the smaller area and the possibility of using a larger supply and thus reducing the loss in the supply regulator. Stacked PAs, however, tend to be more non-linear because they are, in effect, a cascade of multiple non-linear transistors. These PAs can greatly benefit from a wideband linearization method, but the existing solutions so far are prohibitively cost and power hungry for such wideband channels. In this paper, we present a new wideband linearization technique to linearize both cascode and other topologies of PAs.

5.1 PA Linearization Techniques Overview

5.1.1 Digital Pre-Distortion (DPD)

Digital pre-distortion utilizes digital signal processing capabilities of a modem to correct PA distortion. Inverse of the PA's non-linear model is applied to the baseband data to equalize one or both of AM-AM and AM-PM distortion of the PA (Fig. 5.2). PA's non-linear model used can be either unique to each PA part or it may be generic to a design. For the former, the non-linear model for each PA can be obtained through a factory calibration test at radio wakeup through a Transmit Signal Strength Indicator (TSSI) measurement. In the latter, a statically weighted model obtained during pre-deployment characterization of many parts is programmed into all chips.

Since the correction is applied on the digital data by the baseband modem, the RF circuit complexity overhead is minimal. DPD is proven very useful in Watt-level base station PAs. EVM improvements in the order of 5dB over tens of megahertz are reported in the literature [32]. However, the bandwidth limitations of both the modem and the baseband analog circuitry following the modem limits the channel bandwidth the modem can linearize. Furthermore, memory effects complicate pre-distortion and increase the power consumption overhead [33, 34]. Another limitation of pre-distortion comes from the static nature of the non-linear model. Changes in PA's operating condition (such as temperature, load variation due to dynamic changes in the antenna environment, supply voltage variations, etc.) can dramatically change PA's performance and govern how effective pre-distortion is in correcting PA's non-linear behavior. ADPD (Adaptive Digital Pre-Distortion) implemented in some high performance radios addresses this issue by periodically adapting the PA model to capture these slow changes. Finally, pre-distortion for massive MIMO systems suffers from prohibitive cost and power

consumption penalties because each PA's output power at a given time maybe different due to either tapering of the antenna array or just due to part-by-part variation among multiple PAs even in the absence of tapering. These restrictions make even state-of-the-art pre-distortion techniques ineffective for microwave and mm-wave radios with wideband channels except for cases where Watt level power is required.

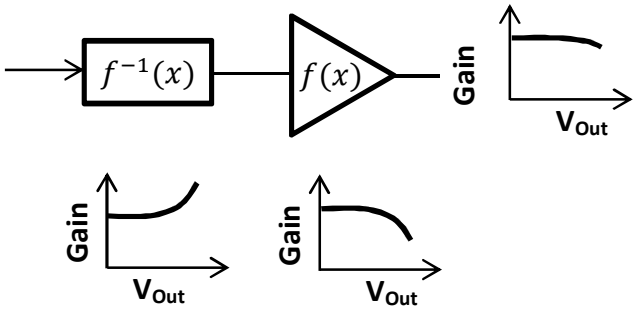


Figure 5.2 Pre-Distortion

5.1.2 Cartesian Feedback

Cartesian feedback utilizes a feedback network around the PA to enforce the output tones of the PA to a linear scaled version of the input tones [35]. The output of the PA is down-converted with an IQ mixer and added to the baseband data before the main IQ mixer (Fig. 5.3). The main advantage of the feedback loop is its capability for linearizing the PA with dynamic changes to the operating conditions such as temperature, load variation, and supply variation as well as part-to-part variation of the same design.

In practice, loop stability limits the application of this method, an issue that is exacerbated even more at microwaves and mm-waves with large channel bandwidths. The loop suffers from small bandwidth due to the group delay of the feedback path. The RF signal at the output of the PA needs to go through many blocks with each contributing some group delay thus

limiting the channel bandwidth over which the error signal's phase is comparable to the baseband signal phase. Another challenge of this approach is the need for a phase shifted version of the LO signal to compensate for the phase delay of the transmit path. With these practical limitations, state-of-the-art feedback linearization is only limited to a few megahertz up to 10MHz [35]. Thus it is not suitable for microwave or mm-wave radios.

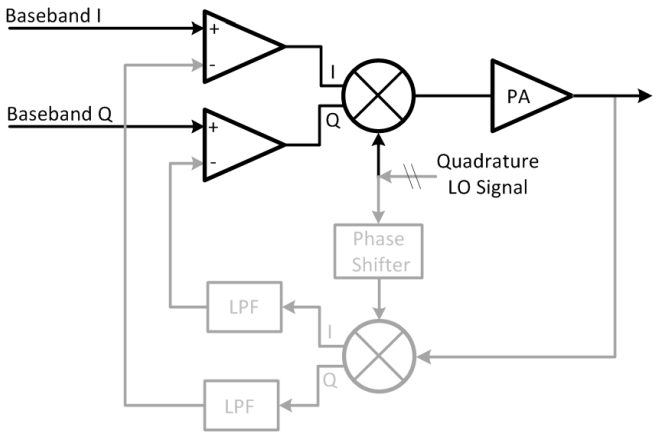


Figure 5.3 Cartesian Feedback

5.1.3 Feedforward

In the feedforward method, output of the PA is scaled by the small signal gain of the PA and subtracted from the PA input signal. The net result is amplified and phase shifted for any error correction and subtracted from the output of the PA. Since there is no feedback loop, the bandwidth and stability issues are greatly reduced compared with the Cartesian Feedback method. The two main issues with this approach are the loss of the final subtractor at the output of the PA (typically in the order of 1dB which results in an overall efficiency degradation of about 20%) and also the gain and phase error between the main PA and the auxiliary path especially with PVT and antenna load variations. Calibrating the latter becomes a more challenging issue with larger channel bandwidth as well.

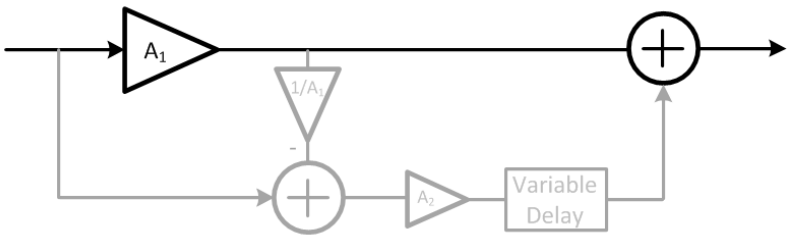


Figure 5.4 Feedforward

5.1.4 Envelop Feedback

In this approach, the output of the PA is scaled down by its small signal gain, its envelop is detected and compared with the envelop of the PA's input signal. The error signal adaptively changes the PA driver's gain to compensate for the main PA's compression in large signal operation. In practice, the envelop or the square of the envelop can be used to change the gain of the PA. If the signal is self-mixed, $|V_{env}(t)|^2$ is obtained. If the signal passes through a limiter that eliminates the envelop, the envelop itself is obtained. In either case, since the signal can be self-mixed, there is no need for a phase shifted version of the LO signal.

In practice, the time delay of the baseband signal going through the PA, scalar, envelop detector (ED), and the op-amp as well as the settling time of the PA driver gain control circuit has to be less than five to ten percent of the $\frac{1}{BW}$ of the baseband signal to avoid stability issues. As an example, imagine the baseband signal is decreasing from its peak value. If the total delay of the loop is large compared with one-tenth of the bandwidth of the baseband signal, by the time the gain of the PA driver is increased the baseband signal has dropped significantly where the main PA is no longer compressed. Consequently, both the PA driver and the main PA have larger gain now resulting in further expansive distortion and possibly a low frequency oscillation.

It is worth noting that this approach does not correct for AM-PM distortion of the PA. It may in fact cause further AM-PM distortion if the phase delay of the PA driver is a function of its gain.

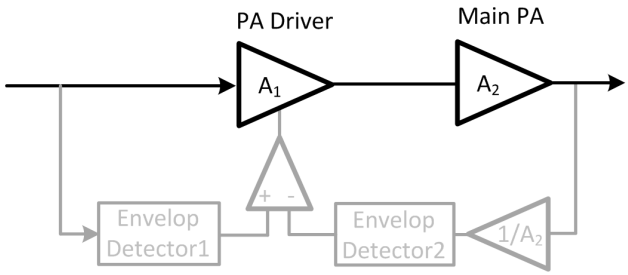


Figure 5.5 Envelop Feedback

5.1.5 Proposed AGPA Approach

The proposed AGPA tracks the envelop of PA output signal and adjusts the gain, phase, and current of the PA thus compensating for both AM-AM and AM-PM distortion. Output of the main PA is self-mixed to obtain the square of the envelop signal thus eliminating the need for a phase shifted LO signal. A simple analog mapping core (AMC) scales the envelop squared signal to generate control signals for adjusting the gain, phase and the current of the PA. Since a large bandwidth (hundreds of megahertz to 1-2GHz) is need at mm-waves, an open loop implementation is chosen. AMC uses digital bits to control the slope and the threshold of the control signals.

These digital settings can be optimized at factory calibration for each radio through the TSSI loop functionality that most mm-wave production radios possess. After proper scaling of the self-mixer output signal by the AMC, the gain of the PA is set by adaptively adjusting resistance of a variable RC feedback network. As the PA starts to compress in large signal operation, feedback resistance is increased to increase the gain of the PA and linearize its gain over a larger output power. Dynamic biasing can also be easily implemented with the existing

AMC with minimal circuit overhead resulting in further improvement of linearity and some DC power saving in low power operation as shown in next sections.

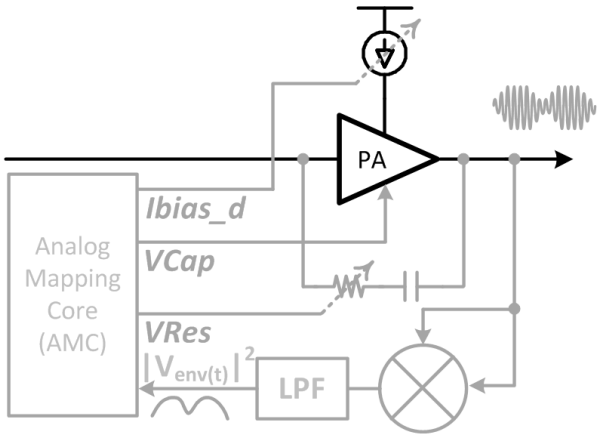


Figure 5.6 Proposed AGPA architecture

5.2 Architecture

5.2.1 Stacked PA Cell

To increase the output power of the PA, a stacked topology is used. To avoid the breakdown of the top cascode transistors (M3 pair), the PA is designed with feedback networks of capacitors C_1 and C_2 and proper sizing of the transistors to divide the total voltage swing across the devices. Analysis from Chapter 4 shows that an optimal gain-power handling trade-off can be obtained if the voltage ratio of the cascode devices to the g_m device is about 1.5, which is implemented in this design.

To avoid drain-oxide breakdown, the cascode devices are implemented in a deep N-well structure. The N-wells are connected to their respective sources with a 10kΩ resistor, thus reducing $v_{drain-bulk}$ and $v_{gate-bulk}$ which makes the PA more reliable.

Inductors l_1 and l_2 improve the power gain of the PA by canceling out the parasitic device capacitors. The inductors are implemented in series instead of shunt to improve the bandwidth of the PA.

Neutralization capacitors are used to cancel out c_{gd} of the g_m transitors (M1 pair) and increase their gain. The neutralization capacitors are implemented with NMOS devices with their sources degenerated with a large resistor. This approach results in a more robust c_{gd} cancelation over PVT compared with using MIM or MOM capacitors.

PA is biased through a diode-connected device with its gate connected to the center tap of the input transformer *X1*. As explained later, the bias current of the PA is the summation of the static *idc1* and the dynamic *ibias_d* (Fig. 5.7). The dynamic *ibias_d* increases with increasing output power when the PA starts to compress. This helps compensate for the drop in G_m in large signal operation mode thus boosting the linearity of the PA.

An adaptively changing RC feedback is used to linearize the PA. As explained later the value of R_{FB} is changed with the output power to compensate for the gain compression of the PA in large signal operation.

A varactor pair C_X is placed between the top cascode device's gate and the top cascode device's source of the opposite branch. As shown later, AM-PM distortion can be partially compensated by adaptive changing value of this varactor.

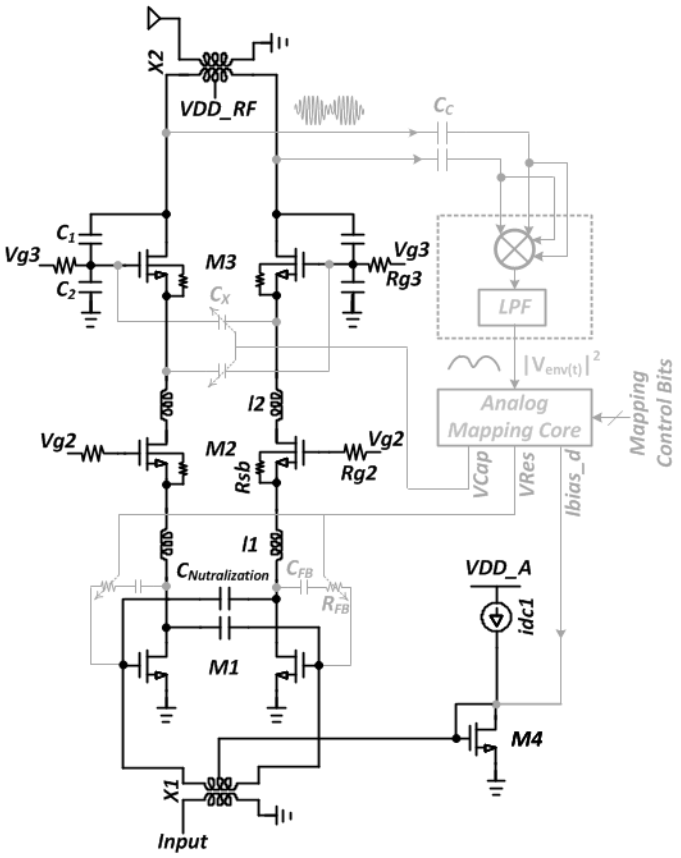


Figure 5.7 AGPA schematic

5.2.2 Self-Mixer

To generate gain and phase correction signals, the envelope of the signal or the square of envelop is necessary. Self-mixing the output signal of the PA and passing it through a low pass filter provides envelop of the signal. Fig. 5.7 shows a simple self-mixer implemented with cross-coupled NMOS and PMOS pairs. When the PA operates in small signal mode, the self-mixer has very low conversion gain and thus does not change the gain, phase and bias control. When the PA's output power is large, it passes a current to the diode-connected device M3 and thus generates a gate voltage. With proper sizing of the self-mixer device sizes (M1 and M2 pairs) and the diode-connected device M3, the desired V_{in} to V_{Rect} mapping can be obtained.

5.2.3 Analog Mapping Core (AMC)

The Analog Mapping Core (AMC) maps the generated V_{Rect} to proper values with proper slopes for each of the gain, phase and bias control lines. This is done simply by a number of current mirrors with variable slopes and variable initial bias points. Depending on whether the slope of the control line needs to be positive or negative with increasing output power of the PA, a scaled version of the current passing though the transistor M3 is added or subtracted from a fixed current (Fig. 5.8).

5.2.4 Gain Control (Variable RC Feedback)

To compensate for the compression of the PA in large signal operation, a variable RC feedback network is implemented between the gate and the drain of the g_m device (Fig. 5.7). The variable resistor is implemented with an NMOS in triode with the drain and the source connected to ground through a larger resistor. This improves the linearity of the switch. The gate of the NMOS resistor is controlled by the Analog Mapping Core. As the output power of the PA increases and the PA starts to compress, V_{Res} decreases thus increasing the resistance of the variable resistor. Since the negative feedback strength of the g_m device decreases by increasing R_{FB}, gain of the PA starts to increase and thus PA compression is compensated. The threshold and the slope of this mechanism is set by I_{Res} and digital bits *r1-rn.* If I_{Res} is increased, the value of the R_{FB} would start to increase at a higher output power because the current through M3 needs to be at a higher value to reach the same gate voltage on variable resistor. If more of *r1-rn* switches are turned ON, the resistance of the switch would increase more sharply with increasing output power.

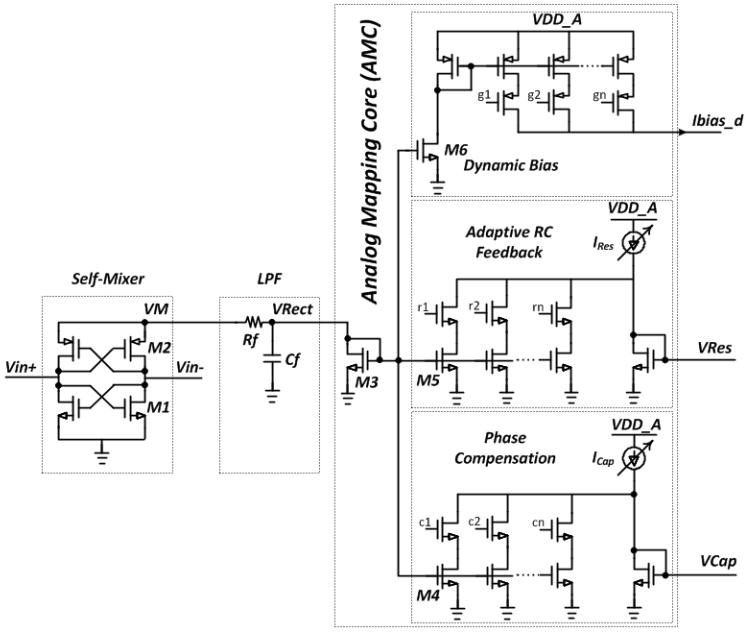


Figure 5.8 AGPA auxiliary circuits

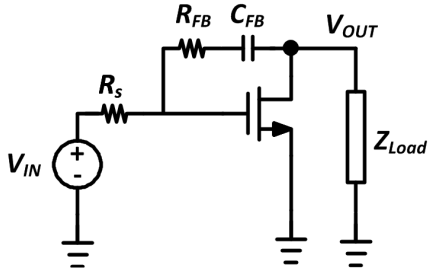


Figure 5.9 A common source amplifier with RC feedback

$$A_V = -\frac{Z_{Load}\left(g_m + s * C_{FB}(g_m * R_{FB} - 1)\right)}{1 + s * C_{FB}(R_{FB} + R_S + Z_{Load} + g_m * R_S * Z_{Load})} \tag{5.1}$$

$$Zero: s_z = -\frac{1}{\mathrm{C_{FB}} * \mathrm{R_{FB}}} \quad (Assuming: \mathrm{g_m} * \mathrm{R_{FB}} \gg 1) \tag{5.2}$$

$$Pole: s_p = -\frac{1}{\mathrm{C_{FB}}(\mathrm{R_{FB}} + \mathrm{R_S} + \mathrm{Z_{Load}} + \mathrm{g_m} * \mathrm{R_S} * \mathrm{Z_{Load}})} \tag{5.3}$$

If the pole and zero are not located at frequencies less than 10% of the operating frequency, as the value of $\mathrm{R_{FB}}$ increases, the zero moves to the left more than the pole. This

results in a positive phase change at the output node (This effect is shown to cause about 0.5º of phase distortion in simulations of the entire PA with the linearization loop turned ON and the phase compensation and dynamic bias controls disabled; see Fig. 5.11). To linearize the gain of the PA, R_{FB} is increased as the output power of the PA is increased thus resulting in a positive phase distortion. To minimize this unwanted phase change, the value of C_{FB} should be increased to push the pole and the zero well below the operating frequency so that their movement does not affect the PA output phase. Large C_{FB} implemented with MIM or MOM capacitors, however, is challenging due to the self-resonance of metal capacitors and the parasitic bottom plate capacitance. Consequently, a phase correction loop is designed to correct for this phase distortion as explained later.

5.2.4 Dynamic Bias

The dynamic bias control voltage increases the DC current of the PA with increasing output power to compensate for the drop in the large signal effective G_m. It improves the OP1dB of the PA by about 1.6dB. It also helps reduce the phase distortion. The dominant phase distortion are caused by the variation of parasitic device capacitors and the movement of the poles due to reduction of G_m. As seen in (3), as G_m compresses due to large signal operation, the pole is pushed to the right resulting in a net positive output phase change. By dynamically increasing current through the device in large signal operation mode, G_m compression is compensated and the pole is held more in place thus compensating for the AM-PM distortion. This phenomenon is observed in the AM-PM simulation of the entire PA (Fig. 5.11).

Adaptive bias has extensively been used to linearize PAs with minimal circuit overhead. In fact due to the square law dependence of current on the gate voltage, transistor's DC current inherently increases as the input power increases:

$$\left(\partial^2 I \Big/ \partial^2 v_g > 0\right) \qquad (5.4)$$

One challenge, however, of conventional dynamic bias circuit is the unwanted gain expansion that occurs when the transistor is de-biased aggressively. [36] shows 6dB of gain expansion when adaptive bias is enabled, for example. Programmability of the activation threshold and the slope of dynamic bias is an issue that needs to be addressed for production worthy PAs relying on dynamic bias. The proposed AMC block enables both activation and power-dependent slope control by means of digital controls.

5.2.5 Phase Correction

To compensate for the AM-PM distortion, a cross-connected varactor between the gates and sources of the top cascodce device is used (C_X in Fig. 5.7). To demonstrate the idea, the transfer function of the top cascode device with the cross-connected capacitor is derived (Fig. 5.10 , (5.5) and (5.6)). Derivate of the phase of the voltage transfer function with respect to is C_X is monotonically negative which means that a desired phase shift can be obtained with a proper control voltage from AMC. Monotonicity of the phase change is important and simplifies the design of the control voltage generated by the AMC. It is worth noting that the required phase change range is only in the order of couple of degrees because the aim of the block is to correct for AM-PM distortion of the PA and the variable RC network each of which only contribute only

one to two degrees (Fig. 5.11). Simulation results show that a 10% change provides about 0.5º of AM-PM correction. Note that 10% change in C_X has minimal effect on the gain.

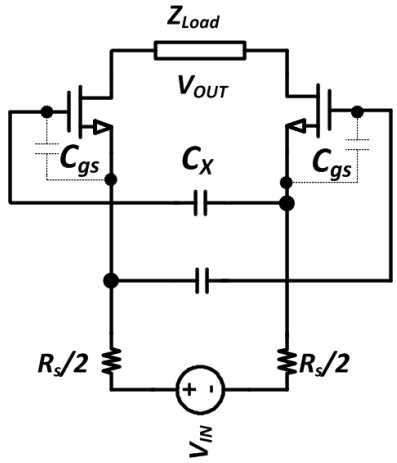


Figure 5.10 Phase correction through C_X

$$A_V = \frac{C_X * g_m * Z_{Load}}{C_{gs} + C_X + C_X * g_m * R_S + 2 * C_{gs} * C_X * R_S * s} \tag{5.5}$$

$$\frac{\partial \angle A_V}{\partial C_X} = -\frac{2 * C_{gs}^2 * R_S * \omega}{\left(C_{gs} + C_X + C_X * g_m * R_S\right)^2 + \left(2 * C_{gs} * C_X * R_S * \omega\right)^2} \tag{5.6}$$

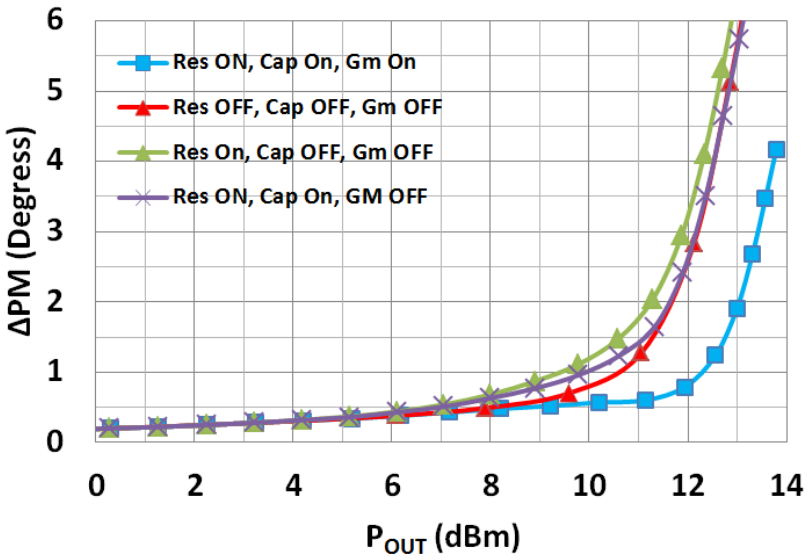


Figure 5.11 Simulated phase distortion *(f=57GHz)*

5.3 Simulation and Measurement Results

Fig. 5.12 shows the simulated s-parameters of the PA. The s-parameters do not change with the AGPA switched ON or OFF because AGPA loop is inactive in small signal operation. It is only in large signal operation that AGPA activates and linearizes the PA.

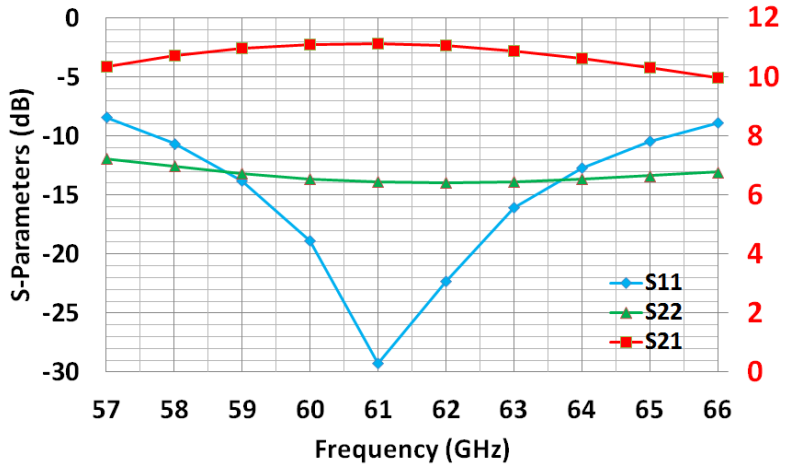


Figure 5.12 Simulated s-parameters of the PA

Fig. 5.13 shows the simulated improvement of OP1dB of the PA with AGPA turned ON. With the AGPA switched OFF, the difference between OP1dB and P_{SAT} is 3dB (OP1dB=10.2dBm, P_{SAT}=13.2dBm). Turning ON the AGPA loop improves the OP1dB by 2.5dB (OP1dB=12.7dBm, P_{SAT}=13.8dBm). Note that the difference between P_{SAT} and OP1dB in this case is only 1.1dB. Turning ON AGPA improves the P_{SAT} by 0.6dB as well due to the dynamic bias loop.

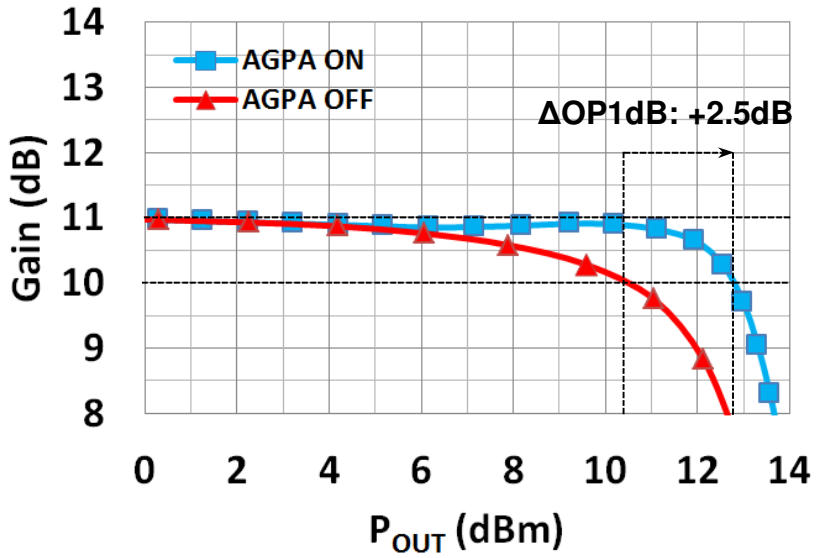


Figure 5.13 Simulated Large Signal Performance of the PA

Fig. 5.14 shows the simulated and measured small signal gain of the PA across frequency. The measured data is downshifted by about 10%. The PA has more gain in measurement than in simulation. This is likely due to pessimistic models and over-estimated ground resistance during extraction.

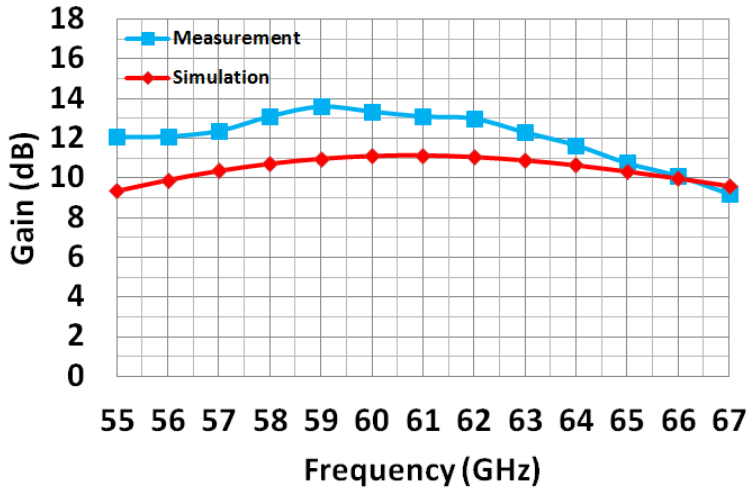


Figure 5.14 Simulated and measured small signal gain

Figure 5.15 shows the measured large signal compression of the PA with and without the AGPA loop. The proposed loop improves the OP1dB of the PA by a 2.8dB bringing OP1dB within 1.3dB of P_{SAT}. This agrees well with simulation results. As shown in Fig. 5.16, the improvement in OP1dB does not have a significant power overhead (for the same output power, the PAE is similar with and without the linearizer.) The AGPA loop enhances the efficiency at OP1dB from 6.5% to 10.5%.

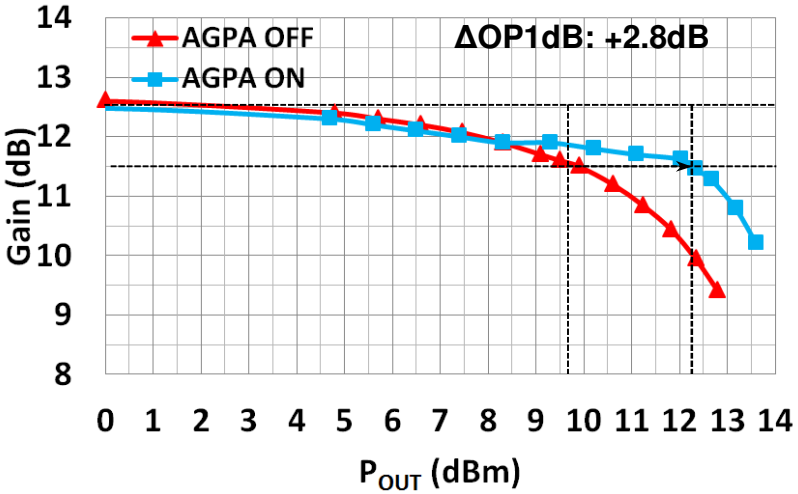


Figure 5.15 Measured OP1dB improvement of AGPA (f=57GHz)

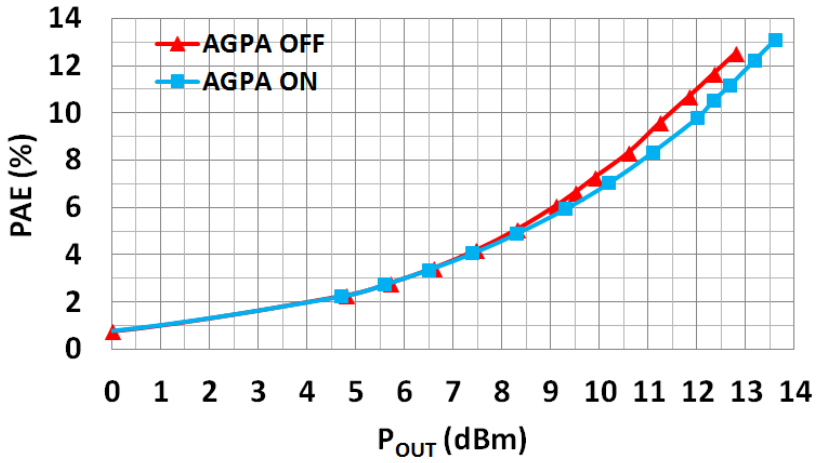


Figure 5.16 Measured PAE of AGPA (f=57GHz)

Two-tone tests are used to characterize the dynamic behavior of the PA with AGPA ON and OFF. Figures 5.17 and 5.18 show the IM3 power in each tone vs. power of a single fundamental tone. For low output powers, AGPA loop is inactive and the IM3 power for both conditions are similar. As the output power of the PA increases, the difference between the IM3 powers for the two test cases increases. When P_{OUT} reaches 8dBm, AGPA reduces the IM3 power by 3dB when the tone spacing is 200MHz. This is one of the largest tone spacing reported in publications demonstrating the wide bandwidth nature of the proposed AGPA. At 1GHz tone spacing, the linearizer reduces the IM3 power by about 1dB at high output power levels.

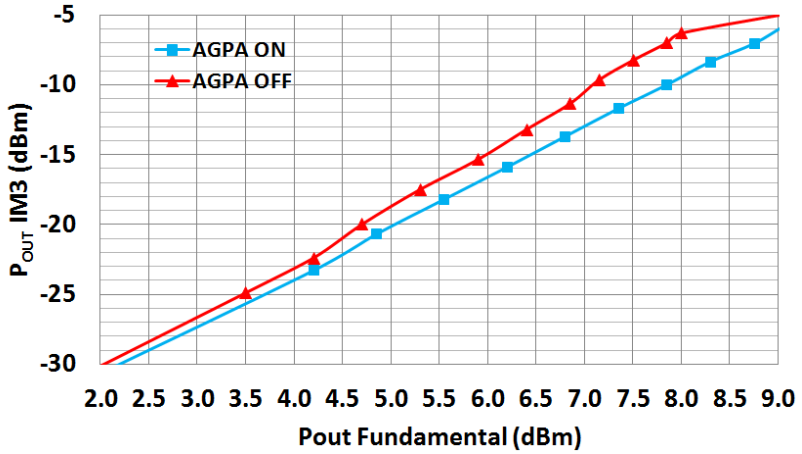


Figure 5.17 Measured IM3 of AGPA
($\Delta f = 200MHz, f1 = 56.9GHz, f2 = 57.1GHz$)

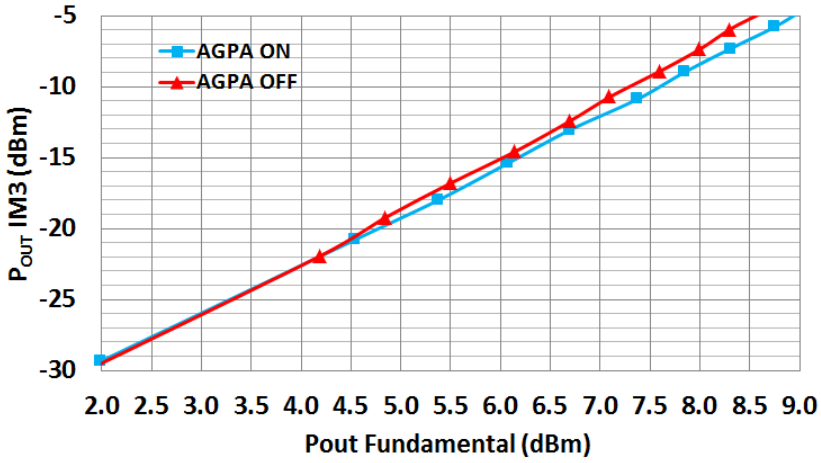


Figure 5.18 Measured IM3 of AGPA
($\Delta f = 1GHz, f1 = 56.5GHz, f2 = 57.5GHz$)

Table I shows the comparison of this PA with state-of-the-art CMOS 60GHz PAs. The PA has a higher efficiency compared with other recent published work and better linear power per area except for [6], which uses a special SOI process with lower loss passives and also a special feature of having access to a back-gate terminal that is used for adjusting the device threshold and thus obtaining some inherent linearization. Table II shows the comparison of this linearization technique with state-of-the-art PA linearization publications. The proposed

technique has a comparable performance improvement but at more than 10x the channel bandwidth with only 3mW of power consumption overhead.

Table 5-1 Overview of state-of-the-art mm-wave CMOS PAs

	This Work	**RFIC '13 [2]**	**ISSCC '11 [1]**	**ISSCC '10 [3]**	**ISSCC '15 [6]**
Technology	28nm HPM	40nm CMOS	65nm CMOS	65nm CMOS	28nm UTBB FS-SOI
Supply (V)	2.4	1.2	1	1	0.8
Gain (dB)	13	29	19.2	19.2	15.4
OP1dB (dBm)	12.3	17	15	15.1	18.6
P_{SAT} – OP1dB (dB)	1.3	5.6	3.2	2.6	0.7
PAE @ OP1dB	10.5%	3%	7%	7%	15%
Area (mm^2)	0.0675	2.16	0.28	0.83	0.162
OP1dB/Area (mW/mm^2)	250	23	112	39	407

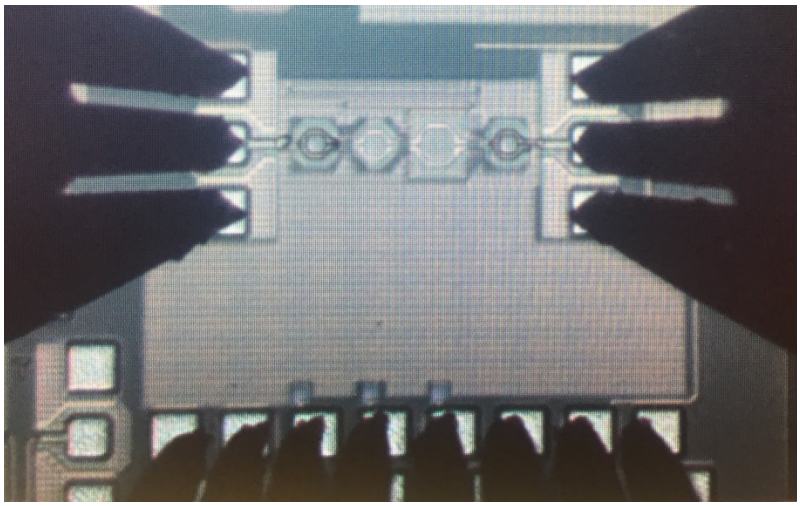


Figure 5.19 Die photo

Table 5-2 Overview of state-of-the-art linearization techniques

	This Work	JSSC '12 [37]	JSSC '10 [35]
Technology	28nm HPM	130nm CMOS	130nm CMOS
Linearization Technique	AGPA	PA-Closed Loop	Cartesian Loop Back
Frequency (GHz)	57	1.88	2
Bandwidth (MHz)	200	3.8	10
Improvement in OP1dB (dB)	2.8	0.9	-
Improvement in PAE	1.6X	1.17x	-
IM3 or ACLR Improvement (dB)	3dB (ΔIM3)	6dB (ΔACLR)	8.2dB (ΔACLR)
Linearizer Power Consumption	3mW	28.3mW	-
PA OP1dB	12.3dBm	29dBm	-

5.4 Conclusion

Stacking is shown to be a practical solution for increasing the saturated output power of mm-wave PAs. It, however, suffers from lower linear power due to the contribution of multiple non-linear devices compared with a simple common source PA. The proposed linearization technique resolves this issue and pushes the PA OP1dB very close to its P_{SAT} thus requiring a smaller backoff for a given EVM requirement.

The proposed linearization technique is also suitable for PAs at lower frequencies where large channel bandwidths are used (e.g., microwave PAs with 200-300MHz channel bandwidth). Being self-contained with minimal reliance on auxiliary circuits makes this technique of particular interest for massive phased arrays of the future.

Chapter 6

Conclusion

The goal of the work presented in this dissertation is to find solutions to some of the challenges of high frequency, high performance circuits, mainly in the realm of low phase noise oscillators and high power linear PAs. The dissertation concludes with the summary of contributions.

6.1 Summary

Chapter 2 introduced a novel approach for designing low phase noise oscillators with large bandwidth and exceptional FOM. One of the 1st demonstrations of mm-wave coupled oscillators in CMOS is presented, its locking method is explained using simple arguments and state-of-the-art performance phase noise performance is demonstrated.

Chapter 3 shows how large-scale power combiners can be done to achieve large powers at mm-waves in standard CMOS technology. Novel passive designs and combining techniques

are used to achieve 22.6dBm at 60GHz in standard bulk CMOS. At the time of writing this dissertation, this is the highest reported P_{SAT} at this frequency in bulk CMOS.

Chapter 4 covers stacked PA design in mm-waves and demonstrates the gain-reliability trade-off of voltage swing allocation for stacked PAs. A case study of three unit cell PA serves to guide how combining/stacking can be utilized together to achieve high power, high frequency PAs.

Chapter 5 covers a novel linearization technique for microwave/mm-Wave PAs with large channel bandwidths. To our knowledge, this is the first self-contained linearization technique for 10-20dBm PAs correcting for both AM-AM and AM-PM distortion at very high speeds at the time of writing this dissertation. It improves OP1dB of the PA by 2.8dB at 57GHz. PAE at OP1dB is improved from 6.5% to 10.5% with the linearization loop activated.

The proposed techniques have immediate applications in microwave and mm-wave phased array systems with *Gbps* data rates. These systems are currently under intensive research and development due to their emerging application from last-mile backhaul wireless systems to distributing internet from low orbit satellites and more.

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