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Ensembles of indium phosphide nanowires: physical properties and functional devices integrated on non-single crystal platforms

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Abstract A new route to grow an ensemble of indium phosphide single-crystal semiconductor nanowires is described. Unlike conventional epitaxial growth of single-crystal semiconductor films, the proposed route for growing semiconductor nanowires does not require a single-crystal semiconductor substrate. In the proposed route, instead of using single-crystal semiconductor substrates that are characterized by their long-range atomic ordering, a template layer that possesses short-range atomic ordering prepared on a non-single-crystal substrate is employed. On the template layer, epitaxial information associated with its short-range atomic ordering is available within an area that is comparable to that of a nanowire root. Thus the template layer locally provides epitaxial information required for the growth of semiconductor nanowires. In the particular demonstration described in this paper, hydrogenated silicon was used as a template layer for epitaxial growth of indium phosphide nanowires. The indium phosphide nanowires grown on the hydrogenerated silicon template layer were found to be single crystal and optically active. Simple photoconductors and pin-diodes were fabricated and tested with the view towards various optoelectronic device applications where group III–V compound semiconductors are functionally integrated onto non-single-crystal platforms.

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1 Introduction

High-quality single-crystal substrates have been used for epitaxial growth of high-quality semiconductor films when large area is required for device fabrication. As a result, significant efforts have been dedicated to developing epitaxial growth processes that produce semiconductor films that are homogeneous in composition and uniform in thicknesses over required area. Even in the synthesis of nanometer-scale semiconductor structures such as quantum dots and nanowires, the use of single-crystal substrates is very common. For example, self-organized InAs quantum dots have been extensively studied on single-crystal GaAs (100) [1]. Epitaxial growth of semiconductor nanowires generally makes use of single-crystal substrates. The growth of group III–V compound semiconductor nanowires has been demonstrated almost exclusively on single-crystal substrates. In Particular, GaAs or InP nanowires were grown on single-crystal group III–V compound semiconductor substrates [2] or on single-crystal Si substrates [3]. In the growth of semiconductor nanowires on single-crystal substrates, the surface of a single-crystal substrate provides epitaxial information (e.g., crystallographic symmetries and lattice constants,

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etc.) to "seed" nanowires in the early stage of their evolution.

A variety of growth mechanisms have been suggested for the various types of nanowires [4, 5]. The growth of nanowires can be viewed as a significantly complicated process due partly to the mechanism that leads to quasi one-dimensional shapes resulted from strong anisotropy in growth rate in two different directions (i.e., directions perpendicular and parallel to a nanowire's long axis). Another feature contributing to various complications of the growth of nanowires is the presence of metal catalysts (e.g., metal-catalyzed nanowires grown with the presence of transition metal or noble metal particles) [6–8]. Catalyst-free nanowire growth was also suggested [9–11], however the level of complications involved in analyzing the growth of nanowires without metal-catalysts appears to be much higher than that in metal-catalyzed nanowire growths. Therefore, the discussion on the role played by single-crystal substrates in the growth of nanowires, with or without metal catalysts, appears to be still in its infancy. However, it is conceivable that if an individual nanowire seed "sees" short-range atomic order within an area on the scale that is comparable to or moderately larger than the size of the nanowire seed, an individual nanowire would not be able to tell whether it sits on a single-crystal substrate or a small crystallite in a non-single-crystal substrate. Apparently the major difference between the two cases is that two different locations on the surface of a single-crystal substrate are correlated with its specific crystallographic translational operation, whereas two different small crystallites that exist in a non-single-crystal substrate are not crystallographically correlated. This implies that as long as geometrical synchronization or organization among a group of nanowires is not required, the use of a single-crystal substrate for the growth of nanowires is not a required condition [12].

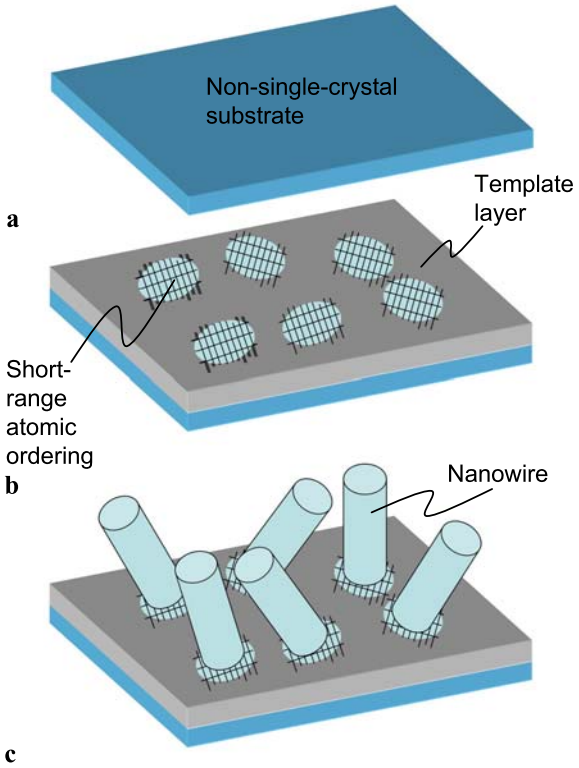

Fig. 1 Structural concept of the proposed route to grow semiconductor nanowires on a non-single-crystal substrate is schematically shown. A starting substrate in (**a**) can be chosen from various types of non-single-crystal including amorphous and poly-crystal. Once an appropriate non-single-crystal substrate is obtained, a template layer is prepared on the non-single-crystal substrate as in (**b**). The template layer can be made of a variety of materials as long as the template layer "locally" exhibits short-range atomic ordering on its surface. After nanowires are grown in (**c**), an ensemble of nanowires can be electrically accessible through the template layer

2 Structural concept

The structural concept of what is proposed is rather simple as schematically illustrated in Figs. 1(a)–(c). As postulated in the introduction, a starting substrate can be chosen from various types of non-single-crystals including amorphous and poly-crystalline materials (note that there are a wide range of variations in this class of material, e.g., microcrystalline and nanocrystalline, etc.). Although a non-single-crystal substrate can be chosen from such materials as glass, metal, or ceramics, one of the requirements that need to be carefully addressed when a non-single-crystal substrate is selected is related to the fact that a non-single-crystal substrate needs to withstand all successive process steps. A selected non-single-crystal substrate has to be physically and chemically stable at every process step in the fabrication process required for a device. This is why it is significantly advantageous to design a series of device fabrication processes by placing a process step that can be carried out at as low temperature as possible.

Once an appropriate non-single-crystal substrate is obtained in Fig. 1(a), a template layer is prepared on the non-single-crystal substrate as shown in Fig. 1(b). The template layer can be made of a variety of materials as long as the template layer "locally" exhibits short-range atomic ordering on its surface. It is this short-range atomic ordering that is transferred, in the same sense as that in conventional epitaxial growth of a single-crystal film on a single-crystal substrate, to semiconductor nanometer-scale structures such as nanowires. When semiconductor nanowires are grown on a surface of a single-crystal substrate, specific crystallographic information required for nanowire growth must be linked to long-range atomic ordering that extends over several centimeters on a single-crystal substrate. However, as postulated earlier, it is conceivable that atomic ordering that

exist on the scale comparable to or several times the diameter of a nanowire is the quantity critically relevant to the formation of epitaxial single-crystal nanowires.

Although semiconductor single-crystal nanowires have been formed on non-single-crystal surfaces that were electrically insulating [13–15] in order to establish an electrical access to a single nanowire, it is more advantageous, in specific applications, to form an ensemble of single-crystal semiconductor nanowires with their one end electrically connected onto a template layer as in Fig. 1(c). It is further advantageous if electrical properties of the template layer are explicitly controlled because then an ensemble of nanowires can be electrically accessed through an electrically conductive template layer. In the idea we are proposing, two intriguing characteristics to be emphasized are: (1) epitaxial growth of semiconductor nanostructures can be achieved on a non-single-crystal substrate by employing a template layer that possesses short-range atomic ordering, and (2) an ensemble of semiconductor nanowires can be electrically accessed from external circuits by having a template layer that is electrically conductive.

In our first demonstration, hydrogenated silicon (Si:H) in either amorphous or microcrystalline phases was chosen as the material for a template layer. Si:H is essentially a semiconductor that can be doped in a controlled manner to explicitly tune its electrical transport properties, which is significantly advantageous when devices that require pn junctions or ohmic contacts are designed. For instance, unintentionally doped nanowires (intrinsic-type) can be sandwiched between a p-type Si:H and an n-type Si:H layers to build a pin diode as described in later sections.

The sample preparation begins with a non-single crystal semiconductor substrate (e.g., quartz substrate in this case) shown in Fig. 1(a). As in Fig. 1(b), a Si:H template layer that provides a surface possessing short-range atomic ordering is prepared on the quartz substrate. Thickness of the Si:H template layer is approximately 200 nm. The Si:H template is deposited by, for instance, plasma-enhanced chemical vapor deposition (PECVD) with silane and hydrogen used as precursors. The thickness and deposition conditions were carefully tuned to ensure that a large number of nanometer-scale silicon crystallites which provide short-range atomic ordering were formed within an amorphous matrix in the Si:H template layer. Three types of Si:H template layers, unintentionally doped, boron-doped (i.e., p-type), and phosphorous-doped (n-type), were prepared. In addition to quartz substrates, various substrates including, stainless steel (type 304), Si substrates coated with a 300-nm chromium layer, and amorphous silicon dioxide thermally prepared on a single-crystal Si substrate (i.e., a-SiO_2/Si) were used and covered by depositing a Si:H template layer [16]. After the Si:H template layer is prepared, colloidal gold nanoparticles (Au–NPs) with nominal diameter of 10 nm were dispensed onto the template layer. Subsequently, indium phosphide (InP) was grown by metalorganic chemical vapor deposition using trimethyilindium and phosphine as precursors as in Fig. 1(c).

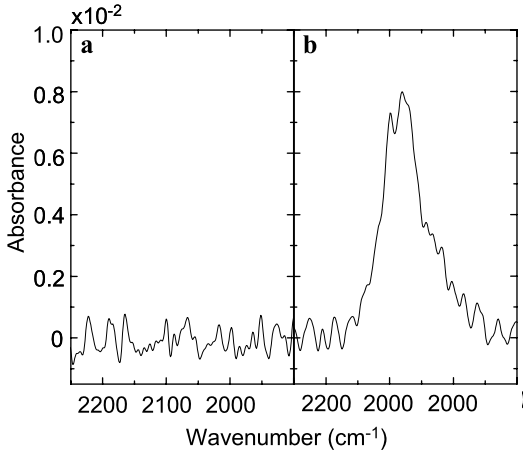

Fig. 2 Reflection absorption infrared spectroscopy (RAIRS) data collected from (**a**) an a-SiO_2/Si substrate and (**b**) an as-deposited amorphous Si:H template layer on an a-SiO_2/Si substrate

3 Characteristics of Si:H template layers

Figures 2(a) and (b) show reflection absorption infrared spectroscopy (RAIRS) data collected from (a) an a-SiO_2/Si substrate and (b) an as-deposited Si:H template layer on an a-SiO_2/Si substrate. The RAIRS measurement was done in nitrogen atmosphere at room temperature. The spectrum was collected in the range of 2350–1900 cm^{-1} where several Si–H vibration modes exist, [17] exhibiting the broad absorption spectrum in (b), while no peak was seen in (a). Fitting the spectrum to known Si–H_n ($n = 1$–3) vibrational modes revealed that the major component was the Si–H_2 stretching mode at ~2082 cm^{-1}, suggesting that the major part of the as-deposited Si:H template layer was amorphous silicon (a-Si:H) [18]. It is conceivable that the as-deposited Si:H template layer could further crystallize via either homogeneous or heterogeneous nucleation processes during subsequent InP nanowire growth even though the growth temperature for InP nanowires is well below the glass transition temperature range reported for amorphous silicon [19, 20]. Nanometer-scale silicon crystallites embedded in the amorphous matrix of the Si:H template layer and exposed at the surface provided the epitaxial information during the InP nanowire growth step.

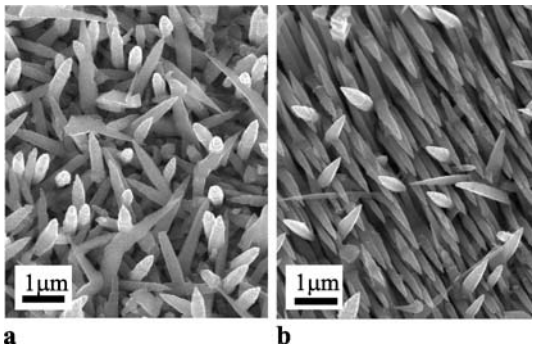

Fig. 3 Scanning electron microscopy (SEM) images of InP nanowires on (**a**) the *a*-Si:H template layer surface and (**b**) a reference surface, single-crystal GaAs(100) substrate

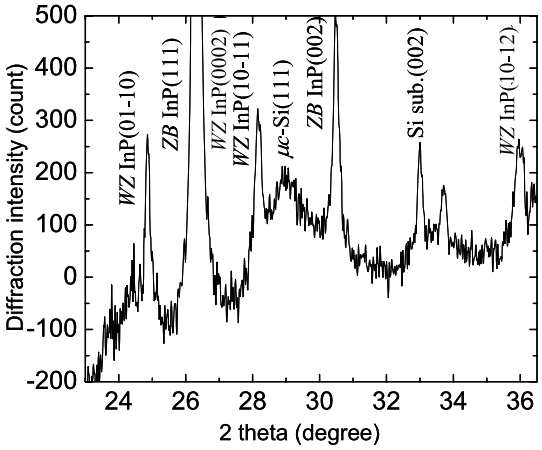

Fig. 4 XRD profile collected from the ensemble of InP nanowires is shown, indicating that both *WZ* and *ZB* InP nanowires co-exist

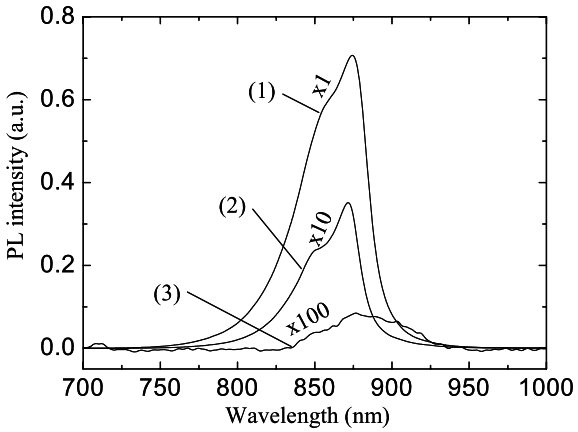

Fig. 5 A set of micro-photoluminescence spectra collected from the ensemble of InP nanowires at room temperature

4 Characteristics of InP nanowires

InP deposited on the Si:H template layer prepared on an *a*-SiO_2/Si(100) substrate with the presence of Au–NPs was found to form nanowires. Figure 3 shows scanning electron microscopy (SEM) images of InP nanowires on (a) the *a*-Si:H template layer surface and (b) a reference surface, single-crystal GaAs(100) substrate. In (a) all nanowires appear to be randomly oriented. In contrast, nanowires in (b) are aligned along one of four ⟨111⟩ directions with respect to [100]GaAs, indicating that the surfaces of the *a*-Si:H layer works as a template for nanowire growth. Two different crystal habits are identified in (a), suggesting that two types of nanowires having different lattices co-exist, that is, as evidenced in (a), two types of nanowires having either triangular cross section (triangular nanowire) or hexagonal cross section (hexagonal nanowire) co-exist. As clearly seen in (a), the nanowires have tapered shapes with a wide base and a sharp tip. Nominal geometrical dimensions of the two types of nanowires are summarized as follows; the length is approximately $1.5–2 \times 10^{-6}$ m, and the lateral size at its bottom is approximately 300–500 nm. Tapering angle (i.e., the angle between a long axis and a side wall) is in the range of 33–39°. On a triangular nanowire, at least, one of the three side walls that bound the nanowire exhibits significant morphological roughness, which would be an indication that there was a substantial nonuniformity in the growth rate in the direction perpendicular to the long axis of the triangular nanowires. The hexagonal nanowire exhibits a number of "kinks" along its ridge, which would indicate the existence of rotational twins generated during the growth. Preliminary transmission electron microscopy studies indicated that the InP nanowires have either zincblende (*ZB*) crystal structure or wurtzite (*WZ*) crystal structure, presumably corresponding to the two types of nanowires having triangular and hexagonal cross sections, respectively.

XRD profiles collected from the ensemble of InP nanowires shown in Fig. 3(a) are displayed in Fig. 4. As discussed, the two types of nanowires, *ZB* and *WZ*, are clearly distinguishable by indexing multiple well-resolved peaks denoted as either *ZB* or *WZ*. The multiple peaks seen in Fig. 4 indicate that the nanowires are randomly oriented with respect to the surface normal of the substrate. A broad peak (peak intensity ∼80 counts) spanning between 28 ∼ 29° can be attributed to Si(111) associated with the *a*-Si:H template layer, which suggests that the as-grown *a*-Si:H template layer would have undergone solid-phase crystallization (i.e., microcrystalline silicon, *mc*-Si:H) during the InP nanowire growth because an as-prepared Si:H template layer is amorphous.

A set of micro-photoluminescence (μ-PL) spectra collected at room temperature is shown in Fig. 5. Each spectrum is plotted with the original PL intensity multiplied by a factor denoted as ×100, ×10, and ×1 for better readability. In the μ-PL measurement, a ensemble of InP nanowires was excited with an Ar laser having beam diameter of approximately 1.5 μm. Three different excitation power densities, 6×10^3, 6×10^2, and 6×10^1 W cm^{-2}, were used for the

three spectra (1), (2), and (3), respectively. Both peak intensity and integral intensity were found to change nonlinearly with the change in the excitation power density, which suggests the presence of strong nonlinear carrier dynamics within the ensemble of InP nanowires. Spectra (1) and (2) were deconvoluted into two Lorentzian peaks centered at 854 and 875 nm, which were shorter than the bandgap wavelength of bulk *ZB* InP by 71 and 50 nm, respectively, suggesting the presence of significant blue shift presumably associated with strong quantum confinement [16].

The origin of the two Lorentzian peaks can be surmised based on the XRD and the TEM analysis. Both *ZB* and *WZ* InP nanowires were found to co-exist on the Si:H. Calculations of the electronic band offset between *WZ* and *ZB* at a hetero-interface for various semiconductors suggest that the bandgap of *WZ* InP differs from that of *ZB* InP by +84 meV [21]. Blue shift caused by quantum confinement of excitons has been reported to vary 50–110 meV depending on the diameter (50–15 nm) of nanowires, [13] thus we assign the two Lorentzian peaks to the emissions from the *WZ* InP nanowires with quantum confinement and from the *ZB* InP nanowires with quantum confinement. In the SEM image shown in Fig. 3(a), the diameter of the tapered nanowires changes from 300 to 10 nm along the growth axis, implying that radiative recombination of excitons must take place within a volume close to the tip of the nanowires in order for the level of quantum confinement to be observed. Residual strain along the direction perpendicular or parallel to the growth direction of the nanowires could have also shifted the bandgap energy [22] or split degenerate hole bands into heavy hole and light hole sub-bands [23]. However, neither the TEM nor the XRD analysis indicated measurable elastic deformation that could have solely accounted for the observed blue shift.

5 InP nanowire photoconductors

In fabricating photoconductors that implement InP nanowires, an amorphous surface was prepared by growing a thick silicon dioxide (SiO_2) layer on a 4-in. Si(100) substrate as in Fig. 6(a). Subsequently, a stack of metal films was deposited onto the SiO_2 surface. The metal films were patterned into a pair of planar ohmic electrodes. A heavily doped n^+mc-Si:H layer was deposited onto the patterned metal electrodes. The n^+mc-Si:H film was then patterned into two segments spatially separated by 2 μm apart and electrically isolated from each other. The processed wafer was then coated with a suspension of colloidal Au particles with a nominal diameter of 10 nm. Finally, InP was deposited by low-pressure metalorganic chemical vapor deposition. InP grew into randomly oriented InP nanowires formed selectively onto the n^+mc-Si:H segments. The

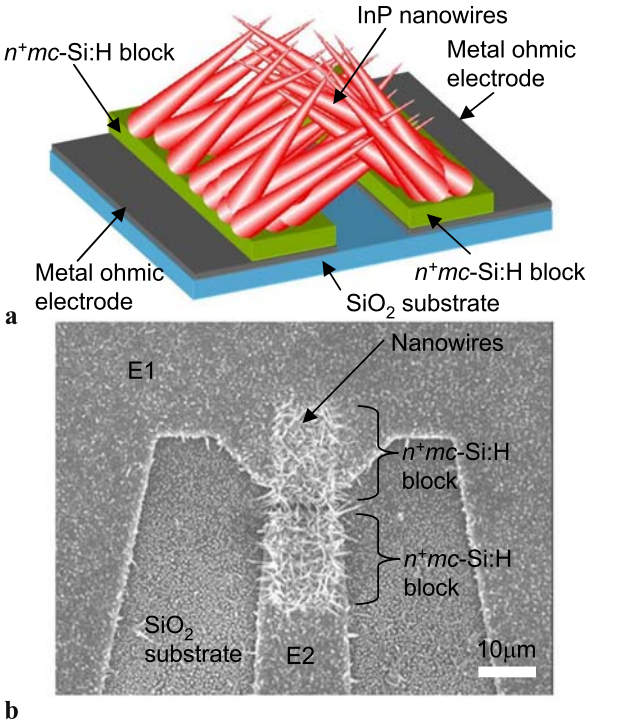

Fig. 6 InP nanowire photoconductor is schematically shown in (**a**). A planar structure in which InP nanowires can be selectively formed on n^+mc-Si:H surface offers great flexibility and simplification in building devices that employ an ensemble of InP nanowires. Shown in (**b**) is an SEM top-view image collected on a representative InP nanowire photoconductor consisting of a pair of metal ohmic electrodes (labeled E1 and E2) in a coplanar configuration that allows us to perform high speed testing

nanowires bridged the gap by either fusing themselves or bridging across the gap between the two n^+mc-Si:H segments. A planar structure in which InP nanowires can be selectively formed on n^+mc-Si:H surfaces offers great flexibility and simplification in building devices that employ an ensemble of InP nanowires. We used this planar structure to evaluate photoconductive properties of an ensemble of InP nanowires.

Shown in Fig. 6(b) is an SEM top-view image collected on a representative InP nanowire photoconductor consisting of a pair of metal ohmic electrodes (labeled E1 and E2) in a coplanar configuration that allows us to perform high-speed testing [24, 25]. The two n^+mc-Si:H segments were entirely covered by InP nanowires, whereas very few nanowires were observed elsewhere even though the Au nanoparticles were dispersed uniformly over the entire surface. The fact that the nanowire growth was selectively catalyzed on the n^+mc-Si:H segments suggests that short-range atomic order on the surfaces of the n^+-Si:H segments is a required condition for nanowire growth as postulated. A large number of randomly oriented nanowires are clearly seen on the two n^+mc-Si:H segments. Detailed inspection by viewing from the side revealed that many of the nanowires approach-

ing from the two facing n^+mc-Si:H segments collided and "fused" together in free space, which established multiple electrical paths that bridged the two n^+mc-Si:H segments. The random orientation manifested by the nanowires ensures that these nanowires collide and fuse together.

DC current–voltage (IV) characteristics of the InP nanowire photoconductor were measured at room temperature and plotted in Fig. 7(a). The IV characteristics are remarkably symmetric with respect to 0 V and essentially ohmic, revealing a clear contrast to nonlinear characteristics observed in ZnO nanowires bridging two Zn electrodes [26]. Photoresponse was obtained by illuminating the device with a laser beam at 633 nm. A 633-nm laser beam with various optical powers (6×10^{-7} to 5×10^{-6} W) was used to illuminate the gap between the two n^+mc-Si:H segments filled with InP nanowires. As a control, the device prior to the InP nanowire growth was also evaluated. The photocurrent collected from the control (i.e., the one without InP nanowires) was approximately 0.5 nA at all bias voltages with the highest illumination level, which was approximately three orders of magnitude smaller than those obtained from the device with InP nanowires, suggesting the presence of negligible leak current in the structure without InP nanowires. In Fig. 7(b), a set of data points in different colors at a specific incident optical power represents resistivities of the InP nanowires obtained at various bias voltages. As in a metal–semiconductor–metal photoconductor, the resistivity at a specific bias voltage decreases as the incident optical power increases. The resistivities seem to saturate at 9.5×10^{-2} ohm-cm, as the illumination increases, suggesting a finite total volume provided by a limited number of nanowires available for the generation of electron-hole pairs. We also examined the photoresponse under illumination with monochromatic light at 1550 and 780 nm (i.e., below and above the bandgap of bulk InP at 300 K) with a comparable optical power density to that used for the 633-nm illumination to assess the contribution from excess carriers that could have been thermally generated. The photocurrents obtained under the 780-nm illumination are approximately 20 times larger than those measured under the 1550-nm illumination at any given bias voltage and optical power density, which suggests that the contribution from thermally generated carriers to the photocurrent is negligible. Unlike other nanowire-based photodetectors, the response of our nanowire photoconductor was insensitive to the polarization of the incident light. This is presumably because the InP nanowires are randomly oriented.

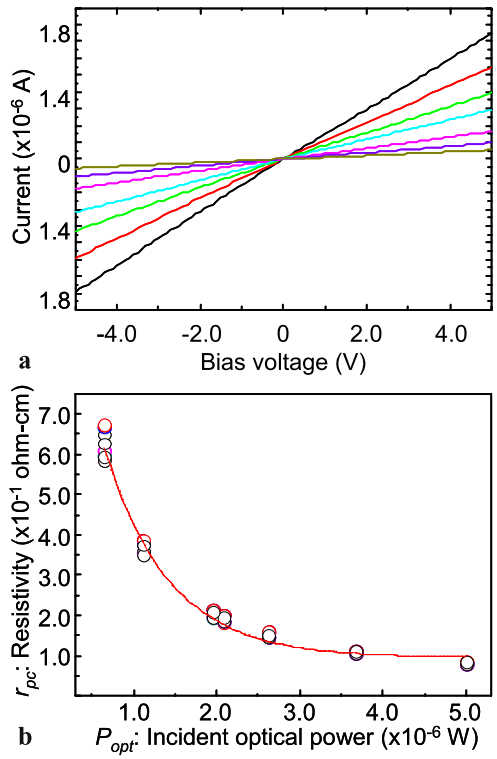

Fig. 7 DC current–voltage (IV) characteristics of the InP nanowire photoconductor are shown in (**a**). Photoresponse shown in (**b**) was obtained by illuminating the device with a laser at 633 nm with varying optical power

6 InP nanowires on a quartz substrate

Figure 8 is an SEM image of InP nanowires on *mc*-Si:H prepared on a quartz substrate. Similar to those seen in Fig. 3(a), all nanowires are randomly oriented. As in Fig. 3(a), two different crystal habits are also identified in Fig. 8, suggesting that two types of nanowires having different lattices coexist. As observed in Fig. 4, the presence of two types of InP nanowires having either *fcc* (*ZB* InP) or *hcp* (*WZ* InP) lattice was confirmed by x-ray diffraction measurements shown in Fig. 9. Diffraction angles for both *ZB* and *WZ* were calculated by assuming that the In-P bond length was the same for both structures. The *ZB* peaks are located very close to those for *WZ*, making it difficult to clearly resolve both signals however, the *ZB*(002) peak at 30.5 degrees confirms that InP

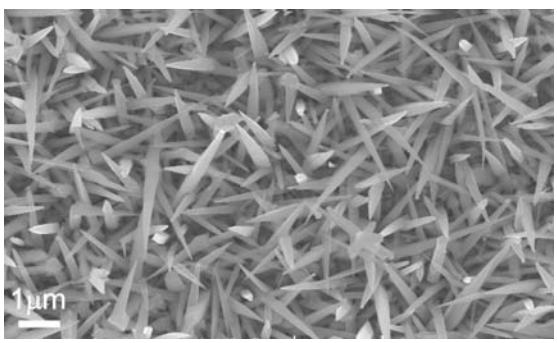

Fig. 8 A representative scanning electron microscopy (SEM) image of randomly oriented InP nanowires grown on *mc*-Si:H template layer on a quartz substrate having both triangular and hexagonal cross sections

nanowires having *fcc* lattice are present. Additional peaks at 24.8, 28.2, and 36.6 degrees are separated from the calculated *ZB* diffraction peaks and confirm that InP nanowires having *hcp* lattice are present as well. Few peaks coincide with InP neither in *fcc* nor in *hcp* lattice, however these peaks not indexed were due to x-rays diffracted from either the sample holder or the quartz substrate. The peak at 28.25 degrees matches well with Si(111) despite the original layer being amorphous. The deposition of InP would have caused the silicon to adopt localized order during the growth as is reported [16]. Overall characteristics are comparable to those seen in Fig. 4.

Raman spectroscopy was also carried out on an ensemble of InP nanowires grown on a 100-nm-thick *mc*-Si:H layer on a quartz substrate as shown in Fig. 10. The measurements were made using a 514-nm laser as an excitation source. Two distinguishable peaks were detected at wavenumber shifts of 298 and 347 cm^{-1}, which closely matched the transverse optical (TO) and longitudinal optical (LO) phonon branches of bulk InP at 298 and 334 cm^{-1} [27] and 303.7 and 345 cm^{-1} [28], respectively. In comparison of Raman shifts between InP bulk and the ensemble of InP nanowires, the slight differences would indicate the contribution (e.g., mode softening due to size effects and large surface to volume ratio) from peculiar features associated with nanowires. Further studies using Raman spectroscopy are currently underway.

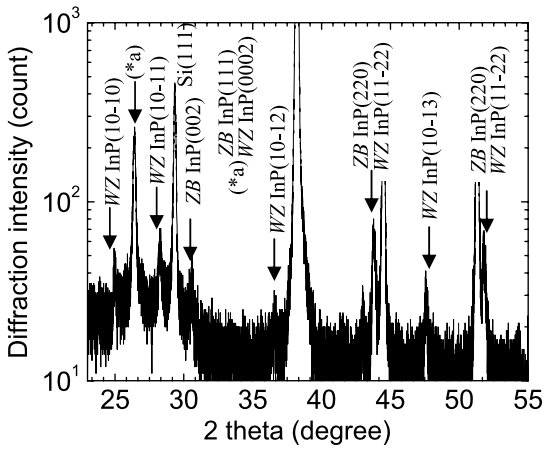

Fig. 9 The XRD profile collected from InP nanowires grown on an *mc*-Si:H template on a quartz substrate shows the presence of *fcc* and *hcp* InP (zincblende and wurtzite, respectively)

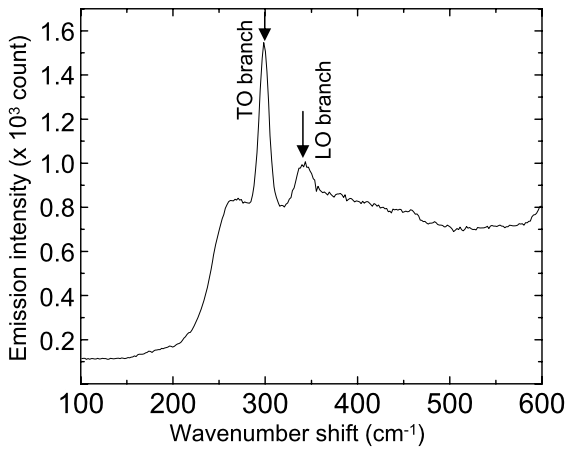

Fig. 10 The Raman spectrum collected from an ensemble of InP nanowires with excitation at 514 nm. The two peaks at wavenumber shifts of 298 and 347 cm^{-1} correspond to TO and LO phonon branches of bulk InP, respectively

7 InP nanowire p-i-n diodes

Nanowire p-n junction diodes with a p-n junctions built into a nanowire have been formed by in-situ doping during nanowire growth [29, 30] or assembled by crossing a p-type and an n-type nanowire [31]. We fabricated a novel p-i-n diode by having randomly oriented InP nanowires bridge p-type and n-type *mc*-Si:H prepared on a quartz substrate [32]. The structure of the p-i-n diode is schematically depicted in Fig. 11. First, a bottom ohmic contact was formed on a quartz substrate. A stack of n-type *mc*-Si:H, amorphous SiO_x insulator, and p-type *mc*-Si:H (500/300/500 nm) was deposited by plasma-enhanced chemical vapor deposition. The SiO_x insulator prevents electrical shorting between the n-type and p-type *mc*-Si:H layers. Short-range atomic order present on the surface of the *mc*-Si:H layers provides epitaxial information for nanowire nucleation and growth, while their high doping level ensures that ohmic contacts are formed with low contact resistance. Subsequently, the top ohmic contact was patterned. Using the top ohmic contact as a self-aligned hard mask, a circular mesa was formed

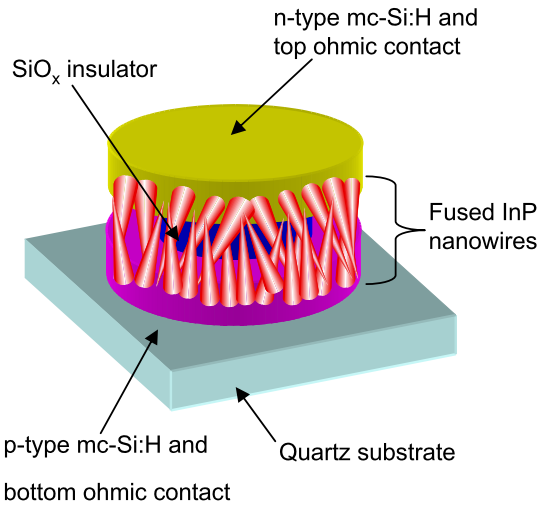

Fig. 11 Schematic shows a p-i-n diode employing randomly oriented InP nanowires prepared on a quartz substrate

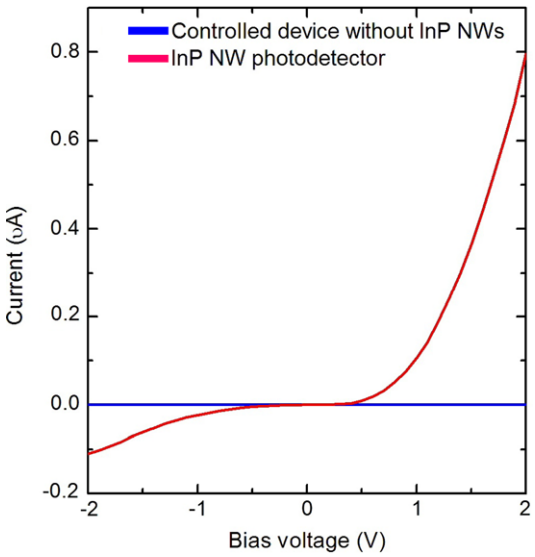

Fig. 12 DC current–voltage measurements were performed on the InP nanowire pin-diode at room temperature (*red curve*). Prior to the nanowire growth, a control device without InP nanowires was tested (*blue curve*)

by etching the top n-type *mc*-Si:H layer, the SiO_x insulator, and the bottom p-type *mc*-Si:H layer. Then, the wafer was covered with a blanket SiO_x layer, and then the SiO_x layer was etched to expose only the side wall of the mesa. Colloidal gold nanoparticles (diameter ∼10 nm) were applied onto the processed wafer and naturally collected along the sidewall of the etched mesa. Unintentionally doped InP nanowires were grown on the exposed sidewalls of the n-type and p-type *mc*-Si:H layers After nanowire growth, the blanket SiO_x layer was stripped off to access the top and bottom ohmic contacts.

As shown in Fig. 12, DC current–voltage measurements were performed on the InP nanowire p-i-n diode at room temperature. Prior to the nanowire growth step, a control device without InP nanowires was tested. In the control device without InP nanowires, the measured current was in the noise level of the measurement system, suggesting leakage between the top n-type *mc*-Si:H layer and the bottom p-type *mc*-Si:H layer was negligible. Rectifying characteristics were clearly seen in the current–voltage characteristics collected from the InP nanowire p-i-n diodes. By fitting the curve to an exponential function from 0 to 0.5 V, the ideality factor ($n \sim 3.9$) was extracted. Above 0.5 V, the nanowire series resistance (MΩ range) dominated the current–voltage measurements. This may indicate that only a limited number of nanowires are bridging. The reverse leakage current at −1 V bias was ∼25 nA, and reverse breakdown was not observed over the measured range. This demonstrates the feasibility of fabricating an ensemble of high-quality InP nanowires into a diode structure with p- and n-type *mc*-Si:H prepared on a non-single-crystal substrates.

8 Summary

In summary, a new route to grow an ensemble of single-crystal semiconductor nanowires was described. Unlike conventional epitaxial growth of single-crystal semiconductor films, the proposed route for growing semiconductor nanowires does not require a single-crystal semiconductor substrate. On a non-single-crystal substrate, epitaxial information required for nanowires is provided by a template layer prepared on a non-single-crystal substrate. In the particular demonstration described in this paper, doped Si:H was used as a template layer for epitaxial growth of InP nanowires so that an ensemble of InP nanowires were be electrically accessed through the doped Si:H template layer. The InP nanowires grown on a Si:H template layer were found to be single crystal and optically active. Simple photoconductors and p-i-n diodes were fabricated with InP nanowires, and their DC current–voltage characteristics were examined. The photoconductors exhibited very linear current–voltage characteristics. When illuminated, the resistivity of the ensemble of InP nanowire photoconductors decreased as the incident optical intensity that excited the InP nanowires increased. Distinctive rectifying characteristics were obtained from the nanowire p-i-n diodes. The proposed structure that employs an ensemble of semiconductor nanowires appears to be a promising semiconductor platform that does not require an expensive single-crystal substrate and that would be suitable for various optoelectronic devices as demonstrated by the photoconductors and the p-i-n diodes.

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