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Non-Linear Clock for Digitizers*

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ABSTRACT

A digital method for generating pulses whose frequency varies with
time is described. The variation of frequency obtained is stable, con-
trollable and predictable. These pulses used in conjunction with time
or charge digitizers allow measurements over a wider range of time or
energy in a digitizer having memory or buffer store of a limited number
of bits or channels. A mathematical relationship between a non-linear
clock and an equivalent linear clock is given which makes this method
extremely flexible and useful.

Introduction

Many time or charge digitizers operate by charging a capacitor to a voltage proportional to time or energy and linearly discharging the capacitor to a predetermined level[1]. Other digitizers[2,3] compare the capacitor voltage to a linear ramp. Pulses generated during the discharging or capacitor voltage/linear ramp comparison period are counted in a scaler, and the number of pulses is directly proportional to the voltage amplitude stored in the capacitor. In instances where the time interval to be measured is long compared to the clock period, the clock pulses are used for a time base, and the time interval is measured directly. Excellent performance of digitizers is obtained because stable clock and very linear, stable discharge circuits and stable discriminators are readily available.

There are occasions when the count capacity associated with the digitizer is too small for the time or energy range of interest and the resolution required. The use of larger memory size is sometimes too costly. Luckily, the more stringent requirements for high resolution usually occur for lower amplitude voltage pulses which correspond to the shorter time intervals and lower energies. Non-linear digitization techniques can be used where the resolution for lower amplitude pulses is maintained, and the resolution of larger pulses is reduced by compression giving increased measurement range. Voltage controlled oscillators (VCO) or non-linear discharge circuits can be used to perform non-linear digitization. Unfortunately, VCO and non-linear discharge circuits which use analog techniques sacrifice the performance usually obtained in digitizers because of drift, non repeatability and some uncertainty to calculate time or energy directly from the digital results without calibration.

A digital method for generating non-linear clock pulses is described which maintains high resolution for lower amplitude pulses and allows for a larger time and energy range for the same number of bits or channels. The variation of clock frequency is stable, controllable and predictable, and the time or energy being measured can be directly calculated. The characteristics of stable clocks and linear, stable discharge circuits are maintained.

Non-Linear Clock

A system for digitally generating non-linear clock pulses is shown in Fig. 1(A) and the timing diagram for the system is shown in Fig. 1(B).

A Clear pulse resets both counters to zero. As a result the two counters are equal (A = B) and the Comparator output is asserted. When a Gate Control signal turns the Gated Clock on, a pulse increments Counter B and also generates a non-linear clock pulse. The non-linear clock pulse increments Counter A and resets Counter B. Now A and B are unequal and the Comparator output is low. Because Counter A now has a count of one, it requires two gated clock pulses into Counter B before the delayed compare output indicates A equals B. The delay insures proper operation of the system and eliminates race problems due to propagation delays. A second non-linear clock pulse is generated which increments Counter A to a count of two and resets Counter B. The Comparator is again unequal. It now takes three gated clock pulses to generate a third non-linear clock pulse, etc., etc.

The mathematical expression for the non-linear clock pattern generated is:

$$\sum_{i=1}^{n} i = \frac{n(n+1)}{2} \tag{1}$$

where i = 1,2,3, ... n, and $n(n+1)/2$ is the number of gated clock pulses required to produce n non-linear clock pulses (or the number of pulses required by a digitizer using a linear clock). A range compression ratio of $(n+1)/2$ is obtained for the non-linear clock over a linear clock. The count stored in Counter A is the digitized value. In a system such as Lawrence Berkeley Laboratory's Large Scale Digitizer (LSD) System [2,3], the non-linear clock pulses would be directed to a number of digitizers simultaneously.

Figure 2(A) shows another configuration similar to Fig. 1(A) but where Counter A is shifted one bit to the left. The non-linear clock pulses are divided by two before comparison is made of Counters A and B. The timing diagram in Fig. 2(B) is similar to Fig. 1(B) and the explanation is left to the reader.

The mathematical expression for the non-linear clock pattern generated is:

$$\sum_{i=1}^{n} 2i = n(n+1) \tag{2}$$

where $2i = 2,4,6, \ldots . 2n$ and $n(n+1)$ is the number of gated clock pulses required to produce $2 \times n$ non-linear clock pulses. The compression ratio is $(n+1)/2$ for $2 \times n$ non-linear clock pulses.

Figures 3(A) and 3(B) show another configuration where Counter B is shifted one bit to the left as opposed to the configuration in Fig. 1(A).

The mathematical expression for the non-linear clock pattern is:

$$\sum_{i=1}^{n} (2i-1) = n^2 \tag{3}$$

where $(2i-1) = 1,3,5,7, \ldots . (2n-1)$, and n^2 is the number of gated clock pulses required to produce n non-linear clock pulses. The compression ratio is n.

Figures 4, 5 and 6 show other configurations which generate additional patterns of non-linear clock pulses.

The mathematical expression for Figs. 4, 5 and 6, respectively, are:

$$\sum_{i=1}^{n} 4i = 2n(n+1) , \tag{4}$$

$$\sum_{i=1}^{n} [4(i-1)+1] = n(2n-1) \text{ and} \tag{5}$$

$$\sum_{i=1}^{n} 2(2i-1) = 2n^2 . \tag{6}$$

General Equation

The general equation for a system consisting of a comparator and counters arranged in a manner similar to any of those in Figs. 1 through 6 is:

$$\sum_{i=1}^{n} a[b(i-1)+1] = an[\frac{b}{2}(n-1)+1] \tag{7}$$

where a = division factor for Counter A, and b = division factor for Coun-
ter B. The expression [b(i-1)+1] obtains the spacing between pulses for
any given value of i for the range i = 1,2,3, ... n, and a is the num-
ber of times the pulse spacing is repeated for value i. The expression
an[$\frac{b}{2}$(n-1)+1] derives the number of gated linear clock pulses required to
produce a x n non-linear clock pulses. Values for a and b for the con-
figurations in Figs. 1 through 6 are indicated in each figure. The com-
pression ratio is [$\frac{b}{2}$(n-1)+1] for a x n non-linear clock pulses.

From the general equation above, a number of pulse train patterns
can be tailored to meet measurement range and resolution requirements for
a limited size of memory, dataway or buffer store. Table I tabulates the
number of linear clock pulses required for a x n non-linear clock pulses
for some values of a and b. Figure 7 plots the results of Table I and
suggests how the shapes of the curves can be manipulated by the appro-
priate choice of coefficients a and b. Coefficient b greatly influences
the slope of the curves by determining the spacing between pulses while
coefficient a dictates the number of times pulses are repeated at a given
pulse spacing.

Although the examples shown in Figs. 1 through 7 show the coefficients
a and b being manipulated in a binary (1,2,4,8, . . .) manner, the co-
efficients a and b can be any integer desired with appropriate circuit
modifications.

Equivalent Linear Clock Determination

It is usually convenient to convert the non-linear clock number (NLC)
into its equivalent linear clock number (LC) before one tackles the task
of analyzing data.

If one takes the equation:

$$\frac{NLC}{a} = n + R ,\tag{8}$$

one can determine n and the remainder (R). By examining Eq. (7) one can
derive an expression for calculating the equivalent linear clock number
which is:

$$LC = an[\frac{b}{2}(n-1)+1] + aR[bn+1],\tag{9}$$

where aR[bn+1] = aR[b({n+1}-1)+1] is derived from the expression on the left hand side of Eq. (7).

Let us take an example. Let NLC=500, a=64 and b=1. What is LC? From Eq. (8) n and R are determined by:

$$\frac{NLC}{a} = \frac{500}{64} = 7.8125 , \tag{10}$$

where n=7 and R=0.8125, and substituting into Eq. (9) we get:

$$LC = 64 \times 7[\frac{1}{2}(7-1)+1] + 64 \times 0.8125[1 \times 7+1] = 2208 \tag{11}$$

Let us take another example where NLC=400, a=512 and b=2. What is LC?

$$\frac{NLC}{a} = \frac{400}{512} = 0.78125 , \tag{12}$$

where n=0 and R=0.78125, and substituting into Eq. (9) we get:

$$LC = 512 \times 0[\frac{2}{2}(0-1)+1] + 512 \times 0.78125[2 \times 0+1] = 400. \tag{13}$$

One can verify the results by examining Fig. 7

Logarithmic Clock

It is easy to see that other devices might be substituted for Counter A to derive different patterns of pulses which one may wish to generate in special cases. A reversible scaler, programmable read-only memory (PROM) and shift register are a few such devices which may be substituted.

The shift register, when substituted for Counter A, generates a logarithmic pattern. See Fig. 8. The shift-in input to the shift register is held at a logical one. A timing pattern similar to that of Fig. 1(B) is generated. The delayed compare output is asserted when Counter B equals the shift register contents, and a clock pulse is allowed through the "AND" gate. Since the shift register contents progress in a 0, 1, 3, 7, 15, 31 . . . manner, the pattern generated is logarithmic, and the equation for the system is:

$$\sum_{i=1}^{n} 2^{(i-1)} = 2^n - 1 . \tag{14}$$

Again, as in the examples before, more flexibility is gained by placing a divider before the shift register. This allows one to manipulate the non-linear clock vs. linear clock relationship in a manner similar to that shown in Table I and Fig. 7. The equation for this relationship is:

$$\sum_{i=1}^{n} a[2^{(i-1)}] = a[2^n-1] \tag{15}$$

where a = division factor of divider placed before the shift register. The shape of the curves relating non-linear clock pulses to linear clock pulses (as in Fig. 7) is logarithmic, and the coefficient a is chosen to fit the time or energy range into the capacity of the memory, dataway or buffer. The generation of a table and plot can easily be done by following the example of Table I and Fig. 7, and the exercise is left to the reader.

Drawing from the past examples [Eqs. (8) through (13)], the equivalent linear clock number (LC_1) can be determined from the logarithmic clock count. First, n and R are determined from Eq. (8). Then n and R are substituted into the following equation:

$$LC_1 = a[2^n-1] + aR[2^n], \tag{16}$$

which is derived by examination of Eq. (15).

The usefulness of a logarithmic clock does not require any elaboration.

Conclusions

A flexible, predictable and controllable pattern of non-linear pulse trains can be generated by a digital method. The pulses generated can be made as stable as any linear clock. Because a digital method is used for producing the clock pulses, digitizers can maintain their very linear and stable characteristics. From a general equation one can tailor a configuration of comparator and counters and/or other devices to give reasonable resolution and increased time or energy range for any given memory or dataway size. A precise, mathematical relationship between a non-linear clock and a linear clock is given which allows one to compute results directly from the non-linear clock information.

Acknowledgements

References

1) D. Wilkinson, "A Stable Ninety-nine Channel Pulse Amplitude Analyzer for Slow Counting", Proc. Cambridge Phil. Soc., (1950) 508.

2) R. F. Althaus, F. A. Kirsten, K. L. Lee, S. R. Olson, and L. J. Wagner, IEEE Trans. Nucl. Sci. NS-24 (1977) 408.

3) R. F. Althaus, K. L. Lee, F. A. Kirsten, and L. J. Wagner, IEEE Trans. Nucl. Sci. NS-24 (1977) 218.

Figure Captions

Fig. 1   Non-linear clock pulse train generator

       (A) Circuit configuration

       (B) Timing diagram

Fig. 2   Non-linear clock - Counter A divides by two

       (A) Circuit configuration

       (B) Timing diagram

Fig. 3   Non-linear clock - Counter B divides by two

       (A) Circuit configuration

       (B) Timing diagram

Fig. 4   Non-linear clock - Counter A divides by four

Fig. 5   Non-linear clock - Counter B divides by four

Fig. 6   Non-linear clock - Both Counters A and B divide by two

Fig. 7   Plot of non-linear clock pulses vs. linear clock pulses.

Fig. 8   Logarithmic clock generator

FIGURE I
XBL 783-7534

(A)
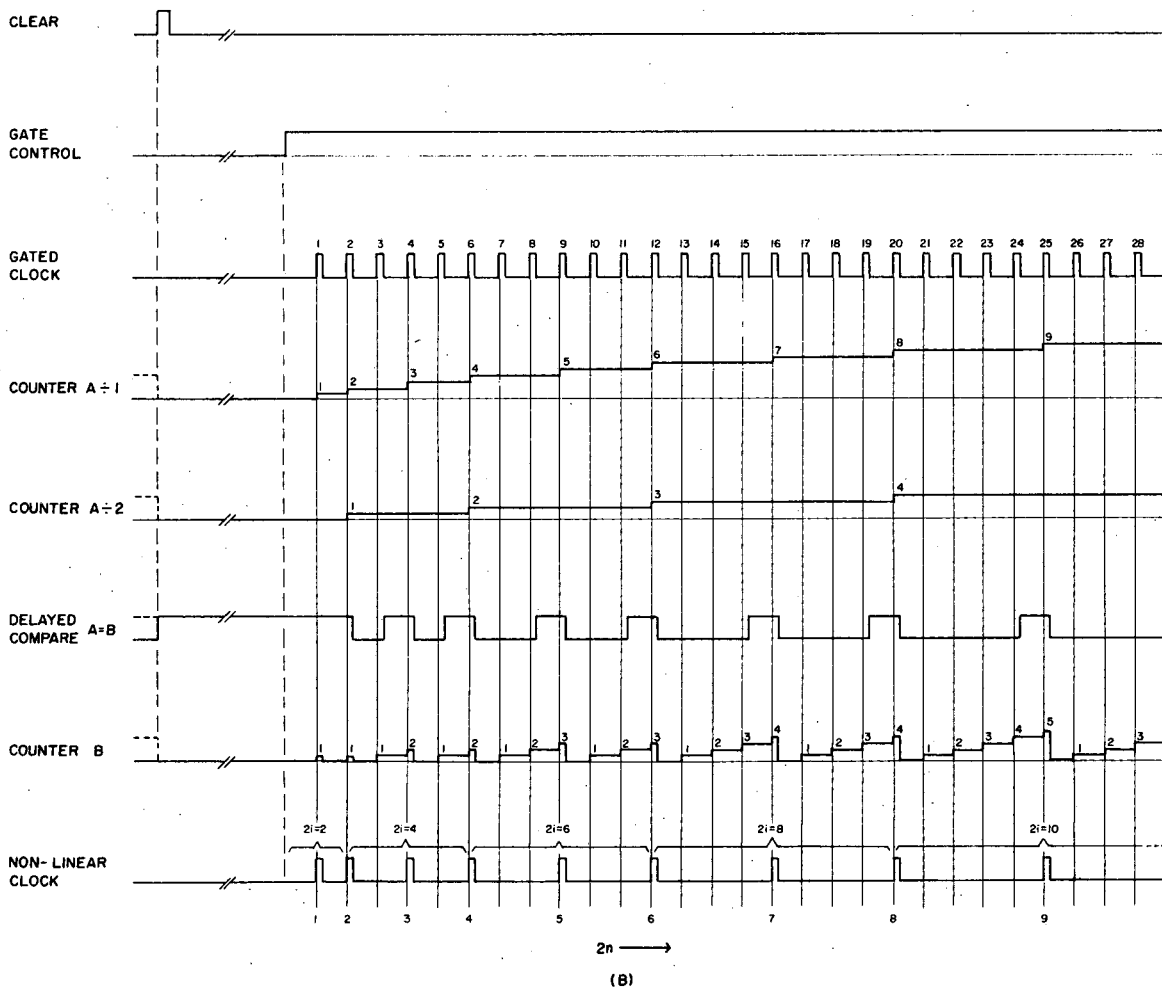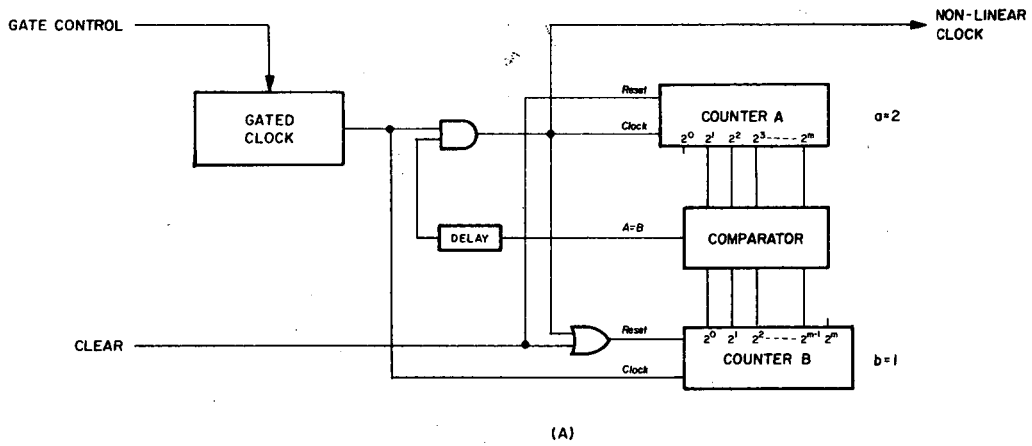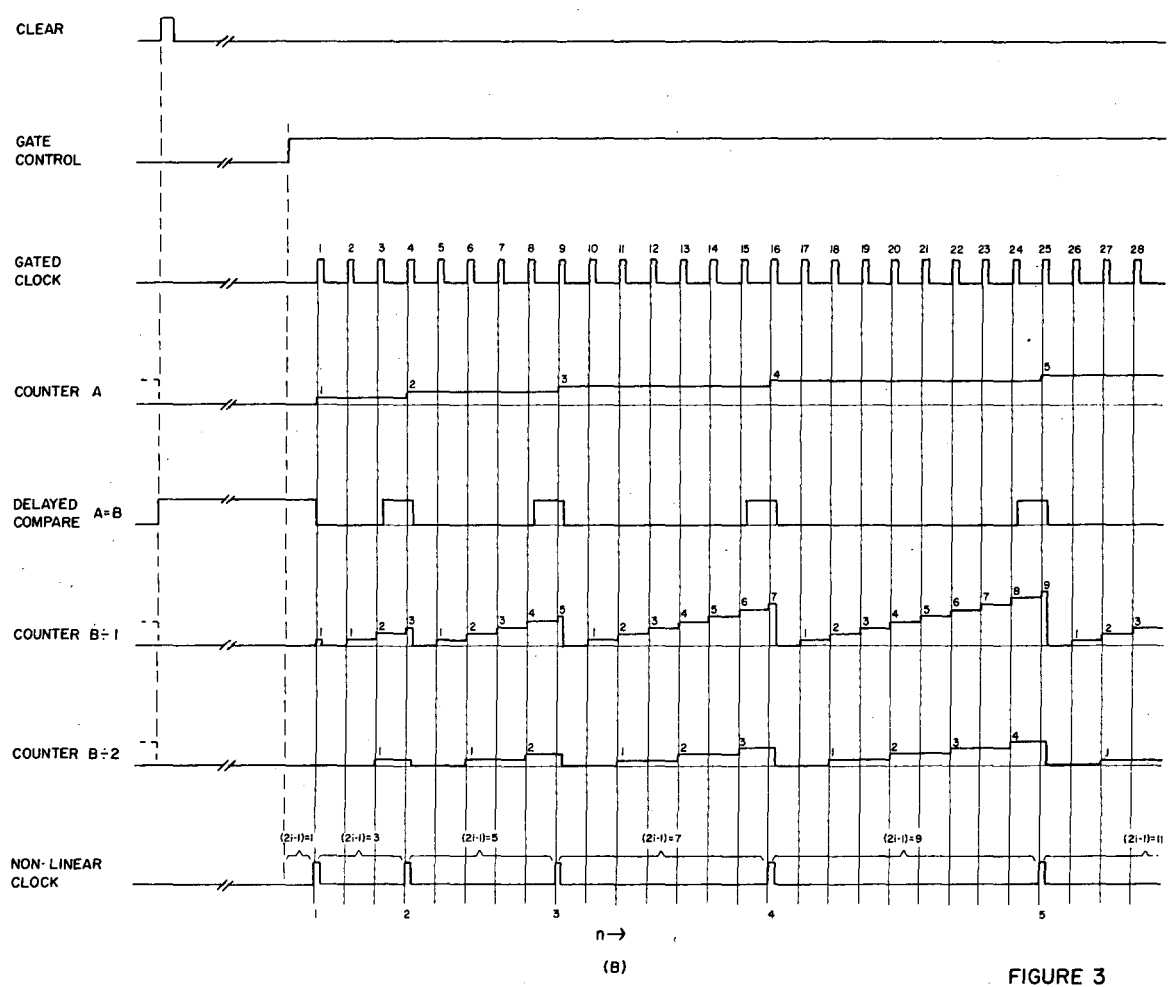
(B)
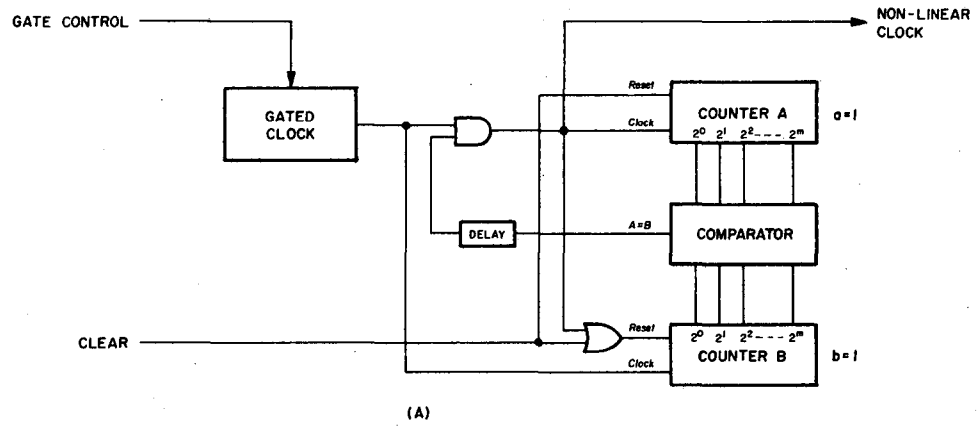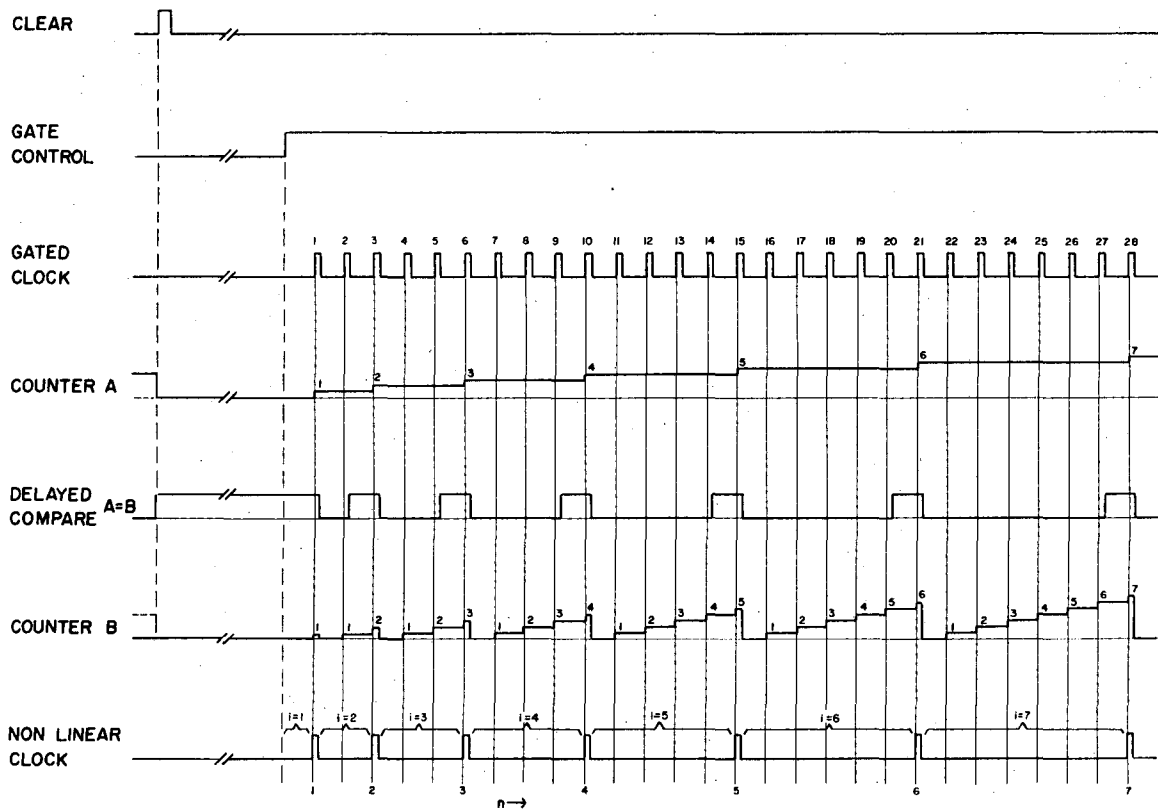
FIGURE 2
XBL 783-7532
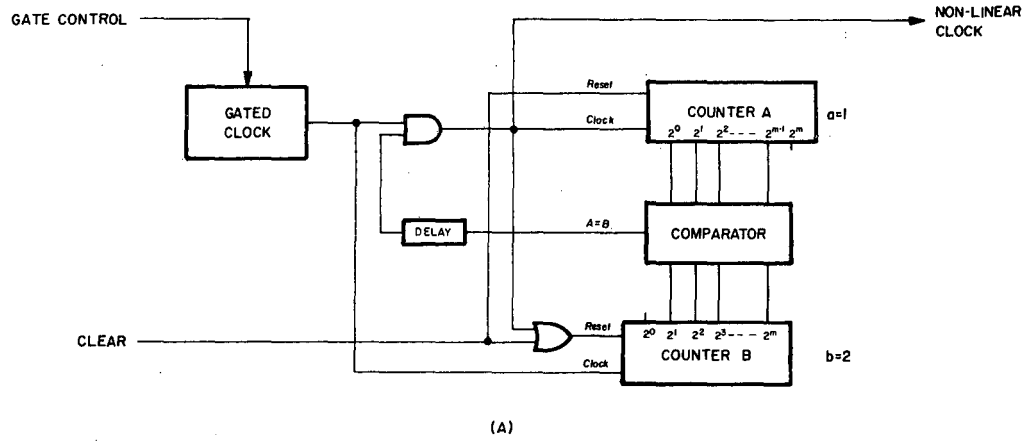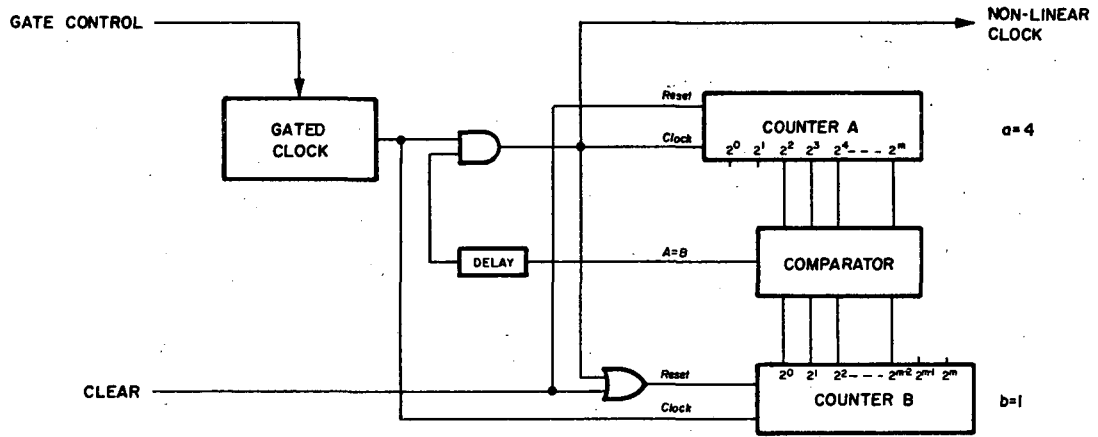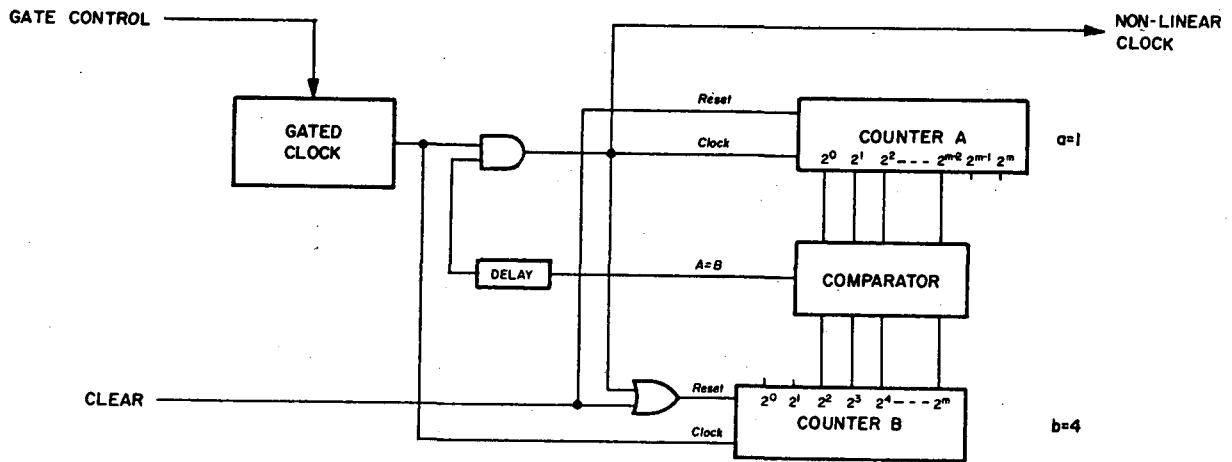
FIGURE 3
XBL 783-7533

XBL 783-7530

Fig 4

XBL 783-7531
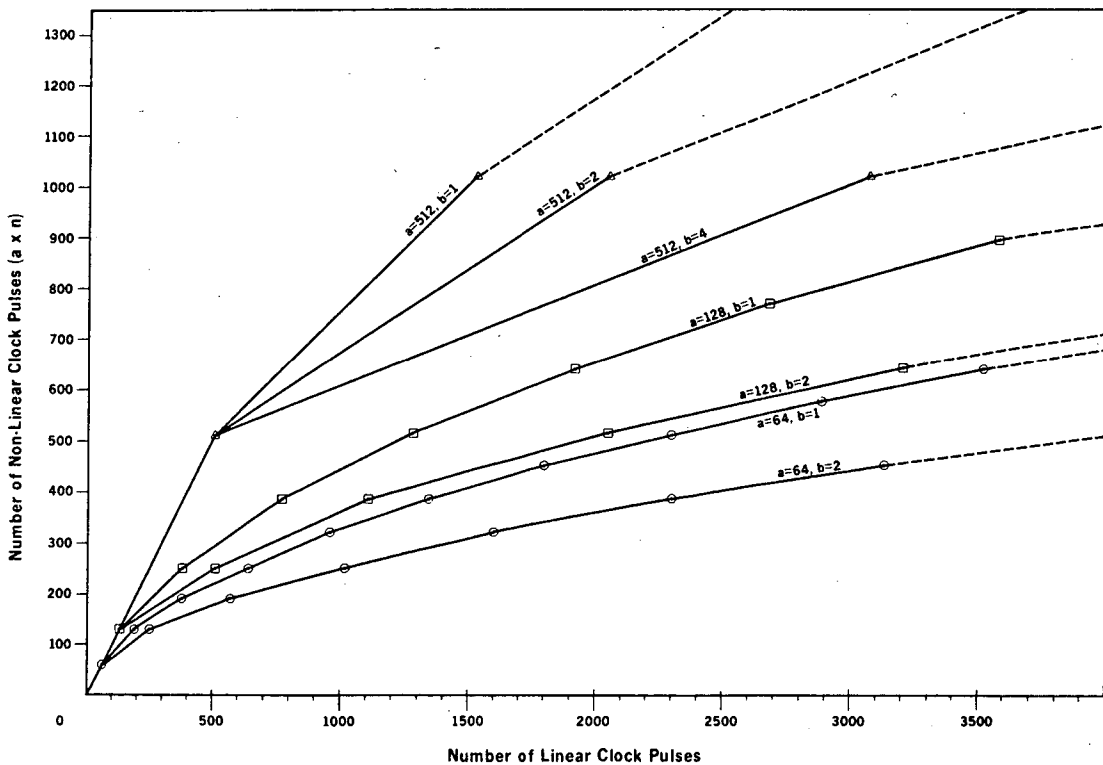
Fig 5
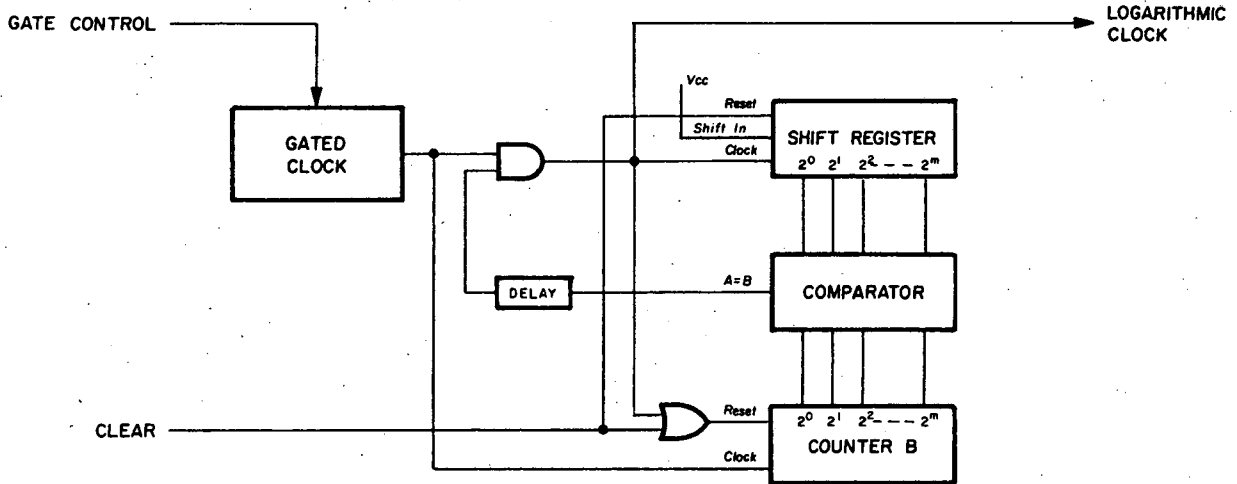
XBL 783-7529

Fig 6

XBL 784-8024

Fig 7

XBL 783-7528

Fig 8

TABLE I

NON-LINEAR CLOCK PULSES VS. LINEAR CLOCK PULSES FOR COFFICIENTS a AND b

n	a = 64			a = 128			a = 512			
	No. of Non-Linear Clock Pulses	Number of Linear Clock Pulses		No. of Non-Linear Clock Pulses	Number of Linear Clock Pulses		No. of Non-Linear Clock Pulses	Number of Linear Clock Pulses		
	(a x n)	b=1	b=2	(a x n)	b=1	b=2	(a x n)	b=1	b=2	b=4
1	64	64	64	128	128	128	512	512	512	512
2	128	192	256	256	384	512	1024	1536	2048	3072
3	192	384	576	384	768	1152	1536	3072	4608	7680
4	256	640	1024	512	1280	2048	2048	5120	8192	
5	320	960	1600	640	1920	3200				
6	384	1344	2304	768	2688	4608				
7	448	1792	3136	896	3584					
8	512	2304	4096							
9	576	2880								
10	640	3520								
11	704	4224								